Power-Efficient Reconfigurable Baseband Processor

The traditional ASIC approach to baseband processing is limited in flexibility and die size usage efficiency for multiple standards. A reconfigurable baseband processor (part of the scalable communication core) promises to reduce size of and increase flexibility for baseband processors running multiple standards.

 ✓ Enables development of new protocols in the high-level language (DPL) with a full set of software tools

- ✓ Uses reconfigurable engine
- ✓ Power efficiency

✓ Reduced time-to-market for implementation of new protocols

✓ Reduced footprint over the sum of single protocol ASIC solutions for multi-radio case



Generic DPE architecture



- •4GMul/s* and 6GAdd/s* of performance
- Average power consumption < 100mW*</p>
- •Die size 5mm2* at 90nm process
- Easily scalable

*For design running at 266MHz, 1 stream workload with activity factor ~50%, supporting 802.11n/802.16e memory requirements



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SW Tools for FW Development And **Architecture Exploration**

Programming of reconfigurable data-streaming architecture with coarse-grained parallelism is a challenging problem.

802.1¹r

802.16

We provide complete technology including:

✓ Data-Streaming Architecture Programming Model

✓ Retargetable SW **Development Toolkit**

✓ DPL, Data-stream Processing Language

✓ DPE Architecture **Exploration tools**

DPL is a new programming language for datastreaming systems designed specially to support the generic DPE structure.

Single Technology – Multiple Solutions

DPE - Soft IP Core: **Reconfigurable Architecture** & Retargetable Toolkit

Customization for Selected Applications Class



Tools DPE

Multi-Radio **Applications**



Multi-Media **Applications**



Others Datastreaming **Applications**



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New Multi-Radio

Device

WiFi, WiMax

and DVB (SimOp)

DPE based Solution for Multi-Radio Base-Band Processing

Tools

DPE

Firmware (FW)

✓ Algorithms design

Development Process:

 Debugging on DPE Simulator ✓ Load ready FW into DPE

✓ Standards/Specifications analysis

✓ Control/Dataflow partitioning & mapping

✓ FW implementation in DPL/DAsm and C

FW Development

Process