22 nm Device Architecture and Performance Elements

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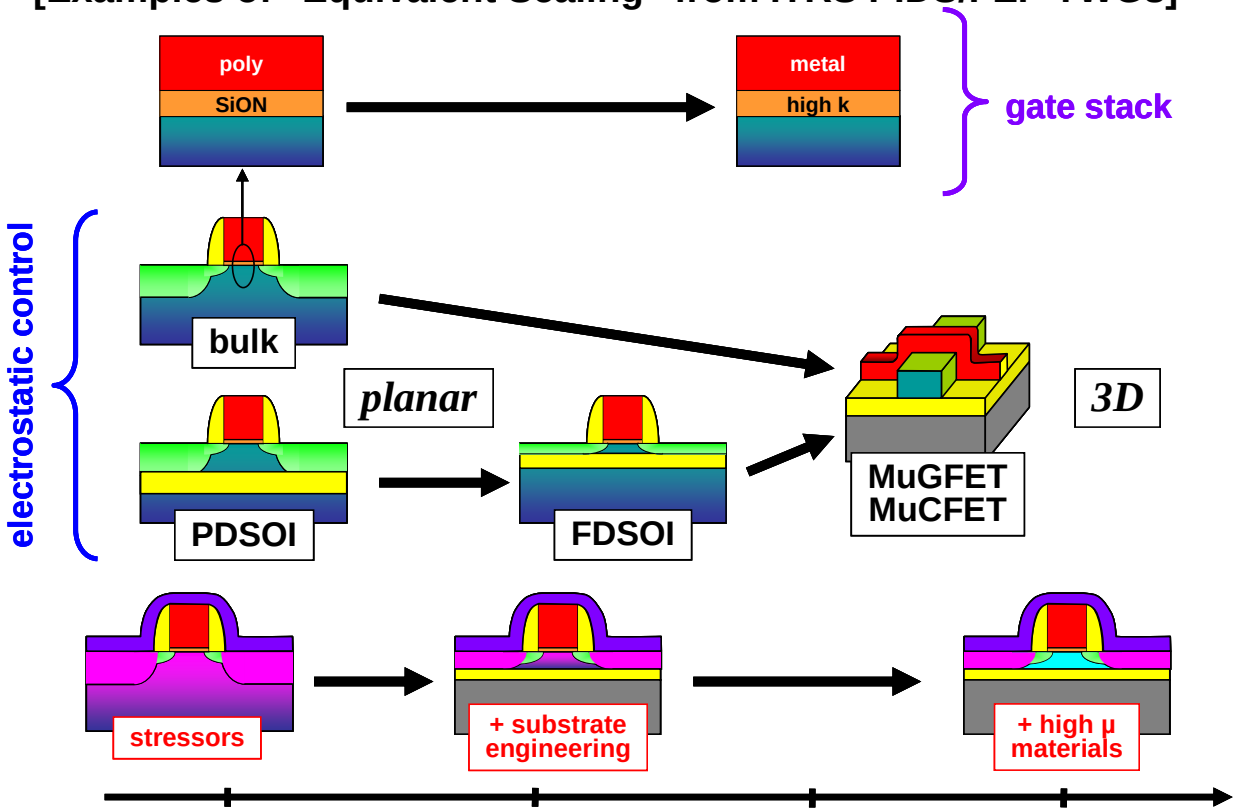
2007 - PIDS/FEP - Simplified Transistor Roadmap

[Examples of "Equivalent Scaling" from ITRS PIDS/FEP TWGs]



[ITRS DRAM/MPU Timing:	2007[7.5]	2010	2013	2016]

Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

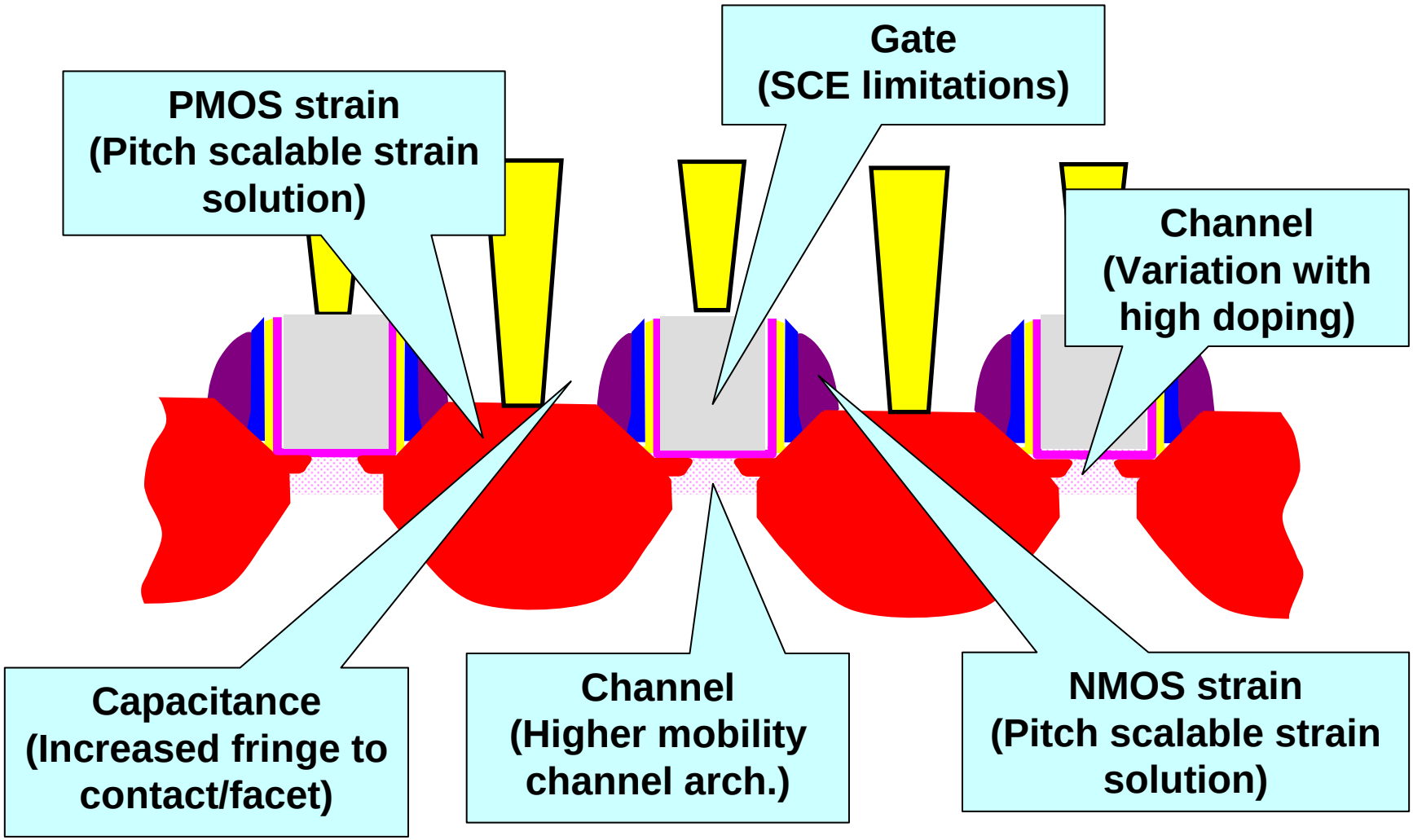
ITRS, Ref [1]

Agenda

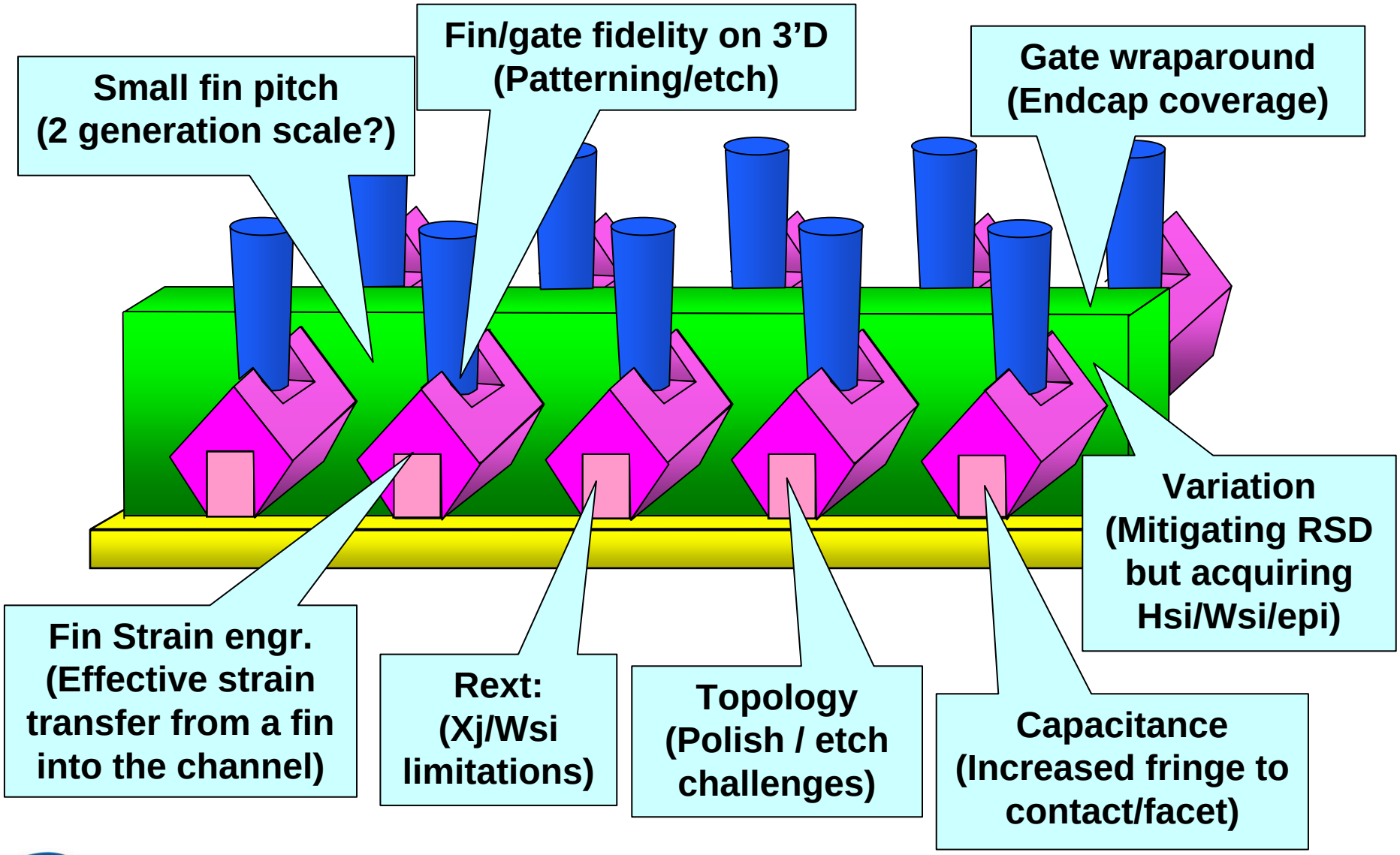
- **Improving Electrostatics**
  - Planar or MuGFET
  - High-k Metal gate
- **Capacitance Challenges**
- **Resistance Challenges**
- **Mobility enhancement**
  - Advanced channel materials
  - Orientation
  - Strain
  - Mobility and electrostatics
- **Summary**

Improving Electrostatics: Planar or MuGFET

Planar Challenges



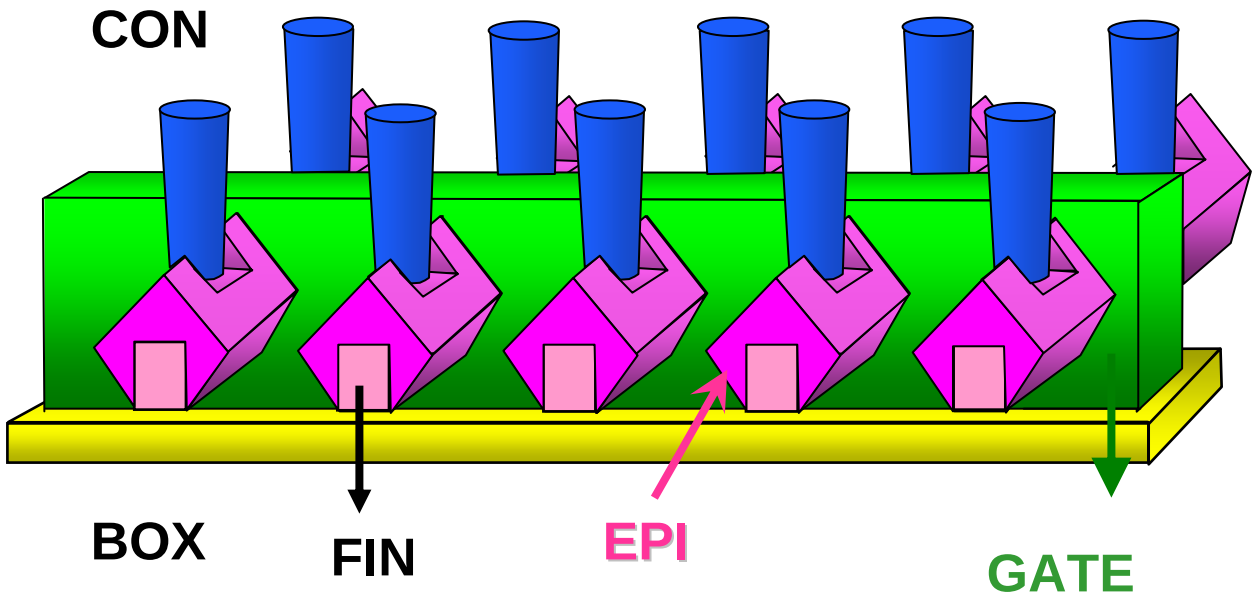
Additional MuGFET Challenges

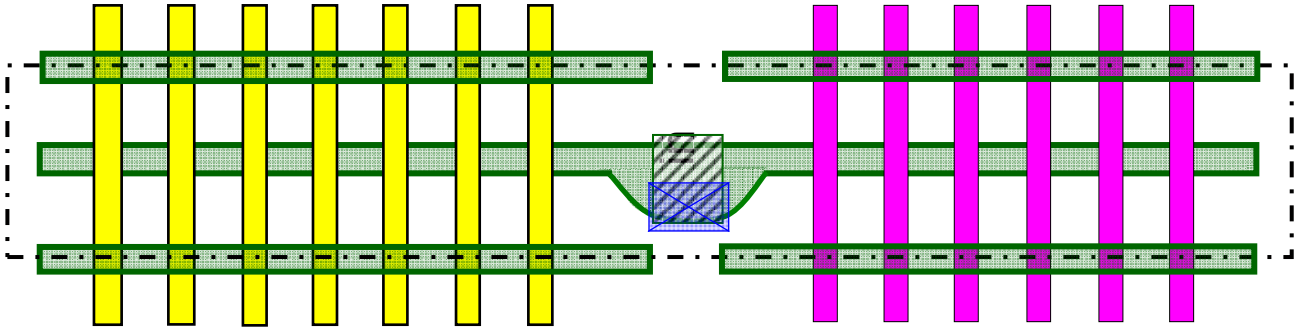


MuGFET vs. Planar Risk-Benefit Summary

	BENEFITS	RISKS
MuGFET	+ Better SCE: ↓Vt + Better performance vs Vcc + Low doping: Improved matching (RDF)	- Very challenging fin patterning - Process challenges with non-planar process - Implementing N and PMOS strain - Very tight process control - High Rext (thin body) - Design challenges with quantization of fins – particularly RF cells
Planar	+ Traditional planar scaling roadmap + Permits advanced strain engineering for both N and PMOS + Traditional litho scaling roadmap	- SCE improvement bottleneck - Reduced S/D area / Rext - Risk of increased variation with scaling - Significant mobility enhancements required for planar 22nm - Increased yield/rel. risks

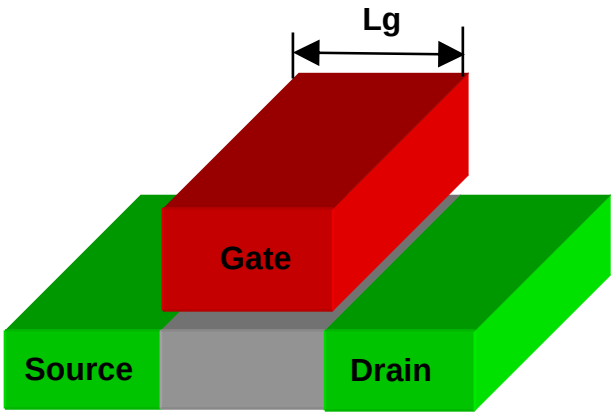
Quantized Diffusion



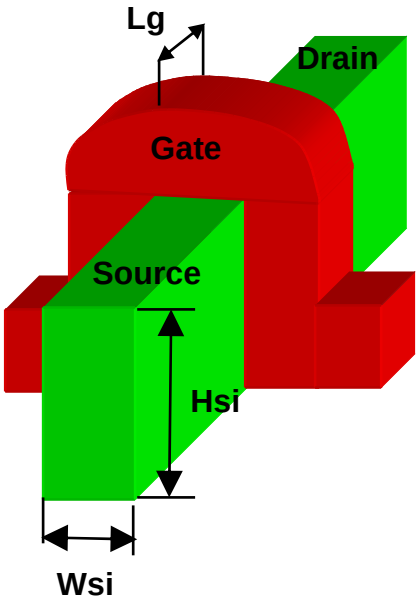


MuGFET INVERTER

Electrostatics Benefit



Conventional Planar FET



MuGFET

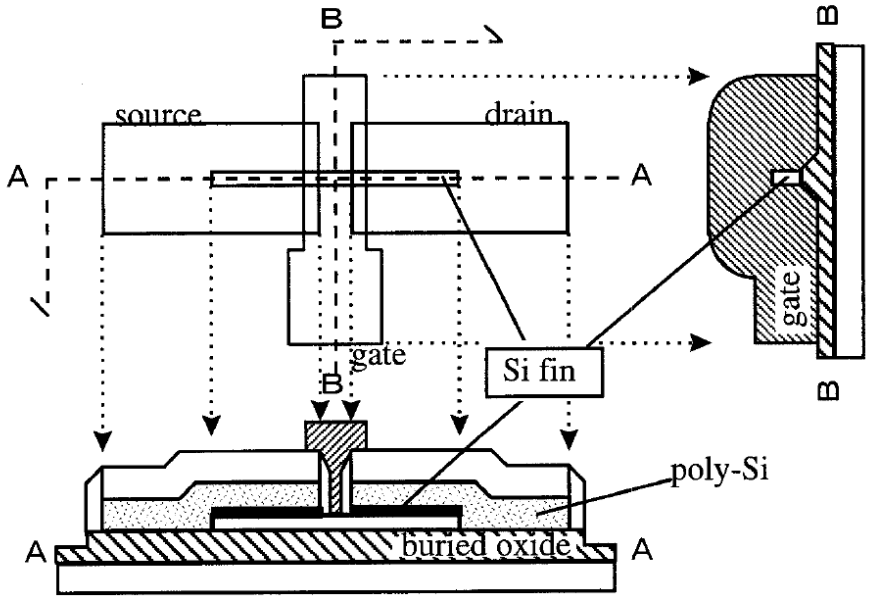
MuGFET electrostatics allows either:

1) Lg Scaling (support smaller Leff at same Ioff)
2) Vg-Vt scaling (support smaller Vt at same Ioff)

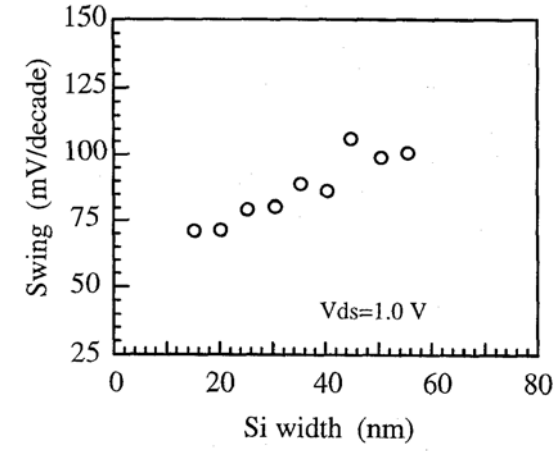
Hisamoto – Hitachi / Berkeley– IEDM 1998 [3]

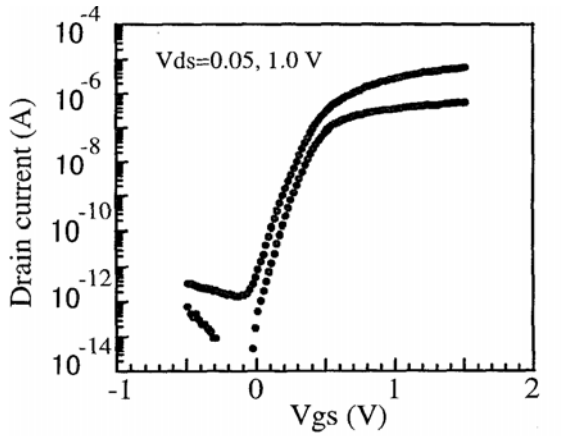
A Folded-channel MOSFET for Deep-sub-tenth Micron Era

Digh Hisamoto, Wen-Chin Lee*, Jakub Kedzierski*, Erik Anderson**, Hideki Takeuchi+,
Kazuya Asano++, Tsu-Jae King*, Jeffrey Bokor*, and Chenming Hu*
Central Research Laboratory, Hitachi Ltd., *) EECS, UC Berkeley,
**) Lawrence Berkeley Laboratory, +) Nippon Steel Corp., ++) NKK Corp.

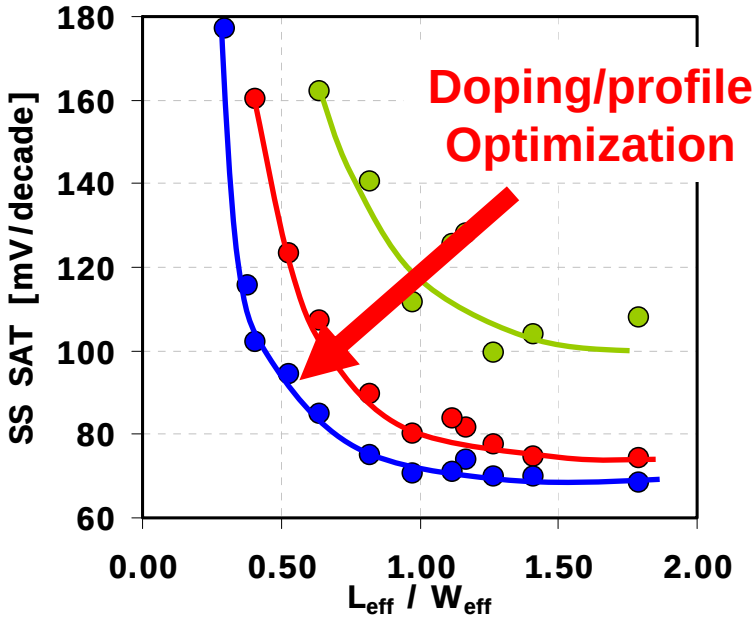


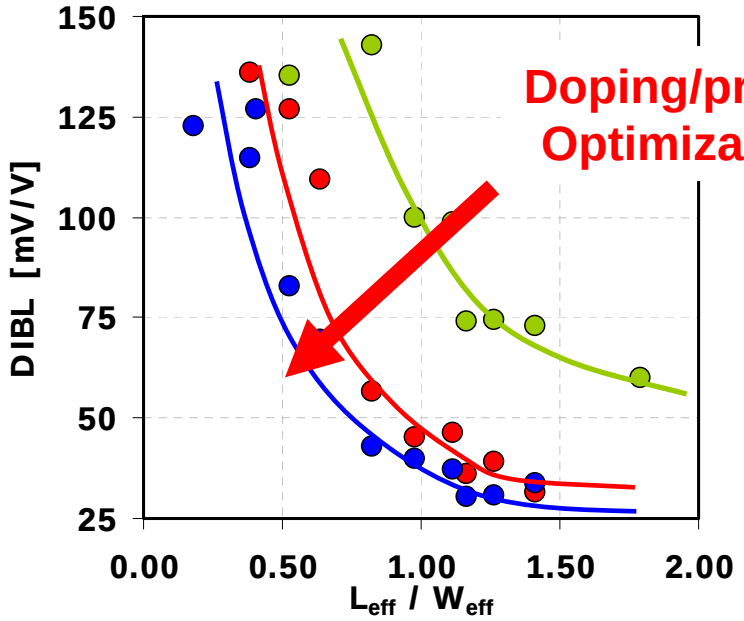
. 1 Folded channel MOSFET layout design and device structure.
: bottom is A-A cross section, and the right is B-B cross section





MuGFET Electrostatics Benefits

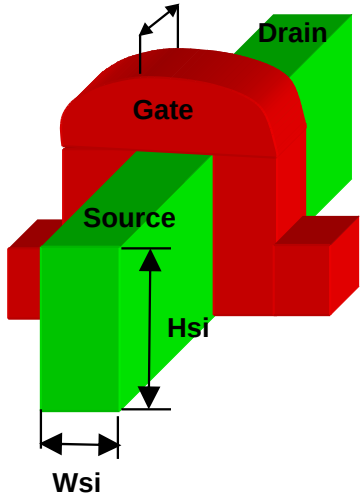




Good news: MuGFET electrostatics strongly depends on the ratio of L_{eff} / W_{eff} as defined by:

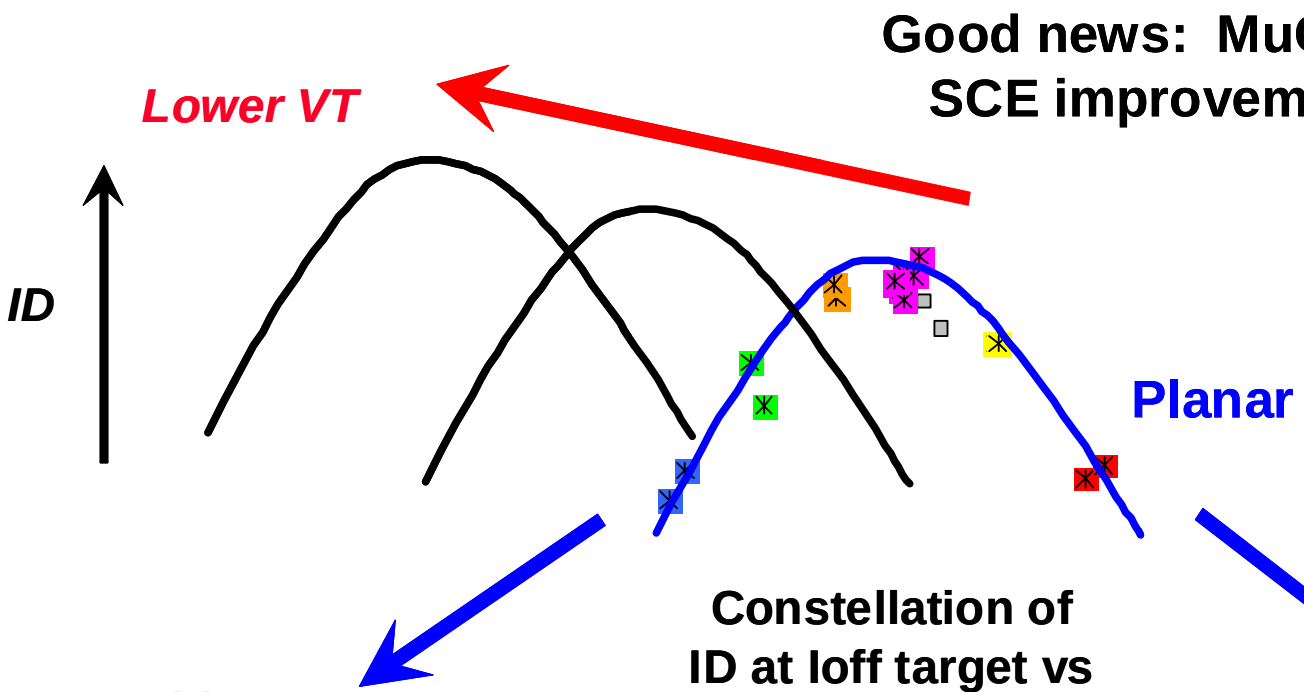
$$L_{eff} = L_G - 2 * X_{UD}$$

$$W_{eff} = W_{Si} + 2(\varepsilon_{Si}/\varepsilon_{OX})*T_{OX}$$



Kavalieros – Intel - VLSI SC 2008 [2]

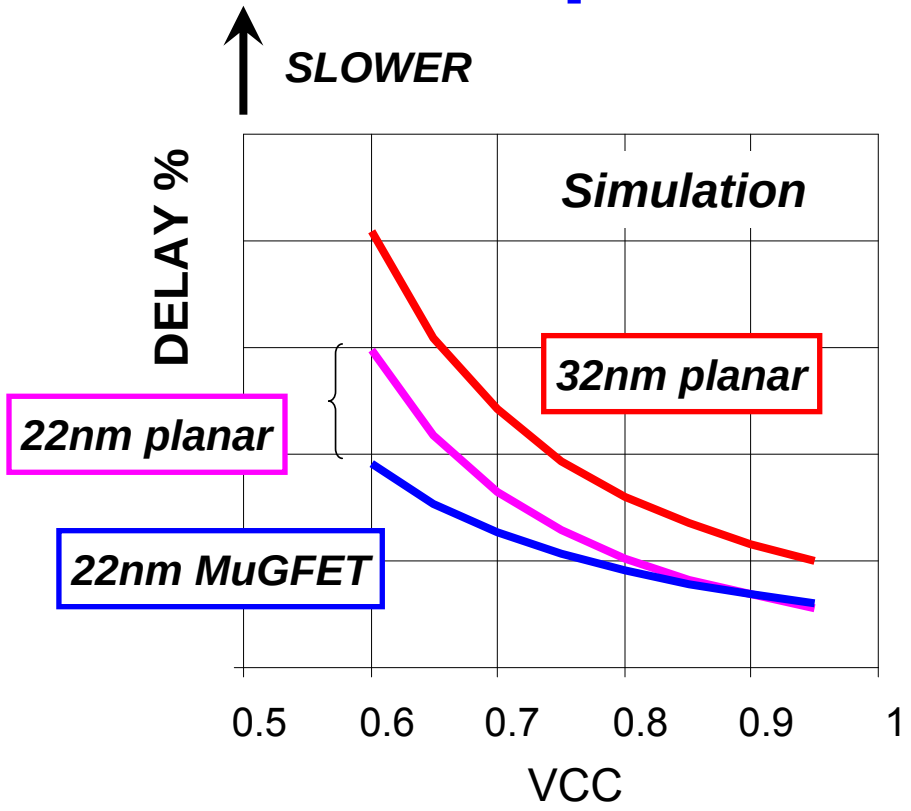
MuGFET Electrostatics Benefits

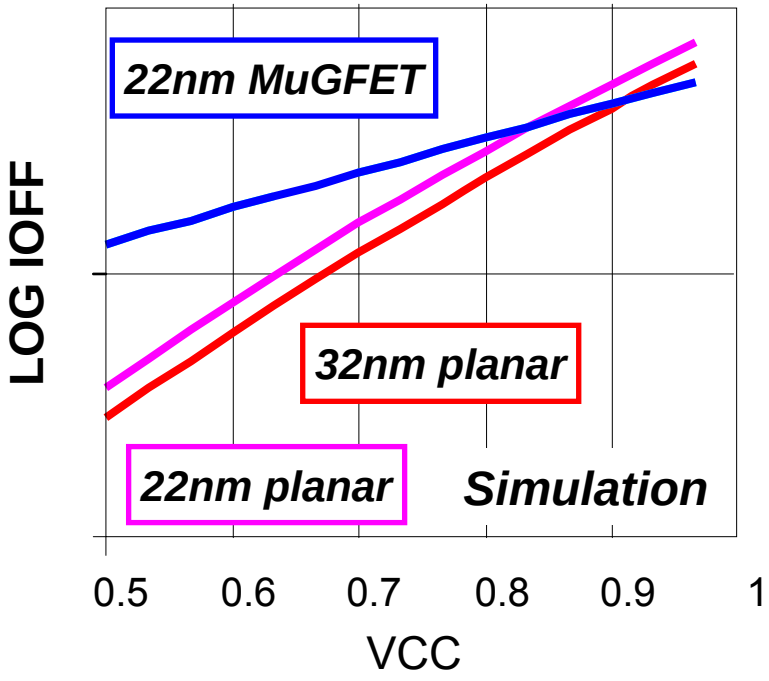


Left side
Long L
SCE roll-off due to low VT
Increase Le to reduce Ioff
Reduced drive due to longer Le

Right side
Short L
SCE roll-off due to short L
Higher doping/VT to reduce Ioff
Reduced drive due to VG-VT

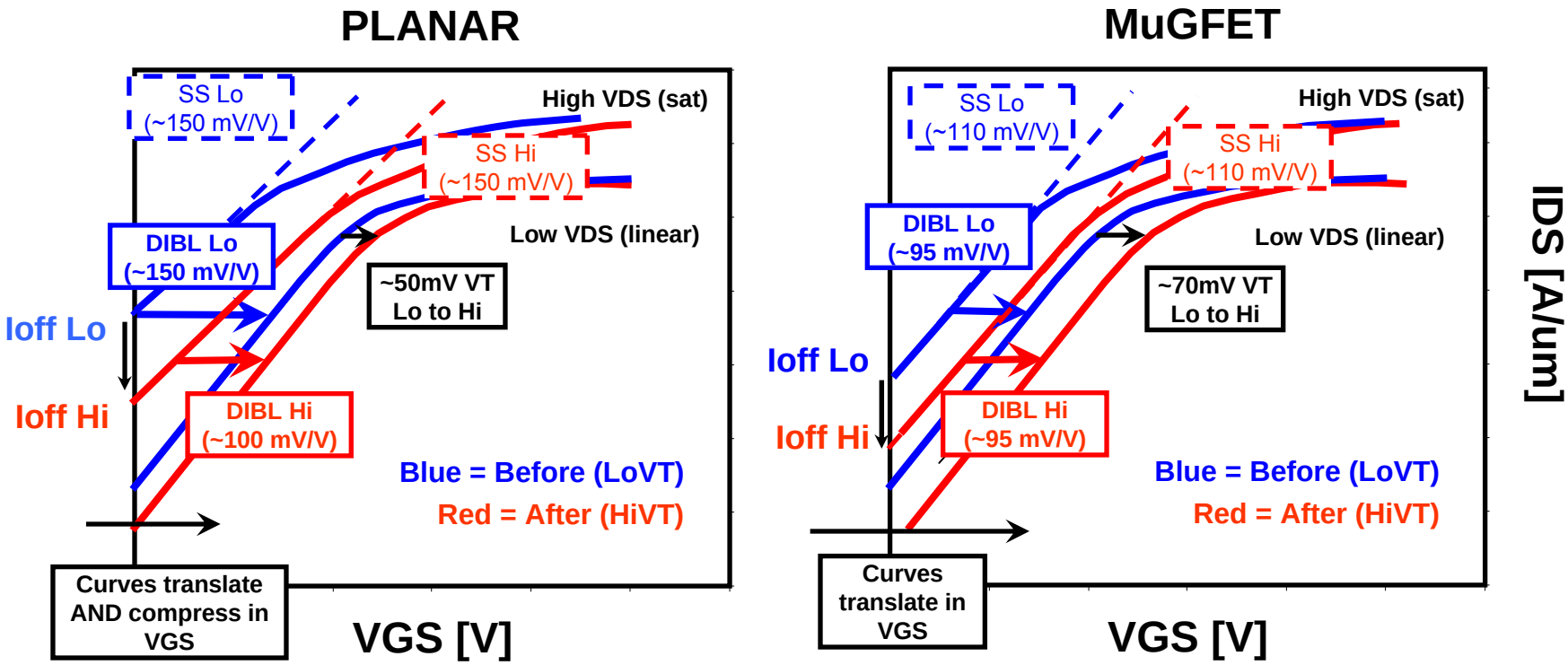
Mixed Blessings of Improved Electrostatics





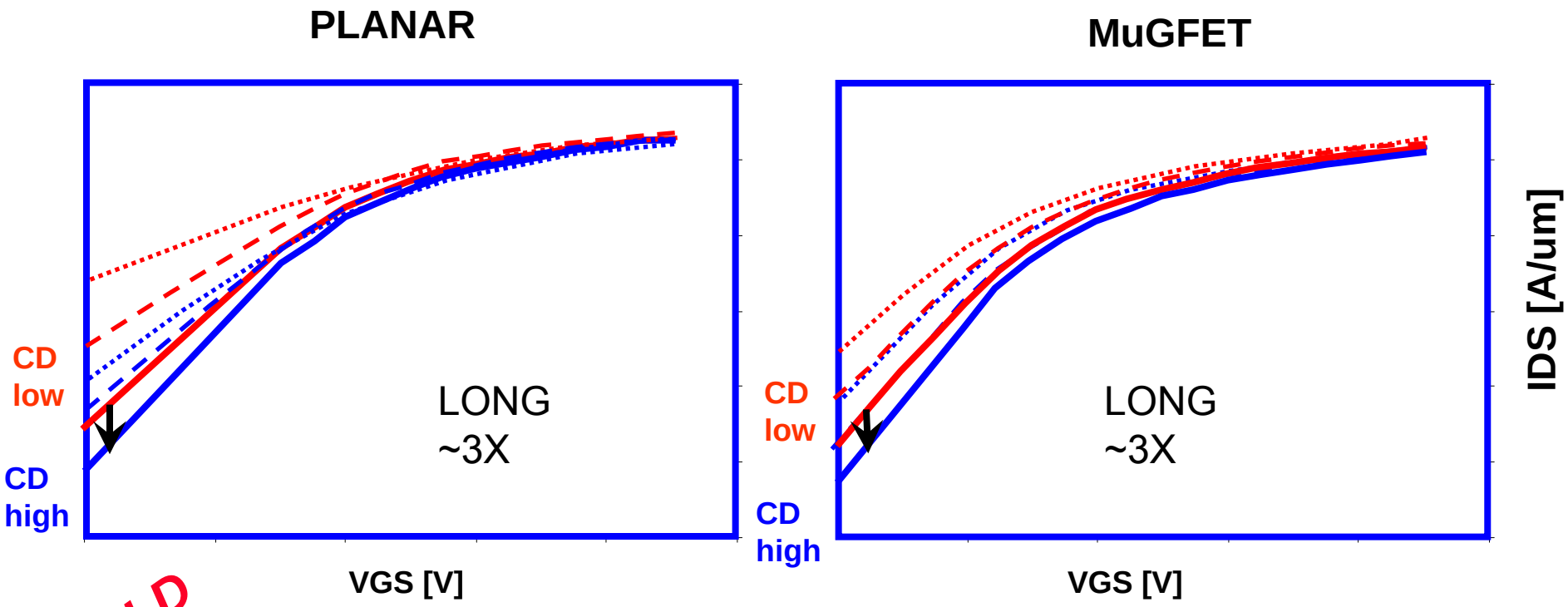
Bad news: Improved voltage scaling (from lower VT) is also associated with increased Ioff (from improved DIBL)

Mixed Blessings of Improved Electrostatics



Bad news: Improved SCE (lower DIBL / SS) means less sensitivity to VT changes. More VT shift is required in low power device options for the same Ioff shift

Mixed Blessings of Improved Electrostatics



PLANAR	
SHORT:	~7X
MEDIUM:	~5X
LONG:	~3X

MuGFET	
SHORT:	~5X
MEDIUM:	~4X
LONG:	~3X

Bad news: Better SCE means less shift in Ioff with CD
Ioff shift with CD is key tool in tailoring low power devices

Improving Electrostatics: High-k Metal Gate

High-k Metal Gate

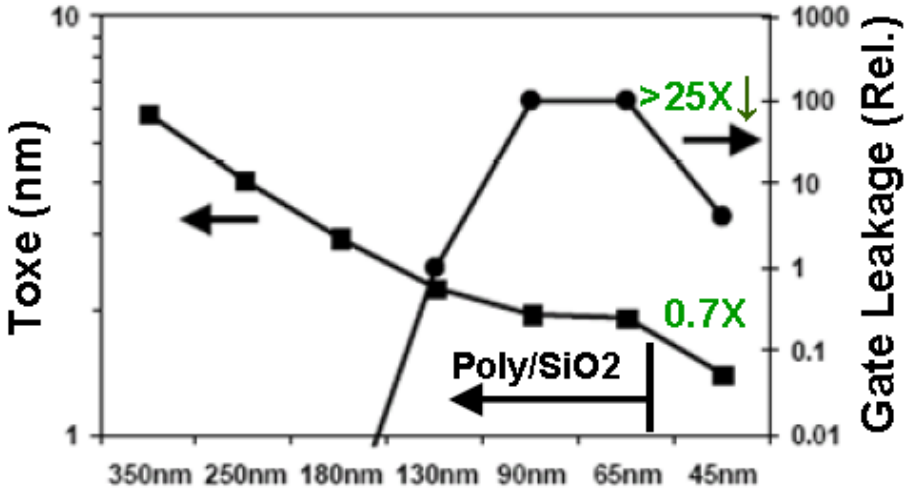
BENEFITS

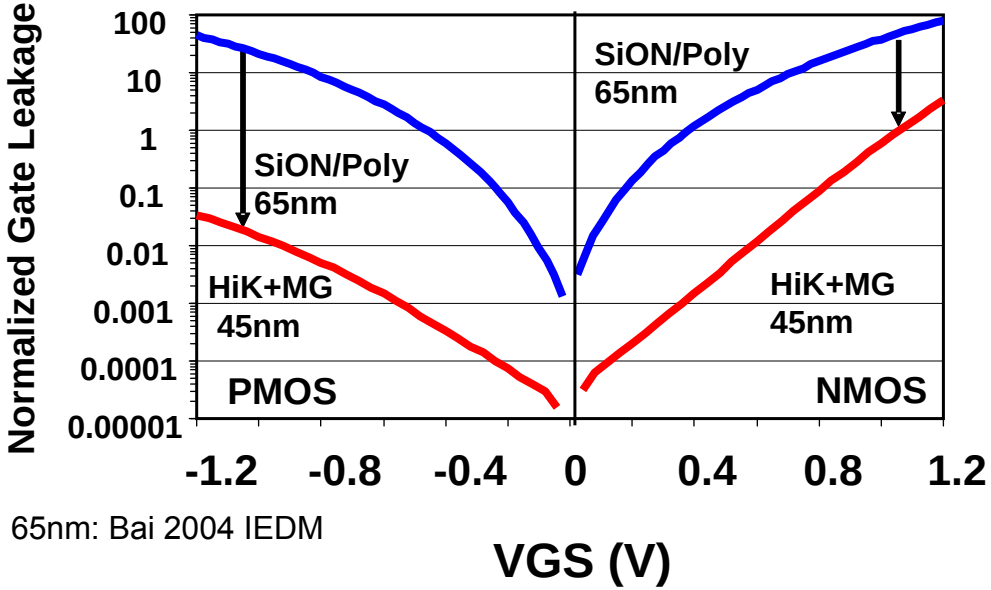
- **High-k gate dielectric**
  - Reduced gate leakage
  - Continued T_{OX} scaling
- **Metal gates**
  - Eliminate polysilicon depletion
  - Resolve V_T pinning for high-k gate dielectrics

CHALLENGES

- **High-k gate dielectric**
  - Reduced reliability
  - Reduced mobility
- **Metal gates**
  - Dual bandedge workfunctions
  - Thermal stability
  - Process integration

High-k Metal Gate: ToxE and Ig





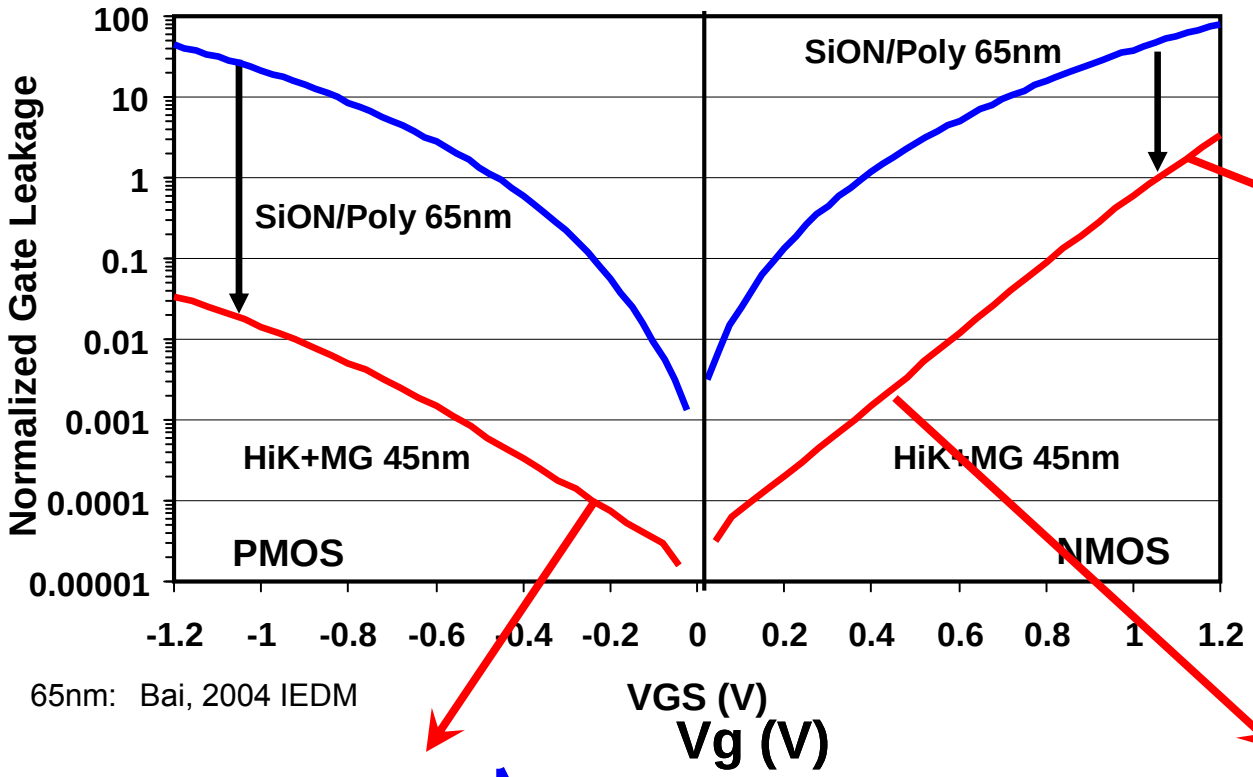
65nm: Bai 2004 IEDM

High-k/MG enables 0.7X ToxE scaling while reducing Ig > 25X at 45nm node

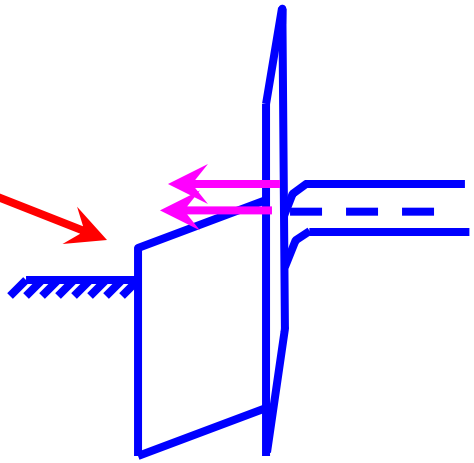
Gate leakage is reduced >25X for NMOS and 1000X for PMOS

Mistry - Intel - IEDM 2007 [4]

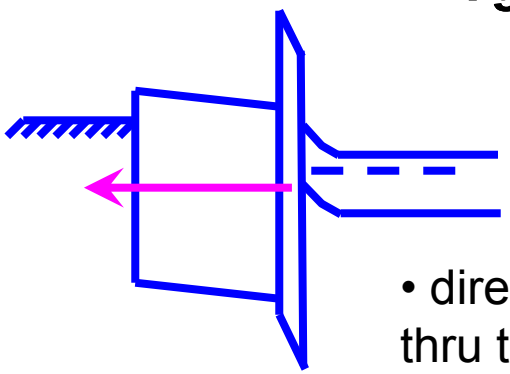
Igate properties of HiK-MG



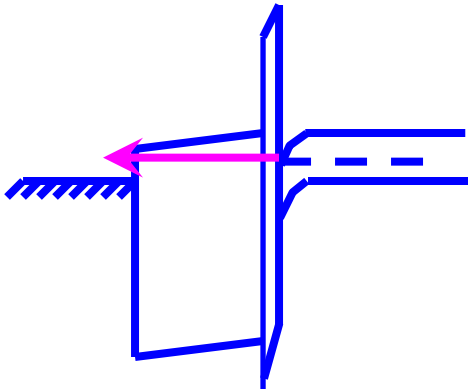
65nm: Bai, 2004 IEDM



• FN thru SiO2 + FP/direct thru High-k



• direct tunneling thru thick High-k

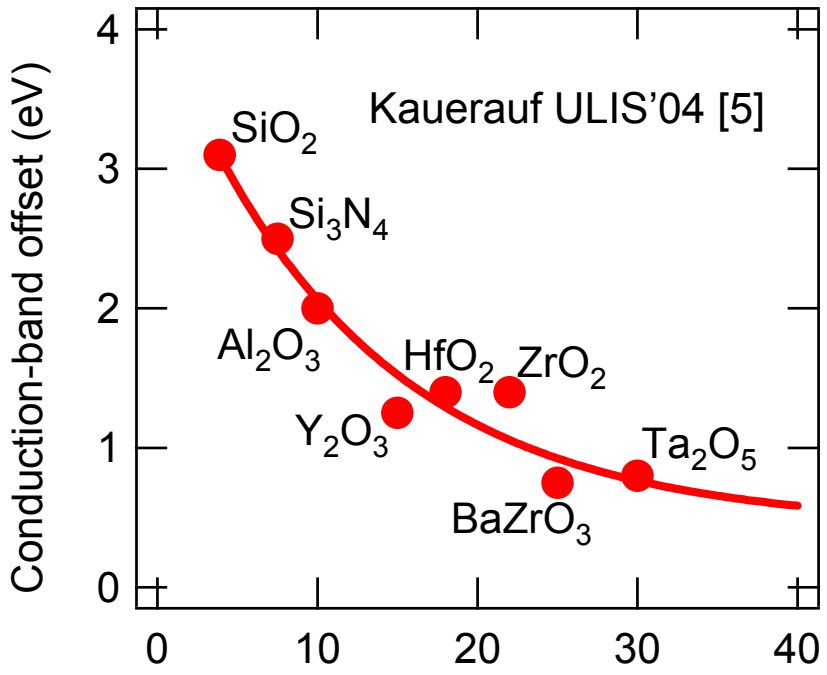


• direct/FP tunneling thru High-k

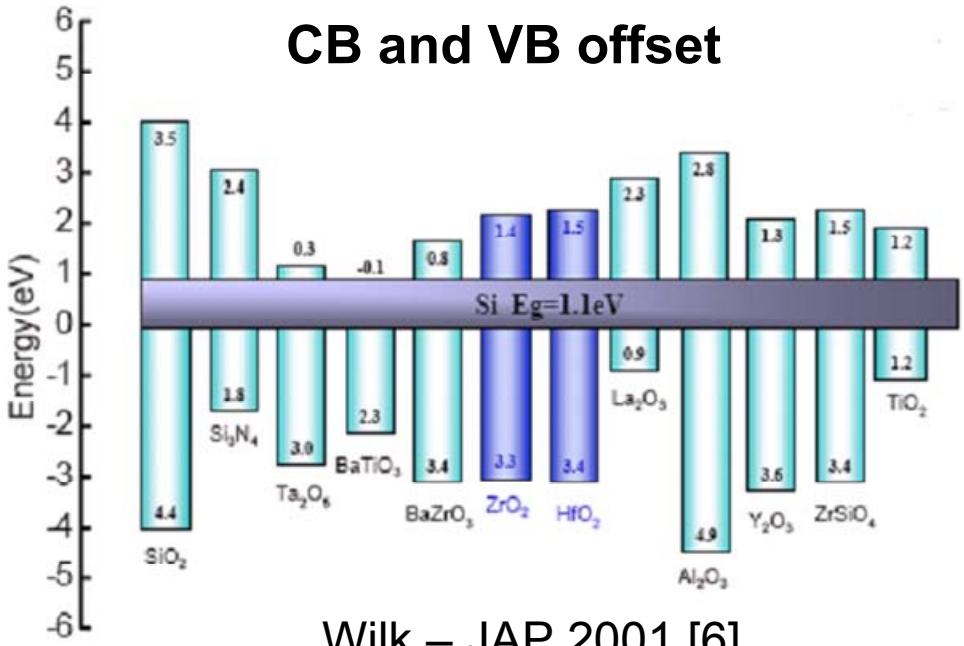
IG-VG from: Mistry - Intel - IEDM 2007 [4]

Improvement needed: Both HiK and Metal

k value vs CB offset

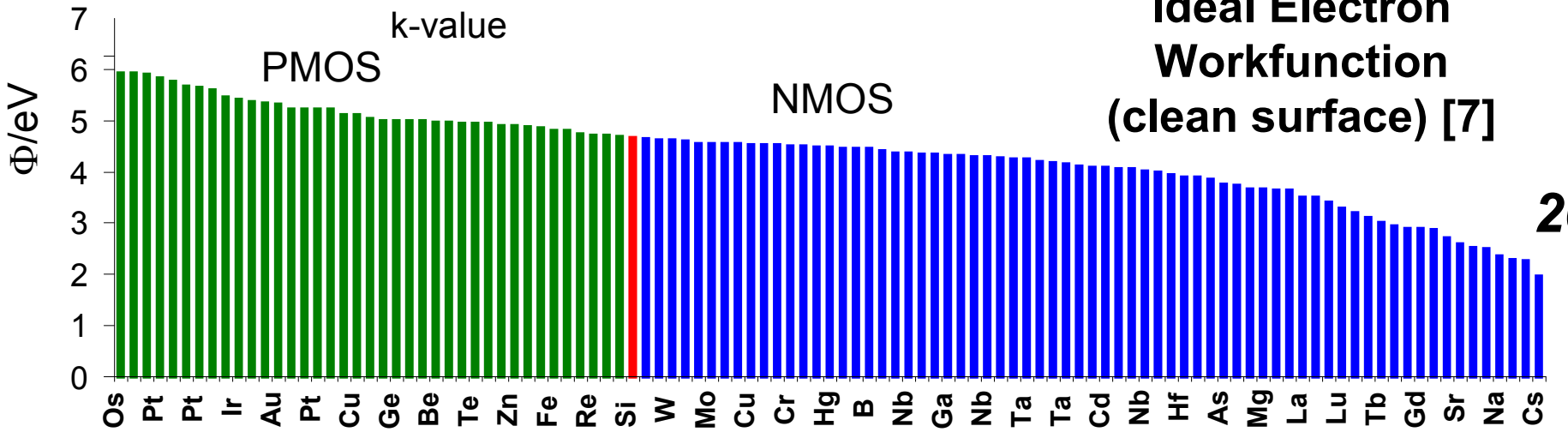


CB and VB offset

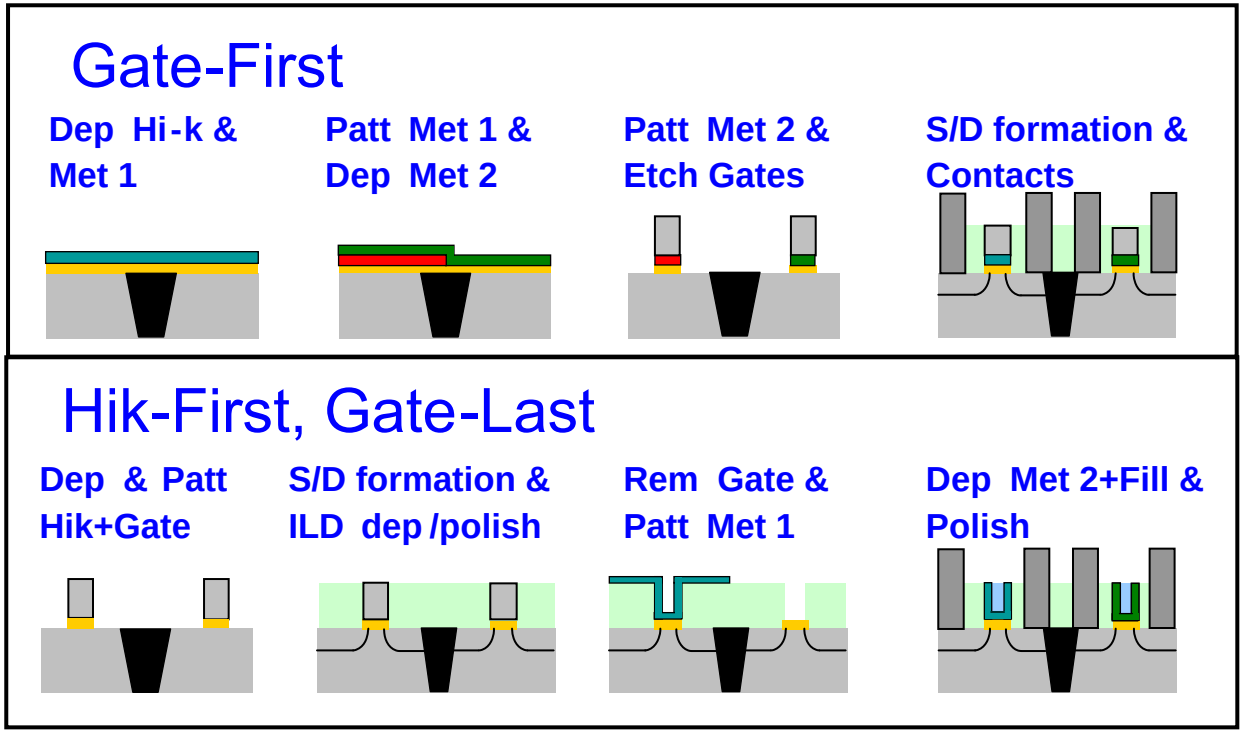


Wilk – JAP 2001 [6]

Ideal Electron Workfunction (clean surface) [7]



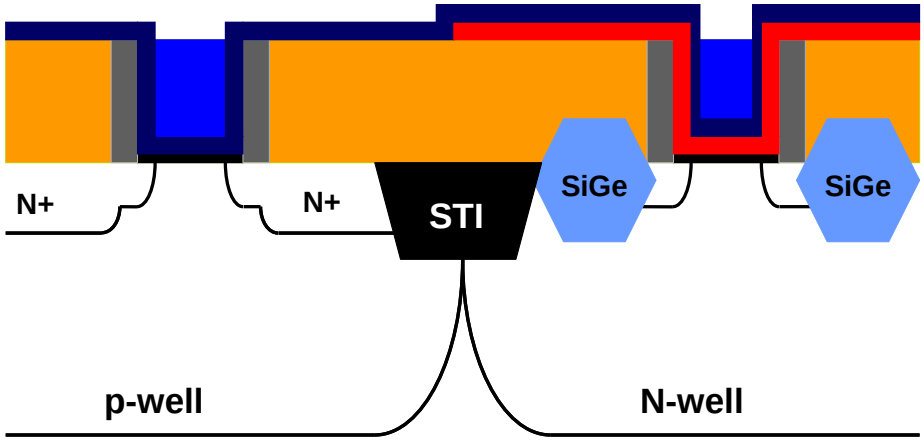
Gate First vs Gate Last



Advantages of gate last flow

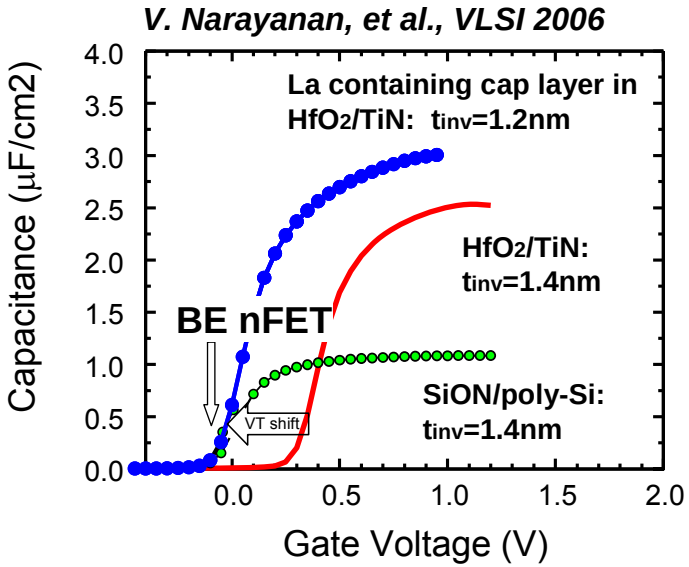
- **High Thermal budget available for Midsection**
  - Better Activation of S/D Implants
- **Low thermal budget for Metal Gate**
  - Large range of Gate Materials available
- **Significant enhancement of strain**
  - Both NMOS and PMOS benefit

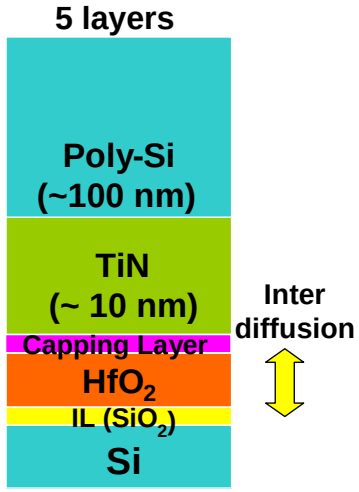
Two metals vs Two dielectrics



One Dielectric,
Two Φm metals

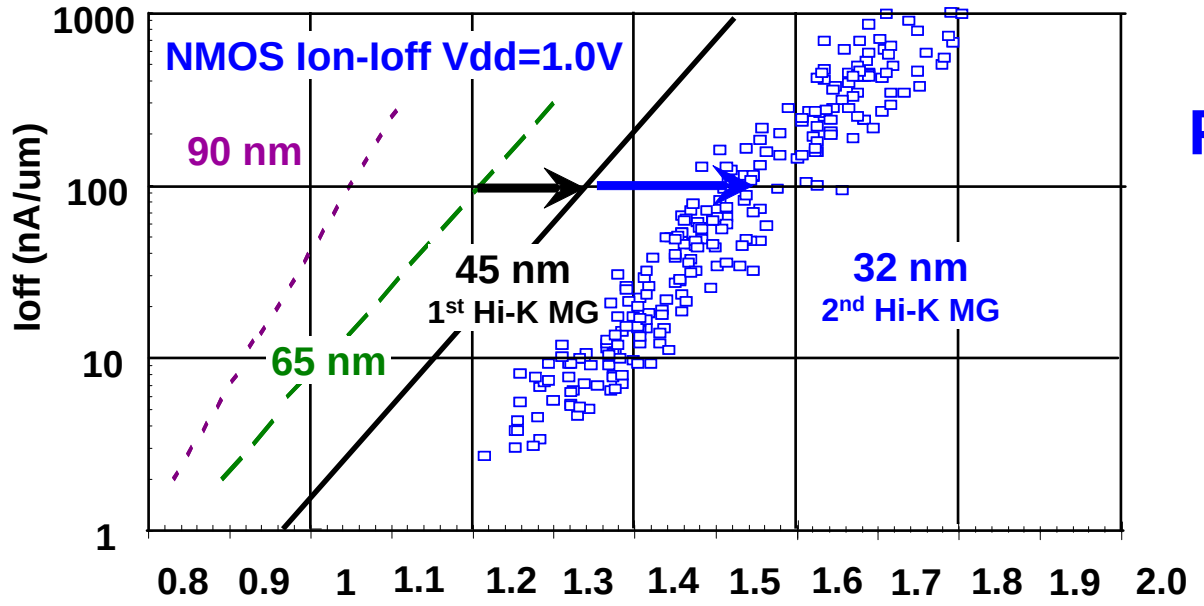
Mistry - Intel
IEDM 2007 [4]

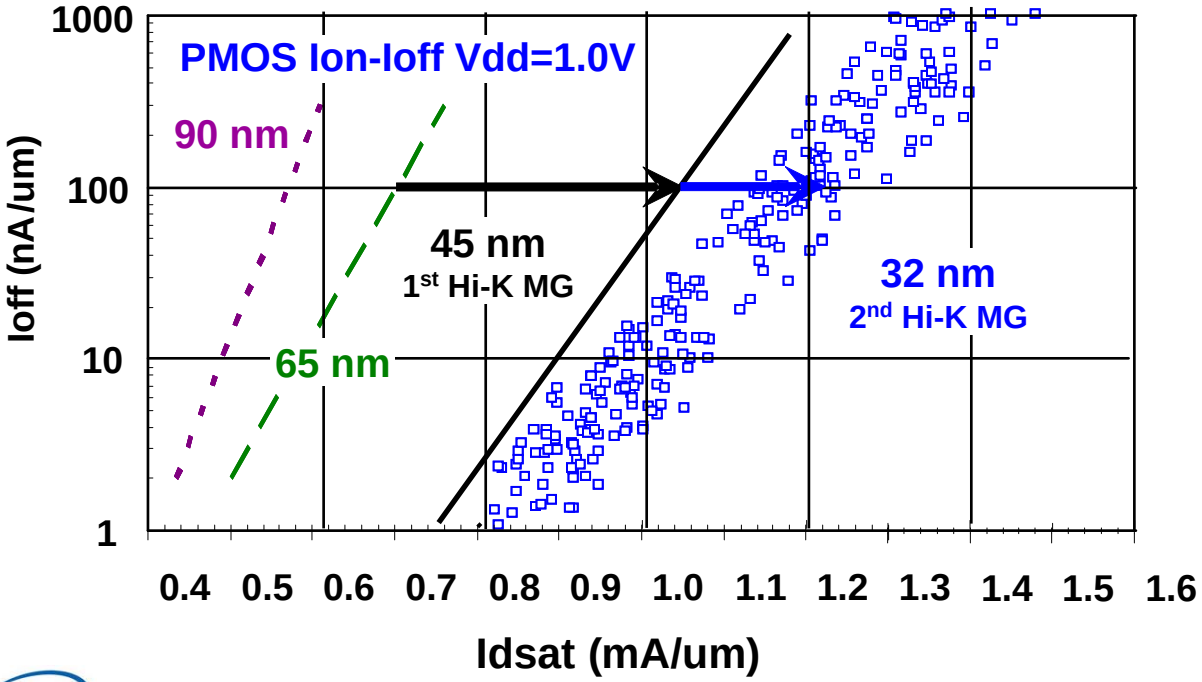




Two dielectric stacks
(with capping layers)
One Φm metal

Cartier - IBM
SEMICON 2008 [9]





FOUR GENERATION COMPARISON

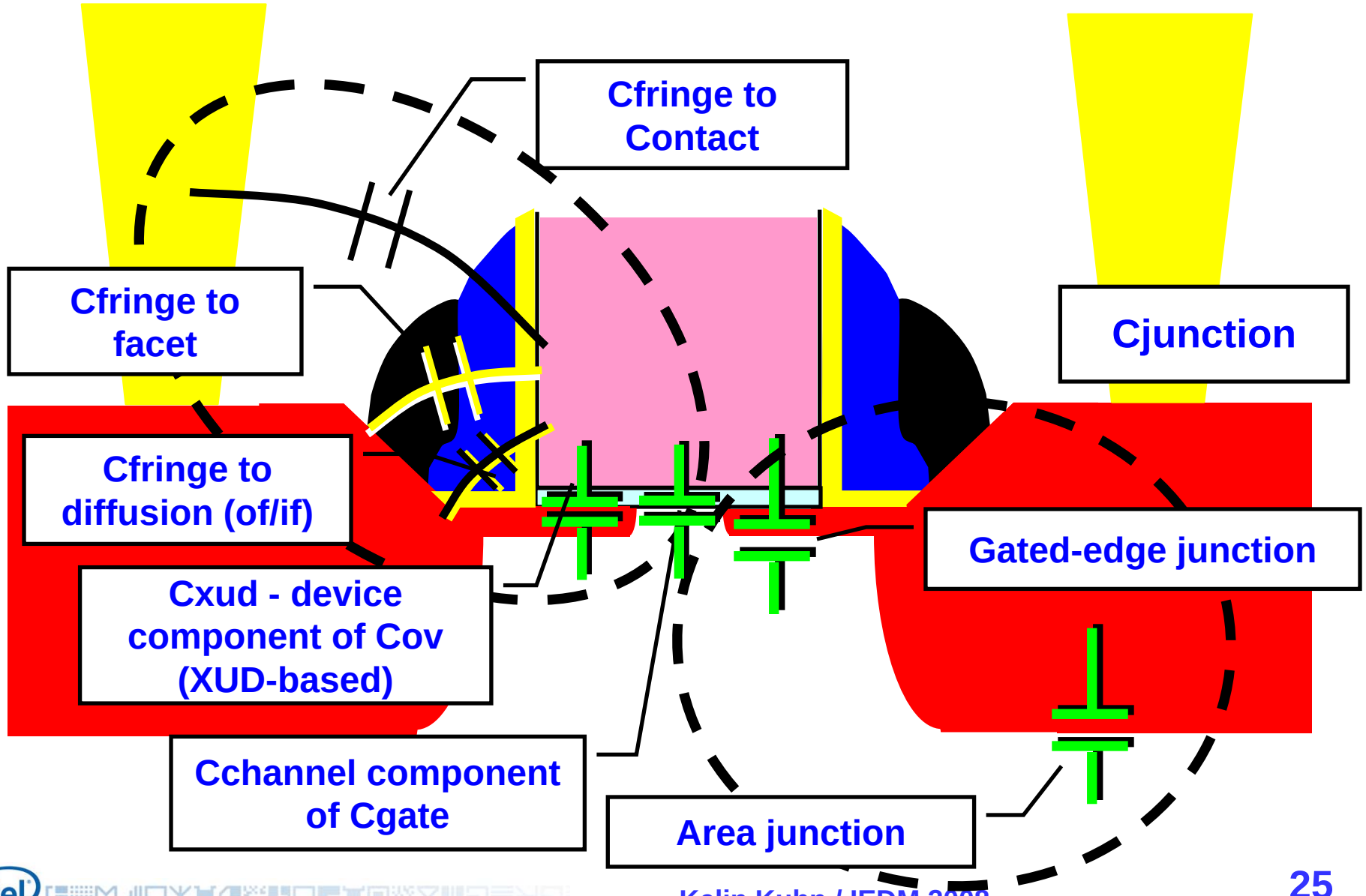
45nm:
1st gen. HiK-MG [4]

32nm:
2nd gen. HiK-MG [10]

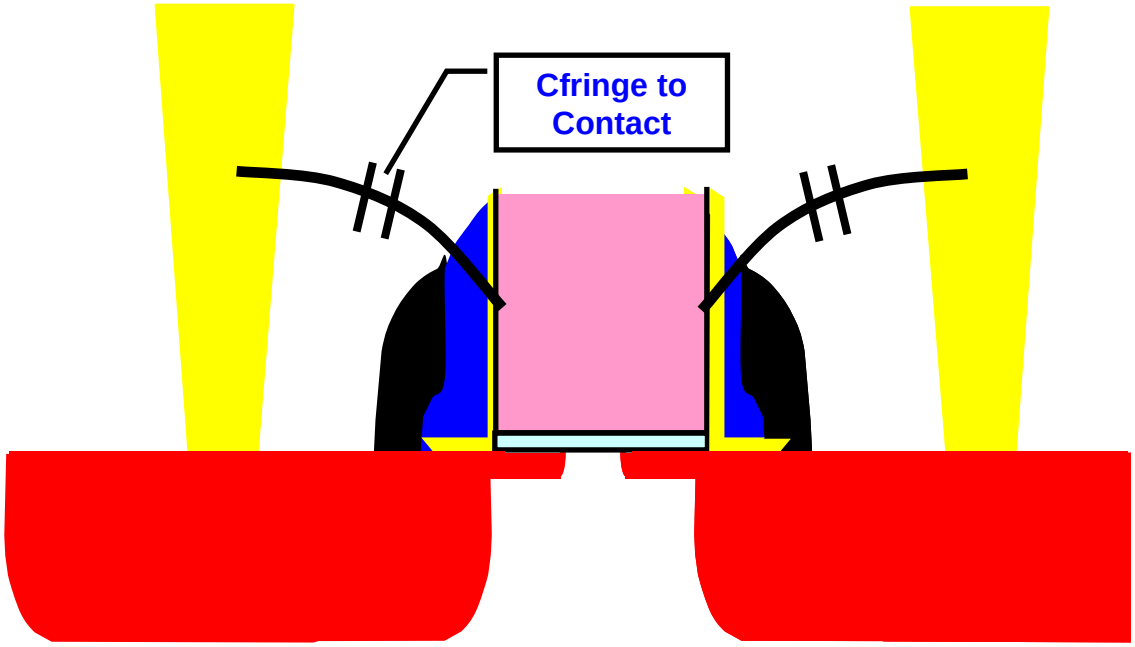
32nm data to be presented by S. Natarajan et al. Session 27.9

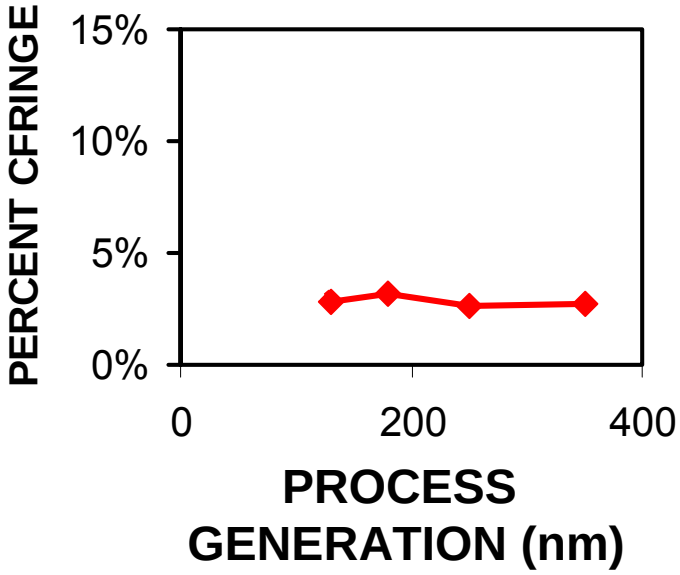
Capacitance

Planar Capacitive Elements



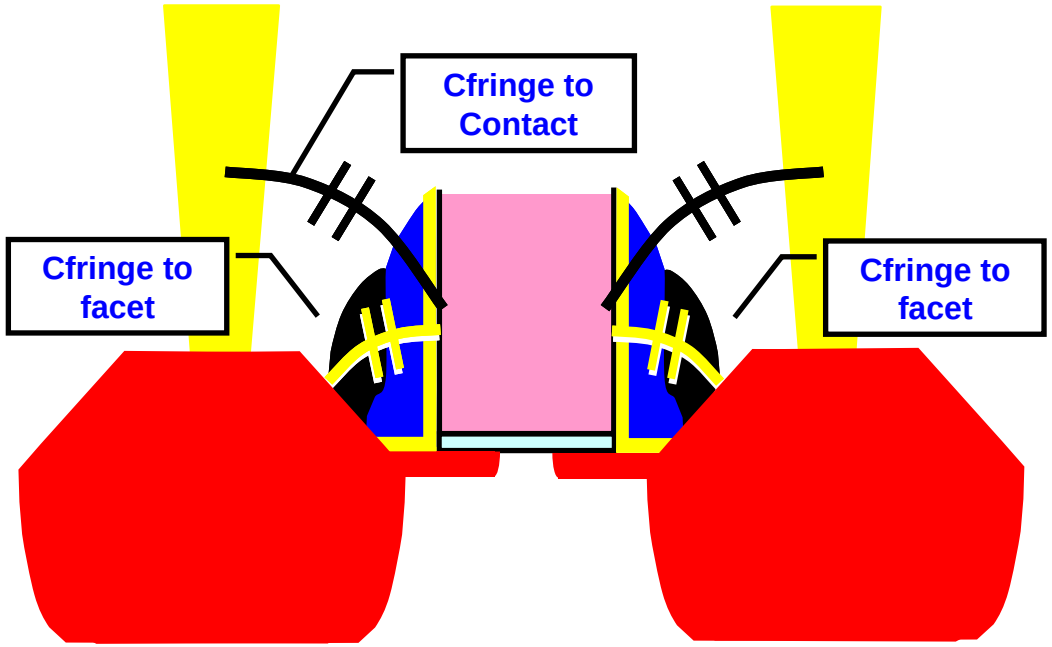
Planar Capacitive Elements

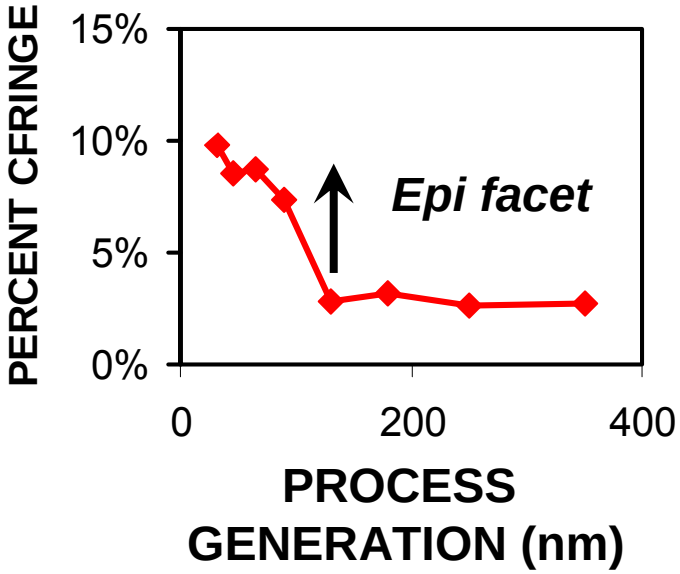




"Golden" days of scaling:
Who worried about Cfringe?

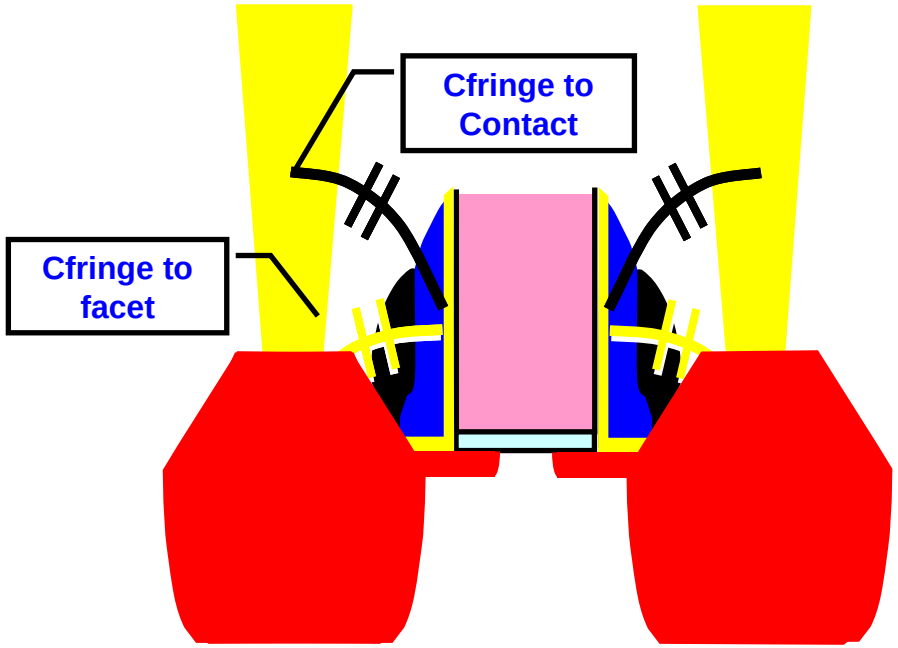
Planar Capacitive Elements

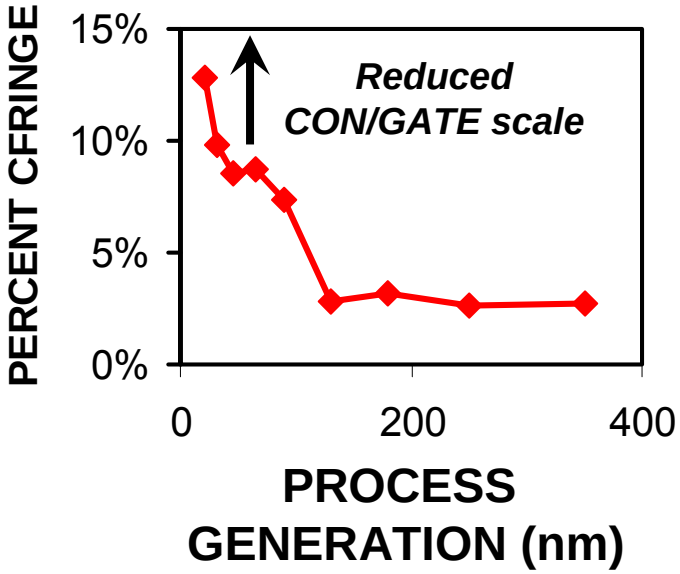




"Silver" days of scaling: Introduction of epi: Increased fringe due to facet

Planar Capacitive Elements

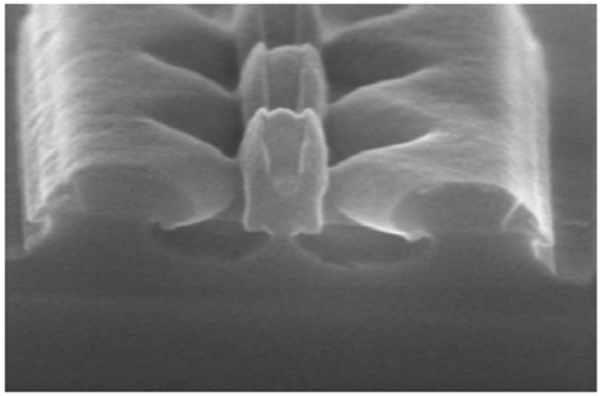




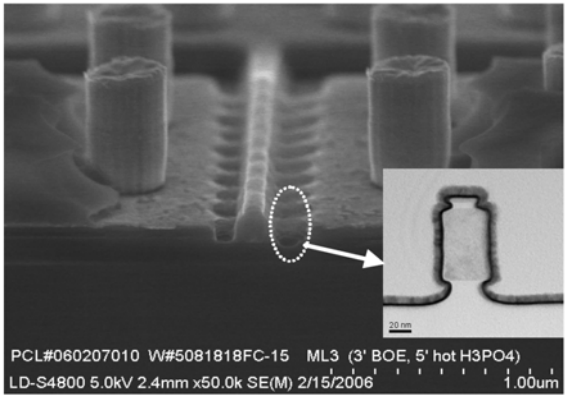
"Bronze" days of scaling

Gate and contact CD dimensions scaling slower than contacted gate pitch – fringe matters

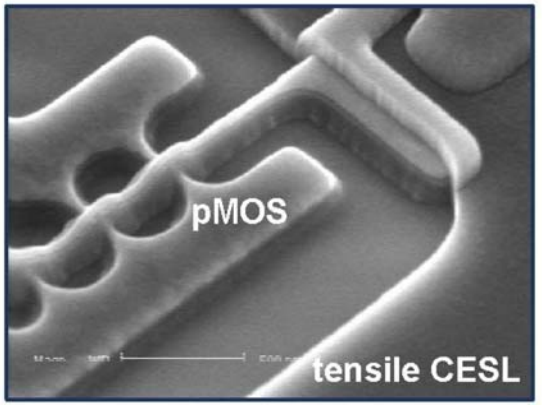
Recent MuGFET geometries in the literature



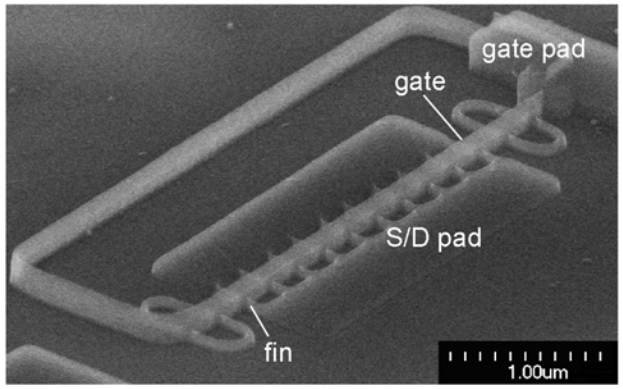
Verheyen–IMEC
VLSI 2005 [11]



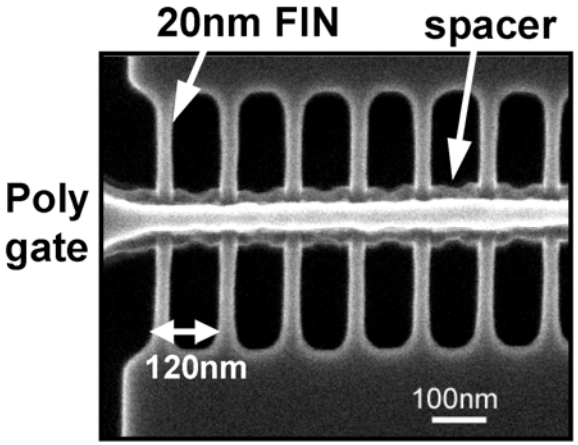
Kang–Sematech
IEDM 2006 [12]



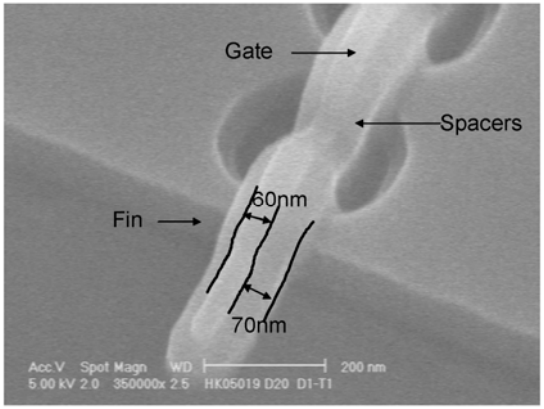
Collaert–IMEC
VLSI-TSA 2007 [13]



Kaneko–Toshiba
IEDM 2005 [14]

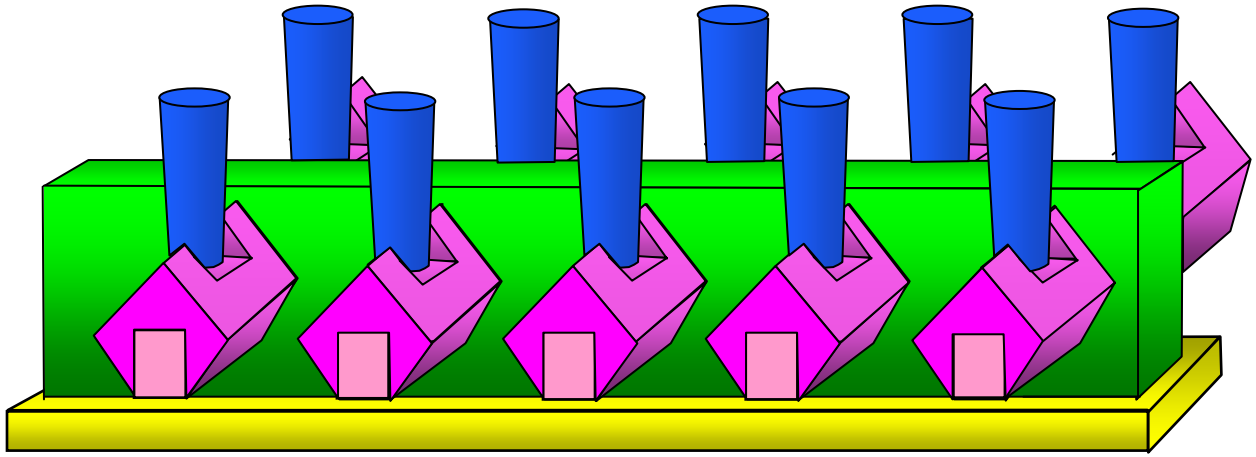


Shang–IBM
VLSI 2006 [15]



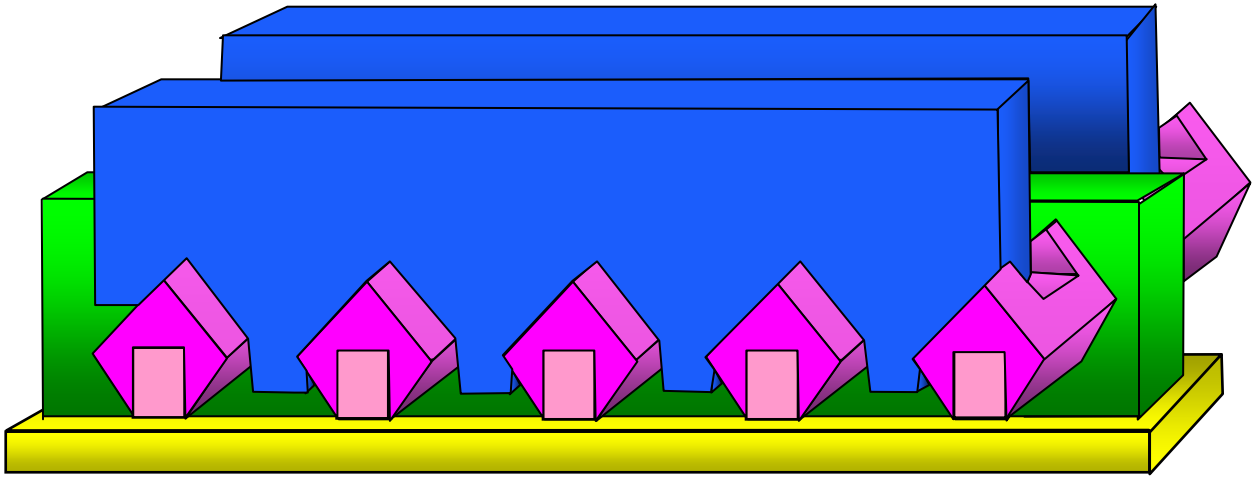
Lenoble–STM/IMEC
VLSI 2006 [16]

Possible production architectures



Unlikely

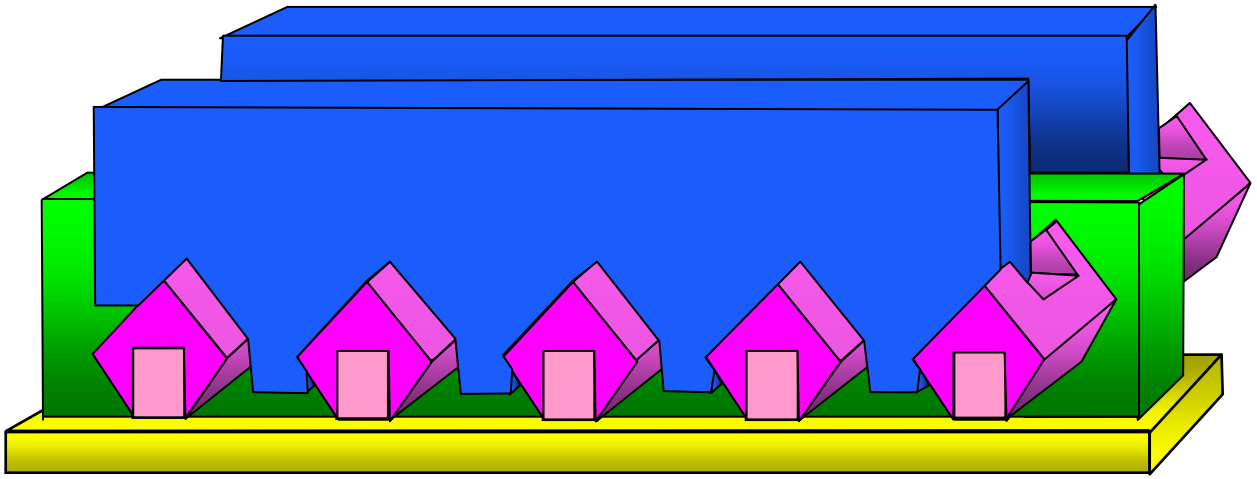
Contact patterning limitations

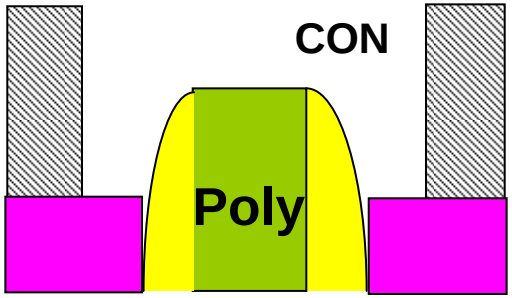


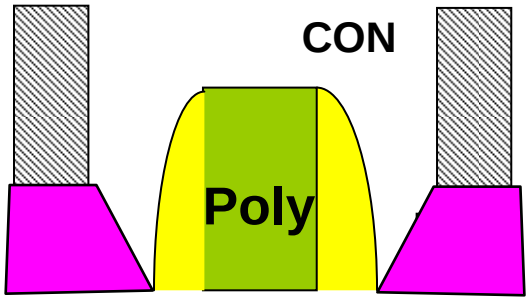
Possible

Leveraging “trench” contact architecture

MuGFET Capacitance Elements

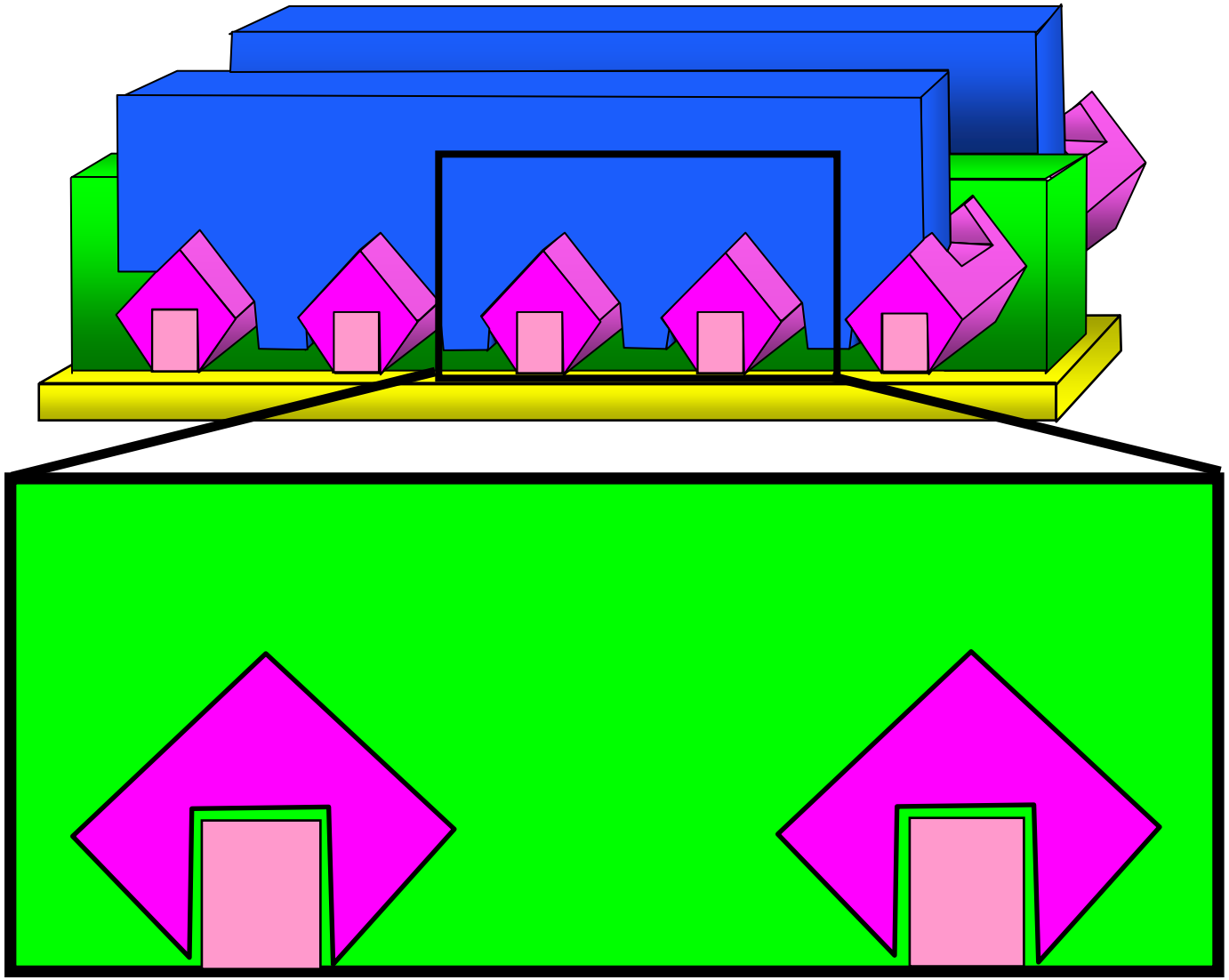


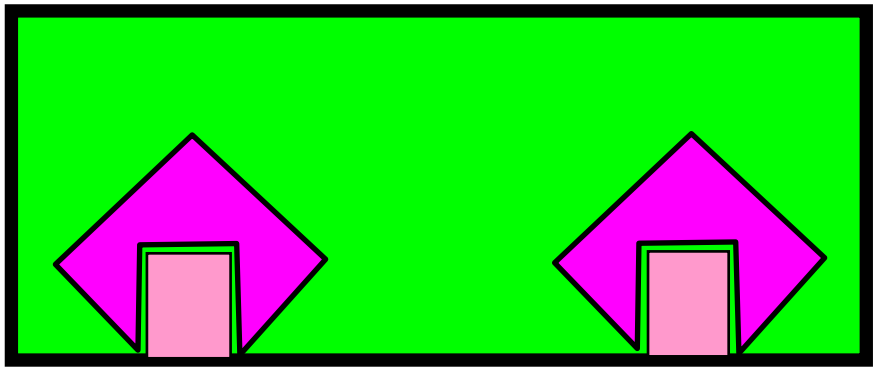




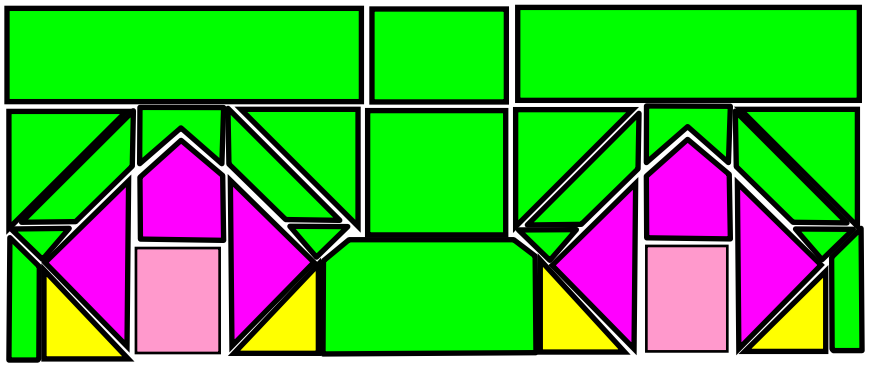
Con-poly and Facet-poly are a critical component of capacitance evaluation

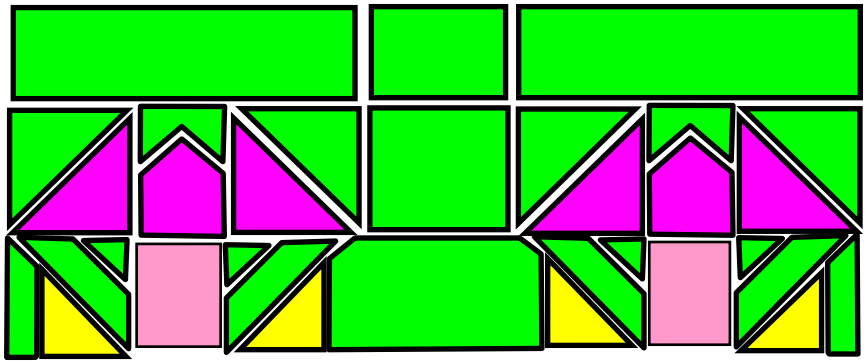
MuGFET Capacitance Elements



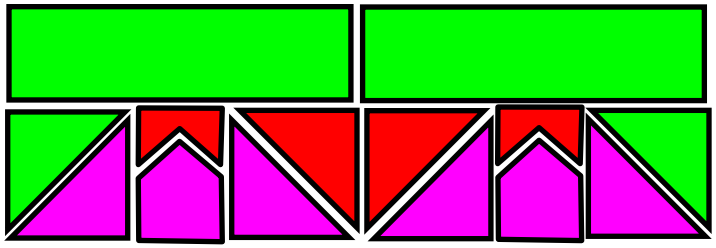


MuGFET to planar "Polyominoes"



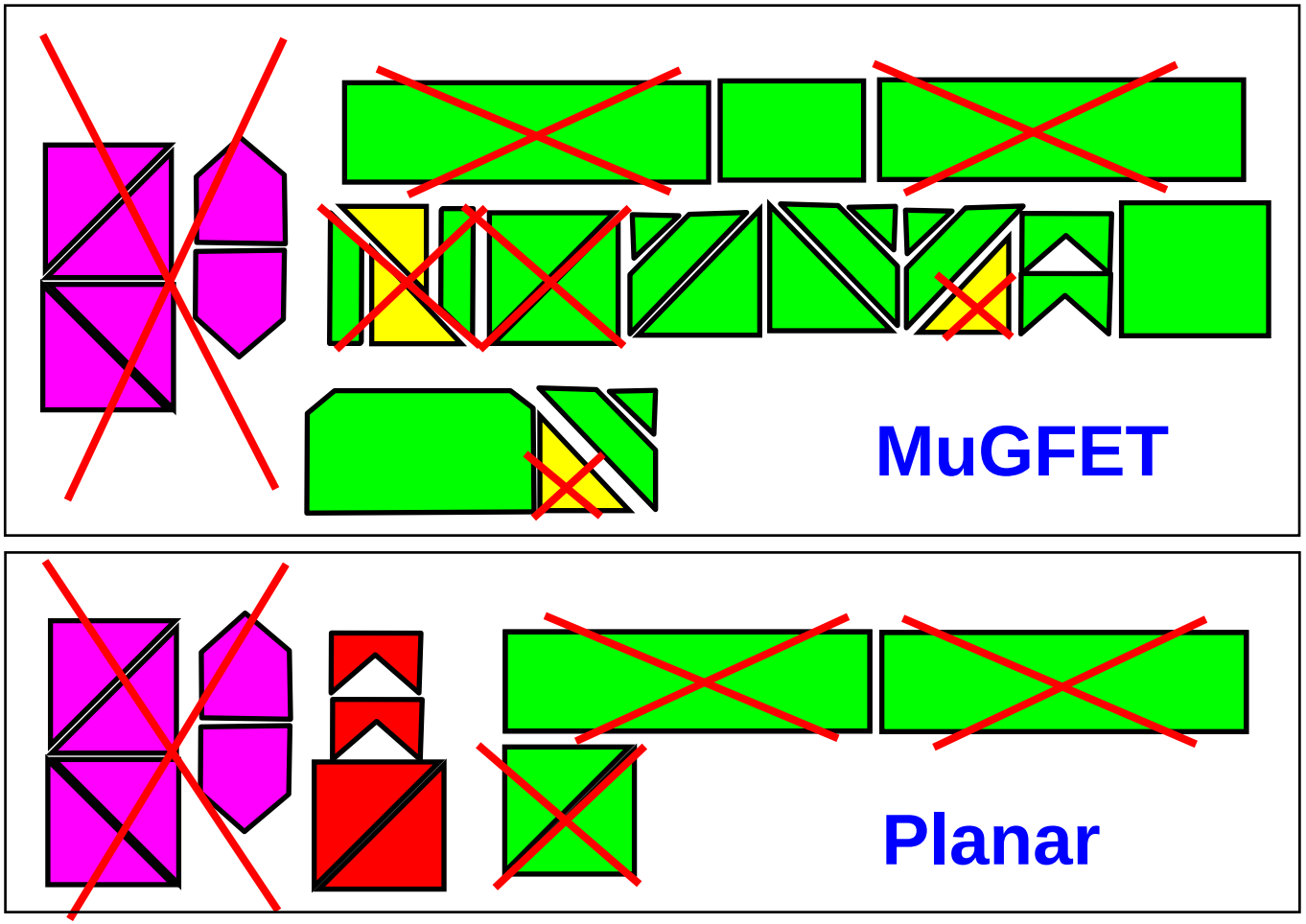


Reorganized to emulate planar



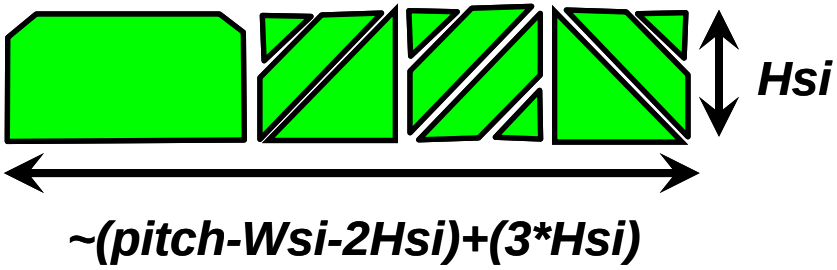
Equivalent planar device

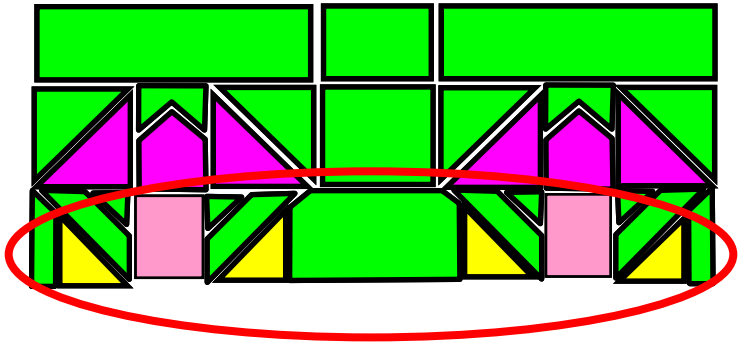
MuGFET – Planar: Differential Capacitance



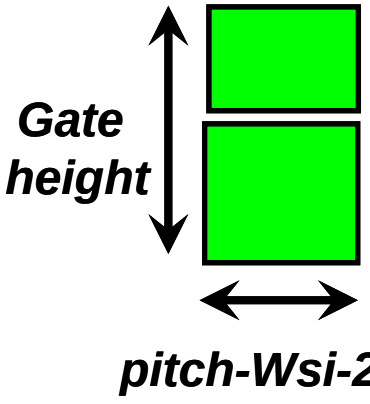
Remove common elements (green/magenta)
Remove non-contributing capacitive elements (yellow)

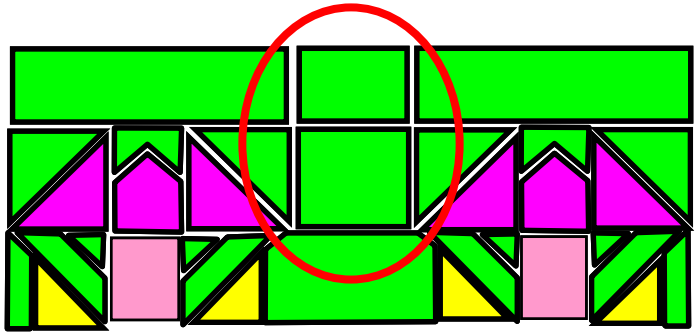
MuGFET – Planar: Differential Capacitance





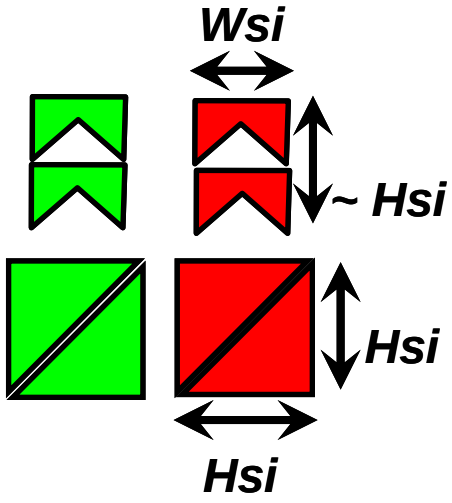
MuGFET has INCREASED CON-poly fringe capacitance (Originates primarily from space around/below fin)



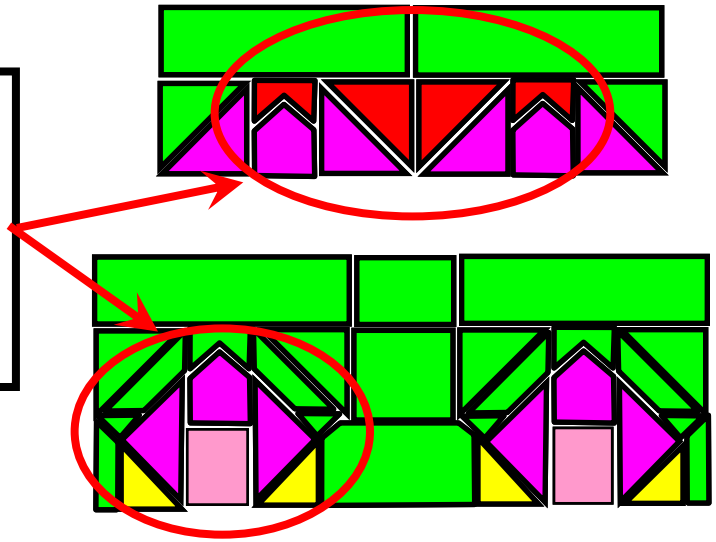


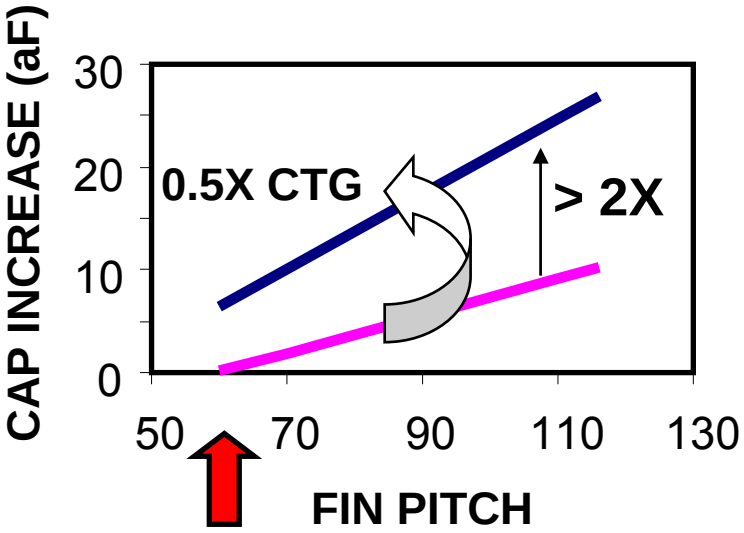
MuGFET has INCREASED Con-poly fringe capacitance due to pitch > 2HSi. (Dead space)

MuGFET – Planar: Differential Capacitance



MuGFET has DECREASED epi-facet to poly capacitance due to facet limited fin growth

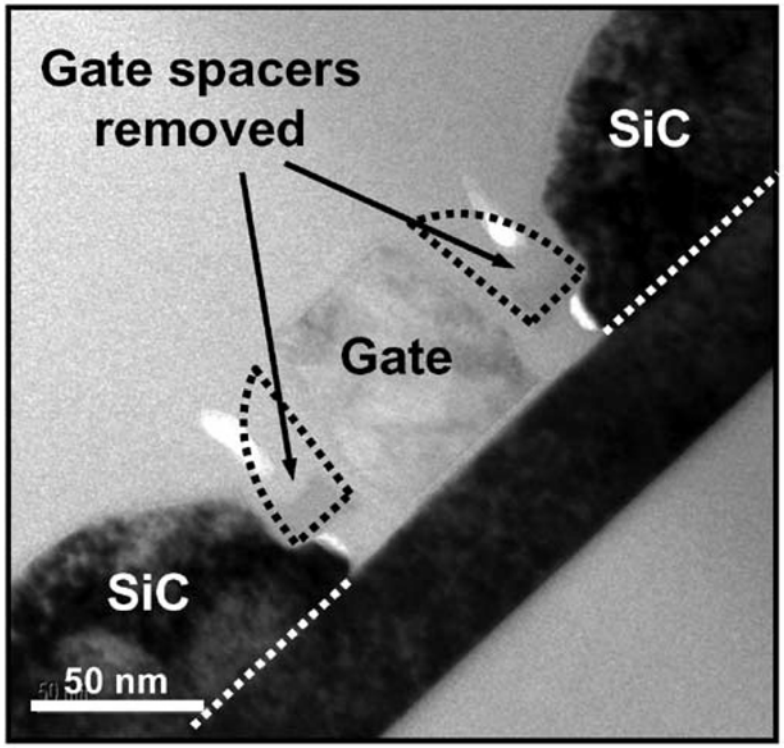




Overall?
MuGFET >> planar
Strong pitch sensitivity
Strong contact-gate sensitivity

>1 generation litho (even w/ 193 wet)

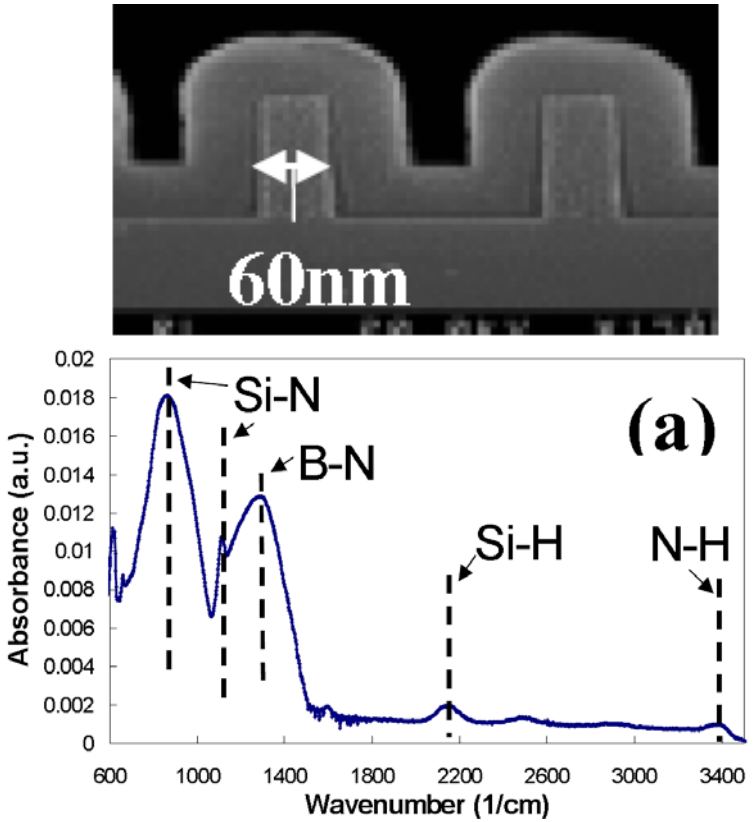
Innovative Spacer Technologies



SPACER REMOVAL

Liow – NUS Singapore

EDL 2008 [17]



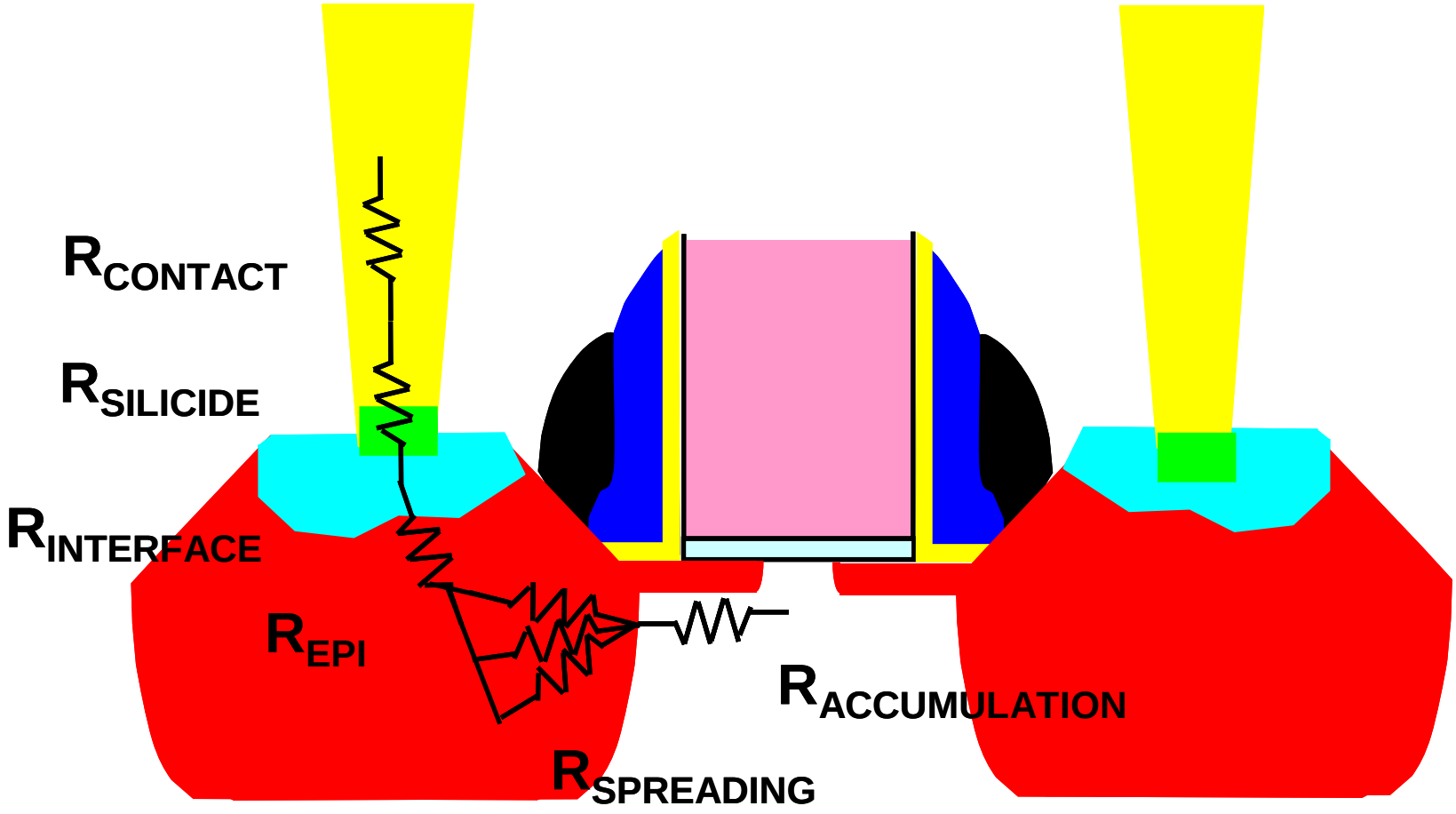
SiBCN (Low-K) SPACER

Ko –TSMC

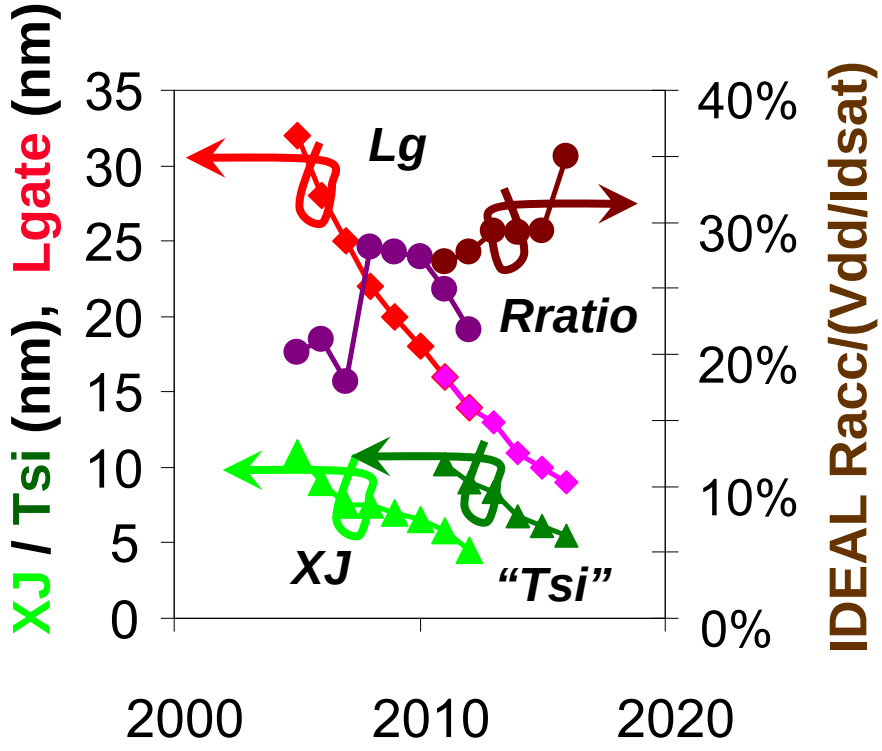
VLSI 2008 [18]

Resistance

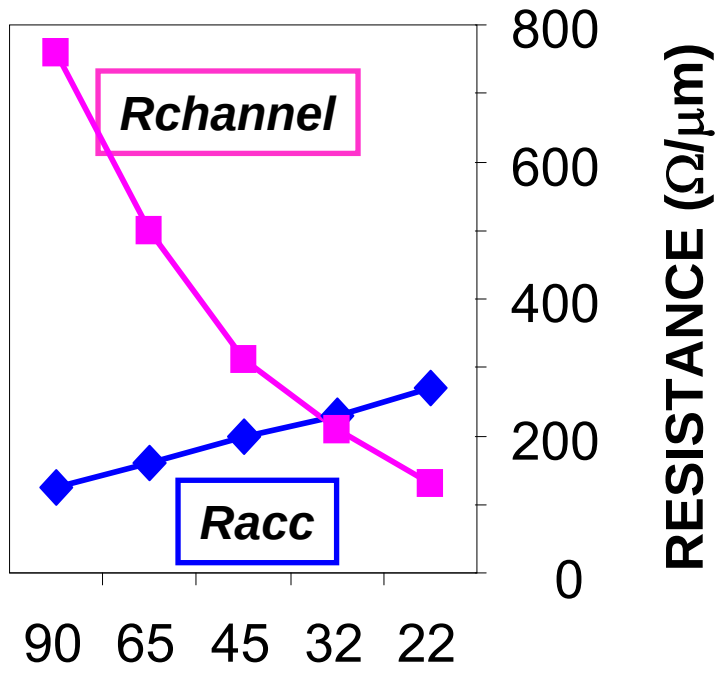
Planar Resistive Elements



Technology trends
Xj/Tsi, Lg, Racc

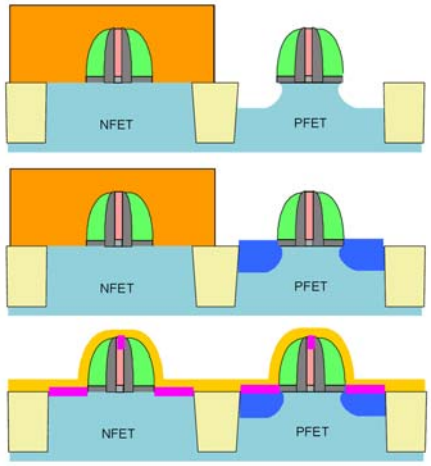


ITRS 2007 [19]



Noori - Applied Materials
TED 2008 [20]

Advanced Laser Anneal Technologies



1. Form protective layer over NFET
2. Si recess RIE

3. e-SiGe module (epi preclean, in situ doped SiGe growth etc)

4. Remove protective layer
5. S/D anneal
6. Ni silicide
7. CSL

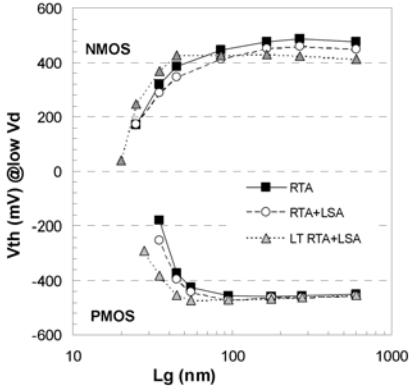


Figure 3: Threshold voltage measured in the linear regime as a function of L_g.

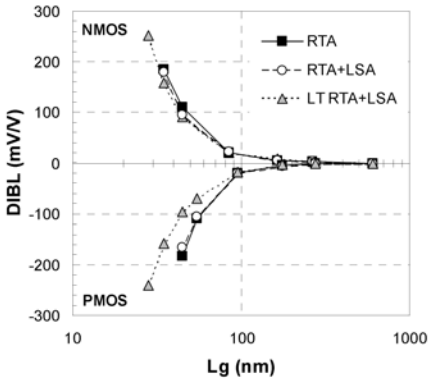
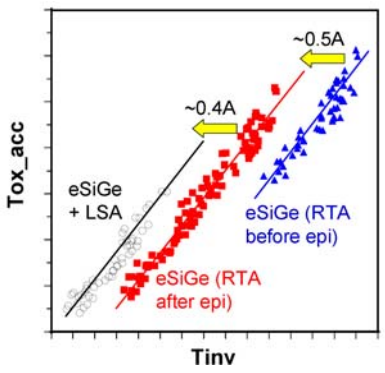
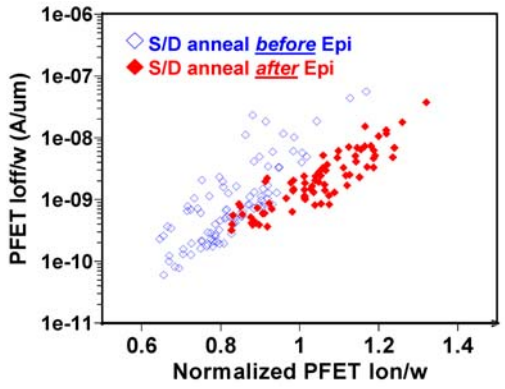
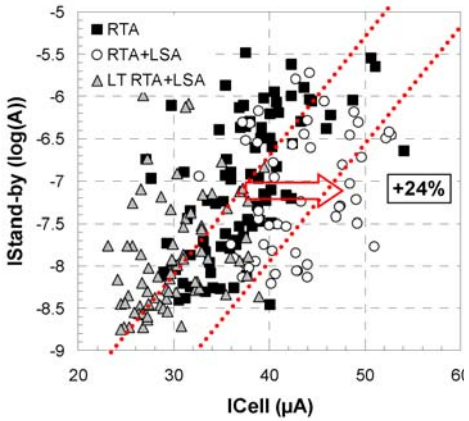
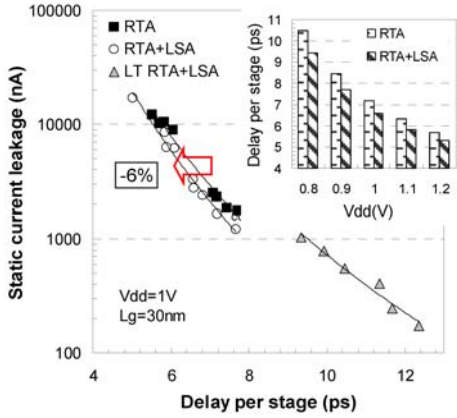


Figure 4: Drain-Induced Barrier lowering (DIBL) regime as a function of L_g.





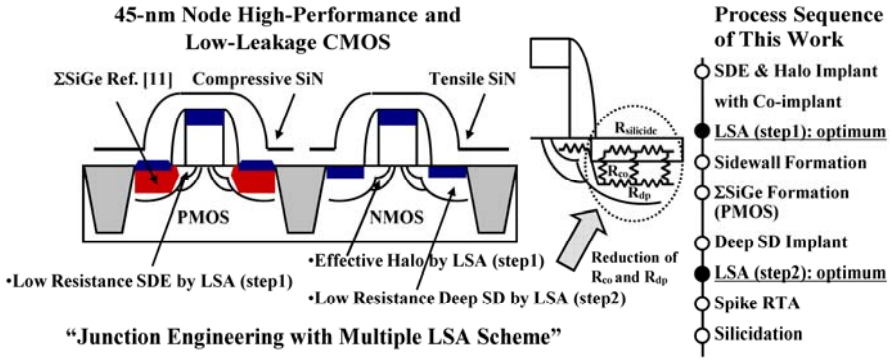


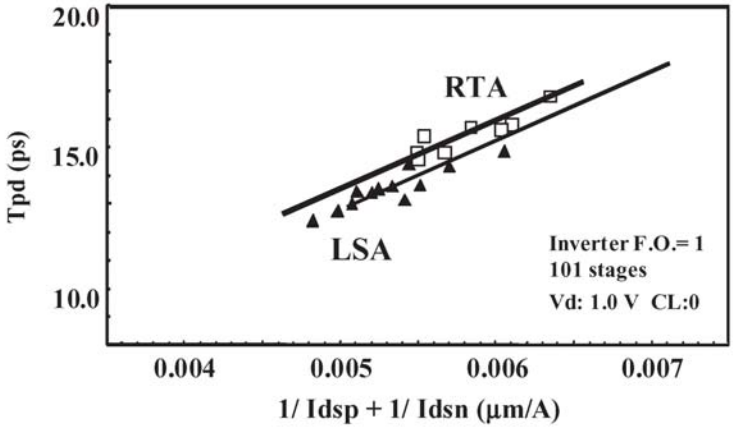


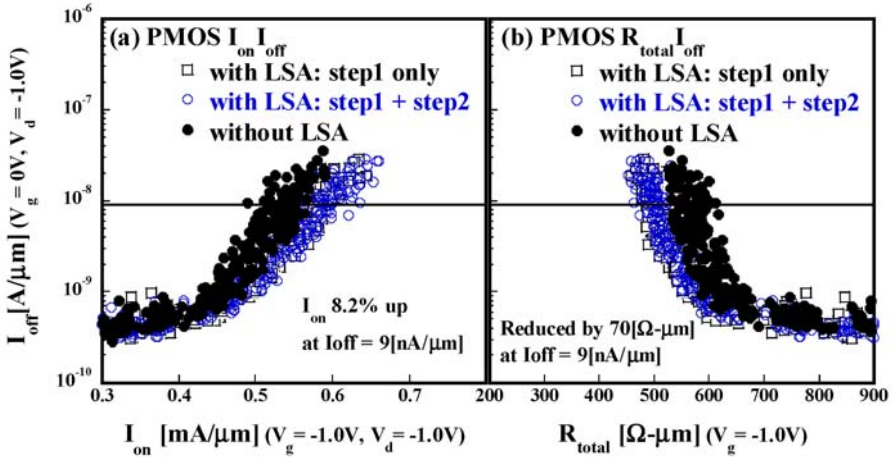
Luo – IBM
IEDM 2005 [21]
E-SGe+CSL and LSA

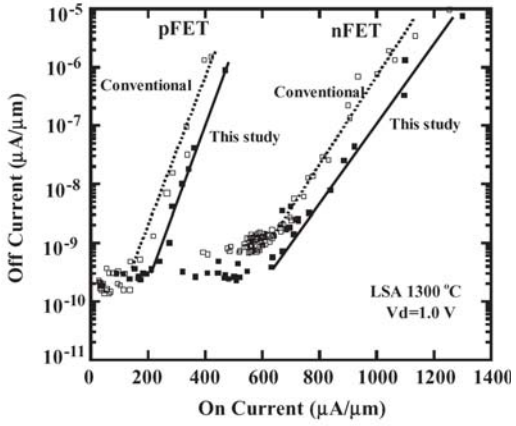
Pouydebasque – Philips
IEDM 2005 [22]
SRAM/RO with LSA

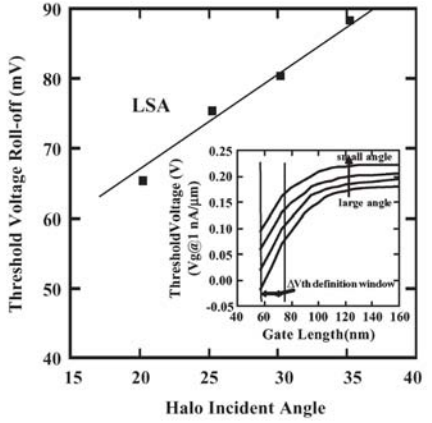
More Advanced Laser Anneal Technologies







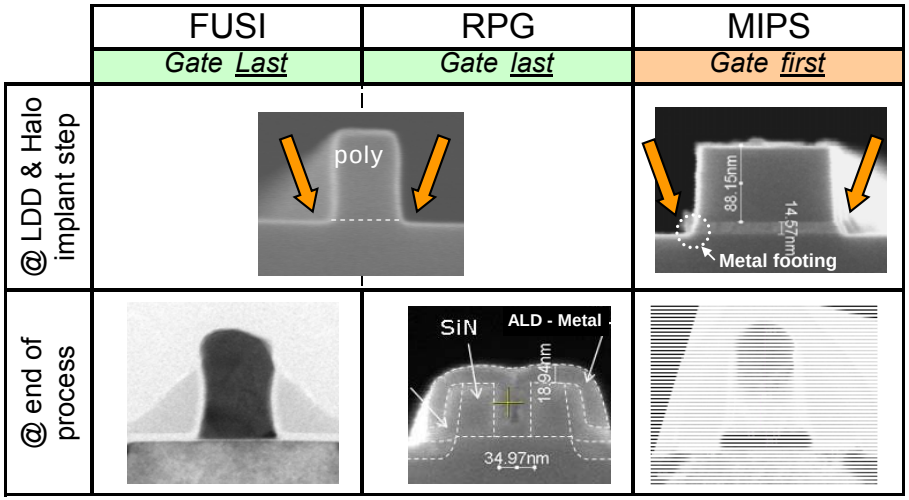


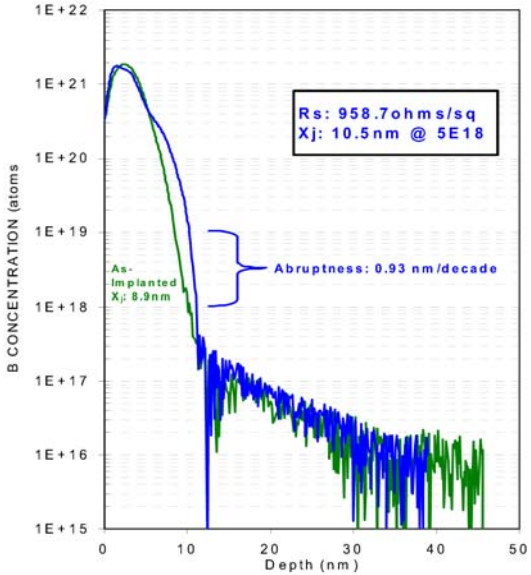


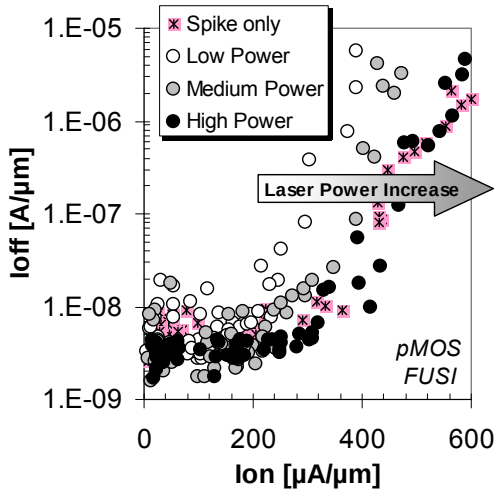
Yamamoto – Fujitsu
IEDM 2007 [23]
Multiple laser spikes + RTA

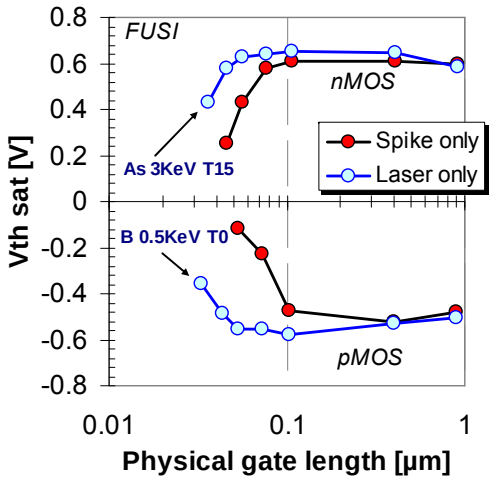
Shima – Hitachi
TED 2007 [24]
Non-melt LSA

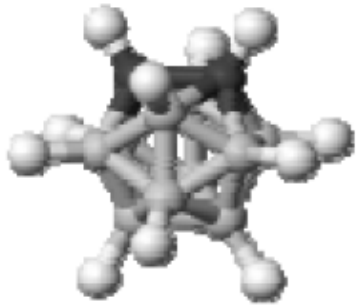
Even More Advanced Technologies Required







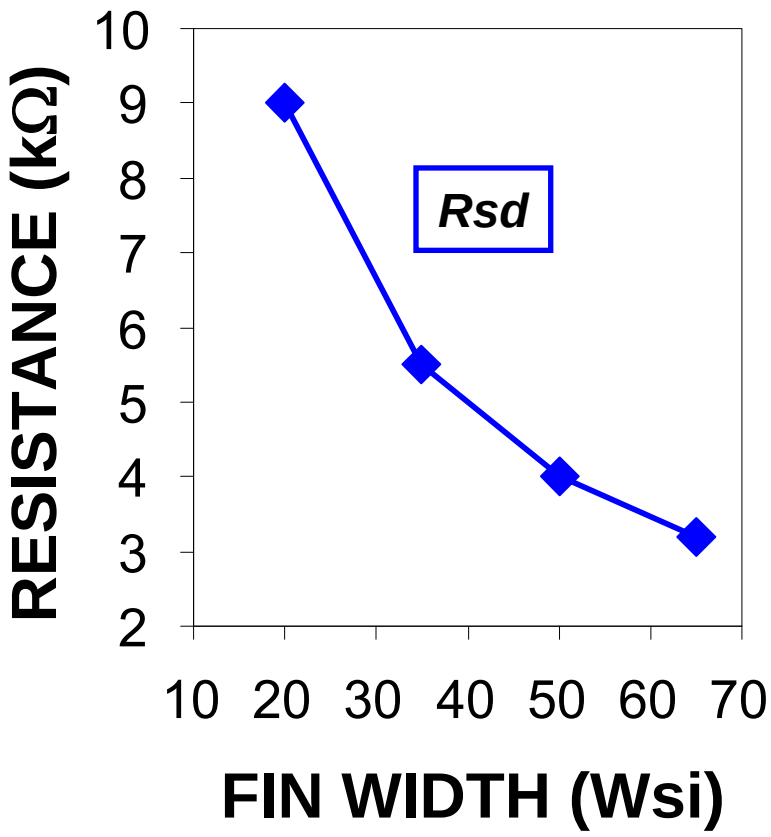




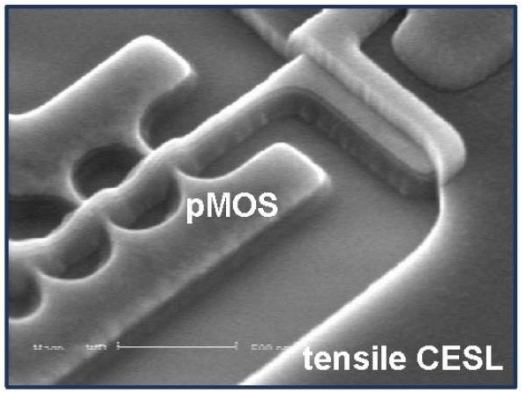
Ortolland – IMEC – VLSI 2008 [25]
Non-melt LSA with adv. gate stacks

Gelpey – Mattson-VSEA – IWJT 2008 [26]
Flash + Adv. doping techniques

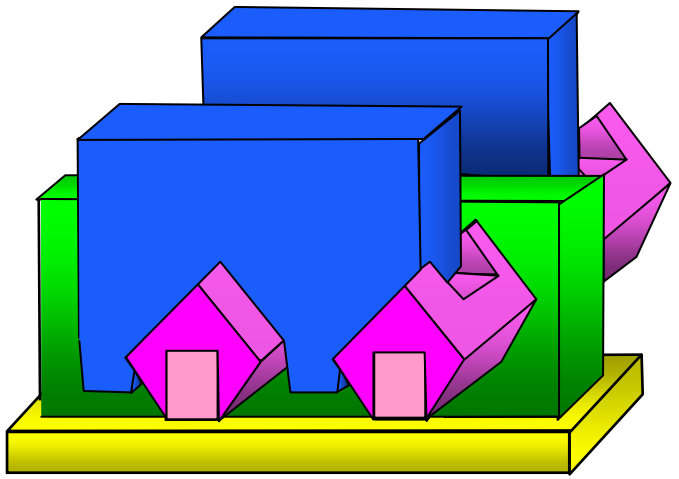
MuGFET Wsi Impact



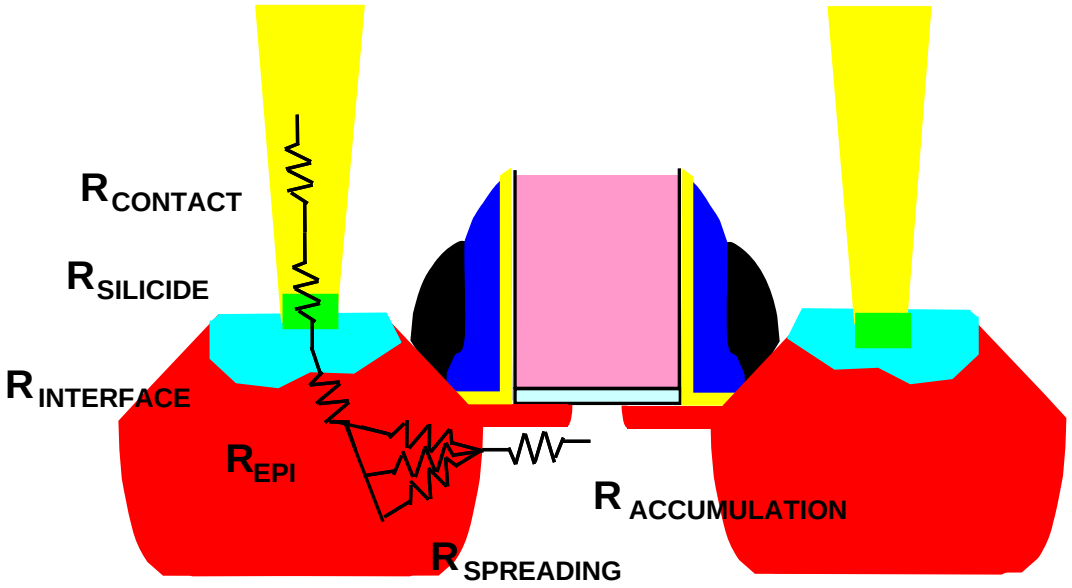
Dixit – IMEC
TED 2005 [27]



Collaert – IMEC – VLSI-TSA 2007 [13]



Low Barrier Height Contacts



$$R_{\text{interface}} \propto \exp\left(\frac{q\phi_B}{\sqrt{N_D}}\right)$$

$$R_{\text{interface}} \propto \frac{1}{A}$$

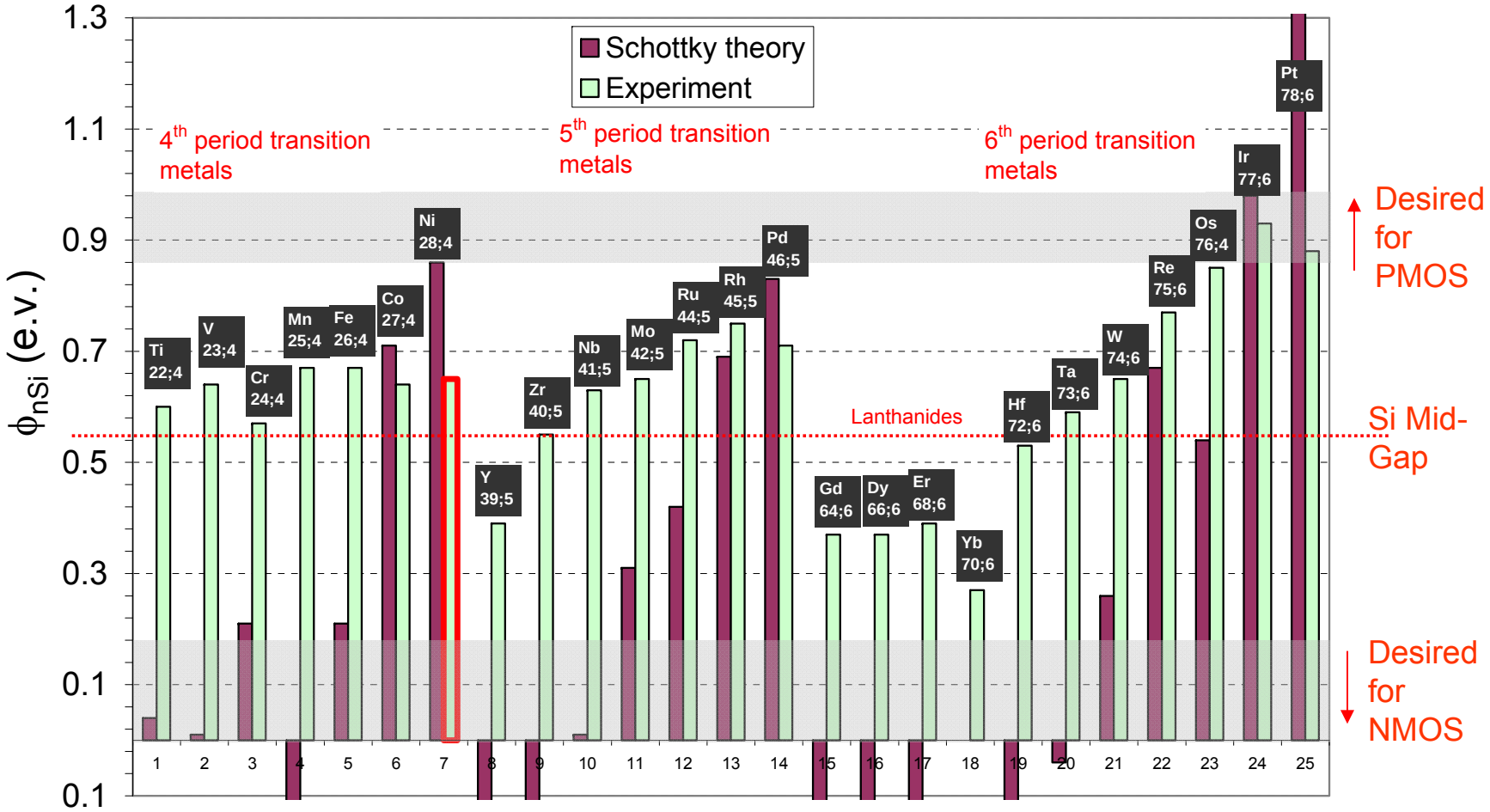
$q\phi_B - Schottky\ \ Barrier\ \ Height\ (SBH)$

$N_D - Substrate\ \ doping\ \ conc.$

$A - Contact\ \ area$

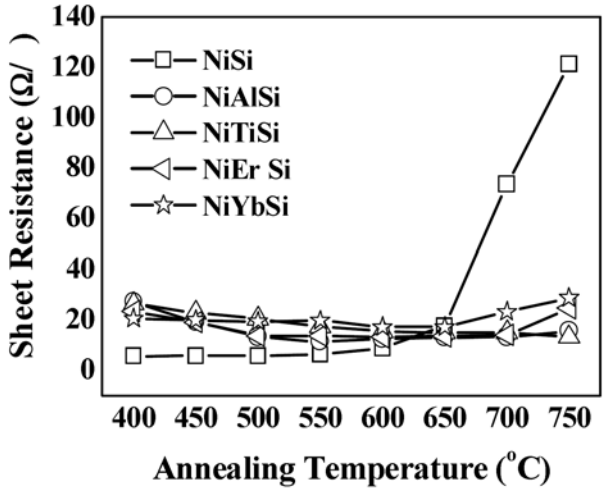
- $R_{interface}$: Schottky Barrier Height (SBH) between silicide and Si
- $R_{silicide}$: intrinsic resistance of silicide
- Limited additional improvement with $R_{silicide}$
  (NiSi has the lowest known resistivity of all silicides at 10.5 μohm-cm)
- Optimized barrier-height SBH for NMOS and PMOS
  (Some potential for further $R_{contact}$ reduction)

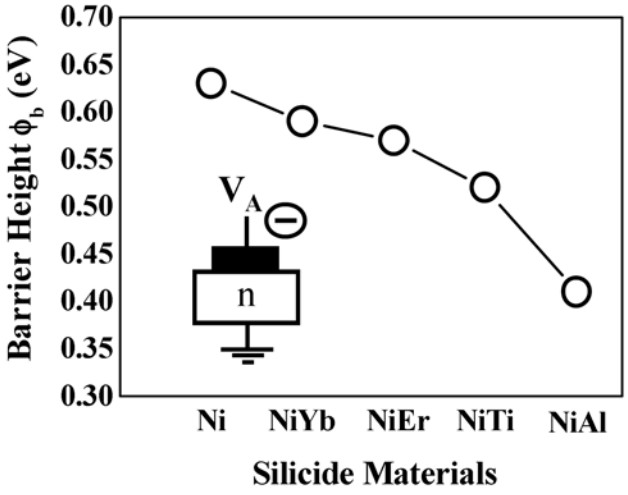
Schottky theory vs. experimental SBHs for metals on nSi
Mukherjee – Intel [28]



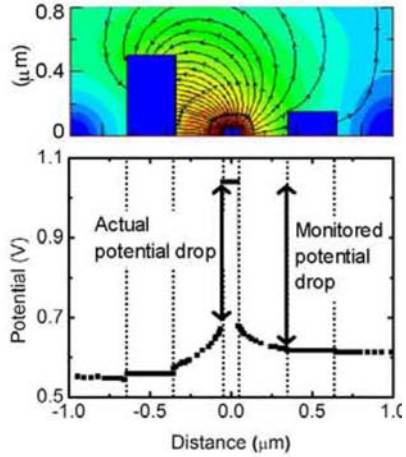
Fermi level pinned to mid-gap for most metals on Si

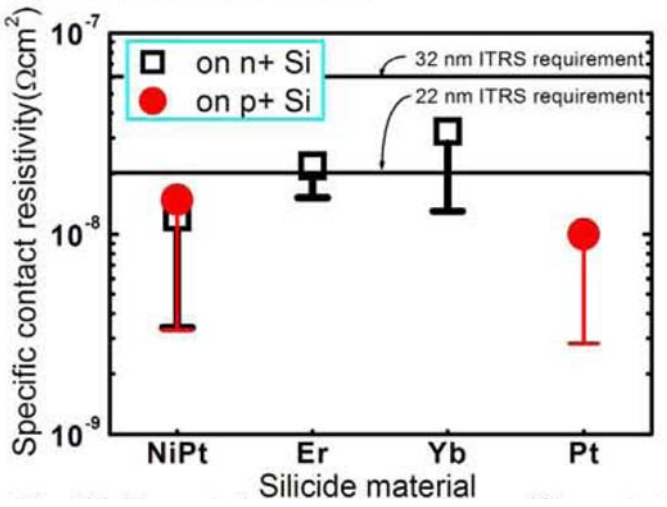
Alloy Modifications to Traditional Silicides





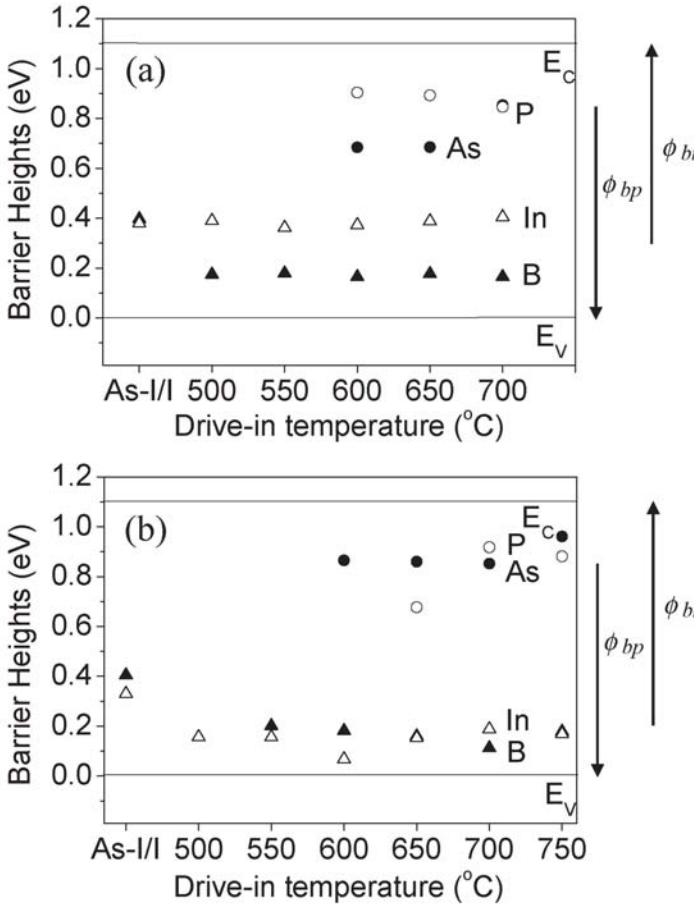
Lee –NUS-Singapore
IEDM 2006 [29]
Ni-alloy silicides



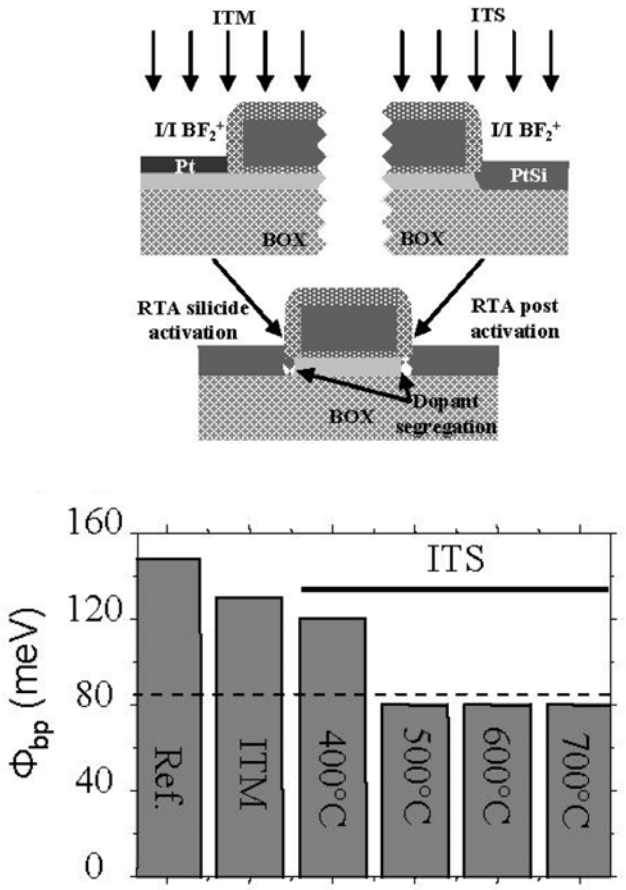


Ohuchi – Toshiba
IEDM 2007 [30]
NiPt-alloy silicides

Implant Modifications to Traditional Silicides

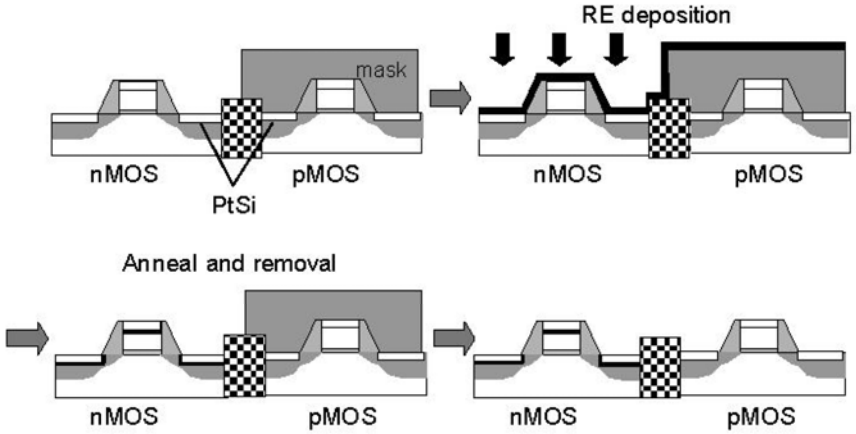


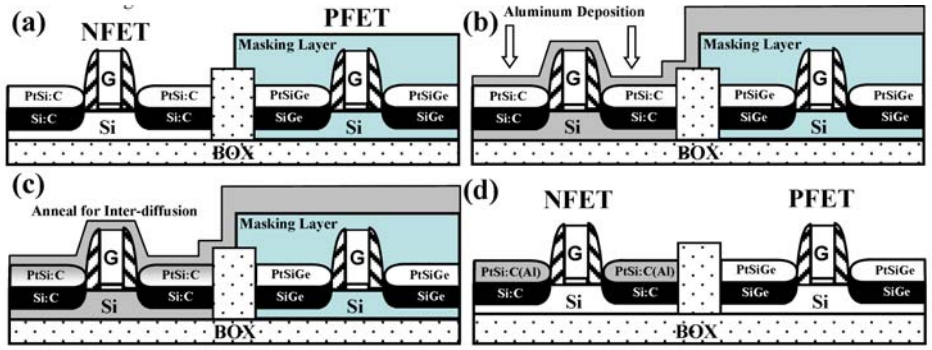
Zhang – KTH Sweden
EDL 2007 [31]
Implant modification of SBH
(SB FET paper)

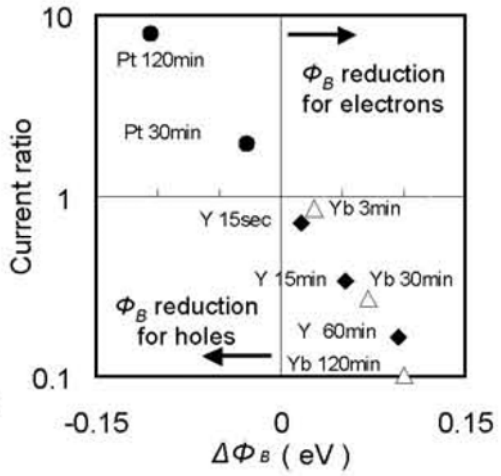


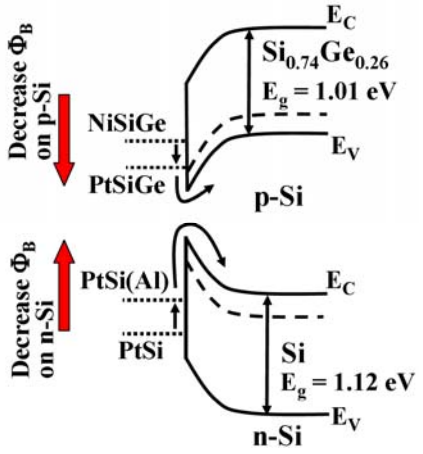
Larrieu – IEMN France
IEDM 2007 [32]
Dopant segregated implant through metal/silicide (SB FET paper)

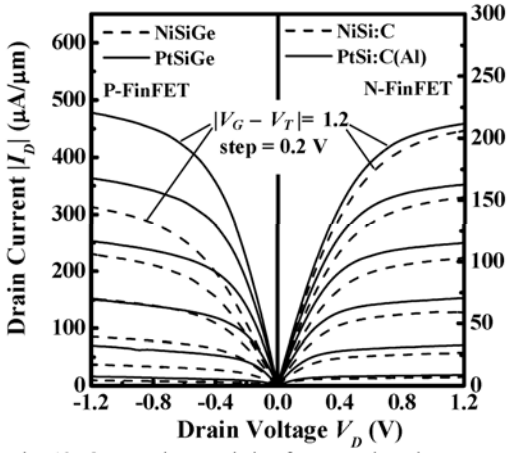
Novel dual silicide concepts







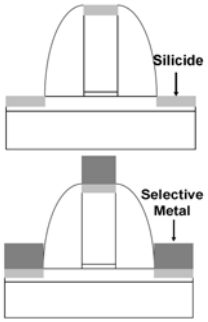


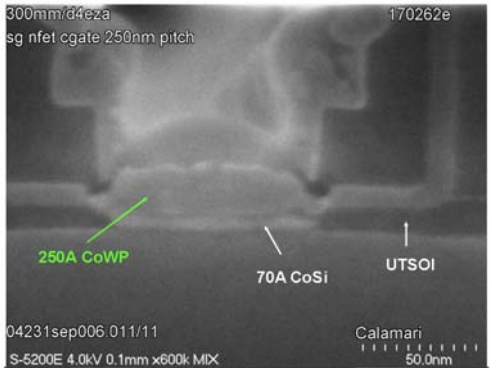


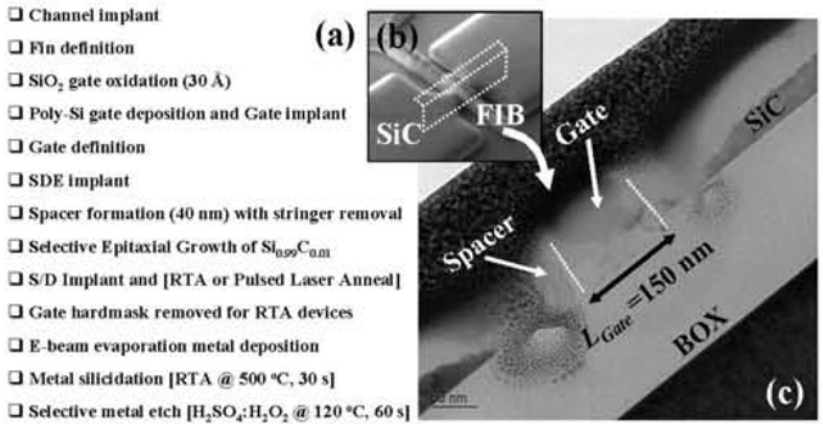
Nishi – Toshiba
IEDM 2007 [33]
Dual silicide
Pt/rare-earth segregation in NiSi/Si

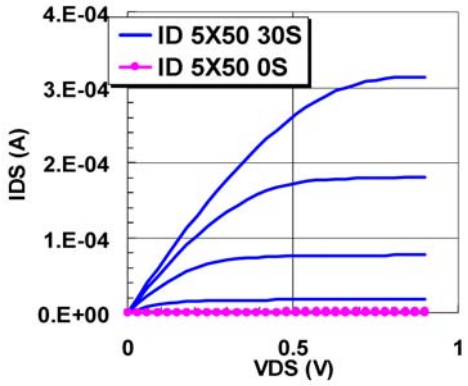
Lee – NUS-Singapore
VLSI 2008 [34]
Dual silicide
Al interdiffusion + PtSi/PtSiGe

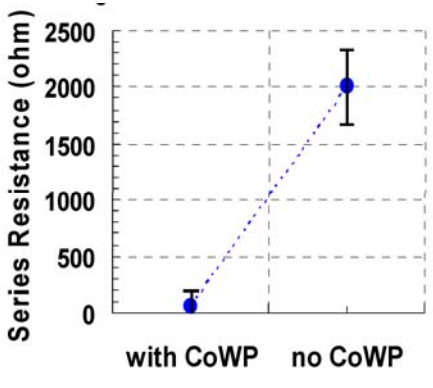
Even More Novel "Silicide" concepts

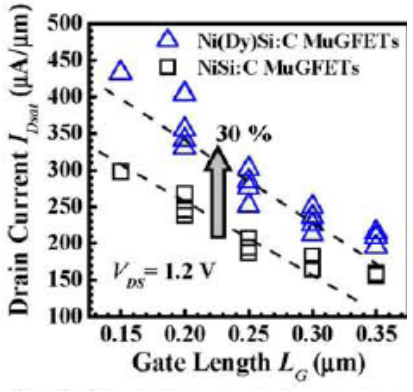


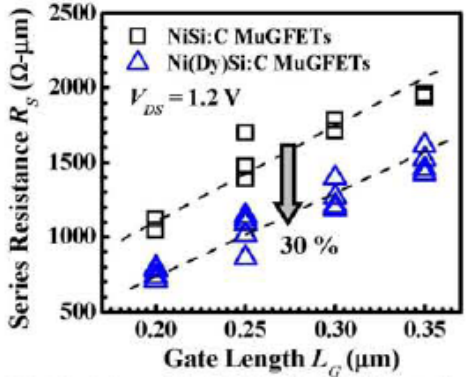










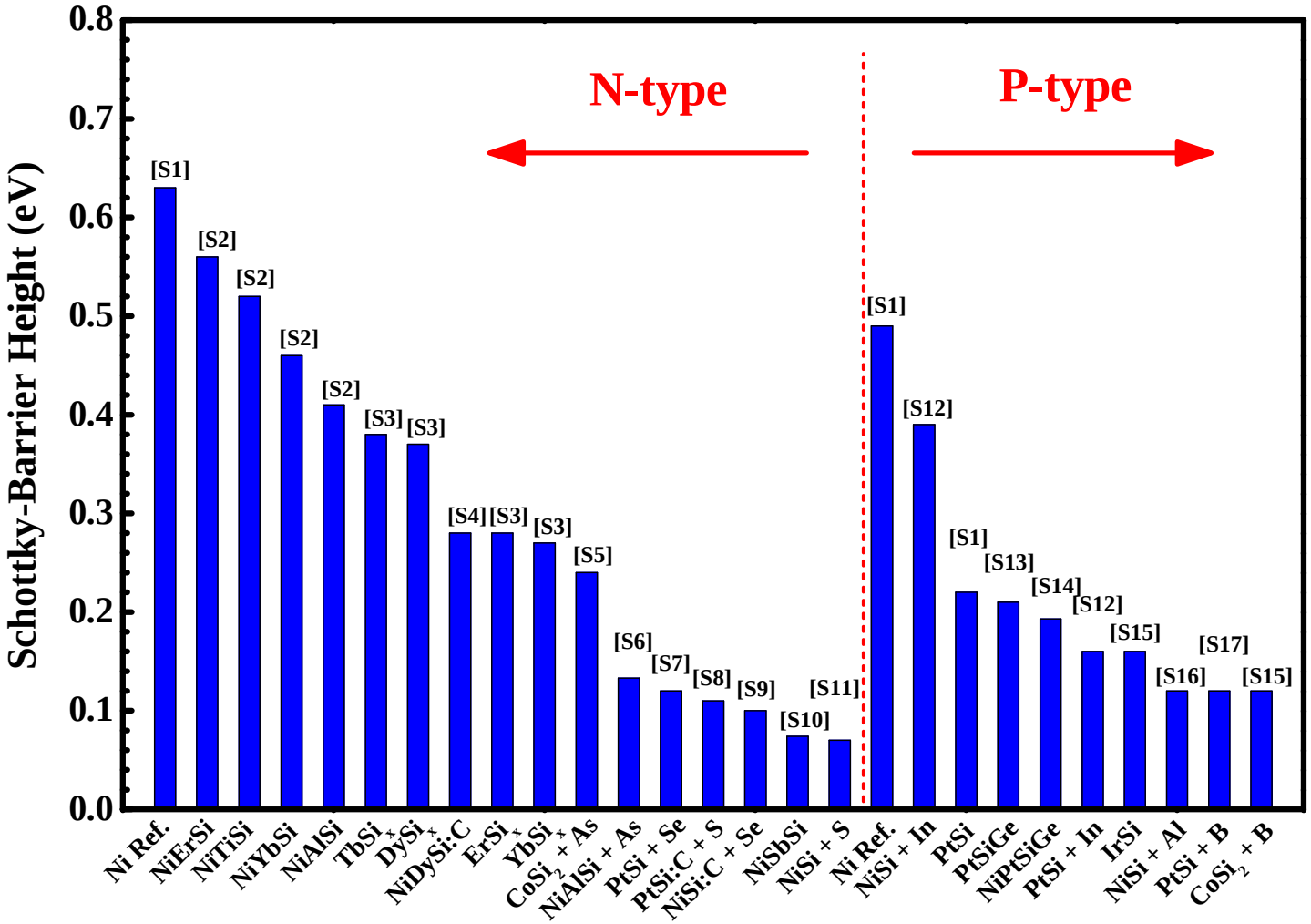


Pan – AMD/IBM
EDL 2006 [35]
Selective metal (electroless) - CoWP

Lee – NUS-Singapore
IEDM 2007 [36]
Ni(Dy)Si:C silicides + laser annealing

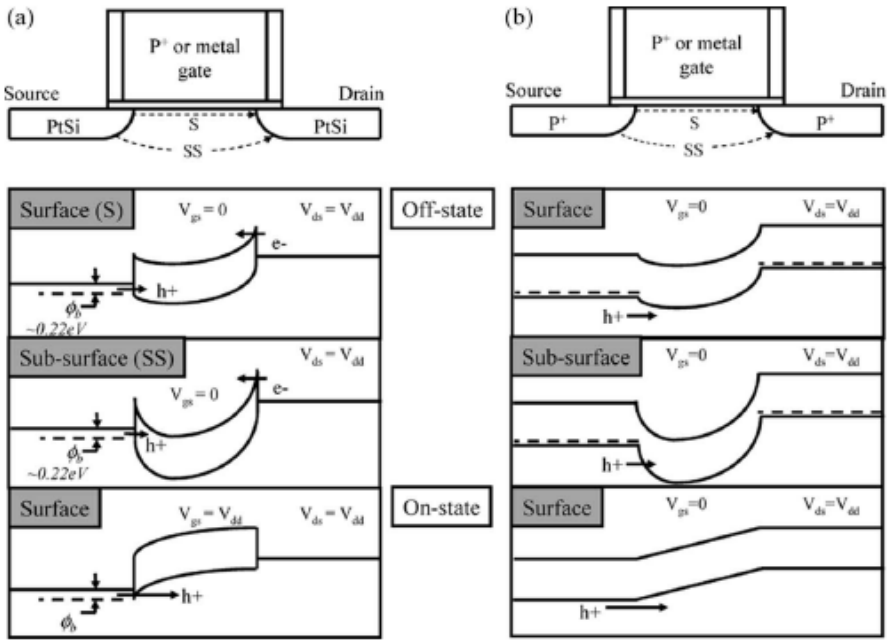
Schottky Barrier heights

Alloy and implant approaches - Lee - NUS-Singapore [37]



See special reference section on Silicides

Schottky barrier S/D – an option?

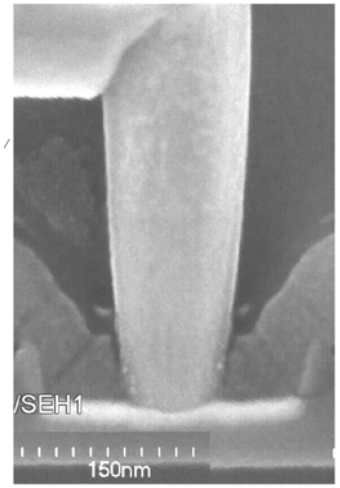


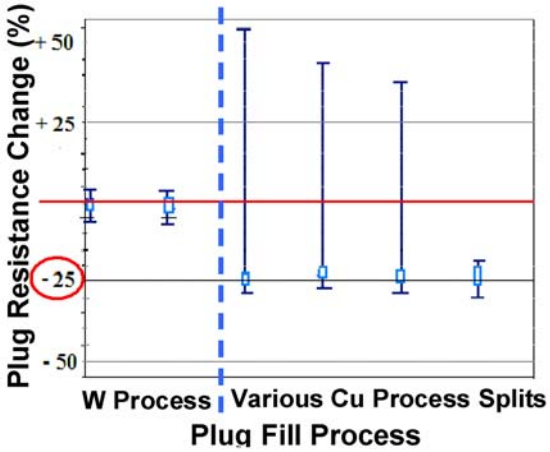
Metallic SD ***Conventional***

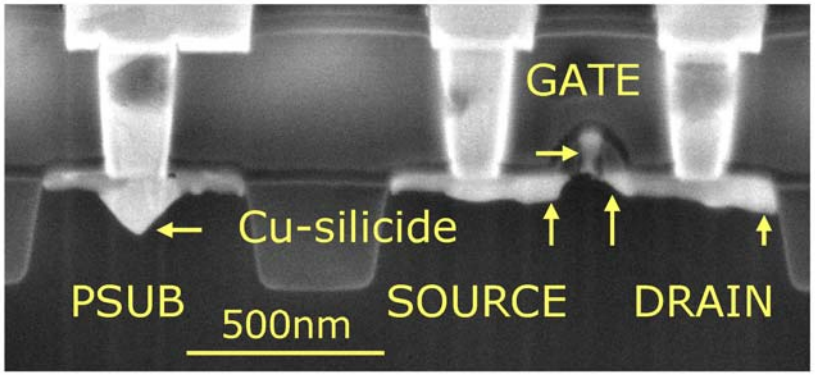
Larson – Spinnaker
TED 2006 [38]

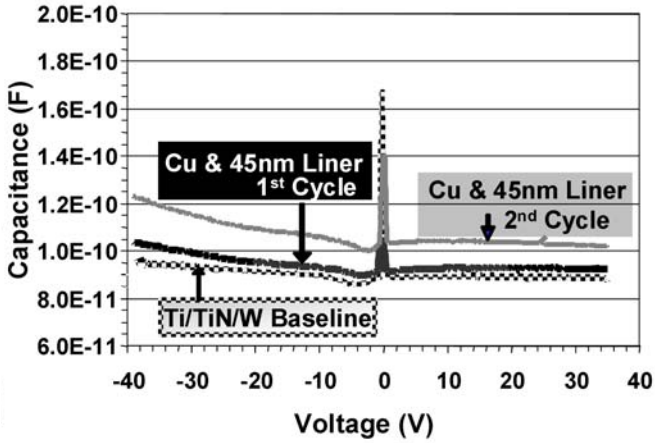
- In a metal SB-MOS, S/D forms an atomically abrupt Schottky-barrier having the height ϕb.
- Unconventional operation (field emission device in the ON state)
- Needs complementary devices (midgap silicide or two silicides)
- Channel doping concentration reduced due to the built-in SB. (Associated advantages in variability and scattering.)
- Silicide requirements are presently believed similar to low-barrier height conventional silicide requirements.

Copper Contacts

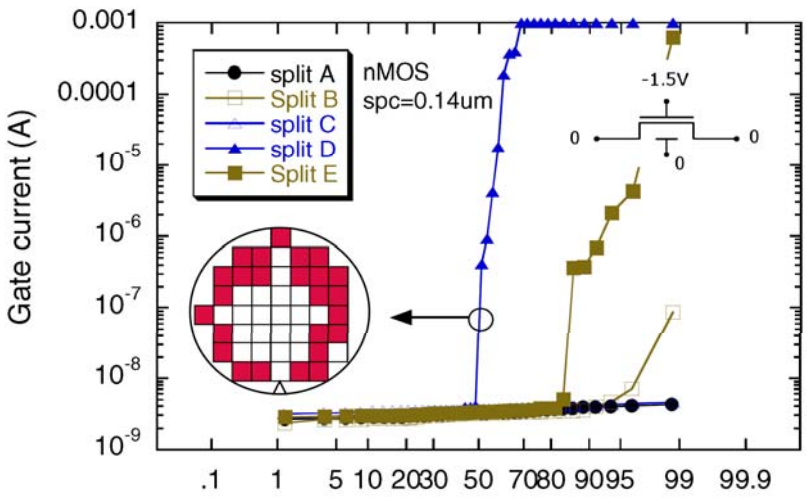








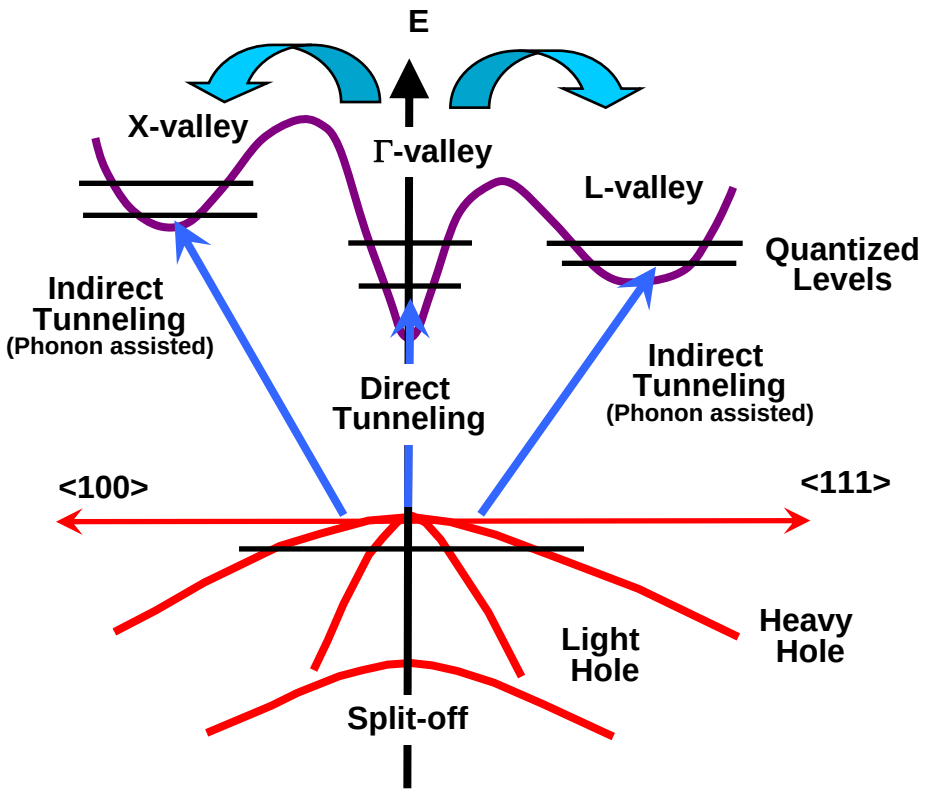
Topol – IBM
VLSI 2006 [39]
Fabrication of Cu contacts



Van den Bosch – IMEC
IEDM 2006 [40]
Challenges of Cu contacts

Mobility Enhancement
III-V/Ge

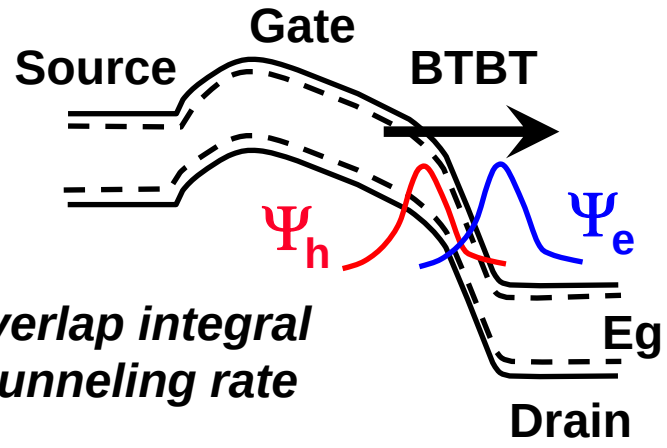
Challenges of Alternative Channel Materials



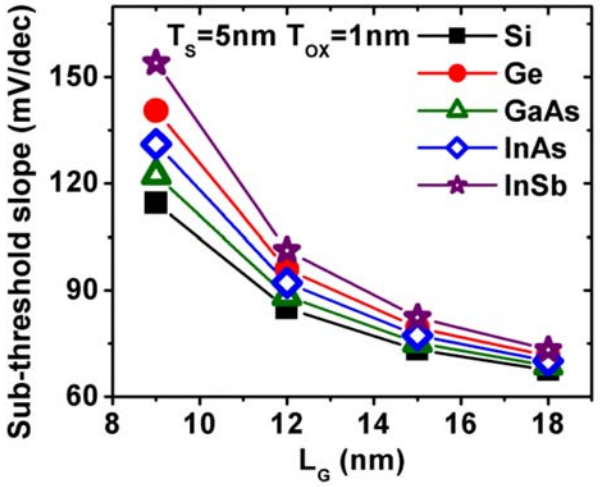
Saraswat – Stanford – IEDM 2006 [41]

- Very high mobility materials (ex: InAs, InSb) have low density of states in the Γ-valley, resulting in reduced Ion.
- At high fields, the quantized energy levels in the Γ-valley rise faster than in the L and X valleys, and thus the current is largely carried in the lower mobility L and X-valleys.

Challenges of Alternative Channel Materials



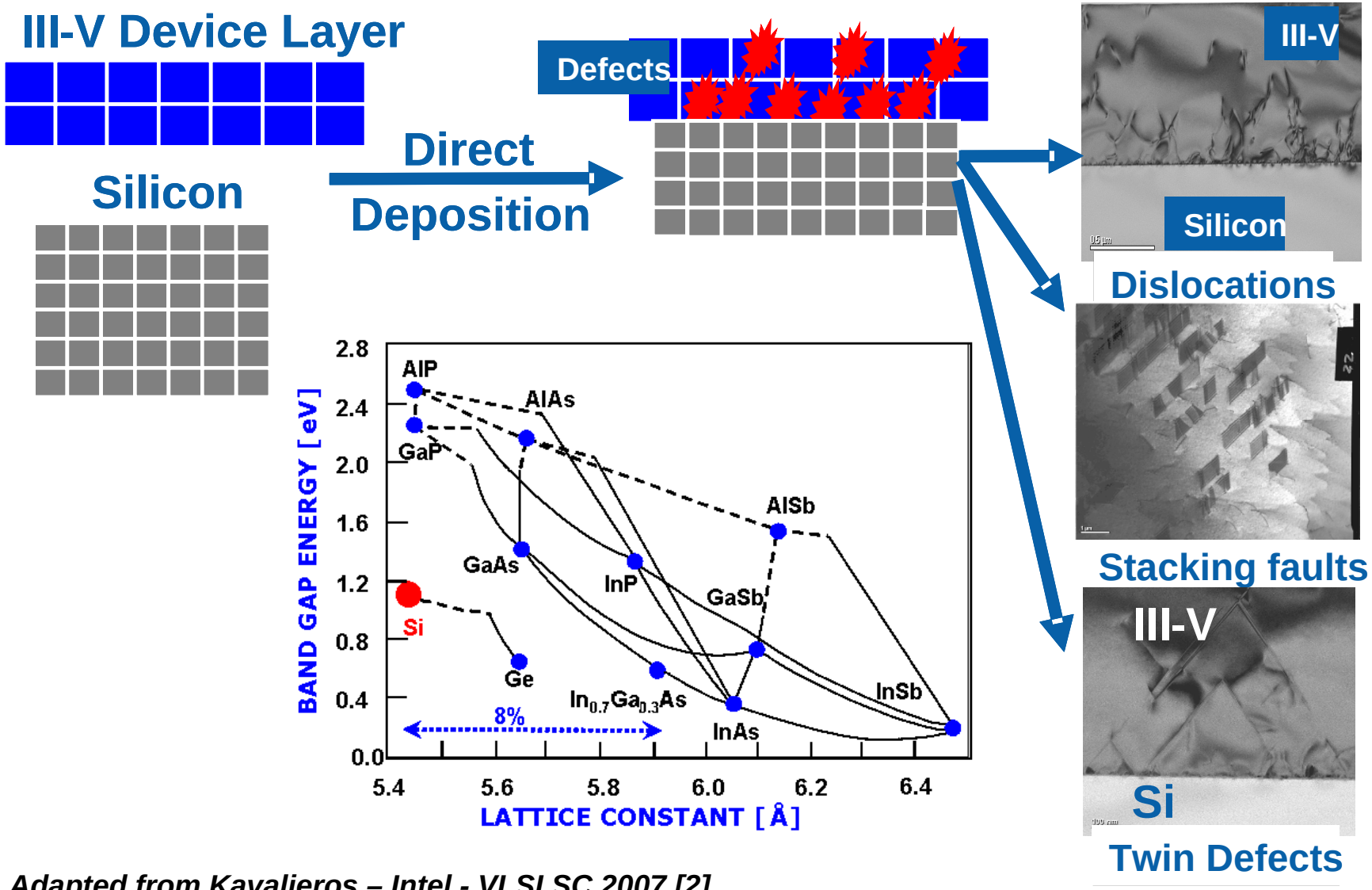
Large overlap integral
Large tunneling rate



Saraswat – Stanford – IEDM 2006 [41]

- Low Eg III-V materials (InAs, InSb) are subject to Ioff increases due to band-to-band tunneling (and the effect worsens with strain).
- Ge is more complex due to the close energy proximity of the Γ valley to the L and Δ valleys. This permits both direct and phonon assisted tunneling (and has the additional complexity of a direct/indirect tradeoff with strain (Kim [42], Krishnamohan[43])
- Higher k materials (InAs, InSb) have increased subthreshold slope.

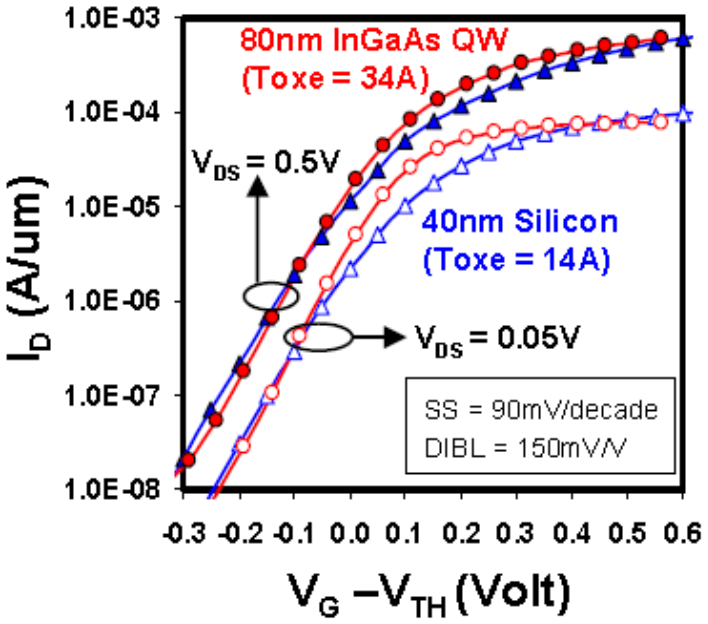
Challenge of Lattice Mismatch Issues

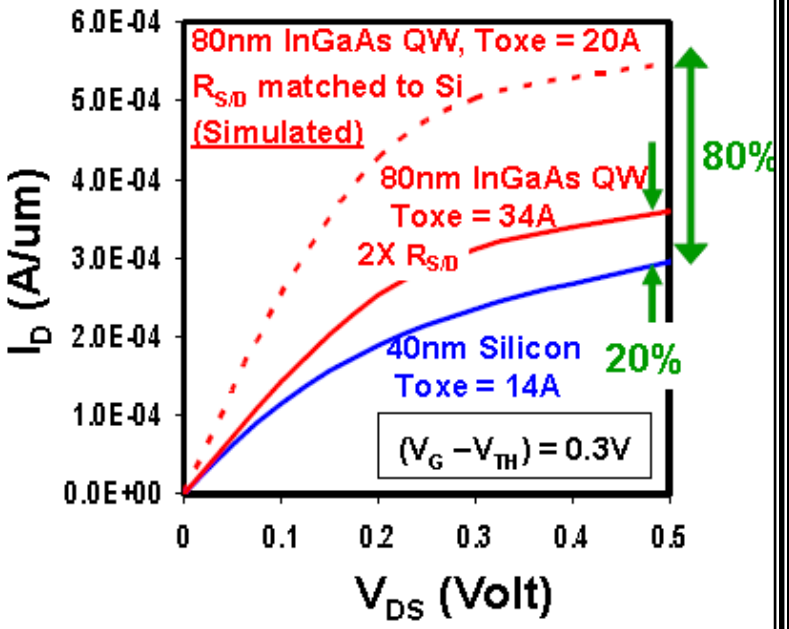


Adapted from Kavalieros – Intel - VLSI SC 2007 [2]

III-V QWFET and Si MOSFET Comparison

Actual and Simulated I_D Gains at Vcc = 0.5V





Experimental

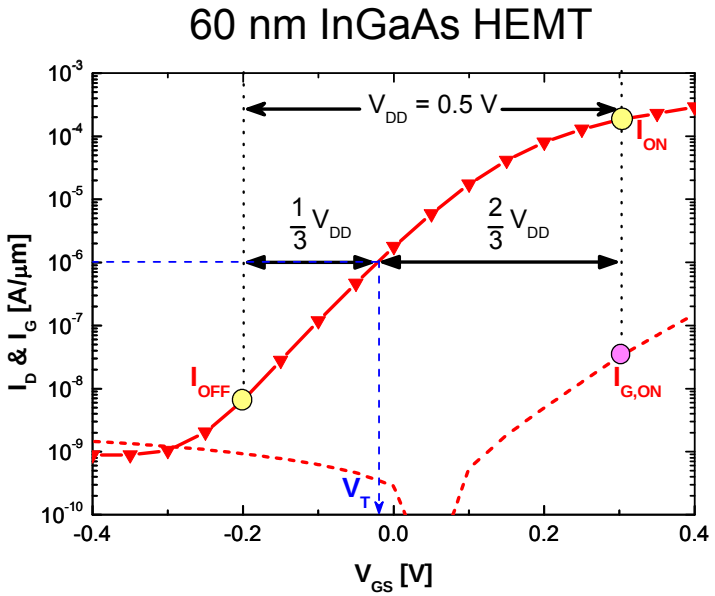
- III-V shows 20% higher drive current than Si at V_{DS} = 0.5V despite thicker Toxe and 2X larger $R_{S/D}$

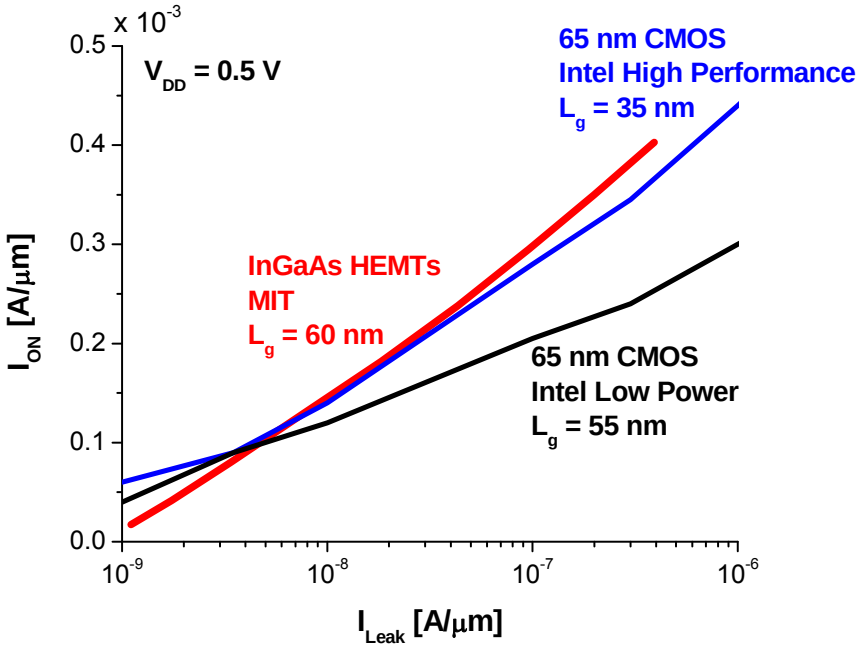
Simulation

- III-V shows 80% higher drive current than Si at V_{DS} = 0.5V when Toxe is reduced and $R_{S/D}$ matched to Si

R. Chau – Intel – ESSDRC / EDL 2008 [44]

Benchmarking Against Si MOSFET: I_{on} vs. I_{off}





$$I_{leak} = \frac{1}{2} \times (I_{OFF} + I_{G,ON})$$

InGaAs data: Kim, IEDM 2006

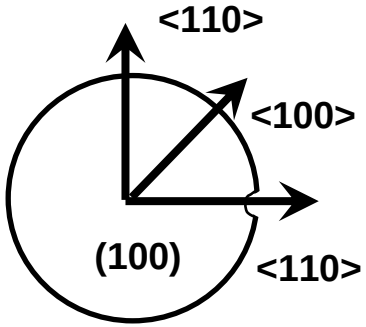
Si data: courtesy of Antoniadis

60 nm InGaAs HEMT outperforms 65 nm CMOS at V_{DD}=0.5 V

Alamo – MIT – IEDM SC 2007 [45]

Mobility Enhancement Orientation

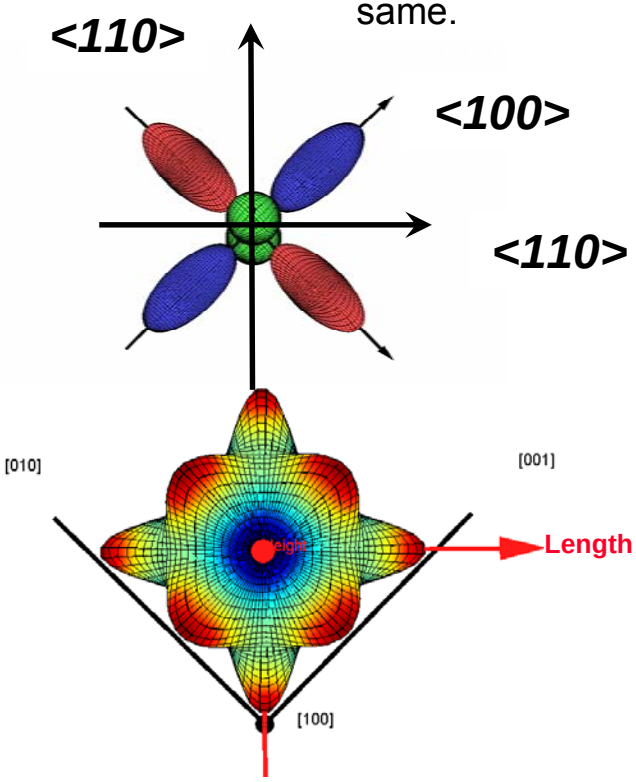
(100) surface – top down



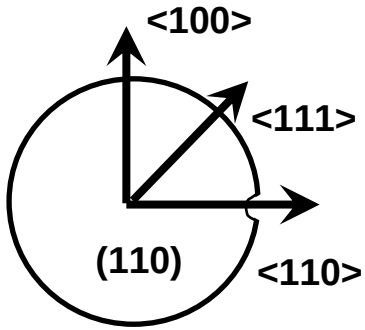
Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a “45 degree” wafer)

Both <110> directions are the same.



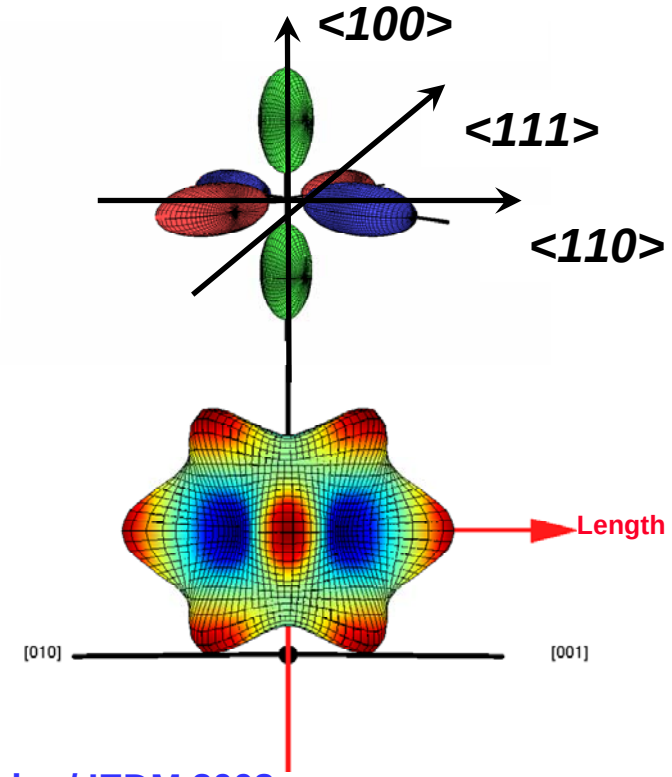
(110) surface – top down



Non-standard

(110) Surface

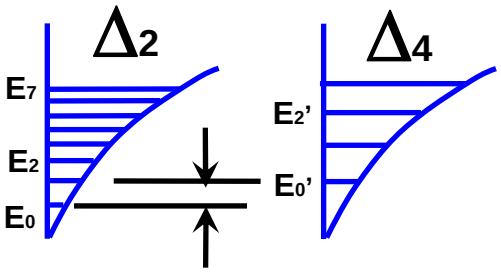
Three possible channel directions
<110> <111> and <100>



MASTAR [46]

Kelin Kuhn / IEDM 2008

Quantization Effects in MOSFETs



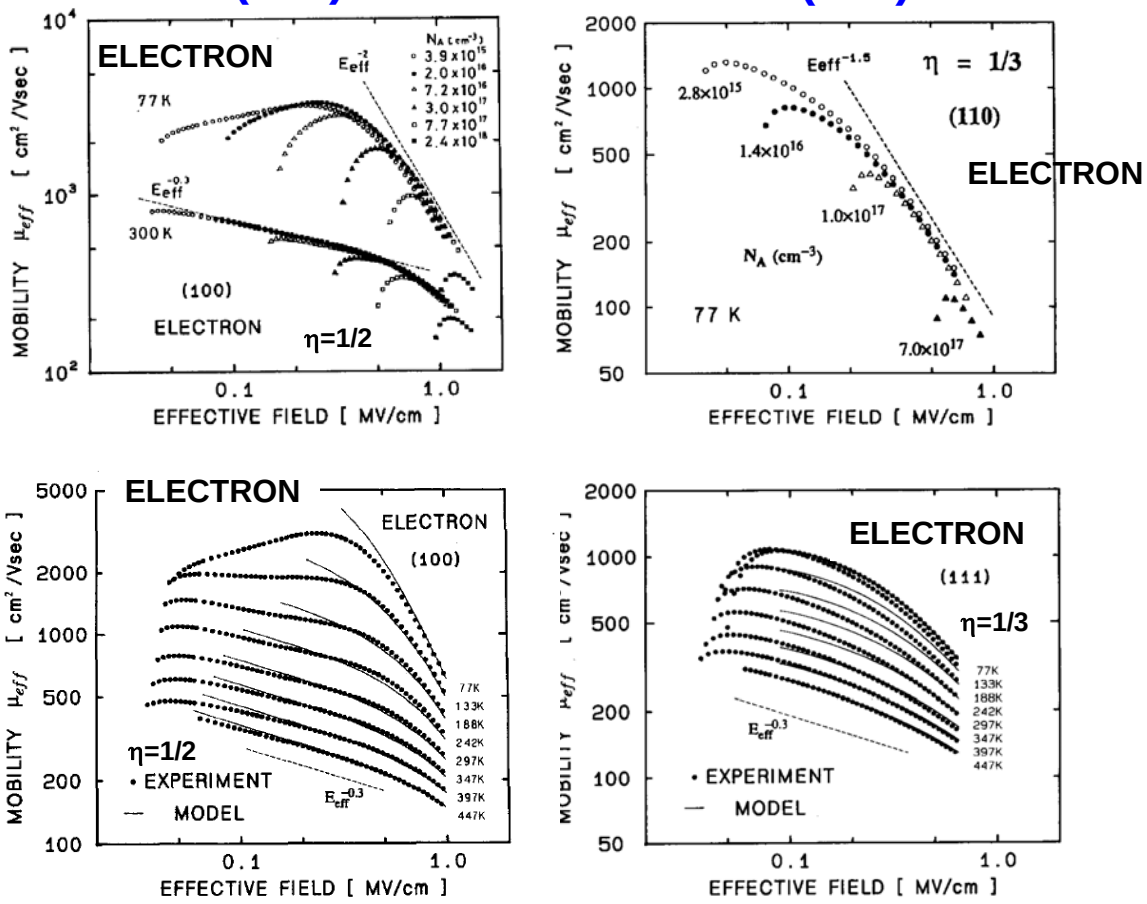
$\Delta E = (\Delta E'_0 - \Delta E_0)$

Unstrained

INVERSION LAYER

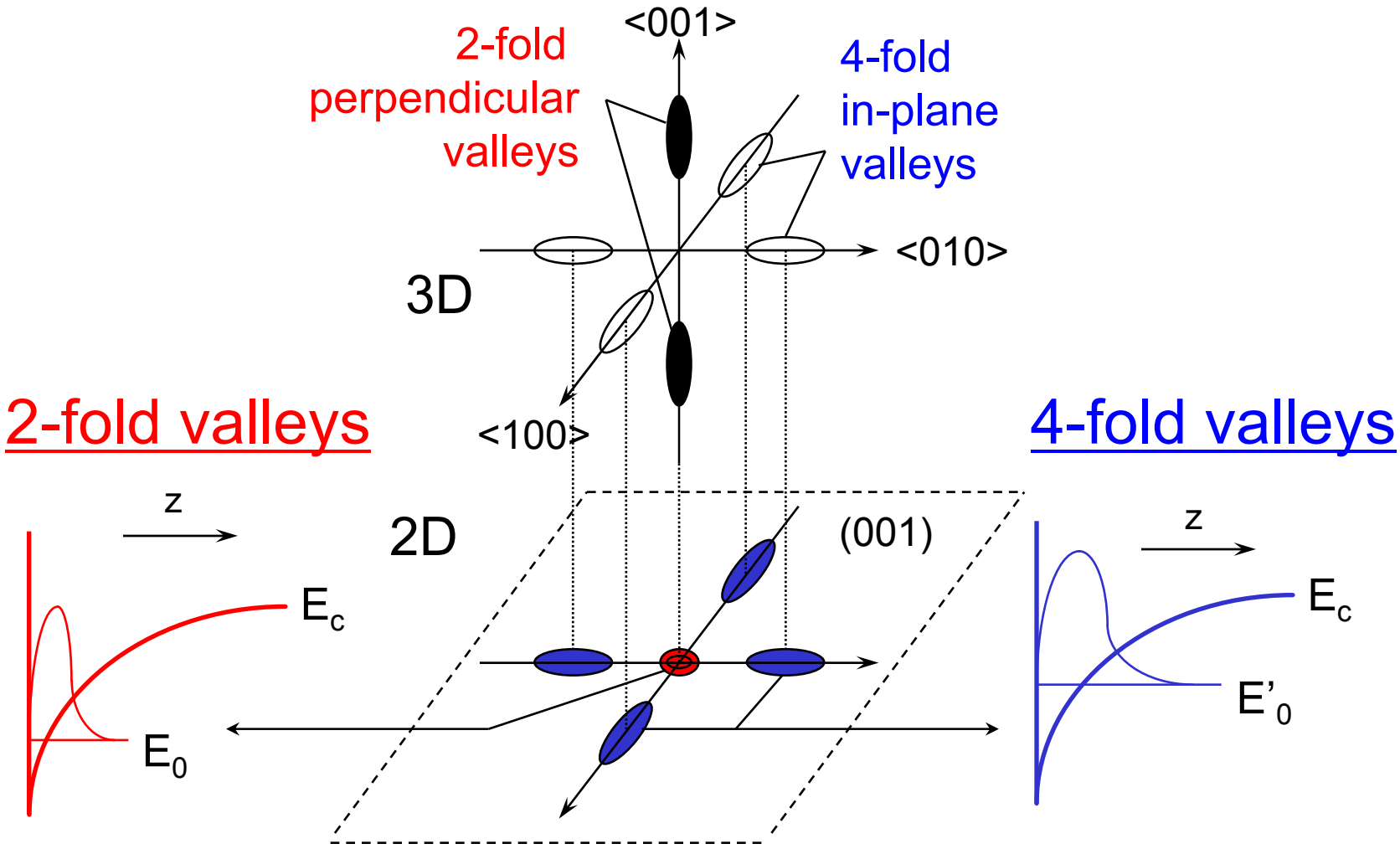
Takagi – Stanford
JAP 1996 [47]

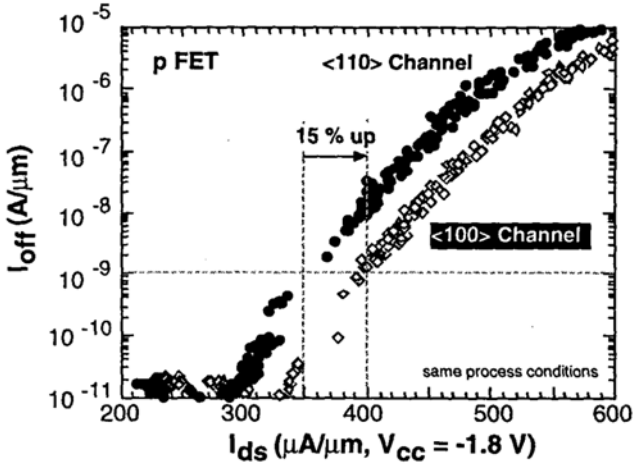
(100) **(110)**

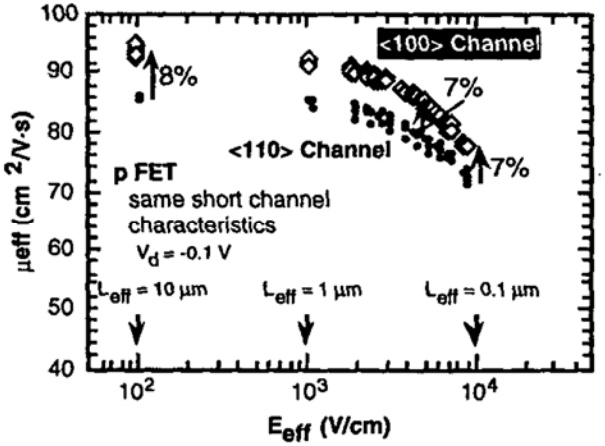


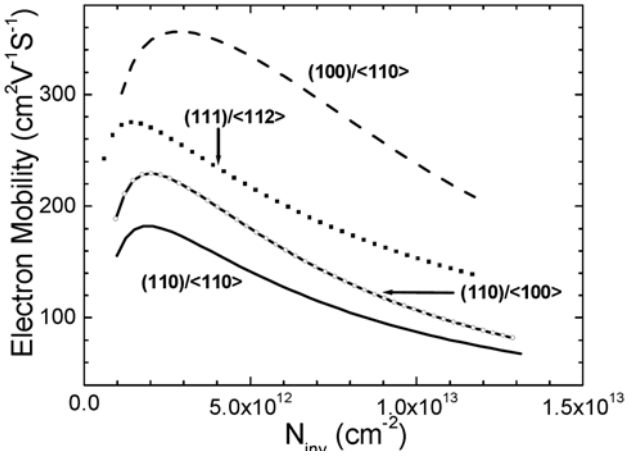
Takagi – Toshiba
TED 1994 [48-49]

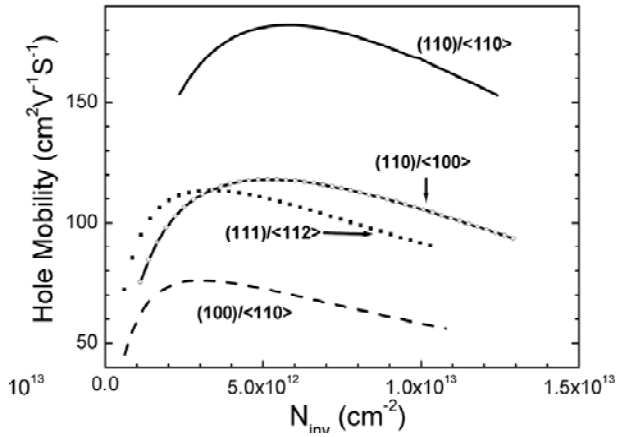
Subband Structure of (001) surface Si MOS inversion layers (from S. Takagi [50])











On (100) surface (no strain)

PMOS best is (100) <100>

NMOS ~isotropic

Sayama – Mitsubishi - IEDM 1999 [51]

On (110) surface (no strain)

NMOS best (110) <100>

PMOS best (110) <110>

NOTE: PMOS not good (110) <100>

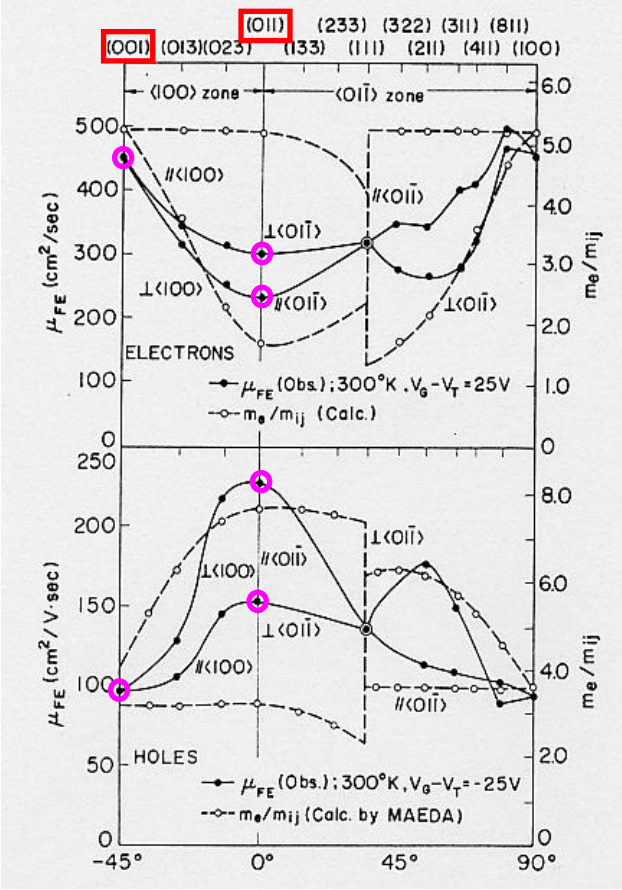
Yang – IBM – IEDM 2003 [52]

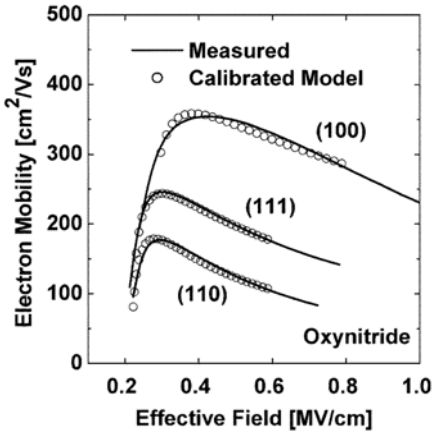
OVERALL BEST?

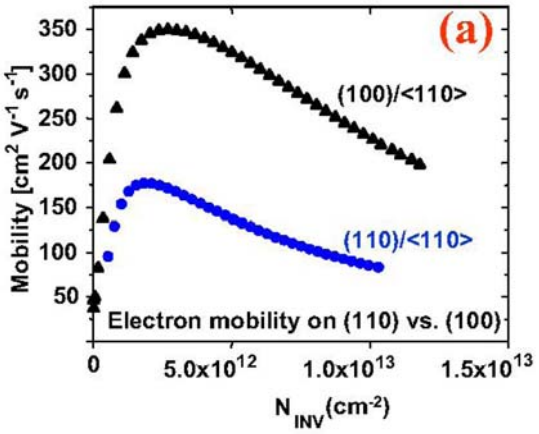
(100) and (110) comparisons (no strain)
NMOS (100) <110>, PMOS (110) <110>

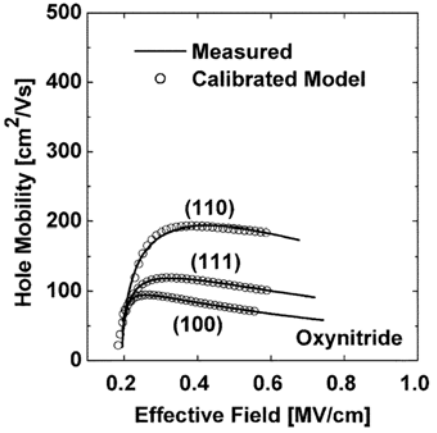
electron

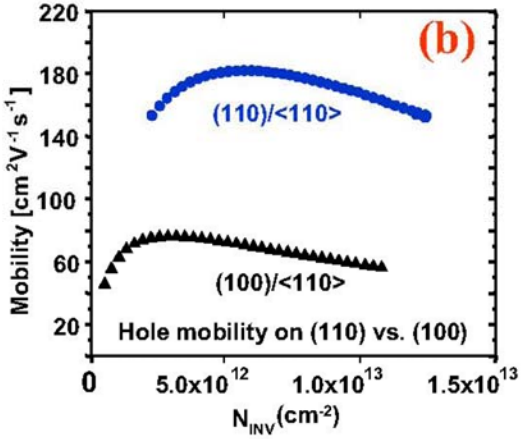
hole









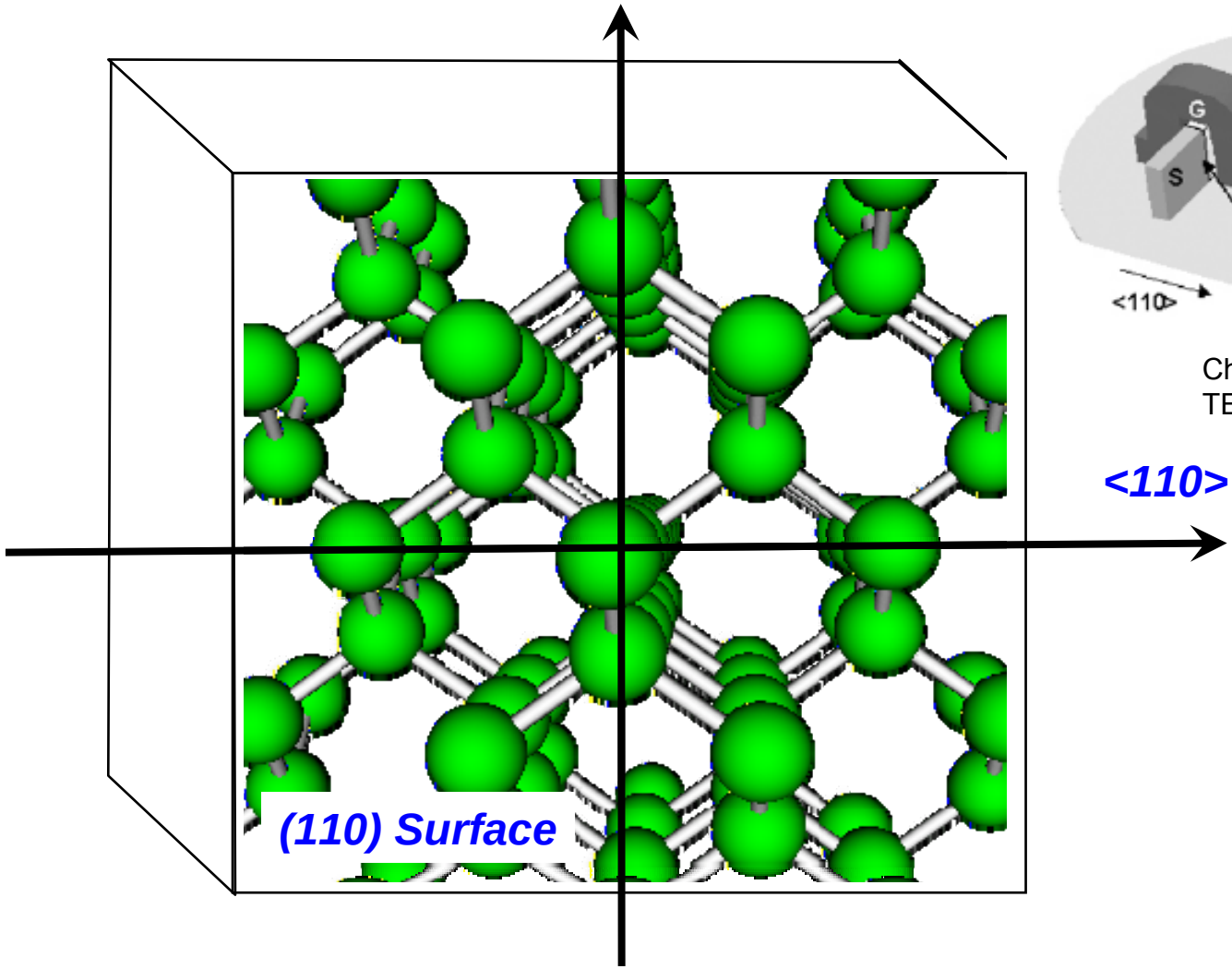


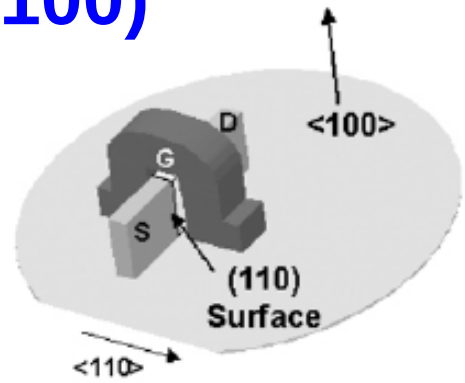
Sato [53]
Phys. Rev. (1971)

Chang - IBM
TED 2004 [54]

Yang – AMD/IBM
EDST 2007 [55]

PMOS VERTICAL DEVICES on (100)





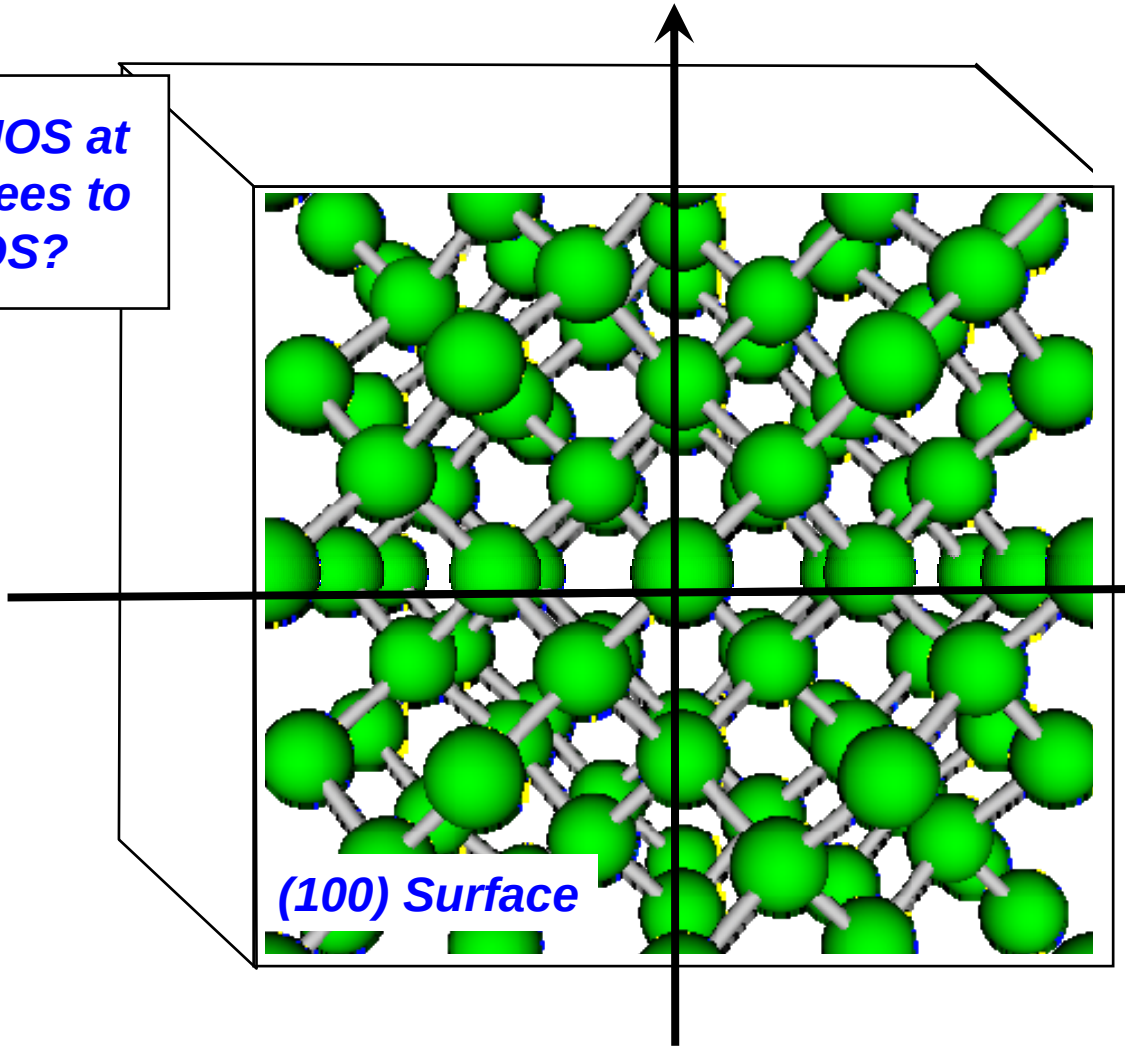
Chang - IBM – TED 2004 [54]

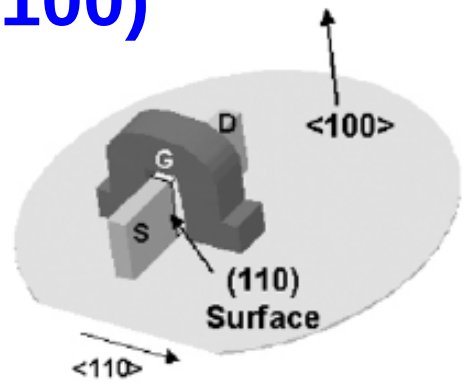
<110> channel

(110) surface <110> channel results when a VFET is fabricated on typical (100) Si - good for PMOS, not for NMOS

NMOS VERTICAL DEVICES on (100)

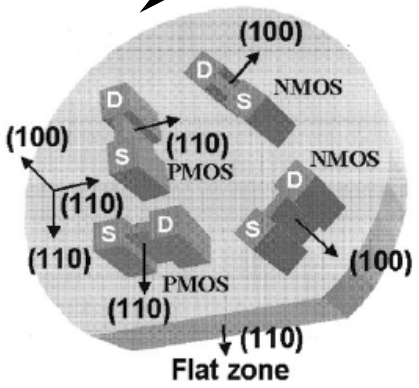
Put NMOS at 45degrees to PMOS?





Chang - IBM – TED 2004 [54]

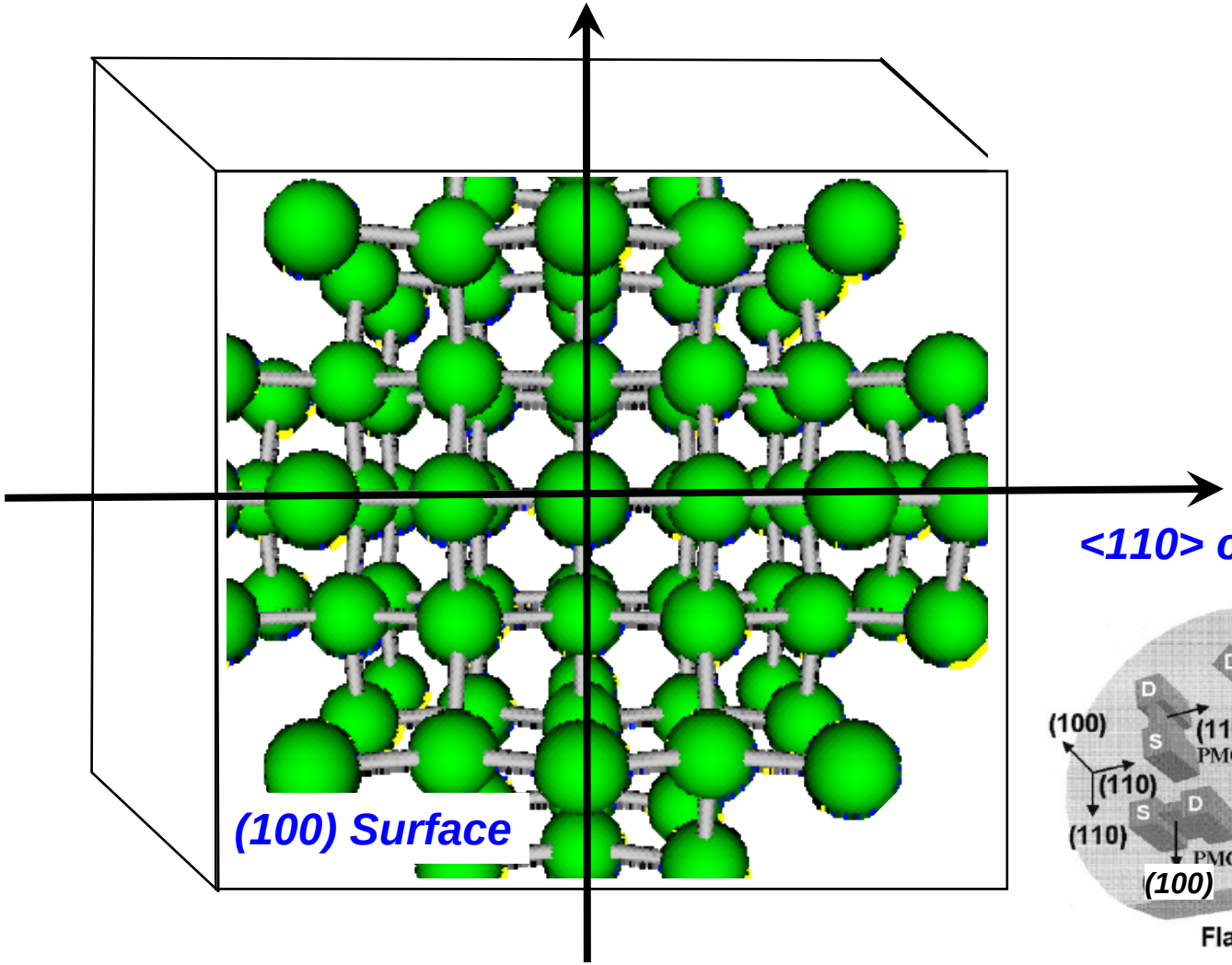
<100> channel

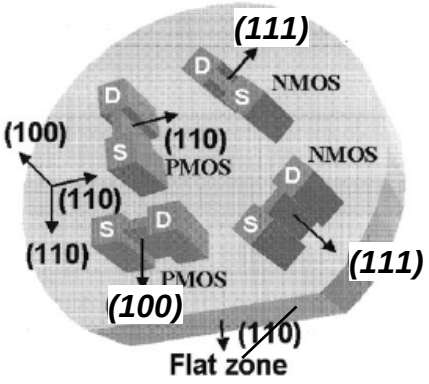


Chang - Berkeley Proc. IEEE 2003 [56]

(100) surface <100> channel for a VFET fabricated at 45 degrees on typical (100) Si – very challenging for lithography at 22nm node

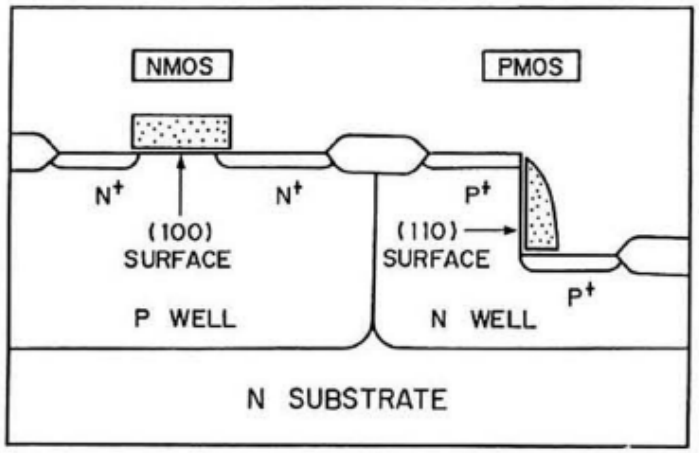
N and PMOS VERTICAL DEVICES on (110)

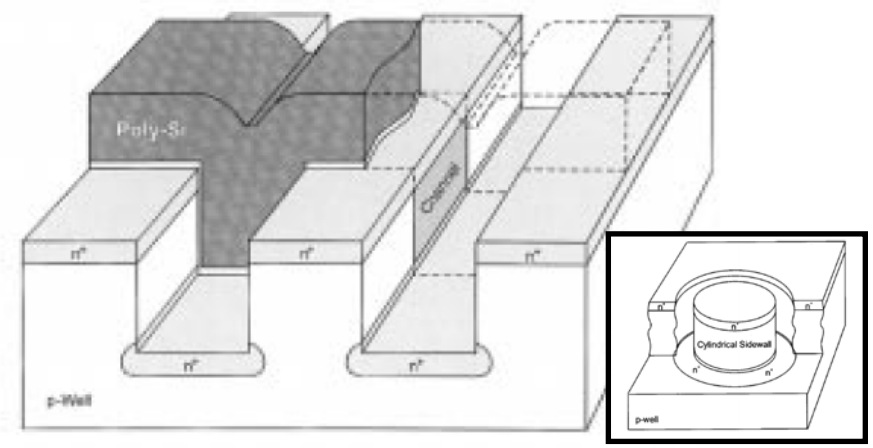


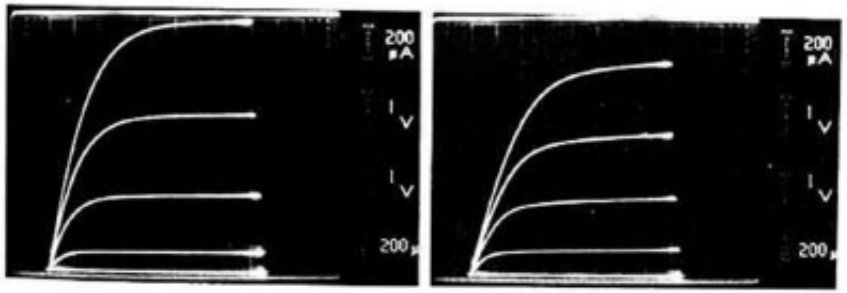


(100) <110> (good NMOS) perpendicular to (110) <100> (poor PMOS)
Both 45 degree directions are the same (111) sidewall, <111> channel

Historical VFET devices

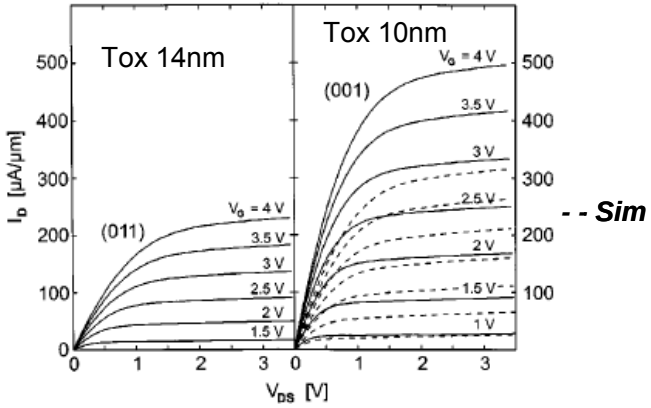






W/L(trench depth)=10/0.8

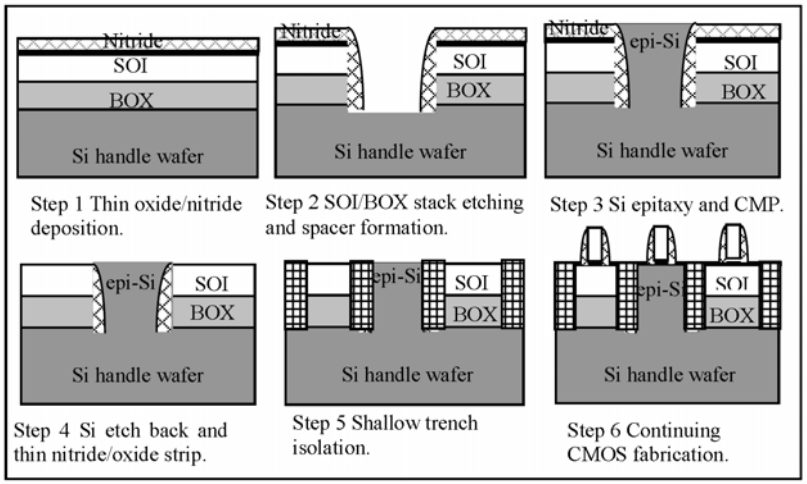
W/L(poly length)=10/0.8

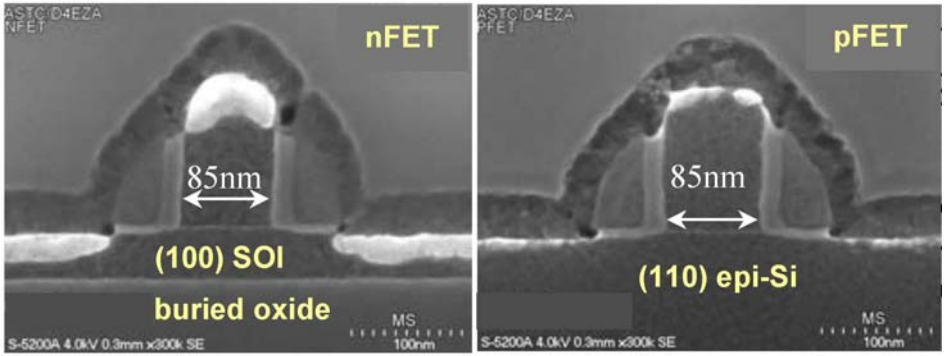


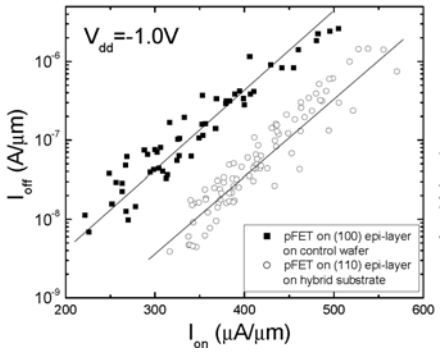
Kinugawa-Toshiba
VLSI 1986 [57]
VPFET

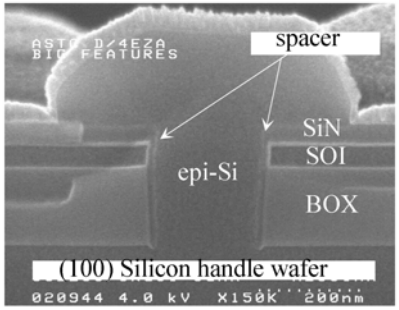
Goebel - Infineon
TED 2001 [58]
VNFET

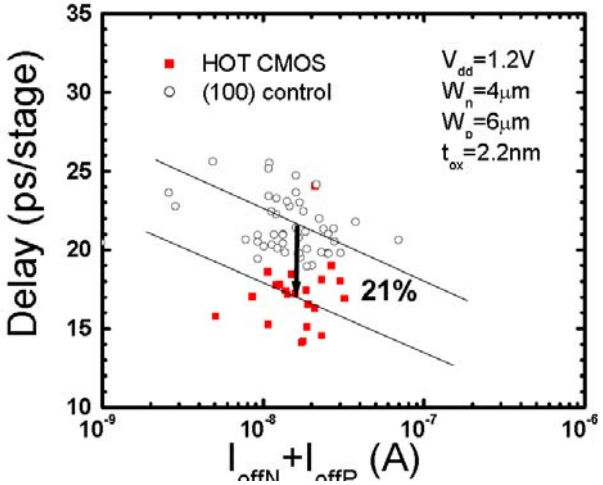
Early HOT







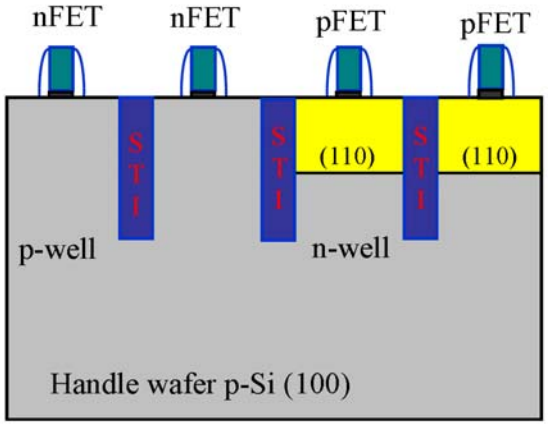


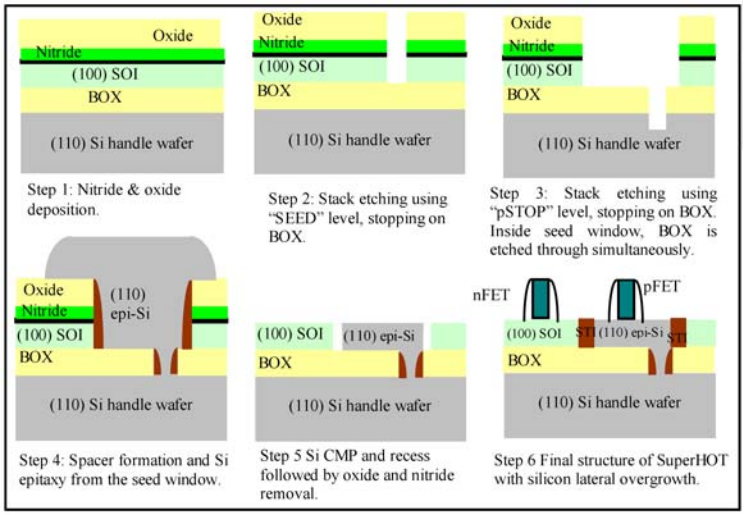


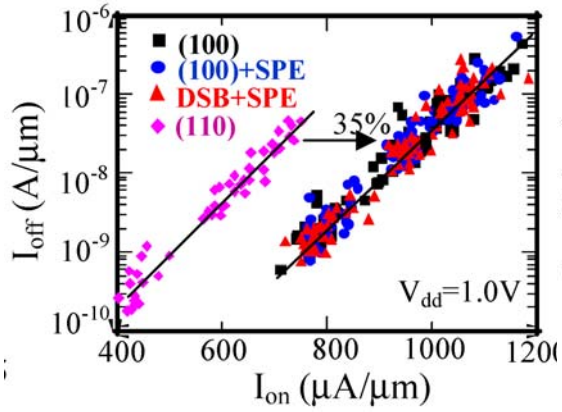
Yang – IBM
IEDM 2003 [52]
First HOT

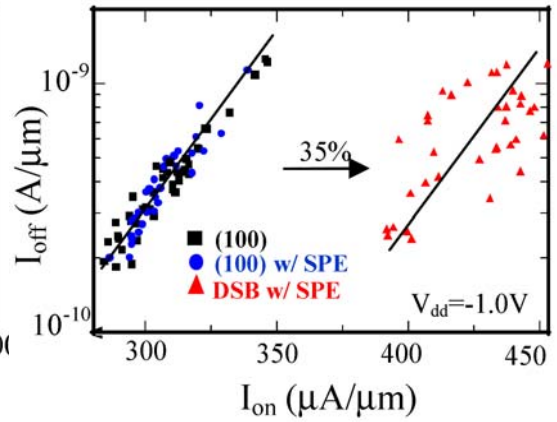
Yang – AMD/IBM
VLSI 2004 [59]
HOT RO

HOT architecture options

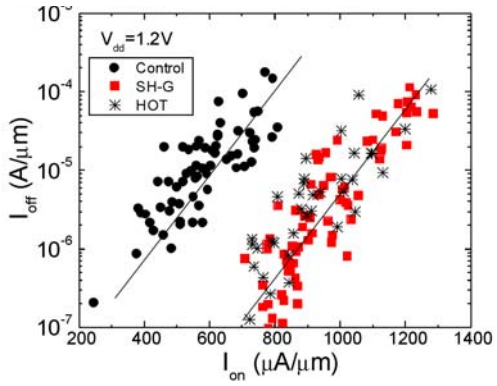






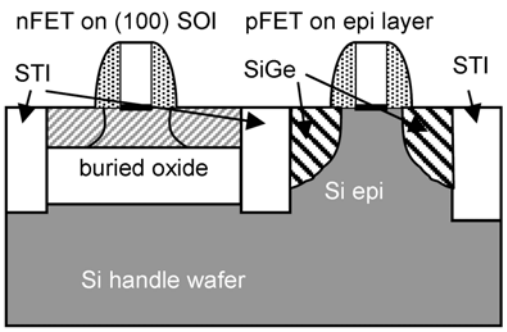


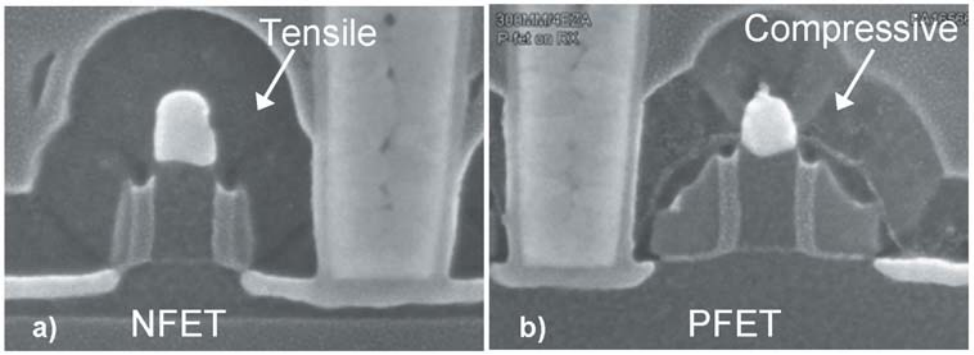
Sung – IBM
IEDM 2005 [60]
Direct silicon-bond HOT

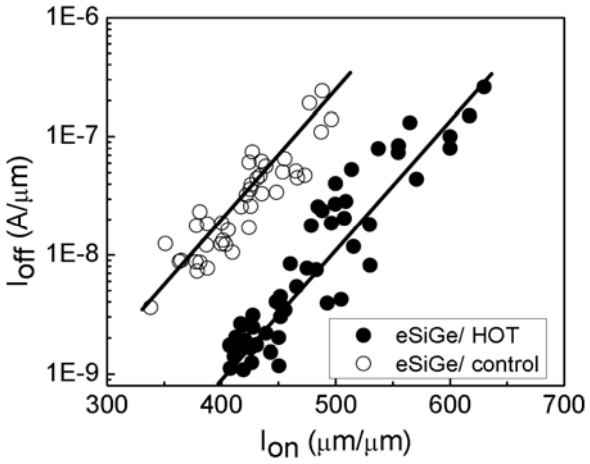


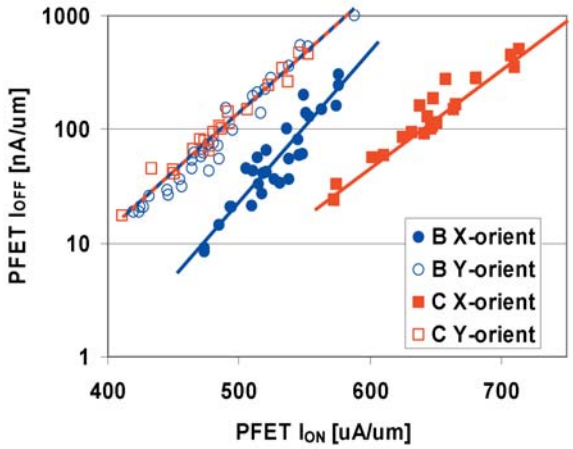
Yang – IBM
VLSI 2006 [61]
~Dual SOI HOT

HOT with strain









Surface	(001)	(110)	
Layout	X/Y	X	Y
Direction	<110>	<110>	<100>
π_L	71.8	71.8	6.6
π_V	-1.1	-66.3	-1.1
π_T	-66.3	-1.1	-1.1

Ouyang – IBM
VLSI 2005 [62]
HOT with eSiGe

Sheraw – IBM
VLSI 2005 [63]
HOT with dual stress liner

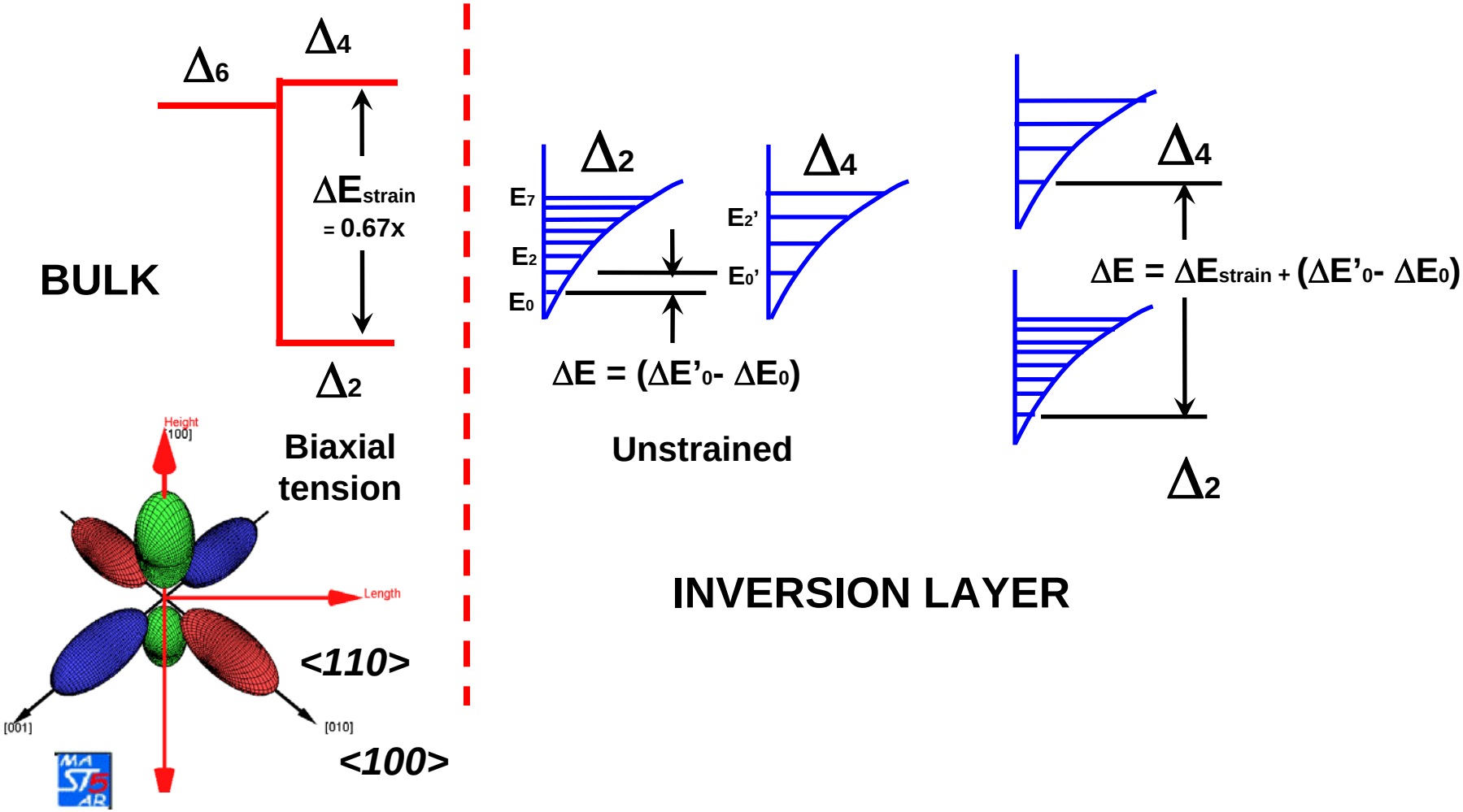
Mobility Enhancement Strain

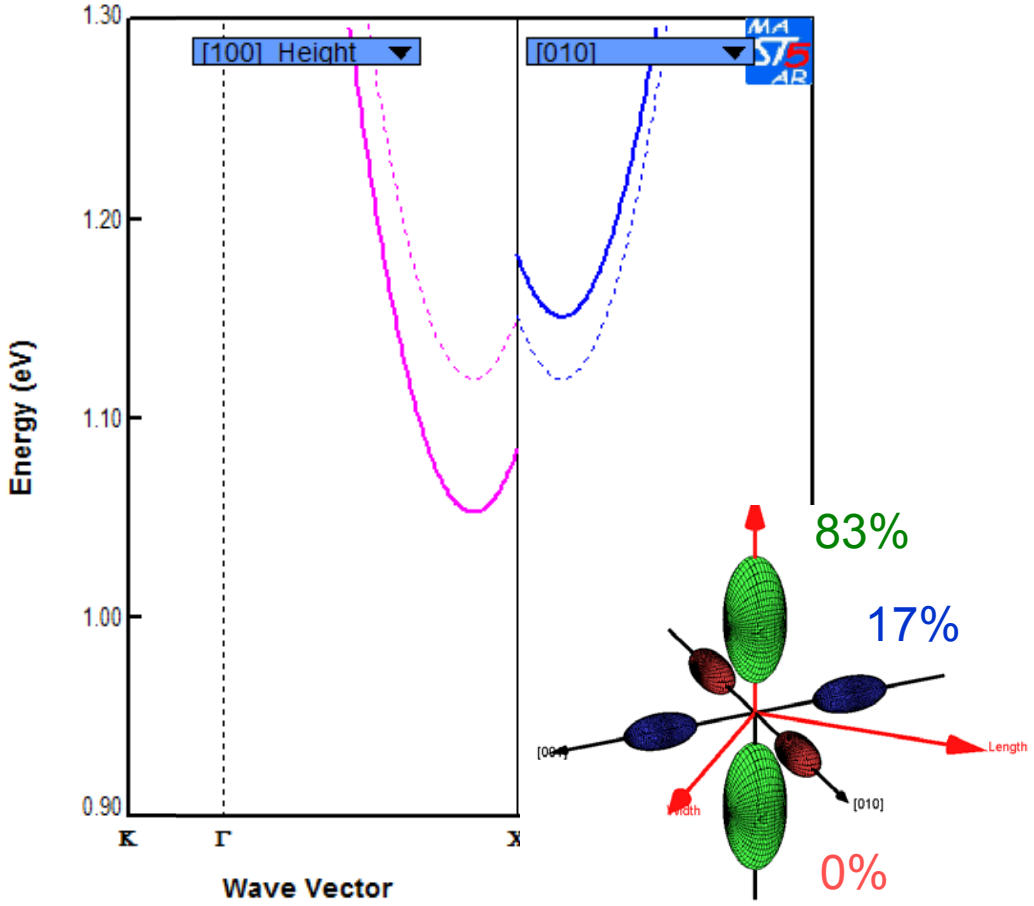
How Stress Improves Conduction

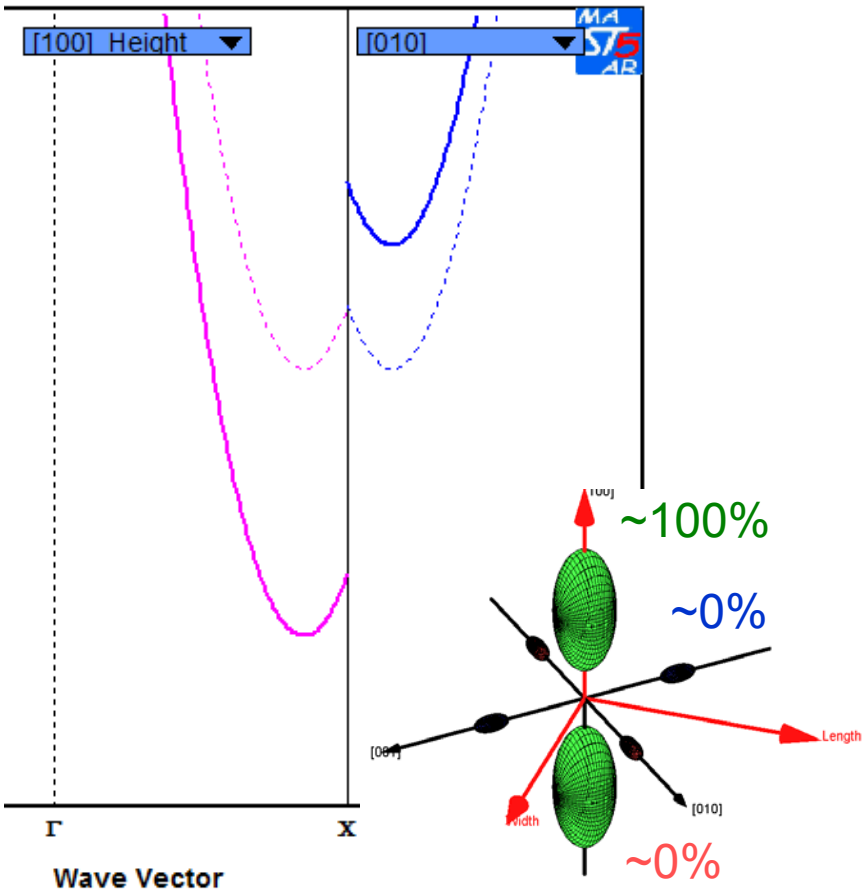
- **Reduces scattering**
  - Warps or shifts the bands to reduce the number of places carriers can go
- **Reduces effective mass**
  - Moves the carriers to places where the effective mass is lower
  - Can warp the bands to make the effective mass lower where the carriers are

Strain and Quantization Effects in MOSFETs

Takagi – Stanford – JAP 1996 [47]



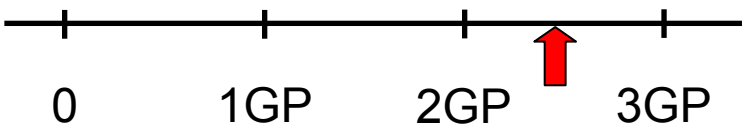




Uniaxial tension (confined)
(100) Surface: <110> channel

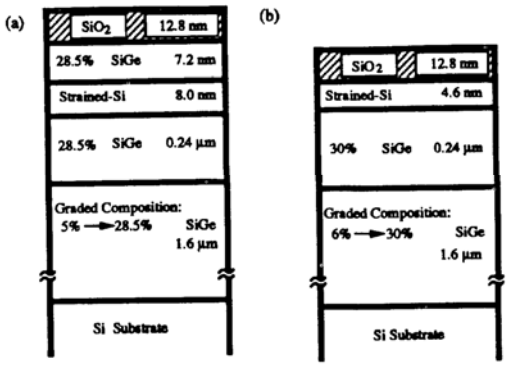
Biaxial tension (confined)
(100) Surface: <110> channel

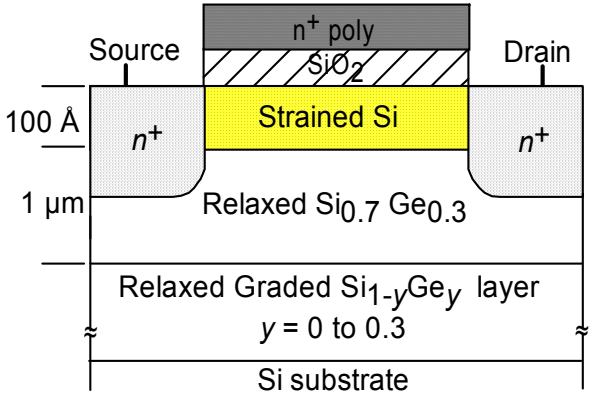
BUILD

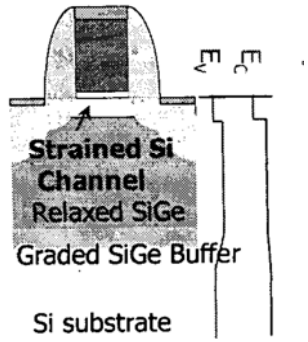


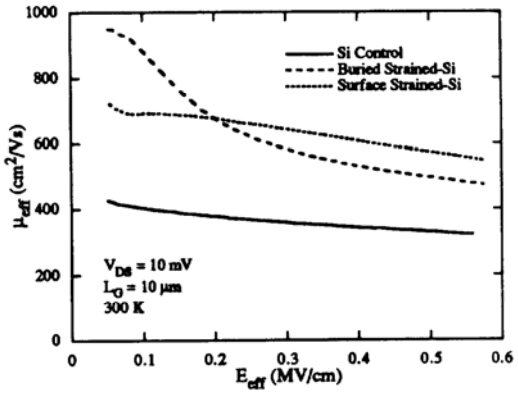
Calculated using MASTAR (http://www.itrs.net/models.html)

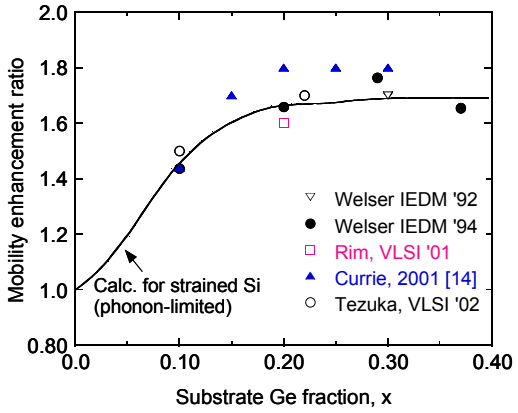
Electron mobility enhancement: Biaxial

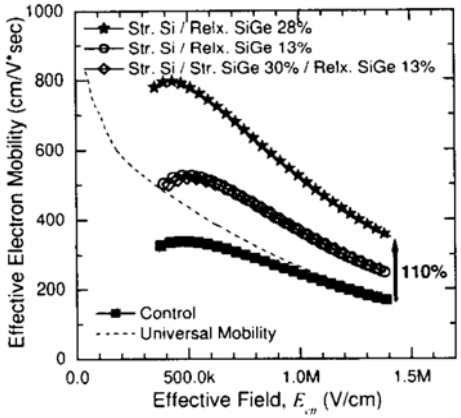












Welser – Stanford
IEDM 1992/1994 [64-65]
Strained Si/
Relaxed SiGe

Hoyt – MIT
IEDM 2002 [66]
Strained Si/
Relaxed SiGe

Rim – IBM
VLSI 2002 [67]
Strained Si/
Relaxed SiGe

NMOS band warping

CB warping occurs under shear crystal strain, is zero for biaxial case

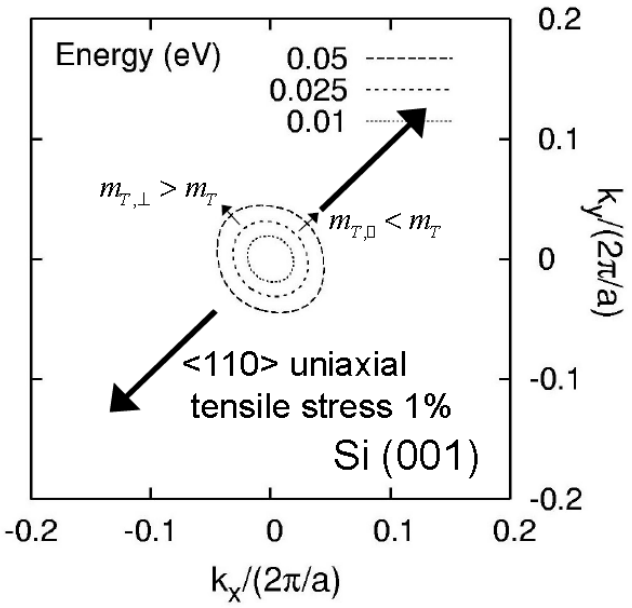


Fig. 14: Energy contour of 2-fold valleys under 1% uniaxial <110> stress. The energy surface is warped.

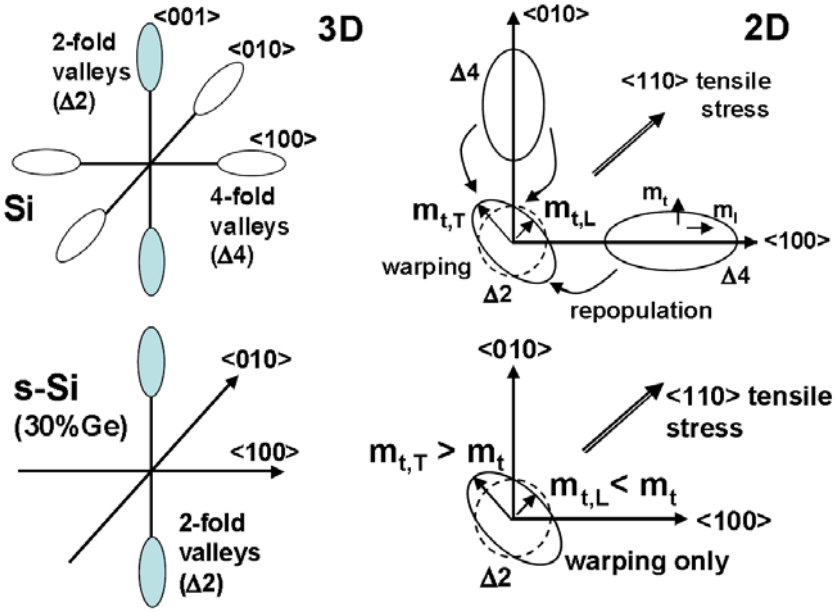


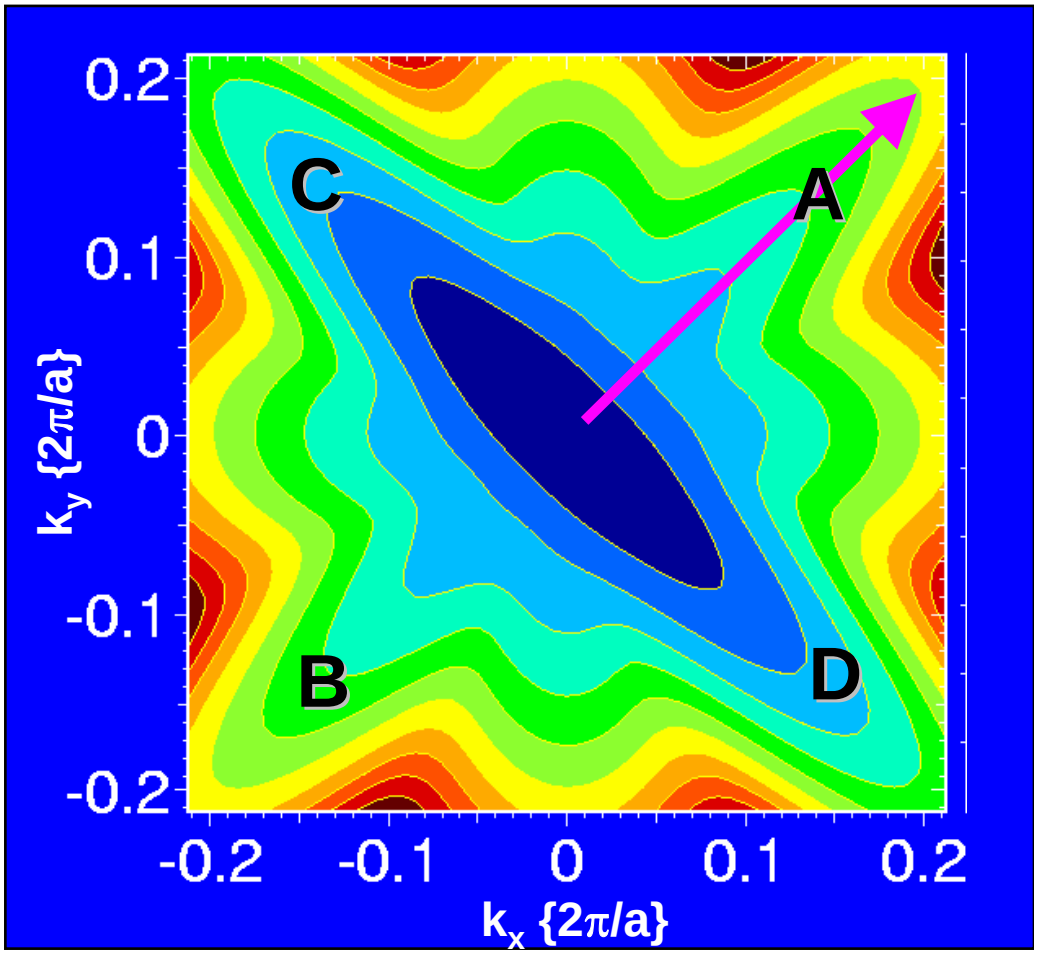
Fig.6 μ_e gain mechanisms in Si and s-Si under <110> stress. In s-Si, due to the initial biaxial strain, only Δ2 valleys are populated. μ_e gain in s-Si is then directly representative of effective mass changes of Δ2.

Uchida – Toshiba/Stanford
IEDM 2005 [68]
Band-warping in NMOS

Weber – U of Tokyo
IEDM 2007 [69]
Band-warping in NMOS

Uniaxial Stress along <110>

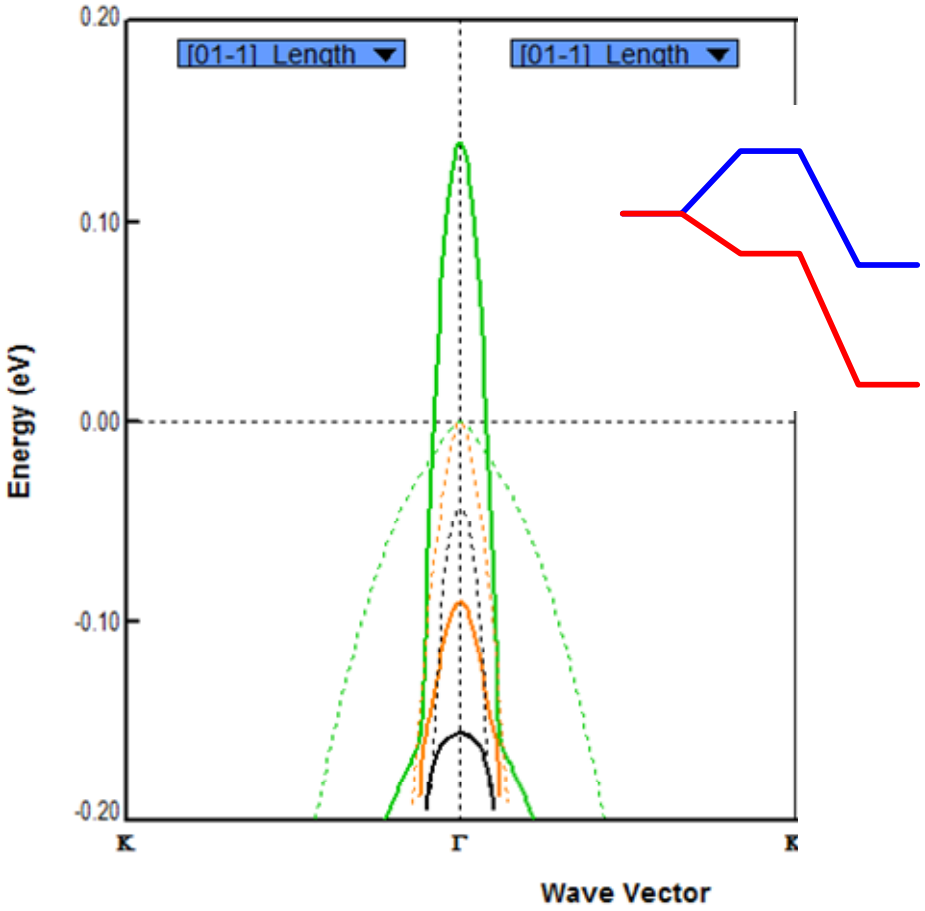
- Uniaxial stress along <110> has shear and biaxial components
- Shear compression lowers the energy of (C,D)
- Holes redistribute from (A,B) to (C,D)
- The effective mass and density of states (DOS) for scattering are reduced

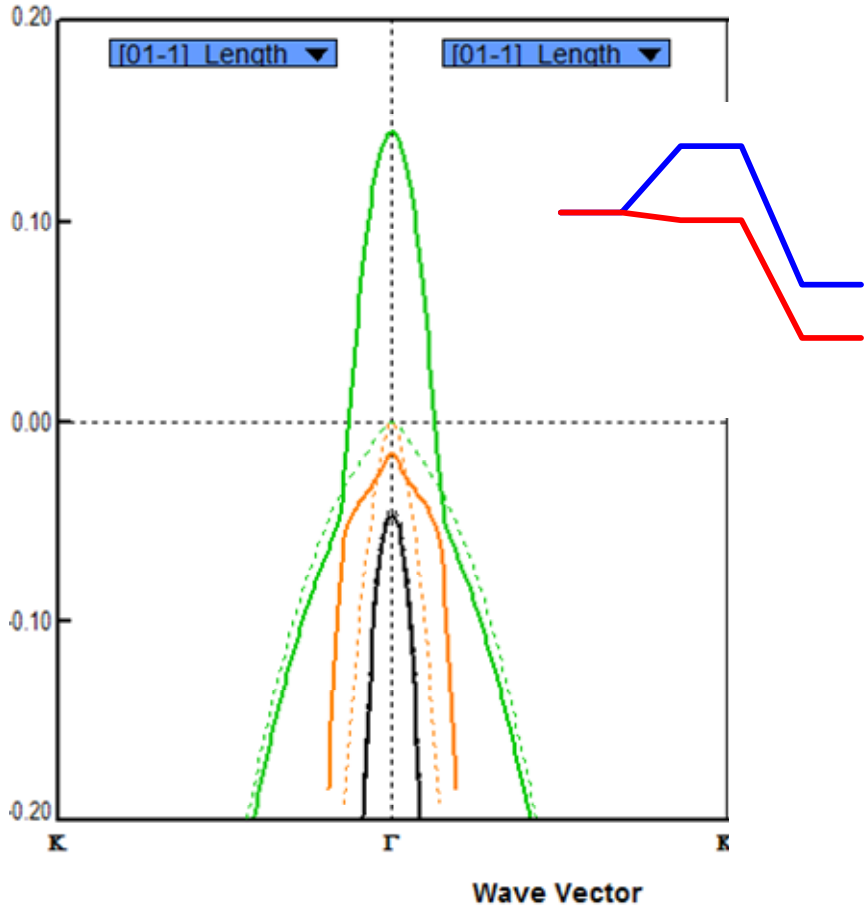


1GPa uniaxial stress along [110], (001) surface, 1MV/cm effective field, 30meV energy contours

Wang – Intel - TED 2006 [70]

Calculated using MASTAR (http://www.itrs.net/models.html)

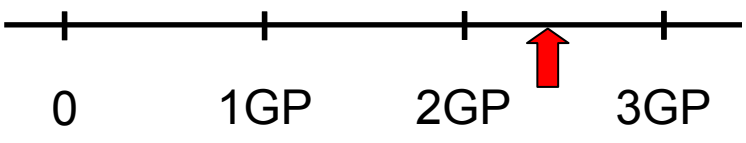




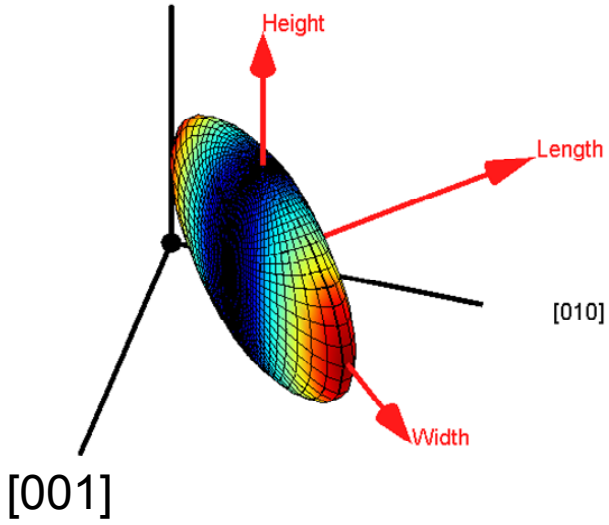
Uniaxial compression
(100) Surface: <110> channel

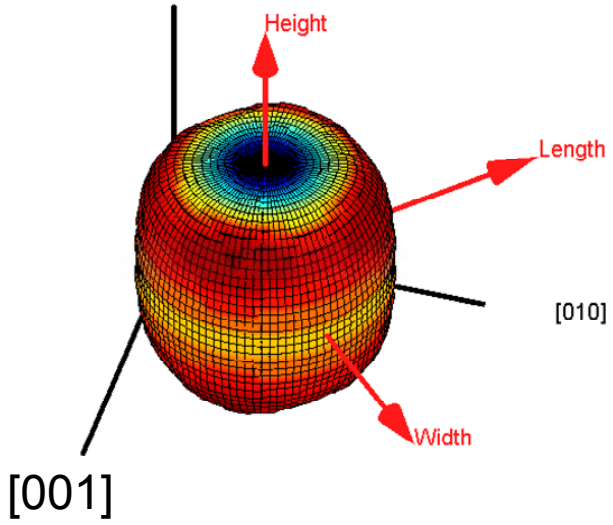
Biaxial tension
(100) Surface: <110> channel

BUILD



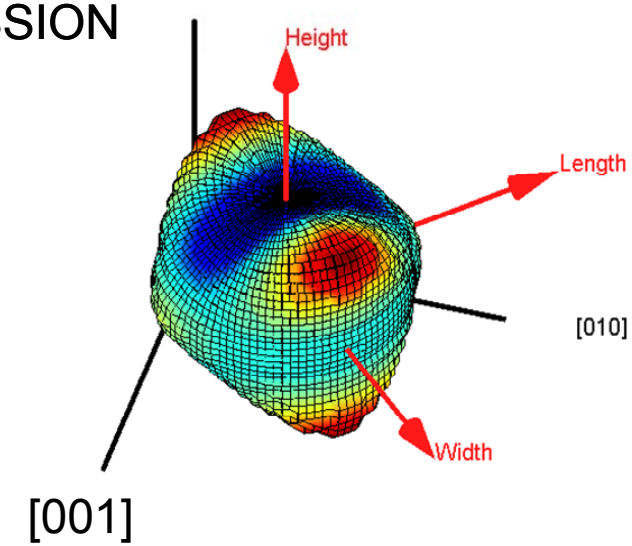
Calculated using MASTAR (http://www.itrs.net/models.html)



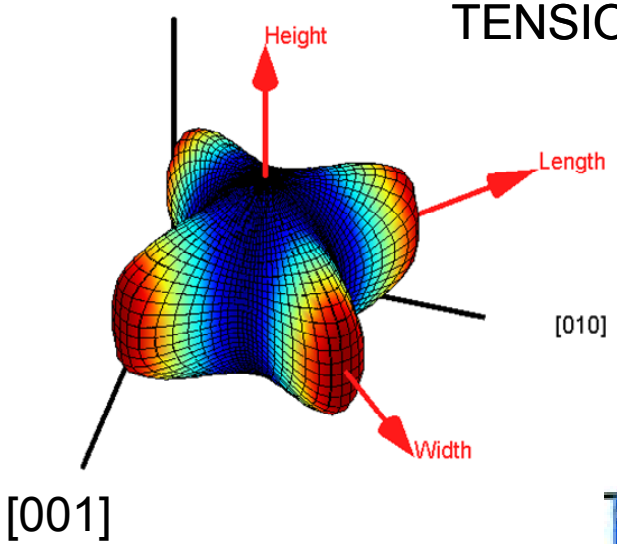


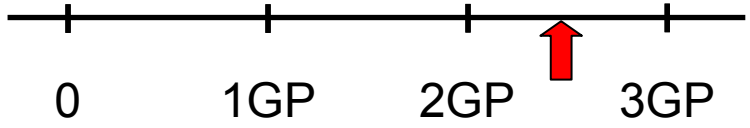
UNIAXIAL COMPRESSION

BUILD

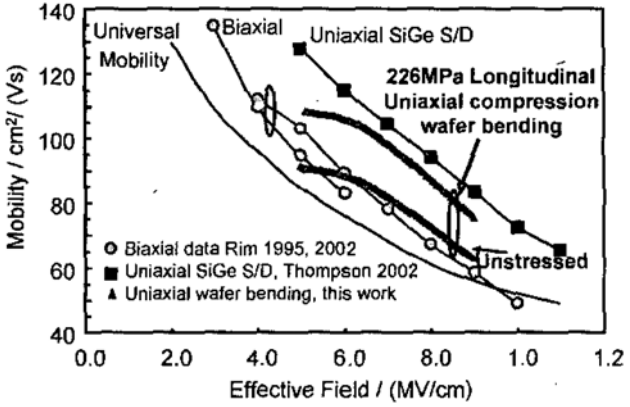


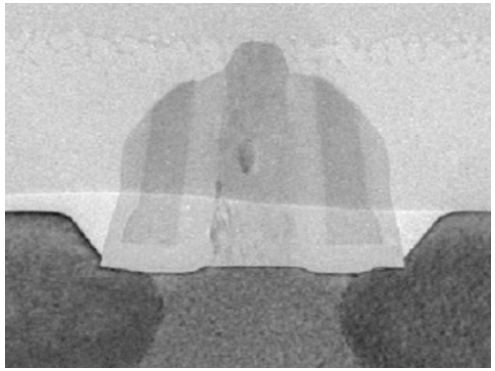
BIAXIAL TENSION

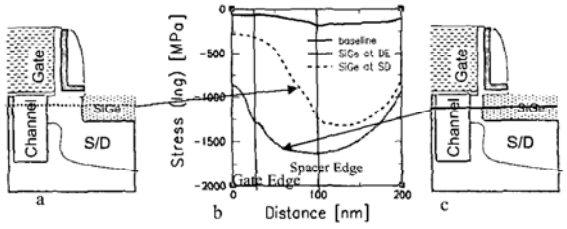


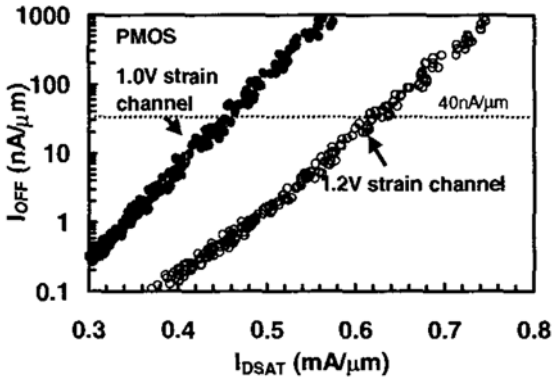


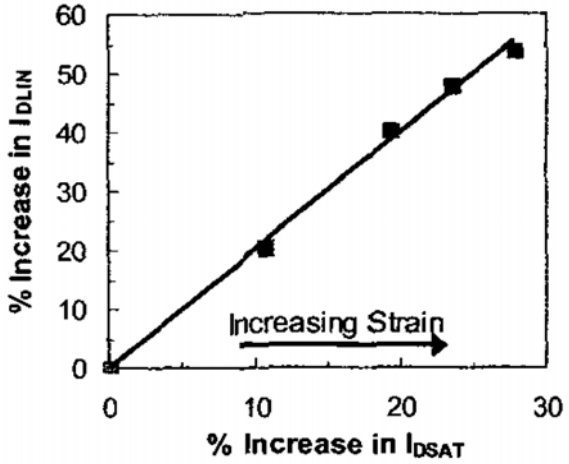
Uniaxial Strain Enhancement with Embedded SiGe (PMOS)

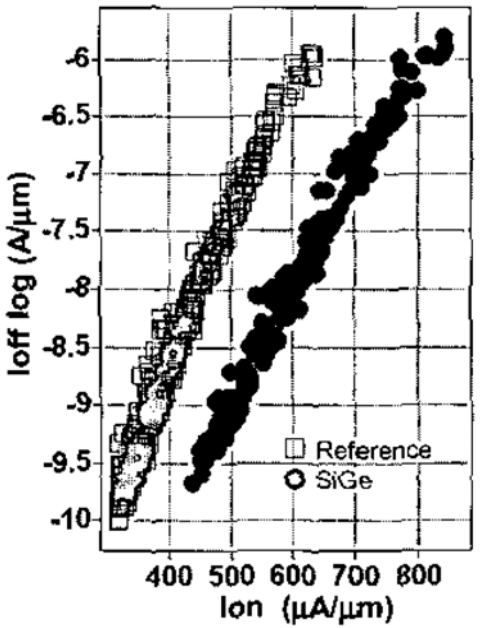










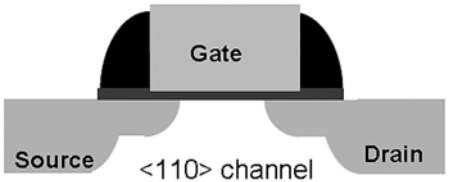


Thompson – Intel
IEDM 2002 / 2004 [71-72]

Ghani – Intel
IEDM 2003 [73]

Chidambaram
TI / Applied Materials
VLSI - 2004 [74]

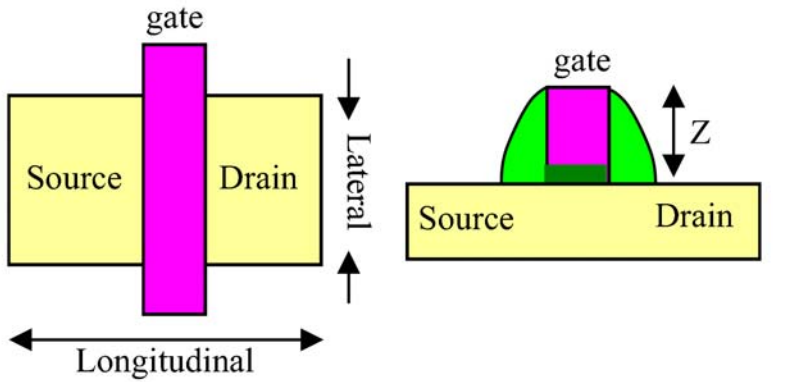
Strain optimization (100) <110>



Type of Stress Needed for Enhanced Mobility

Direction	NMOS	PMOS
Longitudinal	Tension +++	Compression ++++
Transverse	Tension ++	Tension +++
Out-of-plane	Compression ++++	Tension +

Thompson – Intel – TED 2004 [75]



		NMOS	PMOS
Longitudinal	X	Tensile	Compressive
Lateral	Y	Tensile	Tensile
Si Depth	Z	Compressive	Tensile

Chan – IBM – CICC 2005 [76]

A Graphical Representation of the Piezoresistance Coefficients in Silicon

Kanda – Hamamatsu University – TED 1982 [77]

Top: (+) piezo (resisitivity increases with tensile stress), Bottom: (-) piezo (resistivity decreases with tensile stress)

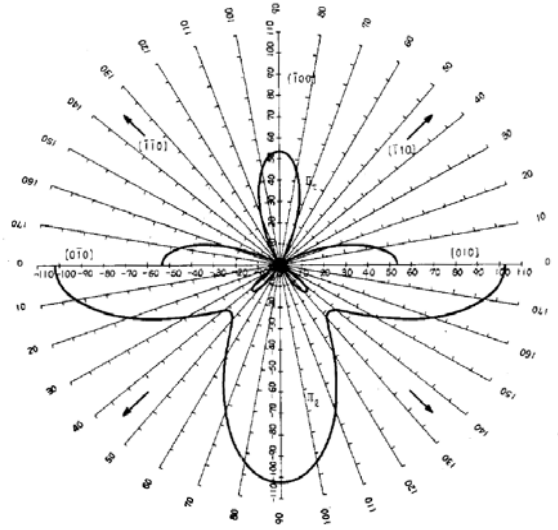


Fig. 2. Room temperature piezoresistance coefficients in the (001) plane of n-Si (10^{-12} cm^2/dyne).

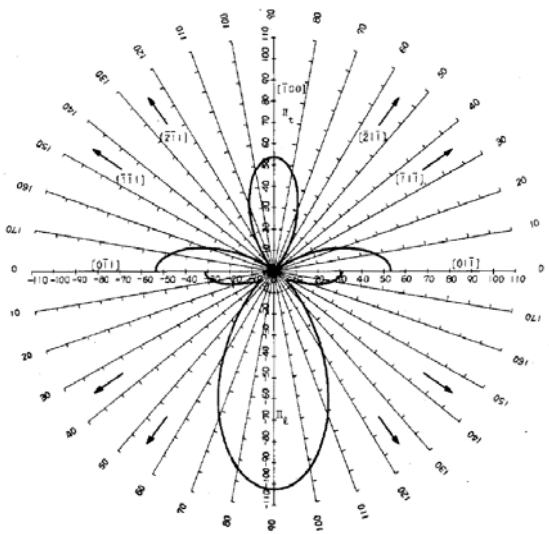


Fig. 3. Room temperature piezoresistance coefficients in the (011) plane of n-Si (10^{-12} cm^2/dyne).

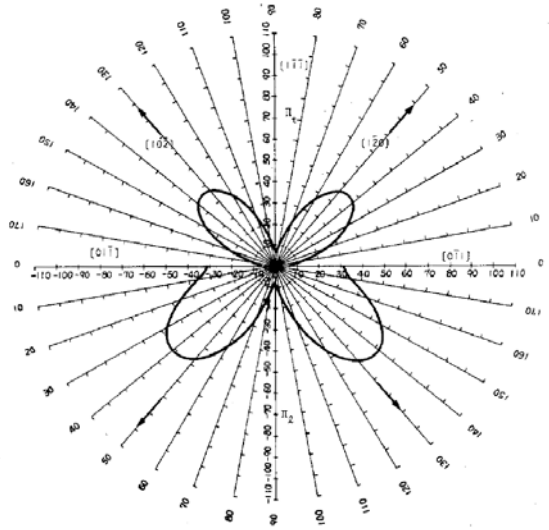


Fig. 4. Room temperature piezoresistance coefficients in the (211) plane of n-Si (10^{-12} cm^2/dyne).

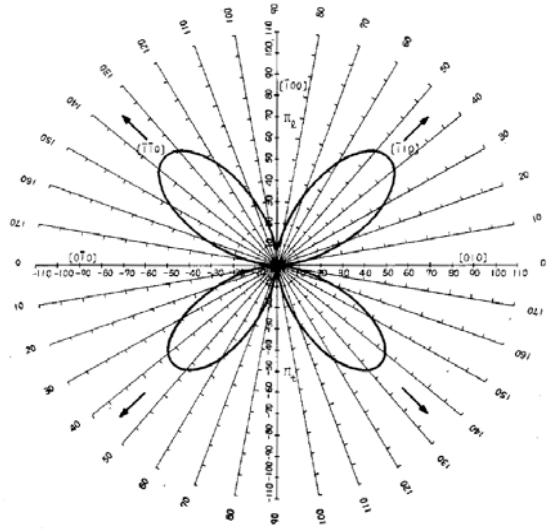


Fig. 5. Room temperature piezoresistance coefficients in the (001) plane of p-Si (10^{-12} cm^2/dyne).

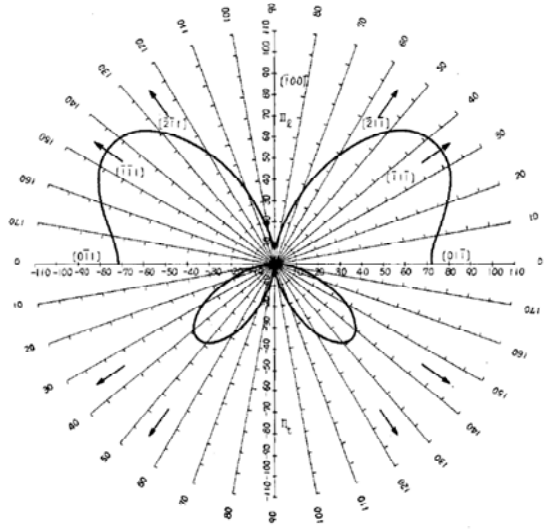


Fig. 6. Room temperature piezoresistance coefficients in the (011) plane of p-Si (10^{-12} cm^2/dyne).

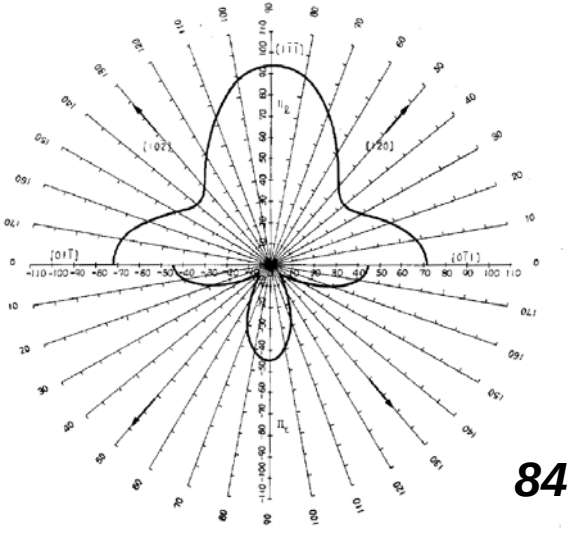
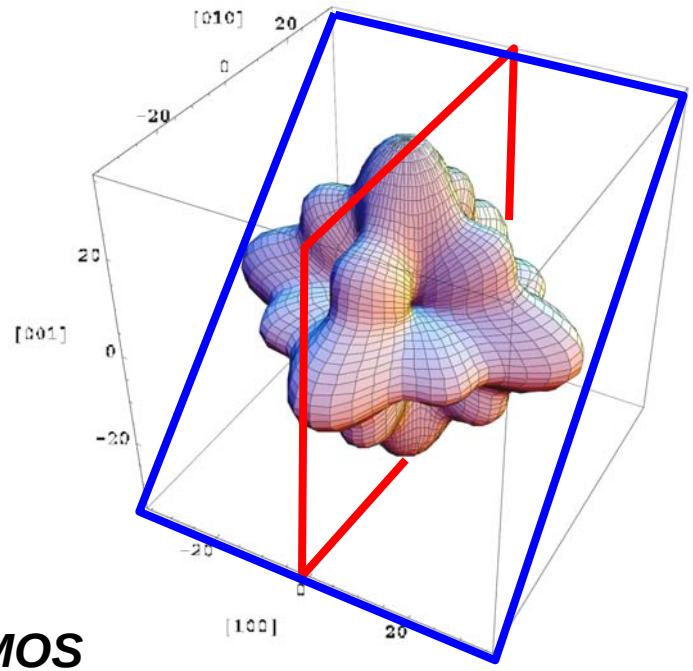


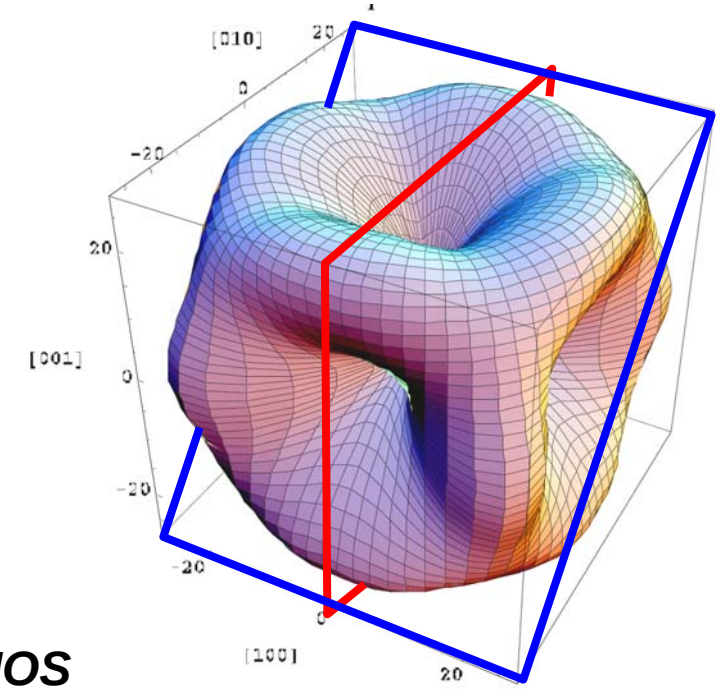
Fig. 7. Room temperature piezoresistance coefficients in the (211) plane of p-Si (10^{-12} cm^2/dyne).

Strain and Orientation
Piezoresistive coefficient as a function of direction

Udo – Infineon – Proc. IEEE Sensors 2004 [78]



NMOS



PMOS

Irie – Univ. of Tokyo – IEDM 2004 [79]

In-Plane Mobility Anisotropy and Universality Under Uni-axial Strains in n- and p-MOS Inversion Layers on (100), (110), and (111) Si

H. Irie, K. Kita, K. Kyuno and A. Toriumi

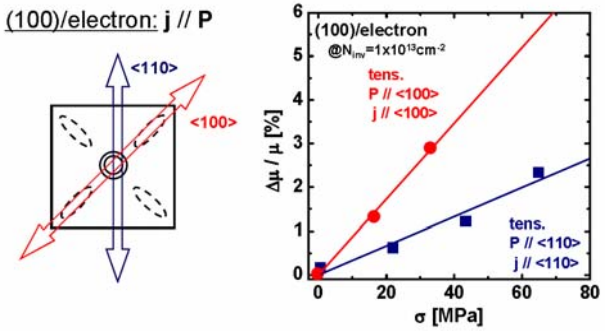


Fig.7 Channel direction(**j**) and strain direction (**P**) dependence of mobility gain. Here **j**//**P** is assumed, because Δμ/μ on (100) is largest when **j**//**P** as shown in Fig.4. Strain with **j**//$\mathbf{P}_{(tens.)}$//<100> gives larger mobility gain than **j**//$\mathbf{P}_{(tens.)}$//<110>.

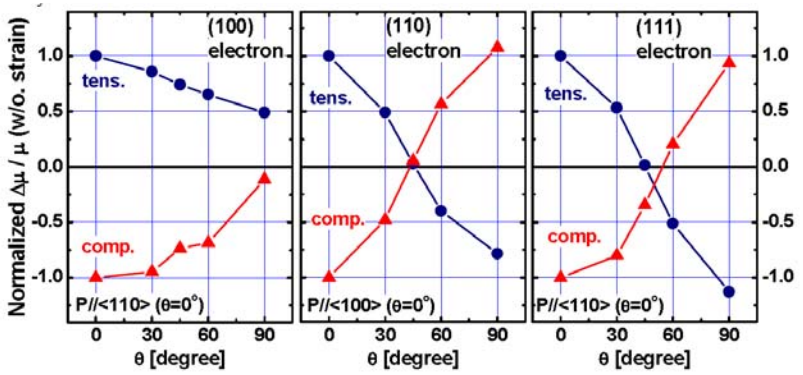


Fig.4 Variation rates of electron mobility under a uni-axial strain along θ=0° as a function of θ. The given value is taken at N_{inv}=5x10^{12}cm^{-2}. Note that the variation rate is normalized by the rate of MOSFET with **j** // θ=0°. The θ dependences of (100)/electron is apparently different from the others.

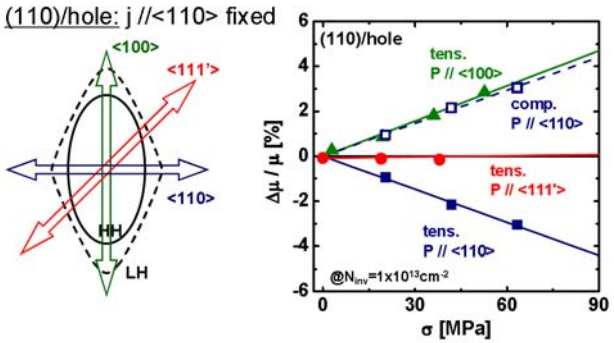


Fig.10 Strain direction dependence of mobility gain for (110)/<110> hole. Here **j**//<110> is assumed, because μ on (110)/<110> is overwhelmingly larger than those in the other channel directions as shown in Fig.3. Strain with **j**//<110>& $\mathbf{P}_{(comp.)}$//<100> or $\mathbf{P}_{(tens.)}$//<110> gives larger mobility gain than the others.

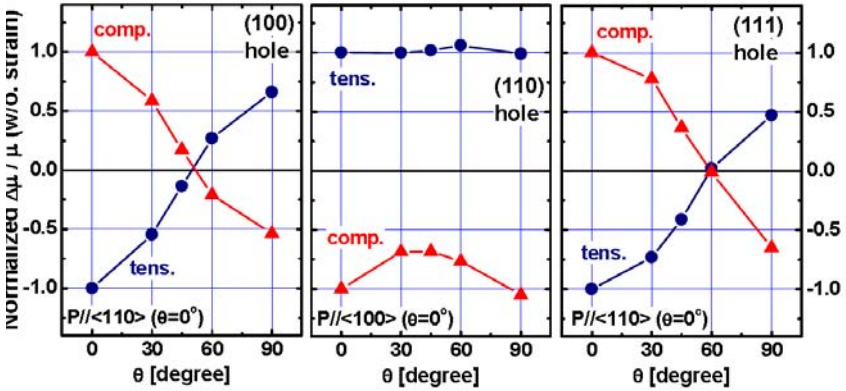
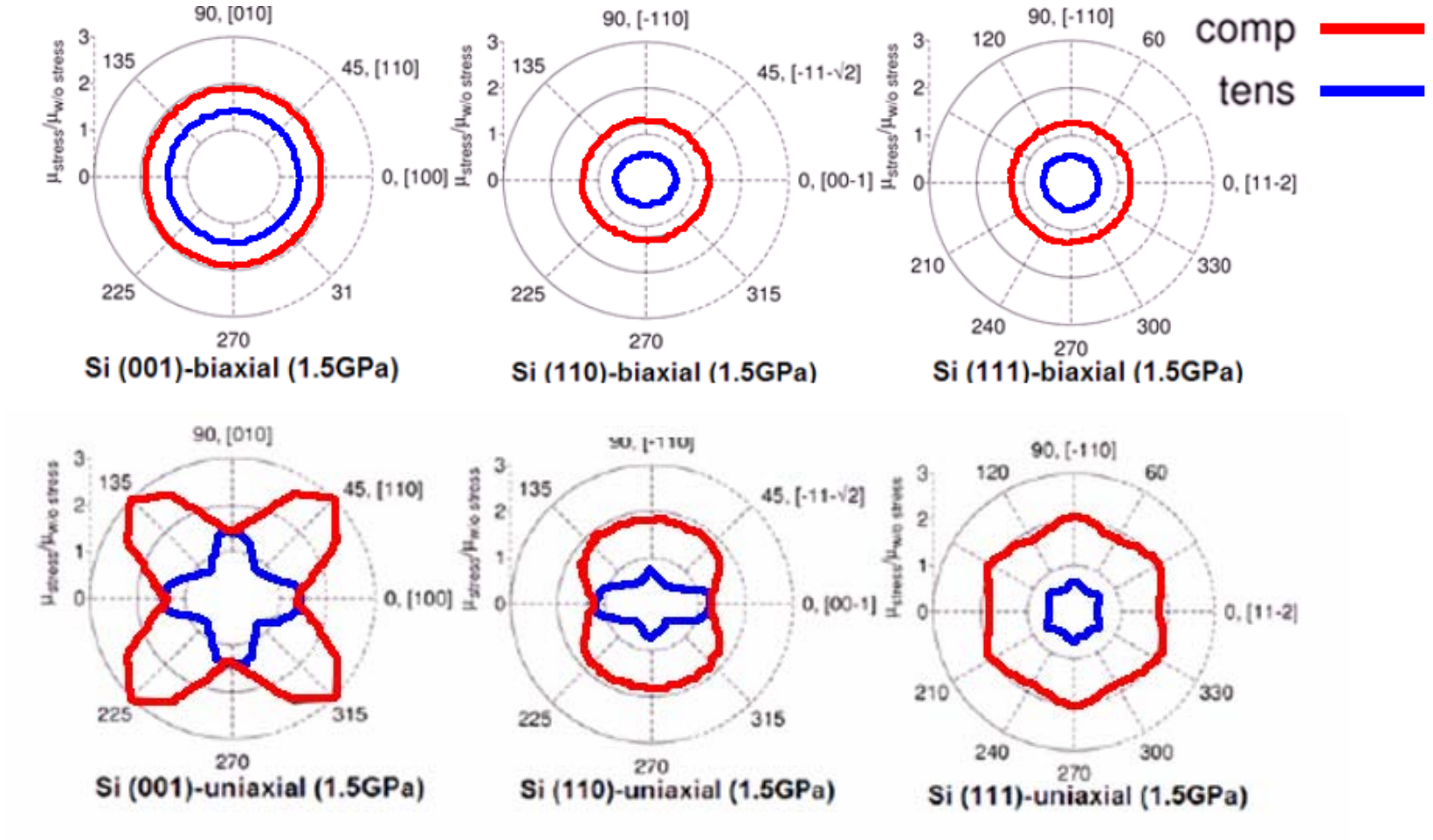


Fig.9 Variation rates of hole mobility under a uni-axial strain along θ=0° as a function of θ. The given value is taken at N_{inv}=5x10^{12}cm^{-2}. The θ dependences of (110)/hole is apparently different from the others.

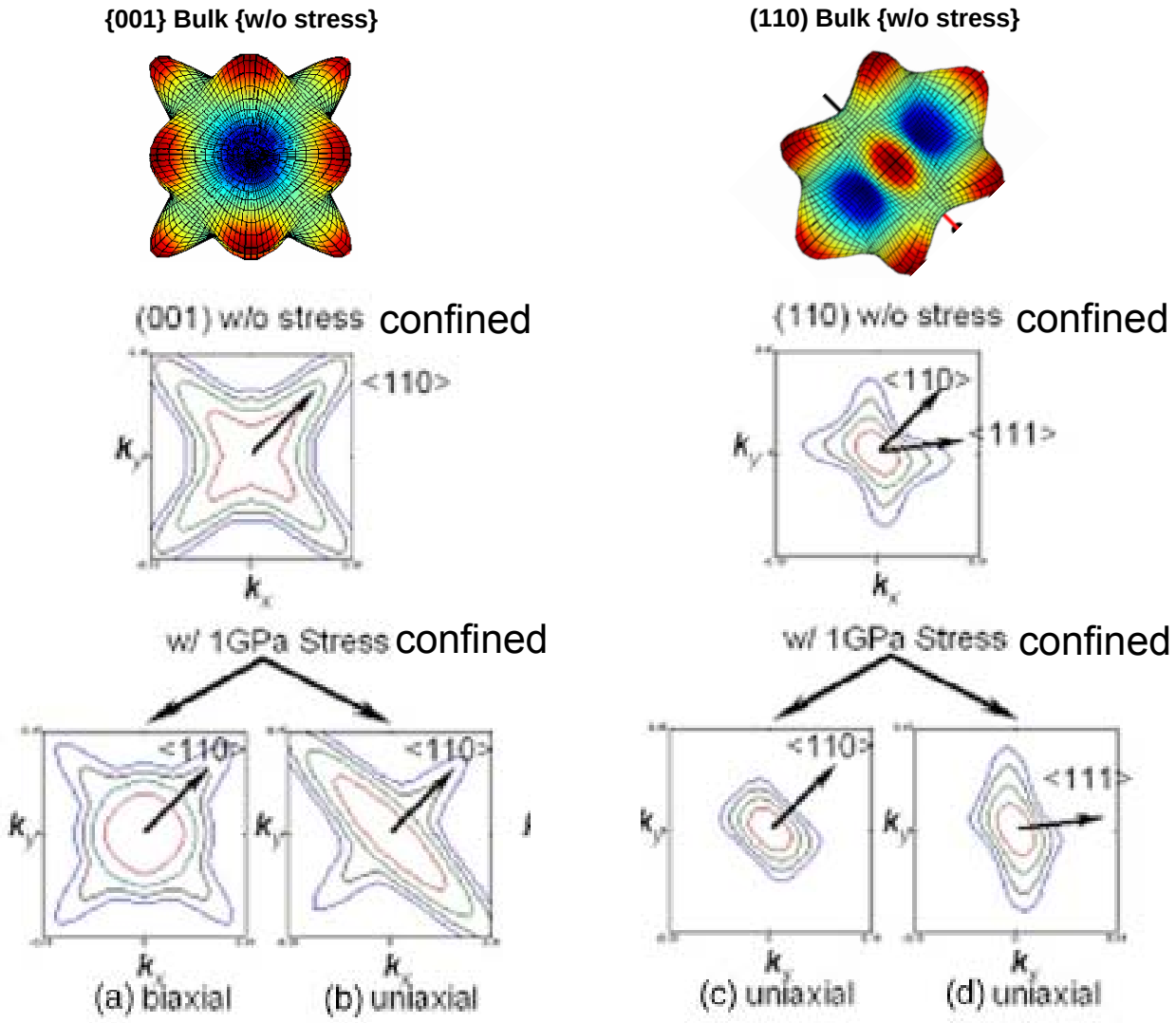
Krishnamohan – Stanford – IEDM 2008 (session 36.5) [80]

Comparison of (001), (110) and (111) Uniaxial- and Biaxial- Strained-Ge and Strained-Si PMOS DGFETs for All Channel orientations: Mobility Enhancement, Drive Current, Delay and Off-State Leakage

[1,4]Tejas Krishnamohan, [1]Donghyun Kim, [2]Thanh Viet Dinh, [3]Anh-tuan Pham,
[3]Bernd Meinerzhagen, [2]Christoph Jungemann, [1]Krishna Saraswat



Strain, Quantization and (110)

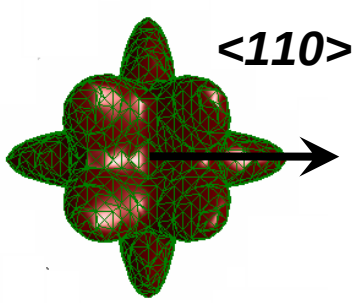


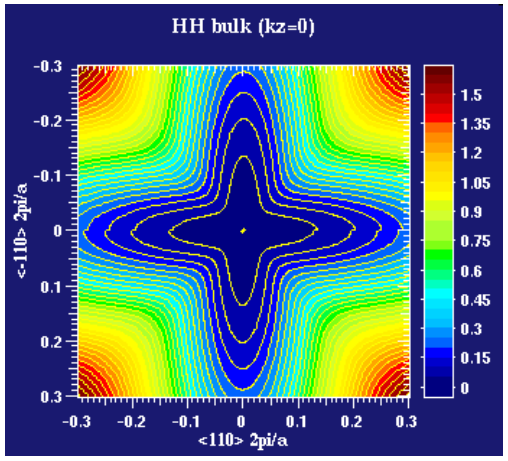
Adapted from Sun, U of Florida - JAP 2007 [81]

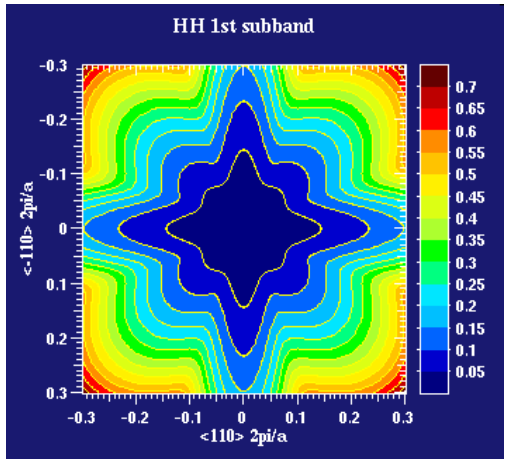
(001) Surface (k⊥=0)

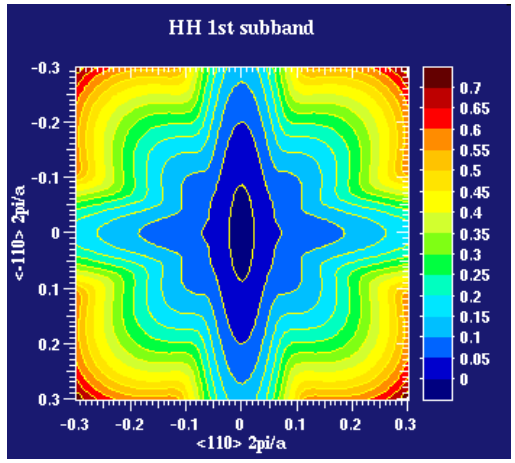
(001) Surface Vg=-1V

(001) Surface Vg=-1V, Sxx=-1GPa





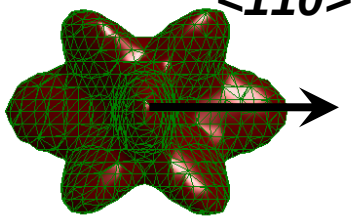


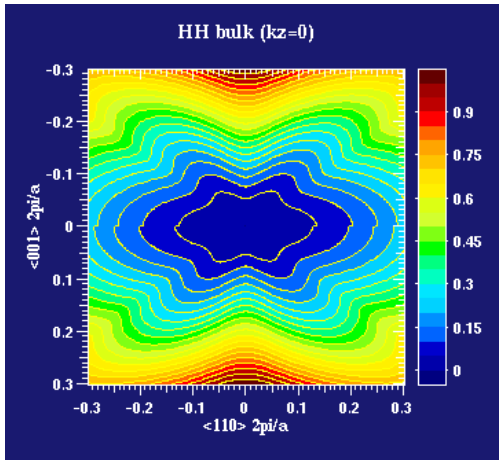


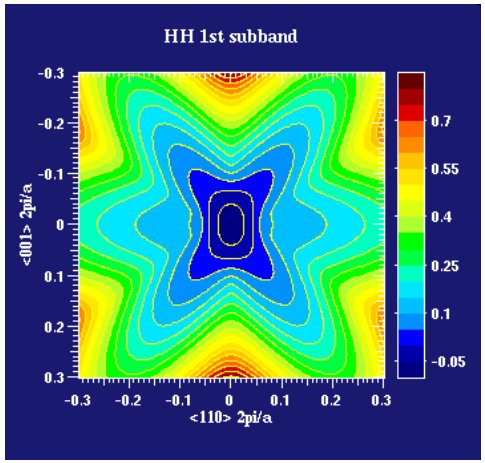
(110) Surface (k⊥=0)

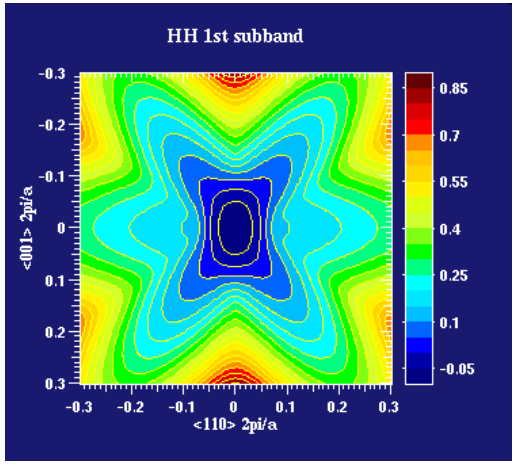
(110) Surface Vg=-1V

(110) Surface Vg=-1V, Sxx=-1GPa









BULK

1'D CONFINED

1'D CONFINED STRAINED

Strain, Quantization, and (110)

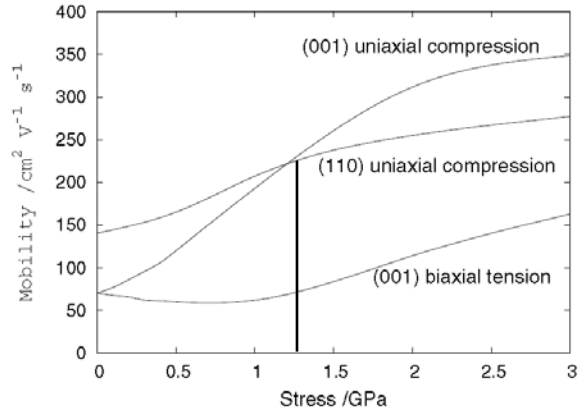
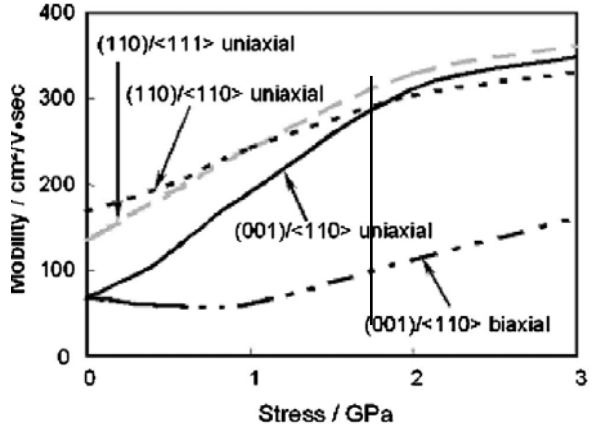


Fig. 9. Modeled mobility vs. longitudinal stress on (100) and (110) wafers. Note the low density of states on (110) limits the stress enhanced mobility.



[G. 3. Hole mobility vs stress (inversion charge=1×10^{13}/cm^2). The enhancement factor is the highest for (001)/⟨110⟩ and lowest for (110)/⟨110⟩ *p*-MOSFETs. At high stress (~3 GPa), the three longitudinal compressive uniaxial stress cases have comparable hole mobility.

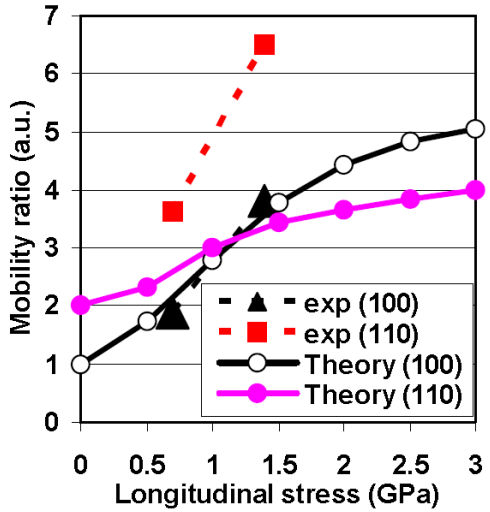


Fig. 12: Hole mobility ratio vs. longitudinal channel stress. The dashed lines with symbols are our experimental mobility ratios for PMOS with 3.5GPa liner or eSiGe+3.5GPa liner, using (100) neutral liner PMOS as reference (1×). The solid lines with symbols are the mobility ratios converted from the theoretical predictions published in Ref. 6.

Thompson – U of Florida IEDM 2006 [82]

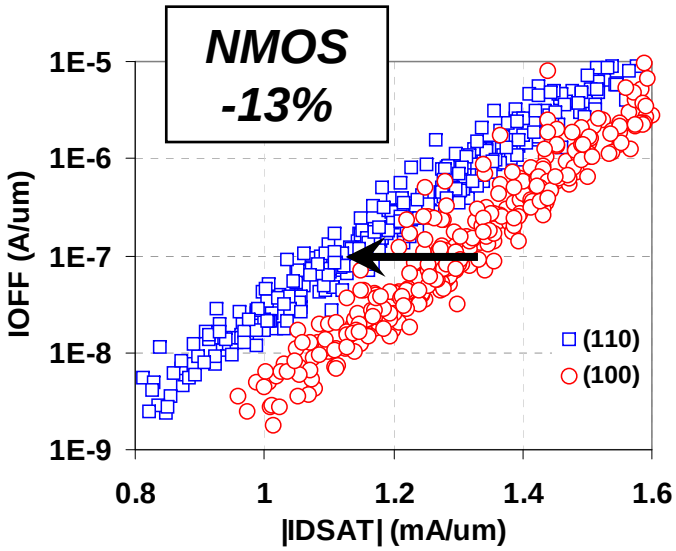
Sun – U of Florida JAP 2007 [81]

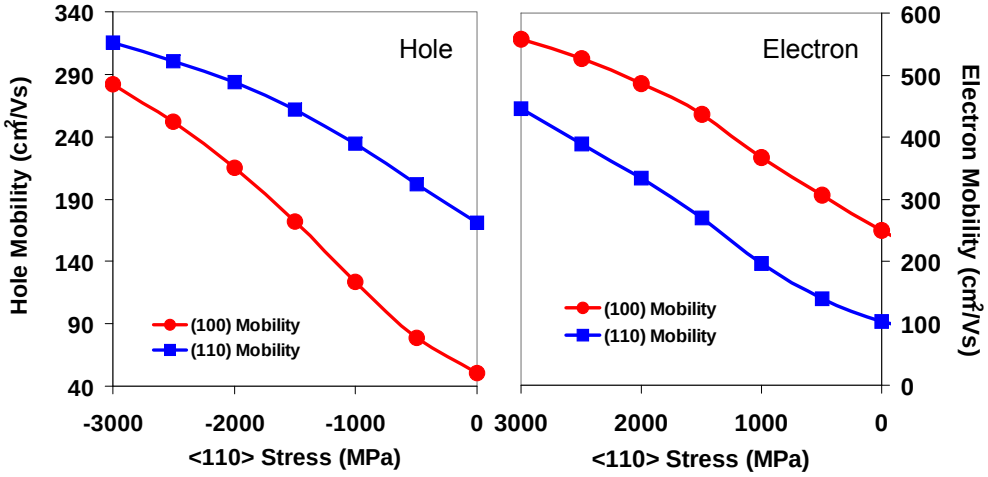
"While (100) mobilities agree reasonably well, a strong discrepancy exists for (110) mobilities" - Yang, AMD/IBM, IEDM 2007, with reference to Fig. 12 (Ref. 6 is Thomson, IEDM 2006) [83]

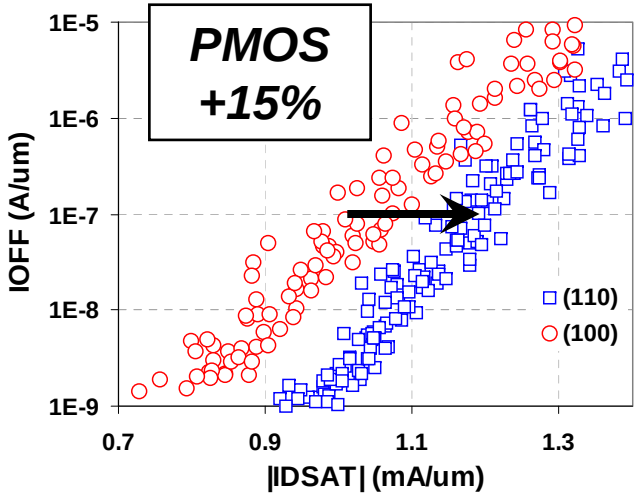
Packan – Intel – IEDM 2008 (session 3.4) [84]

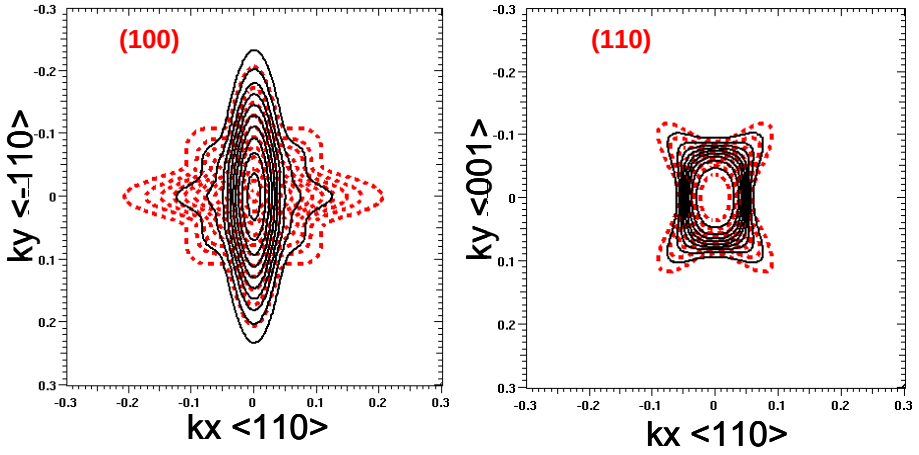
High Performance Hi-K + Metal Gate Strain Enhanced Transistors on (110) Silicon

P.Packan, S.Cea, H.Deshpande, T.Ghani, M.Giles, O.Golonzka, M.Hattendorf, R.Kotlyar, K.Kuhn, A.Murthy, P.Ranade, L.Shifren, C.Weber and K.Zawadzki

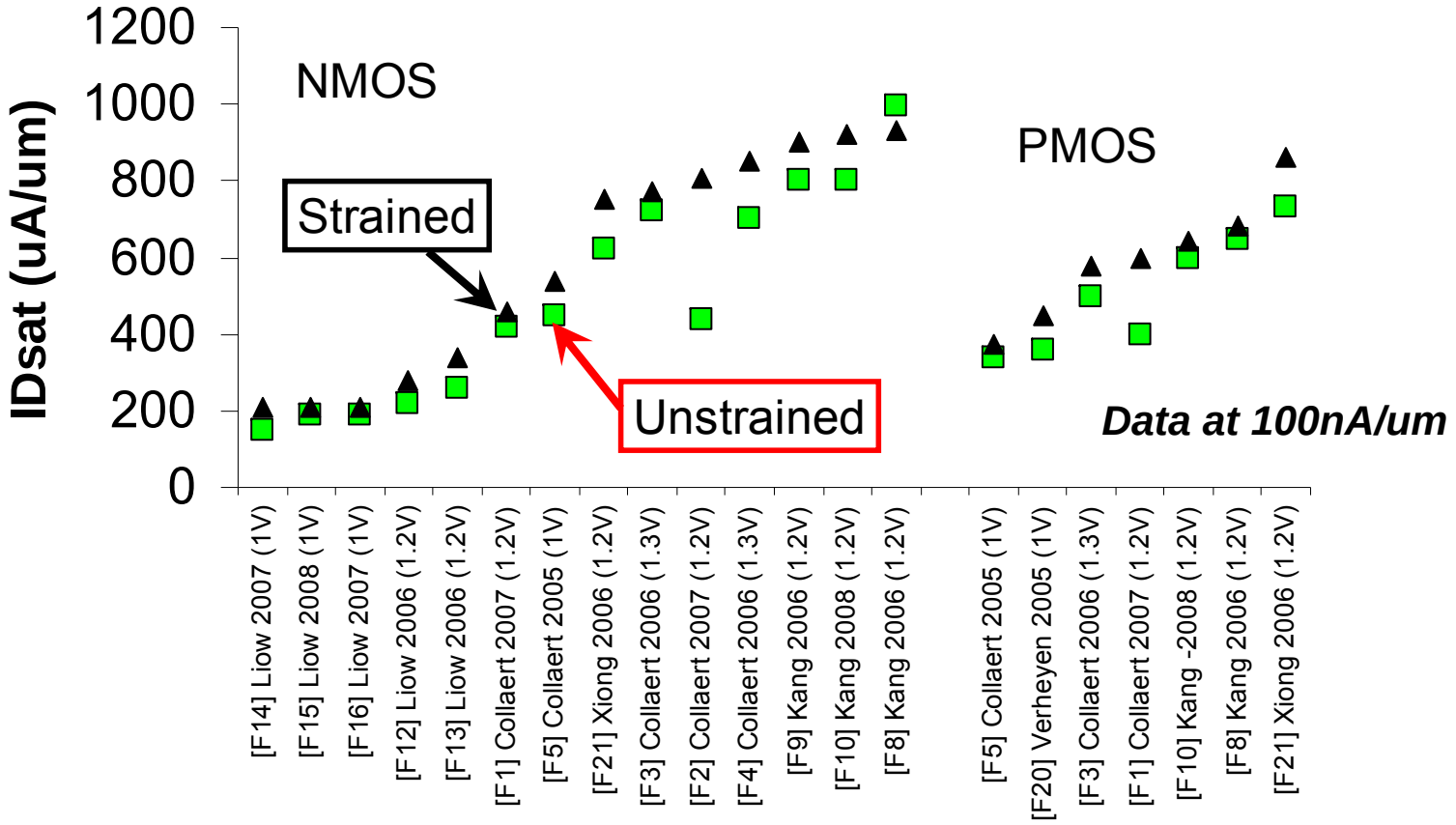








Strain and MuGFETs



Literature reports on stressing MuGFETs have not shown dramatic enhancements – challenges to achieving a high stress state in a free-standing fin (free surfaces?)

See special reference section on MuGFETS

(110) and HiK-MG
Harris – AMD/Sematech – IEDM 2007 [85]

Flexible, Simplified CMOS on Si(110) with Metal Gate / High κ for HP and LSTP

H. R. Harris[1], S. E. Thompson[†], S. Krishnan, P. Kirsch, P. Majhi[2], C.E. Smith, M.M. Hussain, G. Sun[†], H. Adhikari,[1] S. Suthram,[†] B.H. Lee, H.-H. Tseng, and R. Jammy[3]

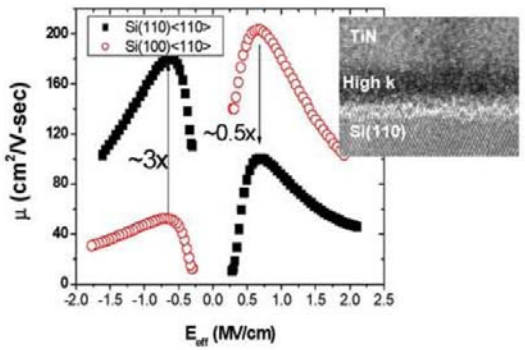


Fig 2. The mobilities of the Si(110) surface and Si(100) surfaces compared with HfO2 as the gate dielectric. (Inset) Gate stack on Si(110) surface.

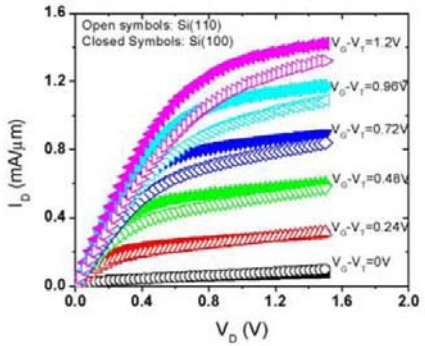


Fig 3. Despite the mobility decrease, the short channel Id-Vd curves have very similar characteristics.

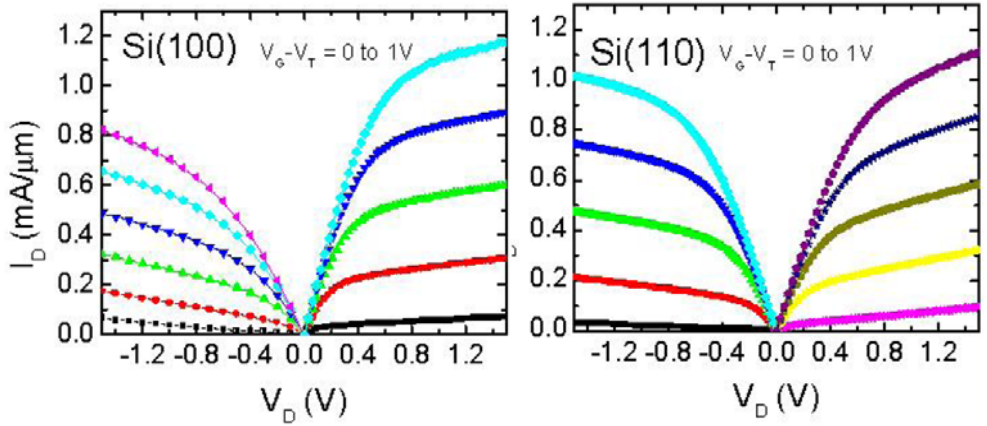
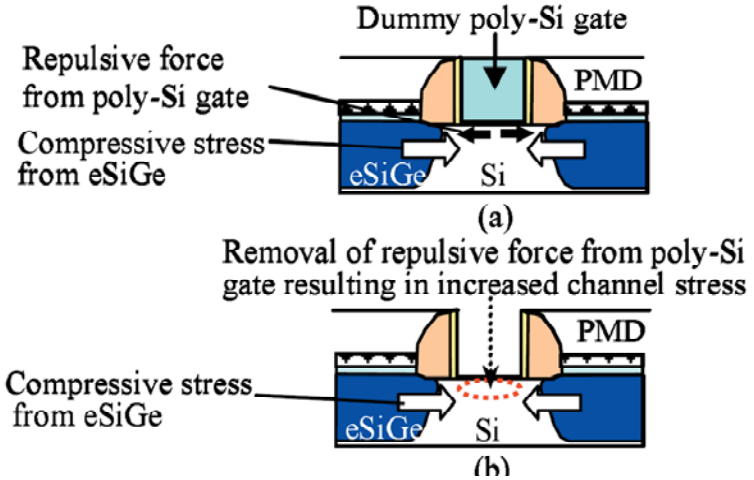


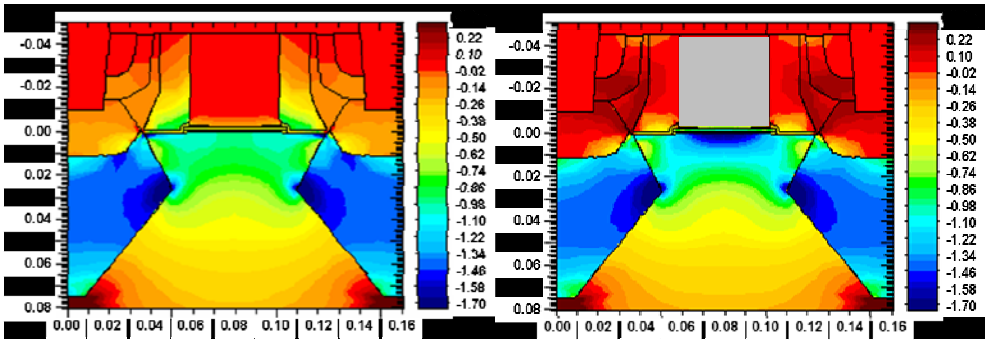
Fig 6. Despite the reduced NMOS Si(110) mobility, the Si(110) Id-Vd shows better symmetric performance than the Si(100) devices.

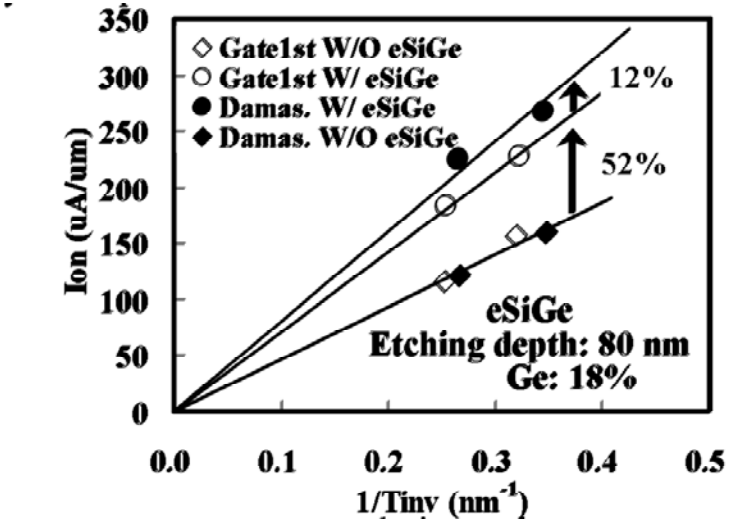
From the paper: **"**Thus the orientation dependant mobility is less important in highly scaled NMOS than in PMOS when a high k gate dielectric is used."

Enhanced PMOS strain: Gate-last HiK-MG

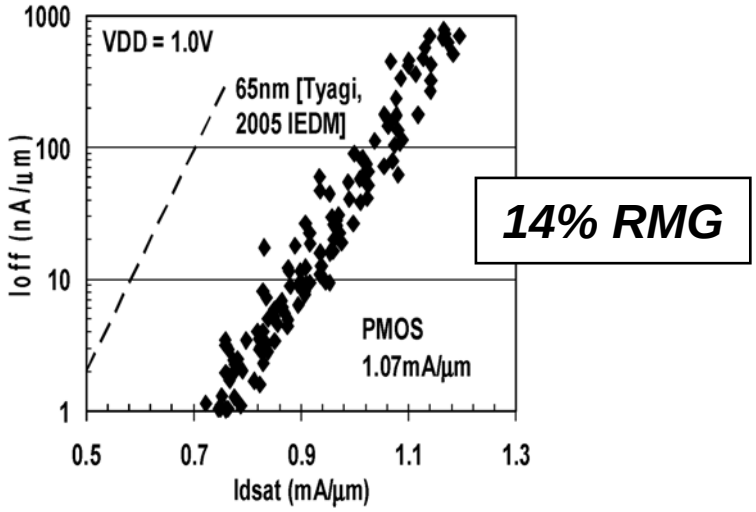


Before gate removal **After gate removal**





Wang – Sony
VLSI 2007 [86]



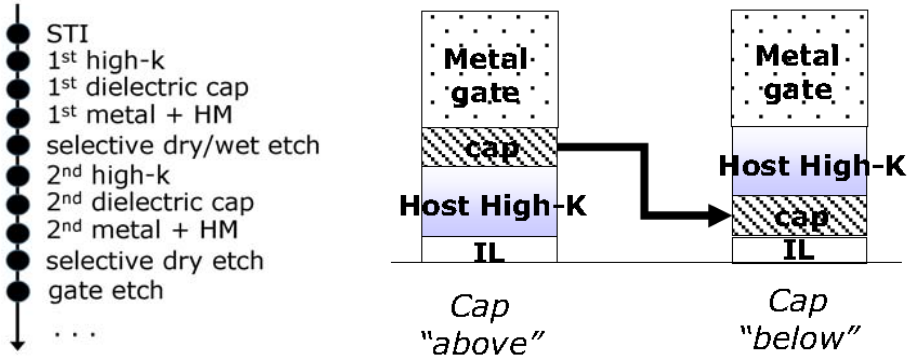
14% RMG

Auth – Intel
VLSI 2008 [8]

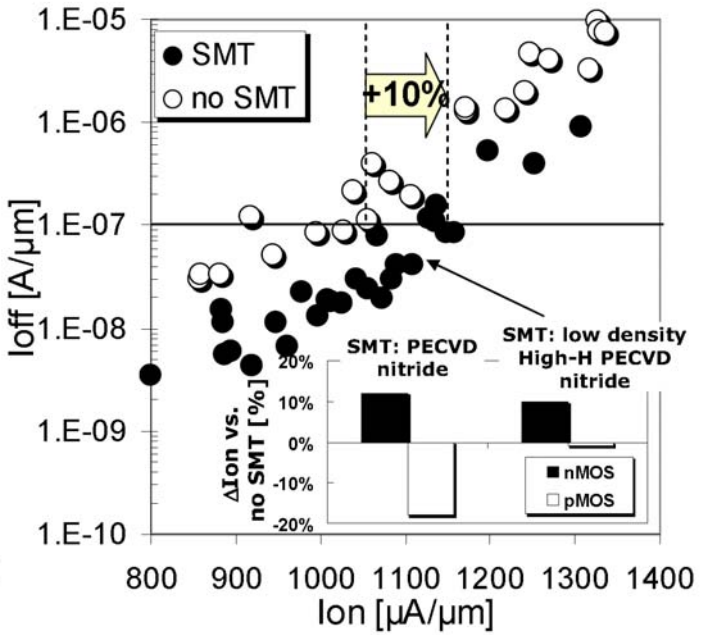
SMT enhancement with HiK-MG
Kubicek – IMEC – VLSI 2008 [87]

Strain enhanced Low-V_T CMOS featuring La/Al-doped HfSiO/TaC and 10ps Invertor Delay

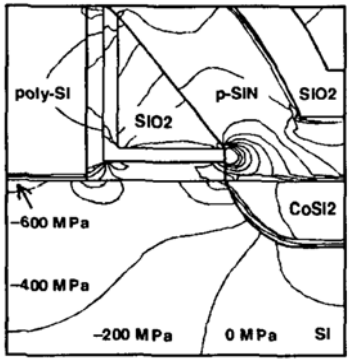
S. Kubicek, T.Schram, E.Rohr, V.Paraschiv, R.Vos, M.Demand, C.Adelmann, T.Witters, L.Nyns, A.Delabie , L.-Å.Ragnarsson, T.Chiarella, C.Kerner, A.Mercha, B.Parvais, M.Aoulaiche†, C.Ortolland, H.Yu, A.Veloso, L.Witters, R.Singanamalla†, T. Kauerauf†, S.Brus, C.Vrancken, V.S.Chang[1], S-Z.Chang[1], R.Mitsuhashi[2], Y.Okuno[2], A.Akheyar[3], H.-J.Cho[4], J.Hooker[5], B. J. O'Sullivan, S.Van Elshocht, K.De Meyer†, M.Jurczak, P.Absil, S.Biesemans and T.Hoffmann

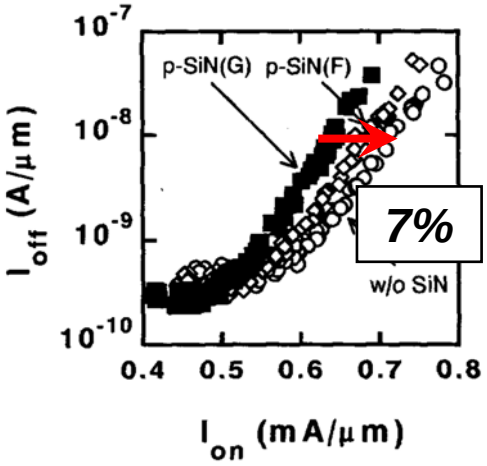


From the paper: ***"…*** the gain from traditional stress boosters (CESL, embedded-SiGe, channel orientation) was maintained on High-κ/Metal gate.."

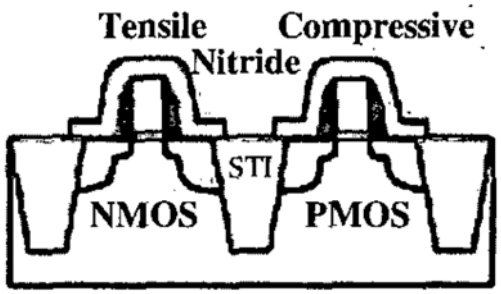


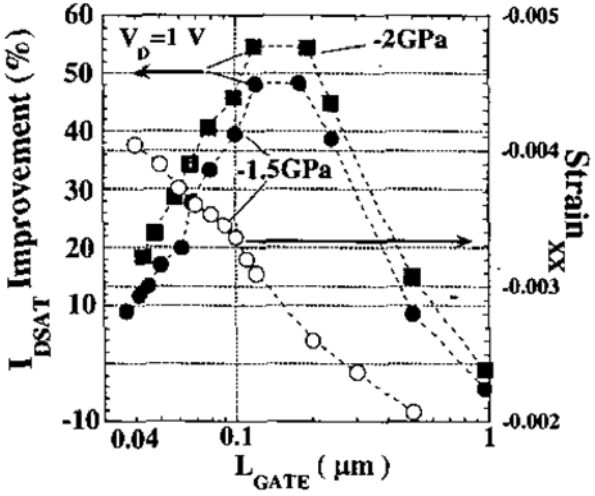
Etch-stop nitride (CESL)



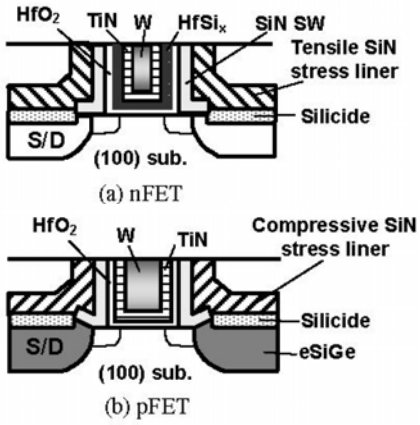


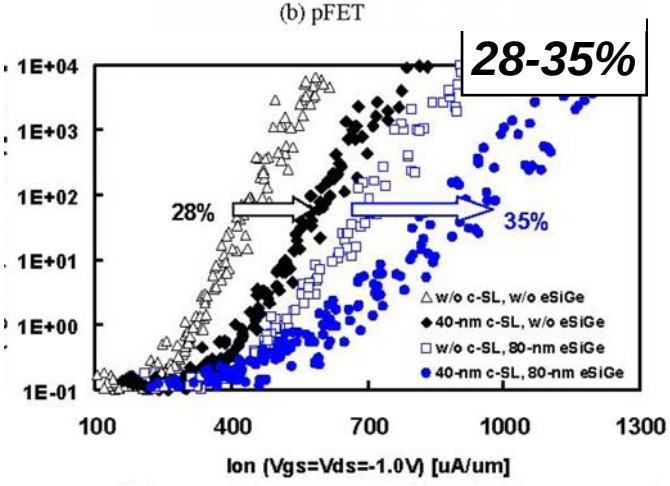
Ito – NEC
IEDM 2000 [88]
NMOS SiN strain





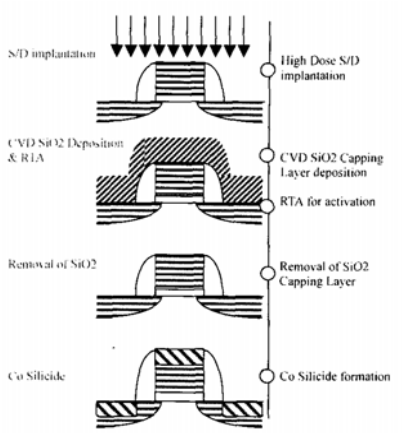
Pidin – Fujitsu
IEDM 2004 [89]
N and PMOS

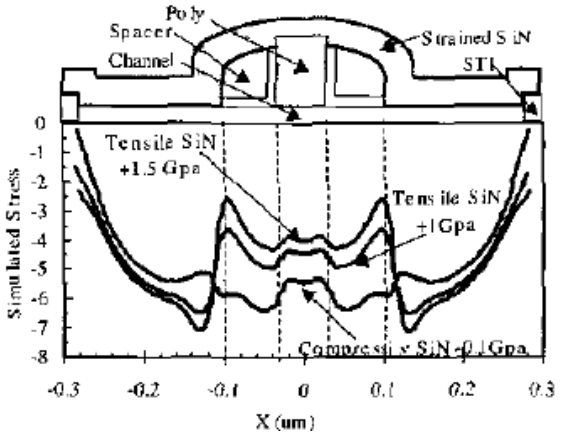


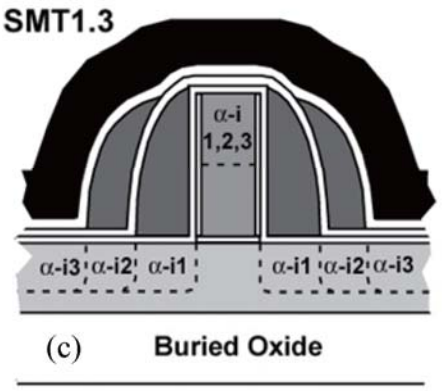


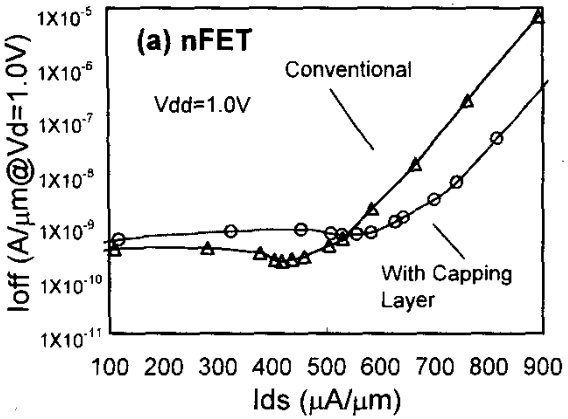
Mayuzumi – Sony
IEDM 2007 [90]
Dual-cut stress liners
(MG process)

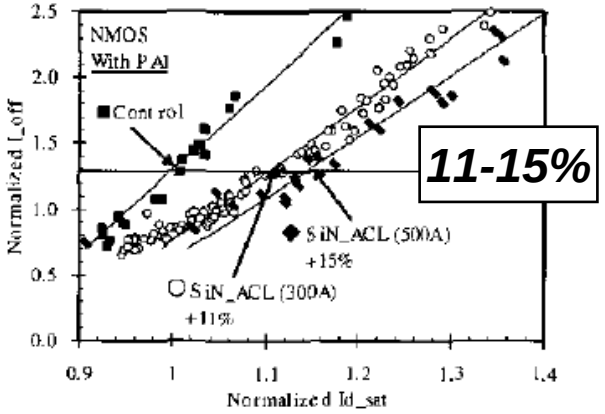
Stress Memorization (SMT)

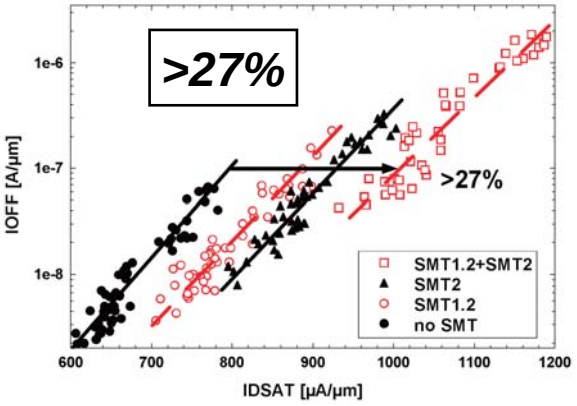










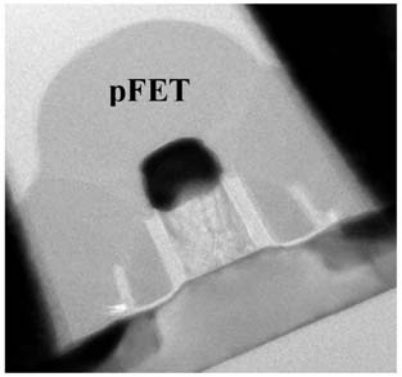


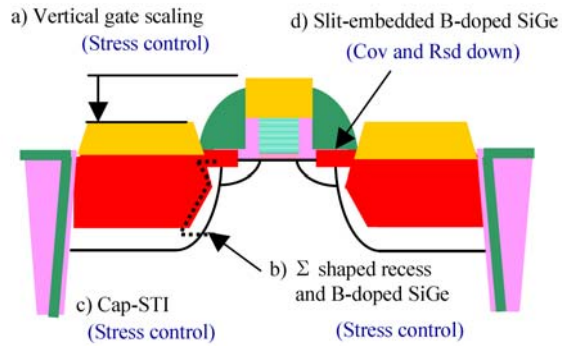
Ota – Mitsubishi
IEDM 2002 [91]
NMOS SMT

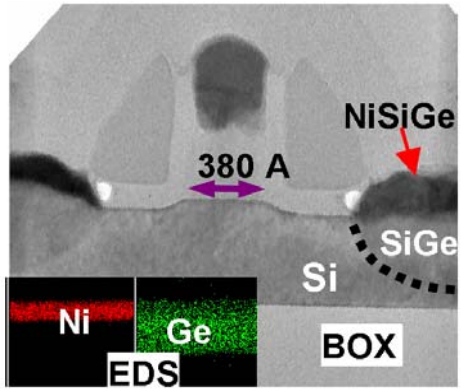
Chen – TSMC
VLSI 2004 [92]
NMOS SMT

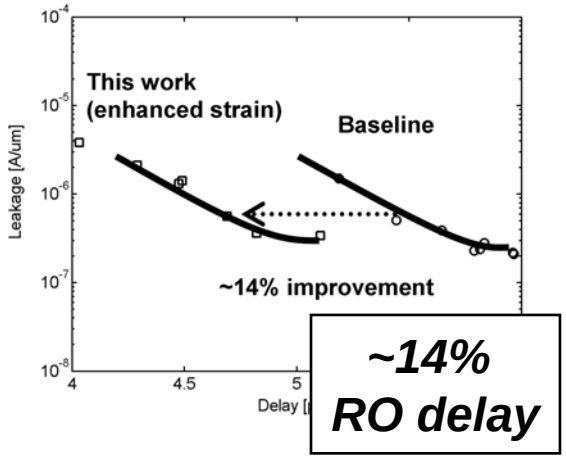
Wei – AMD
VLSI 2007 [93]
Multiple liners

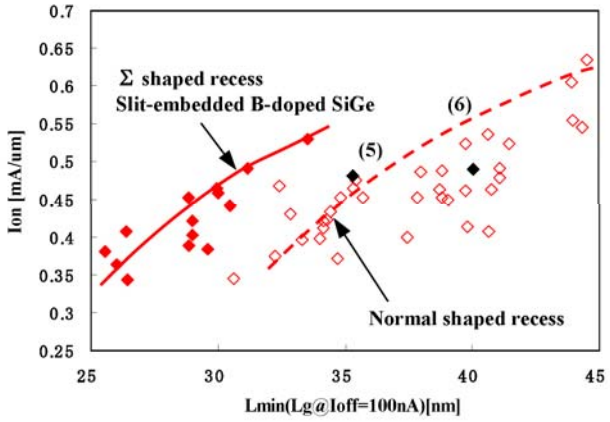
Embedded SiGe (PMOS)

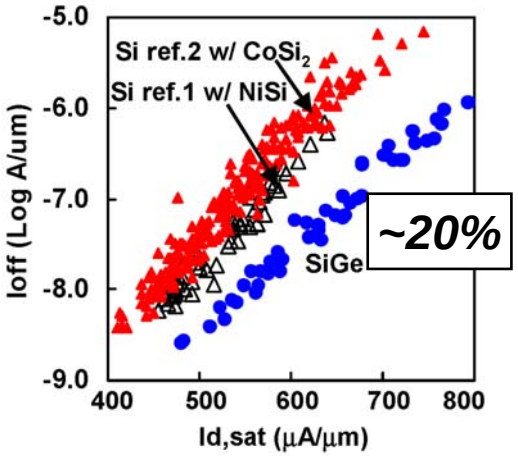










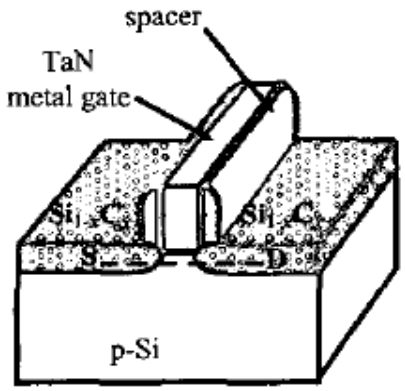


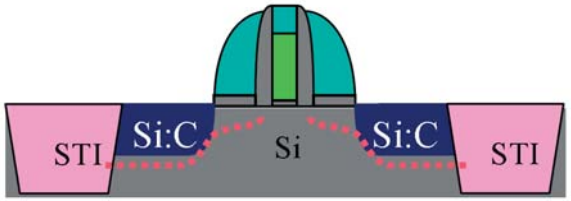
Lee - IBM
IEDM 2005 [94]
SOI and e-SiGe

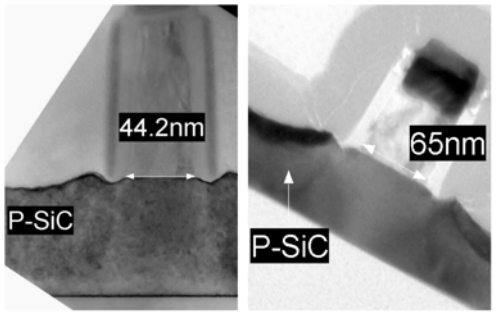
Ohta – Fujitsu
IEDM 2005 [95]
Profile engr.

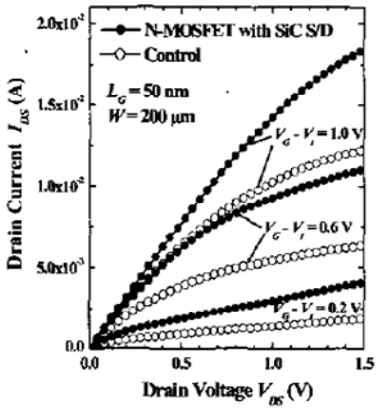
Zhang – Freescale
VLSI 2005 [96]
Thin body SOI

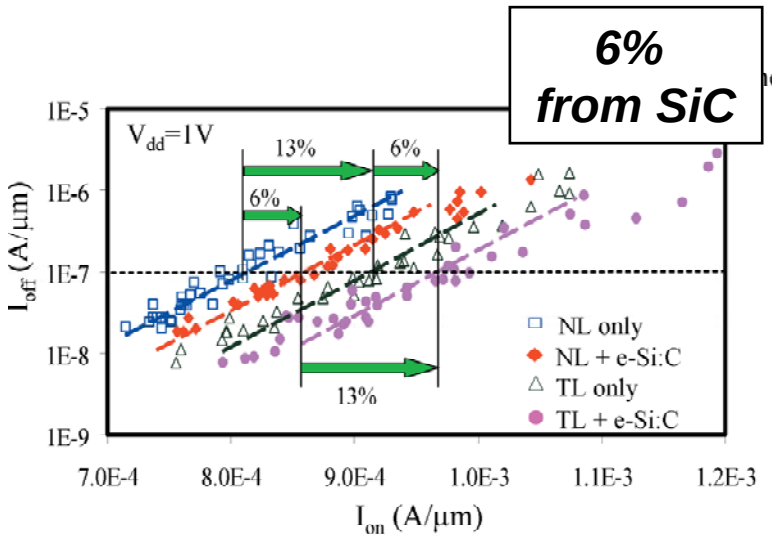
Embedded Si:C (NMOS)

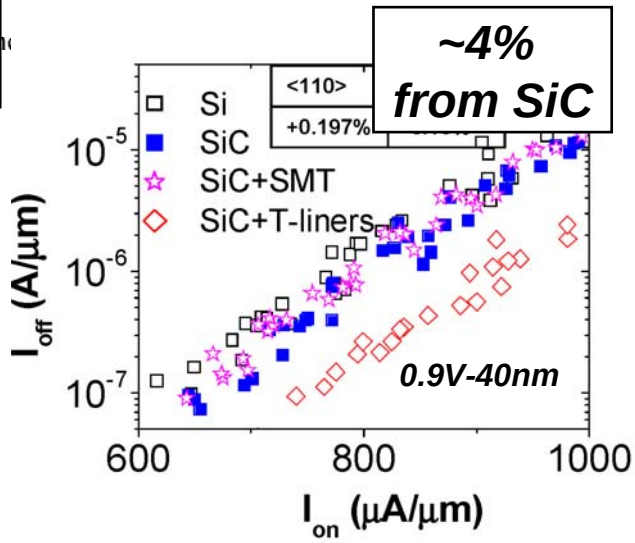










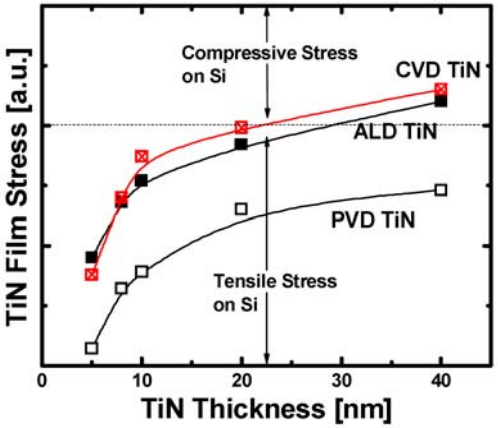


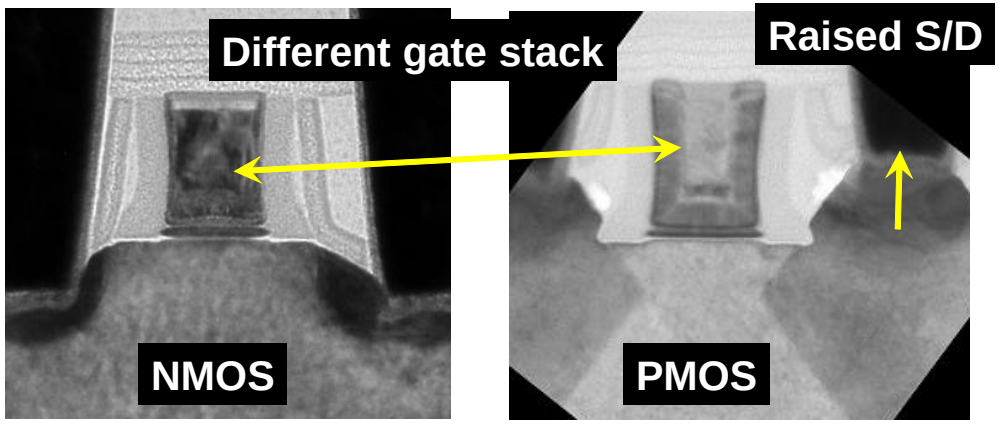
Ang – NUS-Singapore
IEDM 2004 [97]
Selective epi SiC (undoped)

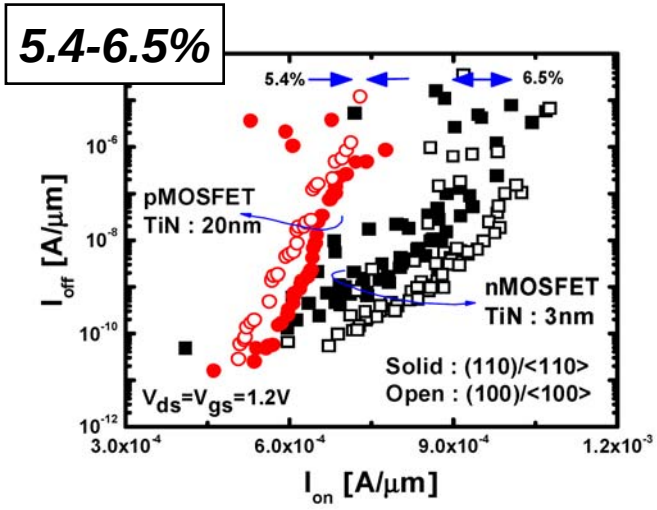
Liu – IBM
VLSI 2007 [98]
Implant + SPE

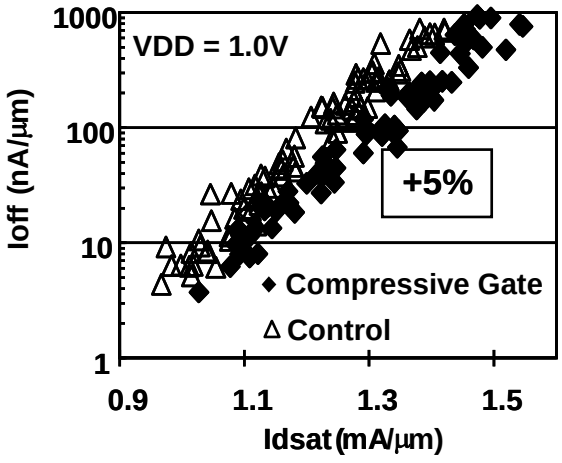
Ren – IBM
VLSI 2008 [99]
In-situ epi P-SiC

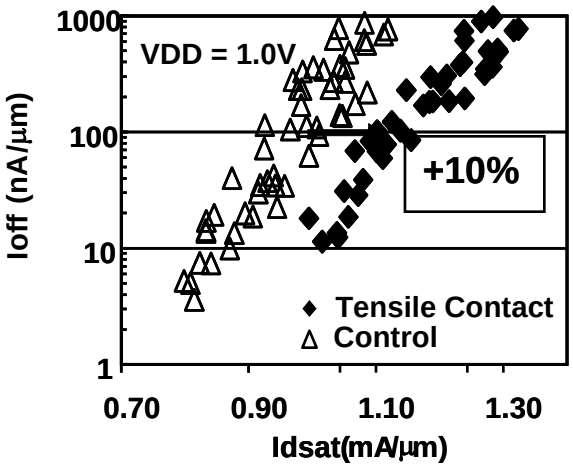
Metal stress (gate and contact)











Kang – Sematech
IEDM 2006 [100]

Auth – Intel
VLSI 2008 [87]

22nm risk assessment

CHANGE	COMMENTS
Further enhancements in strain technology	Low risk – evolutionary change – large suite of proven successful options
Further enhancements in HiK-MG technology	Low risk – continual improvement – driven by strong research/development efforts
Optimized substrate and channel orientation	Medium risk – requires some solution to the (100)<110>N vs (110)/<110>P issue
Reduction in MOS parasitic resistance	Medium risk – new annealing technologies, RE/NM silicide options
Reduction in MOS parasitic capacitance	Medium-high risk – low-k FE dielectrics pose significant process challenges
MuGFETs	High risk – significant challenges with parasitic R, parasitic C and topology
III/V or Ge channel material	Very high risk – fundamental issues still at research level.
Metallic S/D	Extremely high risk – significant architecture change AND remaining fundamental issues

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