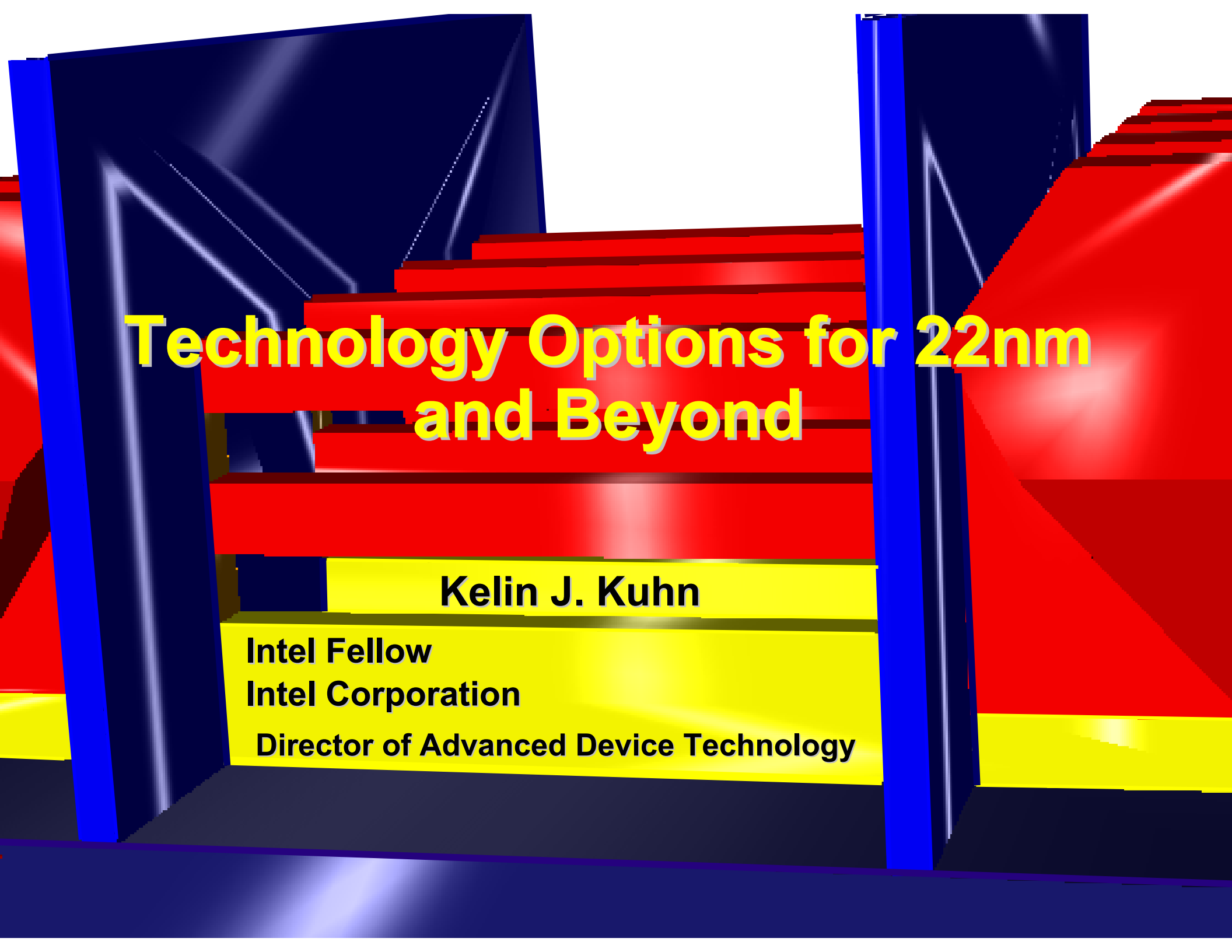
Technology Options for 22nm and Beyond
Kelin J. Kuhn
Intel Fellow
Intel Corporation
Director of Advanced Device Technology

AGENDA

- Scaling
- Gate control
- Mobility
- Resistance
- Capacitance
- Summary

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- Scaling
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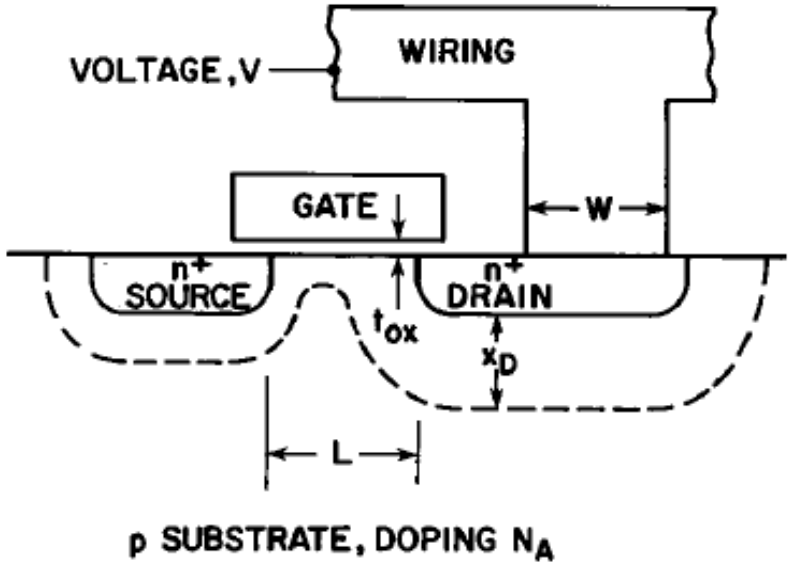
MOSFET Scaling

Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	1/κ
Doping concentration *Na*	κ
Voltage *V*	1/κ
Current *I*	1/κ
Capacitance *εA/t*	1/κ
Delay time/circuit *VC/I*	1/κ
Power dissipation/circuit *VI*	$1/\kappa^2$
Power density *VI/A*	1

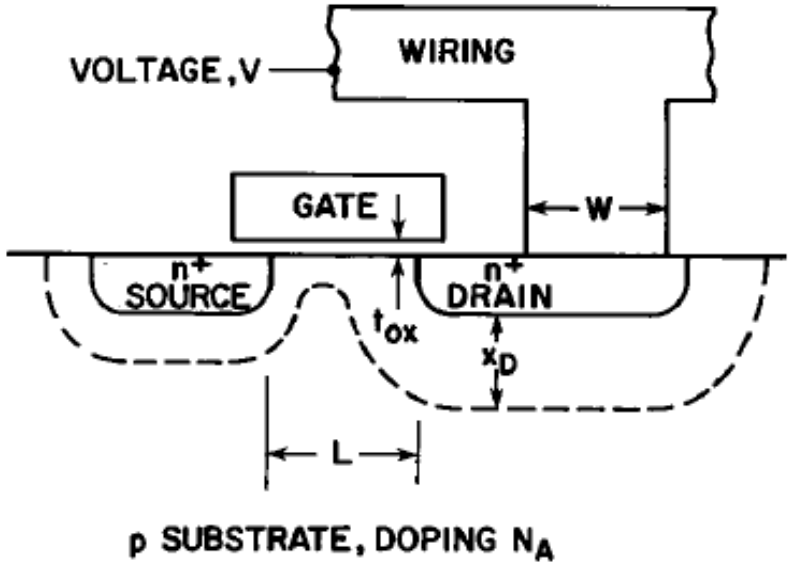


R. Dennard, IEEE JSSC, 1974

Classical MOSFET scaling was first described by Dennard in 1974

MOSFET Scaling

Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	1/κ
Doping concentration *Na*	κ
Voltage *V*	1/κ
Current *I*	1/κ
Capacitance *εA/t*	1/κ
Delay time/circuit *VC/I*	1/κ
Power dissipation/circuit *VI*	$1/\kappa^2$
Power density *VI/A*	1

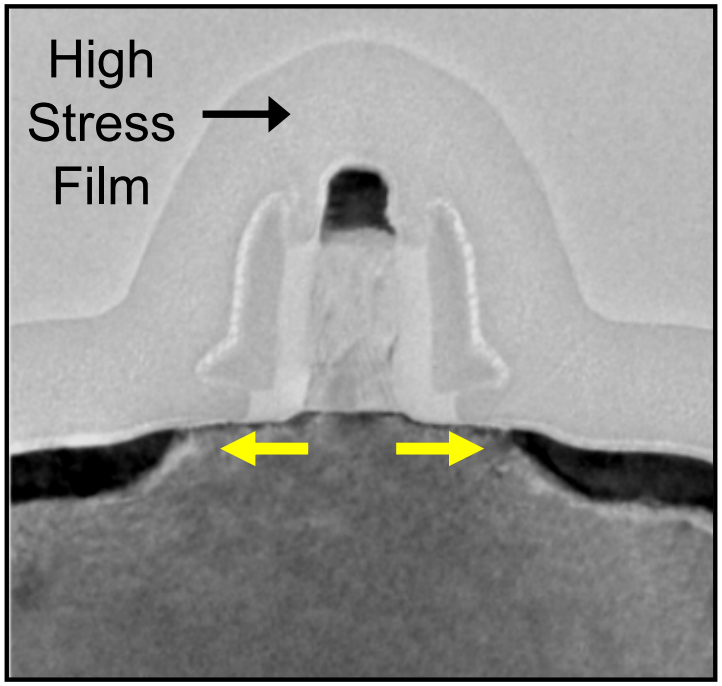


R. Dennard, IEEE JSSC, 1974

Classical MOSFET scaling ENDED at the 130nm node (and nobody noticed …)

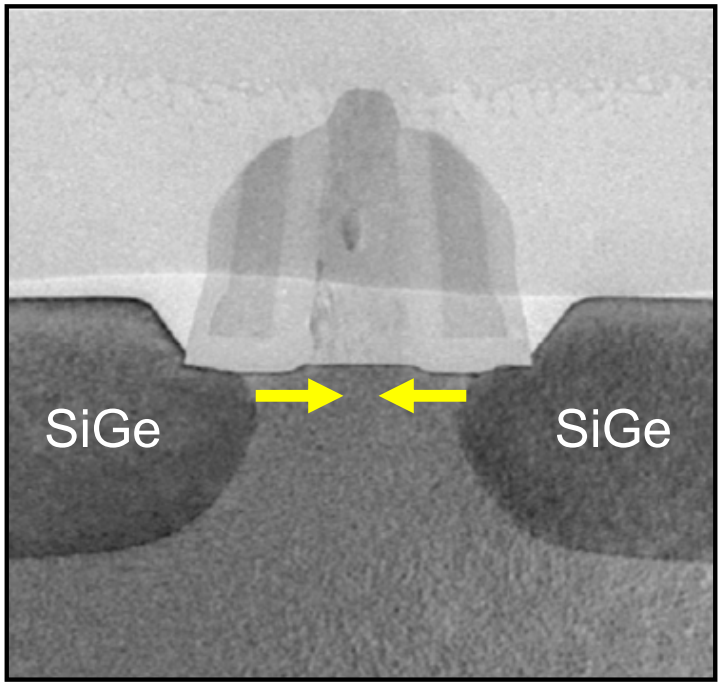
90 nm Strained Silicon Transistors

NMOS



SiN cap layer
Tensile channel strain

PMOS

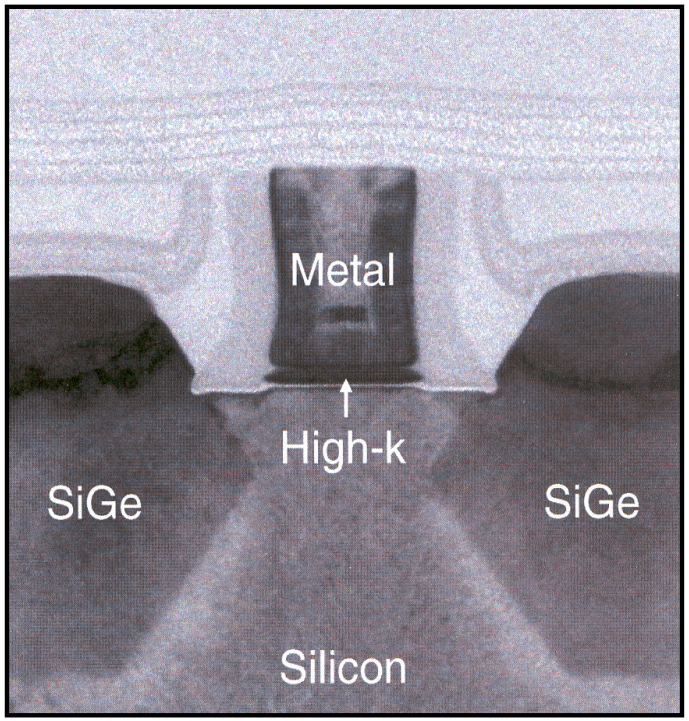


SiGe source-drain
Compressive channel strain

Strained silicon provided increased drive currents, making up for the loss of classical Dennard scaling

45nm High-k + Metal Gate Transistors

45 nm HK+MG



Hafnium-based dielectric

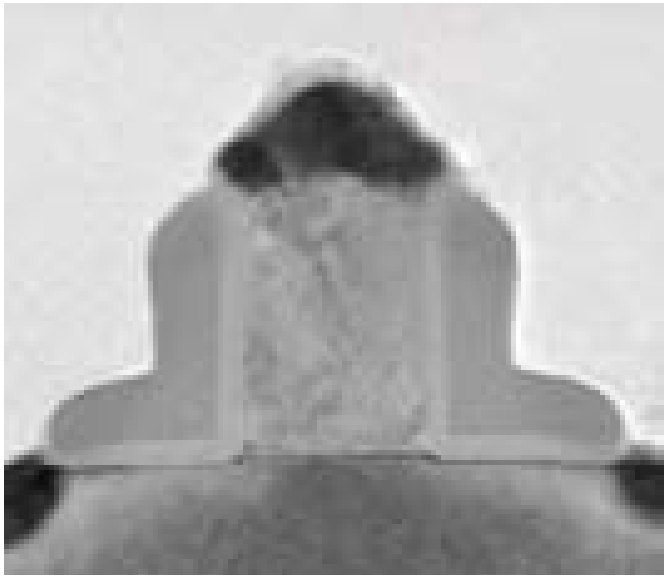
Metal gate electrode

High-k + metal gate transistors restored gate oxide scaling at the 45nm node

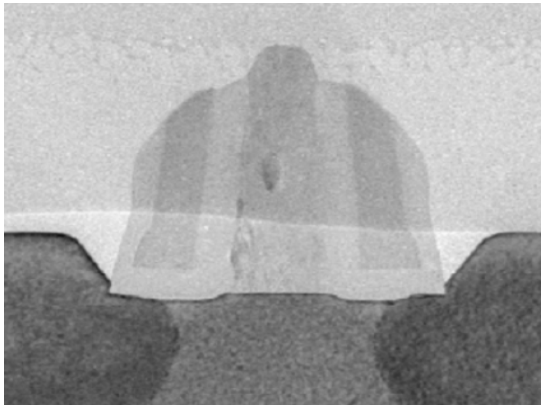
Changes in Scaling

THEN

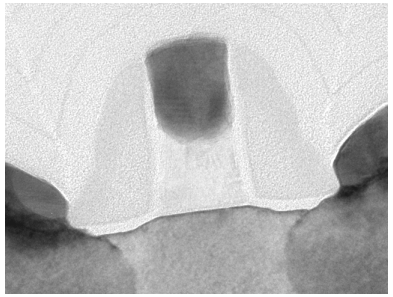
- Scaling drove down cost
- Scaling drove performance
- Performance constrained
- Active power dominates
- Independent design-process



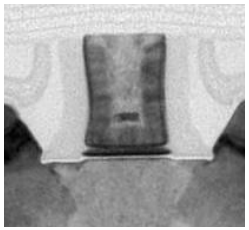
130nm



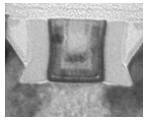
90nm



65nm



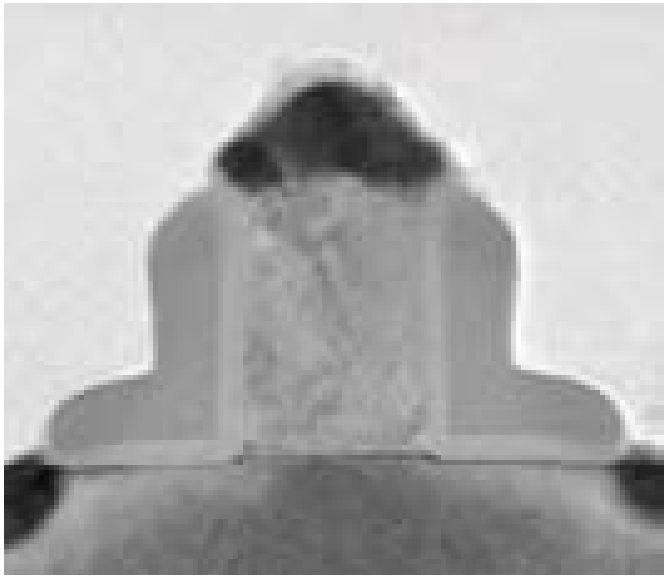
45nm



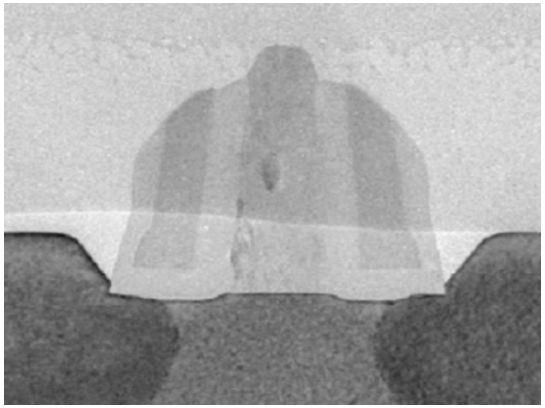
32nm

Changes in Scaling

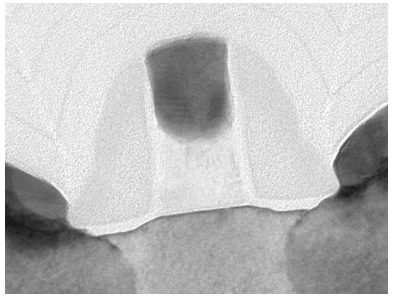
THEN	NOW
• Scaling drove down cost	• Scaling drives down cost
• Scaling drove performance	• Materials drive performance
• Performance constrained	• Power constrained
• Active power dominates	• Standby power dominates
• Independent design-process	• Collaborative design-process



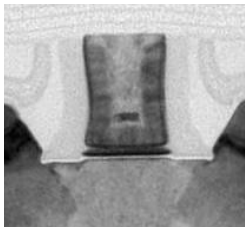
130nm



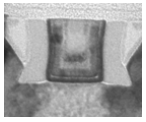
90nm



65nm

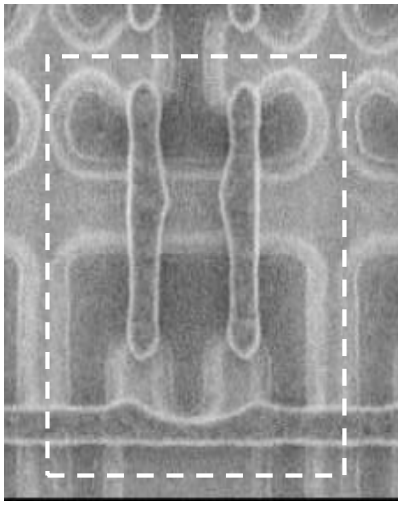


45nm

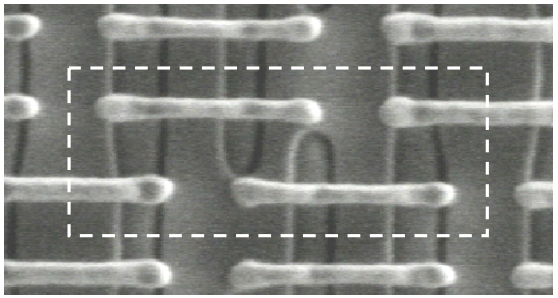


32nm

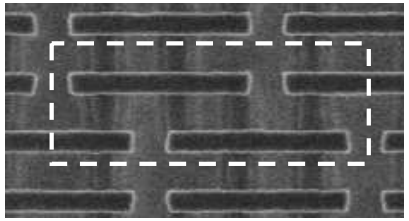
Consistent 2-year scaling



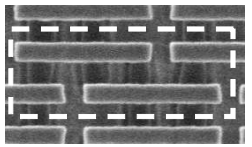
90nm – TALL
1.0 μm²



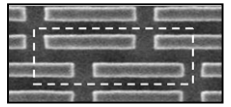
65nm – WIDE - 0.57 μm²



45nm – WIDE
0.346 μm²

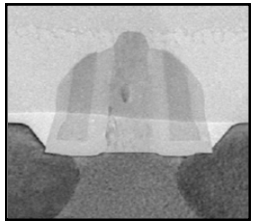
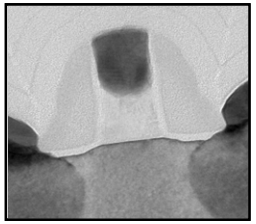
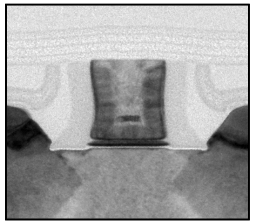
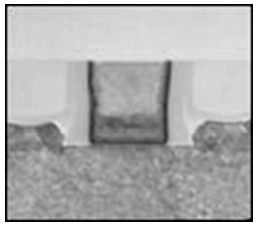
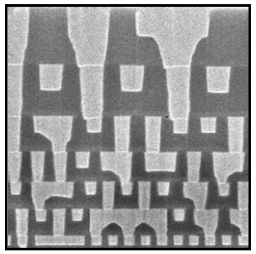
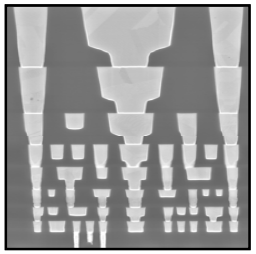
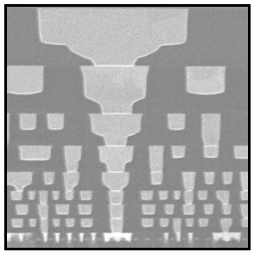
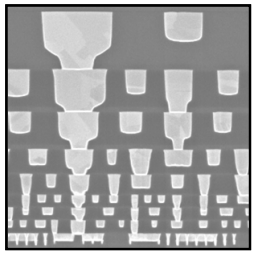
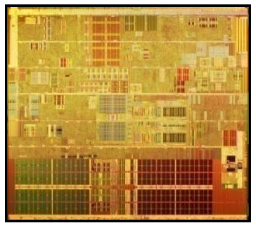
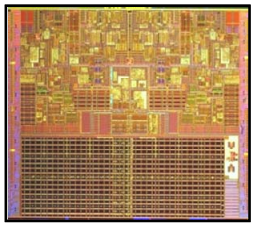
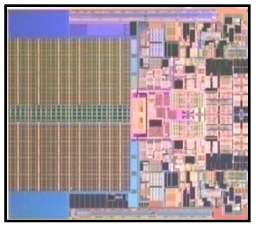
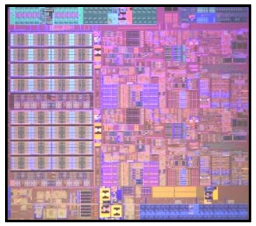
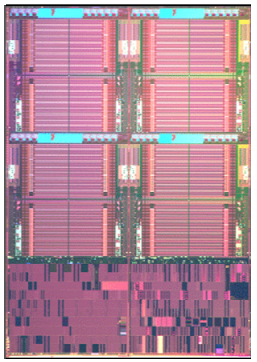


32nm – WIDE
0.171 μm²

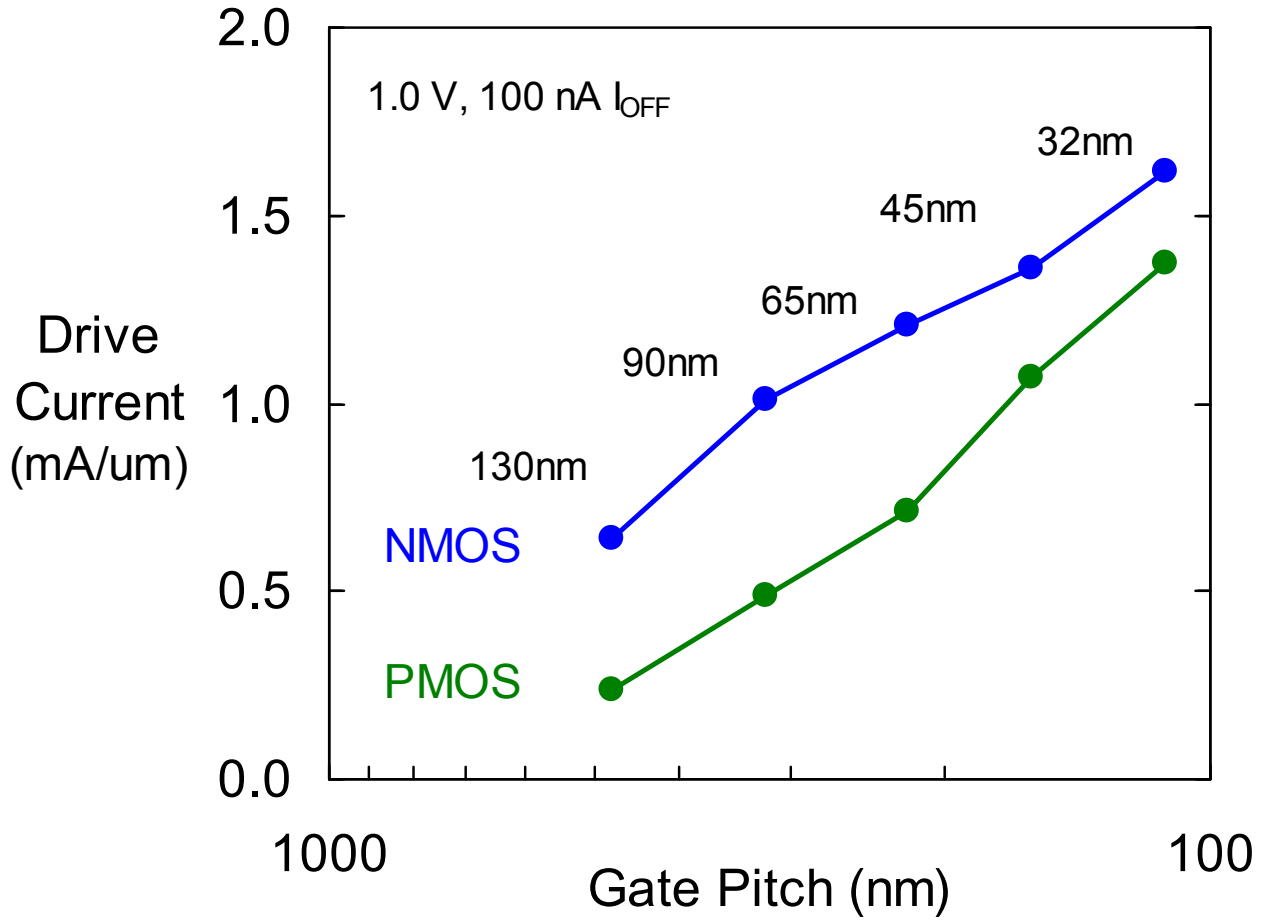


22nm – WIDE
0.092 μm²

90 nm	65 nm	45 nm	32 nm	22 nm
2003	2005	2007	2009	2011 *projected*

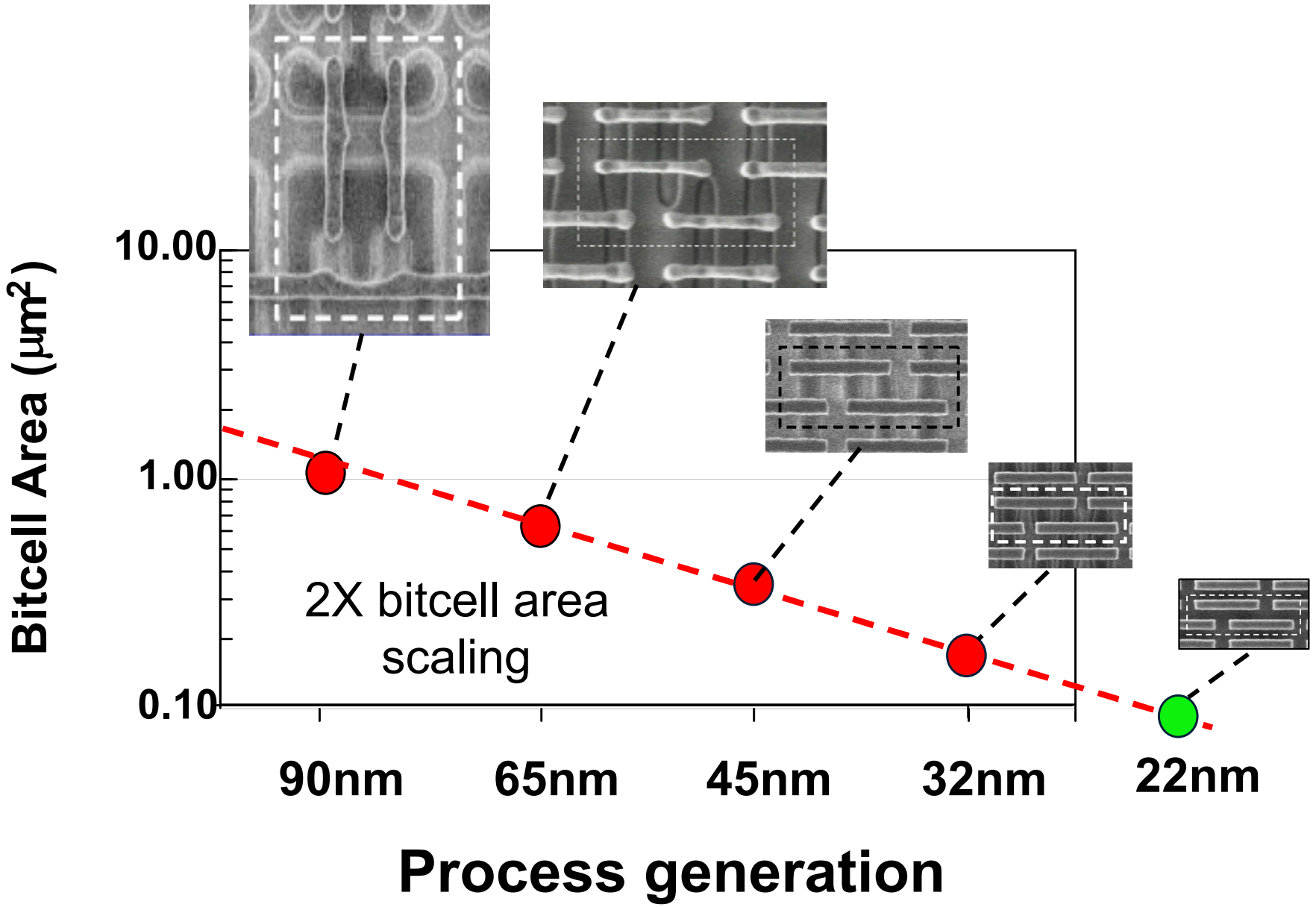














Transistor Performance



32 nm transistors continue Moore's Law with improved drive at reduced pitch

Consistent SRAM Density Scaling

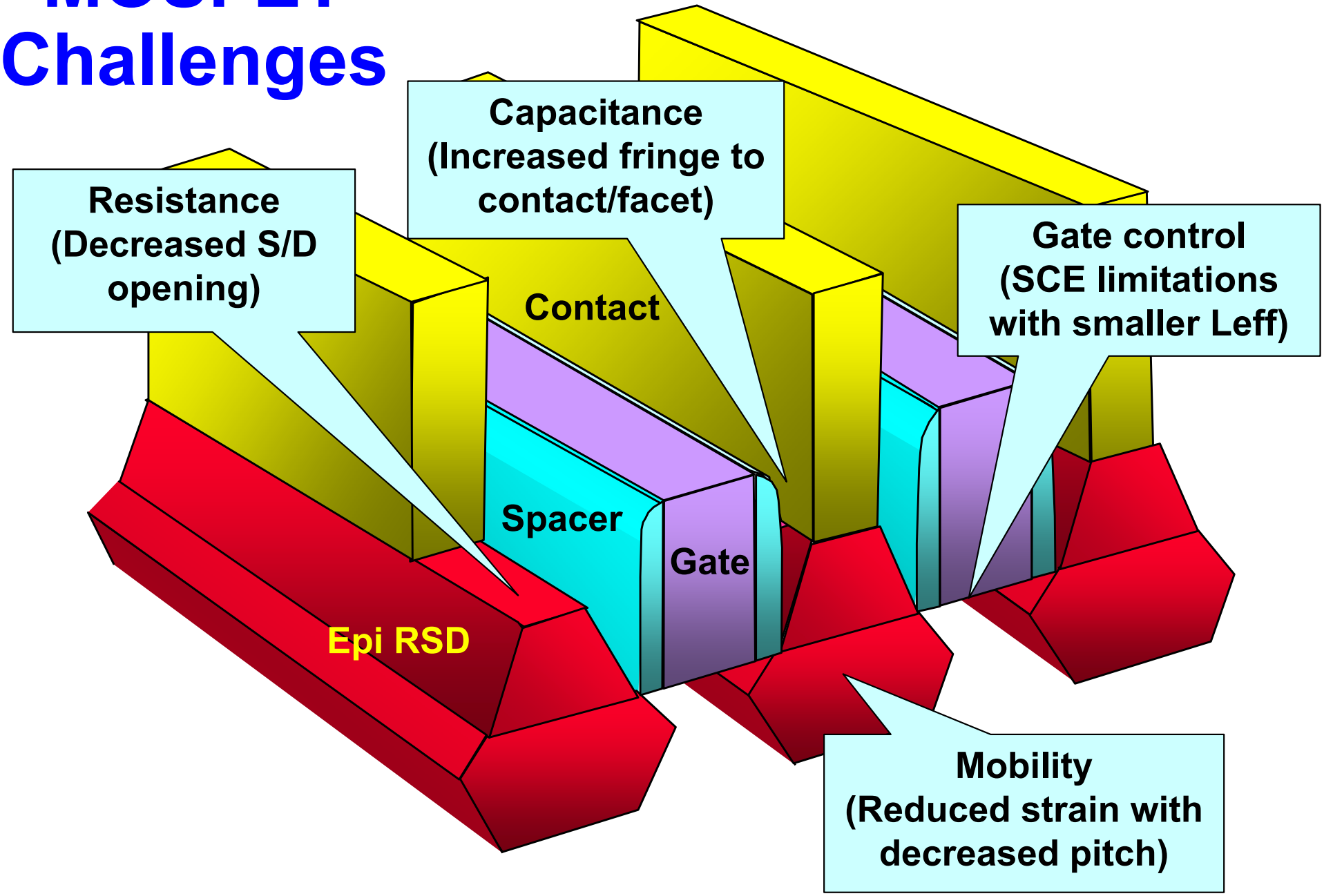


K. Zhang, ISCC, 2009; M. Bohr IDF 2010

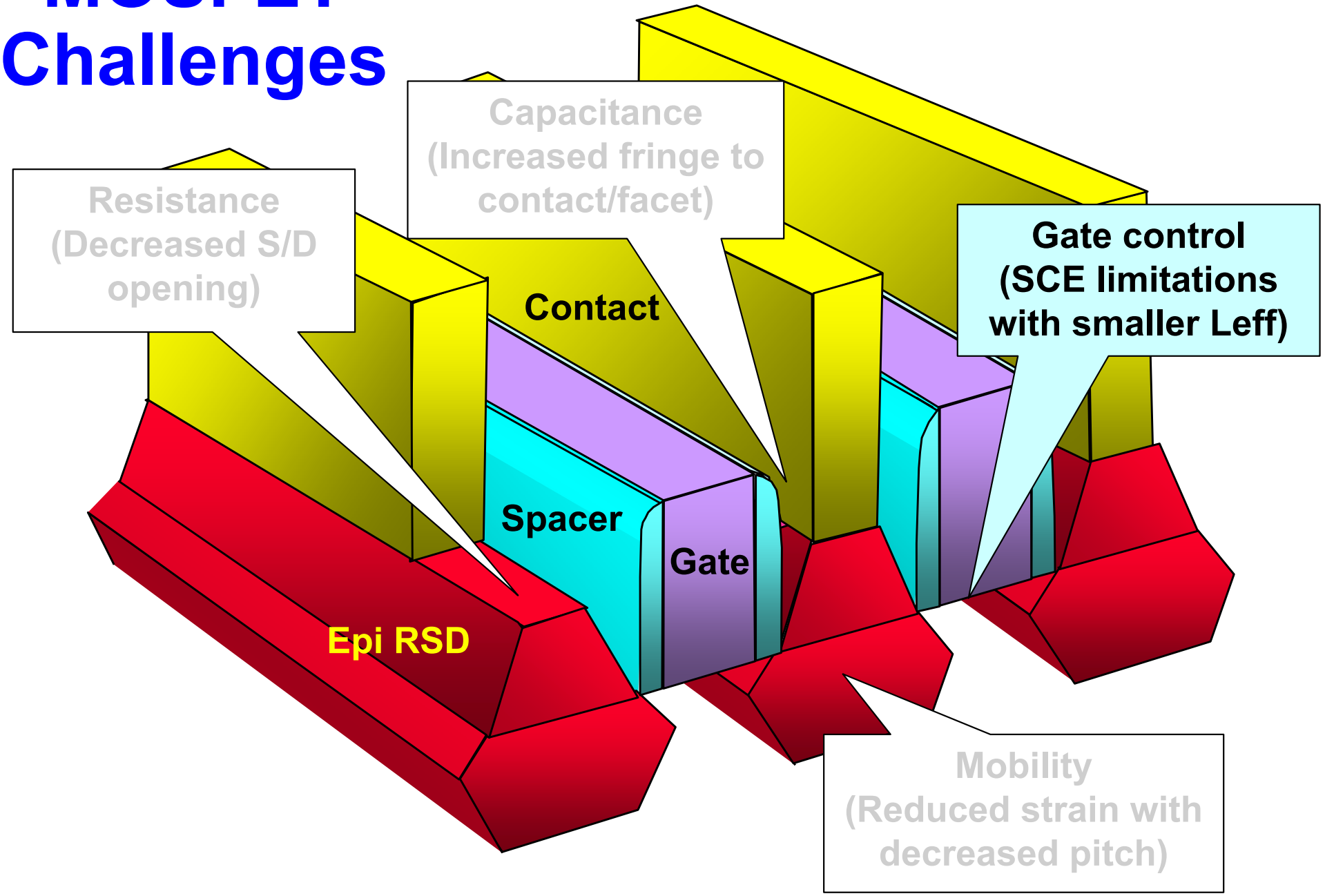
AGENDA

- Scaling
- Gate control
- Mobility
- Resistance
- Capacitance
- Summary

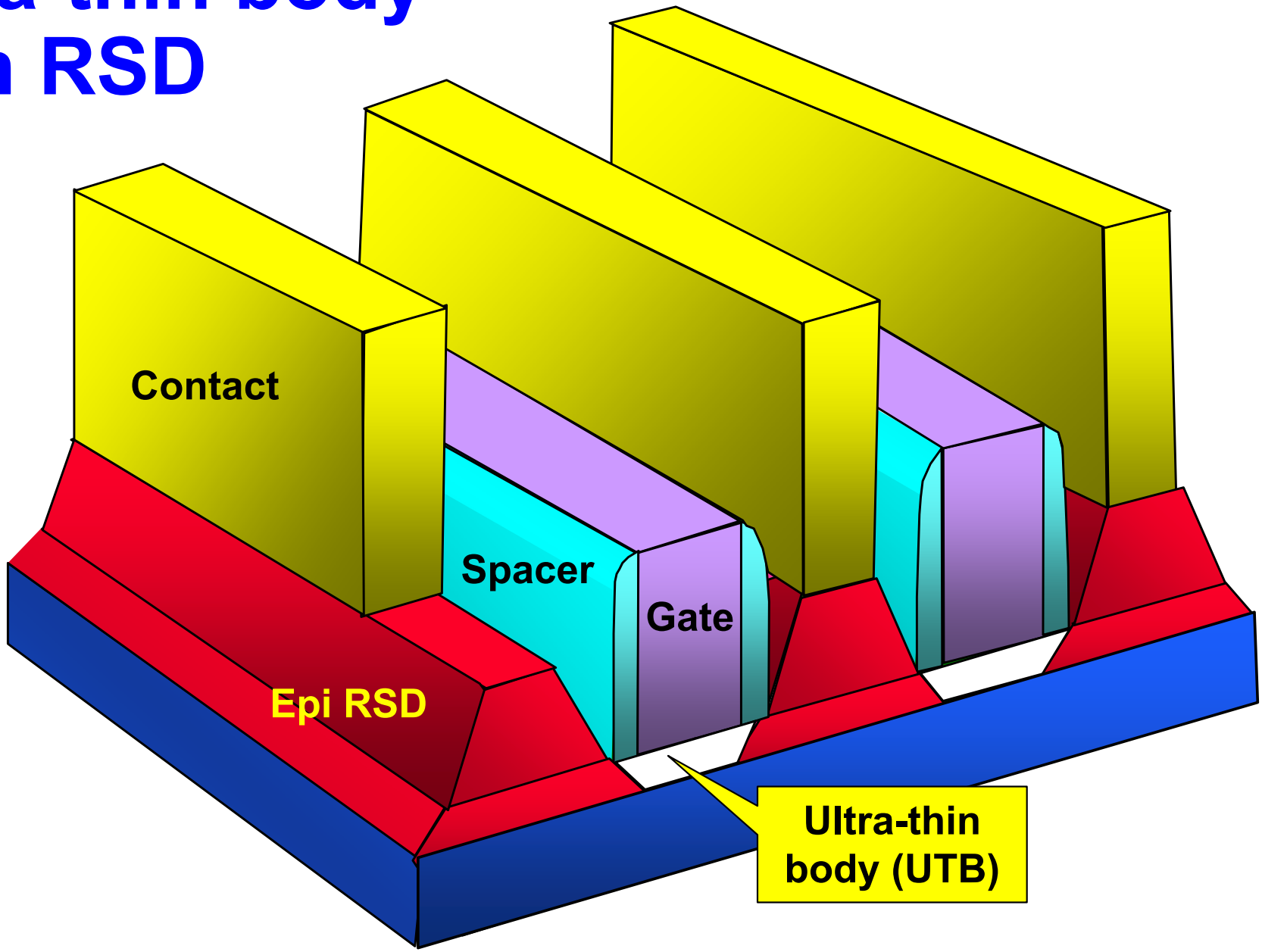
MOSFET Challenges



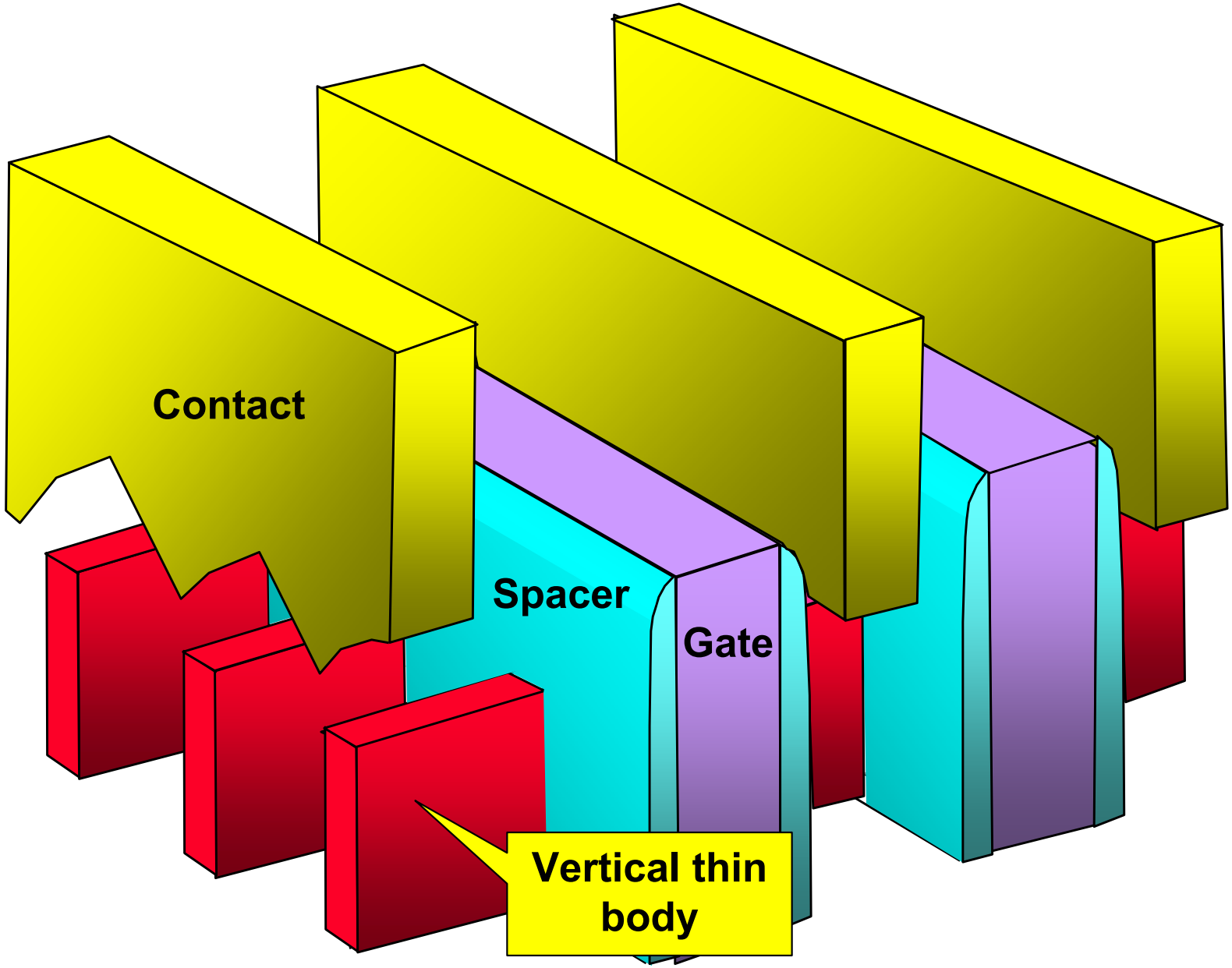
MOSFET Challenges



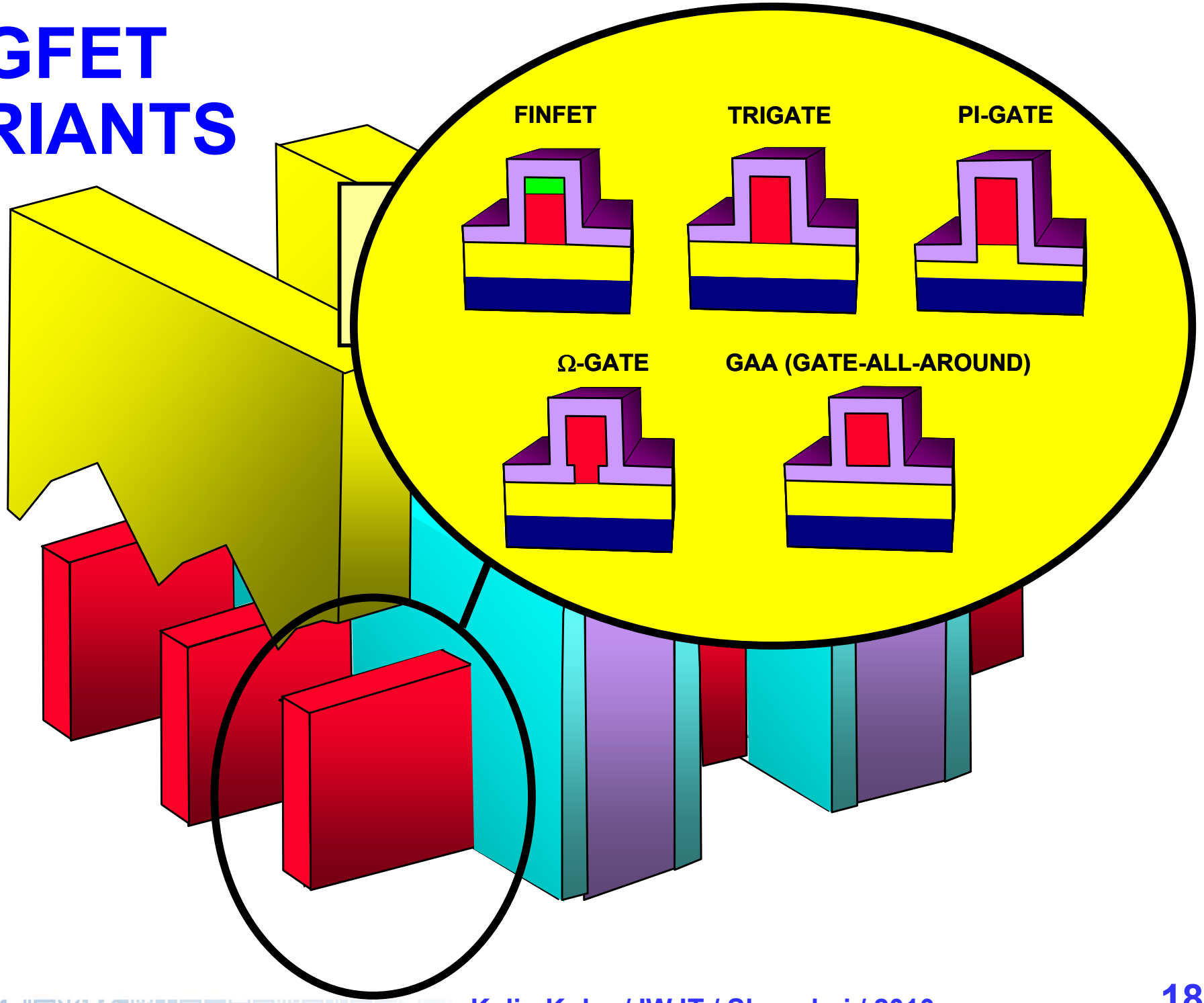
Ultra-thin body with RSD



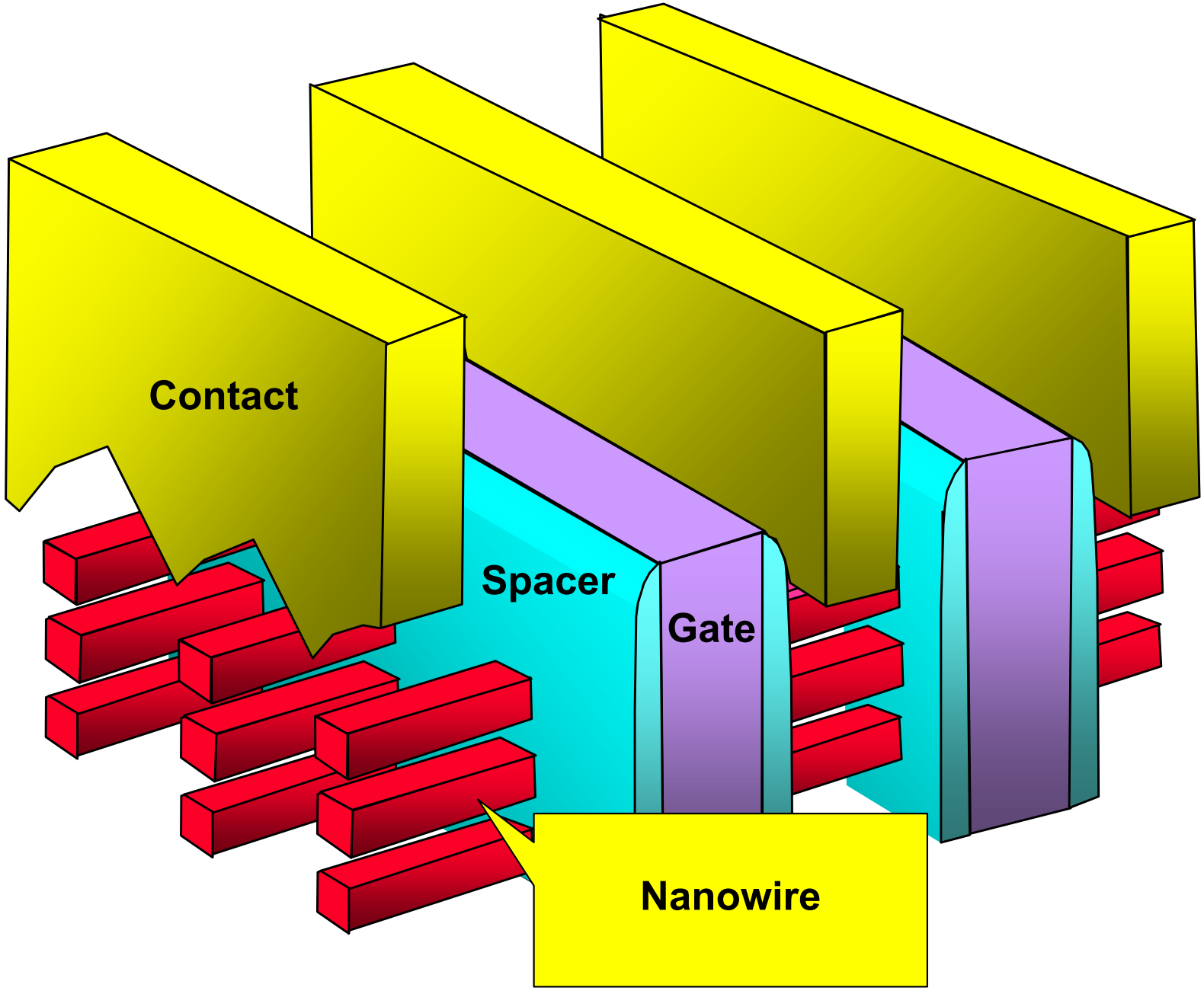
MuGFET



MuGFET VARIANTS



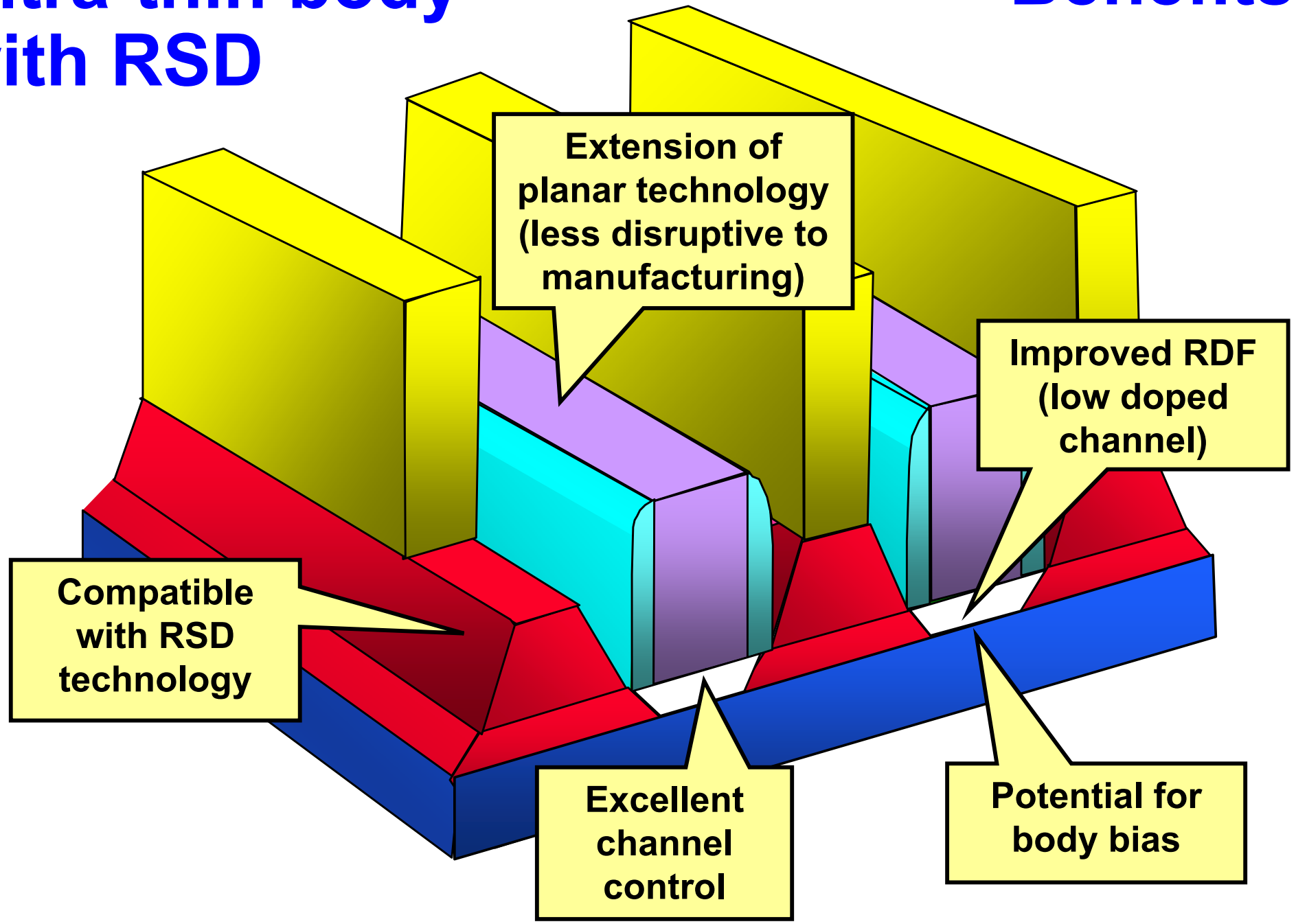
Nanowire



Looking at all these in more detail

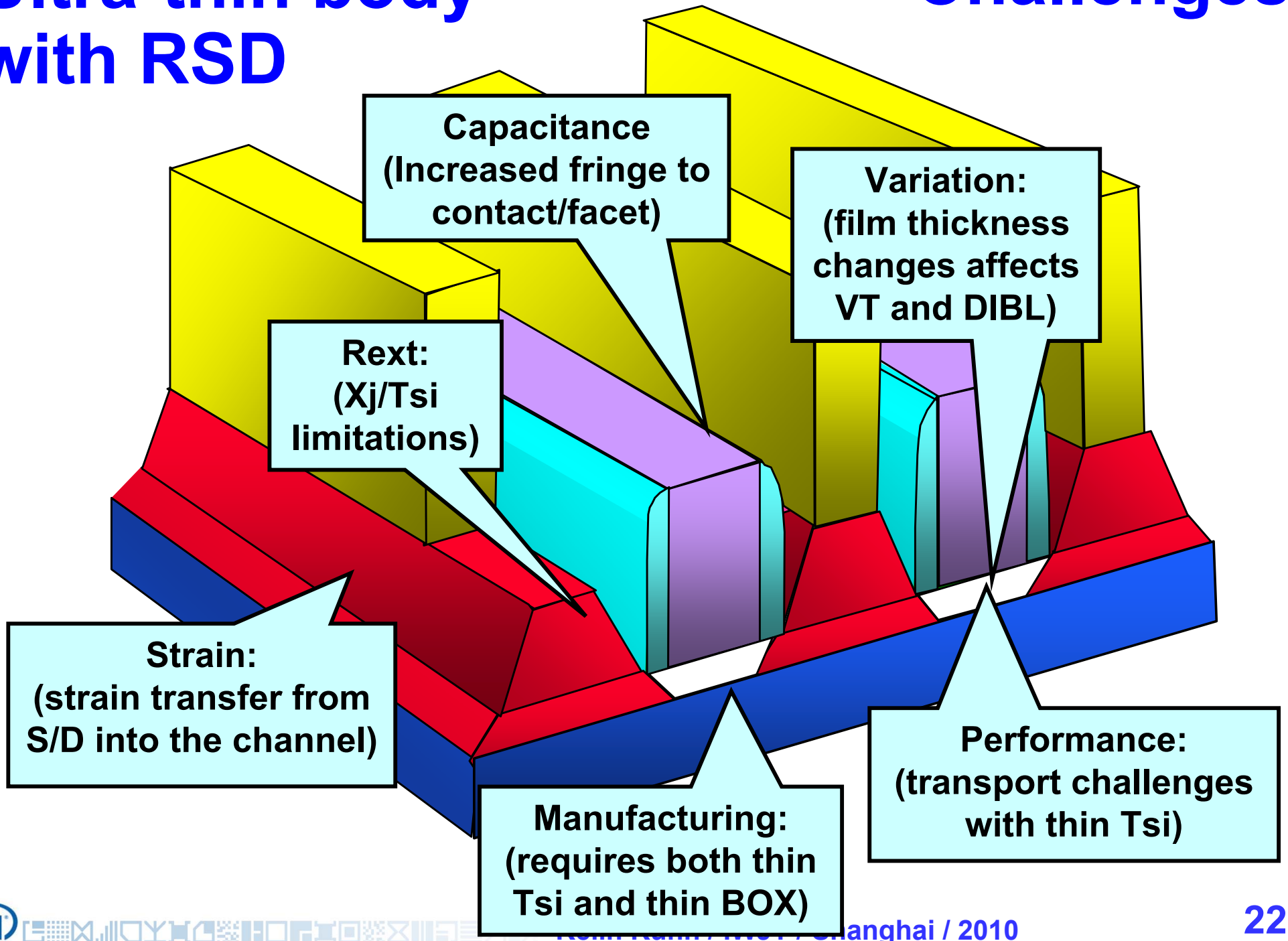
Ultra-thin body with RSD

Benefits



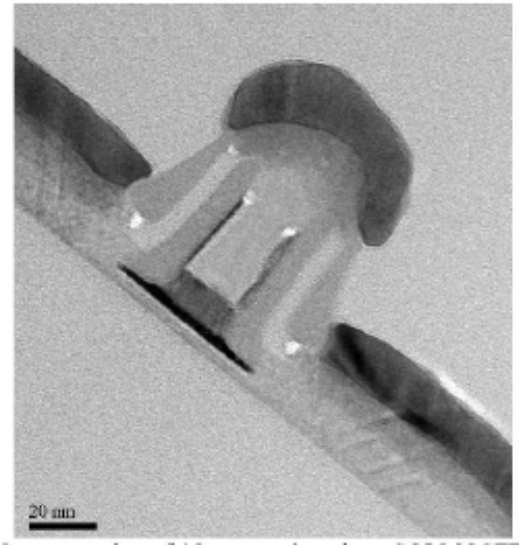
Ultra-thin body with RSD

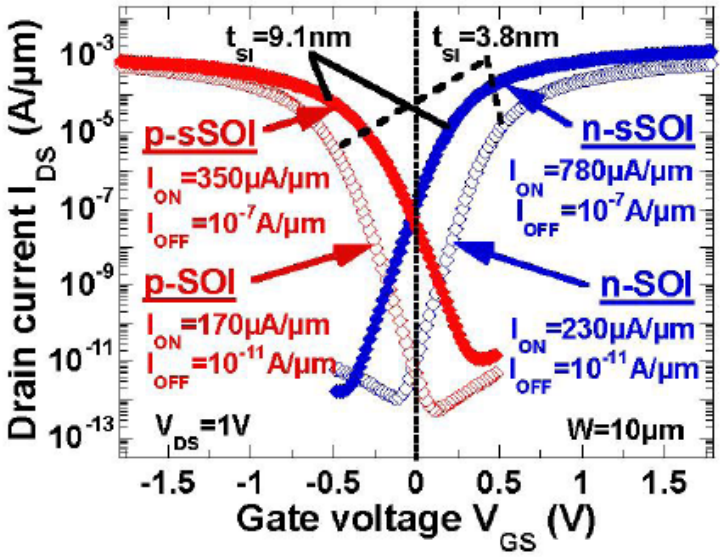
Challenges

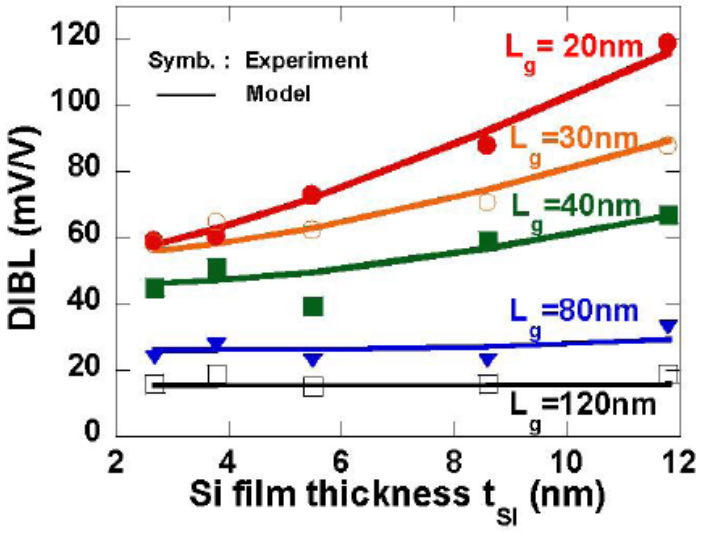


Ultra-thin body

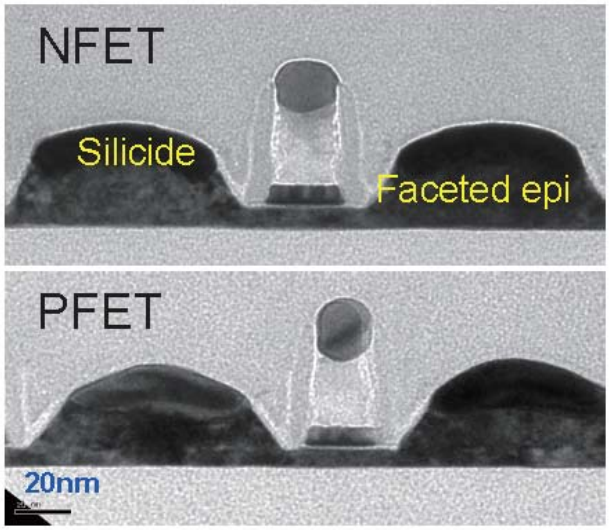
Barral – CEA-LETI– IEDM 2007

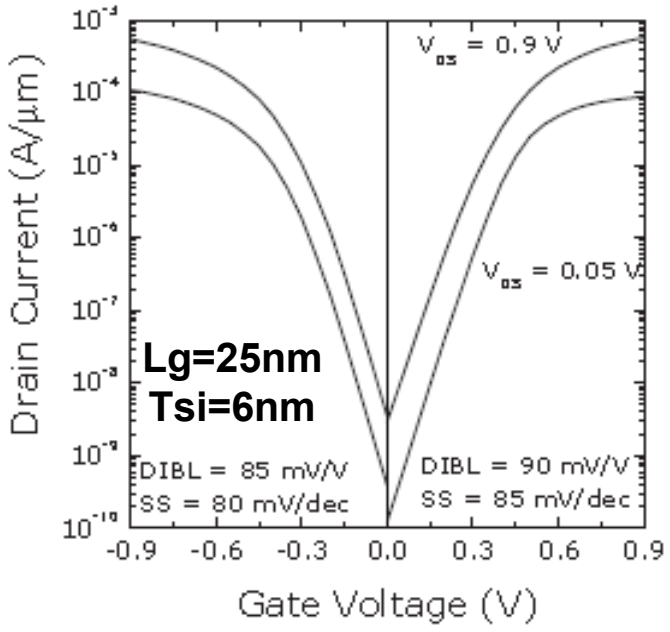


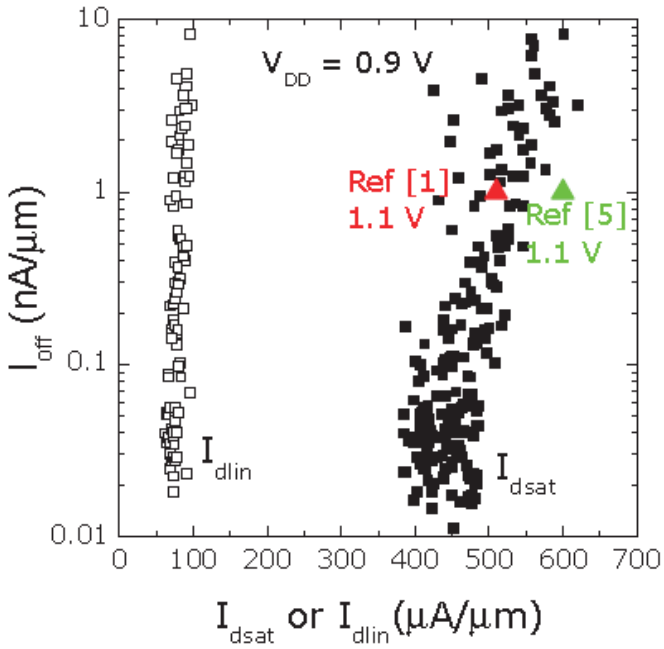




Cheng – IBM – VLSI 2009

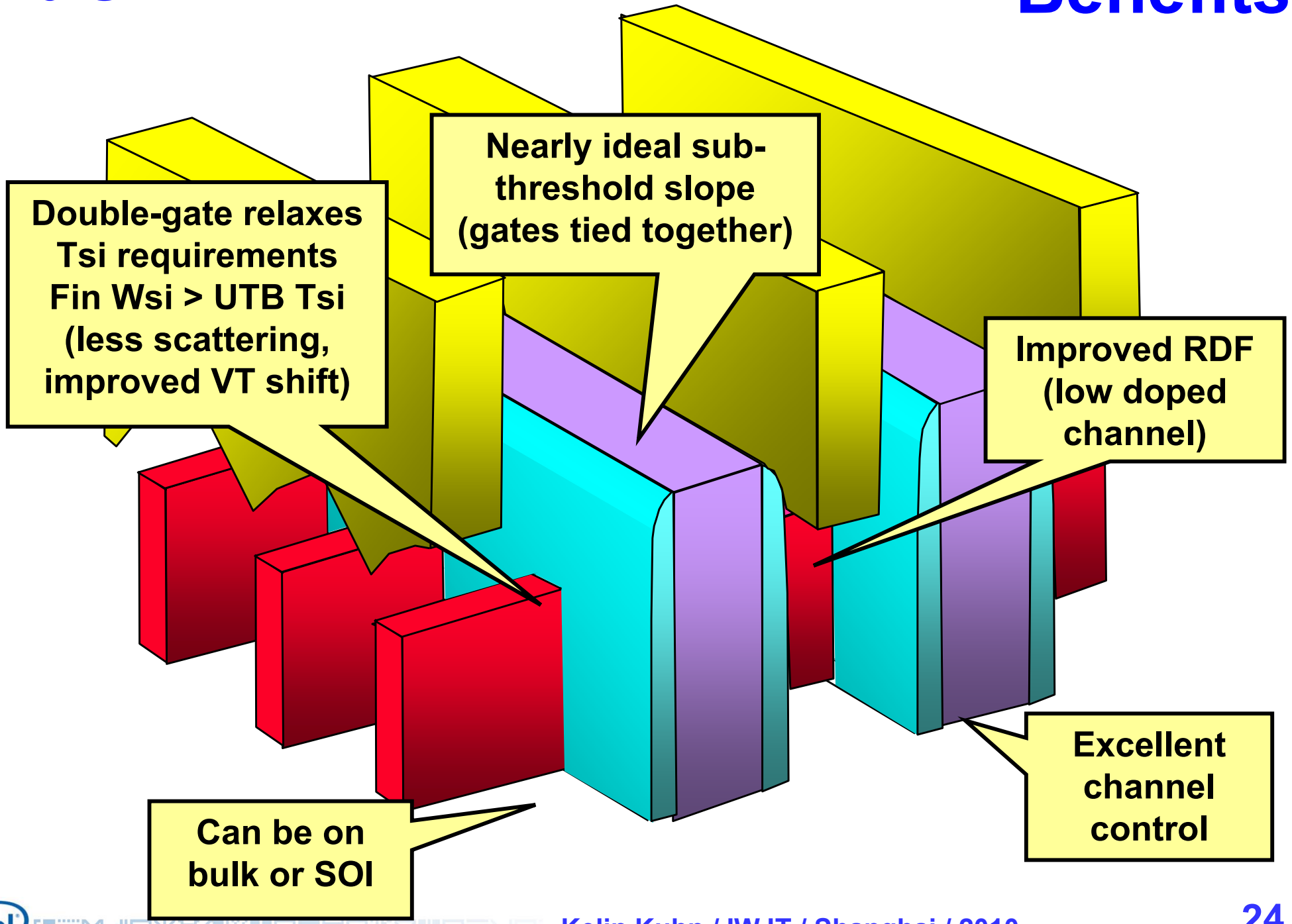






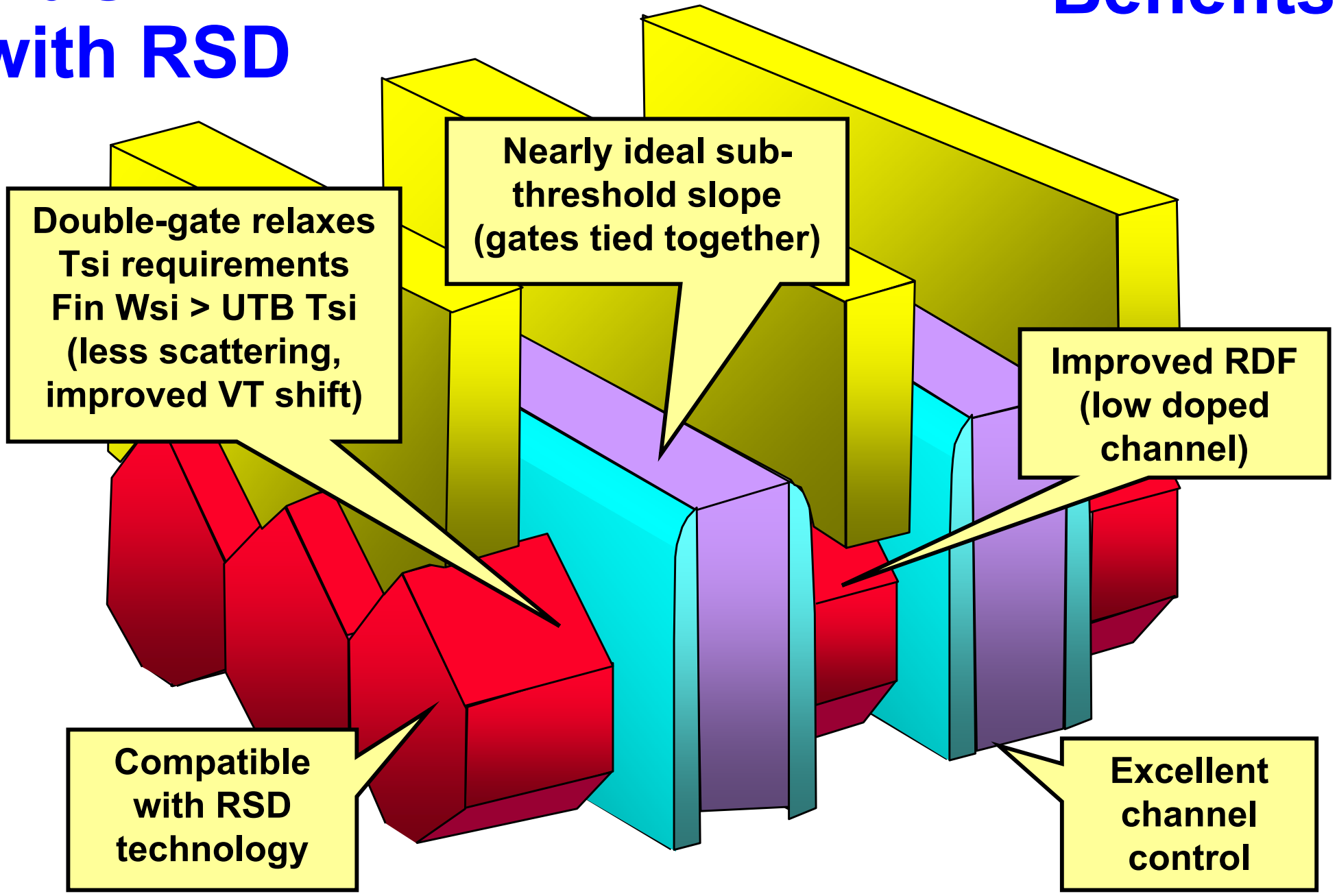
MuGFET

Benefits



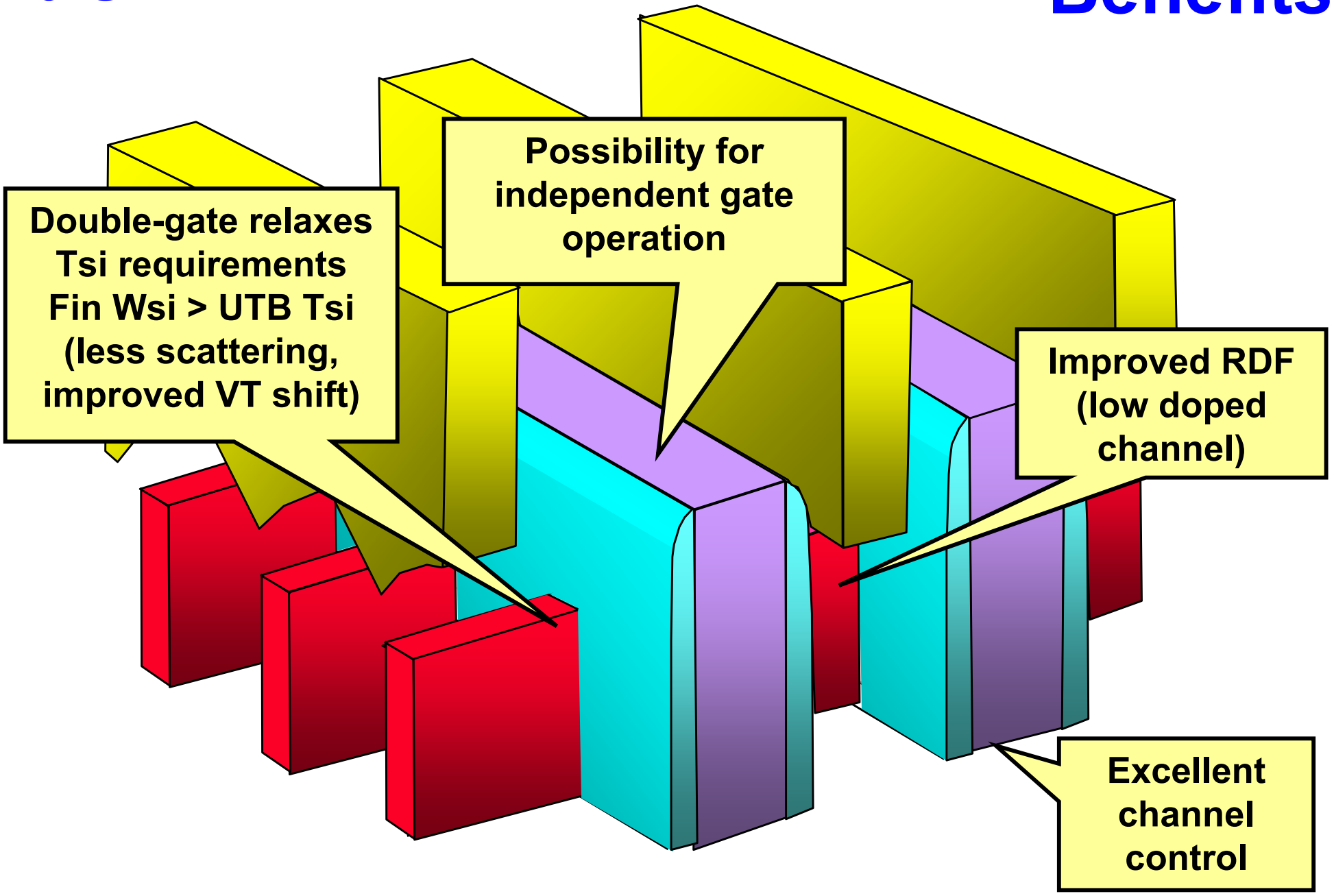
MuGFET with RSD

Benefits

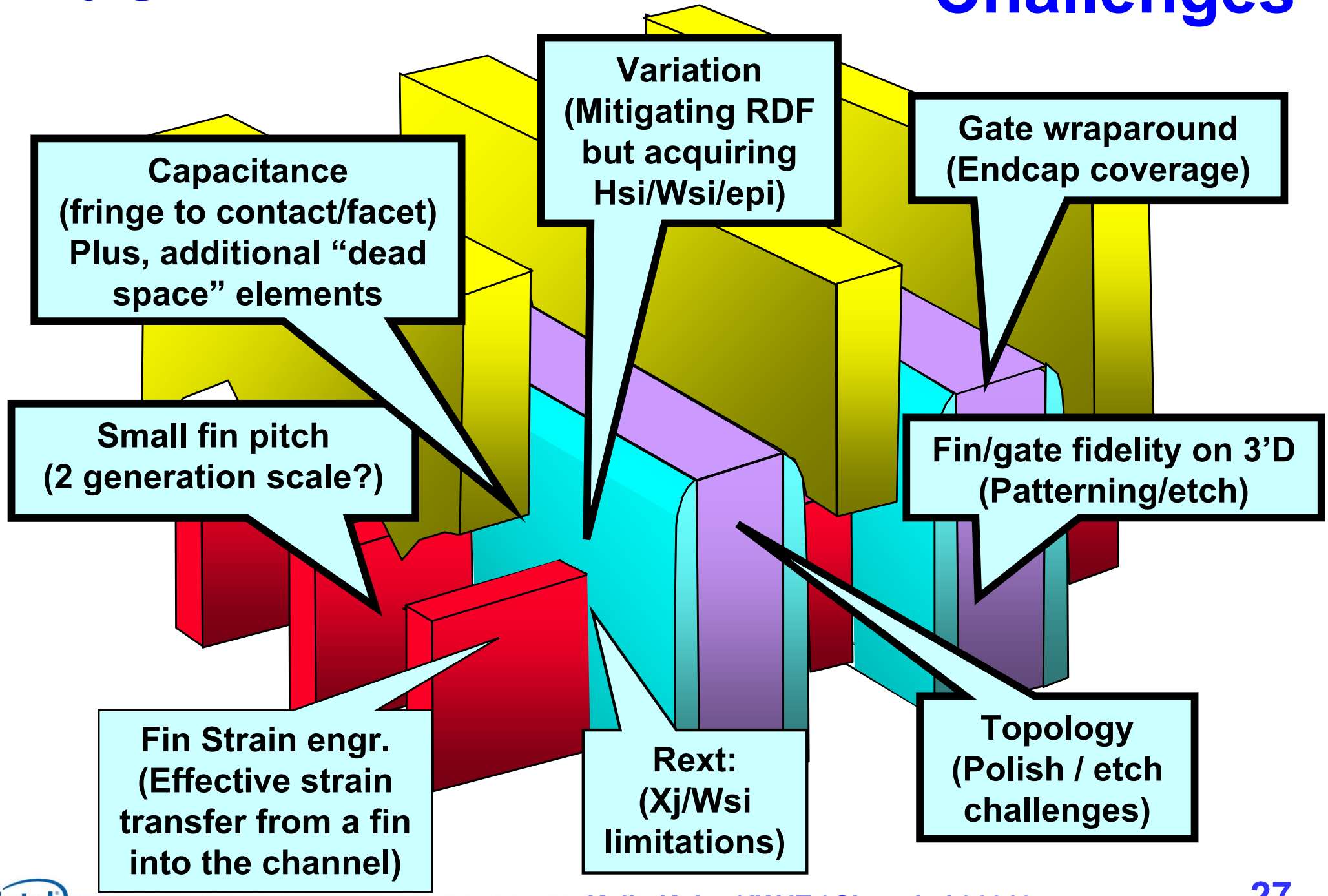


MuGFET

Benefits



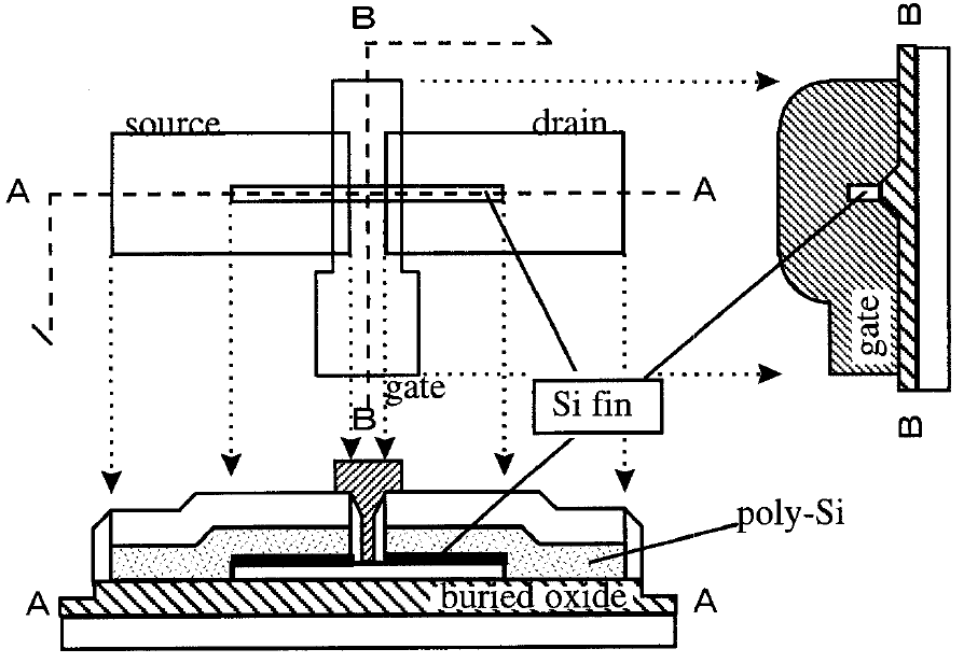
MuGFET Challenges



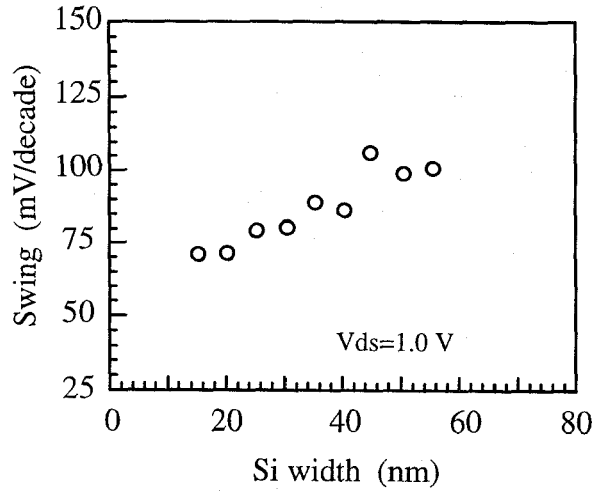
Hisamoto – Hitachi / Berkeley– IEDM 1998 [3]

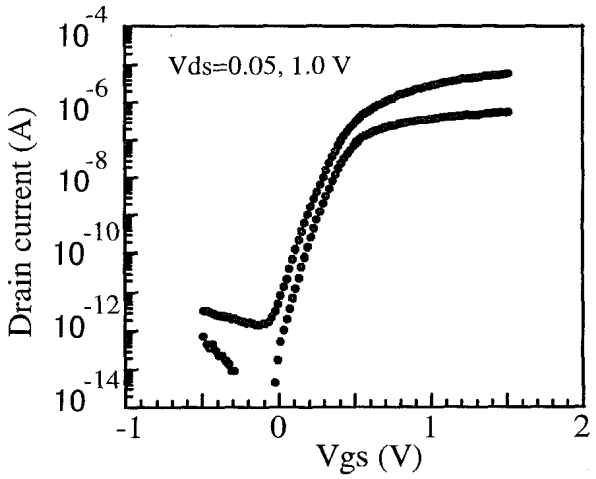
A Folded-channel MOSFET for Deep-sub-tenth Micron Era

Digh Hisamoto, Wen-Chin Lee*, Jakub Kedzierski*, Erik Anderson**, Hideki Takeuchi+,
Kazuya Asano++, Tsu-Jae King*, Jeffrey Bokor*, and Chenming Hu*
Central Research Laboratory, Hitachi Ltd., *) EECS, UC Berkeley,
**) Lawrence Berkeley Laboratory, +) Nippon Steel Corp., ++) NKK Corp.



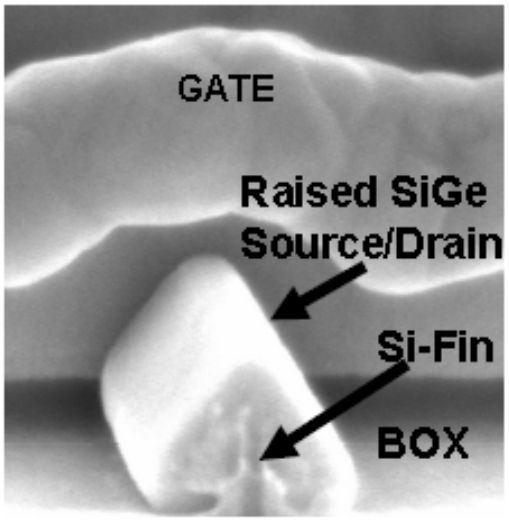
. 1 Folded channel MOSFET layout design and device structure.
: bottom is A-A cross section, and the right is B-B cross section

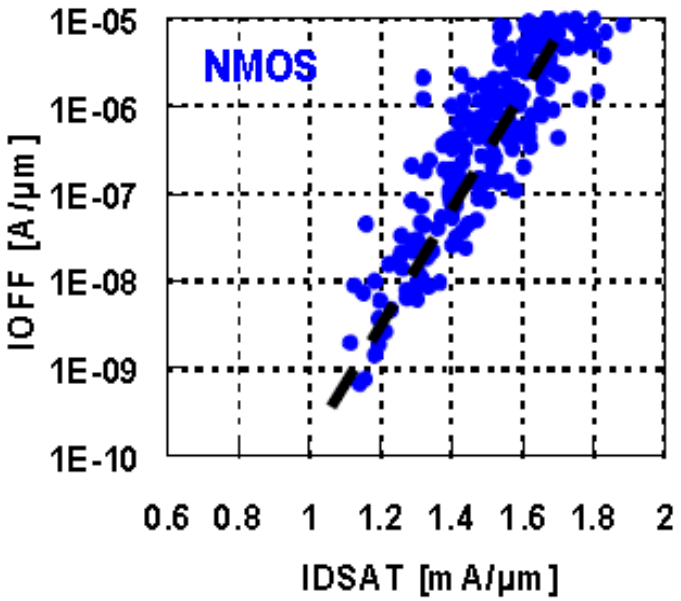


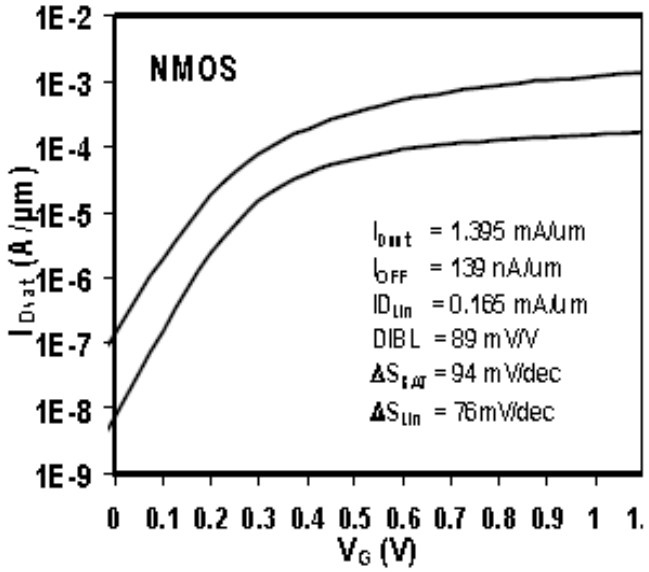


MuGFET

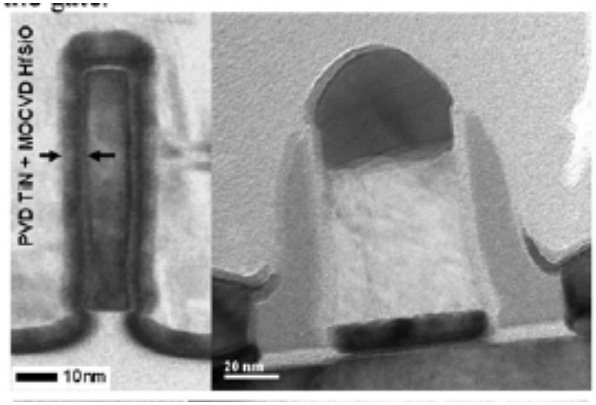
Kavalieros – Intel – IEDM 2006

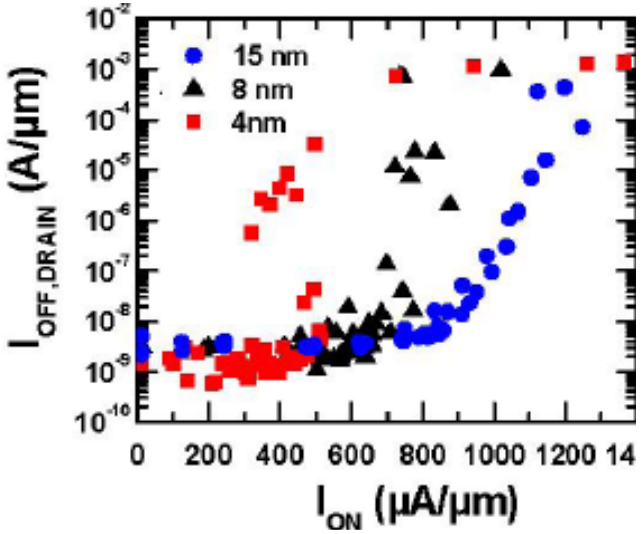


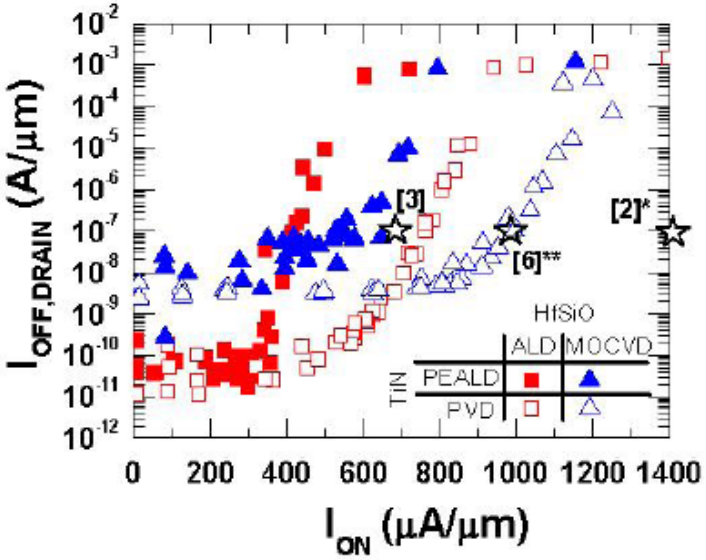




Vellianitis – NXP-TSMC – IEDM 2007

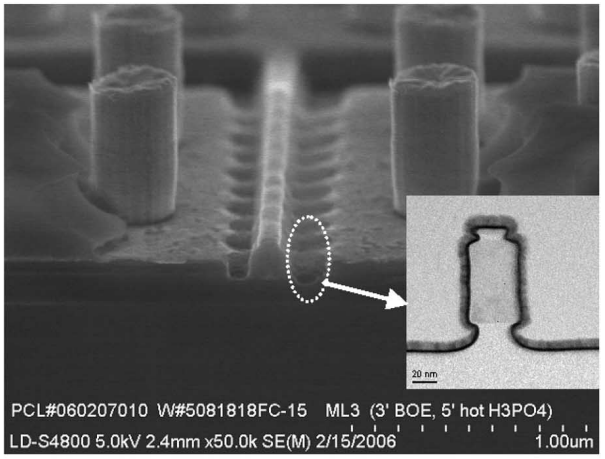


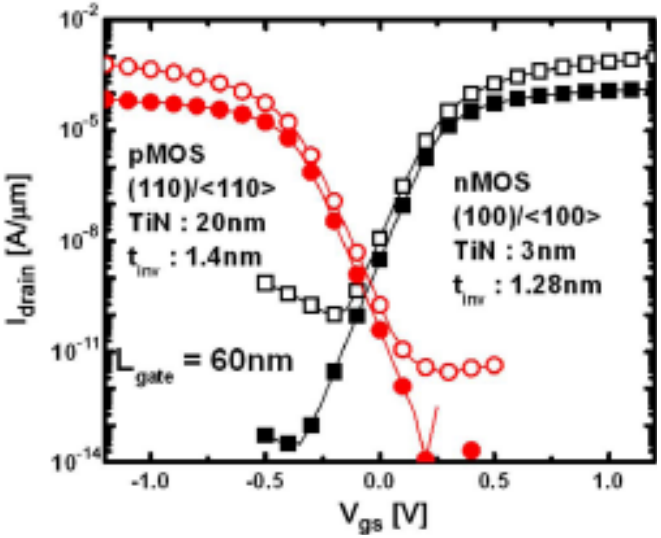


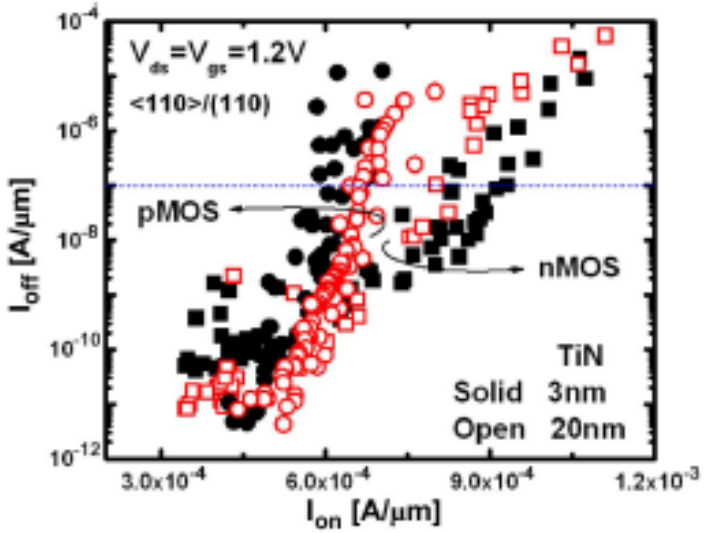


MuGFET

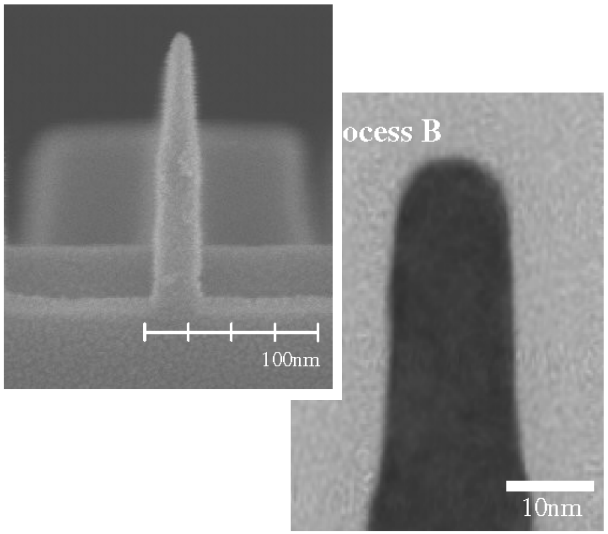
Kang – Sematech – VLSI 2008

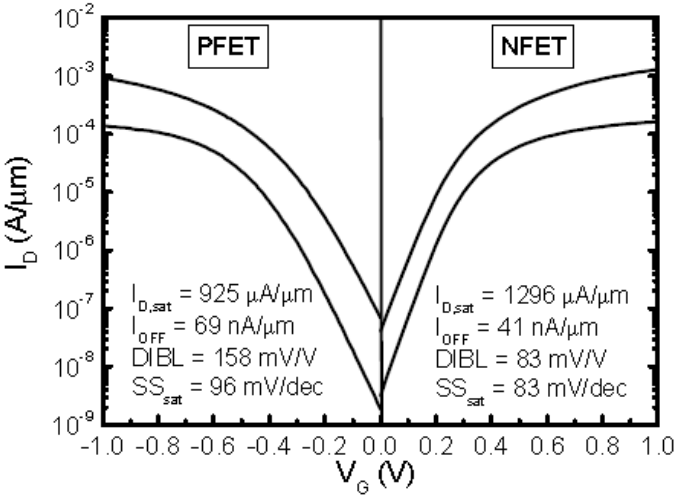


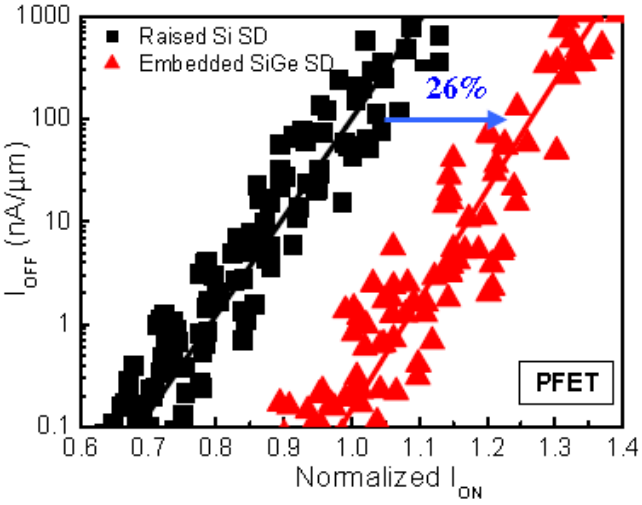




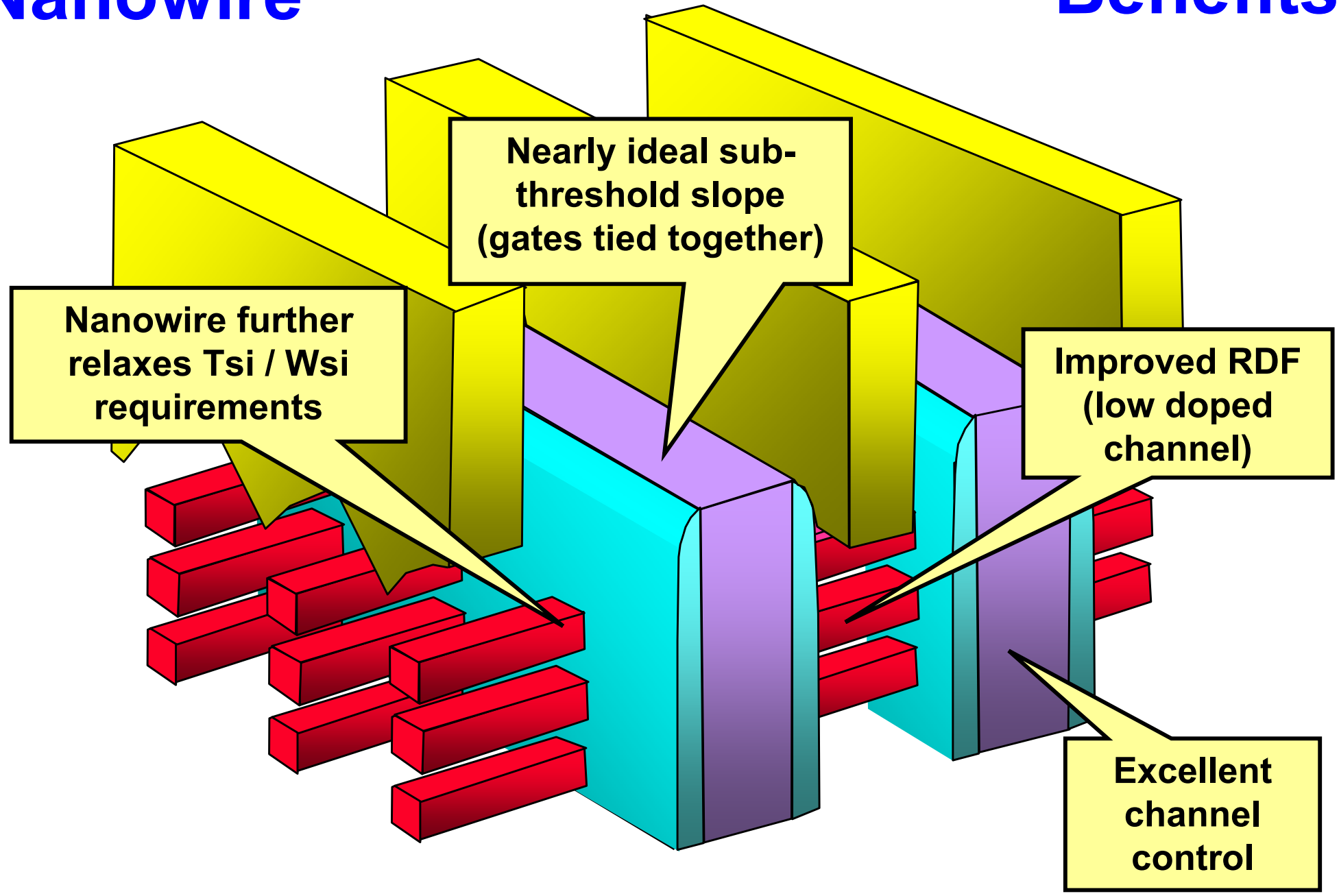
Chang – TSMC – IEDM 2009



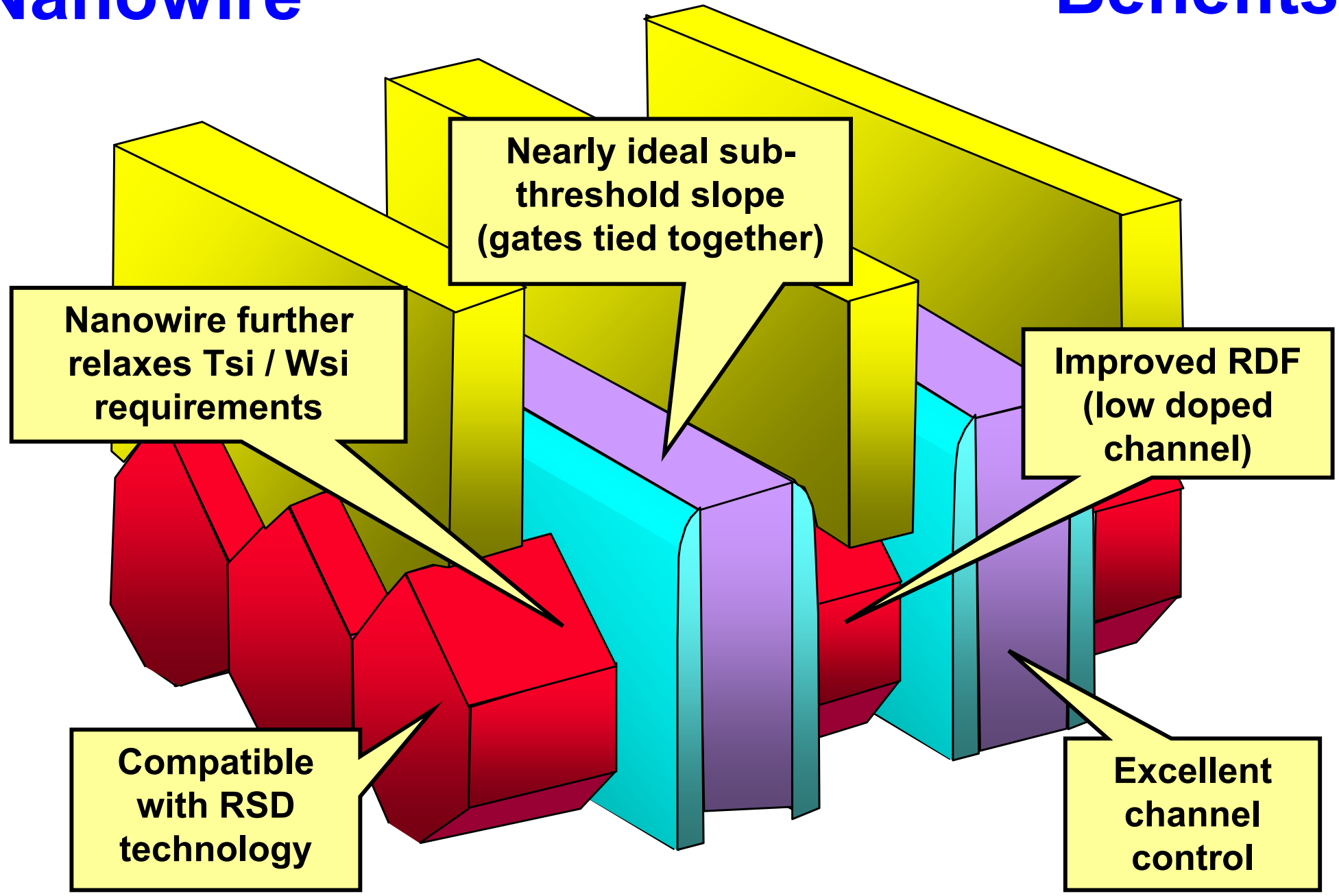




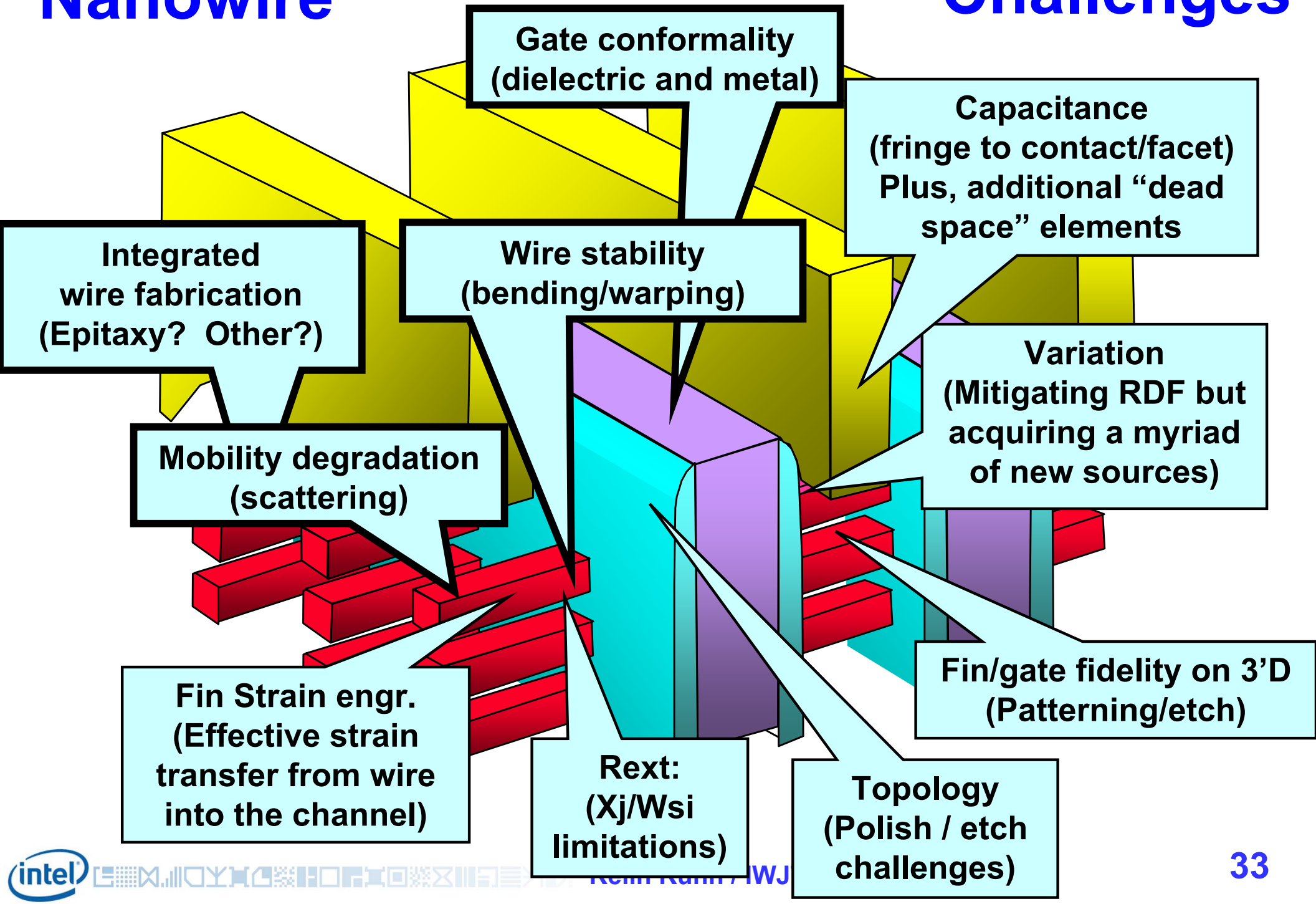
Nanowire Benefits



Nanowire Benefits

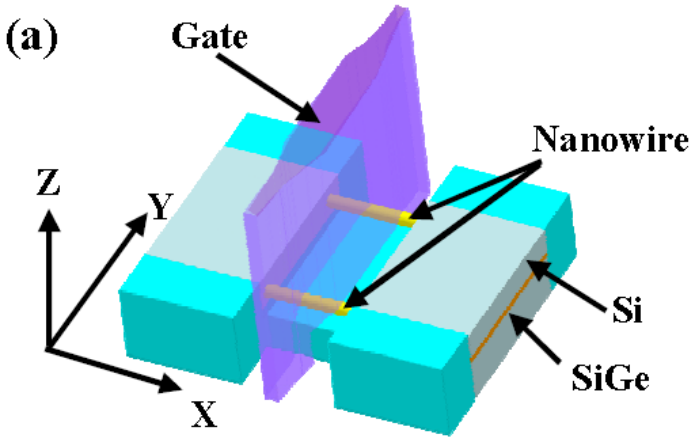


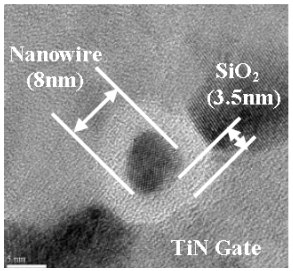
Nanowire Challenges

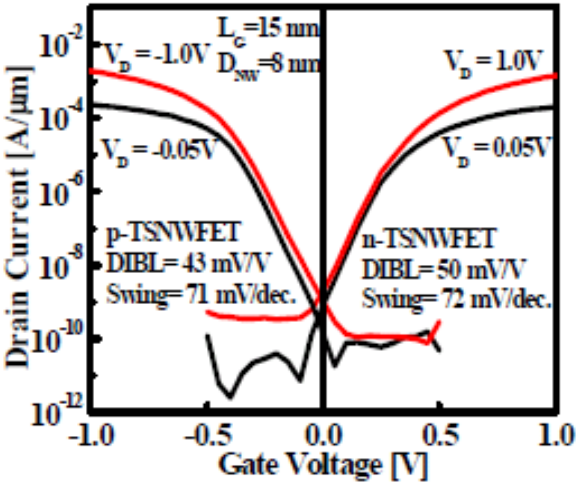


Nanowire FETs

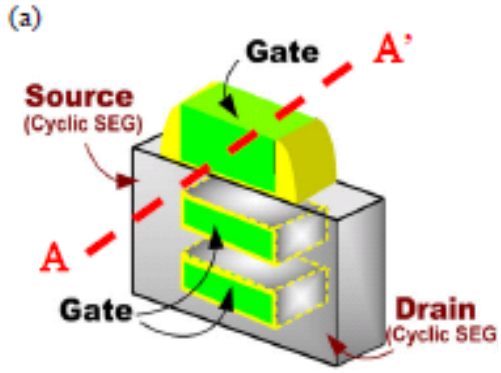
Yeo – Samsung – IEDM 2006

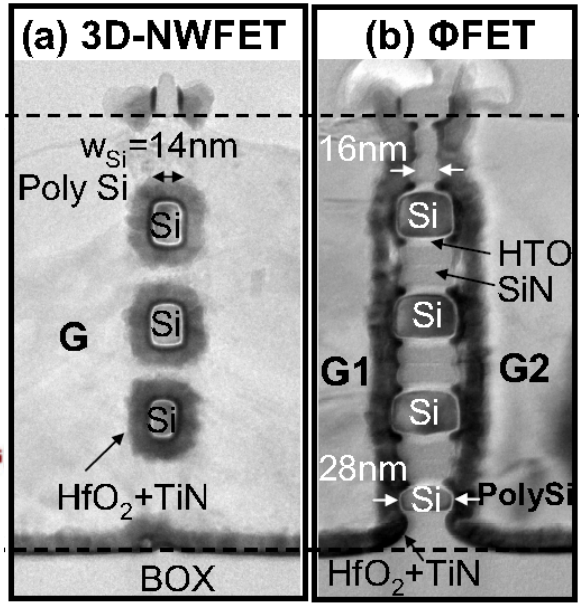


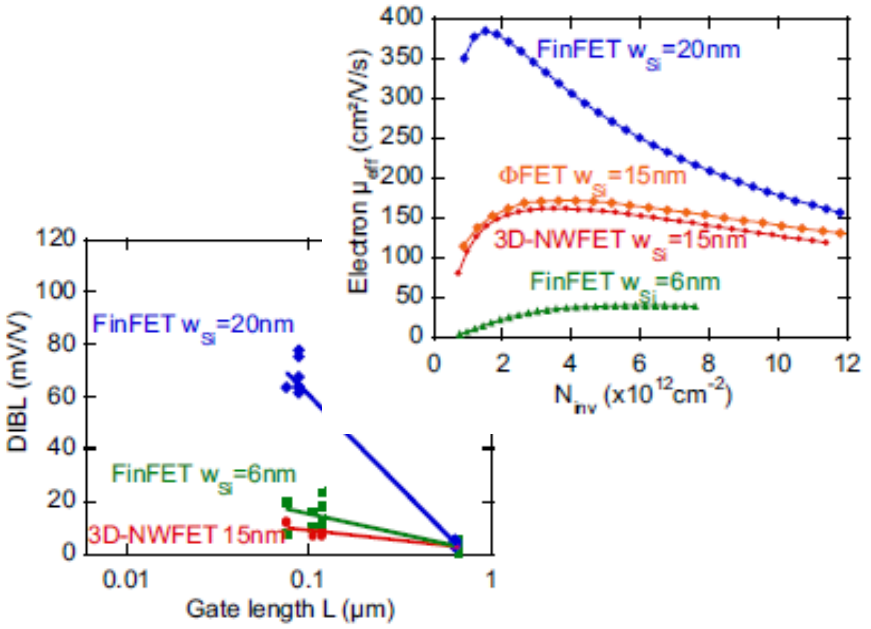




Dupre – CEA-LETI – IEDM 2008

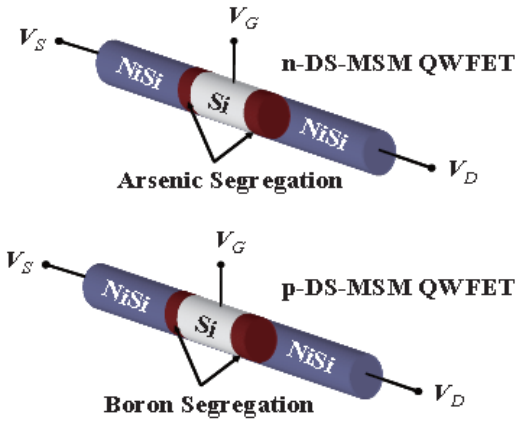


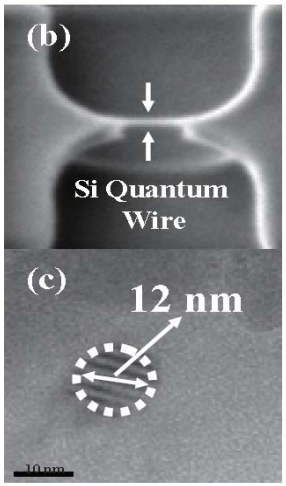


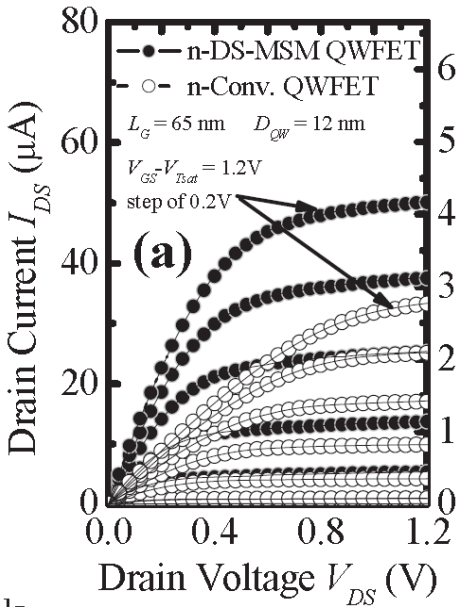


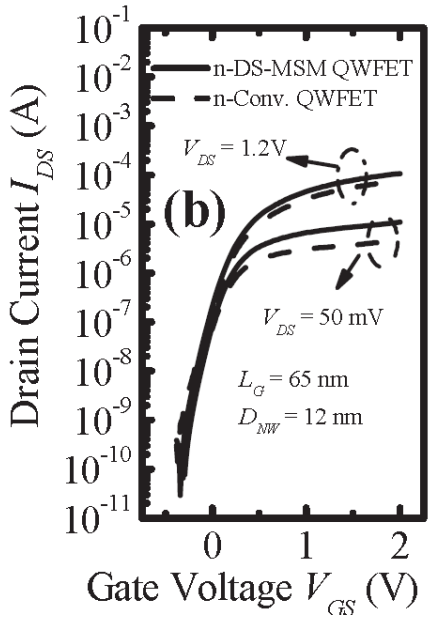
Nanowire FETs

Wong – NUS Singapore – VLSI 2009

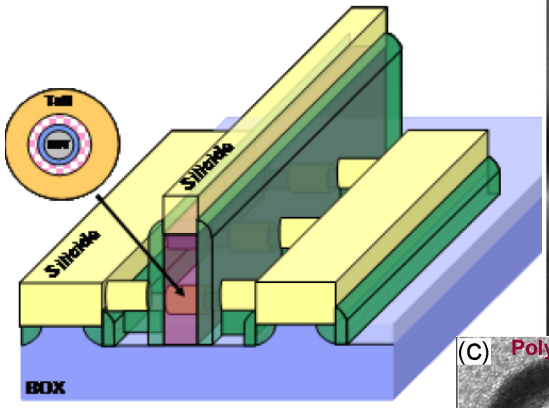


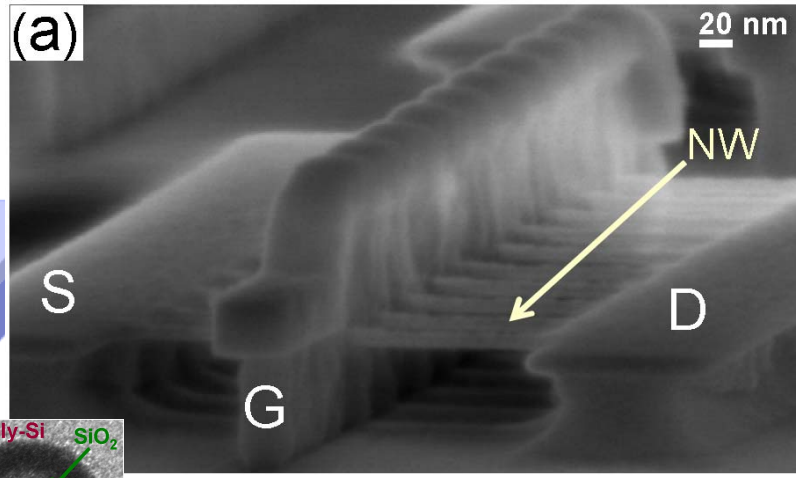


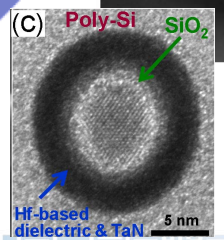


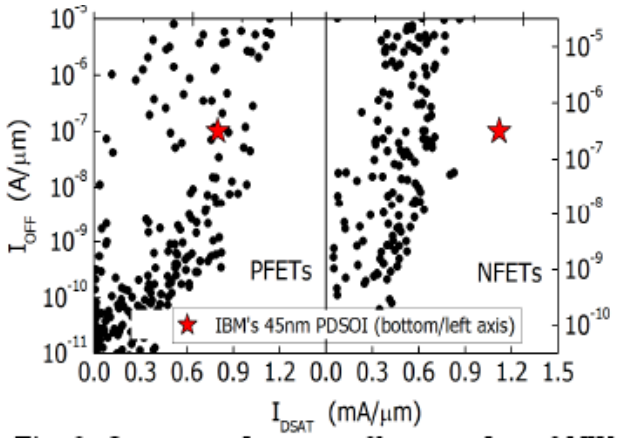


Bangsaruntip – IBM – IEDM 2009

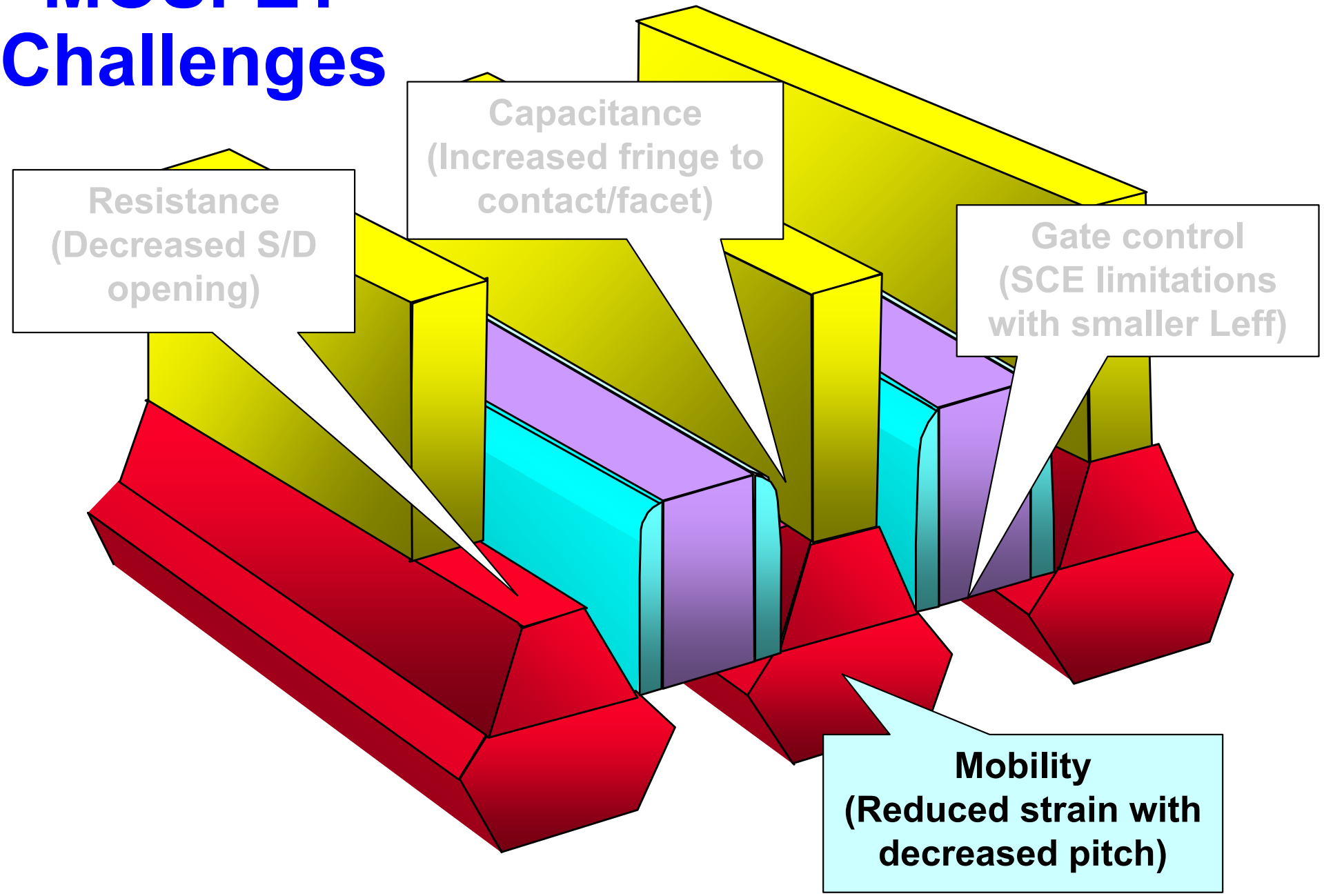




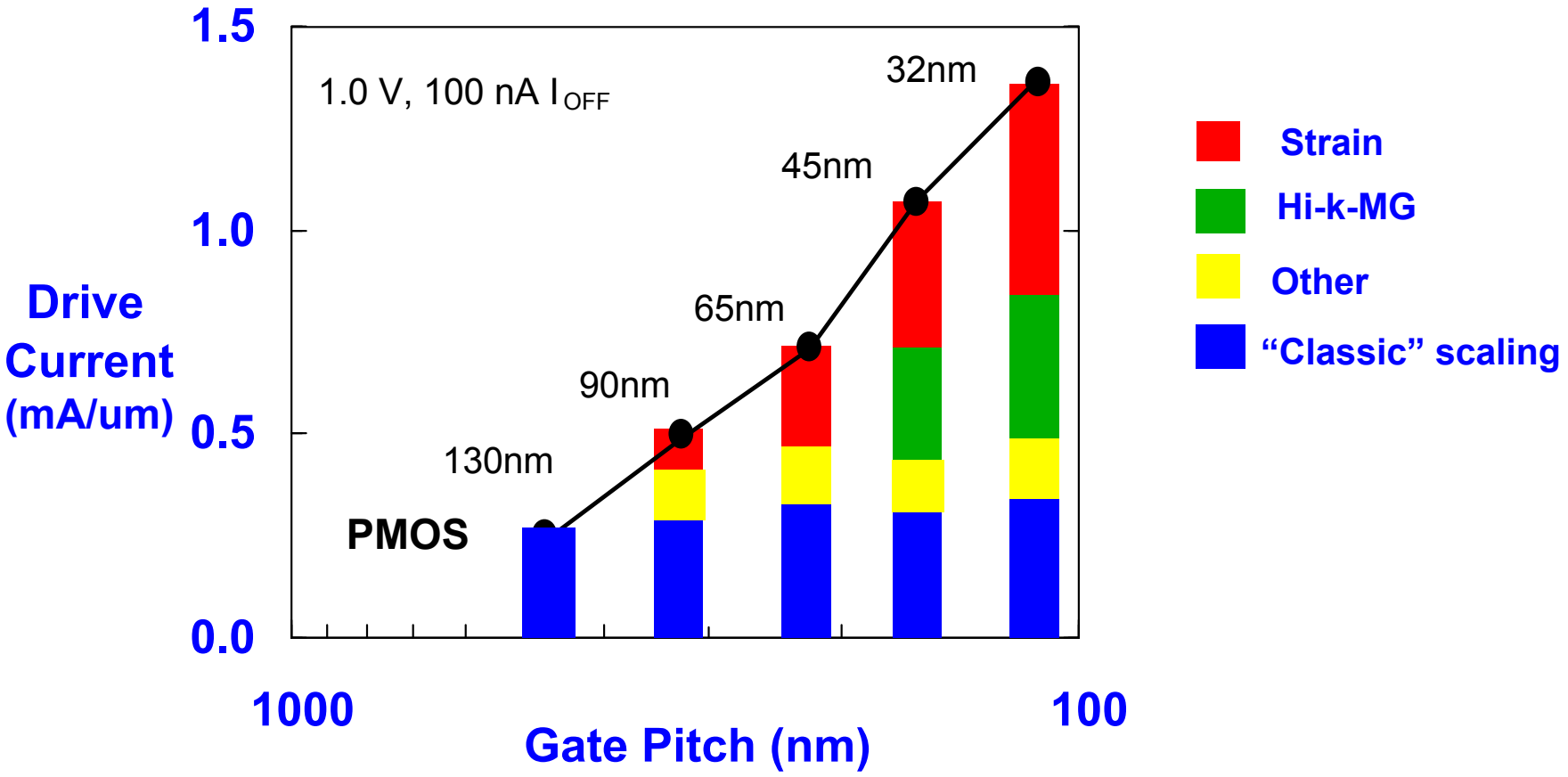




MOSFET Challenges



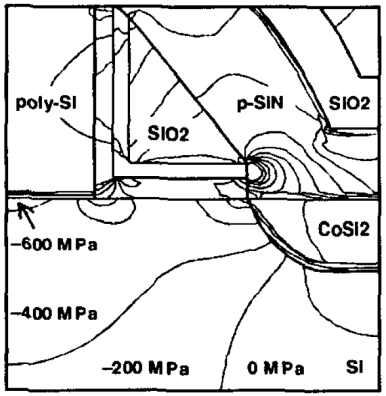
Transistor Performance Trend

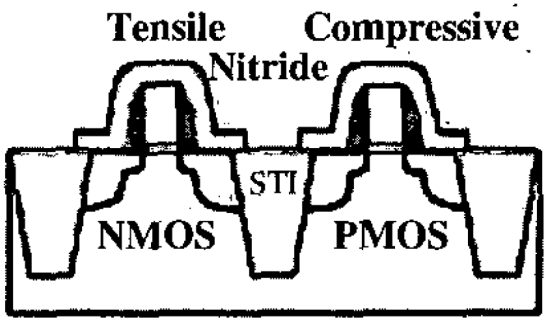


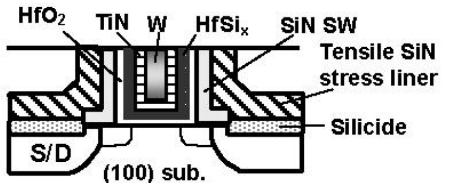
Strain is a critical ingredient in modern transistor scaling

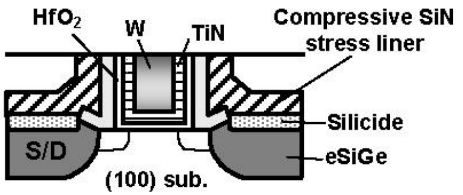
Strain was first introduced at 90nm, and its contribution has increased in each subsequent generation

Etch-stop nitride (CESL)

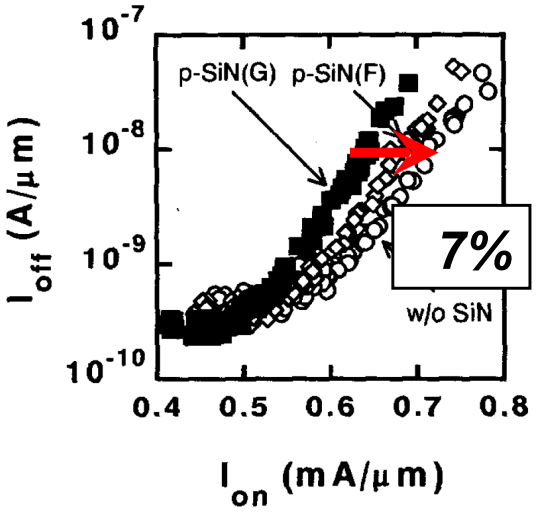


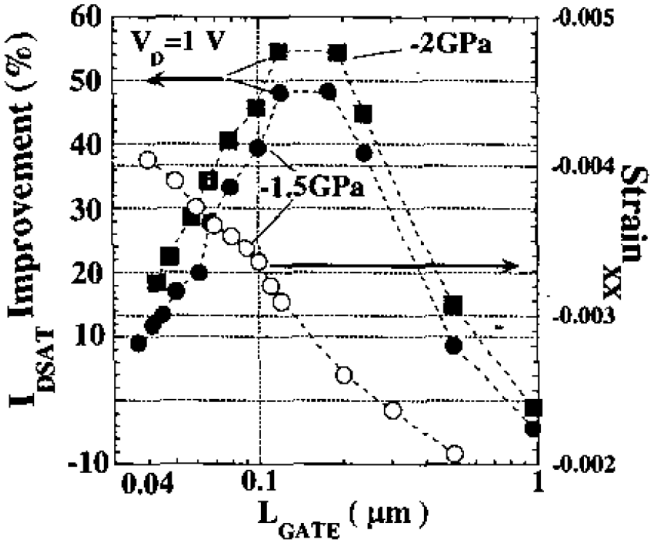


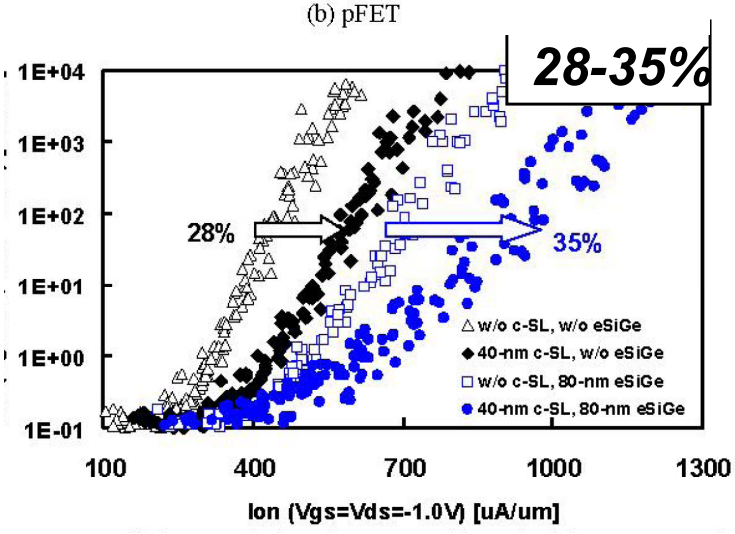




(b) pFET





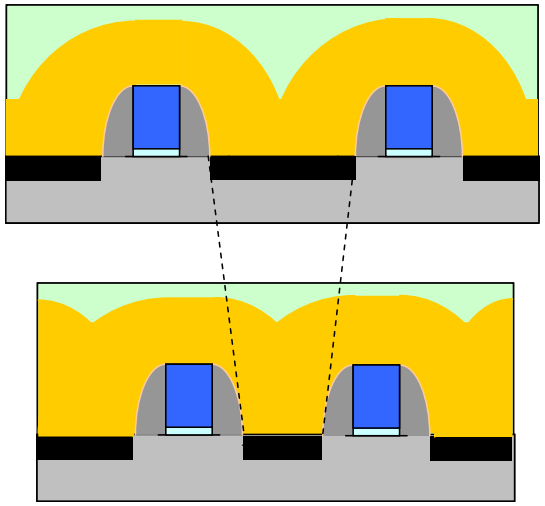


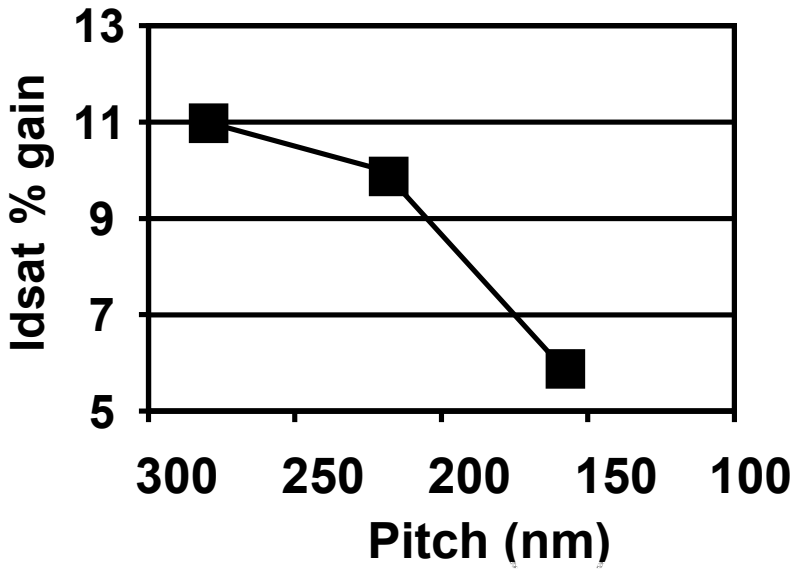
Ito – NEC
IEDM 2000
NMOS SiN strain

Pidin – Fujitsu
IEDM 2004
N and PMOS

Mayuzumi – Sony
IEDM 2007
Dual-cut stress liners
(MG process)

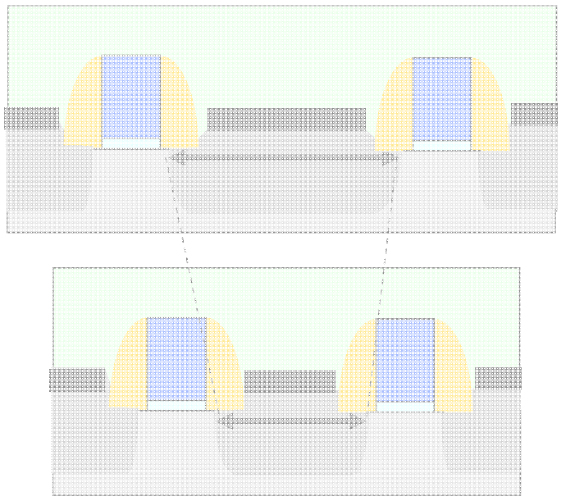
Strain: Pitch dependence

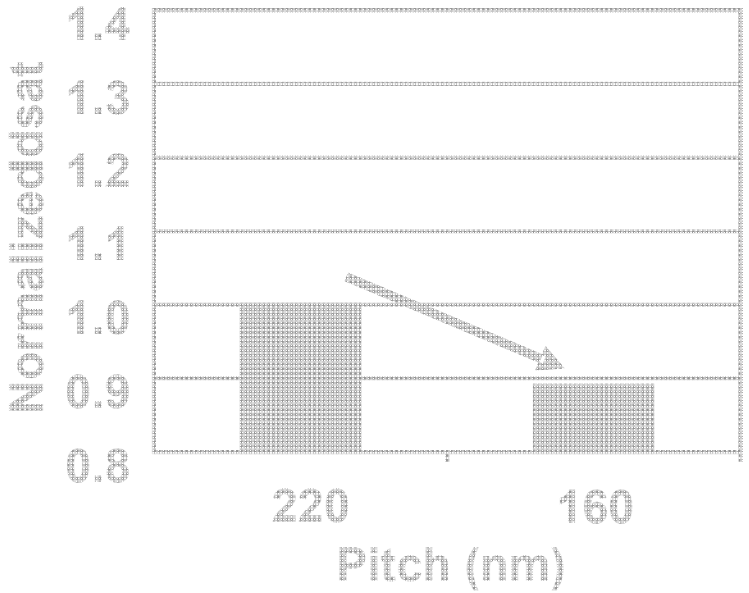




NMOS

Pitch degradation increases with film pinchoff, requires higher stress, thinner films



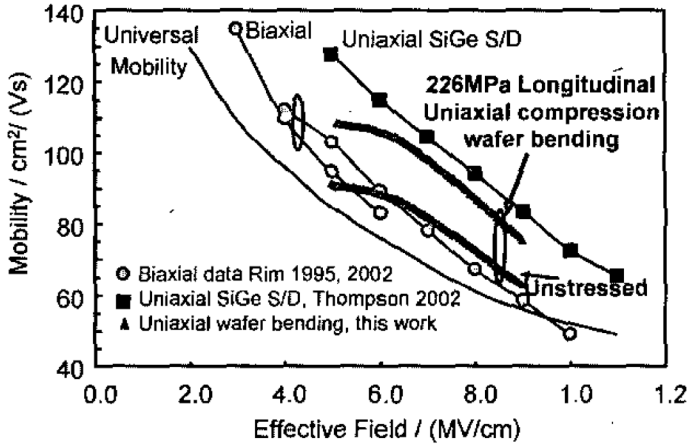


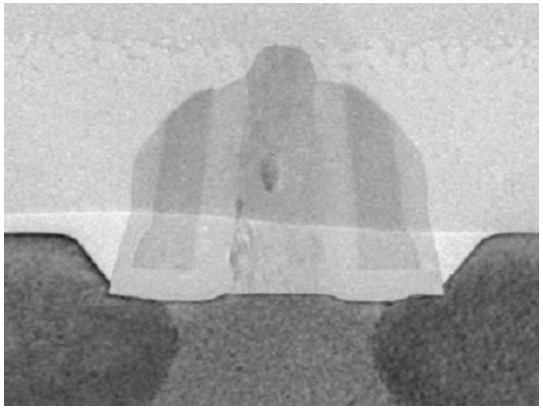
PMOS

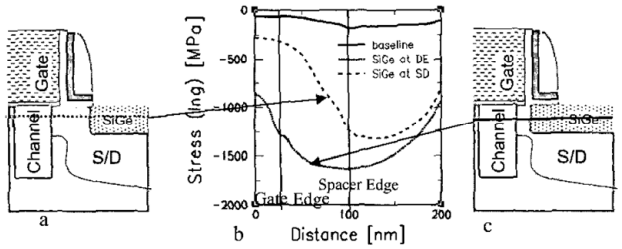
eSiGe S/D mobility strongly dependent on pitch

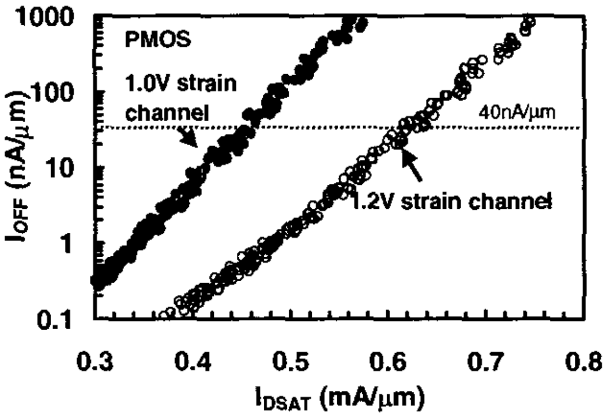
Auth, Intel, VLSI 2008

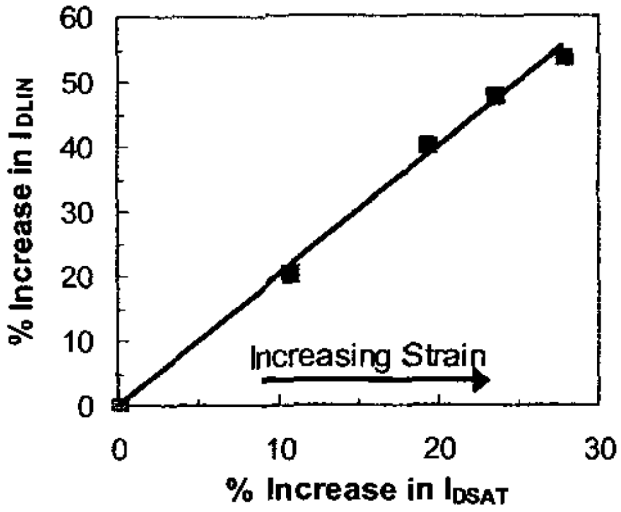
Embedded SiGe (PMOS)

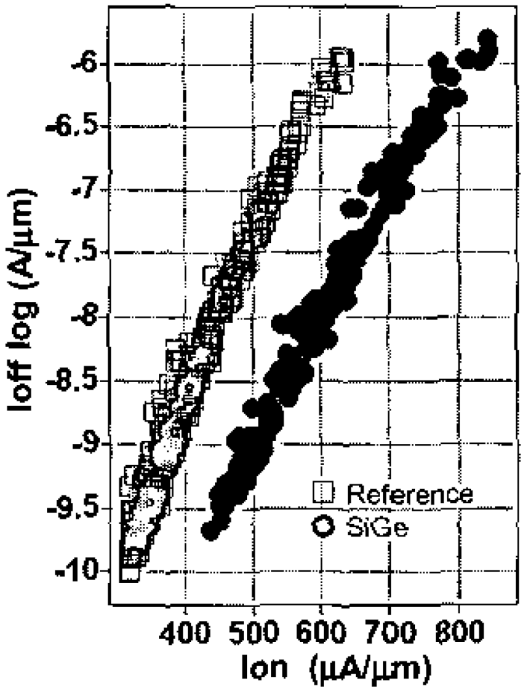










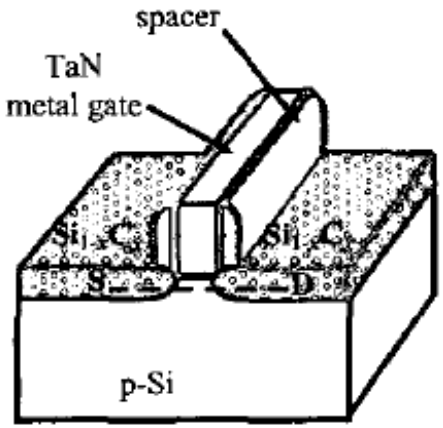


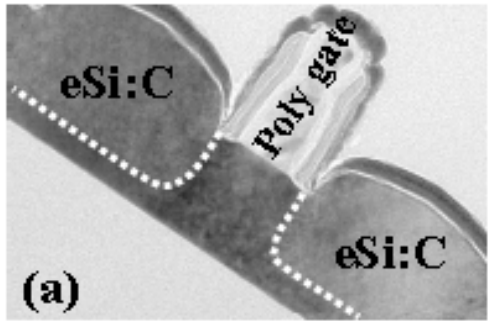
Thompson – Intel
IEDM 2002 / 2004

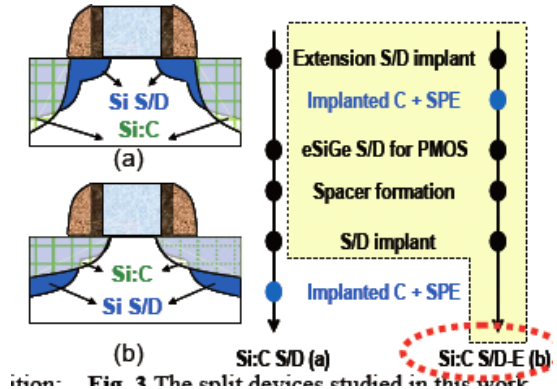
Ghani – Intel
IEDM 2003

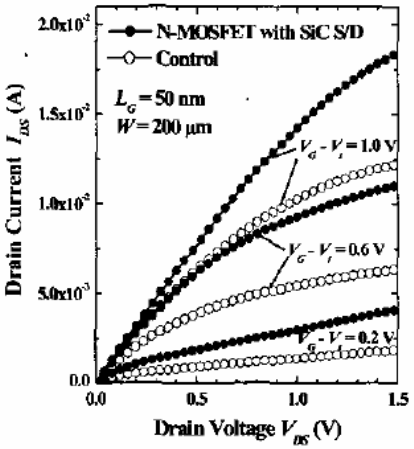
Chidambaram
TI / Applied Materials
VLSI - 2004

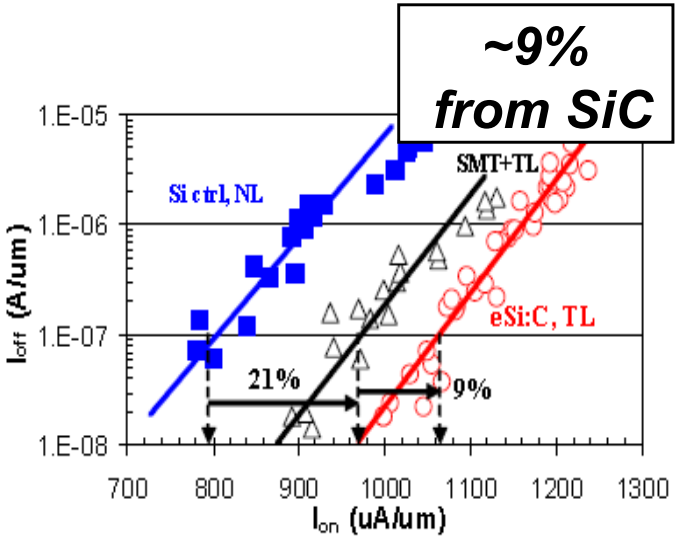
Embedded Si:C (NMOS)

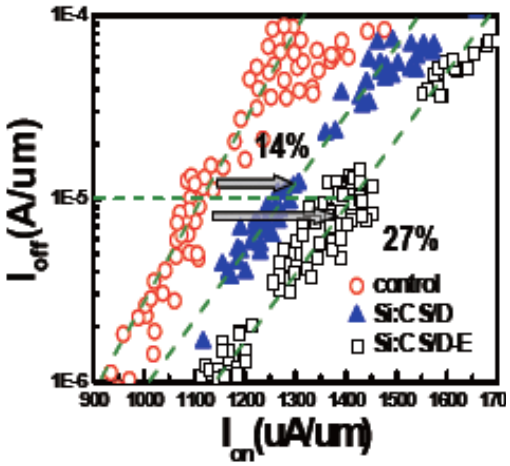










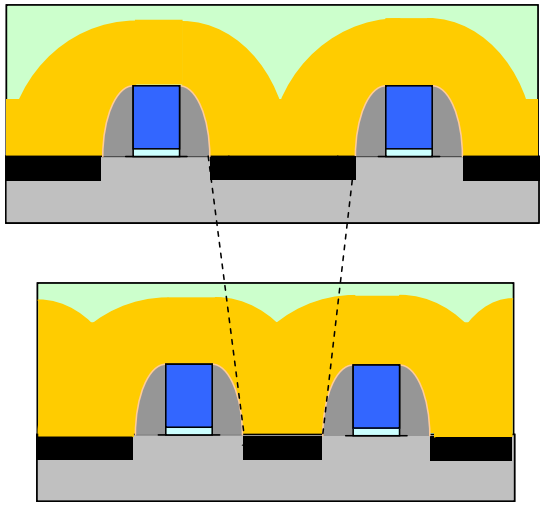


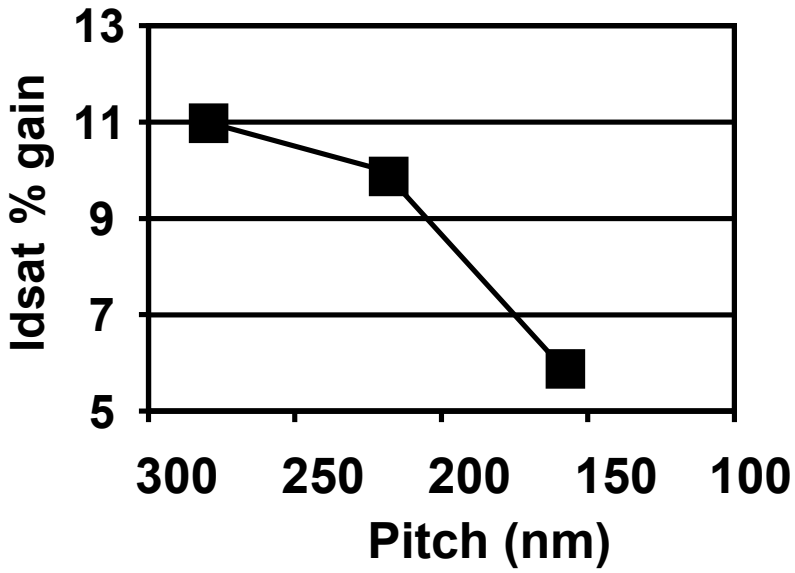
Ang – NUS-Singapore
IEDM 2004
Selective epi SiC (undoped)

Yang – IBM
IEDM 2008
In-situ epi P-SiC

Chung – Nat'l Chiao Tung U.
VLSI 2009
Implanted C + SPE

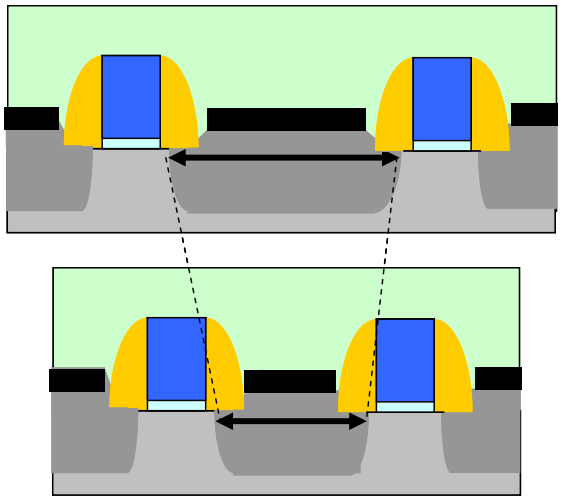
Strain: Pitch dependence

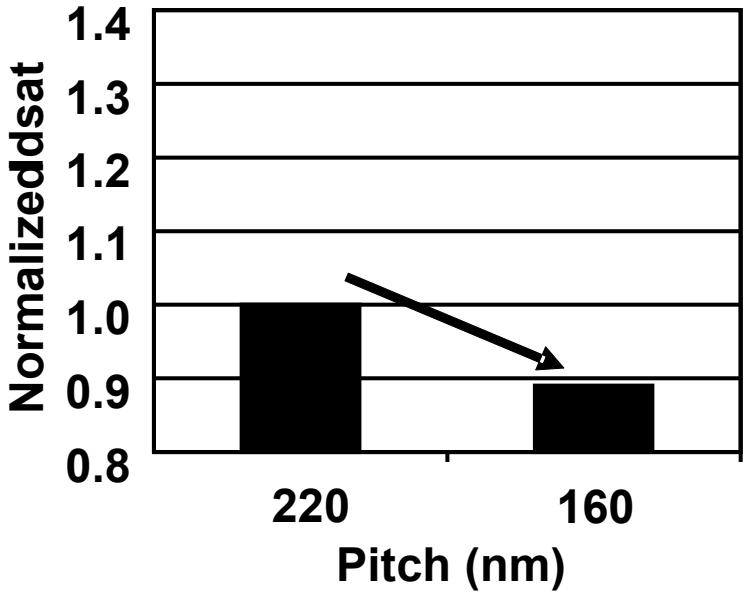




NMOS

Pitch degradation increases with film pinchoff, requires higher stress, thinner films





PMOS

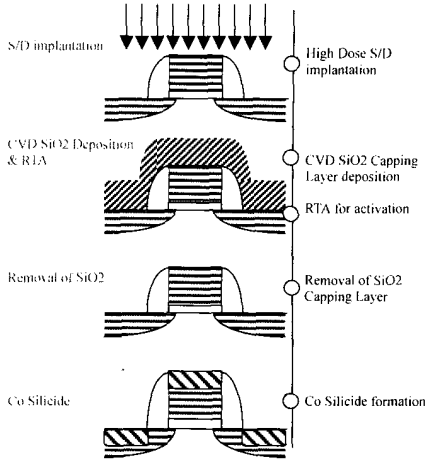
eSiGe S/D mobility strongly dependent on pitch

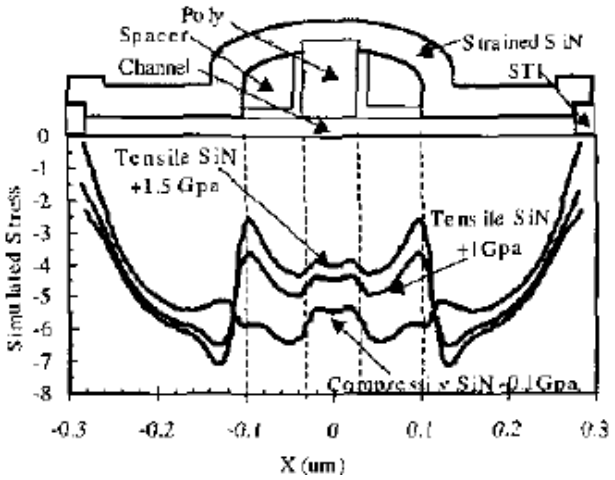
Auth, Intel, VLSI 2008

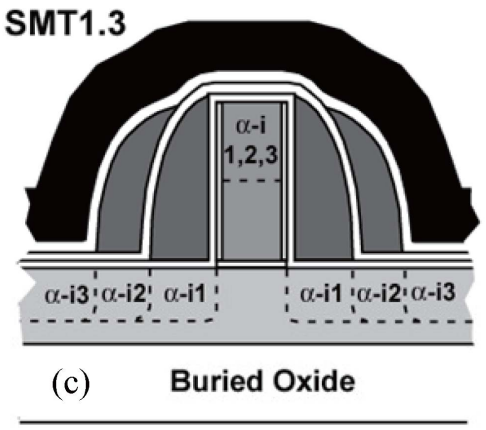
Strain: Pitch dependence

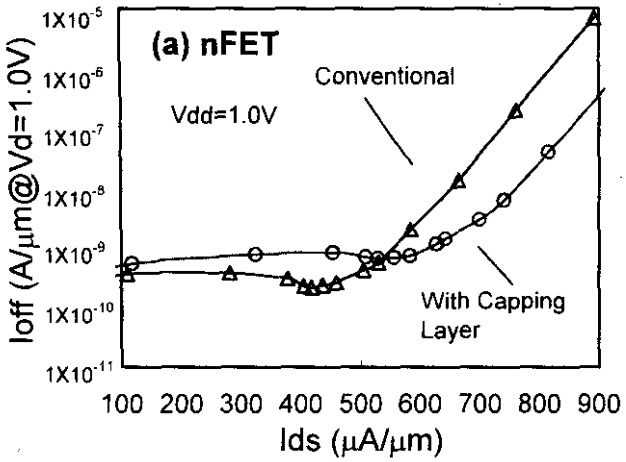
What about strain options less sensitive to pitch?

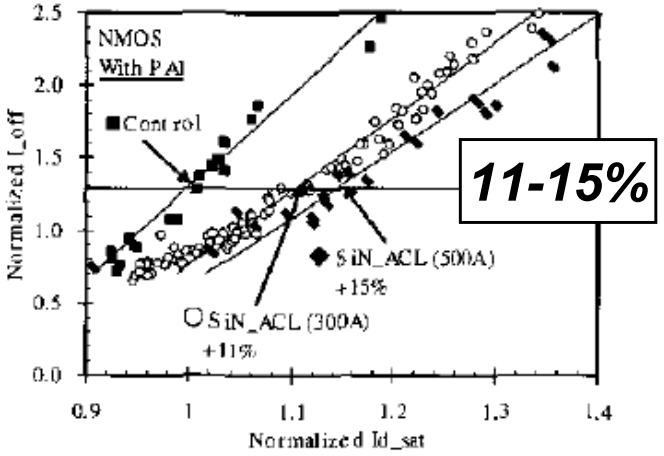
Stress Memorization (SMT)

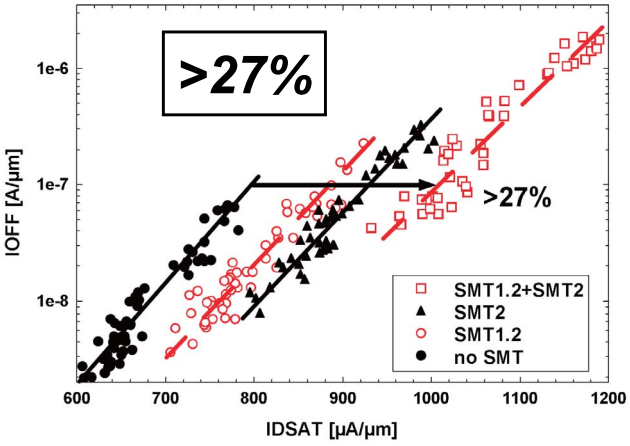










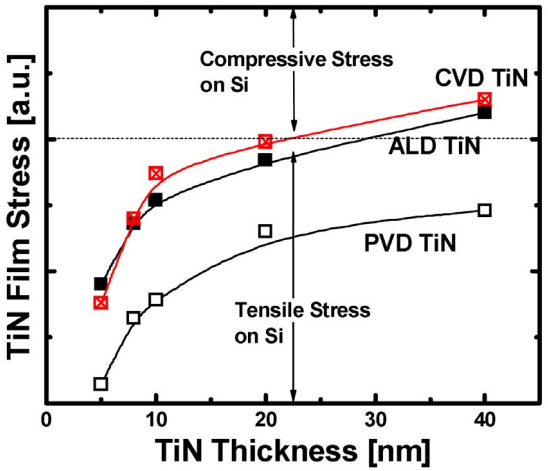


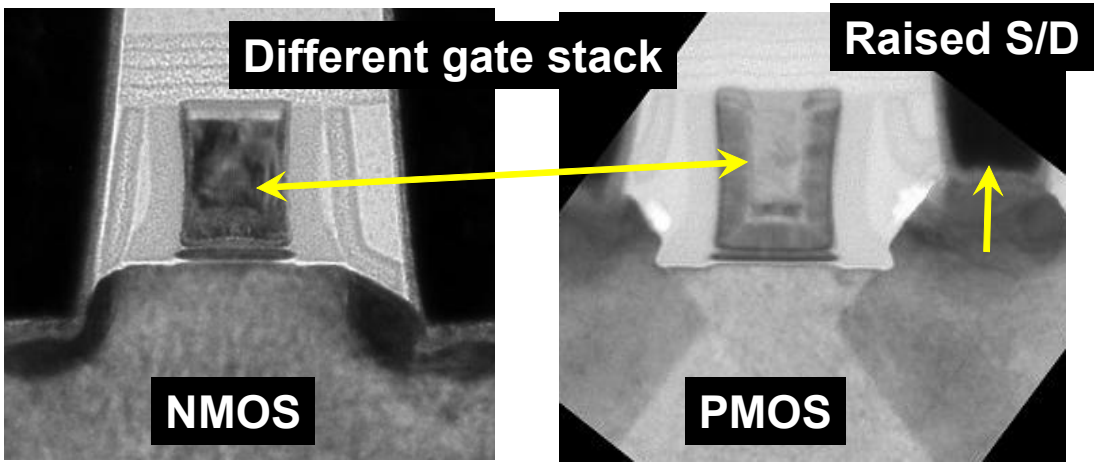
Ota – Mitsubishi
IEDM 2002
NMOS SMT

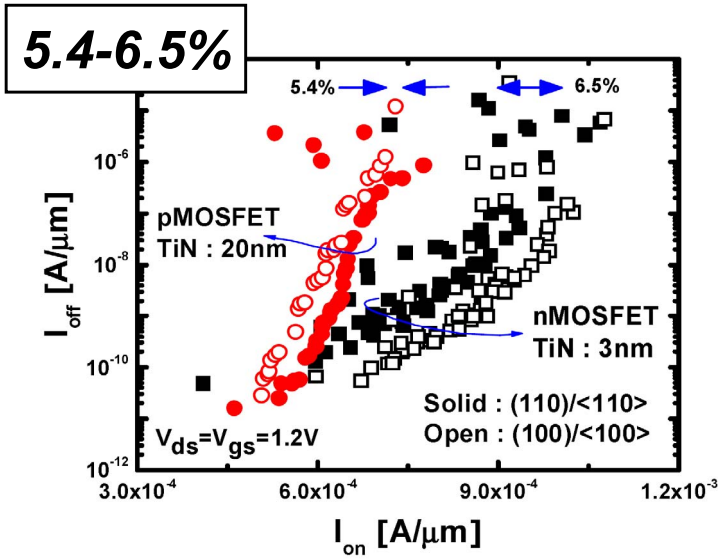
Chen – TSMC
VLSI 2004
NMOS SMT

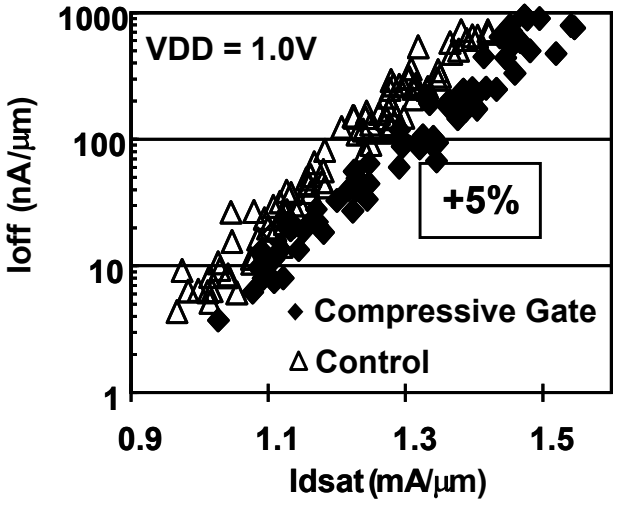
Wei – AMD
VLSI 2007
Multiple liners

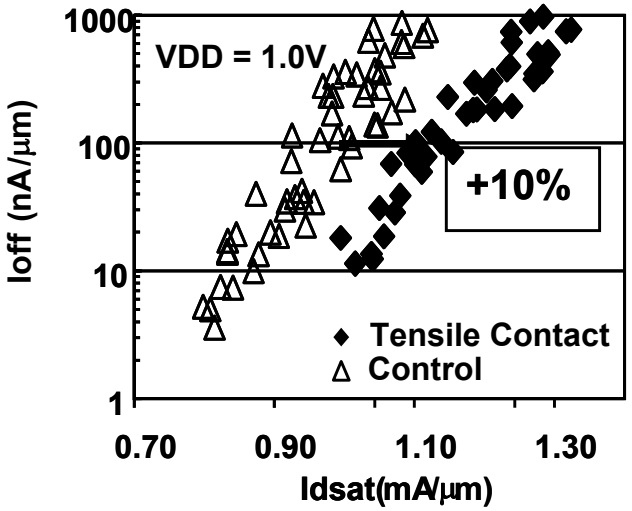
Metal stress (gate and contact)







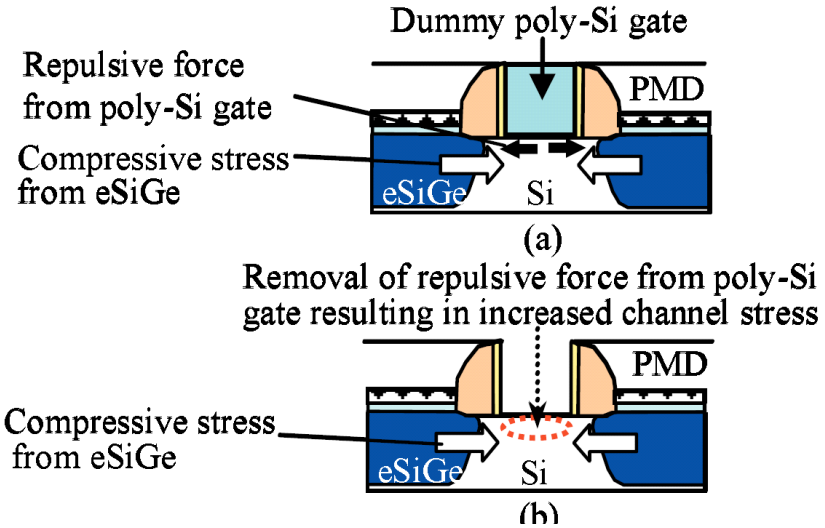




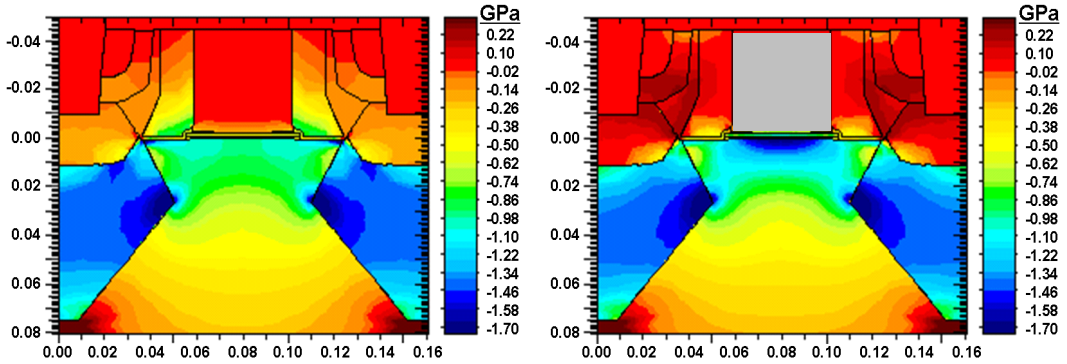
Kang – Sematech
IEDM 2006

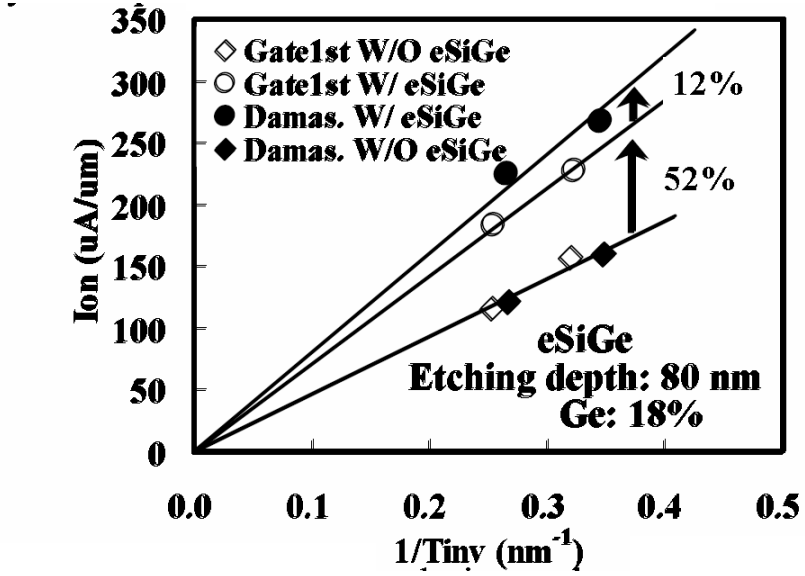
Auth – Intel
VLSI 2008

Enhanced PMOS strain: Gate last HiK-MG

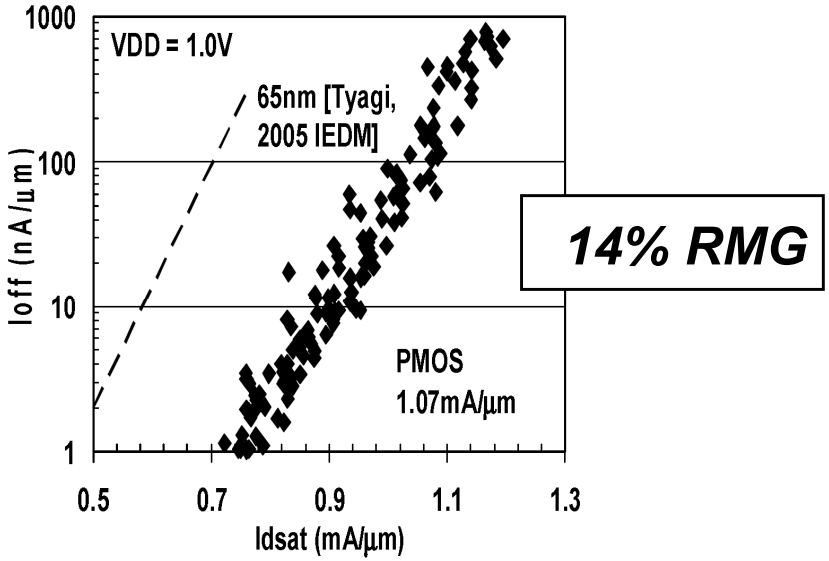


Before gate removal **After gate removal**





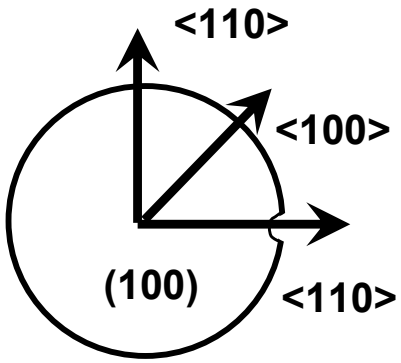
Wang – Sony
VLSI 2007



Auth – Intel
VLSI 2008

ORIENTATION

(100) surface – top down

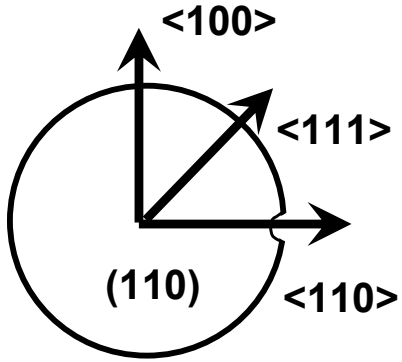


Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a “45 degree” wafer)

Both <110> directions are the same.

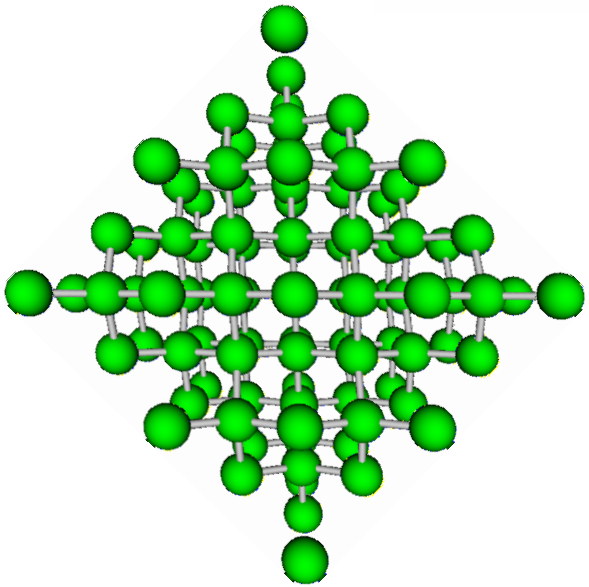
(110) surface – top down

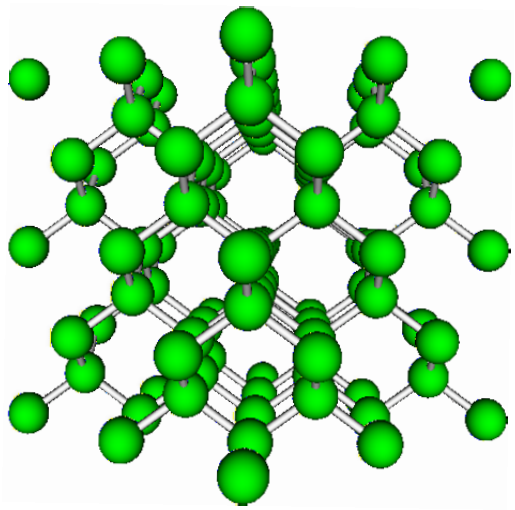


Non-standard

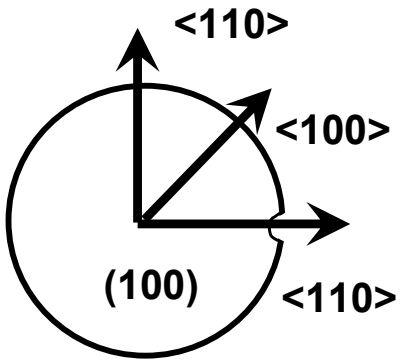
(110) Surface

Three possible channel directions
<110> <111> and <100>





(100) surface – top down



Standard wafer / direction
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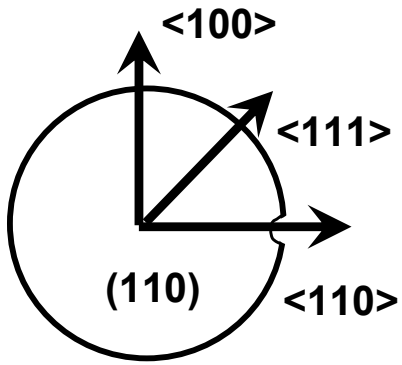
(110) surface – top down

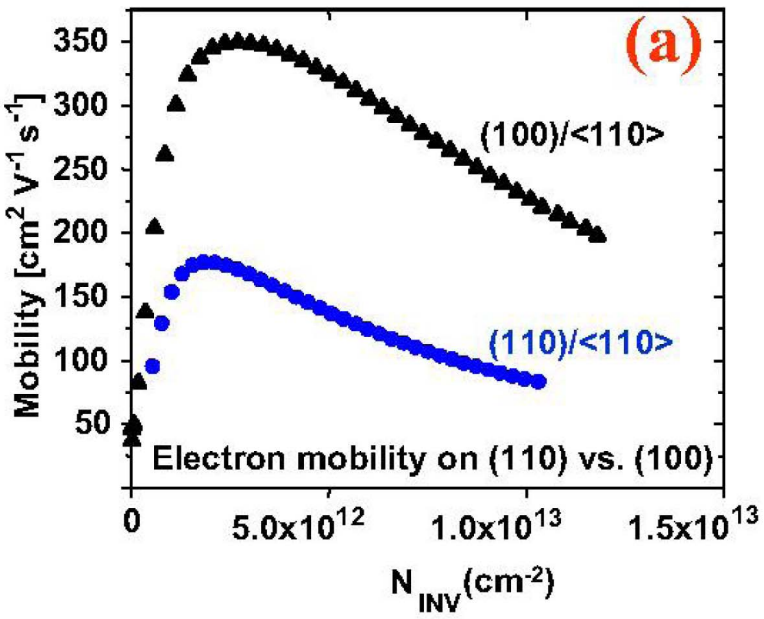


Non-standard

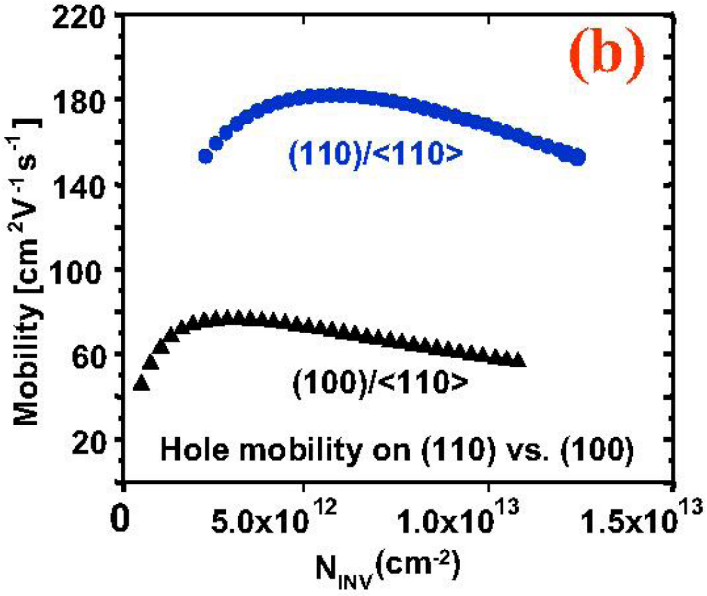
(110) Surface

Three possible channel directions
<110> <111> and <100>

(100) BEST NMOS

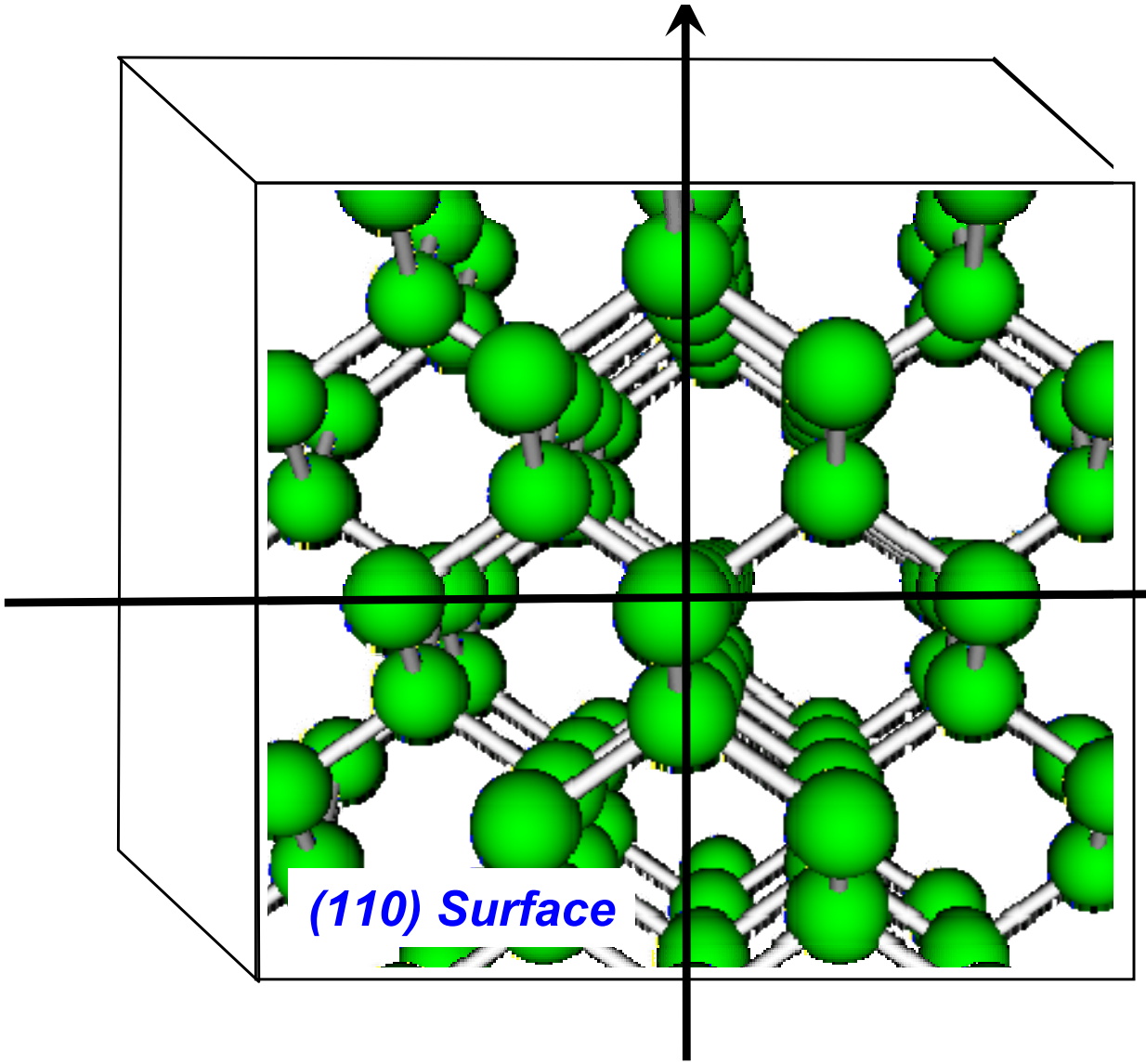


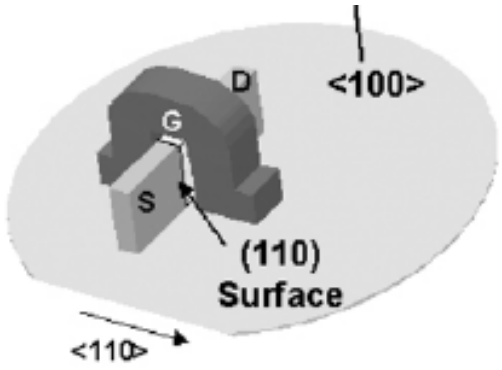
(110) <110> BEST PMOS



Yang
AMD/IBM
EDST 2007

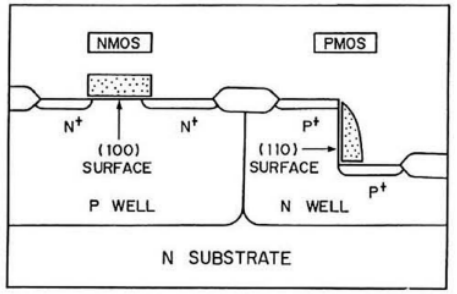
PMOS Vertical Devices on (100)





Chang - IBM – TED 2004

<110> channel

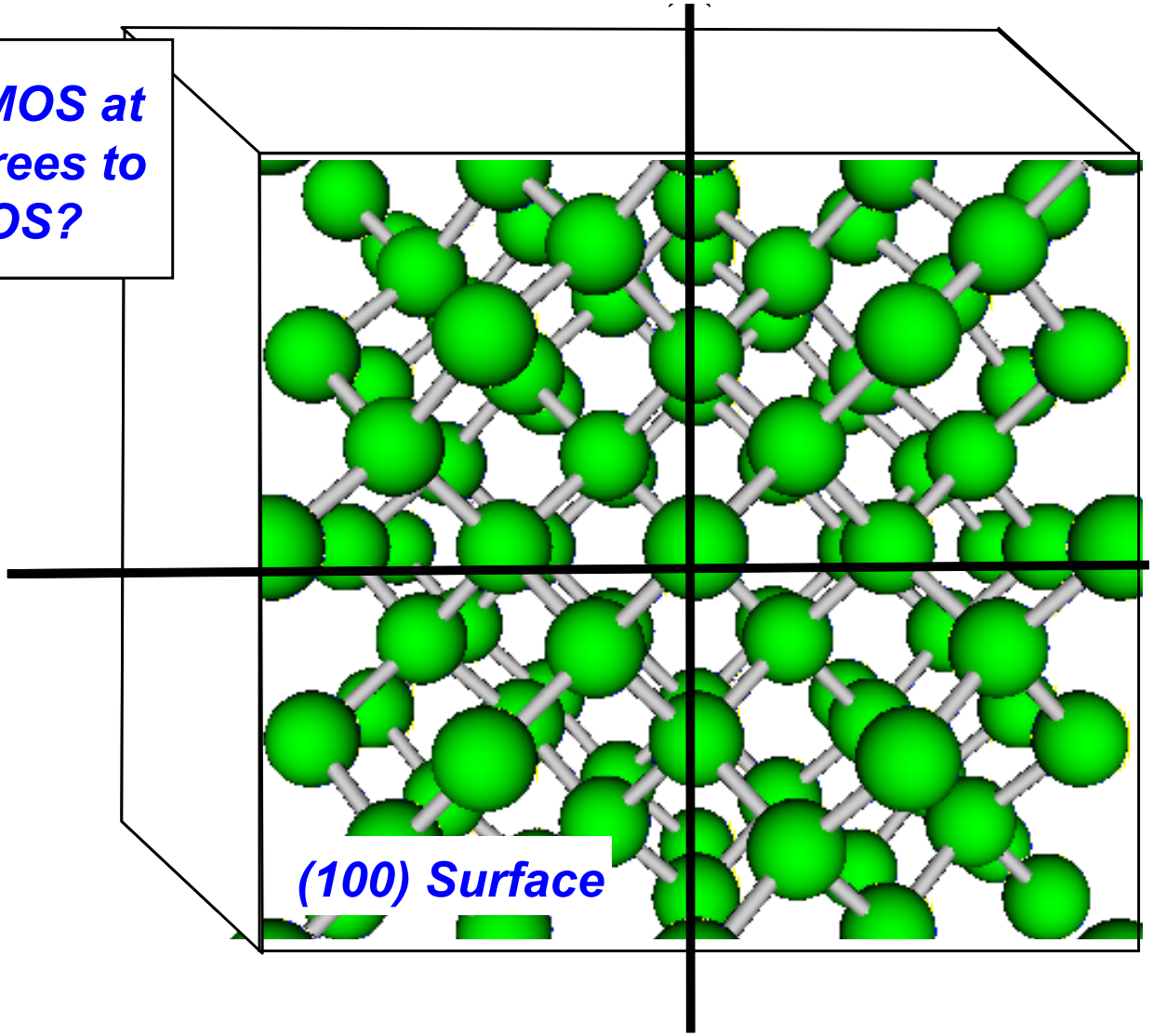


Kinugawa-Toshiba VLSI 1986

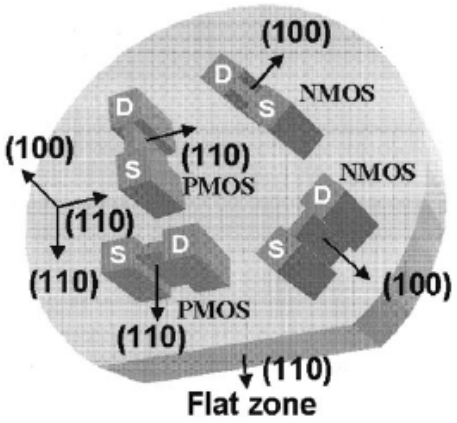
(110) surface <110> channel results when a VFET is fabricated on typical (100) Si - good for PMOS, not for NMOS

NMOS Vertical Devices on (100)

Put NMOS at 45degrees to PMOS?



<100> channel

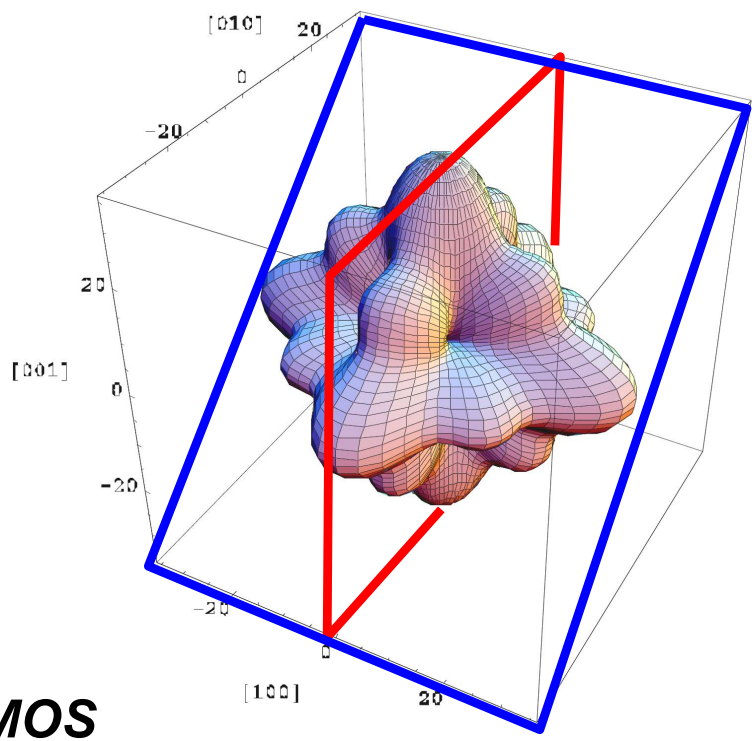


Chang - Berkeley
Proc. IEEE 2003

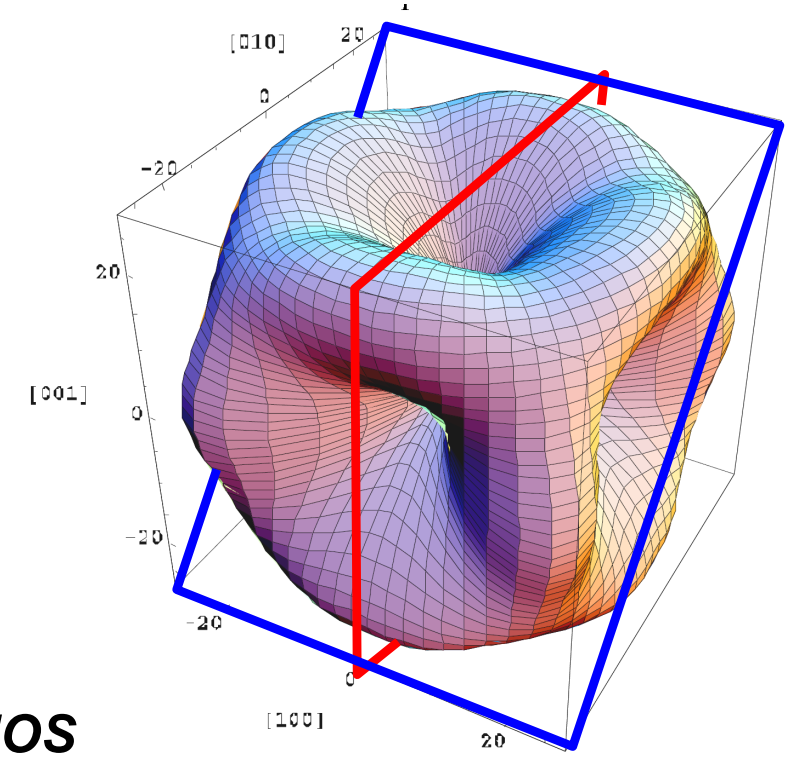
(100) surface <100> channel for a VFET fabricated at 45 degrees typical (100) Si – very challenging for lithography

Strain and Orientation
Piezoresistive coefficient as a function of direction

Udo – Infineon – Proc. IEEE Sensors 2004



NMOS

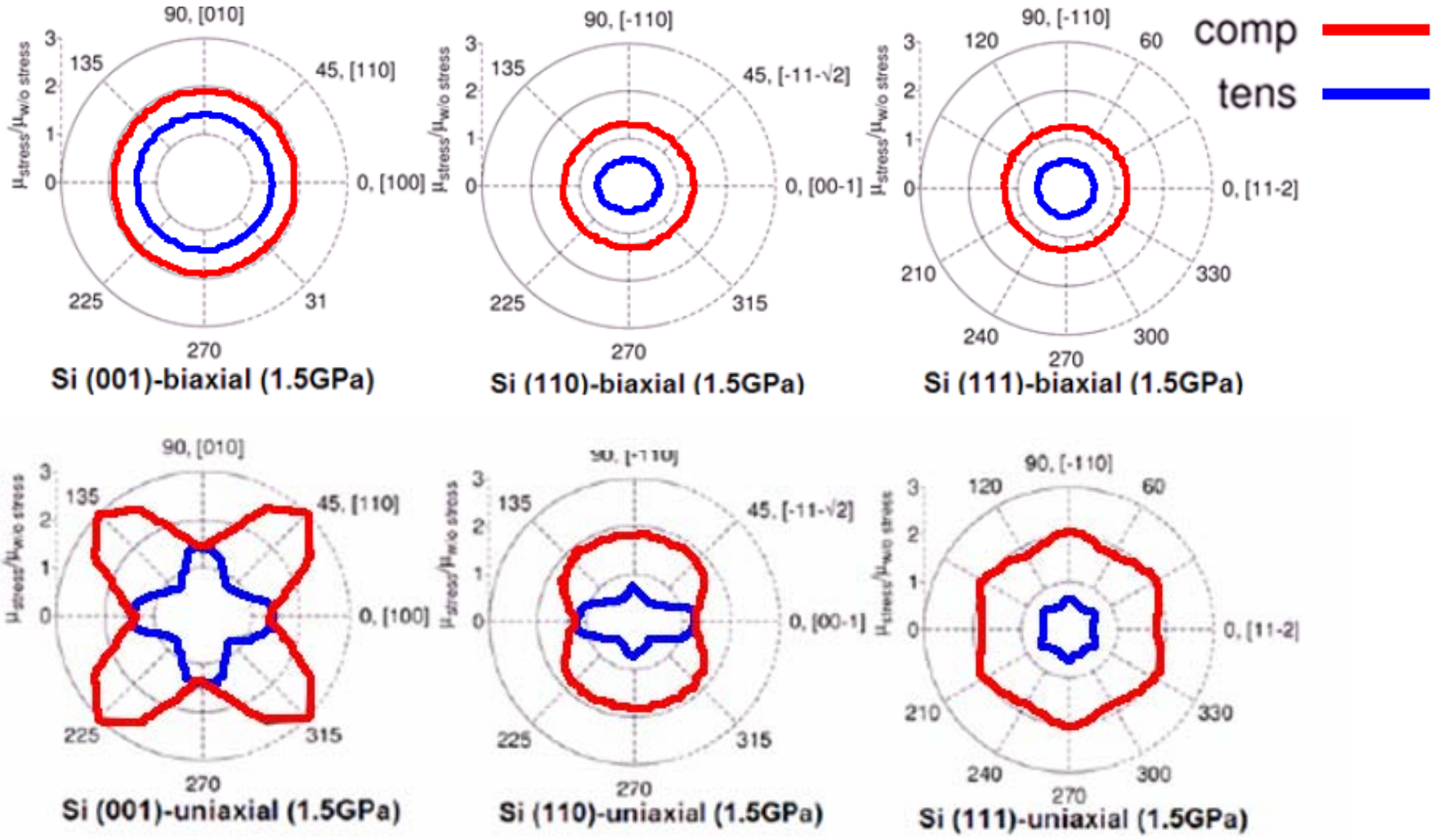


PMOS

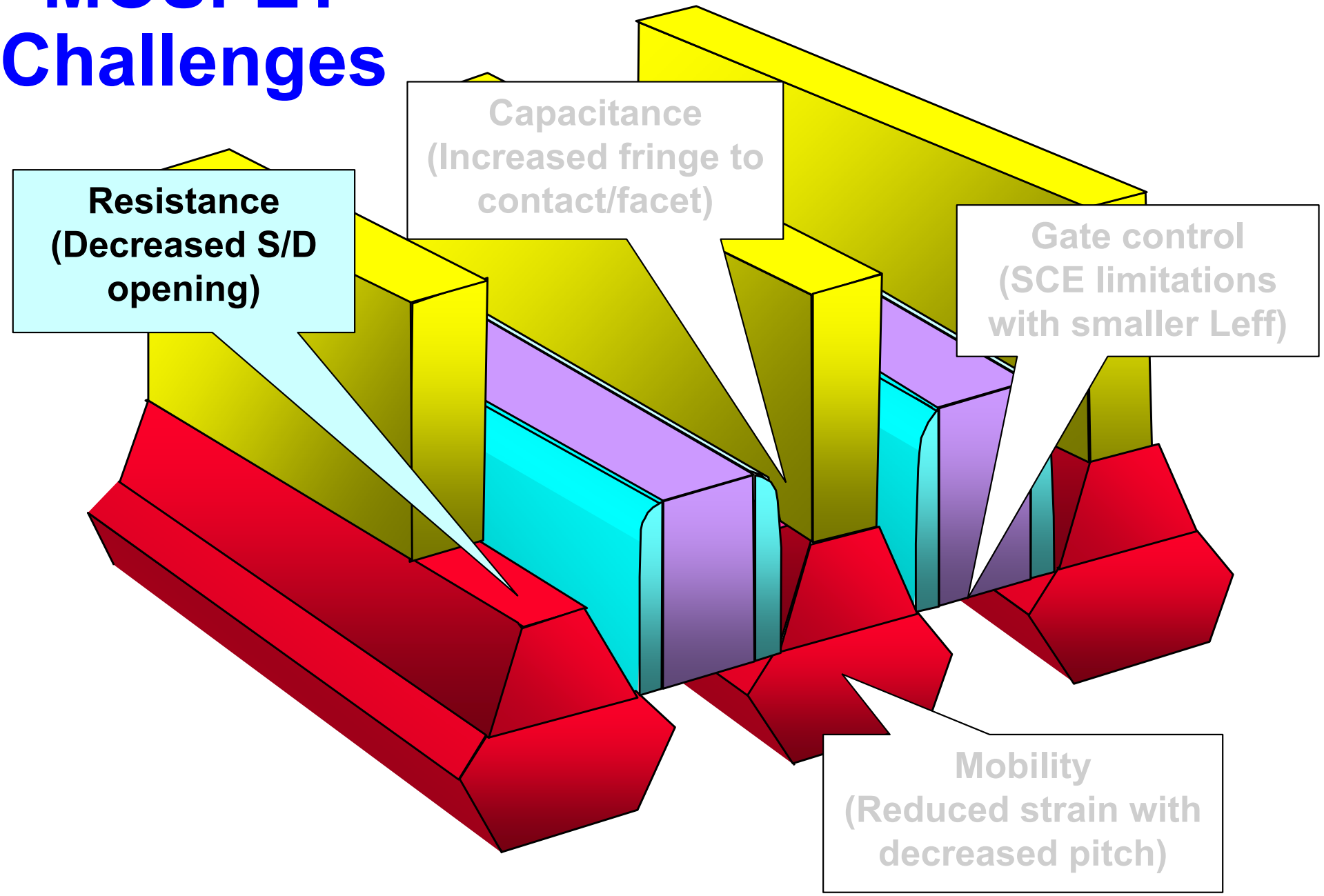
Krishnamohan – Stanford – IEDM 2008

Comparison of (001), (110) and (111) Uniaxial- and Biaxial- Strained-Ge and Strained-Si PMOS DGFETs for All Channel orientations: Mobility Enhancement, Drive Current, Delay and Off-State Leakage

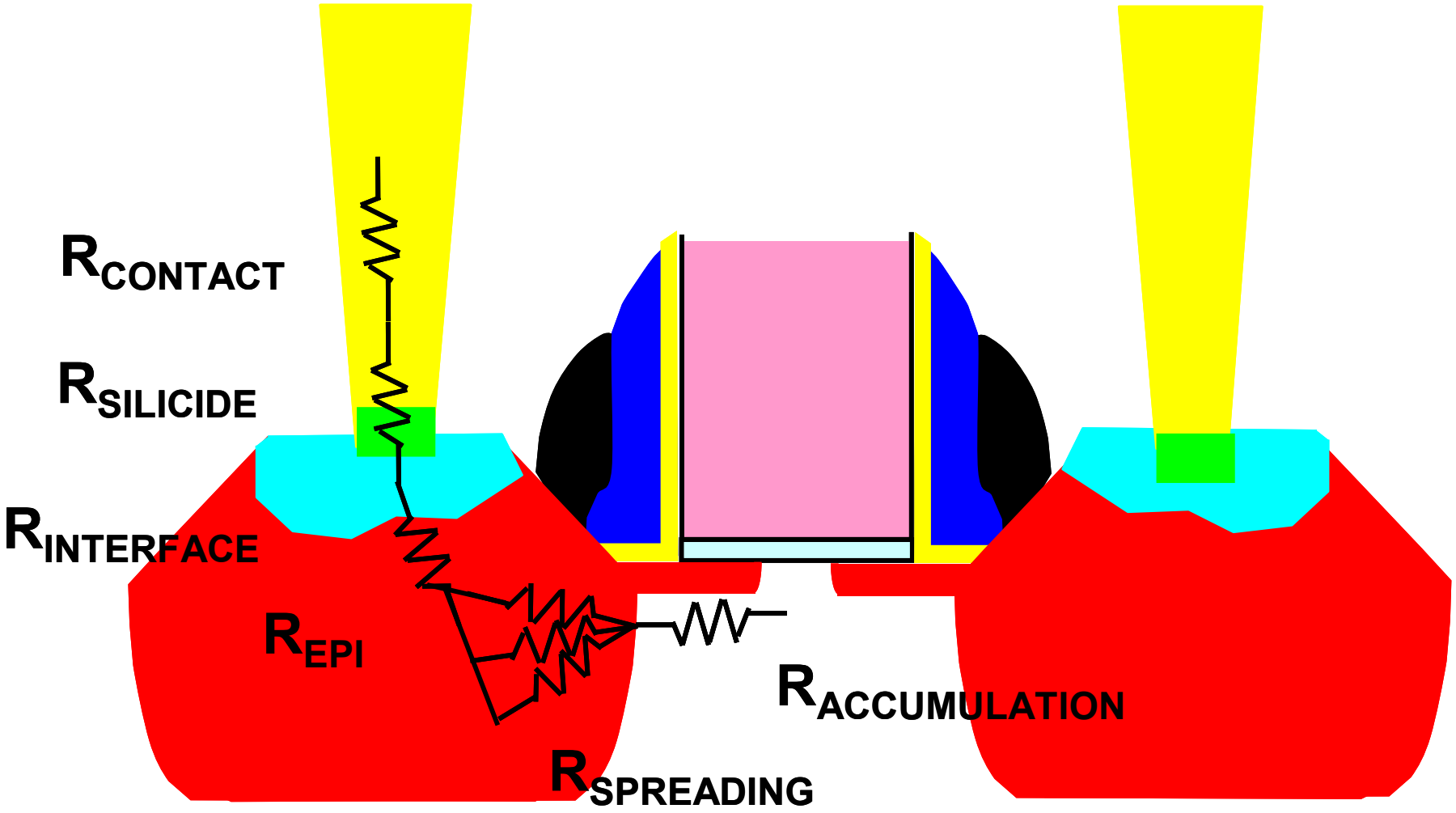
[1,4]Tejas Krishnamohan, [1]Donghyun Kim, [2]Thanh Viet Dinh, [3]Anh-tuan Pham,
[3]Bernd Meinerzhagen, [2]Christoph Jungemann, [1]Krishna Saraswat



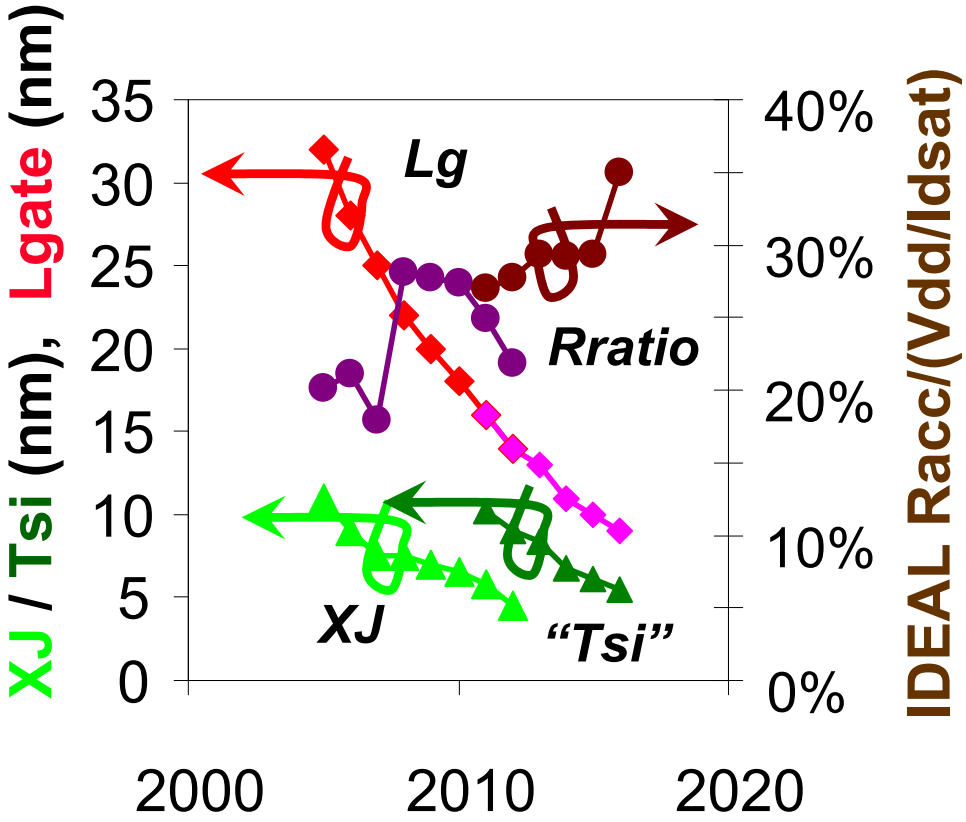
MOSFET Challenges



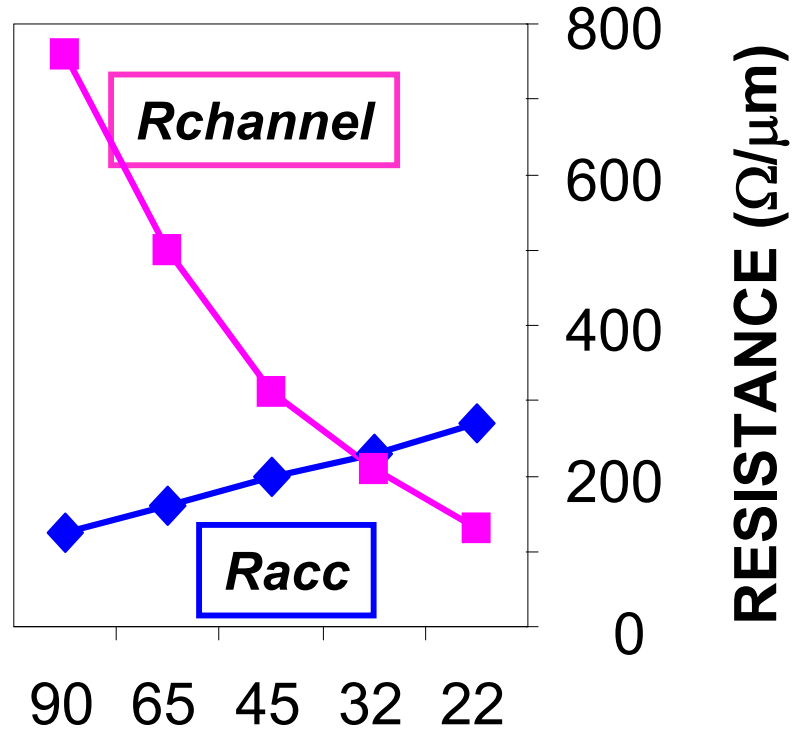
Planar Resistive Elements



Technology trends
Xj/Tsi, Lg, Racc



ITRS 2007 [19]



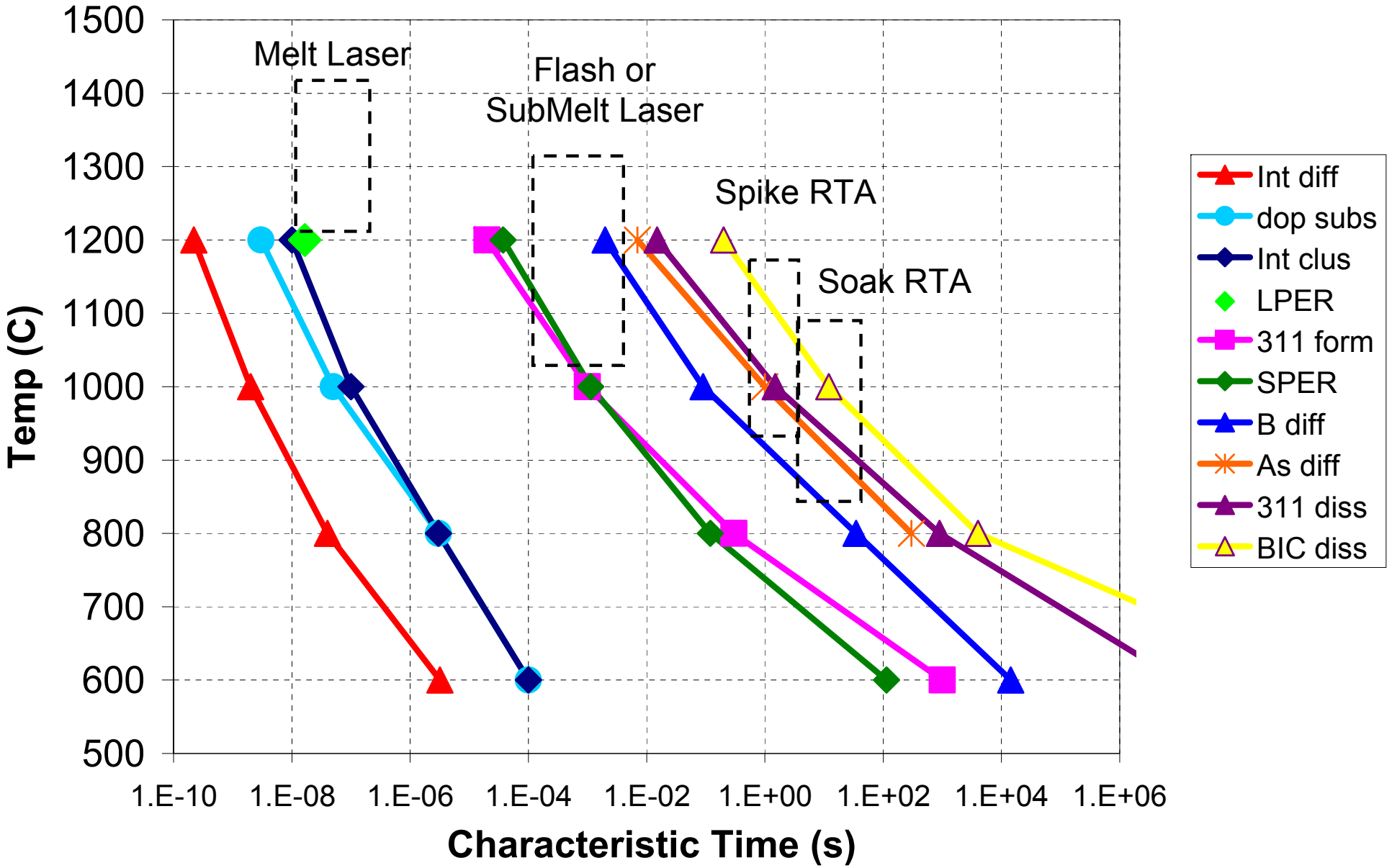
Noori - Applied Materials
TED 2008 [20]

RTA effective annealing times

Cycle	Rampup Rate (C/s)	Typical peak time (s)	Rampdown Rate (C/s)	Effective Time (s)
Soak	75	5-30	40	~5+t_{hold}
Spike	250	<0.5	75	~1
Flash	1e5-1e6	<1e-6	~1e6	0.1-1 ms
Scanning laser	1e5-1e6	<1e-6	>1e6	0.1-1 ms
Melt (laser)	1e7-1e8	<1e-8	>1e7	10-100ns

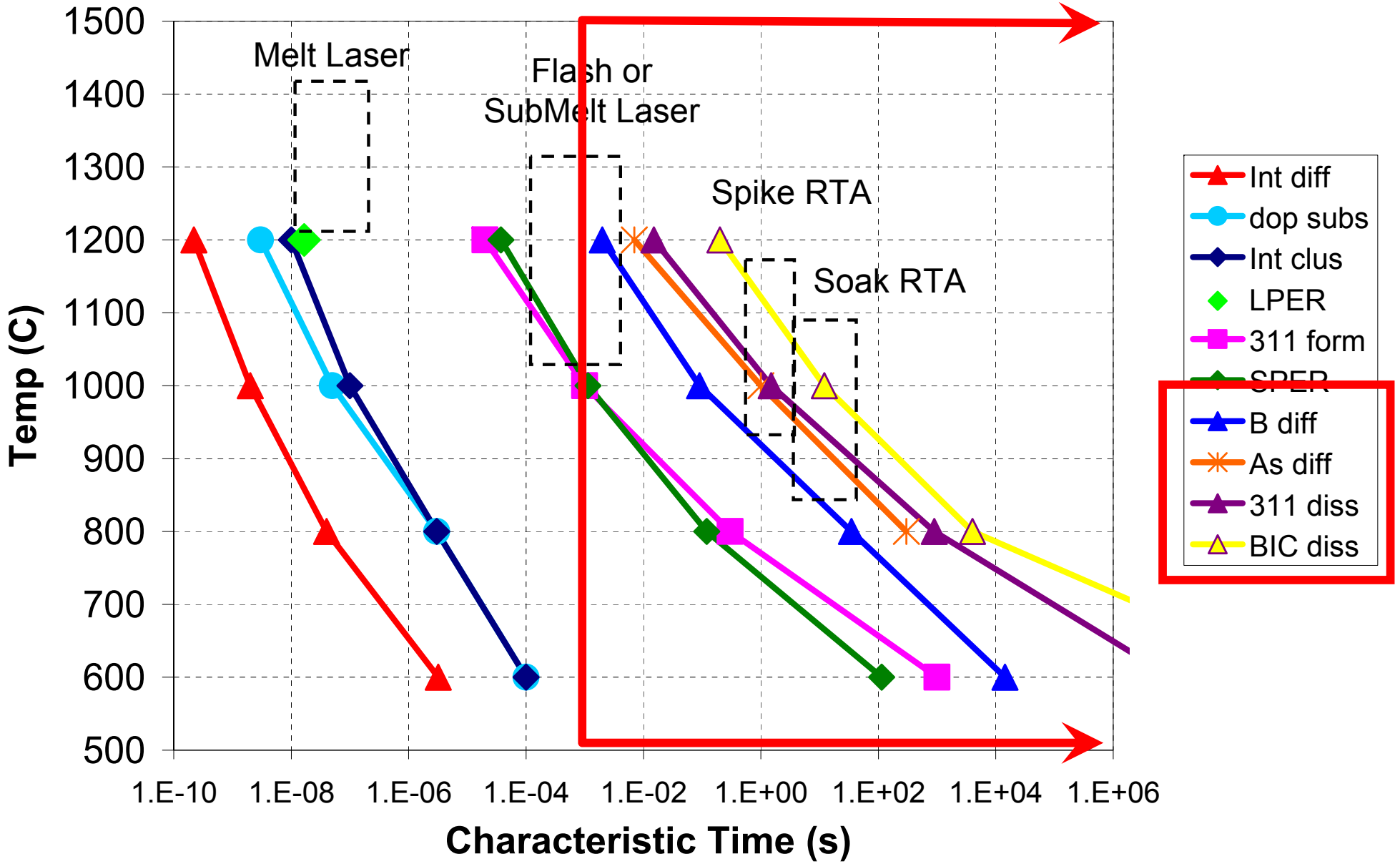
Effective annealing times are computed with realistic ramp shapes, assuming dominant Ea~5eV.

Annealing techniques: by physics of activation

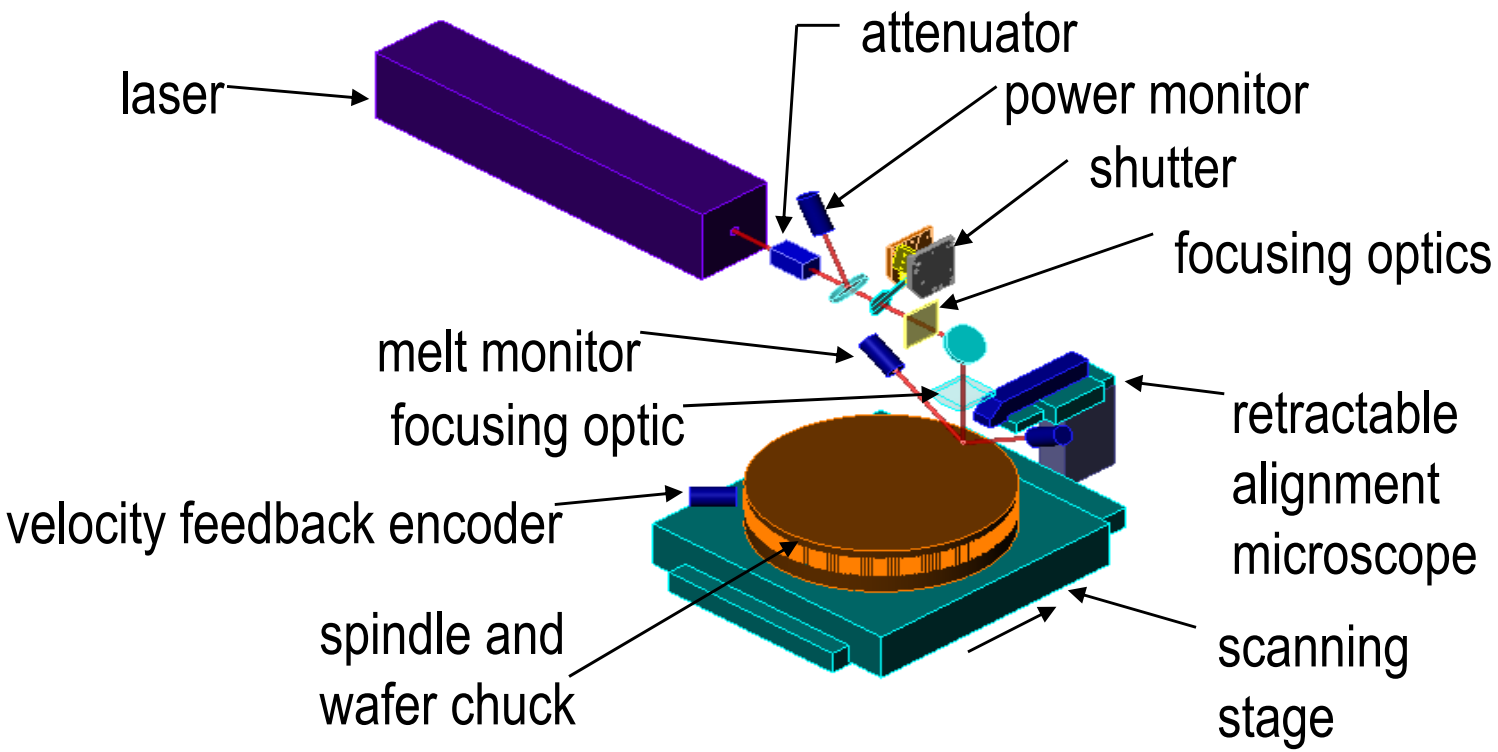


Annealing techniques: by phys

Flash/submelt laser processes have the potential to “freeze” dopant profiles in place



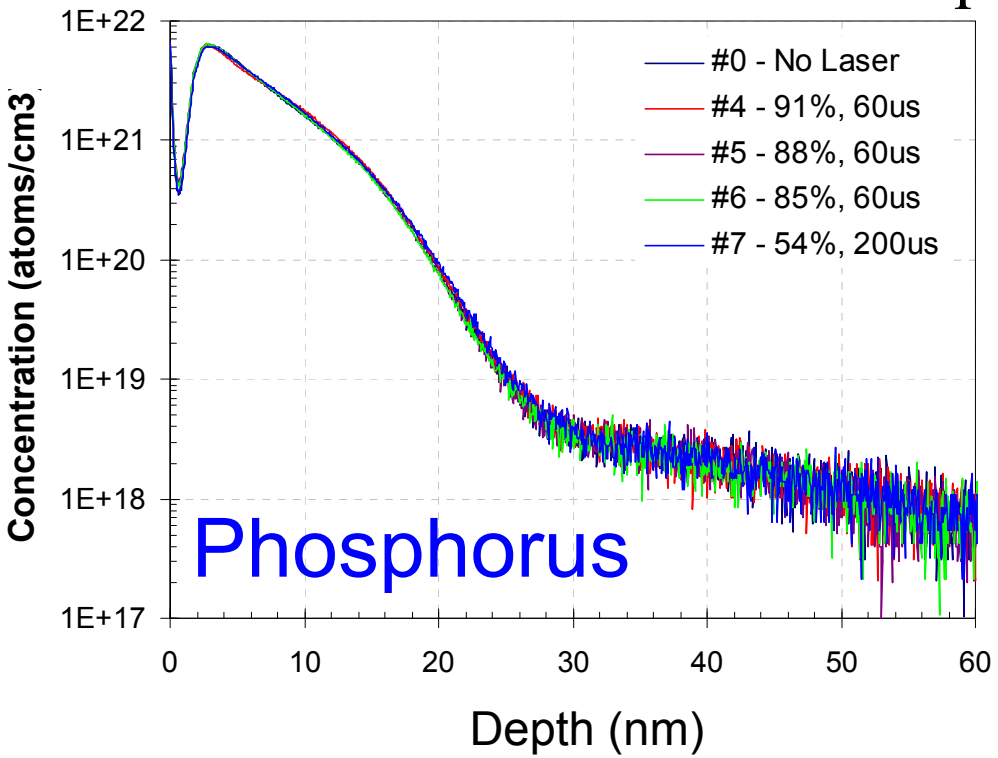
Submelt Laser Anneal Test Stand



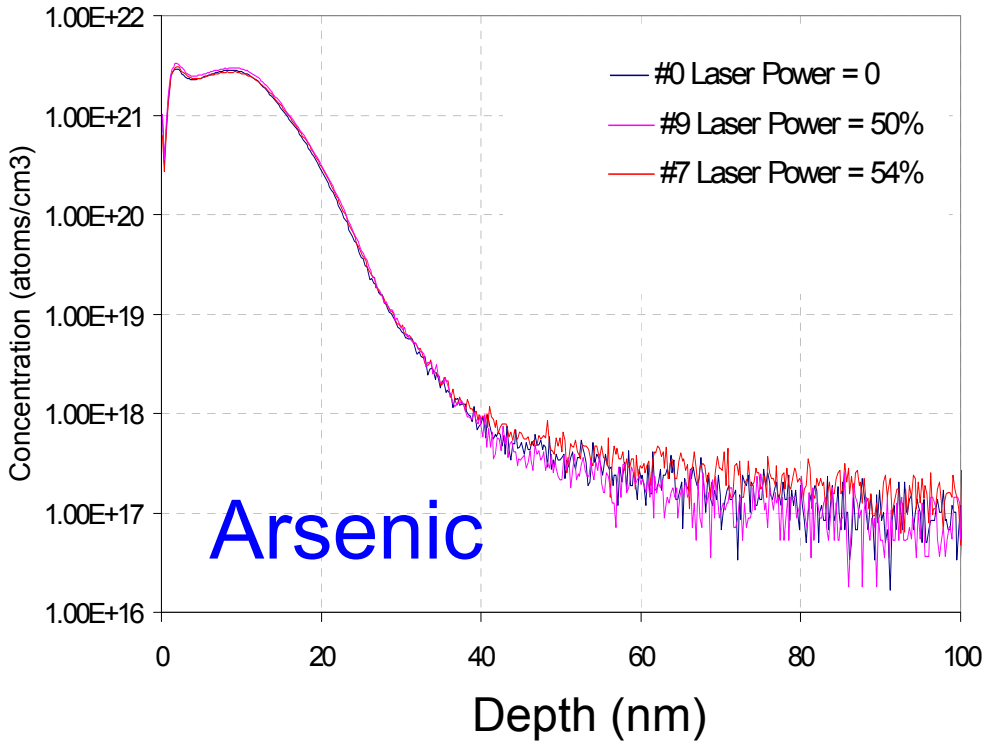
- Guassian beam: 400 μm wide (FWHM)
- Spinning stage: dwell time 60 – 200 μs
- Constant dwell time and track spacing are maintained by synchronizing spin speed and x-stage position

Submelt Laser Anneal Test Results

Junction depth = 26 nm
Sheet resistance = 150 Ω/sq



Junction depth = 28 nm,
Sheet resistance = 150 Ω/sq

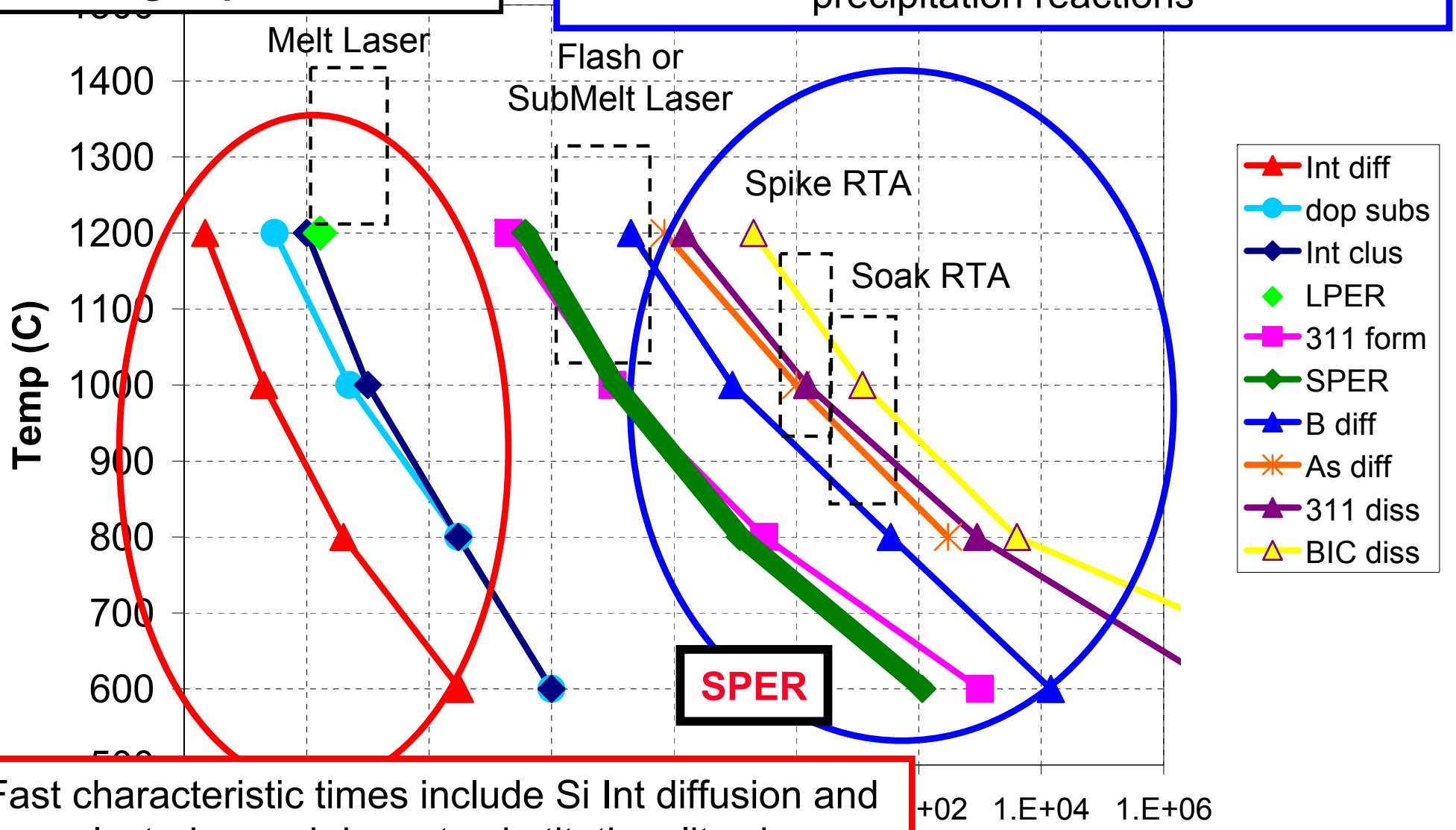


Freezing implants in place:
Submelt laser anneal showing no diffusion after 200 µS anneal

aling techniques:

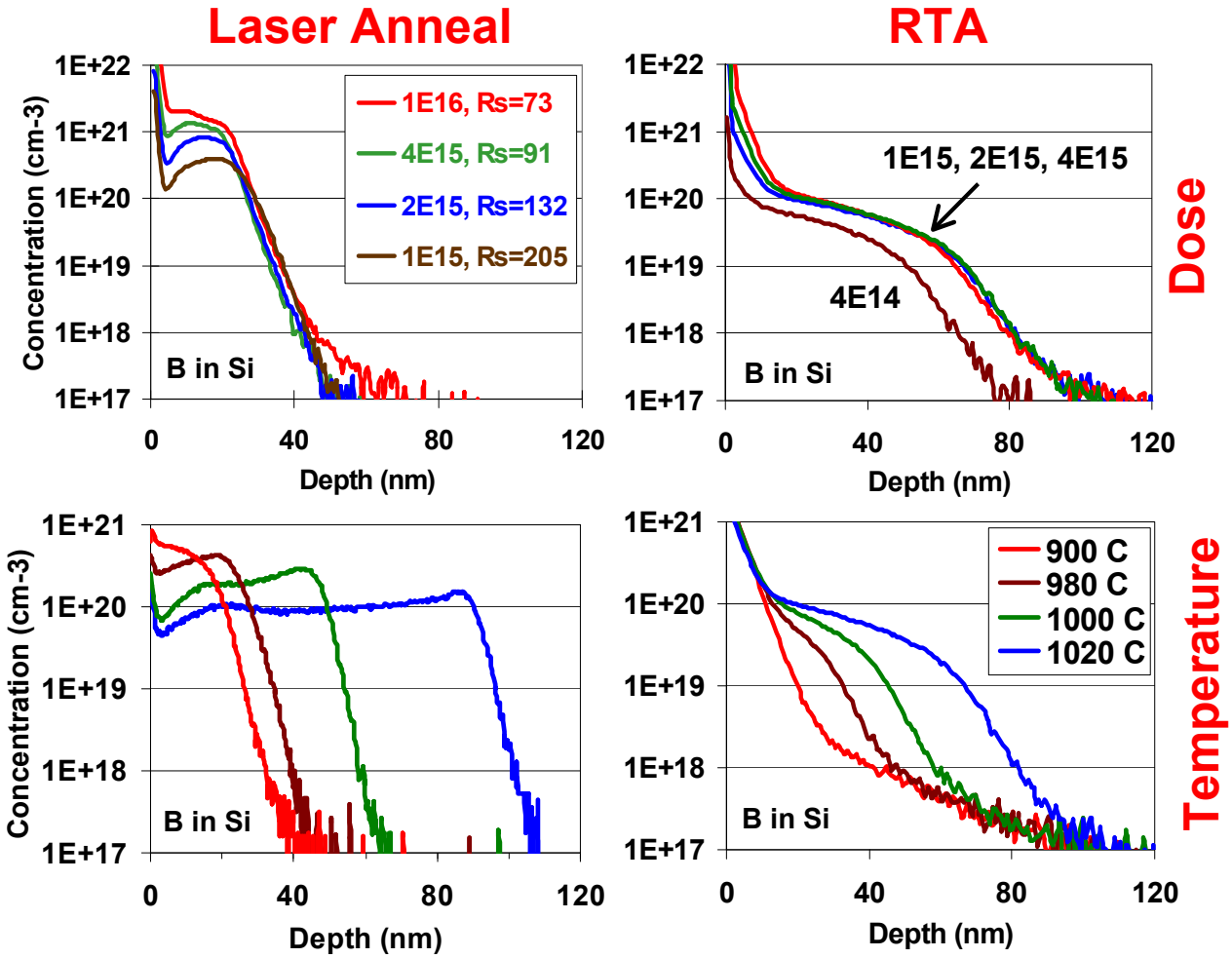
Dopant solubility limits are controlled by slower rather than faster processes permitting super-activation

Slow characteristic times include clustering or precipitation reactions



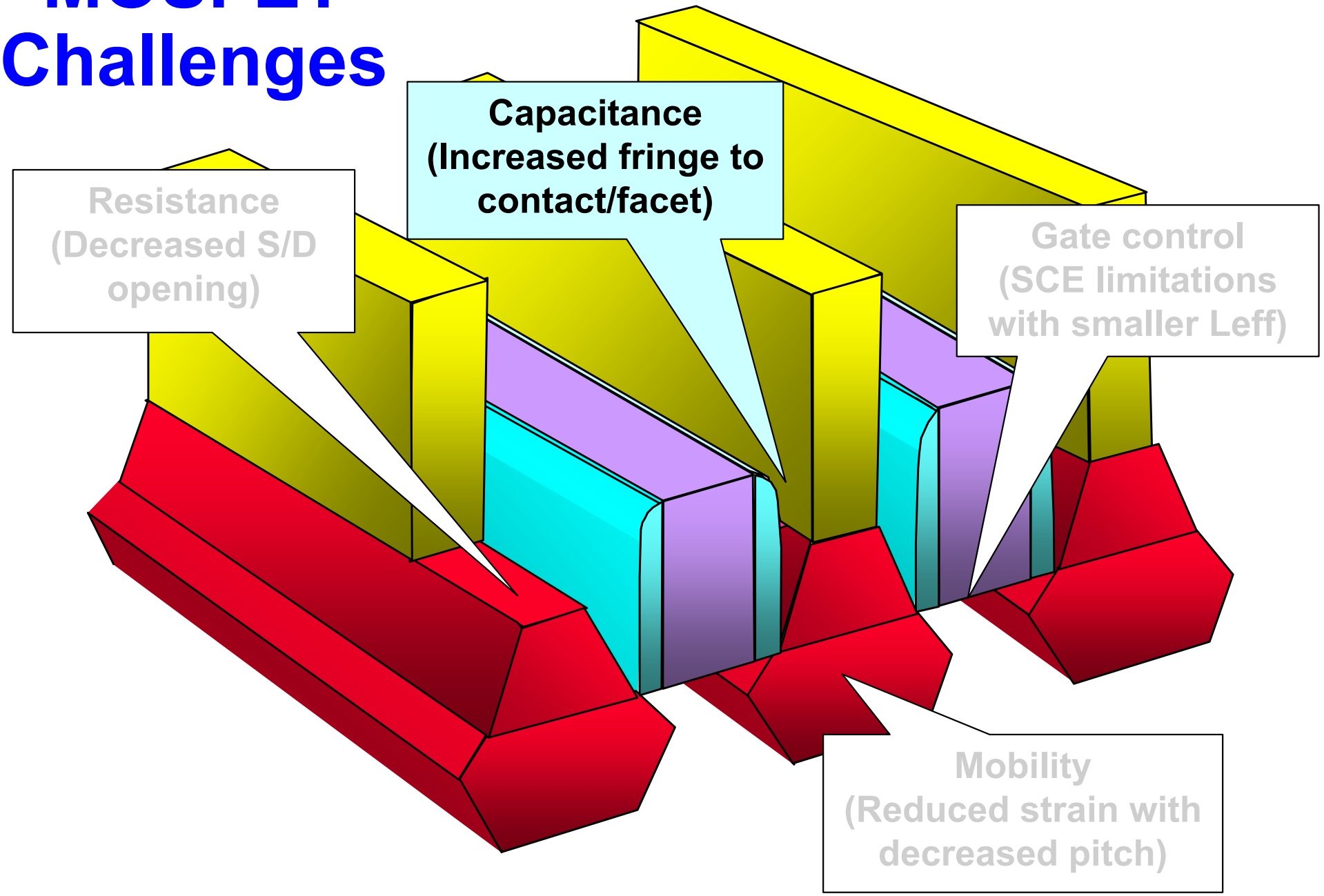
Fast characteristic times include Si Int diffusion and clustering and dopant substitutionality via substitutional-interstitial exchange reaction

Superactivation with solid-phase epitaxial regrowth (SPER)

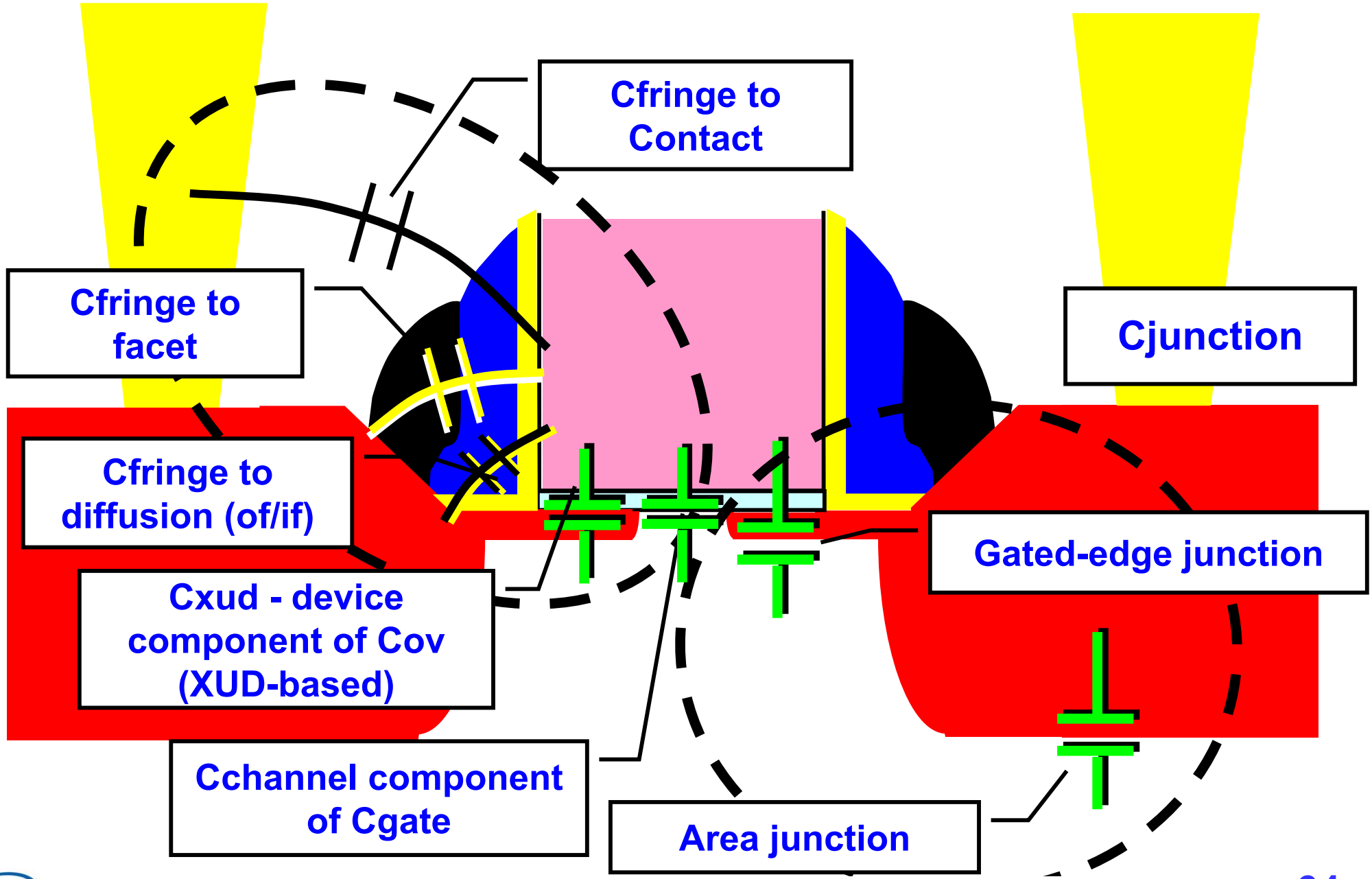


Laser melt anneal vs RTA, showing increased abruptness and non-equilibrium enhanced activation (superactivation).

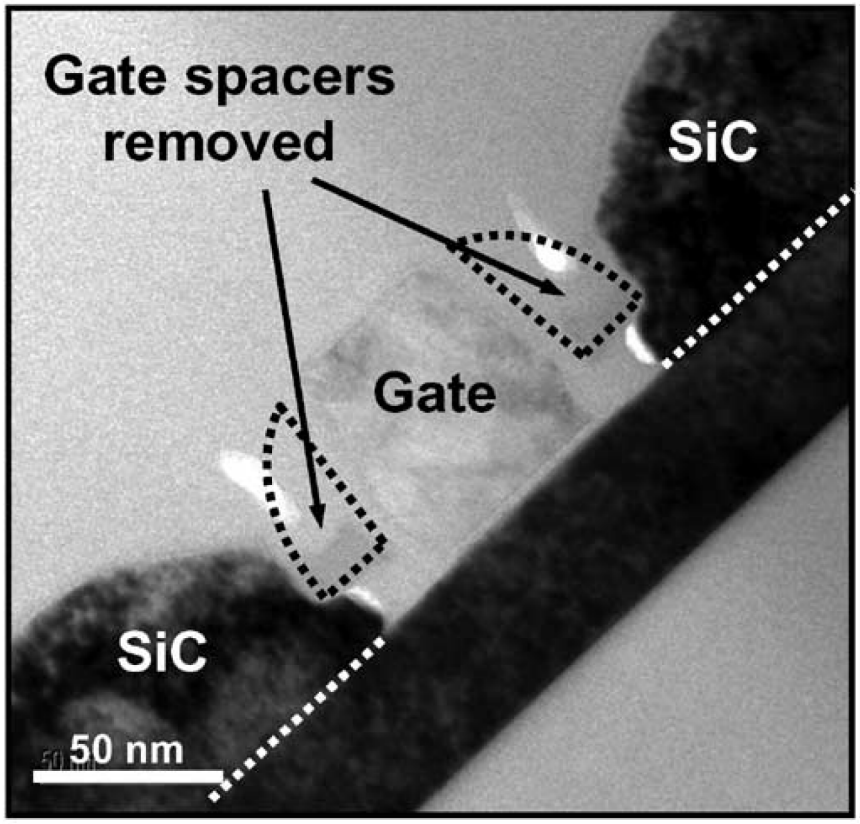
MOSFET Challenges

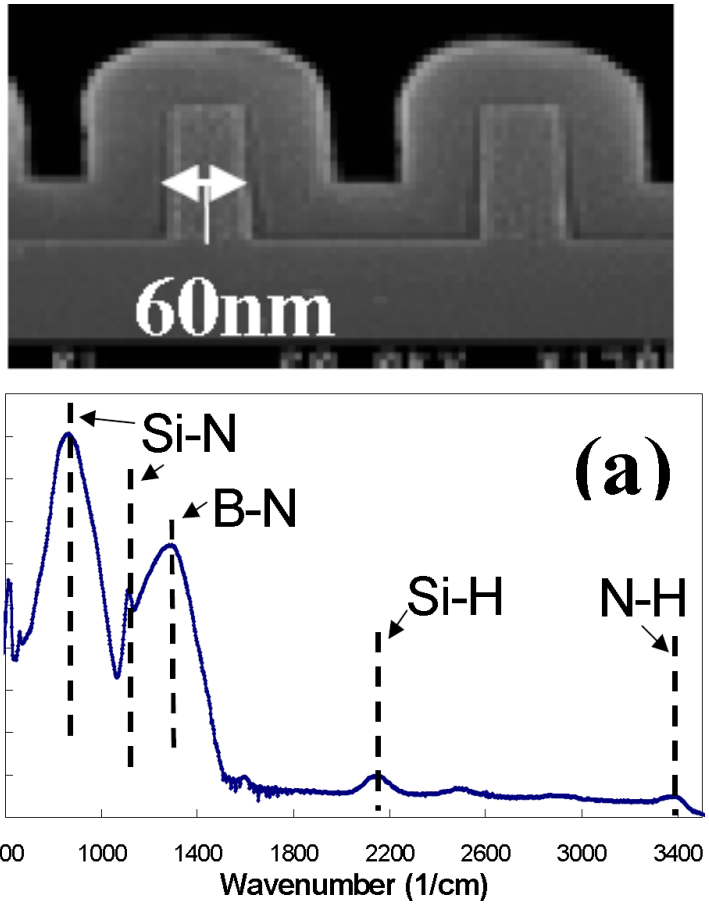


Planar Capacitive Elements



Innovative Spacer Technologies





SPACER REMOVAL
Liow – NUS Singapore
EDL 2008

SiBCN (Low-K) SPACER
Ko –TSMC
VLSI 2008

AGENDA

- Scaling
- Gate control
- Mobility
- Resistance
- Capacitance
- Summary

Looking Forward

Low risk

Enhancements in strain technology

Enhancements in annealing/implant technology

Medium Risk

Optimized substrate and channel orientation

Reduction in MOS parasitic resistance

Reduction in MOS parasitic capacitance

High risk

UTB devices

MuGFETS

Nanowires