

WHITE PAPER

LVDS Flat Panel Display Interface on Intel® Desktop Boards

July 2009

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1.0	Initial release of the LVDS Flat Panel Interface on Intel Desktop Boards White Paper	July 2009

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1 Introduction

LVDS flat panel displays are common in the industry because they are the building block for all modern flat panel monitors. The interface for such displays, however, is not standardized and, as a consequence, Intel Desktop Boards with direct LVDS flat panel connectivity follow a specific implementation.

Furthermore, system EMC certification is highly dependent on the target chassis. While select Intel Desktop Boards with an LVDS interface are tested against EMI compliance with the interface fully operational, the actual EMC certification of the desktop board is performed using standard "off-the-shelf" desktop-style chassis which do not accommodate LVDS panels. These desktop boards are, therefore, shipped from the factory with the LVDS flat panel display interface disabled in order to comply with EMC regulations.

Enabling the LVDS flat panel display interface is a system integrator option and is only supported as a joint effort with system integrators using LVDS flat panel displays in their system designs. System integrators (or resellers) enabling the LVDS interface as part of their product lineup own the support and EMC certification of such system (or potential system) for end-users.

1.1 Overview

Select Intel Desktop Boards may support a local flat panel display via onboard LVDS connectivity. Such implementation of the LVDS flat panel display interface can enable a wide range of display panels for maximum flexibility when defining All-in-One system configurations.

Table 1 summarizes the major features of the LVDS flat panel display interface implementation on select Intel Desktop Boards.

Table 1. LVDS Interface on Select Intel Desktop Boards

Panel Connectivity	30-pin header (data, clock, EDID and panel logic power)
Panel Power	Voltage selection jumper for 3.3 V/5 V/12 V panel voltage support
Inverter Connectivity	7-pin header supporting backlight lamp PWM control and inverter power
Inverter Power	Voltage selection jumper for 5 V/12 V backlight inverter voltage support

1.2 24-bpp Display Panel Compatibility

LVDS support for 18 bpp (6-bits/color) is based on three differential data-pairs, plus a differential clock signal, per channel. In contrast, 24-bpp (8 bits/color) panels require four differential data-pairs, plus the differential clock signal, per channel.

Consequently, an onboard 18-bpp LVDS solution does not support 24-bpp panels in 24-bpp mode; however, certain types of 24-bpp panels can operate in 18-bpp mode.

For a 24-bpp panel to function properly on an 18-bpp interface the panel must expect the RGB Least Significant Bits (Red[1:0], Green[1:0] and Blue[1:0]) to be transmitted on the fourth differential data pair. This is referred to as the 24.0 LVDS data format.¹

Figure 1 shows the LVDS connection between an 18-bpp interface and a 24-bpp panel:

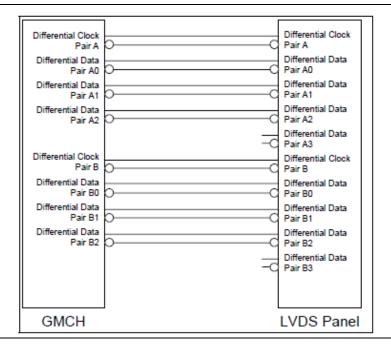


Figure 1. LVDS Connection Between 18-bpp Interface and 24-bpp Panel

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For more information on LVDS data formats, refer to

<u>Using 24-bpp LVDS Panels with Intel® Mobile Chipsets for Embedded Applications</u>, Section 3.2 "24-bpp Panel On A 18-bpp Interface".

2 Hardware Support

The LVDS flat panel display interface on select Intel Desktop Boards consists of a group of connectors and jumpers.

2.1 LVDS Panel Connector

The LVDS panel connector is a 30-pin (dual-row) shrouded white header of 1.00-mm pitch, supporting video data, clock, and EDID signals, as well as panel logic power.

2.1.1 LVDS Panel Connector Pinout

Refer to Table 2 for LVDS panel header pinout definition.

Table 2. LVDS Panel Header Pinout on Select Intel Desktop Boards

Pin	Signal Name	Description	Pin	Signal Name	Description
1	LA_CLKN	LVDS Channel A diff clock output - negative	2	LB_CLKN	LVDS Channel B diff clock output - negative
3	LA_CLKP	LVDS Channel A diff clock output - positive	4	LB_CLKP	LVDS Channel B diff clock output - positive
5	EDID_3.3V	Power for EDID ROM	6	EDID_GND	Ground for EDID signals
7	LA_DATANO	LVDS Channel A diff data output – negative	8	LB_DATANO	LVDS Channel B diff data output – negative
9	LA_DATAP0	LVDS Channel A diff data output – positive	10	LB_DATAP0	LVDS Channel B diff data output – positive
11	LA_DATAN1	LVDS Channel A diff data output – negative	12	LB_DATAN1	LVDS Channel B diff data output – negative
13	LA_DATAP1	LVDS Channel A diff data output – positive	14	LB_DATAP1	LVDS Channel B diff data output – positive
15	GND	Ground	16	GND	Ground
17	LA_DATAN2	LVDS Channel A diff data output – negative	18	LB_DATAN2	LVDS Channel B diff data output – negative
19	LA_DATAP2	LVDS Channel A diff data output – positive	20	LB_DATAP2	LVDS Channel B diff data output – positive
21	GND	Ground	22	GND	Ground
23	GND	Ground	24	GND	Ground
25	3.3 V/5 V/12 V	Selectable LCD power output	26	3.3 V/5 V/12 V	Selectable LCD power output
27	3.3 V/5 V/12 V	Selectable LCD power output	28	3.3 V/5 V/12 V	Selectable LCD power output
29	EDID_CLK	EDID/DDC clock signal	30	EDID_DATA	EDID/DDC data signal

2.1.2 LVDS Panel Cable Recommendations

It is recommended that the cable used for connecting the onboard 30-pin LVDS header to the connector on the display panel support the following:

- 15 twisted-pairs for data, clock, EDID, and panel logic power connectivity
- ground shielding in the cable harness for EMI protection as well as a path to ground for 3.3 V/5 V/12 V power pins 25-28
- ground wire/connector from the shield for mounting hole attachment

2.1.3 LVDS Panel Voltage Selection

Select Intel Desktop Boards with LVDS interface connectivity provide configurable voltage levels for powering a wide range of display panels.

LVDS header pins 25-28 can supply a voltage level of 3.3 V (default), 5 V or 12 V by properly setting the LVDS panel voltage selection jumper, comprised of a 2×3 , 2.00-mm pitch red header with a black jumper, keyed at pins 1 and 5.

Table 3 defines the configuration options for the LVDS panel voltage selection jumper.

Table 3. LVDS Panel Voltage Selection Jumper Configuration on Select Intel Desktop Boards

Voltage	Jumper 9	Setting	Configuration
3.3 V	2 and 4	2 6	Jumper position for 3.3 V (default)
5 V	6 and 4	2 6	Jumper position for 5 V
12 V	3 and 4	2 6	Jumper position for 12 V

2.2 Backlight Inverter Power Connector

The backlight inverter power connector is a 7-pin (single-row) shrouded red header of 2.00-mm pitch and 2 A current rating per pin, supporting backlight lamp enable and PWM control signals as well as inverter power.

2.2.1 Backlight Inverter Power Connector Pinout

Refer to Table 4 for backlight inverter power header pinout definition.

Table 4. Backlight Inverter Power Header Pinout on Select Intel Desktop Boards

Pin	Signal Name	Description
1	GND	Ground
2	GND	Ground
3	5 V/12 V	Inverter power
4	5 V/12 V	Inverter power
5	INV_RATING	Inverter rating
6	BKLT_PWM	Backlight PWM
7	BKLT_EN	Backlight enable

2.2.2 Backlight Inverter Power Cable Recommendation

It is recommended that the cable used for connecting the onboard 7-pin backlight inverter power header to the connector on the inverter board supports the current rating per wire as required by the inverter board (up to 2 A per pin).

2.2.3 Backlight Inverter Power Voltage Selection

The board provides configurable voltage levels for powering diverse backlight inverter boards.

Backlight inverter power header pins 3-4 can supply a voltage level of 5 V (default) or 12 V by properly setting the backlight inverter power voltage selection jumper, comprised of a 1 x 3, 2.54-mm pitch red header with a black jumper, with 3 A rating per pin.

Table 5 defines the configuration options for the backlight inverter power voltage selection jumper.

Table 5. Backlight Inverter Power Voltage Selection Jumper Configuration on Select Intel Desktop Boards

Voltage	Jumper Setting	Configuration
5 V	1 and 2	Jumper position for 5 V (default)
12 V	3 and 2	Jumper position for 12 V