Intel® Server Board S2600CP Family

Intel® Server System P4000CP Family

Technical Product Specification

Intel order number G26942-003

Revision 1.1

March, 2012

Enterprise Platforms and Services Division - Marketing

Revision History

Date	Revision Number	Modifications
January, 2012	1.0	Initial release.
March, 2012	1.1	Added Intel® Server Board S2600CP2J.

Disclaimers

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1. Introduction

This *Technical Product Specification* (TPS) provides information on Intel® Server Board S2600CP and Intel® Server System P4000CP including architecture, features and functionality.

In addition, you can obtain design-level information for a given subsystem by ordering the *External Product Specifications* (EPS) for the specific subsystem. EPS documents are not publicly available and you must order them through your local Intel representative.

Chapter Outline

This document is divided into the following chapters:

- Chapter 1 - Introduction
- Chapter 2 - Intel® Server Board S2600CP Overview
- Chapter 3 - Intel® Server System P4000CP Overview
- Chapter 4 - Intel® Server Board S2600CP Functional Architecture
- Chapter 5 – System Security
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- Chapter 8 - Intel® Server Board S2600CP Jumper Blocks
- Chapter 9 - Intel® Light Guided Diagnostics
- Chapter 10 - Intel® Server System P4000CP Front Control Panel and Back Panel
- Chapter 11 - Intel® Server System P4000CP Storage and Peripheral Drive Bays
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1.1 Server Board Use Disclaimer

Intel® Server Boards contain a number of high-density VLSI (Very-large-scale integration) and power delivery components that require adequate airflow for cooling. Intel ensures through its own chassis development and testing that when Intel® server building blocks are used together, the fully integrated system meets the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of the published operating or non-operating limits.

2. Intel® Server Board S2600CP Overview

The Intel® Server Board S2600CP is a monolithic printed circuit board (PCBs) with features designed to support the pedestal server markets. This server board is designed to support the Intel® Xeon® processor E5-2600 product family. Previous generation Intel® Xeon® processors are not supported.

The Intel® Server Board S2600CP family includes different board configurations:

- Intel® Server Board S2600CP2: dual NIC ports
- Intel® Server Board S2600CP4: quad NIC ports
- Intel® Server Board S2600CP2J: dual NIC ports and no SCU ports

2.1 Intel® Server Board S2600CP Feature Set

Table 1. Intel® Server Board S2600CP Feature Set

Feature	Description
Processors	▪ Support for one or two Intel® Xeon® E5-2600 Processor(s) ▪ 8 GT/s Intel® Quick Path Interconnect (Intel® QPI) ▪ LGA 2011 Socket ▪ Thermal Design Power up to 135-W
Memory	▪ Eight memory channels (four channels for each processor socket) ▪ Channels A, B, C, D, E, F, G and H ▪ Support for 800/1066/1333/1600 MHz/s Registered DDR3 Memory (RDIMM), Unbuffered DDR3 memory ((UDIMM) and Load Reduced DDR3 memory (LRDIMM). ▪ DDR3 standard I/O voltage of 1.5V and DDR3 Low Voltage of 1.35V **Refer to chapter 4.2.2 for detail information for memory support.**
▪ Chipset	Intel® C600 -A chipset with support for Intel® C600 RAID Upgrade Keys
Cooling Fan Support	▪ Two processor fans (4-pin headers) ▪ Six front system fans (6-pin headers) ▪ One rear system fan (4-pin header)
Add-in Card Slots	▪ Support up to six expansion slots ▪ From first processor: o Slot 1: PCIe Gen III x4/x8 electrical with x8 physical connector o Slot 2: PCIe Gen III x8 electrical with x8 physical connector o Slot 3: PCIe Gen III x8 electrical with x8 open-ended physical connector o Slot 4: PCIe Gen III x8 electrical with x8 physical connector o Slot 6: PCIe Gen III x8 electrical with x16 connector, support riser card. ▪ From second processor: o Slot 5: PCIe Gen III x8 electrical with x8 open-ended physical connector. **PCIe slot 5 is functional only when the second processor is installed.**

Feature	Description
Hard Drive and Optical Drive Support	▪ Intel® Server Board S2600CP2/S2600CP2J/S2600CP4: Two SATA connectors at 6 Gbps (white connectors) and four SATA connectors at 3 Gbps (black connectors). **The 6 Gbps connectors are recommended connectors for ODDs.** ▪ Intel® Server Board S2600CP2/S2600CP4: Up to eight SATA/SAS connectors at 3 Gbps with optional Intel® C600 RAID Upgrade Keys
RAID Support	▪ Intel RSTe SW RAID 0/1/10/5 ▪ LSI SW RAID 0/1/10
External I/O Connectors	▪ One DB-15 video connector ▪ One DB9 serial port A connection ▪ Support two or four 10/100/1000Mb NIC ▪ Four USB 2.0 ports
Internal I/O Connectors/Headers	▪ One 2x5 pin connector providing front panel support for two USB ports ▪ One internal Type-A USB 2.0 port ▪ One internal USB port to support low profile eUSB SSD ▪ One DH-10 serial Port B connector ▪ One combined header consists of a 24-pin SSI-EEB compliant front panel header and a 4-pin header for optional NIC3/4 LED ▪ One 1x7pin header for optional Intel® Local Control Panel support
Video Support	Integrated Matrox* G200 2D Video Graphics controller
LAN	Intel® Server Board S2600CP2/S2600CP2J : Two Gigabit network through Intel® I350 10/100/1000 integrated MAC and PHY controller Intel® Server Board S2600CP4: Four Gigabit network through Intel® I350 10/100/1000 integrated MAC and PHY controller
Server Management	▪ Onboard ServerEngines* LLC Pilot III* Controller ▪ Support for Intel® Remote Management Module 4 solutions ▪ Intel® Light-Guided Diagnostics on field replaceable units ▪ Support for Intel® System Management Software ▪ Support for Intel® Intelligent Power Node Manager (Need PMBus-compliant power supply)
BIOS Flash	▪ Winbond* W25Q64BV
Form Factor	▪ SSI EEB (12"x13")
Compatible Intel® Server Chassis	Inte!® Server Chassis P4000M chassis

2.2 Server Board Layout

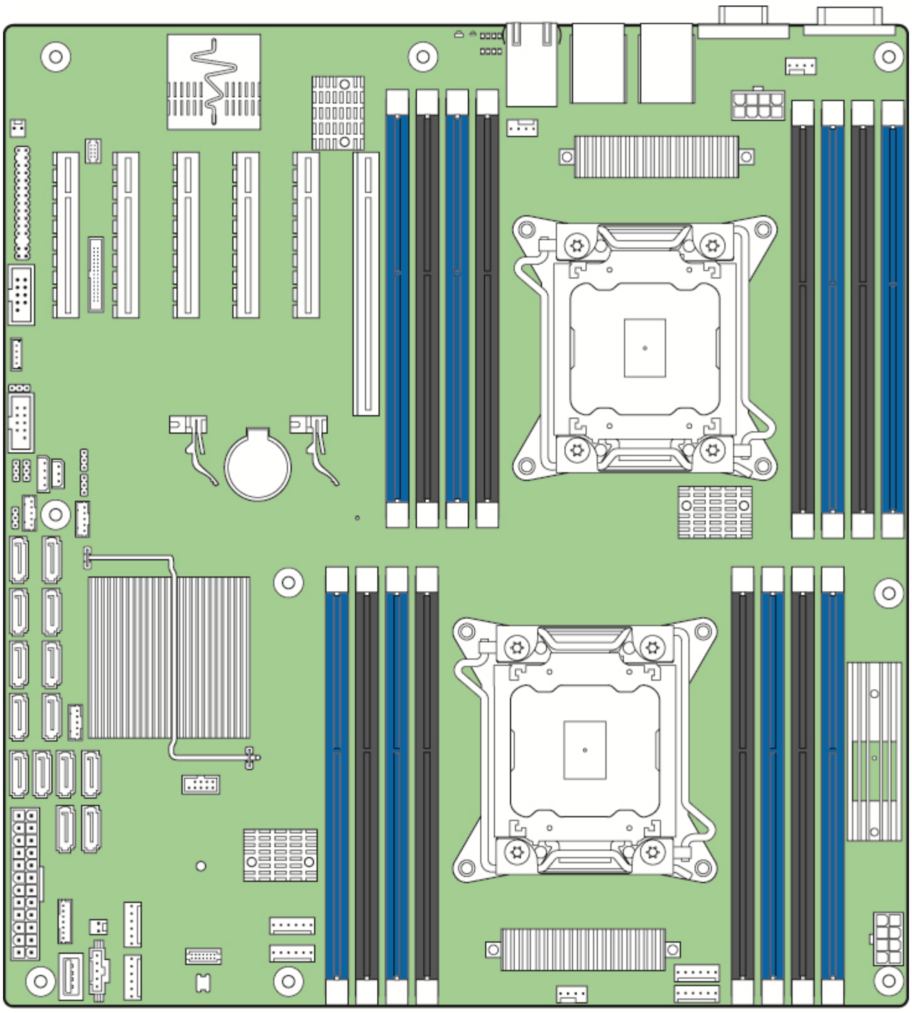


Figure 1. Intel® Server Board S2600CP4, Quad NIC

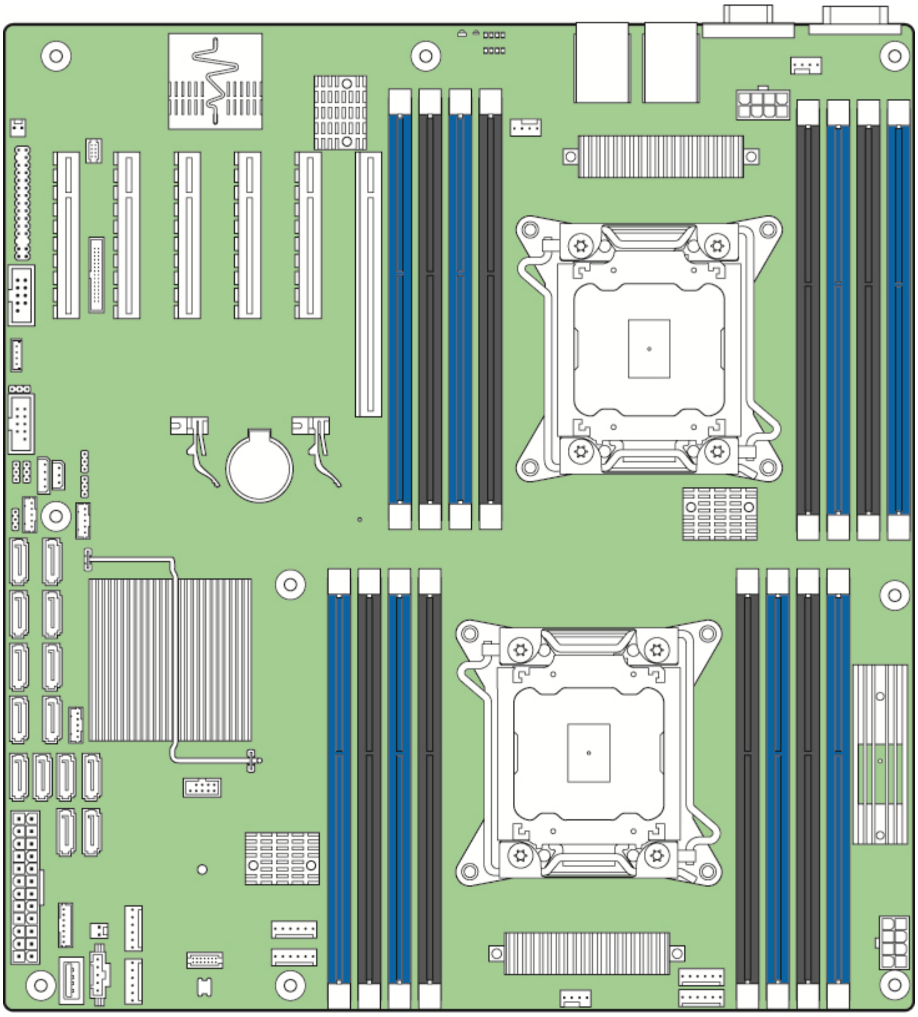


Figure 2. Intel® Server Board S2600CP2, Dual NIC

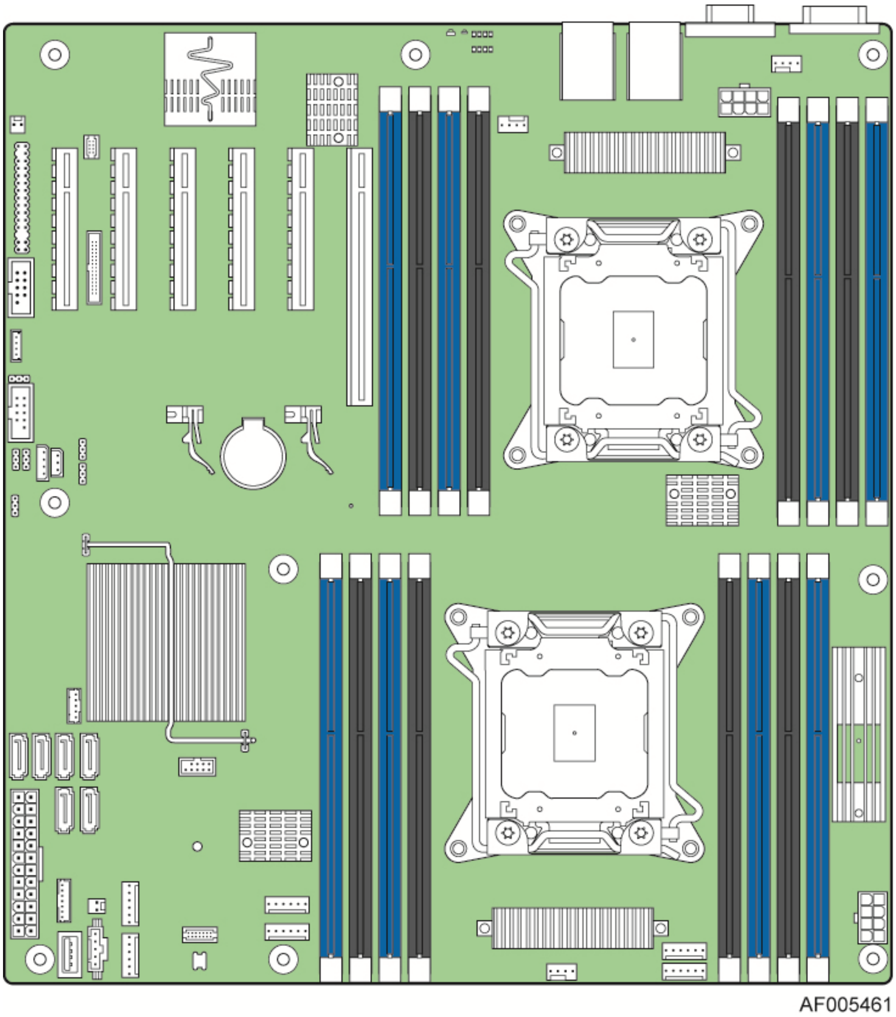
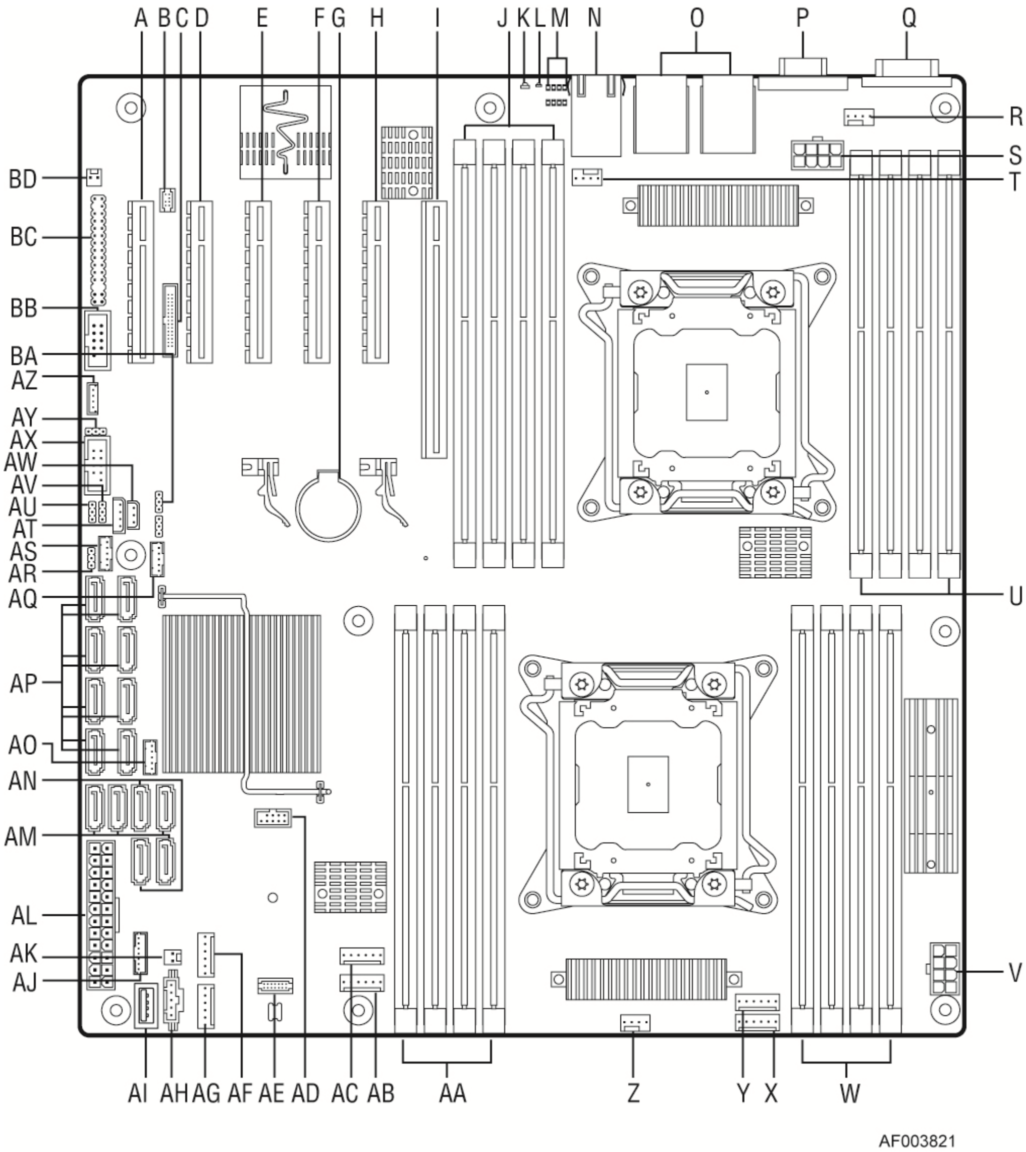


Figure 3. Intel® Server Board S2600CP2J, Dual NIC

2.2.1 Server Board Connector and Component Layout

The following figure shows the layout of the server board. Each connector and major component is identified by a number or letter, and a description is given below the figure.



Callout	Description	Callout	Description
A	Slot 1, PCI Express* Gen3	AC	System Fan 4 connector
B	RMM4 LITE	AD	Internal eUSB SSD
C	RMM4 NIC	AE	TPM
D	Slot 2, PCI Express* Gen3	AF	System Fan 2
E	Slot 3, PCI Express* Gen3, open-ended	AG	System Fan 1
F	Slot 4, PCI Express* Gen3	AH	PMBus
G	Battery	AI	Type-A USB
H	Slot 5, PCI Express* Gen3, from second processor, open-ended	AJ	LCP
I	Slot 6, PCI Express* Gen3, support riser card	AK	HDD activity LED
J	DIMM E1/E2/F1/F2	AL	Main Power

Callout	Description	Callout	Description
K	System Status LED	AM	SATA 3G connector
L	ID LED	AN	SATA 6G connector
M	Diagnostic LED	AO	SATA SGPIO
N	NIC 3/4 (only on Intel® Server Board S2600CP4)	AP	SATA/SAS 3G connector (NOT available on Intel® Server Board S2600CP2J)
O	USB 0/1/2/3, NIC 1,2	AQ	SAS SGPIO 2
P	VGA	AR	Password Clear
Q	Serial Port A	AS	SAS SGPIO 1
R	Processor 2 Fan connector	AT	IPMB
S	Processor 2 Power connector	AU	ME Force Update
T	System Fan 7 connector	AV	BMC Force Update
U	DIMM H1/H2/G1/G2	AW	HSBP_I2C
V	Processor 1 Power connector	AX	USB to front panel
W	DIMM A1/A2/B1/B2	AY	BIOS Default
X	System Fan 5 connector	AZ	Intel C600 RAID Upgrade key connector
Y	System Fan 6 connector	BA	BIOS Recovery
Z	Processor 1 Fan connector	BB	Serial B connector
AA	DIMM C1/C2/D1/D2	BC	SSI Front Panel (24-pin) and NIC 3/4 LED (4-pin)
AB	System Fan 3 connector	BD	Chassis Intrusion

Figure 4. Major Board Components

2.2.2 Server Board Mechanical Drawings

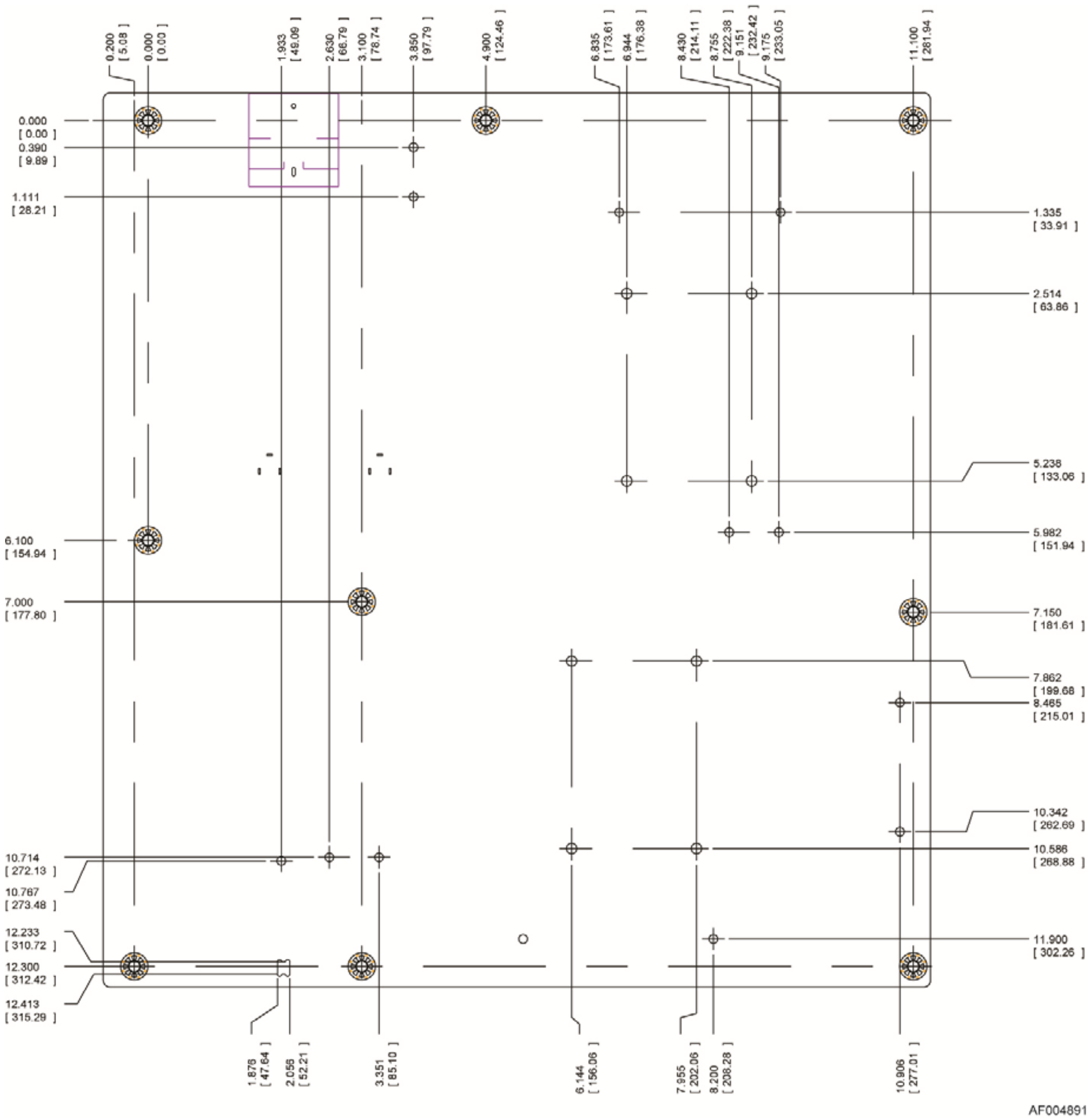


Figure 5. Mounting Hole Locations (1 of 2)

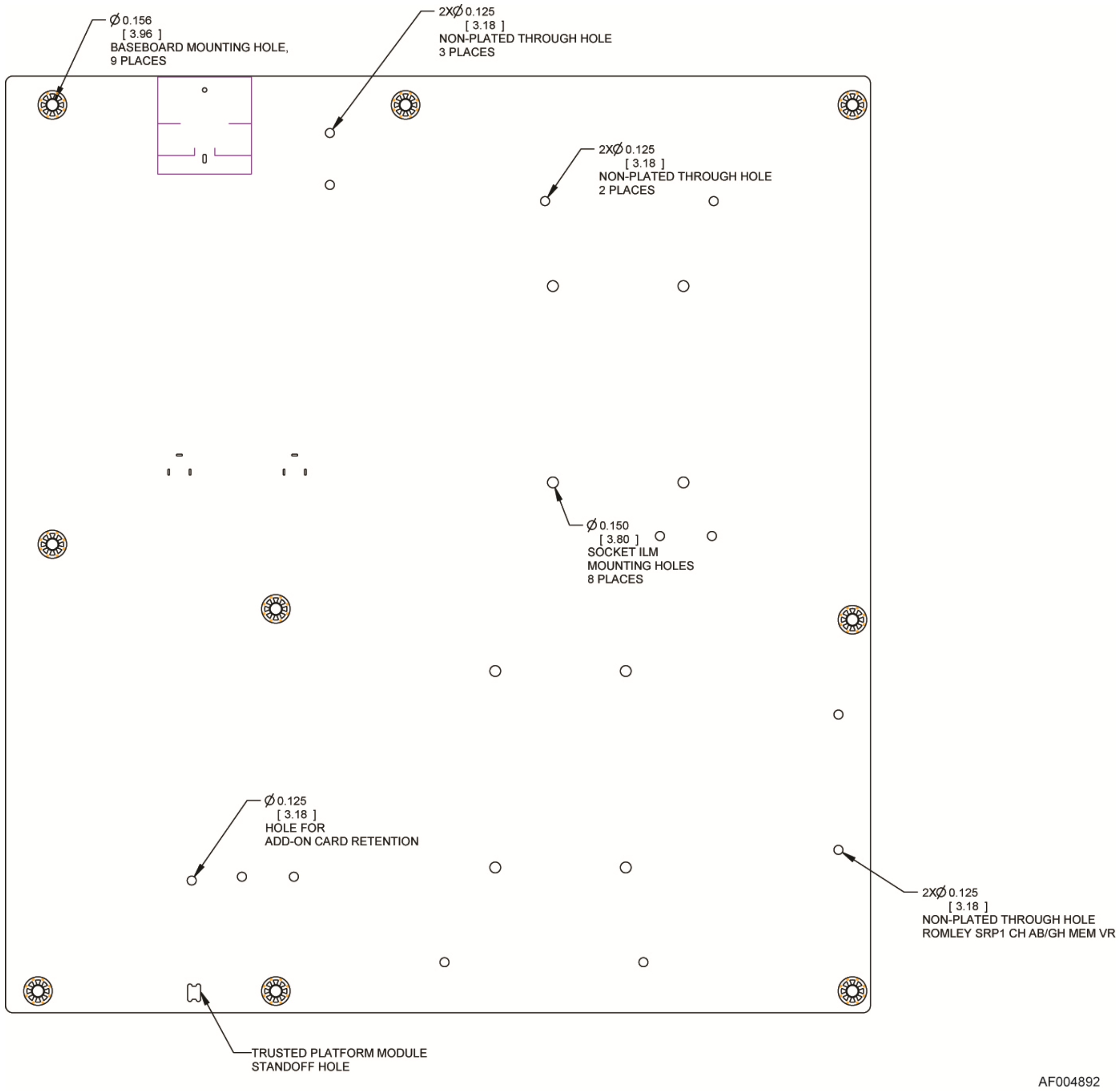


Figure 6. Mounting Hole Locations (2 of 2)

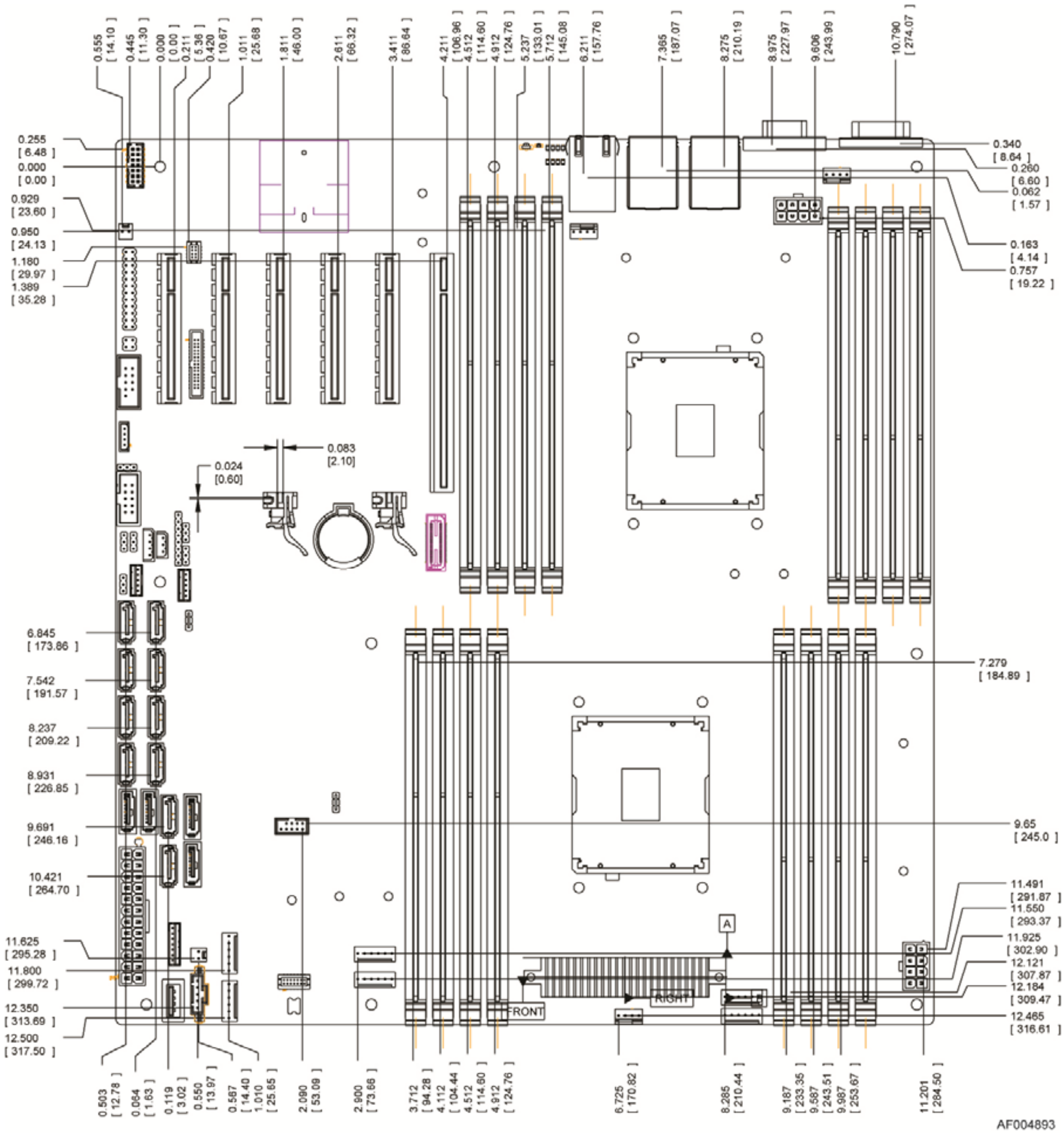


Figure 7. Major Connector Pin-1 Locations (1 of 3)

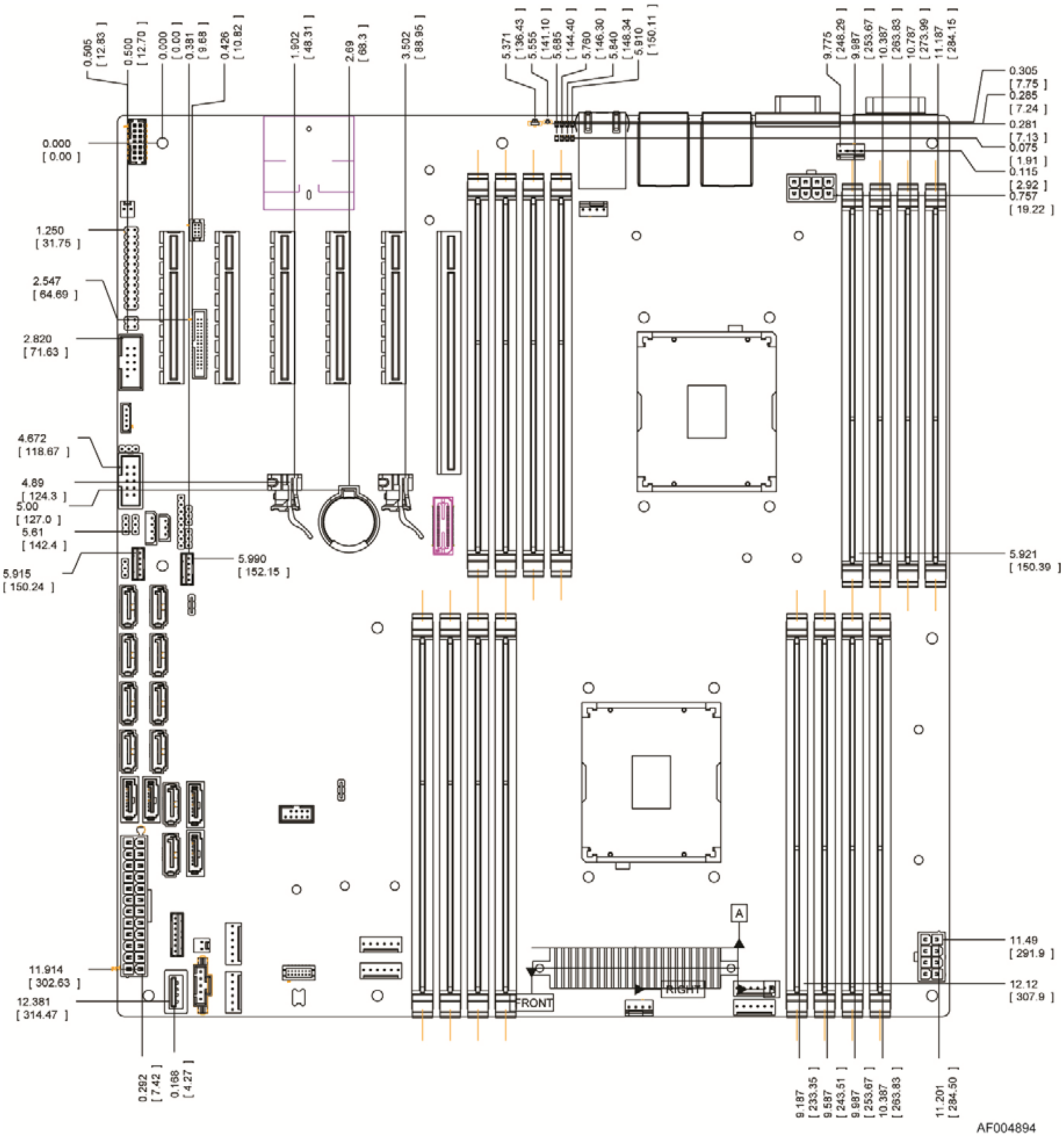


Figure 8. Major Connector Pin-1 Locations (2 of 3)

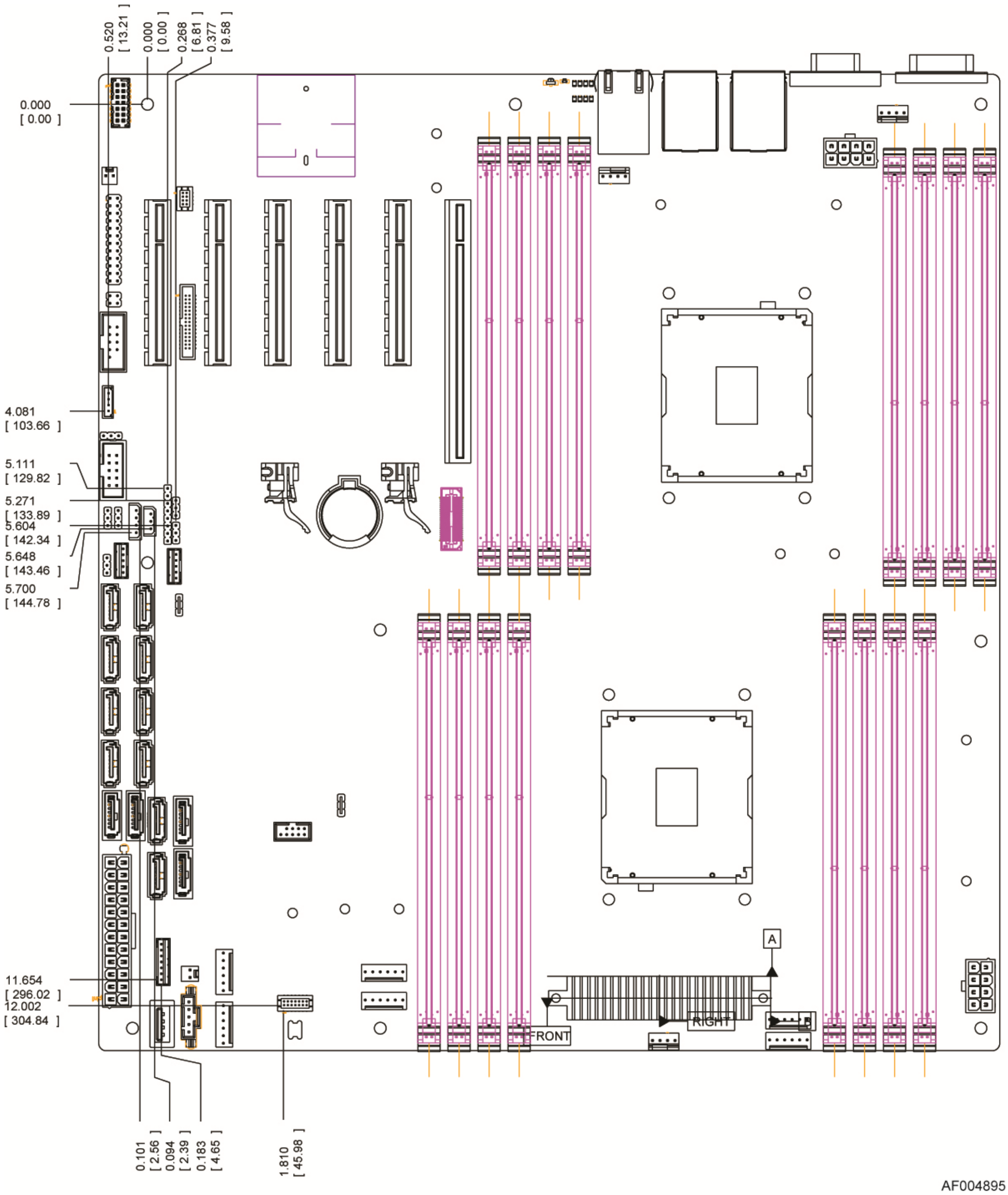


Figure 9. Major Connector Pin-1 Locations (3 of 3)

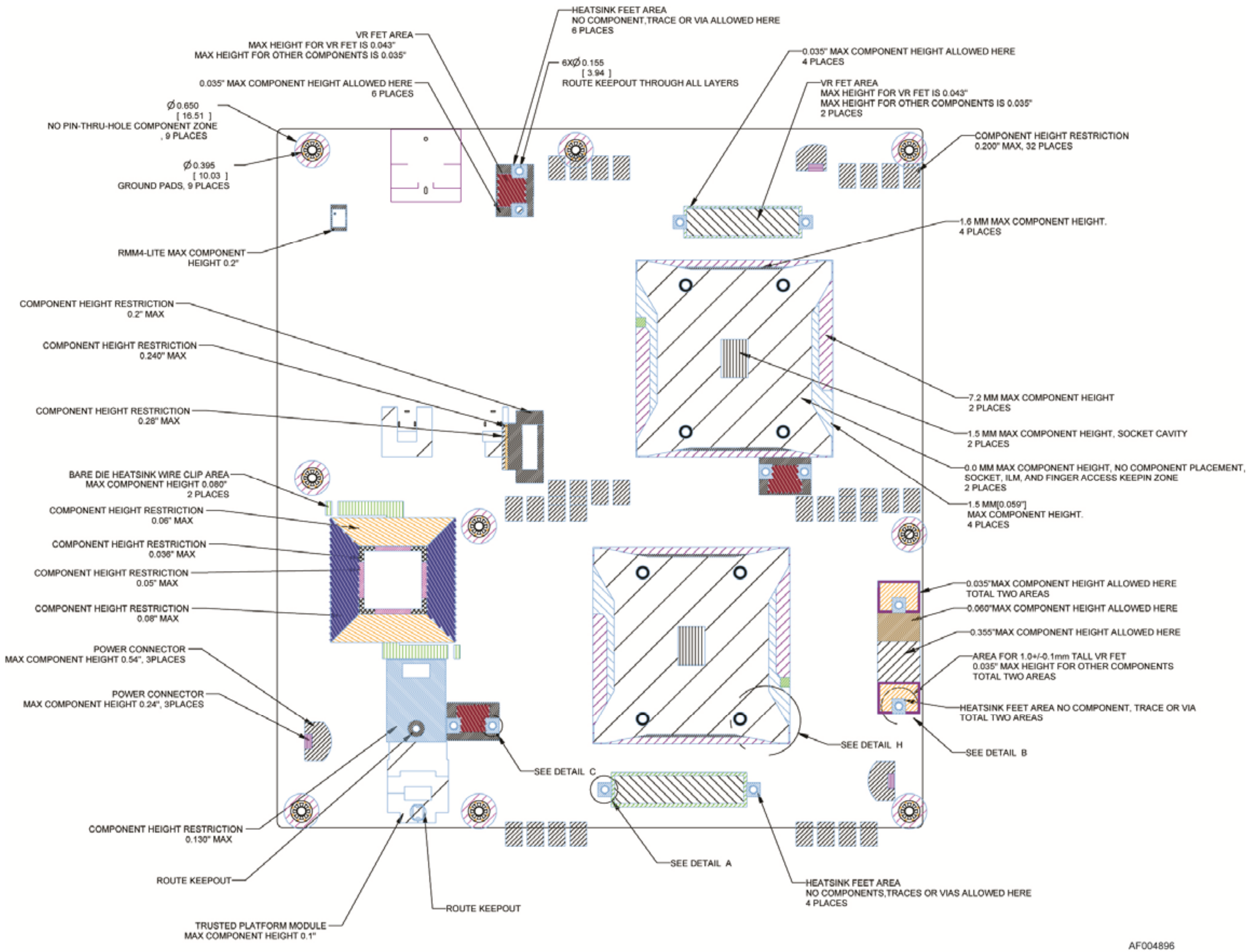


Figure 10. Primary Side Keep-out Zone (1 of 2)

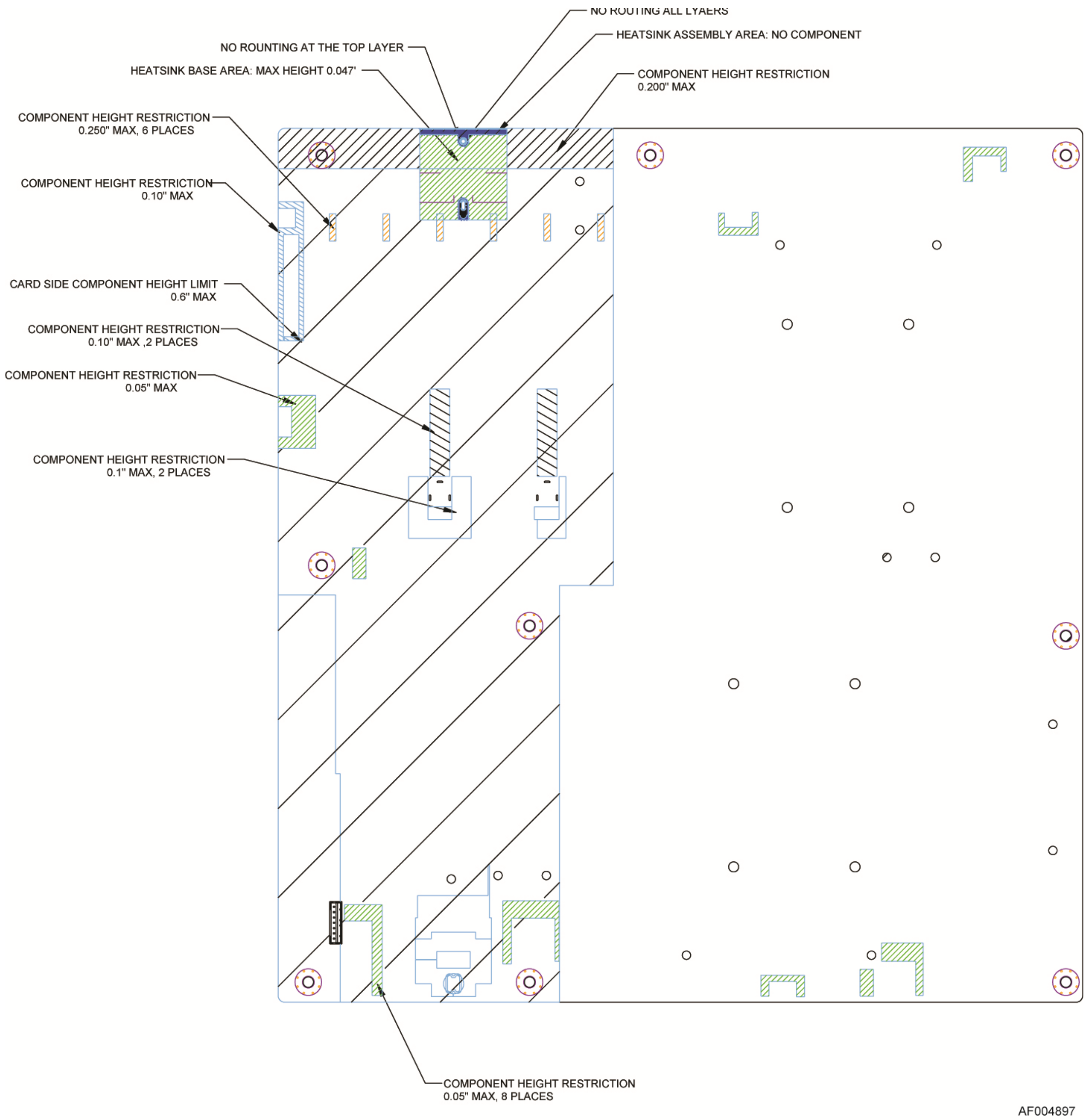


Figure 11. Primary Side Card-Side Keep-out Zone

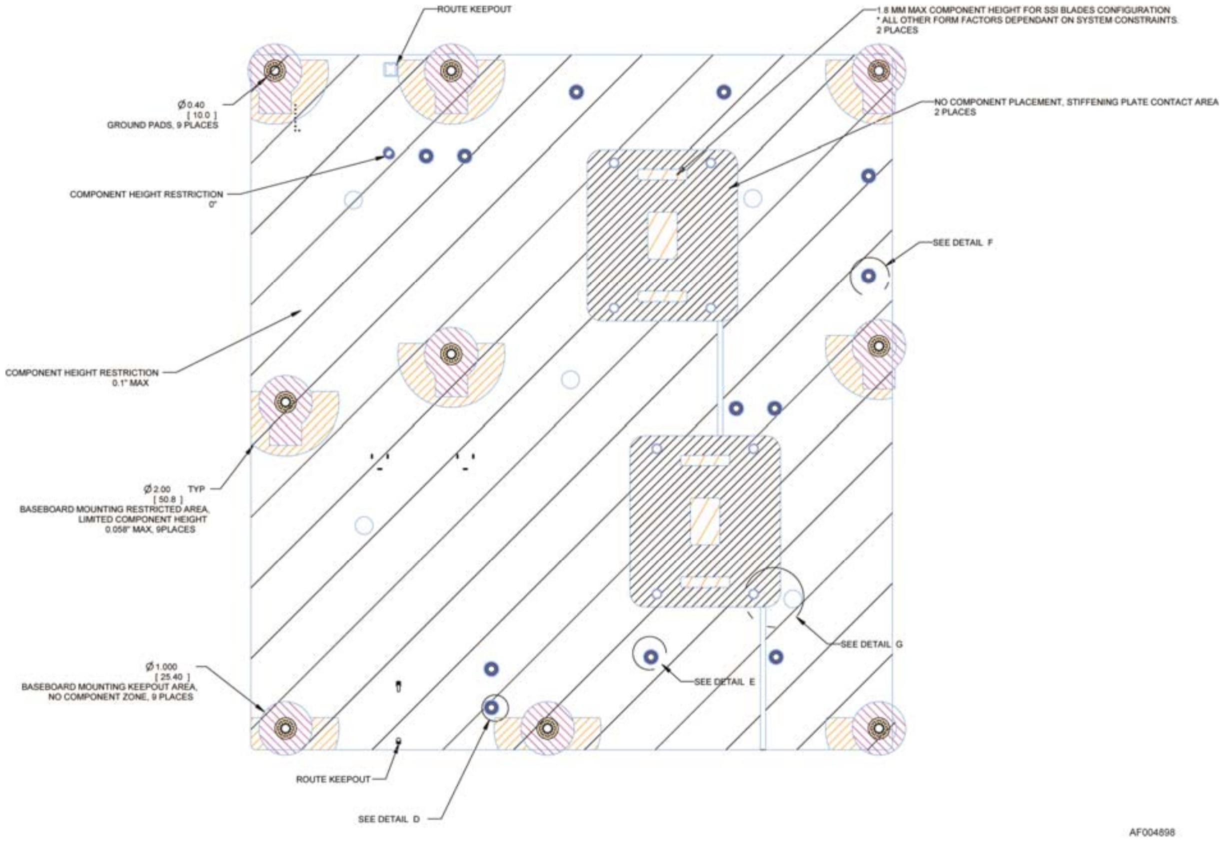
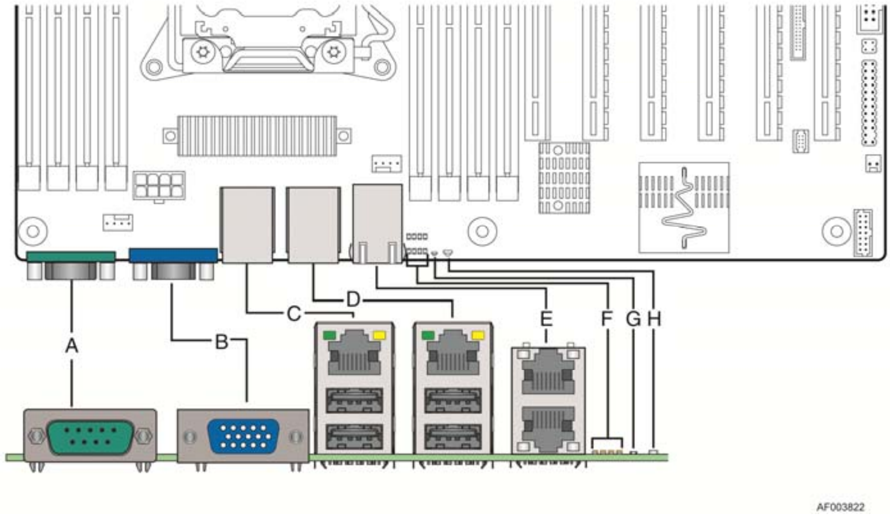


Figure 12. Second Side Keep-out Zone

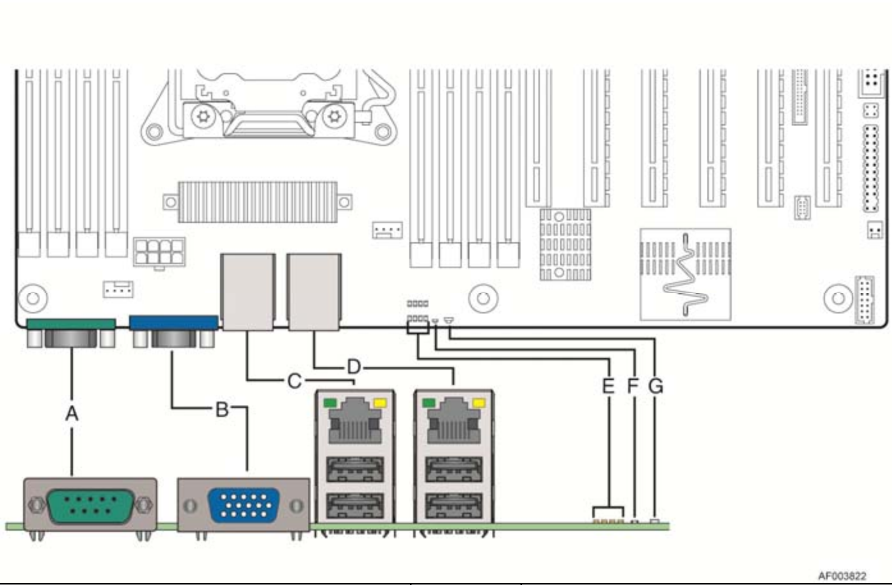
2.2.3 Server Board Rear I/O Layout

The following drawing shows the layout of the rear I/O components for the server boards.



Callout	Description	Callout	Description
A	Serial Port A	E	NIC Port 3 (top) and 4 (bottom)
B	Video	F	Diagnostics LED's
C	NIC Port 1, USB Port 0 (top) and 1 (bottom)	G	ID LED
D	NIC Port 2, USB Port 2 (top) and 3 (bottom)	H	System Status LED

Figure 13. Rear I/O Layout of Intel® Server Board S2600CP4



Callout	Description	Callout	Description
A	Serial Port A	E	Diagnostics LED's
B	Video	F	ID LED
C	NIC Port 1, USB Port 0 (top) and 1 (bottom)	G	System Status LED
D	NIC Port 2, USB Port 2 (top) and 3 (bottom)		

Figure 14. Rear I/O Layout of Intel® Server Board S2600CP2/S2600CP2J

3. Intel® Server System P4000CP Overview

The Intel® Server System P4000CP is a server product family including Intel® Server System P4308CP4MHEN, P4308CP4MHGC and P4208CP4MHGC which are integrated with different chassis models from Intel® Server Chassis P4000M family, Intel® Server Board S2600CP4 and other accessories.

This document provides system level information for the Intel® Server System P4000CP product family. This document will describe the functions and features provided by the integrated server system. For chassis layout, system boards, power sub-system, cooling sub-system or storage sub-system, please refer to *Intel® Server Chassis P4000M Family Technical Product Specification*.

3.1 Integrated System Family Overview

The dimension of Intel® Server System P4000CP is 17.24 in (438 mm) x 6.81 in (173mm) x 25 in (612 mm) (Height X Width X Depth).

The color of Intel® Server System P4000CP is cosmetic black (GE 701 or equivalent), with service parts as Intel blue, and hot swap parts as Intel green.

Intel® Server System P4308CP4MHEN includes:

- Intel® Server Board S2600CP4
- Intel® Server Chassis P4308XXMXXMHEN
- Intel® C600 RAID Upgrade Key RKSATA8

Intel® Server Chassis P4308XXMXXMHEN includes a fixed single 550W non-redundant 80+ Silver power supply and one 8x3.5" hot-swap HDD cage allows support for up to eight hot-swap SATA/SAS drives. Two tachometer output fans (120mmX38mm) are mounted at the front edge of the chassis and one air duct for Intel® Server Board. Three 5.25-inch half-height peripheral bays are available for the installation of a floppy drive, CD-ROM drive, and/or other accessories. The standard chassis configuration is pedestal.

Intel® Server System P4308CP4MHGC includes:

- Intel® Server Board S2600CP4
- Intel® Server Chassis P4308XXMXXMHGC
- Intel® C600 RAID Upgrade Key RKSATA8

Intel® Server Chassis P4308XXMXXMHGC includes two 750-W redundant PSUs and one 8x3.5" hot-swap HDD cage allows support for up to eight hot-swap SATA/SAS drives. Five redundant hot-swap fans (80x38mm) at the front edge of the chassis and one air duct for Intel® Server Board. Three 5.25-inch half-height peripheral bays are available for the installation of a floppy drive, CD-ROM drive, and/or other accessories. The standard chassis configuration is pedestal.

Intel® Server System P4208CP4MHGC includes:

- Intel® Server Board S2600CP4
- Intel® Server Chassis P4208XXMXXMHGC

- Intel C600 RAID Upgrade Key RKSAS8

Intel® Server Chassis P4208XXMXXMHGC includes two 750-W redundant PSU and one 8x2.5" hot-swap HDD cage allows support for up to eight 2.5" hot-swap SATA/SAS drives. Five redundant hot-swap fans (80x38mm) at the front edge of the chassis and one air duct for Intel® Server Board. Three 5.25-inch half-height peripheral bays are available for the installation of a floppy drive, CD-ROM drive, and/or other accessories. The standard chassis configuration is pedestal.

The following table summarizes the Intel® Server System P4000CP features:

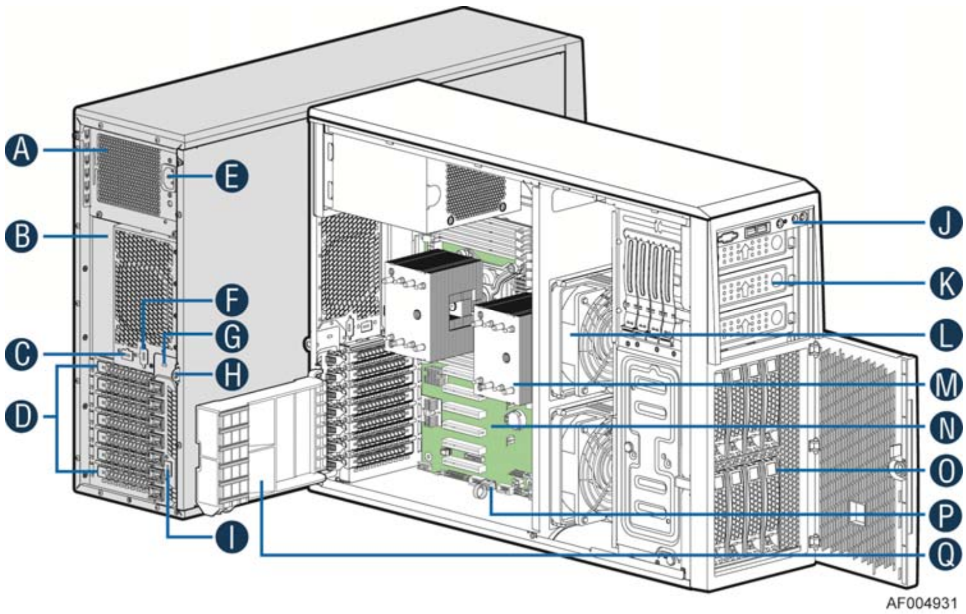
Table 2. Intel® Server System P4000CP family Features

Feature	Description
Processors	▪ Support for one or two Intel® Xeon® E5-2600 Processor(s) ▪ 8 GT/s Intel® Quick Path Interconnect (Intel® QPI) ▪ LGA 2011 Socket ▪ Thermal Design Power up to 135-W
Memory	▪ Eight memory channels (four channels for each processor socket) ▪ Channels A, B, C, D, E, F, G and H ▪ Support for 800/1066/1333/1600 MHz/s Registered DDR3 Memory (RDIMM), Unbuffered DDR3 memory ((UDIMM) and Load Reduced DDR3 memory (LRDIMM) ▪ DDR3 standard I/O voltage of 1.5V and DDR3 Low Voltage of 1.35V **Refer to chapter 4.2.2 for detail information for memory support.**
Chipset	Intel® C600 -A chipset with support for Intel® C600 RAID Upgrade Keys
Cooling Fan Support	▪ Two processor fans (4-pin headers) ▪ Six front system fans (6-pin headers) ▪ One rear system fan (4-pin header)
Add-in Card Slots	▪ Support up to six expansion slots ▪ From first processor: o Slot 1: PCIe Gen III x4/x8 electrical with x8 physical connector o Slot 2: PCIe Gen III x8 electrical with x8 physical connector o Slot 3: PCIe Gen III x8 electrical with x8 open-ended physical connector o Slot 4: PCIe Gen III x8 electrical with x8 physical connector o Slot 6: PCIe Gen III x8 electrical with x16 connector, support riser card. ▪ From second processor: o Slot 5: PCIe Gen III x8 electrical with x8 open-ended physical connector **PCIe slot 5 is functional only when the second processor is installed.**
Hard Drive and Optical Drive Support	▪ Two SATA connectors at 6 Gbps and four SATA connectors at 3 Gbps. **The 6 Gbps connectors are recommended connectors for ODDs.** ▪ Up to eight SATA/SAS connectors at 3 Gbps with optional Intel® C600 RAID Upgrade Keys
RAID Support	▪ Intel RSTe SW RAID 0/1/10/5 ▪ LSI SW RAID 0/1/10
External I/O Connectors	▪ One DB-15 video connector ▪ One DB9 serial port A connection ▪ Support two or four 10/100/1000Mb NIC ▪ Four USB 2.0 ports

Feature	Description
Internal I/O Connectors/Headers	▪ One 2x5 pin connector providing front panel support for two USB ports ▪ One internal Type-A USB 2.0 port ▪ One internal USB port to support low profile eUSB SSD ▪ One DH-10 serial Port B connector ▪ One combined header consists of a 24-pin SSI-EEB compliant front panel header and a 4-pin header for optional NIC3/4 LED ▪ One 1x7pin header for optional Intel® Local Control Panel support
Video Support	Integrated Matrox* G200 2D Video Graphics controller
LAN	▪ Four Gigabit network through Intel® I350 10/100/1000 integrated MAC and PHY controller
Server Management	▪ Onboard ServerEngines* LLC Pilot III* Controller ▪ Support for Intel® Remote Management Module 4 solutions ▪ Intel® Light-Guided Diagnostics on field replaceable units ▪ Support for Intel® System Management Software ▪ Support for Intel® Intelligent Power Node Manager (Need PMBus-compliant power supply)
BIOS Flash	Winbond* W25Q64BV
Form Factor	SSI EEB (12"x13")
Compatible Intel® Server Chassis	Intel® Server Chassis P4000M chassis

3.2 Intel® Server System P4000CP Family View

3.2.1 Intel® Server System P4308CP4MHEN View



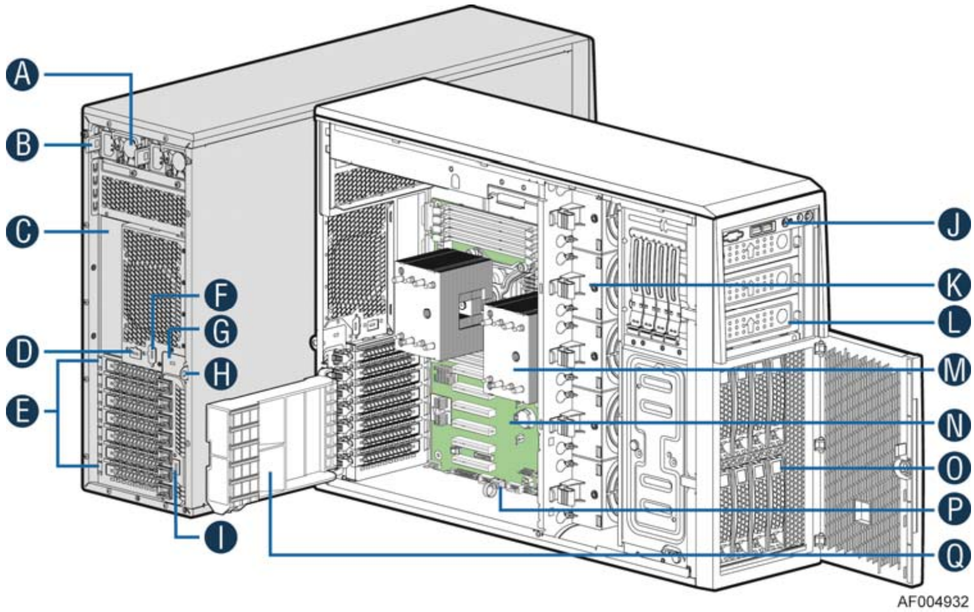
A. 550-W Fixed Power supply
B. I/O Ports
C. Alternate RMM4 Knockout
D. PCI Add-in Board Slot Covers

E. AC Input Power Connector
F. Serial Port Knockout
G. A Kensington* Cable Lock Mounting Hole
H. Padlock Loop
I. Alternate RMM4 Knockout
J. Front Control Panel
K. 5.25" Peripheral Bays
L. Fixed System Fan
M. Heat-sink
N. Intel® Server Board S2600CP4
O. 8x3.5" Hot-swap HDD Cage
P. Intel® RAID C600 Upgrade Key RKSATA8
Q. PCI-e Retainer

Figure 15. Intel® Server System P4308CP4MHEN View

Note: Airduct is not shown.

3.2.2 Intel® Server System P4308CP4MHGC View



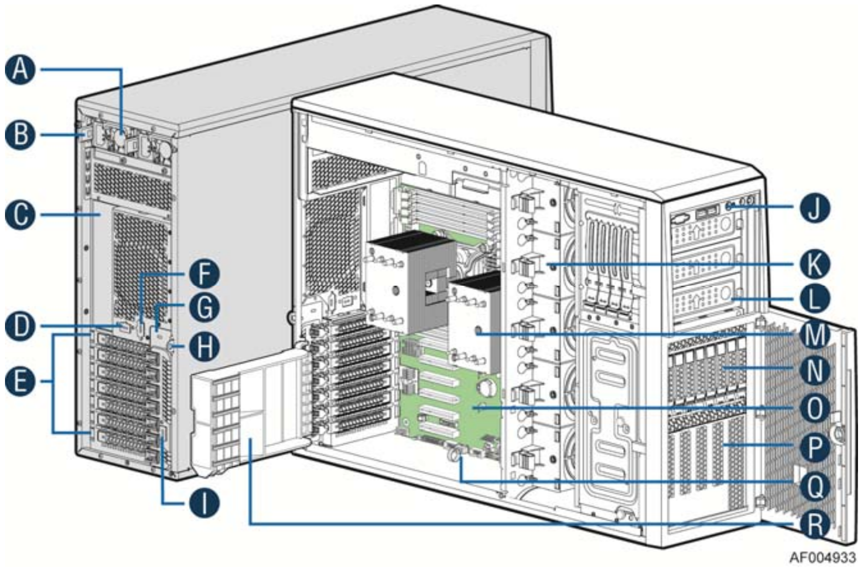
A. 750-W Redundant Power Supply
B. AC Input Power Connector
C. I/O Ports
D. Alternate RMM4 Knockout
E. PCI Add-in Board Slot Covers
F. Serial Port Knockout
G. A Kensington* Cable Lock Mounting Hole
H. Padlock Loop
I. Alternate RMM4 Knockout
J. Front Control Panel
K. Hot-swap System Fan
L. 5.25" Peripheral Bays
M. Heat-sink
N. Intel® Server Board S2600CP4
O. 8x3.5" Hot-swap HDD Cage

P. Intel® RAID C600 Upgrade Key RKSATA8
Q. PCI-e Retainer

Figure 16. Intel® Server System P4308CP4MHGC View

Note: Airduct is not shown.

3.2.3 Intel® Server System P4208CP4MHGC View



A. 750-W Redundant Power Supply
B. AC Input Power Connector
C. I/O Ports
D. Alternate RMM4 Knockout
E. PCI Add-in Board Slot Covers
F. Serial Port Knockout
G. A Kensington* Cable Lock Mounting Hole
H. Padlock Loop
I. Alternate RMM4 Knockout
J. Front Control Panel
K. Hot-swap System Fan
L. 5.25" Peripheral Bays
M. Heat-sink
N. 8x3.5" Hot-swap HDD Cage
O. Intel® Server Board S2600CP4
P. EMI Cover
Q. Intel® RAID C600 Upgrade Key RKSAS8
R. PCI-e Retainer

Figure 17. Intel® Server System P4208CP4MHGC View

Note: Airduct is not shown.

4. Intel® Server Board S2600CP Functional Architecture

The architecture and design of the Intel® Server Board S2600CP is based on the Intel® Xeon E5-2600 processor, the Intel® C602 or C602J chipset, the Intel® Ethernet Controller I350 GbE controller chip, and the Server Engines* Pilot-III Server Management Controller. This chapter provides a high-level description of the functionality associated with each chipset component and the architectural blocks that make up the server boards.

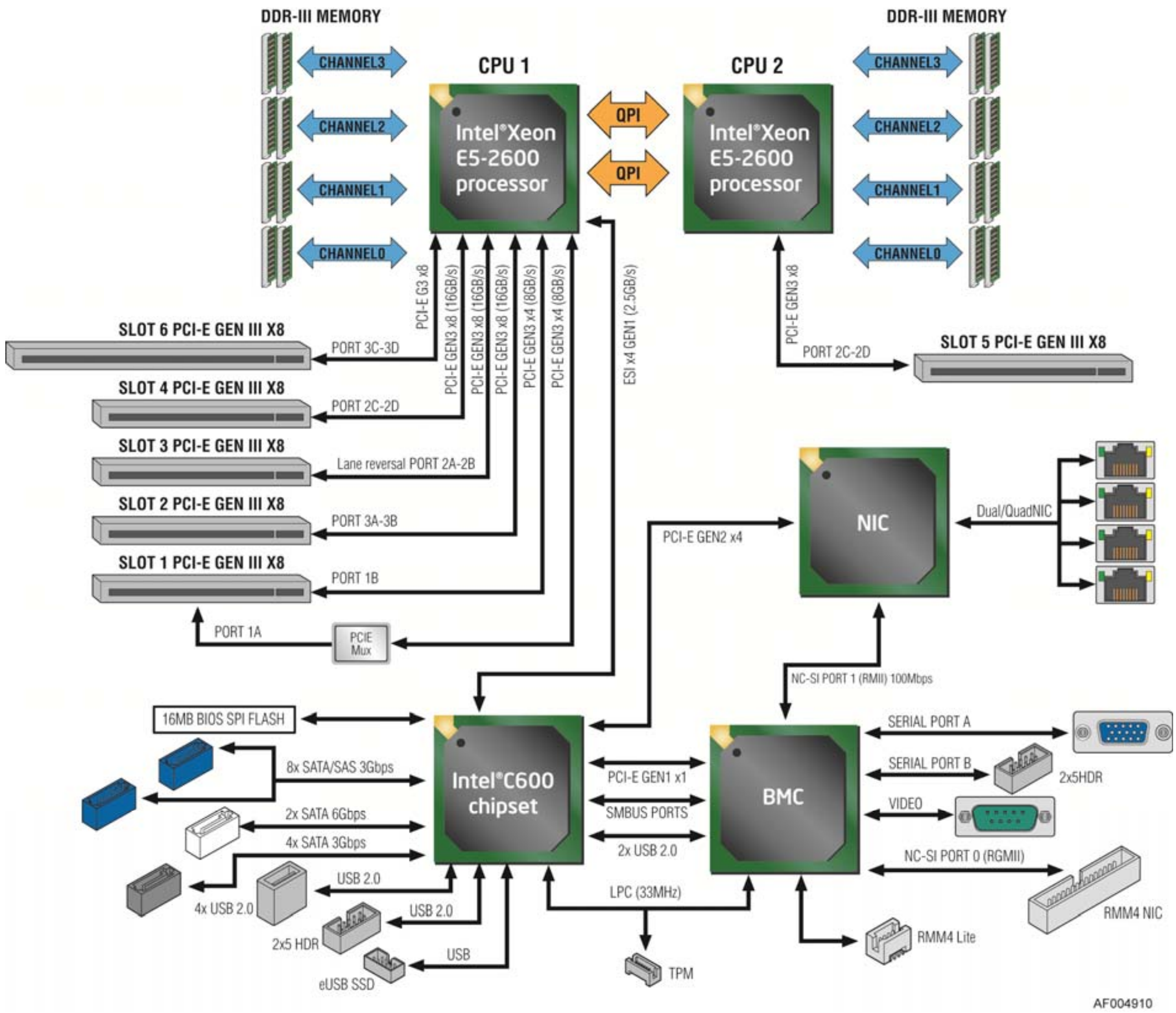


Figure 18. Intel® Server Board S2600CP2/S2600CP4 Functional Block Diagram with Intel® C602 chipset

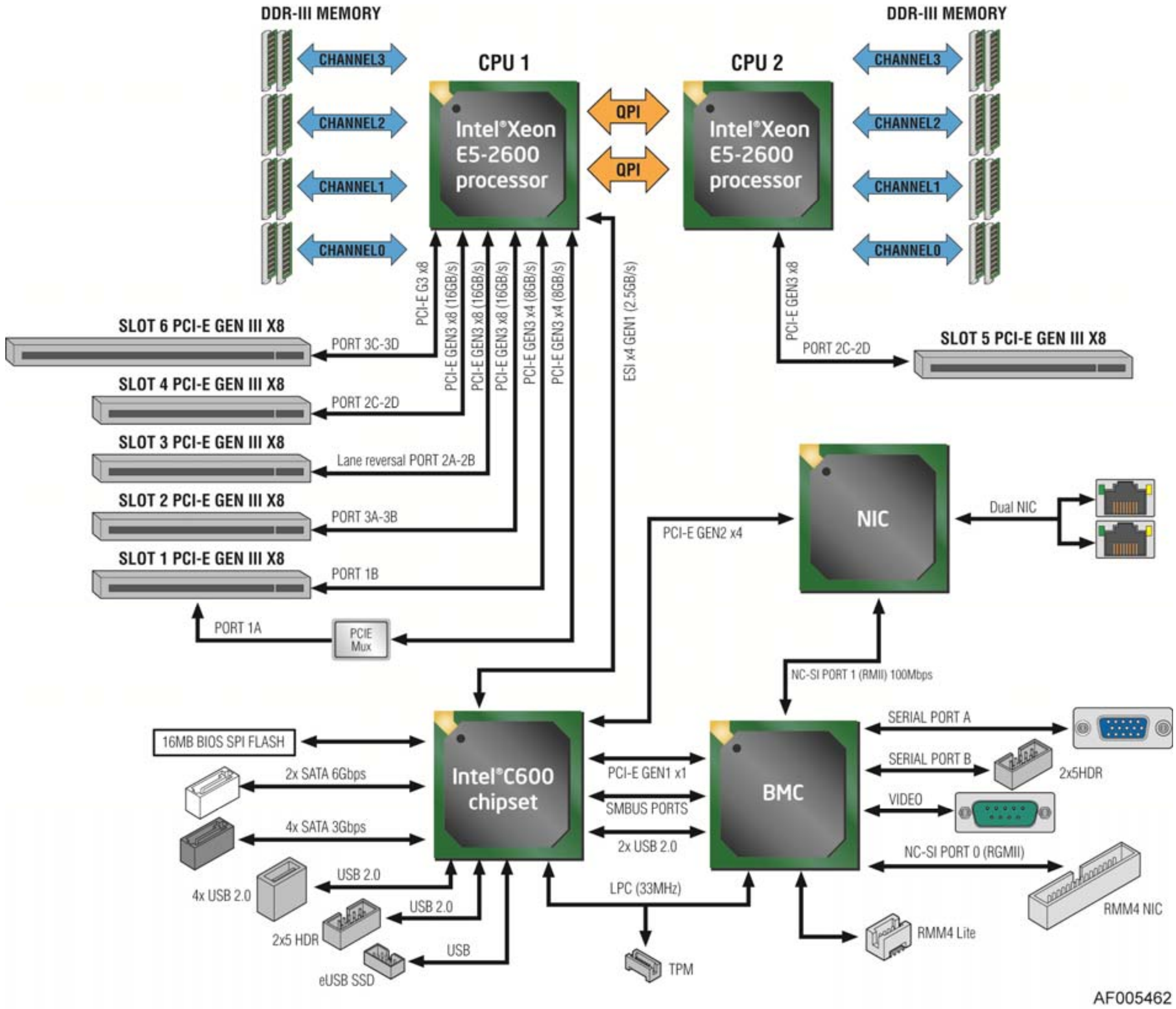


Figure 19. Intel® Server Board S2600CP2J Functional Block Diagram with Intel® C602J chipset

4.1 Processor Support

The server board includes two Socket-R (LGA2011) processor sockets and can support two processors from Intel® Xeon® processor E5-2600 product family with a Thermal Design Power (TDP) of up to 135W.

Previous generation Intel® Xeon® processors are not supported on the Intel server boards described in this document.

Visit the Intel web site for a complete list of supported processors.

4.1.1 Processor Socket Assembly

Each processor socket of the server board is pre-assembled with an Independent Latching Mechanism (ILM) and Back Plate which allow for secure placement of the processor and processor heat to the server board.

The illustration below identifies each sub-assembly component.

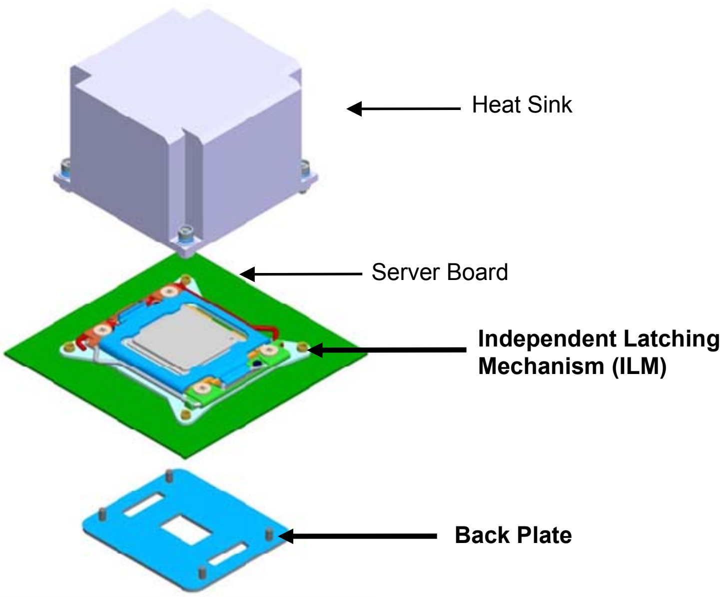


Figure 20. Processor Socket Assembly

4.1.2 Processor Population Rules

Note: Although the server board does support dual-processor configurations consisting of different processors that meet the defined criteria below, Intel does not perform validation testing of this configuration. For optimal system performance in dual-processor configurations, Intel recommends that identical processors be installed.

When using a single processor configuration, the processor must be installed into the processor socket labeled CPU1.

When two processors are installed, the following population rules apply:

- Both processors must be of the same processor family.
- Both processors must have the same number of cores
- Both processors must have the same cache sizes for all levels of processor cache memory.
- Processors with different core frequencies can be mixed in a system, given the prior rules are met. If this condition is detected, all processor core frequencies are set to the lowest common denominator (highest common speed) and an error is reported.
- Processors which have different QPI link frequencies may operate together if they are otherwise compatible and if a common link frequency can be selected. The common link frequency would be the highest link frequency that all installed processors can achieve.
- Processor stepping within a common processor family can be mixed as long as it is listed in the processor specification updates published by Intel Corporation.

The following table describes mixed processor conditions and recommended actions for all Intel® server boards and Intel server systems designed around the Intel® Xeon® processor E5-2600 product family and Intel® C600 chipset product family architecture. The errors fall into one of the following three categories:

- **Fatal**: If the system can boot, it pauses at a blank screen with the text "Unrecoverable fatal error found. System will not boot until the error is resolved" and "Press <F2> to enter setup", regardless of whether the "Post Error Pause" setup option is enabled or disabled.

  When the operator presses the <F2> key on the keyboard, the error message is displayed on the Error Manager screen, and an error is logged to the System Event Log (SEL) with the POST Error Code.

  The system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system.

  For Fatal Errors during processor initialization, the System Status LED will be set to a steady Amber color, indicating an unrecoverable system failure condition.
- **Major**: If the "Post Error Pause" setup option is enabled, the system goes directly to the Error Manager to display the error, and logs the POST Error Code to SEL. Operator intervention is required to continue booting the system.

  Otherwise, if "POST Error Pause" is disabled, the system continues to boot and no prompt is given for the error, although the Post Error Code is logged to the Error Manager and in a SEL message.
- **Minor**: The message is displayed on the screen or on the Error Manager screen, and the POST Error Code is logged to the SEL. The system continues booting in a degraded state. The user may want to replace the erroneous unit. The POST Error Pause option setting in the BIOS setup does not have any effect on this error.

Table 3. Mixed Processor Configurations

Error	Severity	System Action
Processor family not Identical	Fatal	The BIOS detects the error condition and responds as follows: ▪ Logs the POST Error Code into the System Event Log (SEL). ▪ Alerts the BMC to set the System Status LED to steady Amber. ▪ Displays "**0194: Processor family mismatch detected**" message in the Error Manager. ▪ Takes Fatal Error action (see above) and will not boot until the fault condition is remedied.
Processor model not Identical	Fatal	The BIOS detects the error condition and responds as follows: ▪ Logs the POST Error Code into the System Event Log (SEL). ▪ Alerts the BMC to set the System Status LED to steady Amber. ▪ Displays "**0196: Processor model mismatch detected**" message in the Error Manager. ▪ Takes Fatal Error action (see above) and will not boot until the fault condition is remedied.
Processor cores/threads not identical	Fatal	The BIOS detects the error condition and responds as follows: ▪ Logs the POST Error Code into the SEL. ▪ Alerts the BMC to set the System Status LED to steady Amber. ▪ Displays "**0191: Processor core/thread count mismatch detected**" message in the Error Manager. ▪ Takes Fatal Error action (see above) and will not boot until the fault condition is remedied.
Processor cache not identical	Fatal	The BIOS detects the error condition and responds as follows: ▪ Logs the POST Error Code into the SEL. ▪ Alerts the BMC to set the System Status LED to steady Amber. ▪ Displays "**0192: Processor cache size mismatch detected** message in the Error Manager. ▪ Takes Fatal Error action (see above) and will not boot until the fault condition is remedied.
Processor frequency (speed) not identical	Fatal	The BIOS detects the processor frequency difference, and responds as follows: ▪ Adjusts all processor frequencies to the highest common frequency. ▪ No error is generated – **this is not an error condition.** ▪ Continues to boot the system successfully. If the frequencies for all processors **cannot be adjusted to be the same,** then this **is** an error, and the BIOS responds as follows: ▪ Logs the POST Error Code into the SEL. ▪ Alerts the BMC to set the System Status LED to steady Amber. ▪ Does not disable the processor. ▪ Displays "**0197: Processor speeds unable to synchronize**" message in the Error Manager. ▪ Takes Fatal Error action (see above) and will not boot until the fault condition is remedied.

Error	Severity	System Action
Processor Intel® QuickPath Interconnect link frequencies not identical	Fatal	The BIOS detects the QPI link frequencies and responds as follows: ▪ Adjusts all QPI interconnect link frequencies to highest common frequency. ▪ No error is generated – **this is not an error condition.** ▪ Continues to boot the system successfully. If the link frequencies for all QPI links **cannot be adjusted to be the same,** then this **is** an error, and the BIOS responds as follows: ▪ Logs the POST Error Code into the SEL. ▪ Alerts the BMC to set the System Status LED to steady Amber. ▪ Displays "**0195: PProcessor Intel(R) QPI link frequencies unable to synchronize**" message in the Error Manager. ▪ Does not disable the processor. Takes Fatal Error action (see above) and will not boot until the fault condition is remedied.
Processor microcode update missing	Minor	The BIOS detects the error condition and responds as follows: ▪ Logs the POST Error Code into the SEL. ▪ Displays "**818x: Processor 0x microcode update not found**" message in the Error Manager or on the screen. ▪ The system continues to boot in a degraded state, regardless of the setting of POST Error Pause in the Setup.
Processor microcode update failed	Major	The BIOS detects the error condition and responds as follows: ▪ Logs the POST Error Code into the SEL. ▪ Displays "**816x: Processor 0x unable to apply microcode update**" message in the Error Manager or on the screen. ▪ Takes Major Error action. The system may continue to boot in a degraded state, depending on the setting of POST Error Pause in Setup, or may halt with the POST Error Code in the Error Manager waiting for operator intervention.

4.2 Processor Functions Overview

With the release of the Intel® Xeon® processor E5-2600 product family, several key system components, including the CPU, Integrated Memory Controller (iMC), and Integrated IO Module (IIO), have been combined into a single processor package and feature per socket; two Intel® QuickPath Interconnect point-to-point links capable of up to 8.0 GT/s, up to 40 lanes of Gen 3 PCI Express* links capable of 8.0 GT/s, and 4 lanes of DMI2/PCI Express* Gen 2 interface with a peak transfer rate of 5.0 GT/s. The processor supports up to 46 bits of physical address space and 48-bit of virtual address space.

The following sections will provide an overview of the key processor features and functions that help to define the performance and architecture of the server board.

Processor Feature Details:

- Up to 8 execution cores
- Each core supports two threads (Intel® Hyper-Threading Technology), up to 16 threads per socket
- 46-bit physical addressing and 48-bit virtual addressing
- 1 GB large page support for server applications
- A 32-KB instruction and 32-KB data first-level cache (L1) for each core
- A 256-KB shared instruction/data mid-level (L2) cache for each core
- Up to 20 MB last level cache (LLC): up to 2.5 MB per core instruction/data last level cache (LLC), shared among all cores

Supported Technologies:

- Intel® Virtualization Technology (Intel® VT)
- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® 64 Architecture
- Intel® Streaming SIMD Extensions 4.1 (Intel® SSE4.1)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Advanced Vector Extensions (Intel® AVX)
- Intel® Hyper-Threading Technology
- Execute Disable Bit
- Intel® Turbo Boost Technology
- Intel® Intelligent Power Technology
- Data Direct I/O (DDIO)
- Enhanced Intel® SpeedStep Technology

4.2.1 Intel® QuickPath Interconnect

The Intel® QuickPath Interconnect is a high speed, packetized, point-to-point interconnect used in the processor. The narrow high-speed links stitch together processors in distributed shared memory and integrated I/O platform architecture. It offers much higher bandwidth with low latency. The Intel® QuickPath Interconnect has an efficient architecture allowing more interconnect performance to be achieved in real systems. It has a snoop protocol optimized for low latency and high scalability, as well as packet and lane structures enabling quick completions of transactions. Reliability, availability, and serviceability features (RAS) are built into the architecture.

The physical connectivity of each interconnect link is made up of twenty differential signal pairs plus a differential forwarded clock. Each port supports a link pair consisting of two uni-directional links to complete the connection between two components. This supports traffic in both directions simultaneously. To facilitate flexibility and longevity, the interconnect is defined as having five layers: Physical, Link, Routing, Transport, and Protocol.

The Intel® QuickPath Interconnect includes a cache coherency protocol to keep the distributed memory and caching structures coherent during system operation. It supports both low-latency source snooping and a scalable home snoop behavior. The coherency protocol provides for direct cache-to-cache transfers for optimal latency.

4.2.2 Integrated Memory Controller (IMC) and Memory Subsystem

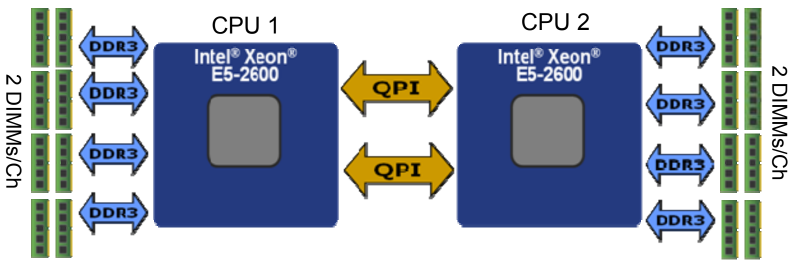


Figure 21. Memory Subsystem for Intel® Server Board S2600CP

Integrated into the processor is a memory controller. Each processor provides four DDR3 channels that support the following:

- Unbuffered DDR3 and registered DDR3 DIMMs
- LR DIMM (Load Reduced DIMM) for buffered memory solutions demanding higher capacity memory subsystems
- Independent channel mode or lockstep mode
- Data burst length of eight cycles for all memory organization modes
- Memory DDR3 data transfer rates of 800, 1066, 1333, and 1600 MT/s
- 64-bit wide channels plus 8-bits of ECC support for each channel
- DDR3 standard I/O Voltage of 1.5 V and DDR3 Low Voltage of 1.35 V
- 1-Gb, 2-Gb, and 4-Gb DDR3 DRAM technologies supported for these devices:
  - UDIMM DDR3 – SR x8 and x16 data widths, DR – x8 data width
  - RDIMM DDR3 – SR,DR, and QR – x4 and x8 data widths
  - LRDIMM DDR3 – QR – x4 and x8 data widths with direct map or with rank multiplication
- Up to 8 ranks supported per memory channel, 1, 2 or 4 ranks per DIMM
- Open with adaptive idle page close timer or closed page policy

- Per channel memory test and initialization engine can initialize DRAM to all logical zeros with valid ECC (with or without data scrambler) or a predefined test pattern
- Isochronous access support for Quality of Service (QoS)
- Minimum memory configuration: independent channel support with 1 DIMM populated
- Integrated dual SMBus master controllers
- Command launch modes of 1n/2n
- RAS Support:
  - Rank Level Sparing and Device Tagging
  - Demand and Patrol Scrubbing
  - DRAM Single Device Data Correction (SDDC) for any single x4 or x8 DRAM device. Independent channel mode supports x4 SDDC. x8 SDDC requires lockstep mode
  - Lockstep mode where channels 0 and 1 and channels 2 and 3 are operated in lockstep mode
  - Data scrambling with address to ease detection of write errors to an incorrect address.
  - Error reporting by Machine Check Architecture
  - Read Retry during CRC error handling checks by iMC
  - Channel mirroring within a socket
    - CPU1 Channel Mirror Pairs (A,B) and (C,D)
    - CPU2 Channel Mirror Pairs (E,F) and (G,H)
  - Error Containment Recovery
- Improved Thermal Throttling with dynamic Closed Loop Thermal Throttling (CLTT)
- Memory thermal monitoring support for DIMM temperature

4.2.2.1 Supported Memory

Table 4. UDIMM Support

Ranks Per DIMM and Data Width	Memory Capacity Per DIMM			Speed (MT/s) and Voltage Validated by Slot per Channel (SPC) and DIMM Per Channel (DPC)			
				Intel® Server Board S2600CP (2 Slots per Channel)			
				1DPC		2DPC	
				1.35V	1.5V	1.35V	1.5V
SRx8 Non-ECC	1GB	2GB	4GB	n/a	1066, 1333	n/a	1066, 1333
DRx8 Non-ECC	2GB	4GB	8GB	n/a	1066, 1333	n/a	1066, 1333
SRx16 Non-ECC	512MB	1GB	2GB	n/a	1066, 1333	n/a	1066, 1333
SRx8 ECC	1GB	2GB	4GB	1066, 1333	1066, 1333	1066	1066, 1333
DRx8 ECC	2GB	4GB	8GB	1066, 1333	1066, 1333	1066	1066, 1333

Table 5. RDIMM Support

Ranks Per DIMM and Data Width	Memory Capacity Per DIMM			Speed (MT/s) and Voltage Validated by Slot per Channel (SPC) and DIMM Per Channel (DPC)			
				Intel® Server Board S2600CP (2 Slots per Channel)			
				1DPC		2DPC	
				1.35V	1.5V	1.35V	1.5V
SRx8	1GB	2GB	4GB	1066, 1333	1066, 1333, 1600	1066,1333	1066, 1333, 1600
DRx8	2GB	4GB	8GB	1066, 1333	1066, 1333, 1600	1066,1333	1066, 1333, 1600
SRx4	2GB	4GB	8GB	1066, 1333	1066, 1333, 1600	1066,1333	1066, 1333, 1600
DRx4	4GB	8GB	16GB	1066, 1333	1066, 1333, 1600	1066,1333	1066, 1333, 1600
QRx4	8GB	16GB	32GB	800	1066	800	800
QRx8	4GB	8GB	16GB	800	1066	800	800

Table 6. LRDIMM Support

Ranks Per DIMM and Data Width	Memory Capacity Per DIMM		Speed (MT/s) and Voltage Validated by Slot per Channel (SPC) and DIMM Per Channel (DPC)	
			2 Slots per Channel	
			1DPC and 2DPC	
			1.35V	1.5V
QRx4 (DDP)	16GB	32GB	1066	1066, 1333
QRx8 (P)	8GB	16GB	1066	1066, 1333

4.2.2.2 Memory Population Rules

Each processor provides four banks of memory, each capable of supporting up to 2 DIMMs.

- DIMMs are organized into physical slots on DDR3 memory channels that belong to processor sockets.
- The memory channels from processor socket 1 are identified as Channel A, B, C and D. The memory channels from processor socket 2 are identified as Channel E, F, G, and H.
- The silk screened DIMM slot identifiers on the board provide information about the channel, and therefore the processor to which they belong. For example, DIMM_A1 is the first slot on Channel A on processor 1; DIMM_E1 is the first DIMM socket on Channel E on processor 2.
- The memory slots associated with a given processor are unavailable if the corresponding processor socket is not populated.
- A processor may be installed without populating the associated memory slots provided and a second processor is installed with associated memory. In this case, the memory is

shared by the processors. However, the platform suffers performance degradation and latency due to the remote memory.

- Processor sockets are self-contained and autonomous. However, all memory subsystem support (such as Memory RAS, Error Management,) in the BIOS setup is applied commonly across processor sockets.

On the Intel® Server Board S2600CP a total of 16 DIMM slots are provided (2 CPUs – 4 Channels/CPU, 2 DIMMs/Channel). The nomenclature for DIMM sockets is detailed in the following table:

Table 7. Intel® Server Board S2600CP DIMM Nomenclature

Processor Socket 1								Processor Socket 2							
(0) Channel A		(1) Channel B		(2) Channel C		(3) Channel D		(0) Channel E		(1) Channel F		(2) Channel G		(3) Channel H	
A1	**A2**	**B1**	**B2**	**C1**	**C2**	**D1**	**D2**	**E1**	**E2**	**F1**	**F2**	**G1**	**G2**	**H1**	**H2**

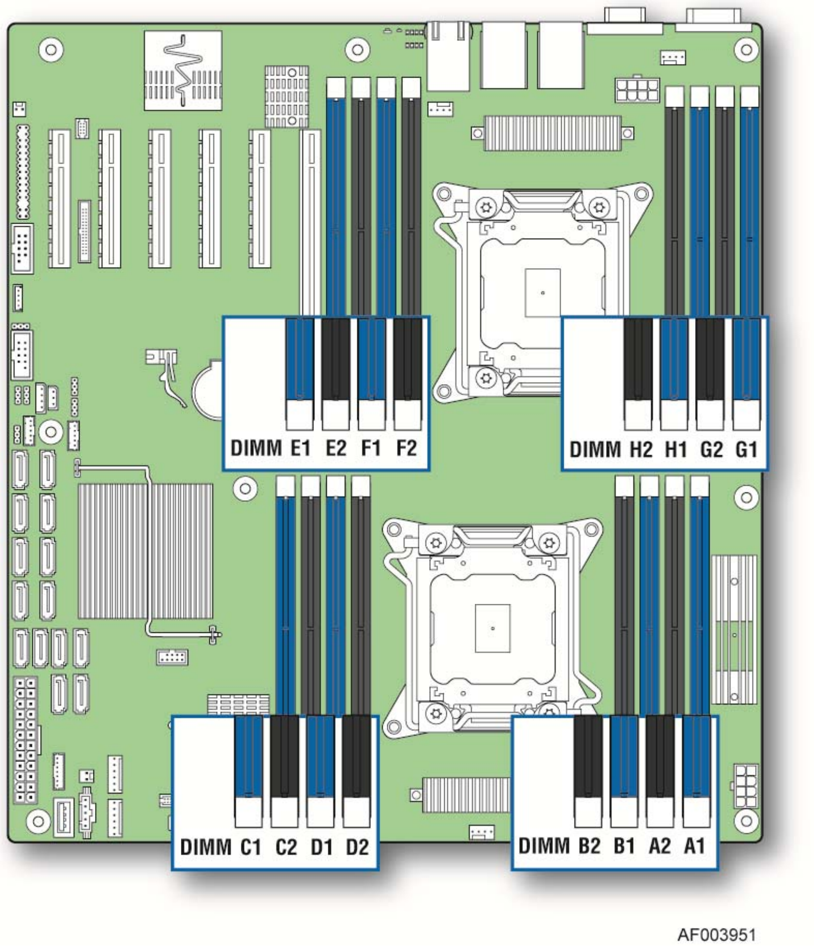


Figure 22. Intel® Server Board S2600CP DIMM Slot Layout

The following are generic DIMM population requirements that generally apply to both the Intel® Server Board S2600CP.

- DIMM slots on any memory channel must be filled following the “farthest fill first” rule.
- A maximum of 8 ranks can be installed on any one channel, counting all ranks in each DIMM on the channel.
- DIMM types (UDIMM, RDIMM, LRDIMM) must not be mixed within or across processor sockets.
- Mixing ECC with non-ECC DIMMs (UDIMMs) is not supported within or across processor sockets.
- Mixing Low Voltage (1.35V) DIMMs with Standard Voltage (1.5V) DIMMs is not supported within or across processor sockets.
- Mixing DIMMs of different frequencies and latencies is not supported within or across processor sockets.
- LRDIMM Rank Multiplication Mode and Direct Map Mode must not be mixed within or across processor sockets.
- Only ECC UDIMMs support Low Voltage 1.35V operation.
- QR RDIMMs may only be installed in DIMM Slot 1 or 2 on a channel.
- 2 DPC QR Low Voltage RDIMMs are not supported.
- In order to install 3 QR LRDIMMs on the same channel, they must be operated with Rank Multiplication as RM = 2.
- RAS Modes Lockstep, Rank Sparing, and Mirroring are mutually exclusive in this BIOS. Only one operating mode may be selected, and it will be applied to the entire system.
- If a RAS Mode has been configured, and the memory population will not support it during boot, the system will fall back to Independent Channel Mode and log and display errors
- Rank Sparing Mode is only possible when all channels that are populated with memory meet the requirement of having at least 2 SR or DR DIMM installed, or at least one QR DIMM installed, on each populated channel.
- Lockstep or Mirroring Modes require that for any channel pair that is populated with memory, the memory population on both channels of the pair must be identically sized.

4.2.2.3 Publishing System Memory

The BIOS displays the “Total Memory” of the system during POST if Quite Boot is disabled in the BIOS setup. This is the total size of memory discovered by the BIOS during POST, and is the sum of the individual sizes of installed DDR3 DIMMs in the system.

The BIOS displays the “Effective Memory” of the system in the BIOS setup. The term Effective Memory refers to the total size of all DDR3 DIMMs that are active (not disabled) and not used as redundant units.

The BIOS provides the total memory of the system in the main page of the BIOS setup. This total is the same as the amount described by the first bullet above.

If Quite Boot is disabled, the BIOS displays the total system memory on the diagnostic screen at the end of POST. This total is the same as the amount described by the first bullet above.

4.2.2.4 RAS Features

The server board supports the following memory RAS modes:

- Independent Channel Mode
- Rank Sparing Mode
- Mirrored Channel Mode
- Lockstep Channel Mode

Regardless of RAS mode, the requirements for populating within a channel given in the section 4.2.2.2 must be met at all times. Note that support of RAS modes that require matching DIMM population between channels (Mirrored and Lockstep) require that ECC DIMMs be populated. Independent Channel Mode is the only mode that supports non-ECC DIMMs in addition to ECC DIMMs.

For RAS modes that require matching populations, the same slot positions across channels must hold the same DIMM type with regards to size and organization. DIMM timings do not have to match but timings will be set to support all DIMMs populated (i.e, DIMMs with slower timings will force faster DIMMs to the slower common timing modes).

4.2.2.4.1 Independent Channel Mode

Channels can be populated in any order in Independent Channel Mode. All four channels may be populated in any order and have no matching requirements. All channels must run at the same interface frequency but individual channels may run at different DIMM timings (RAS latency, CAS Latency, and so forth).

4.2.2.4.2 Rank Sparing Mode

In Rank Sparing Mode, one rank is a spare of the other ranks on the same channel. The spare rank is held in reserve and is not available as system memory. The spare rank must have identical or larger memory capacity than all the other ranks (sparing source ranks) on the same channel. After sparing, the sparing source rank will be lost.

4.2.2.4.3 Mirrored Channel Mode

In Mirrored Channel Mode, the memory contents are mirrored between Channel 0 and Channel 2 and also between Channel 1 and Channel 3. As a result of the mirroring, the total physical memory available to the system is half of what is populated. Mirrored Channel Mode requires that Channel 0 and Channel 2, and Channel 1 and Channel 3 must be populated identically with regards to size and organization. DIMM slot populations within a channel do not have to be identical but the same DIMM slot location across Channel 0 and Channel 2 and across Channel 1 and Channel 3 must be populated the same.

4.2.2.4.4 Lockstep Channel Mode

In Lockstep Channel Mode, each memory access is a 128-bit data access that spans Channel 0 and Channel 1, and Channel 2 and Channel 3. Lockstep Channel mode is the only RAS mode that allows SDDC for x8 devices. Lockstep Channel Mode requires that Channel 0 and Channel 1, and Channel 2 and Channel 3 must be populated identically with regards to size and organization. DIMM slot populations within a channel do not have to be identical but the same DIMM slot location across Channel 0 and Channel 1 and across Channel 2 and Channel 3 must be populated the same.

4.2.3 Processor Integrated I/O Module (IIO)

The processor's integrated I/O module provides features traditionally supported through chipset components. The integrated I/O module provides the following features:

4.2.3.1.1 PCI Express Interfaces

The integrated I/O module incorporates the PCI Express interface and supports up to 40 lanes of PCI Express. Intel® Server Board S2600CP supports 6 PCI-e slots from two processors:

- From first processor:
  - Slot 1: PCIe Gen III x4/x8 electrical with x8 physical connector
  - Slot 2: PCIe Gen III x8 electrical with x8 physical connector
  - Slot 3: PCIe Gen III x8 electrical with x8 open-ended physical connector
  - Slot 4: PCIe Gen III x8 electrical with x8 physical connector
  - Slot 6: PCIe Gen III x8 electrical with x16 connector, support riser card.
- From second processor:
  - Slot 5: PCIe Gen III x8 electrical with x8 open-ended physical connector

Note: PCIe slot 5 is functional only when the second processor is installed.

4.2.3.1.2 DMI2 Interface to the PCH

The platform requires an interface to the legacy Southbridge (PCH) which provides basic, legacy functions required for the server platform and operating systems. Since only one PCH is required and allowed for the system, any sockets which do not connect to PCH would use this port as a standard x4 PCI Express 2.0 interface.

4.2.3.1.3 Integrated IOAPIC

Provides support for PCI Express devices implementing legacy interrupt messages without interrupt sharing.

4.2.3.1.4 Intel® QuickData Technology

Used for efficient, high bandwidth data movement between two locations in memory or from memory to I/O.

4.3 Intel® C600 Chipset Functional Overview

The following sub-sections will provide an overview of the key features and functions of the Intel® C600-A chipset used on the server board.

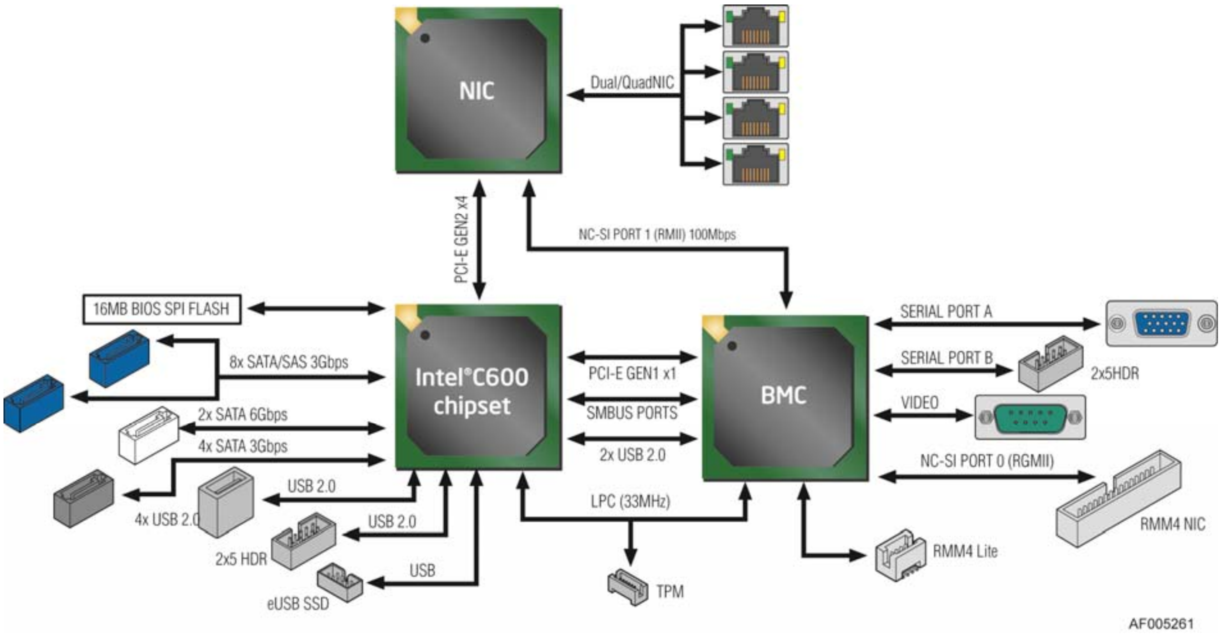


Figure 23. Intel® Server Board S2600CP2/S2600CP4 Chipset Functional Block Diagram

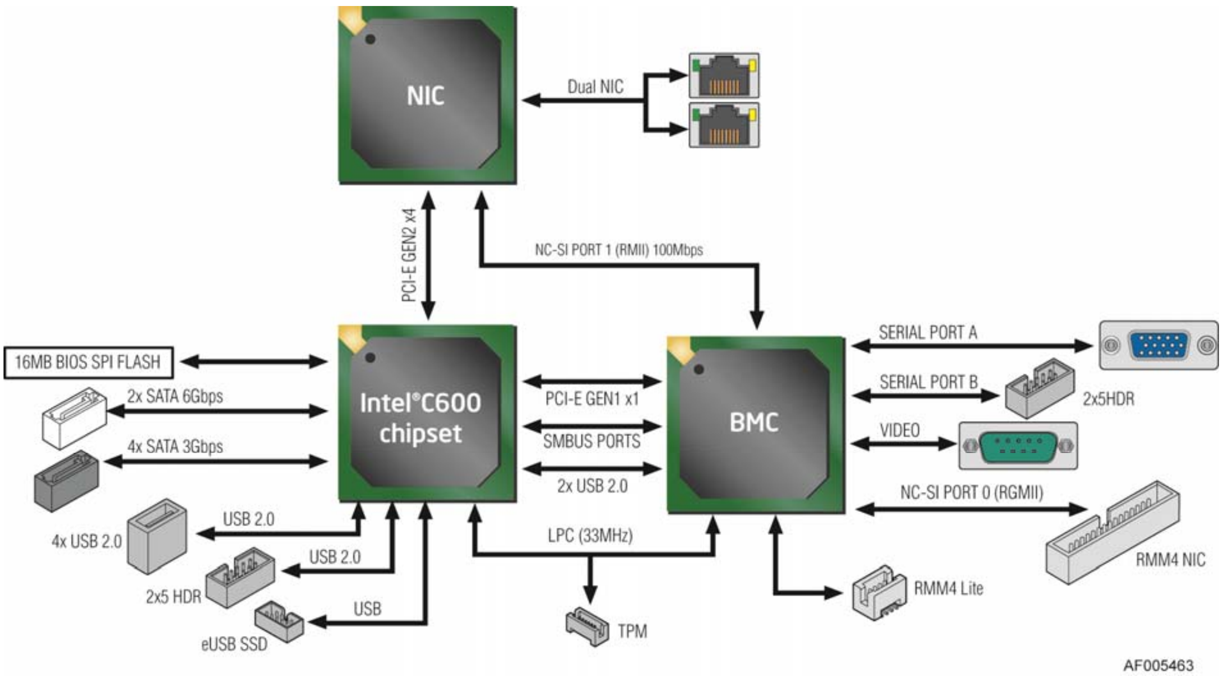


Figure 24. Intel® Server Board S2600CP2J Chipset Functional Block Diagram

The Intel® C600 chipset in the Intel® Server Board S2600CP provide a connection point between various I/O components and Intel® Xeon E5-2600 processors, which includes the following core platform functions:

- Digital Media Interface (DMI)
- PCI Express* Interface
- Serial ATA (SATA) Controller
- Serial Attached SCSI (SAS)/SATA Controller (S2600CP2/S2600CP4 only)
- AHCI
- Rapid Storage Technology
- PCI Interface
- Low Pin Count (LPC) Interface
- Serial Peripheral Interface (SPI)
- Compatibility Modules (DMA Controller, Timer/Counters, Interrupt Controller)
- Advanced Programmable Interrupt Controller (APIC)
- Universal Serial Bus (USB) Controllers
- Gigabit Ethernet Controller
- RTC
- GPIO
- Enhanced Power Management
- Intel® Active Management Technology (Intel® AMT)
- Manageability
- System Management Bus (SMBus 2.0)
- Virtualization Technology for Directed I/O (Intel® VT-d)
- KVM/Serial Over LAN (SOL) Function

4.3.1 Digital Media Interface (DMI)

Digital Media Interface (DMI) is the chip-to-chip connection between the processor and C600 chipset. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software-transparent, permitting current and legacy software to operate normally.

4.3.2 PCI Express* Interface

The C600 chipset provides up to 8 PCI Express Root Ports, supporting the PCI Express Base Specification, Revision 2.0. Each Root Port x1 lane supports up to 5 Gb/s bandwidth in each direction (10 Gb/s concurrent). PCI Express Root Ports 1-4 or Ports 5-8 can independently be configured to support four x1s, two x2s, one x2 and two x1s, or one x4 port widths.

4.3.3 Serial ATA (SATA) Controller

The C600 chipset has two integrated SATA host controllers that support independent DMA operation on up to six ports and supports data transfer rates of up to 6.0 Gb/s (600 MB/s) on up to two ports (Port 0 and 1 Only) while all ports support rates up to 3.0 Gb/s (300 MB/s) and up to 1.5 Gb/s (150 MB/s). The SATA controller contains two modes of operation – a legacy mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities.

Note: When connecting the four SATA 3G ports to backplanes, the SATA SGPIO cable needs to be properly connected in order to enable the LED indicator for the drives. The two SATA 6G ports do not have SGPIO signal routed, the LED indicator will not light up if connecting the ports to backplane. The ports can be used for ODD devices.

4.3.4 Serial Attached SCSI (SAS)/SATA Controller

On Intel® Server Board S2600CP2/S2600CP4, the C600 chipset supports up to 8 SAS ports support rates up to 3.0 Gb/s. Please refer to section “On-board SAS/SATA Support and Options” for detail information of the port features with C600 upgrade keys. The feature is not available on Intel® Server Board S2600CP2J

4.3.5 AHCI

The C600 chipset provides hardware support for Advanced Host Controller Interface (AHCI), a standardized programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features. AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (for example, an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

4.3.6 PCI Interface

The C600 chipset PCI interface provides a 33 MHz, Revision 2.3 implementation. The C600 chipset integrates a PCI arbiter that supports up to four external PCI bus masters in addition to the internal C600 chipset requests. This allows for combinations of up to four PCI down devices and PCI slots.

4.3.7 Low Pin Count (LPC) Interface

The C600 chipset implements an LPC Interface as described in the LPC 1.1 Specification. The Low Pin Count (LPC) bridge function of the C600 resides in PCI Device 31: Function 0. In addition to the LPC bridge interface function, D31:F0 contains other functional units including DMA, interrupt controllers, timers, power management, system management, GPIO, and RTC.

4.3.8 Serial Peripheral Interface (SPI)

The C600 chipset implements an SPI Interface as an alternative interface for the BIOS flash device. The SPI flash is required to support Gigabit Ethernet and Intel® Active Management Technology. The C600 chipset supports up to two SPI flash devices with speeds up to 50 MHz.

4.3.9 Compatibility Modules (DMA Controller, Timer/Counters, Interrupt Controller)

The DMA controller incorporates the logic of two 82C37 DMA controllers, with seven independently programmable channels. The C600 chipset supports LPC DMA through the C600 chipset’s DMA controller.

The timer/counter block contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. These three counters are combined to provide the system timer function, and speaker tone.

The C600 chipset provides an ISA-Compatible Programmable Interrupt Controller (PIC) that incorporates the functionality of two 82C59 interrupt controllers. In addition, the C600 chipset supports a serial interrupt scheme.

All of the registers in these modules can be read and restored. This is required to save and restore system state after power has been removed and restored to the platform.

4.3.10 Advanced Programmable Interrupt Controller (APIC)

In addition to the standard ISA compatible Programmable Interrupt controller (PIC) described in the previous section, the C600 incorporates the Advanced Programmable Interrupt Controller (APIC).

4.3.11 Universal Serial Bus (USB) Controllers

The C600 chipset has up to two Enhanced Host Controller Interface (EHCI) host controllers that support USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480 Mb/s which is 40 times faster than full-speed USB. The C600 chipset supports up to fourteen USB 2.0 ports. All fourteen ports are high-speed, full-speed, and low-speed capable.

4.3.12 Gigabit Ethernet Controller

The Gigabit Ethernet Controller provides a system interface using a PCI function. The controller provides a full memory-mapped or IO mapped interface along with a 64 bit address master support for systems using more than 4 GB of physical memory and DMA (Direct Memory Addressing) mechanisms for high performance data transfers. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor. Two large configurable transmit and receive FIFOs (up to 20 KB each) help prevent data underruns and overruns while waiting for bus accesses. This enables the integrated LAN controller to transmit data with minimum inter-frame spacing (IFS).

The LAN controller can operate at multiple speeds (10/100/1000 MB/s) and in either full duplex or half duplex mode. In full duplex mode the LAN controller adheres with the IEEE 802.3x Flow Control Specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

4.3.13 RTC

The C600 chipset contains a real-time clock with 256 bytes of battery-backed RAM. The real-time clock performs two key functions: keeping track of the time of day and storing system data. The RTC operates on a 32.768 KHz crystal and a 3 V battery.

4.3.14 GPIO

Various general purpose inputs and outputs are provided for custom system design. The number of inputs and outputs varies depending on the C600 chipset configuration.

4.3.15 Enhanced Power Management

The C600 chipset's power management functions include enhanced clock control and various low-power (suspend) states. A hardware-based thermal management circuit permits software-independent entrance to low-power states. The C600 chipset contains full support for the Advanced Configuration and Power Interface (ACPI) Specification, Revision 4.0a.

4.3.16 Manageability

The C600 chipset integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

4.3.17 System Management Bus (SMBus 2.0)

The C600 chipset contains a SMBus Host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I2C devices. Special I2C commands are implemented.

The C600 chipset's SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). Also, the C600 chipset supports slave functionality, including the Host Notify protocol. Hence, the host controller supports eight command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification*, Version 2.0): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify.

The C600 chipset's SMBus also implements hardware-based Packet Error Checking for data robustness and the Address Resolution Protocol (ARP) to dynamically provide address to all SMBus devices.

4.3.18 Virtualization Technology for Directed I/O (Intel® VT-d)

The C600 chipset provides hardware support for implementation of Intel® Virtualization Technology with Directed I/O (Intel® VT-d). Intel VT-d consists of technology components that support the virtualization of platforms based on Intel® Architecture Processors. Intel VT-d Technology enables multiple operating systems and applications to run in independent partitions. A partition behaves like a virtual machine (VM) and provides isolation and protection across partitions. Each partition is allocated its own subset of host physical memory.

4.3.19 KVM/Serial Over LAN (SOL) Function

These functions support redirection of keyboard, mouse, and text screen to a terminal window on a remote console. The keyboard, mouse, and text redirection enables the control of the client machine through the network. Text, mouse, and keyboard redirection allows the remote machine to control and configure the client by entering BIOS setup. The KVM/SOL function emulates a standard PCI serial port and redirects the data from the serial port to the management console using LAN. KVM has additional requirements of internal graphics and SOL may be used when KVM is not supported.

4.3.20 On-board SAS/SATA Support and Options

The Intel® C600 chipset on Intel® Server Board S2600CP2/S2600CP4 provides storage support by two integrated controllers: AHCI and SCU. By default the server board will support up to 10 SATA ports: Two white 6Gb/sec SATA ports and four black 3Gb/sec SATA ports routed from the AHCI controller labeled as “SATA_0” through “SATA_5” and eight blue 3Gb/sec SATA/SAS ports routed from the SCU controller labeled as “SAS_0” through “SAS_7”. On Intel® Server Board S2600CP2J, only 6 SATA ports from ACHI controller are available.

Note: The four blue ports from SCU labeled as "SAS_4"~"SAS_7" are NOT functional by default and is only enabled with the addition of an Intel® RAID C600 Upgrade Key option supporting 8 SAS/SATA ports.

The server board is capable of supporting additional chipset embedded SAS and RAID options from the SCU controller when configured with one of several available Intel® RAID C600 Upgrade Keys. Upgrade keys install onto a 4-pin connector on the server board labeled as "Storage Upgrade key". The following table identifies available upgrade key options and their supported features. The Intel® RAID C600 Upgrade Keys do NOT work on Intel® Server Board S2600CP2J.

Table 8. Intel® RAID C600 Upgrade Key Options

Intel® RAID C600 Upgrade Key Options (Intel Product Codes)	Key Color	Description
Default – No option key installed	N/A	4 Port SATA with Intel® ESRT RAID 0,1,10 and Intel® RSTe RAID 0,1,5,10
RKSATA4R5	Black	4 Port SATA with Intel® ESRT2 RAID 0,1, **5**, 10 and Intel® RSTe RAID 0,1,5,10
RKSATA8	Blue	8 Port SATA with Intel® ESRT2 RAID 0,1, 10 and Intel® RSTe RAID 0,1,5,10
RKSATA8R5	White	8 Port SATA with Intel® ESRT2 RAID 0,1, **5**, 10 and Intel® RSTe RAID 0,1,5,10
RKSAS4	Green	4 Port SAS with Intel® ESRT2 RAID 0,1, 10 and Intel® RSTe RAID 0,1,10
RKSAS4R5	Yellow	4 Port SAS with Intel® ESRT2 RAID 0,1, **5**, 10 and Intel® RSTe RAID 0,1,10
RKSAS8	Orange	8 Port SAS with Intel® ESRT2 RAID 0,1, 10 and Intel® RSTe RAID 0,1,10
RKSAS8R5	Purple	8 Port SAS with Intel® ESRT2 RAID 0,1, **5**, 10 and Intel® RSTe RAID 0,1,10

Additional information for the on-board RAID features and functionality can be found in the *Intel® RAID Software Users Guide* (Intel Document Number D29305-015).

The storage ports from SCU can be configured with the two embedded software RAID options:
- Intel® Embedded Server RAID Technology 2 (ESRT2) based on LSI* MegaRAID SW RAID technology supporting RAID levels 0, 1, and 10.
- Intel® Rapid Storage Technology (RSTe) supporting RAID levels 0, 1, 5, and 10.

4.3.20.1 Intel® Embedded Server RAID Technology 2 (ESRT2)

Features of the embedded software RAID option Intel® Embedded Server RAID Technology 2 (ESRT2) include the following:

- Based on LSI* MegaRAID Software Stack
- Software RAID with system providing memory and CPU utilization
- Supported RAID Levels – 0,1,5,10
    - 4 and 8 Port SATA RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key

- o 4 and 8 Port SAS RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key
- Maximum drive support = 8 (with or without SAS expander option installed)

4.3.20.2 Intel® Rapid Storage Technology (RSTe)

Features of the embedded software RAID option Intel® Rapid Storage Technology (RSTe) include the following:

- Software RAID with system providing memory and CPU utilization
- Supported RAID Levels – 0,1,5,10
  - o 4 Port SATA RAID 5 available standard (no option key required)
  - o 8 Port SATA RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key
  - o No SAS RAID 5 support
- Maximum drive support = 32 (in arrays with 8 port SAS), 16 (in arrays with 4 port SAS), 128 (JBOD)

Note: No boot drive support to targets attached through SAS expander card

4.4 PCI Subsystem

The primary I/O buses for the Intel® Server Board S2600CP are PCI Express* Gen3 with six independent PCI bus segments. The following tables list the characteristics of the PCI bus segments.

Table 9. Intel® Server Board S2600CP PCI Bus Segment Characteristics

Voltage	Width	Speed	Type	PCI I/O Card Slots
3.3 V	X4 or x8 (with mux)	8 GB/S or 16 GB/S	PCI Express* Gen3	X4 or x8 (with mux) PCI Express* Gen3 throughput to Slot1 (x8 mechanically)
3.3 V	x8	16 GB/S	PCI Express* Gen3	x8 PCI Express* Gen3 throughput to Slot 2 (x8 mechanically)
3.3 V	x8	16 GB/S	PCI Express* Gen3	x8 PCI Express* Gen3 throughput to Slot 3 (x8 mechanically, open end connector)
3.3 V	x8	16 GB/S	PCI Express* Gen3	x8 PCI Express* Gen3 throughput to Slot 4 (x8 mechanically)
3.3 V	x8	16 GB/S	PCI Express* Gen3	x8 PCI Express* Gen3 throughput to Slot 5 (x8 mechanically, open end connector), from CPU2
3.3 V	x8	16 GB/S	PCI Express* Gen3	x8 PCI Express* Gen3 throughput to Slot 6 (x16 mechanically)

The following diagram shows the PCI layout for Intel® Server Board S2600CP4:

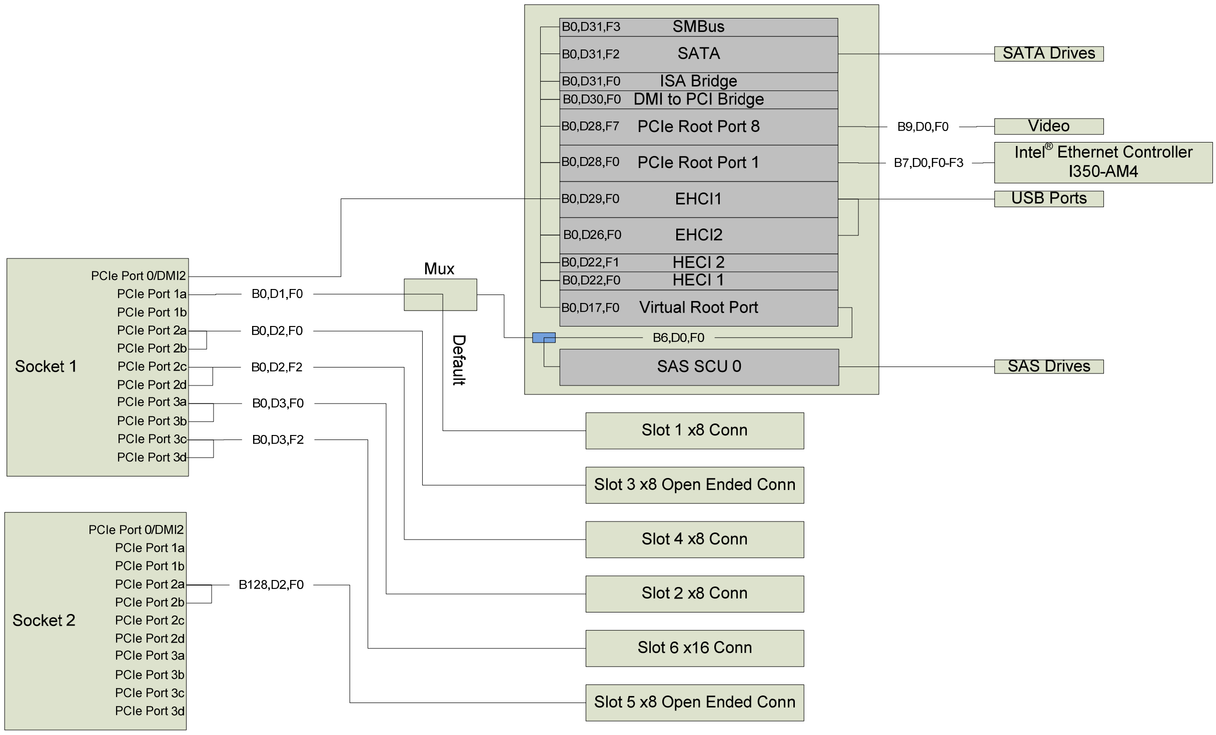


Figure 25. PCI Layout Diagram

4.5 Integrated Baseboard Management Controller Overview

The server board utilizes the I/O controller, Graphics Controller, and Baseboard Management features of the Emulex* Pilot-III Management Controller. The following is an overview of the features as implemented on the server board from each embedded controller.

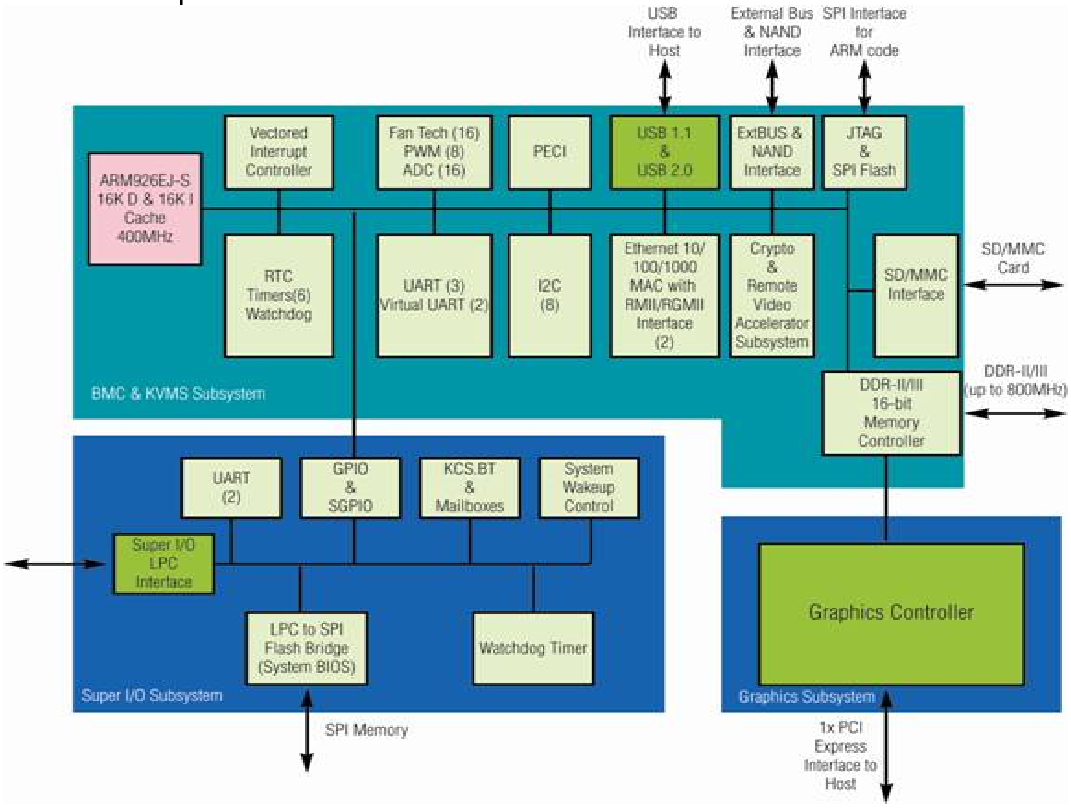


Figure 26. Integrated BMC Functional Block Diagram

4.5.1 Super I/O Controller

The integrated super I/O controller provides support for the following features as implemented on the server board:

- Two Fully Functional Serial Ports, compatible with the 16C550
- Serial IRQ Support
- Up to 16 Shared direct GPIO's
- Serial GPIO support for 80 general purpose inputs and 80 general purpose outputs available for host processor
- Programmable Wake-up Event Support
- Plug and Play Register Set
- Power Supply Control
- Host SPI bridge for system BIOS support

4.5.1.1 Keyboard and Mouse Support

The server board does not support PS/2 interface keyboards and mice. However, the system BIOS recognizes USB specification-compliant keyboard and mice.

4.5.1.2 Wake-up Control

The super I/O contains functionality that allows various events to power on and power off the system.

4.5.2 Graphics Controller and Video Support

The integrated graphics controller provides support for the following features as implemented on the server board:

- Integrated Graphics Core with 2D Hardware accelerator
- DDR-3 memory interface with 16 MB of memory allocated and reported for graphics memory
- High speed Integrated 24-bit RAMDAC
- Single lane PCI-Express host interface running at Gen 1 speed

The integrated video controller supports all standard IBM VGA modes. The following table shows the 2D modes supported for both CRT and LCD:

Table 10. Video Modes

2D Mode	2D Video Mode Support			
	8 bpp	16 bpp	24 bpp	32 bpp
640x480	X	X	X	X
800x600	X	X	X	X
1024x768	X	X	X	X
1152x864	X	X	X	X
1280x1024	X	X	X	X
1600x1200**	X	X		

** Video resolutions at 1600x1200 and higher are only supported through the external video connector located on the rear I/O section of the server board. Utilizing the optional front panel video connector may result in lower video resolutions.

The BIOS supports dual-video mode when an add-in video card is installed.

- In the single mode (dual monitor video = disabled), the on-board video controller is disabled when an add-in video card is detected.

In the dual mode (on-board video = enabled, dual monitor video = enabled), the on-board video controller is enabled and is the primary video device. The add-in video card is allocated resources and is considered the secondary video device. The BIOS Setup utility provides options to configure the feature as follows:

Table 11. Video mode

On-board Video	**Enabled** Disabled	
Dual Monitor Video	**Enabled** Disabled	Shaded if on-board video is set to "Disabled"

4.5.3 Baseboard Management Controller

The server board utilizes the following features of the embedded baseboard management controller.

- IPMI 2.0 Compliant
- 400MHz 32-bit ARM9 processor with memory management unit (MMU)
- Two independent10/100/1000 Ethernet Controllers with RMII/RGMII support
- DDR2/3 16-bit interface with up to 800 MHz operation
- 12 10-bit ADCs
- Sixteen fan tachometers
- Eight Pulse Width Modulators (PWM)
- Chassis intrusion logic
- JTAG Master
- Eight I2C interfaces with master-slave and SMBus timeout support. All interfaces are SMBus 2.0 compliant.
- Parallel general-purpose I/O Ports (16 direct, 32 shared)
- Serial general-purpose I/O Ports (80 in and 80 out)
- Three UARTs
- Platform Environmental Control Interface (PECI)
- Six general-purpose timers
- Interrupt controller
- Multiple SPI flash interfaces
- NAND/Memory interface
- Sixteen mailbox registers for communication between the BMC and host
- LPC ROM interface
- BMC watchdog timer capability
- SD/MMC card controller with DMA support
- LED support with programmable blink rate controls on GPIOs
- Port 80h snooping capability
- Secondary Service Processor (SSP), which provides the HW capability of off-loading time critical processing tasks from the main ARM core.

4.5.3.1 Remote Keyboard, Video, Mouse, and Storage (KVMS) Support

- USB 2.0 interface for Keyboard, Mouse and Remote storage such as CD/DVD ROM and floppy
- USB 1.1/USB 2.0 interface for PS2 to USB bridging, remote Keyboard and Mouse
- Hardware Based Video Compression and Redirection Logic
- Supports both text and Graphics redirection
- Hardware assisted Video redirection using the Frame Processing Engine
- Direct interface to the Integrated Graphics Controller registers and Frame buffer
- Hardware-based encryption engine

4.5.3.2 Integrated BMC Embedded LAN Channel

The Integrated BMC hardware includes two dedicated 10/100 network interfaces. These interfaces are not shared with the host system. At any time, only one dedicated interface may be enabled for management traffic. The default active interface is the NIC 1 port.

For these channels, support can be enabled for IPMI-over-LAN and DHCP. For security reasons, embedded LAN channels have the following default settings:

- IP Address: Static.
- All users disabled.

For a functional overview of the baseboard management features, refer to Chapter 5 – Platform Management Overview.

4.6 Network Interface

The Intel® Server Board S2600CP has a Intel® Ethernet Controller I350 (“Powerville”) GbE Controller providing up to four 10/100/1000 Mb Ethernet ports. The controller is a fully integrated MAC/PHY in a single low power package that supports quad-port and dual-port Gb Ethernet designs. The device offers up to four fully integrated GbE media access control (MAC), physical layer (PHY) ports, and up to four SGMII/SerDes ports that can be connected to an external PHY.

The controller supports PCI Express* PCIe v2.0 (5GT/s and 2.5GT/s). The controller enables four-port or two-port 1000BASE-T implementations using integrated PHY’s. The controller supports VMDq, SR-IOV, EEE, and DMA Coalescing.

Each Ethernet port drives two LEDs located on each network interface connector. The LED at the right of the connector is the link/activity LED and indicates network connection when on, and transmit/receive activity when blinking. The LED at the left of the connector indicates link speed as defined in the following table.

Table 12. External RJ45 NIC Port LED Definition

LED Color	LED State	NIC State
Green/Amber (Right)	Off	10 Mbps
	Amber	100 Mbps
	Green	1000 Mbps
Green (Left)	On	Active Connection
	Blinking	Transmit/Receive activity

5. System Security

5.1 BIOS Password Protection

The BIOS uses passwords to prevent unauthorized tampering with the server setup. Passwords can restrict entry to the BIOS Setup, restrict use of the Boot Popup menu, and suppress automatic USB device reordering.
There is also an option to require a Power On password entry in order to boot the system. If the Power On Password function is enabled in Setup, the BIOS will halt early in POST to request a password before continuing POST.

Both Administrator and User passwords are supported by the BIOS. An Administrator password must be installed in order to set the User password. The maximum length of a password is 14 characters. A password can have alphanumeric (a-z, A-Z, 0-9) characters and it is case sensitive. Certain special characters are also allowed, from the following set:

! @ # $ % ^ & * ( ) - _ + = ?

The Administrator and User passwords must be different from each other. An error message will be displayed if there is an attempt to enter the same password for one as for the other.
The use of “Strong Passwords” is encouraged, but not required. In order to meet the criteria for a “Strong Password”, the password entered must be at least 8 characters in length, and must include at least one each of alphabetic, numeric, and special characters. If a “weak” password is entered, a popup warning message will be displayed, although the weak password will be accepted.

Once set, a password can be cleared by changing it to a null string. This requires the Administrator password, and must be done through BIOS Setup or other explicit means of changing the passwords. Clearing the Administrator password will also clear the User password.

Alternatively, the passwords can be cleared by using the Password Clear jumper if necessary. Resetting the BIOS configuration settings to default values (by any method) has no effect on the Administrator and User passwords.

Entering the User password allows the user to modify only the System Time and System Date in the Setup Main screen. Other setup fields can be modified only if the Administrator password has been entered. If any password is set, a password is required to enter the BIOS setup.

The Administrator has control over all fields in the BIOS setup, including the ability to clear the User password and the Administrator password.

It is strongly recommended that at least an Administrator Password be set, since not having set a password gives everyone who boots the system the equivalent of Administrative access. Unless an Administrator password is installed, any User can go into Setup and change BIOS settings at will.

In addition to restricting access to most Setup fields to viewing only when a User password is entered, defining a User password imposes restrictions on booting the system. In order to simply boot in the defined boot order, no password is required. However, the F6 Boot popup prompts for a password, and can only be used with the Administrator password. Also, when a User password is defined, it suppresses the USB Reordering that occurs, if enabled, when a new USB boot device is attached to the system. A User is restricted from booting in anything other than the Boot Order defined in the Setup by an Administrator.

As a security measure, if a User or Administrator enters an incorrect password three times in a row during the boot sequence, the system is placed into a halt state. A system reset is required to exit out of the halt state. This feature makes it more difficult to guess or break a password.

In addition, on the next successful reboot, the Error Manager displays a Major Error code 0048, which also logs a SEL event to alert the authorized user or administrator that a password access failure has occurred

5.2 Trusted Platform Module (TPM) Support

The Trusted Platform Module (TPM) option is a hardware-based security device that addresses the growing concern on boot process integrity and offers better data protection. TPM protects the system start-up process by ensuring it is tamper-free before releasing system control to the operating system. A TPM device provides secured storage to store data, such as security keys and passwords. In addition, a TPM device has encryption and hash functions. The server board implements TPM as per *TPM PC Client Specifications* revision 1.2 by the Trusted Computing Group (TCG).

A TPM device is optionally installed onto a high density 14-pin connector labeled “TPM” on the server board, and is secured from external software attacks and physical theft. A pre-boot environment, such as the BIOS and operating system loader, uses the TPM to collect and store unique measurements from multiple factors within the boot process to create a system fingerprint. This unique fingerprint remains the same unless the pre-boot environment is tampered with. Therefore, it is used to compare to future measurements to verify the integrity of the boot process.

After the system BIOS completes the measurement of its boot process, it hands off control to the operating system loader and in turn to the operating system. If the operating system is TPM-enabled, it compares the BIOS TPM measurements to those of previous boots to make sure the system was not tampered with before continuing the operating system boot process. Once the operating system is in operation, it optionally uses TPM to provide additional system and data security (for example, Microsoft Vista* supports Bitlocker drive encryption).

5.2.1 TPM security BIOS

The BIOS TPM support conforms to the *TPM PC Client Implementation Specification* for Conventional BIOS and to the *TPM Interface Specification,* and the *Microsoft Windows BitLocker* Requirements*. The role of the BIOS for TPM security includes the following:

- Measures and stores the boot process in the TPM microcontroller to allow a TPM enabled operating system to verify system boot integrity.
- Produces EFI and legacy interfaces to a TPM-enabled operating system for using TPM.
- Produces ACPI TPM device and methods to allow a TPM-enabled operating system to send TPM administrative command requests to the BIOS.
- Verifies operator physical presence. Confirms and executes operating system TPM administrative command requests.

- Provides BIOS Setup options to change TPM security states and to clear TPM ownership.

For additional details, refer to the *TCG PC Client Specific Implementation Specification*, the *TCG PC Client Specific Physical Presence Interface Specification*, and the *Microsoft BitLocker* Requirement* documents.

5.2.2 Physical Presence

Administrative operations to the TPM require TPM ownership or physical presence indication by the operator to confirm the execution of administrative operations. The BIOS implements the operator presence indication by verifying the setup Administrator password.

A TPM administrative sequence invoked from the operating system proceeds as follows:

1. User makes a TPM administrative request through the operating system's security software.
2. The operating system requests the BIOS to execute the TPM administrative command through TPM ACPI methods and then resets the system.
3. The BIOS verifies the physical presence and confirms the command with the operator.
4. The BIOS executes TPM administrative command(s), inhibits BIOS Setup entry and boots directly to the operating system which requested the TPM command(s).

5.2.3 TPM Security Setup Options

The BIOS TPM Setup allows the operator to view the current TPM state and to carry out rudimentary TPM administrative operations. Performing TPM administrative options through the BIOS setup requires TPM physical presence verification.

Using BIOS TPM Setup, the operator can turn ON or OFF TPM functionality and clear the TPM ownership contents. After the requested TPM BIOS Setup operation is carried out, the option reverts to No Operation.

The BIOS TPM Setup also displays the current state of the TPM, whether TPM is enabled or disabled and activated or deactivated. Note that while using TPM, a TPM-enabled operating system or application may change the TPM state independent of the BIOS setup. When an operating system modifies the TPM state, the BIOS Setup displays the updated TPM state.

The BIOS Setup TPM Clear option allows the operator to clear the TPM ownership key and allows the operator to take control of the system with TPM. You use this option to clear security settings for a newly initialized system or to clear a system for which the TPM ownership security key was lost.

5.2.3.1 Security Screen

To enter the BIOS Setup, press the F2 function key during boot time when the OEM or Intel logo displays. The following message displays on the diagnostics screen and under the Quiet Boot logo screen:

```
Press <F2> to enter setup
```

When the Setup is entered, the Main screen displays. The BIOS Setup utility provides the Security screen to enable and set the user and administrative passwords and to lock out the front panel buttons so they cannot be used. The Intel® Server Board S2600CP provides TPM settings through the security screen.

To access this screen from the Main screen, select the **Security** option.

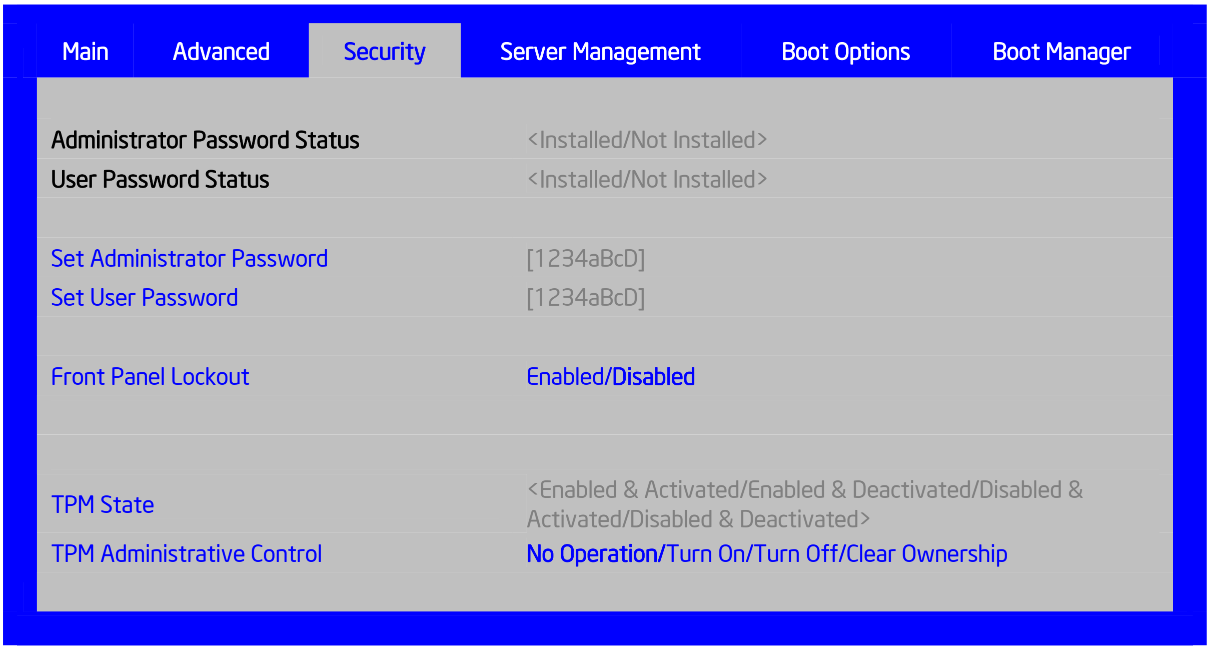


Figure 27. Setup Utility – TPM Configuration Screen

Table 13. TSetup Utility – Security Configuration Screen Fields

Setup Item	Options	Help Text	Comments
TPM State*	Enabled and Activated Enabled and Deactivated Disabled and Activated Disabled and Deactivated		**Information only**. Shows the current TPM device state. A disabled TPM device will not execute commands that use TPM functions and TPM security operations will not be available. An enabled and deactivated TPM is in the same state as a disabled TPM except setting of TPM ownership is allowed if not present already. An enabled and activated TPM executes all commands that use TPM functions and TPM security operations will be available.
TPM Administrative Control**	**No Operation** Turn On Turn Off Clear Ownership	[No Operation] - No changes to current state. [Turn On] - Enables and activates TPM. [Turn Off] - Disables and deactivates TPM. [Clear Ownership] - Removes the TPM ownership authentication and returns the TPM to a factory default state. **Note**: The BIOS setting returns to [No Operation] on every boot cycle by default.	

5.3 Intel® Trusted Execution Technology

The Intel® Xeon® Processor E5-2600 support Intel® Trusted Execution Technology (Intel® TXT), which is a robust security environment. Designed to help protect against software-based attacks, Intel® Trusted Execution Technology integrates new security features and capabilities into the processor, chipset and other platform components. When used in conjunction with Intel® Virtualization Technology, Intel® Trusted Execution Technology provides hardware-rooted trust for your virtual applications.

This hardware-rooted security provides a general-purpose, safer computing environment capable of running a wide variety of operating systems and applications to increase the confidentiality and integrity of sensitive information without compromising the usability of the platform.

Intel® Trusted Execution Technology requires a computer system with Intel® Virtualization Technology enabled (both VT-x and VT-d), an Intel® Trusted Execution Technology-enabled processor, chipset and BIOS, Authenticated Code Modules, and an Intel® Trusted Execution

Technology compatible measured launched environment (MLE). The MLE could consist of a virtual machine monitor, an OS or an application. In addition, Intel® Trusted Execution Technology requires the system to include a TPM v1.2, as defined by *the Trusted Computing Group TPM PC Client Specifications*, Revision 1.2.

When available, Intel Trusted Execution Technology can be enabled or disabled in the processor by a BIOS Setup option.

For general information about Intel® TXT, visit the Intel® Trusted Execution Technology website, http://www.intel.com/technology/security/.

6. Intel® Server Board S2600CP and Intel® Server System P4000CP Platform Management

6.1 Server Management Function Architecture

6.1.1 Feature Support

6.1.1.1 IPMI 2.0 Features

The IPMI 2.0 features are as follows:

- Baseboard management controller (BMC)
- IPMI Watchdog timer
- Messaging support, including command bridging and user/session support
- Chassis device functionality, including power/reset control and BIOS boot flags support
- Event receiver device: The BMC receives and processes events from other platform subsystems.
- Field Replaceable Unit (FRU) inventory device functionality: The BMC supports access to system FRU devices using IPMI FRU commands.
- System Event Log (SEL) device functionality: The BMC supports and provides access to a SEL.
- Sensor Data Record (SDR) repository device functionality: The BMC supports storage and access of system SDRs.
- Sensor device and sensor scanning/monitoring: The BMC provides IPMI management of sensors. It polls sensors to monitor and report system health.
- IPMI interfaces
- Host interfaces include system management software (SMS) with receive message queue support, and server management mode (SMM)
- IPMB interface
- LAN interface that supports the IPMI-over-LAN protocol Remote Management Control Protocol (RMCP, RMCP+)
- Serial-over-LAN (SOL)
- ACPI state synchronization: The BMC tracks ACPI state changes that are provided by the BIOS.
- BMC Self Test: The BMC performs initialization and run-time self-tests and makes results available to external entities.

See also the *Intelligent Platform Management Interface Specification Second Generation,* v2.0.

6.1.1.2 Non IPMI features

The BMC supports the following non-IPMI features. This list does not preclude support for future enhancements or additions.

- In-circuit BMC firmware update
- Fault resilient booting (FRB): FRB2 is supported by the watchdog timer functionality.

- Chassis intrusion detection (dependent on platform support)
- Basic fan control using Control version 2 SDRs
- Fan redundancy monitoring and support
- Power supply redundancy monitoring and support
- Hot-swap fan support
- Acoustic management: Support for multiple fan profiles
- Signal testing support: The BMC provides test commands for setting and getting platform signal states.
- The BMC generates diagnostic beep codes for fault conditions.
- System GUID storage and retrieval
- Front panel management: The BMC controls the system status LED and chassis ID LED. It supports secure lockout of certain front panel functionality and monitors button presses. The chassis ID LED is turned on using a front panel button or a command.
- Power state retention
- Power fault analysis
- Intel® Light-Guided Diagnostics
- Power unit management: Support for power unit sensor. The BMC handles power-good dropout conditions.
- DIMM temperature monitoring: New sensors and improved acoustic management using closed-loop fan control algorithm taking into account DIMM temperature readings.
- Address Resolution Protocol (ARP): The BMC sends and responds to ARPs (supported on embedded NICs).
- Dynamic Host Configuration Protocol (DHCP): The BMC performs DHCP (supported on embedded NICs).
- Platform environment control interface (PECI) thermal management support
- E-mail alerting
- Embedded web server
- Integrated KVM
- Integrated Remote Media Redirection
- Lightweight Directory Access Protocol (LDAP) support
- Intel® Intelligent Power Node Manager support

6.1.1.3 New Manageability Features

Intel® S2600CP Server Platforms offer a number of changes and additions to the manageability features that are supported on the previous generation of servers. The following is a list of the more significant changes that are common to this generation Integrated BMC based Intel® Server boards:

- Sensor and SEL logging additions/enhancements (for example, additional thermal monitoring capability)
- SEL Severity Tracking and the Extended SEL

- Embedded platform debug feature which allows capture of detailed data for later analysis.
- Provisioning and inventory enhancements:
  - Inventory data/system information export (partial SMBIOS table)
- Enhancements to fan speed control.
- DCMI 1.1 compliance (product-specific).
- Support for embedded web server UI in *Basic Manageability* feature set.
- Enhancements to embedded web server
  - Human-readable SEL
  - Additional system configurability
  - Additional system monitoring capability
  - Enhanced on-line help
- Enhancements to KVM redirection
  - Support for higher resolution
- Support for EU Lot6 compliance
- Management support for PMBus rev1.2 compliant power supplies
- BMC Data Repository (Managed Data Region Feature)
- Local Control Display Panel
- System Airflow Monitoring
- Exit Air Temperature Monitoring
- Ethernet Controller Thermal Monitoring
- Global Aggregate Temperature Margin Sensor
- Memory Thermal Management
- Power Supply Fan Sensors
- Energy Star Server Support
- Smart Ride Through (SmaRT)/Closed Loop System Throttling (CLST)
- Power Supply Cold Redundancy
- Power Supply FW Update
- Power Supply Compatibility Check
- BMC FW reliability enhancements:
  - Redundant BMC boot blocks to avoid possibility of a corrupted boot block resulting in a scenario that prevents a user from updating the BMC.
  - BMC System Management Health Monitoring

6.1.2 Basic and Advanced Features

The bellowing table lists basic and advanced feature support. Individual features may vary by platform. See the appropriate Platform Specific EPS addendum for more information.

Table 14. Basic and Advanced Features

Feature	Basic	Advanced
IPMI 2.0 Feature Support	X	X

Feature	Basic	Advanced
In-circuit BMC Firmware Update	X	X
FRB 2	X	X
Chassis Intrusion Detection	X	X
Fan Redundancy Monitoring	X	X
Hot-Swap Fan Support	X	X
Acoustic Management	X	X
Diagnostic Beep Code Support	X	X
Power State Retention	X	X
ARP/DHCP Support	X	X
PECI Thermal Management Support	X	X
E-mail Alerting	X	X
Embedded Web Server	X	X
SSH Support	X	X
Integrated KVM		X
Integrated Remote Media Redirection		X
Lightweight Directory Access Protocol (LDAP)	X	X
Intel® Intelligent Power Node Manager Support	X	X
SMASH CLP	X	X

6.1.3 Integrated BMC Hardware: Emulex* Pilot III

6.1.3.1 Emulex* Pilot III Baseboard Management Controller Functionality

The Integrated BMC is provided by an embedded ARM9 controller and associated peripheral functionality that is required for IPMI-based server management. Firmware usage of these hardware features is platform dependant.

The following is a summary of the Integrated BMC management hardware features that comprise the BMC:

- 400MHz 32-bit ARM9 processor with memory management unit (MMU)
- Two independent10/100/1000 Ethernet Controllers with Reduced Media Independent Interface (RMII)/Reduced Gigabit Media Independent Interface (RGMII) support
- DDR2/3 16-bit interface with up to 800 MHz operation
- 16 10-bit ADCs
- Sixteen fan tachometers
- Eight Pulse Width Modulators (PWM)
- Chassis intrusion logic
- JTAG Master
- Eight I^2C interfaces with master-slave and SMBus timeout support. All interfaces are SMBus 2.0 compliant.
- Parallel general-purpose I/O Ports (16 direct, 32 shared)
- Serial general-purpose I/O Ports (80 in and 80 out)
- Three UARTs
- Platform Environmental Control Interface (PECI)
- Six general-purpose timers
- Interrupt controller

- Multiple Serial Peripheral Interface (SPI) flash interfaces
- NAND/Memory interface
- Sixteen mailbox registers for communication between the BMC and host
- LPC ROM interface
- BMC watchdog timer capability
- SD/MMC card controller with DMA support
- LED support with programmable blink rate controls on GPIOs
- Port 80h snooping capability
- Secondary Service Processor (SSP), which provides the HW capability of offloading time critical processing tasks from the main ARM core.

Emulex* Pilot III contains an integrated SIO, KVMS subsystem and graphics controller with the following features:

6.1.3.1.1 Super I/O (SIO)

The BMC integrates a super I/O module with the following features:

- Keyboard Style/BT interface for BMC support
- Two Fully Functional Serial Ports, compatible with the 16C550
- Serial IRQ Support
- Up to 16 Shared GPIO available for host processor
- Programmable Wake-up Event Support
- Plug and Play Register Set
- Power Supply Control

6.1.3.1.2 Graphics Controller

The graphics controller provides the following features:

- Integrated Graphics Core with 2D Hardware accelerator
- High speed Integrated 24-bit RAMDAC
  DDR-2/3 memory interface with 16Mbytes of memory allocated and reported for graphics memory.

6.1.3.1.3 Remote Keyboard, Video, Mouse, and Storage (KVMS)

The Integrated BMC contains a remote KVMS subsystem with the following features:

- USB 2.0 interface for Keyboard, Mouse and Remote storage such as CD/DVD ROM and floppy
- USB 1.1/USB 2.0 interface for PS2 to USB bridging, remote Keyboard and Mouse
- Hardware Based Video Compression and Redirection Logic
- Supports both text and Graphics redirection
- Hardware assisted Video redirection using the Frame Processing Engine
- Direct interface to the Integrated Graphics Controller registers and Frame buffer
- Hardware-based encryption engine

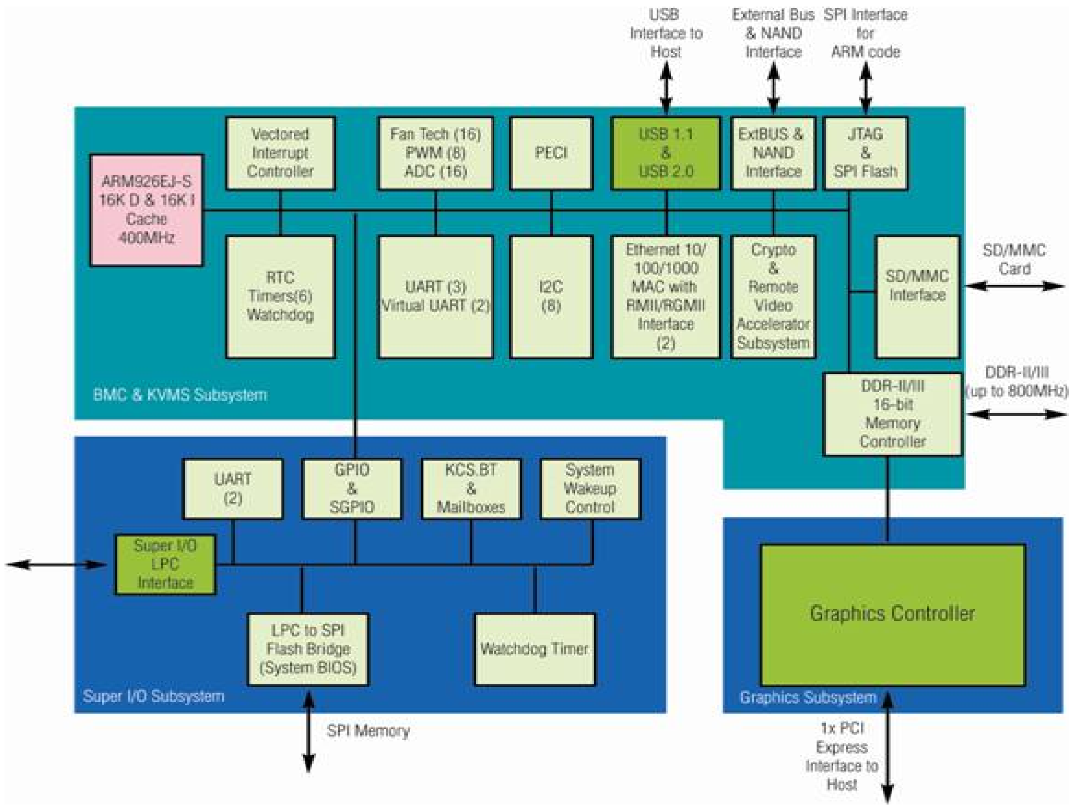


Figure 28. Integrated BMC Hardware

6.2 Server Management Functional Specifications

6.2.1 BMC Internal Timestamp Clock

The BMC maintains an internal timestamp clock that is used by various BMC subsystems, for example, for time stamping SEL entries. As part of BMC initialization after AC power is applied or the BMC is reset, the BMC initializes this internal clock to the value retrieved from the SSB component's RTC by a SMBus slave read operation. This is the system RTC and is on the battery power well so it maintains the current time even when there is no AC supplied to the system.

6.2.1.1 System Clock Synchronization

The BIOS must send the *Set SEL Time* command with the current system time to the BMC during system Power-on Self-Test (POST). Synchronization during very early POST is preferred, so that any SEL entries recorded during system boot can be accurately time stamped. Additionally, during sleep state transitions other than S0 the BIOS will synchronize the time.

If the time is modified through an OS interface, then the BMC's time is not synchronized until the next system reboot.

6.2.2 System Event Log (SEL)

The BMC implements the system event log as specified in the *Intelligent Platform Management Interface Specification, Version 2.0.* The SEL is accessible regardless of the system power state through the BMC's in-band and out-of-band interfaces.

The BMC allocates 95231 bytes (approx 93 KB) of non-volatile storage space to store system events. The SEL timestamps may not be in order. Up to 3,639 SEL records can be stored at a time. Any command that results in an overflow of the SEL beyond the allocated space is rejected with an “Out of Space” IPMI completion code (C4h).

6.2.2.1 Sensor Data Record (SDR) Repository

The BMC implements the sensor data record (SDR) repository as specified in the *Intelligent Platform Management Interface Specification, Version 2.0.* The SDR is accessible through the BMC’s in-band and out-of-band interfaces regardless of the system power state The BMC allocates 65,519 bytes of non-volatile storage space for the SDR.

6.2.3 Field Replaceable Unit (FRU) Inventory Device

The BMC implements the interface for logical FRU inventory devices as specified in the *Intelligent Platform Management Interface Specification, Version 2.0.* This functionality provides commands used for accessing and managing the FRU inventory information. These commands can be delivered through all interfaces.

The BMC provides FRU device command access to its own FRU device and to the FRU devices throughout the server. The FRU device ID mapping is defined in the Platform Specific Information. The BMC controls the mapping of the FRU device ID to the physical device.

6.2.4 BMC Beep Codes

The BMC may generate beep codes upon detection of failure conditions. Beep codes are sounded each time the problem is discovered (for example, on each power-up attempt), but are not sounded continuously. Common supported codes are listed in below table.

Additional platform-specific beep codes can be found in the appropriate Platform Specific Information. Each digit in the code is represented by a sequence of beeps whose count is equal to the digit.

Table 15. BMC Beep Codes

Code	Reason for Beep	Associated Sensors
1-5-2-1	No CPUs installed or first CPU socket is empty.	CPU Missing Sensor
1-5-2-4	MSID Mismatch.	MSID Mismatch Sensor.
1-5-4-2	Power fault: DC power is unexpectedly lost (power good dropout).	Power unit – power unit failure offset.
1-5-4-4	Power control fault (power good assertion timeout).	Power unit – soft power control failure offset.
1-5-1-2	VR Watchdog Timer sensor assertion	VR Watchdog Timer

Code	Reason for Beep	Associated Sensors
1-5-1-4	The system does not power on or unexpectedly powers off and a power supply unit (PSU) is present that is an incompatible model with one or more other PSUs in the system	PS Status

6.2.5 Diagnostic Interrupt (NMI) Button

The BMC generates an NMI pulse under certain conditions. The BMC-generated NMI pulse duration is at least 30 ms. Once an NMI has been generated by the BMC, the BMC does not generate another NMI until the system has been reset or powered down.

The following actions cause the BMC to generate an NMI pulse:

a. Receiving a *Chassis Control* command to pulse the diagnostic interrupt. This command does not cause an event to be logged in the SEL.
b. Watchdog timer pre-timeout expiration with NMI/diagnostic interrupt pre-timeout action enabled.

Table 16 shows behavior regarding NMI signal generation and event logging by the BMC.

Table 16. NMI Signal Generation and Event Logging

Causal Event	NMI	
	Signal Generation	Front Panel Diag Interrupt Sensor Event Logging Support
Chassis Control command (pulse diagnostic interrupt)	X	–
Front panel diagnostic interrupt button pressed	X	X
Watchdog Timer pre-timeout expiration with NMI/diagnostic interrupt action	X	X

6.2.6 BMC Watchdog

The BMC FW is increasingly called upon to perform system functions that are time-critical in that failure to provide these functions in a timely manner can result in system or component damage. Intel® Server Platforms introduce a BMC watchdog feature to provide a safe-guard against this scenario by providing an automatic recovery mechanism. It also can provide automatic recovery of functionality that has failed due to a fatal FW defect triggered by a rare sequence of events or a BMC hang due to some type of HW glitch (for example, power).

This feature is comprised of a set of capabilities whose purpose is to detect misbehaving subsections of BMC firmware, the BMC CPU itself, or HW subsystems of the BMC component, and to take appropriate action to restore proper operation. The action taken is dependent on the nature of the detected failure and may result in a restart of the BMC CPU, one or more BMC HW subsystems, or a restart of malfunctioning FW subsystems.

The BMC watchdog feature will only allow up to three resets of the BMC CPU (such as HW reset) or entire FW stack (such as a SW reset) before giving up and remaining in the uBOOT code. This count is cleared upon cycling of power to the BMC or upon continuous operation of the BMC without a watchdog-generated reset occurring for a period of > 30 minutes. The BMC

FW logs a SEL event indicating that a watchdog-generated BMC reset (either soft or hard reset) has occurred. This event may be logged after the actual reset has occurred. Refer sensor section for details for the related sensor definition. The BMC will also indicate a degraded system status on the Front Panel Status LED after an BMC HW reset or FW stack reset. This state (which follows the state of the associated sensor) will be cleared upon system reset or (AC or DC) power cycle.

Note: A reset of the BMC may result in the following system degradations that will require a system reset or power cycle to correct:

1. Timeout value for the rotation period can be set using this parameterPotentially incorrect ACPI Power State reported by the BMC.
2. Reversion of temporary test modes for the BMC back to normal operational modes.
3. FP status LED and DIMM fault LEDs may not reflect BIOS detected errors.

6.3 Sensor Monitoring

6.3.1 Overview

The BMC monitors system hardware and reports system health. The information gathered from physical sensors is translated into IPMI sensors as part of the “IPMI Sensor Model”. The BMC also reports various system state changes by maintaining virtual sensors that are not specifically tied to physical hardware. This section describes the BMC sensors as well as describing how specific sensor types are modeled. Unless otherwise specified, the term “sensor” refers to the IPMI sensor-model definition of a sensor.

6.3.2 Core Sensors

Specific server boards may only implement a sub-set of sensors and/or may include additional sensors. The system-specific details of supported sensors and events are described in the Appendix of this document. The actual sensor name associated with a sensor number may vary between server boards or systems.

Sensor Type Codes

Sensor table given below lists the sensor identification numbers and information regarding the sensor type, name, supported thresholds, assertion and de-assertion information, and a brief description of the sensor purpose. Refer to the *Intelligent Platform Management Interface Specification, Version 2.0* for sensor and event/reading-type table information.

1. **Sensor Type**
   The sensor type references the values in the Sensor Type Codes table in the *Intelligent Platform Management Interface Specification Second Generation, Version 2.0*. It provides a context to interpret the sensor.
2. **Event/Reading Type**
   The event/reading type references values from the Event/Reading Type Code Ranges and the Generic Event/Reading Type Code tables in the *Intelligent Platform Management Interface Specification Second Generation*, *Version 2.0*. Digital sensors are specific type of discrete sensors that only have two states.
3. **Event Thresholds/Triggers**
   The following event thresholds are supported for threshold type sensors:

- [u,l][nr,c,nc] upper non-recoverable, upper critical, upper non-critical, lower non-recoverable, lower critical, lower non-critical uc, lc upper critical, lower critical

  Event triggers are supported event-generating offsets for discrete type sensors. The offsets can be found in the *Generic Event/Reading Type Code* or *Sensor Type Code* tables in the *Intelligent Platform Management Interface Specification Second Generation Version 2.0*, depending on whether the sensor event/reading type is generic or a sensor-specific response.

4. **Assertion/Deassertion**
   Assertion and de-assertion indicators reveal the type of events this sensor generates:
   - As: Assertion
   - De: De-assertion
5. **Readable Value/Offsets**
   - Readable value indicates the type of value returned for threshold and other non-discrete type sensors.
   - Readable offsets indicate the offsets for discrete sensors that are readable by means of the *Get Sensor Reading* command. Unless otherwise indicated, event triggers are readable. Readable offsets consist of the reading type offsets that do not generate events.
6. **Event Data**
   Event data is the data that is included in an event message generated by the associated sensor. For threshold-based sensors, these abbreviations are used:
   - R: Reading value
   - T: Threshold value
7. **Rearm Sensors**
   The rearm is a request for the event status for a sensor to be rechecked and updated upon a transition between good and bad states. Rearming the sensors can be done manually or automatically. This column indicates the type supported by the sensor. The following abbreviations are used in the comment column to describe a sensor:
   - A: Auto-rearm
   - M: Manual rearm
   - I: Rearm by init agent
8. **Default Hysteresis**
   The hysteresis setting applies to all thresholds of the sensor. This column provides the count of hysteresis for the sensor, which can be 1 or 2 (positive or negative hysteresis).
9. **Criticality**
   Criticality is a classification of the severity and nature of the condition. It also controls the behavior of the front panel status LED.
10. **Standby**
    Some sensors operate on standby power. These sensors may be accessed and/or generate events when the main (system) power is off, but AC power is present.

6.3.3 BMC System Management Health Monitoring

The BMC tracks the health of each of its IPMI sensors and report failures by providing a "BMC FW Health" sensor of the IPMI 2.0 sensor type Management Subsystem Health with support for the Sensor Failure offset. Only assertions should be logged into the SEL for the Sensor Failure offset. The sensor number of the failed sensor is provided in event data byte 2, as per the *IPMI 2.0 Specification.* The BMC Firmware Health sensor asserts for any sensor when 10 consecutive sensor errors are read. These are not standard sensor events (that is, threshold crossings or discrete assertions). These are BMC Hardware Access Layer (HAL) errors like I2C NAKs or internal errors while attempting to read a register. If a successful sensor read is completed, the counter resets to zero.

IPMI Sensor Characteristics

a. Event reading type code: 6Fh (Sensor specific)
b. Sensor type code: 28h (Management Subsystem Health)
c. Rearm type: Auto

If this sensor is implemented, then the following sensor-specific offsets are supported.

Table 17. Supported BMC FW Health Sensor Offsets

Offset	Description	Event Logging
04h	Sensor failure	Assertion and deassertion

6.3.4 Processor Sensors

The BMC provides IPMI sensors for processors and associated components, such as voltage regulators and fans. The sensors are implemented on a per-processor basis.

Table 18. Processor Sensors

Sensor Name	Per-Processor Socket	Description
Processor Status	Yes	Processor presence and fault state
Digital Thermal Sensor	Yes	Relative temperature reading by means of PECI
Processor VRD Over-Temperature Indication	Yes	Discrete sensor that indicates a processor VRD has crossed an upper operating temperature threshold
Processor Voltage	Yes	Threshold sensor that indicates a processor power-good state
Processor Thermal Control (Prochot)	Yes	Percentage of time a processor is throttling due to thermal conditions

6.3.5 Thermal and Acoustic Management

This feature refers to enhanced fan management to keep the system optimally cooled while reducing the amount of noise generated by the system fans. Aggressive acoustics standards might require a trade-off between fan speed and system performance parameters that contribute to the cooling requirements, primarily memory bandwidth. The BIOS, BMC, and SDRs work together to provide control over how this trade-off is determined.

This capability requires the BMC to access temperature sensors on the individual memory DIMMs. Additionally, closed-loop thermal throttling is only supported with buffered DIMMs.

6.3.6 Thermal Sensor Input to Fan Speed Control

The BMC uses various IPMI sensors as input to the fan speed control. Some of the sensors are IPMI models of actual physical sensors whereas some are “virtual” sensors whose values are derived from physical sensors using calculations and/or tabular information.

The following IPMI thermal sensors are used as input to the fan speed control:

- Front panel temperature sensor
- Baseboard temperature sensors
- CPU DTS-Spec margin sensors
- DIMM thermal margin sensors
- Exit air temperature sensor
- Global aggregate thermal margin sensors
- PCH temperature sensor
- On-board Ethernet controller temperature sensors (support for this is specific to the Ethernet controller being used)
- Add-in Intel SAS/IO module temperature sensor(s) (if present)
- Power supply thermal sensors (only available on PMBus-compliant power supplies).

A simple model is shown in the following figure which gives a high level graphic of the fan speed control structure creates the resulting fan speeds.

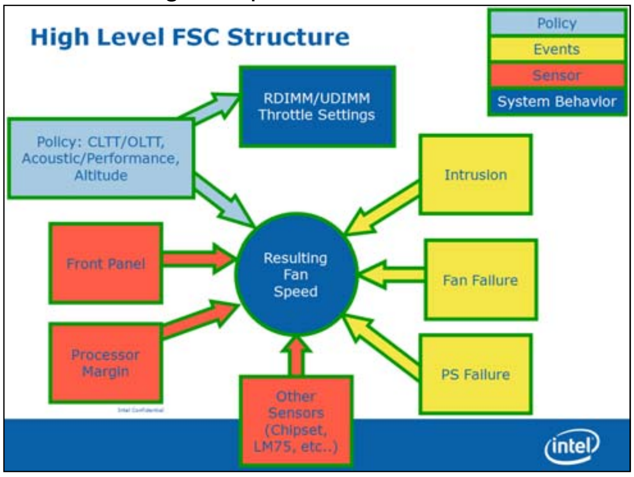


Figure 29. High-level Fan Speed Control Process

6.3.7 Power Supply Status\Health Sensors

The BMC supports one Power Supply Status sensor for each system power supply module. In order to track problems in which the PSU firmware is not operating to full capacity, an additional case (degraded condition if the PSU firmware is not operating to full capacity) is added to the existing Power Supply Status sensor offset definitions. This is handled by assertion of the “configuration error” offset of the PSU status sensor. These sensors are only supported for systems that use PMBus-compliant power supplies.

IPMI Sensor Characteristics

a. Event reading type code: 6Fh (Sensor Specific)
b. Event sensor type code: 08h (Power Supply)

c. Rearm type: Auto

The following sensor-specific offsets are supported.

Table 19. Supported Power Supply Status Sensor Offsets

Offset	Description	Event Logging
00h	Presence detected – Asserted if power supply module is present. Events are only logged for power supply presence upon changes in the presence state after AC power is applied (no events logged for initial state).	Assertion and Deassertion
01h	Power supply failure detected – Asserted if power supply module has failed. The following codes for failure modes are put into the SEL Event Data 2 byte: ▪ 01h - Output voltage fault ▪ 02h - Output power fault ▪ 03h - Output over-current fault ▪ 04h - Over-temperature fault ▪ 05h – Fan fault The SEL Event Data 3 byte will have the contents of the associated PMBus Status register to allow for showing multiple conditions for the event. For example, Data 3 will have the contents of the VOLTAGE_STATUS register at the time an Output Voltage fault was detected. Refer to the *PMBus Specification* for details on specific resister contents	Assertion and Deassertion
02h	Predictive failure – Asserted if some condition, such as failing fan, has been detected that is likely to lead to a power supply module failure. The following codes for warning modes are put into the SEL Event Data 2 byte: ▪ 01h - Output voltage warning ▪ 02h - Output power warning ▪ 03h - Output over-current warning ▪ 04h - Over-temperature warning ▪ 05h - Fan warning ▪ 06h - Under-voltage warning ▪ 07h - Input over-current warning ▪ 08h - Input over-power warning The SEL Event Data 3 byte will have the contents of the associated PMBus Status register to allow for showing multiple conditions for the event. For example, Data 3 will have the contents of the VOLTAGE_STATUS register at the time an Output Voltage Warning was detected. Refer to the *PMBus Specification* for details on specific resister contents.	Assertion and Deassertion
03h	Power supply AC lost – Asserted if there is no AC power input to power supply module.	Assertion and Deassertion

Offset	Description	Event Logging
06h	Configuration error – The following codes for configuration errors are put into the SEL Event Data 2 byte: ▪ 01h - The BMC cannot access the PMBus device on the PSU but its FRU device is responding. ▪ 02h - The PMBUS_REVISION command returns a version number that is not supported (only version 1.1 and 1.2 are supported for platforms covered under this FW EAS). ▪ 03h - The PMBus device does not successfully respond to the PMBUS_REVISION command. ▪ 04h – The PSU is incompatible with one or more PSUs that are present in the system. 05h –The PSU FW is operating in a degraded mode (likely due to a failed firmware update).	Assertion and Deassertion

6.3.8 System Event Sensor

The BMC supports a System Event sensor and logs SEL event for following events.

Table 20. Support System Event Sensor Offsets

Offset	Description	Event Logging
02h	OEM code (Undetermined system HW failure)	Assertion and Deassertion
04h	PEF action	Assertion only

For offset 2, OEM code will be logged in event data byte 2 to indicate the type of failure. Only one value will be supported at this time, but others may be added in the future. The code for this particular fault will be 0x00 (PECI access failure) and all other values reserved. Upon detection of the CPU PECI fault condition, the offset shall assert. It shall deassert upon system power cycle or system reset. Assertion of offset 02h shall contribute a “fatal” condition to the system status as reflected in the Front Panel system status LED.

6.4 Channel Management

This section describes the supported BMC communication interfaces:

- Host SMS interface by means of low pin count (LPC)/keyboard controller style (KCS) interface
- Host SMM interface by means of low pin count (LPC)/keyboard controller style (KCS) interface
- Intelligent Platform Management Bus (IPMB) I2C interface
- LAN interface using the IPMI-over-LAN protocols

6.4.1 Channel Management

Every messaging interface is assigned an IPMI channel ID by IPMI 2.0. Commands are provided to configure each channel for privilege levels and access modes. Table 21 shows the standard channel assignments:

Table 21. Standard Channel Assignments

Channel ID	Interface	Supports Sessions
0	Primary IPMB	No
1	LAN 1	Yes
2	LAN 2	Yes
3	LAN3 [1] (Provided by the Intel® Dedicated Server Management NIC)	Yes
4	Reserved	Yes
5	USB	No
6	Secondary IPMB	No
7	SMM	No
8 – 0Dh	Reserved	–
0Eh	Self [2]	–
0Fh	SMS/Receive Message Queue	No

Notes:

1. Optional hardware supported by the server system.
2. Refers to the actual channel used to send the request.

6.4.2 User Model

The BMC supports the IPMI 2.0 user model. 15 user IDs are supported. These 15 users can be assigned to any channel. The following restrictions are placed on user-related operations:

1. User names for User IDs 1 and 2 cannot be changed. These are always "" (Null/blank) and "root" respectively.
2. User 2 ("root") always has the administrator privilege level.
3. All user passwords (including passwords for 1 and 2) may be modified.
4. User IDs 3-15 may be used freely, with the condition that user names are unique. Therefore, no other users can be named "" (Null), "root," or any other existing user name.

6.4.3 LAN Interface

The BMC implements both the IPMI 1.5 and IPMI 2.0 messaging models. These provide out-of-band local area network (LAN) communication between the BMC and the network.

Run-time determination of LAN channel capabilities can be determined by both standard IPMI defined mechanisms.

6.4.3.1 IPMI 1.5 Messaging

The communication protocol packet format consists of IPMI requests and responses encapsulated in an IPMI session wrapper for authentication, and wrapped in an RMCP packet, which is wrapped in an IP/UDP packet. Although authentication is provided, no encryption is provided, so administrating some settings, such as user passwords, through this interface is not advised.

Session establishment commands are IPMI commands that do not require authentication or an associated session.

The BMC supports the following authentication types over the LAN interface.

1. None (no authentication)
2. Straight password/key
3. MD5

6.4.3.2 IPMI 2.0 Messaging

IPMI 2.0 messaging is built over RMCP+ and has a different session establishment protocol. The session commands are defined by RMCP+ and implemented at the RMCP+ level, not IPMI commands. Authentication is implemented at the RMCP+ level. RMCP+ provides link payload encryption, so it is possible to communicate private/sensitive data (confidentiality).

The BMC supports the cipher suites identified in Table 22.

Table 22. Supported RMCP+ Cipher Suites

ID	Authentication Algorithm	Integrity Algorithm(s)	Confidentiality Algorithm(s)
0[1]	RAKP-none	None	None
1	RAKP-HMAC-SHA1	None	None
2	RAKP-HMAC-SHA1	HMAC-SHA1-96	None
3	RAKP-HMAC-SHA1	HMAC-SHA1-96	AES-CBC-128
6	RAKP-HMAC-MD5	None	None
7	RAKP-HMAC-MD5	HMAC-MD5-128	None
8	RAKP-HMAC-MD5	HMAC-MD5-128	AES-CBC-128
11	RAKP-HMAC-MD5	MD5-128	None
12	RAKP-HMAC-MD5	MD5-128	AES-CBC-128

Note: Cipher suite 0 defaults to callback privilege for security purposes. This may be changed by any administrator.

For user authentication, the BMC can be configured with 'null' user names, whereby password/key lookup is done based on 'privilege level only', or with non-null user names, where the key lookup for the session is determined by user name.

IPMI 2.0 messaging introduces payload types and payload IDs to allow data types other than IPMI commands to be transferred. IPMI 2.0 serial-over-LAN is implemented as a payload type.

Table 23. Supported RMCP+ Payload Types

Payload Type	Feature	IANA
00h	IPMI message	N/A
01h	Serial-over-LAN	N/A
02h	OEM explicit	Intel (343)
10h – 15h	Session setup	N/A

6.4.3.3 RMCP/ASF Messaging

The BMC supports RMCP ping discovery in which the BMC responds with a pong message to an RMCP/ASF ping request. This is implemented per the *Intelligent Platform Management Interface Specification Second Generation, Version 2.0*.

6.4.3.4 BMC LAN Channels

The BMC supports three RMII/RGMII ports that can be used for communicating with Ethernet devices. Two ports are used for communication with the on-board NICs and one is used for communication with an Ethernet PHY located on an optional add-in card (or equivalent on-board circuitry).

6.4.3.4.1 Baseboard NICs

The specific Ethernet controller (NIC) used on a server is platform-specific but all baseboard device options provide support for an NC-SI manageability interface. This provides a sideband high-speed connection for manageability traffic to the BMC while still allowing for a simultaneous host access to the OS if desired.

The Network Controller Sideband Interface (NC-SI) is a DMTF industry standard protocol for the side band management LAN interface. This protocol provides a fast multi-drop interface for management traffic.

The baseboard NIC(s) are connected to a single BMC RMII/RGMII port that is configured for RMII operation. The NC-SI protocol is used for this connection and provides a 100 Mb/s full-duplex multi-drop interface which allows multiple NICs to be connected to the BMC. The physical layer is based upon RMII, however RMII is a point-to-point bus whereas NC-SI allows 1 master and up to 4 slaves. The logical layer (configuration commands) is incompatible with RMII.

Multi-port baseboard NICs on some products will provide support for a dedicated management channel than can be configured to be hidden from the host and only used by the BMC. This mode of operation is configured by a BIOS setup option.

6.4.3.4.2 Dedicated Management Channel

An additional LAN channel dedicated to BMC usage and not available to host SW is supported by an optional add-in card. There is only a PHY device present on the add-in card. The BMC has a built-in MAC module that uses the RGMII interface to link with the card's PHY. Therefore, for this dedicated management interface, the PHY and MAC are located in different devices.

The PHY on the card connects to the BMC's other RMII/RGMII interface (that is, the one that is not connected to the baseboard NICs). This BMC port is configured for RGMII usage.

In addition to the use of an add-in card for a dedicated management channel, on systems that support multiple Ethernet ports on the baseboard, the system BIOS provides a setup option to allow one of these baseboard ports to be dedicated to the BMC for manageability purposes. When this is enabled, that port is hidden from the OS.

6.4.3.4.3 Concurrent Server Management Use of Multiple Ethernet Controllers

Provided the HW supports a management link between the BMC and a NIC port, the BMC FW supports concurrent OOB LAN management sessions for the following combination:

- 2 on-board NIC ports

- 1 on-board NIC and the optional dedicated add-in management NIC.
- 2 on-board NICs and optional dedicated add-in management NIC.

All NIC ports must be on different subnets for the above concurrent usage models.
MAC addresses are assigned for management NICs from a pool of up to 3 MAC addresses allocated specifically for manageability. The total number of MAC addresses in the pool is dependent on the product HW constraints (for example, a board with 2 NIC ports available for manageability would have a MAC allocation pool of 2 addresses).For these channels, support can be enabled for IPMI-over-LAN and DHCP.

For security reasons, embedded LAN channels have the following default settings:

- IP Address: Static
- All users disabled

IPMI-enabled network interfaces may not be placed on the same subnet. This includes the Intel® Dedicated Server Management NIC and either of the BMC's embedded network interfaces.

Host-BMC communication over the same physical LAN connection – also known as "loopback" – is not supported. This includes "ping" operations.

On baseboards with more than two onboard NIC ports, only the first two ports can be used as BMC LAN channels. The remaining ports have no BMC connectivity.

Maximum bandwidth supported by BMC LAN channels are as follows:

- BMC LAN1 (Baseboard NIC port) ----- 100M (10M in DC off state)
- BMC LAN 2 (Baseboard NIC port) ----- 100M (10M in DC off state)
- BMC LAN 3 (Dedicated NIC) ----- 100M

6.4.3.5 Dedicated Management NIC MAC Address

Intel® Server Board S2600CP has up to seven MAC addresses assigned to it at the Intel factory. The printed MAC address is assigned to NIC1 on the server board.

There will be seven MAC addresses assigned as follows:

- NIC 1 MAC address (for OS usage)
- NIC 2 MAC address = NIC 1 MAC address + 1 (for OS usage)
- NIC 3 MAC address = NIC 1 MAC address + 2 (for OS usage)
- NIC 4 MAC address = NIC 1 MAC address + 3 (for OS usage)
- BMC LAN channel 1 MAC address = NIC1 MAC address + 4
- BMC LAN channel 2 MAC address = NIC1 MAC address + 5
- BMC LAN channel 3 (RMM) MAC address = NIC1 MAC address + 6.

6.4.3.6 IPV6 Support

In addition to IPv4, Intel® S2600CP Server Board support IPv6 for manageability channels. Configuration of IPv6 is provided by extensions to the IPMI Set and Get LAN Configuration Parameters commands as well as through a Web Console IPv6 configuration web page.

The BMC supports IPv4 and IPv6 simultaneously so they are both configured separately and completely independently. For example, IPv4 can be DHCP configured while IPv6 is statically configured or vice versa.

6.4.3.6.1 LAN Failover

The BMC FW provides a LAN failover capability such that the failure of the system HW associated with one LAN link will result in traffic being rerouted to an alternate link. This functionality is configurable by IPMI methods as well as by the BMC's Embedded UI, allowing for user to specify the physical LAN links constitute the redundant network paths or physical LAN links constitute different network paths. BMC will support only a all or nothing" approach – that is, all interfaces bonded together, or none are bonded together.

The LAN Failover feature applies only to BMC LAN traffic. It bonds all available Ethernet devices but only one is active at a time. When enabled, If the active connection's leash is lost, one of the secondary connections is automatically configured so that it has the same IP address (the next active LAN link will be chosen randomly from the pool of backup LAN links with link status as "UP"). Traffic immediately resumes on the new active connection.
The LAN Failover enable/disable command may be sent at any time. After it has been enabled, standard IPMI commands for setting channel configuration that specify a LAN channel other than the first will return an error code.

Standard IPMI commands for getting channel configuration will return the cached settings for the inactive channels.

6.4.3.7 BMC IP Address Configuration

Enabling the BMC's network interfaces requires using the *Set LAN Configuration Parameter* command to configure LAN configuration parameter 4, *IP Address Source*.

6.4.3.8 DHCP BMC Hostname

The BMC allows setting a DHCP Hostname. DHCP Hostname can be set regardless of the IP Address source configured on the BMC. But this parameter is only used if the IP Address source is set to DHCP.

6.4.3.9 Address Resolution Protocol (ARP)

The BMC can receive and respond to ARP requests on BMC NICs. Gratuitous ARPs are supported, and disabled by default.

6.4.3.10 Virtual Local Area Network (VLAN)

The BMC supports VLAN as defined by *IPMI 2.0 Specifications*. VLAN is supported internally by the BMC, not through switches. VLAN provides a way of grouping a set of systems together so that they form a logical network. This feature can be used to set up a management VLAN where only devices which are members of the VLAN will receive packets related to management and members of the VLAN will be isolated from any other network traffic. Please note that VLAN does not change the behavior of the host network setting, it only affects the BMC LAN communication.

LAN configuration options are now supported (by means of the Set LAN Config Parameters command, parameters 20 and 21) that allow support for 802.1Q VLAN (Layer 2). This allows VLAN headers/packets to be used for IPMI LAN sessions. VLAN ID's are entered and enabled by means of parameter 20 of the Set LAN Config Parameters IPMI command. When a VLAN ID is configured and enabled, the BMC only accepts packets with that VLAN tag/ID. Conversely, all BMC generated LAN packets on the channel include the given VLAN tag/ID. Valid VLAN ID's are 1 through 4094, VLAN ID's of 0 and 4095 are reserved, per the 802.1Q VLAN specification. Only one VLAN can be enabled at any point in time on a LAN channel. If an existing VLAN is enabled, it must first be disabled prior to configuring a new VLAN on the same LAN channel.

Parameter 21 (VLAN Priority) of the Set LAN Config Parameters IPMI command is now implemented and a range from 0-7 will be allowed for VLAN Priorities. Please note that bits 3 and 4 of Parameter 21 are considered Reserved bits.

Parameter 25 (VLAN Destination Address) of the Set LAN Config Parameters IPMI command is not supported and returns a completion code of 0x80 (parameter not supported) for any read/write of parameter 25.

If the BMC IP address source is DHCP, then the following behavior is seen:

- If the BMC is first configured for DHCP (prior to enabling VLAN), when VLAN is enabled, the BMC performs a discovery on the new VLAN in order to obtain a new BMC IP address.
- If the BMC is configured for DHCP (before disabling VLAN), when VLAN is disabled, the BMC performs a discovery on the LAN in order to obtain a new BMC IP address.

If the BMC IP address source is Static, then the following behavior is seen:

- If the BMC is first configured for static (prior to enabling VLAN), when VLAN is enabled, the BMC has the same IP address that was configured before. It is left to the management application to configure a different IP address if that is not suitable for VLAN.
- If the BMC is configure for static (prior to disabling VLAN), when VLAN is disabled, the BMC has the same IP address that was configured before. It is left to the management application to configure a different IP address if that is not suitable for LAN.

6.4.3.11 Secure Shell (SSH)

Secure Shell (SSH) connections are supported for one SMASH-CLP session to the BMC.

6.4.3.12 Serial-over-LAN (SOL 2.0)

The BMC supports IPMI 2.0 SOL.

IPMI 2.0 introduced a standard serial-over-LAN feature. This is implemented as a standard payload type (01h) over RMCP+.

Three commands are implemented for SOL 2.0 configuration:

1. *"Get SOL 2.0 Configuration Parameters"* and *"Set SOL 2.0 Configuration Parameters":* These commands are used to get and set the values of the SOL configuration parameters. The parameters are implemented on a per-channel basis.

2. *"Activating SOL":* This command is not accepted by the BMC. It is sent by the BMC when SOL is activated to notify a remote client of the switch to SOL.

3. Activating a SOL session requires an existing IPMI-over-LAN session. If encryption is used, it should be negotiated when the IPMI-over LAN session is established. SOL sessions are only supported on serial port 1 (COM1).

6.4.3.13 Platform Event Filter (PEF)

The BMC includes the ability to generate a selectable action, such as a system power-off or reset, when a match occurs to one of a configurable set of events. This capability is called *Platform Event Filtering,* or PEF. One of the available PEF actions is to trigger the BMC to send a LAN alert to one or more destinations.

The BMC supports 20 PEF filters. The first twelve entries in the PEF filter table are pre-configured (but may be changed by the user). The remaining entries are left blank, and may be configured by the user.

Table 24. Factory Configured PEF Table Entries

Event Filter Number	Offset Mask	Events
1	Non-critical, critical and non-recoverable	Temperature sensor out of range
2	Non-critical, critical and non-recoverable	Voltage sensor out of range
3	Non-critical, critical and non-recoverable	Fan failure
4	General chassis intrusion	Chassis intrusion (security violation)
5	Failure and predictive failure	Power supply failure
6	Uncorrectable ECC	BIOS
7	POST error	BIOS: POST code error
8	FRB2	Watchdog Timer expiration for FRB2
9	Policy Correction Time	Node Manager
10	Power down, power cycle, and reset	Watchdog timer
11	OEM system boot event	System restart (reboot)
12	Drive Failure, Predicted Failure	Hot Swap Controller

Additionally, the BMC supports the following PEF actions:

- Power off
- Power cycle
- Reset
- OEM action
- Alerts

The “Diagnostic interrupt” action is not supported.

6.4.3.14 LAN Alerting

The BMC supports sending embedded LAN alerts, called SNMP PET (Platform Event traps), and SMTP email alerts.

The BMC supports a minimum of four LAN alert destinations.

6.4.3.14.1 SNMP Platform Event Traps (PETs)

This feature enables a target system to send SNMP traps to a designated IP address by means of LAN. These alerts are formatted per the *Intelligent Platform Management Interface Specification Second Generation, Version 2.0*. A MIB file associated with the traps is provided with the BMC firmware to facilitate interpretation of the traps by external software.

The format of the MIB file is covered under RFC 2578.

6.4.3.15 Alert Policy Table

Associated with each PEF entry is an alert policy that determines which IPMI channel the alert is to be sent. There is a maximum of 20 alert policy entries. There are no pre-configured entries in the alert policy table because the destination types and alerts may vary by user. Each entry in the alert policy table contains four bytes for a maximum table size of 80 bytes.

6.4.3.15.1 E-mail Alerting

The Embedded Email Alerting feature allows the user to receive e-mails alerts indicating issues with the server. This allows e-mail alerting in an OS-absent (for example, Pre-OS and OS-Hung) situation. This feature provides support for sending e-mail by means of SMTP, the Simple Mail Transport Protocol as defined in Internet RC 821. The e-mail alert provides a text string that describes a simple description of the event. SMTP alerting is configured using the embedded web server.

6.4.3.16 SM-CLP (SM-CLP Lite)

SMASH refers to Systems Management Architecture for Server Hardware. SMASH is defined by a suite of specifications, managed by the DMTF, that standardize the manageability interfaces for server hardware. CLP refers to Command Line Protocol. SM-CLP is defined by the *Server Management Command Line Protocol Specification (SM-CLP) ver1.0*, which is part of the SMASH suite of specifications. The specifications and further information on SMASH can be found at the DMTF website (http://www.dmtf.org/).
The BMC provides an embedded “lite” version of SM-CLP that is syntax-compatible but not considered fully compliant with the DMTF standards.

6.4.3.17 Embedded Web Server

BMC Base manageability provides an embedded web server and an OEM-customizable web GUI which exposes the manageability features of the BMC base feature set. It is supported over all on-board NICs that have management connectivity to the BMC as well as an optional dedicated add-in management NIC. At least two concurrent web sessions from up to two different users is supported. The embedded web user interface shall support the following client web browsers:

1. Microsoft Internet Explorer 7.0*
2. Microsoft Internet Explorer 8.0*
3. Microsoft Internet Explorer 9.0*
4. Mozilla Firefox 3.0*
5. Mozilla Firefox 3.5*
6. Mozilla Firefox 3.6*

The embedded web user interface supports strong security (authentication, encryption, and firewall support) since it enables remote server configuration and control. Embedded web server uses ports #80 and #443. The user interface presented by the embedded web user interface shall authenticate the user before allowing a web session to be initiated. Encryption using 128-bit SSL is supported. User authentication is based on user id and password.

The GUI presented by the embedded web server authenticates the user before allowing a web session to be initiated. It presents all functions to all users but grays-out those functions that the user does not have privilege to execute. (for example, if a user does not have privilege to power control, then the item shall be displayed in grey-out font in that user's UI display). The web GUI also provides a launch point for some of the advanced features, such as KVM and media redirection. These features are grayed out in the GUI unless the system has been updated to support these advanced features.

Additional features supported by the web GUI includes:

- Presents all the Basic features to the users.
- Power on/off/reset the server and view current power state.
- Displays BIOS, BMC, ME and SDR version information.
- Display overall system health.
- Configuration of various IPMI over LAN parameters for both IPV4 and IPV6
- Configuration of alerting (SNMP and SMTP).
- Display system asset information for the product, board, and chassis.
- Display of BMC-owned sensors (name, status, current reading, enabled thresholds), including color-code status of sensors.
- Provides ability to filter sensors based on sensor type (Voltage, Temperature, Fan and Power supply related)
- Automatic refresh of sensor data with a configurable refresh rate.
- On-line help.
- Display/clear SEL (display is in easily understandable human readable format).
- Supports major industry-standard browsers (Microsoft Internet Explorer* and Mozilla Firefox*).
- The GUI session automatically times-out after a user-configurable inactivity period. By default, this inactivity period is 30 minutes.
- Embedded Platform Debug feature - Allow the user to initiate a "diagnostic dump" to a file that can be sent to Intel for debug purposes.
- Virtual Front Panel. The Virtual Front Panel provides the same functionality as the local front panel. The displayed LEDs match the current state of the local panel LEDs. The displayed buttons (for example, power button) can be used in the same manner as the local buttons.
- Display of ME sensor data. Only sensors that have associated SDRs loaded will be displayed.
- Ability to save the SEL to a file.
- Ability to force HTTPS connectivity for greater security. This is provided through a configuration option in the UI.
- Display of processor and memory information as is available over IPMI over LAN.
- Ability to get and set Node Manager (NM) power policies.
- Display of power consumed by the server.
- Ability to view and configure VLAN settings.
- Warn user the reconfiguration of IP address will cause disconnect.

- Capability to block logins for a period of time after several consecutive failed login attempts. The lock-out period and the number of failed logins that initiates the lock-out period are configurable by the user.
- Server Power Control - Ability to force into Setup on a reset.

6.4.3.18 Virtual Front Panel

- Virtual Front Panel is the module present as “Virtual Front Panel” on the left side in the embedded web server when "remote Control" tab is clicked.
- Main Purpose of the Virtual Front Panel is to provide the front panel functionality virtually.
- Virutal Front Panel (VFP) will mimic the status LED and Power LED status and Chassis ID alone. It is automatically in sync with BMC every 40 seconds.
- For any abnormal status LED state, Virtual Front Panel will get the reason behind the abnormal or status LED changes and displayed in VFP side.
- As Virtual Front Panel uses the chassis control command for power actions. It won’t log the Front button press event since Logging the front panel press event for Virtual Front Panel press will mislead the administrator.
- For Reset by Virtual Front Panel, the reset will be done by a “Chassis control” command.
- For Reset by Virtual Front Panel, the restart cause will be because of “Chassis control” command.
- During Power action, Power button/Reset button should not accept the next action until current Power action is complete and the acknowledgment from BMC is received.
- EWS will provide a valid message during Power action until it completes the current Power action.
- The VFP does not have any effect on whether the front panel is locked by “Set Front Panel Enables” command.
- The chassis ID LED provides a visual indication of a system being serviced. The state of the chassis ID LED is affected by the following actions:
- Toggled by turning the chassis ID button on or off.
- There is no precedence or lock-out mechanism for the control sources. When a new request arrives, previous requests are terminated. For example, if the chassis ID button is pressed, then the chassis ID LED changes to solid on. If the button is pressed again, then the chassis ID LED turns off.
- Note that the chassis ID will turn on because of the original chassis ID button press and will reflect in the Virtual Front Panel after VFP sync with BMC. Virtual Front Panel won’t reflect the chassis LED software blinking by software command as there is no mechanism to get the chassis ID Led status.
- Only Infinite chassis ID ON/OFF by software command will reflect in EWS during automatic/manual EWS sync up with BMC.
- Virtual Front Panel help should available for virtual panel module.
- At present, NMI button in VFP is disabled. It can be used in future.

6.4.3.19 Embedded Platform Debug

The Embedded Platform Debug feature supports capturing low-level diagnostic data (applicable MSRs, PCI config-space registers, and so on). This feature allows a user to export this data into a file that is retrievable by the embedded web GUI, as well as through host and remote IPMI methods, for the purpose of sending to an Intel engineer for an enhanced debugging capability. The files are compressed, encrypted, and password protected. The file is not meant to be viewable by the end user but rather to provide additional debugging capability to an Intel support engineer.

6.4.3.20 Data Center Management Interface (DCMI)

The DCMI specification is an emerging standard that is targeted to provide a simplified management interface for Internet Portal Data Center (IPDC) customers. It is expected to become a requirement for server platforms which are targeted for IPDCs. DCMI is an IPMI-based standard that builds upon a set of required IPMI standard commands by adding a set of DCMI-specific IPMI OEM commands. Intel® Server Platforms will be implementing the mandatory DCMI features in the BMC firmware (DCMI 1.1 Errata 1 compliance). Please refer to DCMI 1.1 errata 1 spec for details. Only mandatory commands will be supported. No support for optional DCMI commands. Optional power management and SEL roll over feature is not supported. DCMI Asset tag will be independent of baseboard FRU asset Tag. Please refer table DCMI Group Extension Commands for more details on DCMI commands.

6.4.3.21 Lightweight Directory Authentication Protocol (LDAP)

The Lightweight Directory Access Protocol (LDAP) is an application protocol supported by the BMC for the purpose of authentication and authorization. The BMC user connects with an LDAP server for login authentication. This is only supported for non-IPMI logins including the embedded web UI and SM-CLP. IPMI users/passwords and sessions are not supported over LDAP.

LDAP can be configured (IP address of LDAP server, port, and so on) by the BMC's Embedded Web UI. LDAP authentication and authorization is supported over the any NIC configured for system management. The BMC uses a standard Open LDAP implementation for Linux.

Only open LDAP is supported by BMC. Windows and Novel LDAP are not supported.

6.5 Advanced Management Feature Support

This section explains the advanced management features supported by the BMC firmware.

6.5.1 Enabling Advanced Management Features

The *Advanced* management features are to be delivered as part of the BMC FW image. The BMC's baseboard SPI flash contains code/data for both the *Basic* and *Advanced* features. An optional add-in card Intel® RMM4 lite is used as the activation mechanism. When the BMC FW initializes, it attempts to access the Intel® RMM4 lite. If the attempt to access Intel® RMM4 lite is successful, then the BMC activates the *Advanced* features.

Advanced manageability features are supported over all NIC ports enabled for server manageability. This includes baseboard NICs as well as the LAN channel provided by the optional Dedicated NIC add-in card.

RMM4 is comprised of two boards – RMM4 lite and the optional Dedicated Server Management NIC (DMN). If the optional Dedicated Server Management NIC is not used then the traffic can only go through the onboard Integrated BMC-shared NIC and share network bandwidth with the host system.

Table 25. Enabling Advanced Management Features

Manageability Hardware	Benefits

Intel® Integrated BMC	Comprehensive IPMI based base manageability features
Intel® Remote Management Module 4 – Lite Package contains one module – 1- Key for advance Manageability features.	No dedicated NIC for management Enables KVM and media redirection by onboard NIC
Intel® Remote Management Module 4 Package includes 2 modules – 1 - key for advance features 2 - Dedicated NIC (1Gbe) for management	Dedicated NIC for management traffic, KVM and media Redirection.

6.5.2 Keyboard, Video, Mouse (KVM) Redirection

The BMC firmware supports keyboard, video, and mouse redirection (KVM) over LAN. This feature is available remotely from the embedded web server as a Java applet. This feature is only enabled when the Intel® RMM4 lite is present. The client system must have a Java Runtime Environment (JRE) version 6.0 or later to run the KVM or media redirection applets.

The BMC supports an embedded KVM application (*Remote Console*) that can be launched from the embedded web server from a remote console. USB1.1 or USB 2.0 based mouse and keyboard redirection are supported. It is also possible to use the KVM-redirection (KVM-r) session concurrently with media-redirection (media-r). This feature allows a user to interactively use the keyboard, video, and mouse (KVM) functions of the remote server as if the user were physically at the managed server.
KVM redirection console support the following keyboard layouts: English, Dutch, French, German, Italian, Russian, and Spanish.
KVM redirection includes a “soft keyboard” function. The “soft keyboard” is used to simulate an entire keyboard that is connected to the remote system. The “soft keyboard” functionality supports the following layouts: English, Dutch, French, German, Italian, Russian, and Spanish.
The KVM-redirection feature automatically senses video resolution for best possible screen capture and provides high-performance mouse tracking and synchronization. It allows remote viewing and configuration in pre-boot POST and BIOS setup, once BIOS has initialized video.
Other attributes of this feature include:

1. Encryption of the redirected screen, keyboard, and mouse
2. Compression of the redirected screen.
3. Ability to select a mouse configuration based on the OS type.
4. supports user definable keyboard macros.

KVM redirection feature supports the following resolutions and refresh rates:

- 640x480 at 60Hz, 72Hz, 75Hz, 85Hz, 100Hz
- 800x600 at 60Hz, 72Hz, 75Hz, 85Hz
- 1024x768 at 60Hx, 72Hz, 75Hz, 85Hz
- 1280x960 at 60Hz
- 1280x1024 at 60Hz
- 1600x1200 at 60Hz
- 1920x1080 (1080p),
- 1920x1200 (WUXGA)
- 1650x1080 (WSXGA+)

6.5.2.1 Force-enter BIOS Setup

KVM redirection can present an option to force-enter BIOS Setup. This enables the system to enter F2 setup while booting which is often missed by the time the remote console redirects the video.

6.5.3 Media Redirection

The embedded web server provides a Java applet to enable remote media redirection. This may be used in conjunction with the remote KVM feature, or as a standalone applet.

The media redirection feature is intended to allow system administrators or users to mount a remote IDE or USB CD-ROM, floppy drive, or a USB flash disk as a remote device to the server. Once mounted, the remote device appears just like a local device to the server, allowing system administrators or users to install software (including operating systems), copy files, update BIOS, and so on, or boot the server from this device.

The following capabilities are supported:

- The operation of remotely mounted devices is independent of the local devices on the server. Both remote and local devices are useable in parallel.
- Either IDE (CD-ROM, floppy) or USB devices can be mounted as a remote device to the server.
- It is possible to boot all supported operating systems from the remotely mounted device and to boot from disk IMAGE (*.IMG) and CD-ROM or DVD-ROM ISO files. See the Tested/supported Operating System List for more information.
- Media redirection supports redirection for both a virtual CD device and a virtual Floppy/USB device concurrently. The CD device may be either a local CD drive or else an ISO image file; the Floppy/USB device may be either a local Floppy drive, a local USB device, or else a disk image file.
- The media redirection feature supports multiple encryption algorithms, including RC4 and AES. The actual algorithm that is used is negotiated with the client based on the client's capabilities.
- A remote media session is maintained even when the server is powered-off (in standby mode). No restart of the remote media session is required during a server reset or power on/off. An BMC reset (for example, due to an BMC reset after BMC FW update) will require the session to be re-established
- The mounted device is visible to (and useable by) managed system's OS and BIOS in both pre-boot and post-boot states.
- The mounted device shows up in the BIOS boot order and it is possible to change the BIOS boot order to boot from this remote device.
- It is possible to install an operating system on a bare metal server (no OS present) using the remotely mounted device. This may also require the use of KVM-r to configure the OS during install.

USB storage devices will appear as floppy disks over media redirection. This allows for the installation of device drivers during OS installation.

If either a virtual IDE or virtual floppy device is remotely attached during system boot, both the virtual IDE and virtual floppy are presented as bootable devices. It is not possible to present only a single-mounted device type to the system BIOS.

6.6 Intel® Intelligent Power Node Manager (NM)

Power management deals with requirements to manage processor power consumption and manage power at the platform level to meet critical business needs. Node Manager (NM) is a platform resident technology that enforces power capping and thermal-triggered power capping policies for the platform. These policies are applied by exploiting subsystem knobs (such as processor P and T states) that can be used to control power consumption. NM enables data center power management by exposing an external interface to management software through which platform policies can be specified. It also implements specific data center power management usage models such as power limiting, and thermal monitoring.

Note: Support for NM is product-specific. This section details how NM would be supported on products that provide this capability

The NM feature is implemented by a complementary architecture utilizing the ME, BMC, BIOS, and an ACPI-compliant OS. The ME provides the NM policy engine and power control/limiting functions (referred to as Node Manager or NM) while the BMC provides the external LAN link by which external management software can interact with the feature. The BIOS provides system power information utilized by the NM algorithms and also exports ACPI Source Language (ASL) code used by OS-Directed Power Management (OSPM) for negotiating processor P and T state changes for power limiting. PMBus-compliant power supplies provide the capability to monitoring input power consumption, which is necessary to support NM.

6.6.1 Hardware Requirements

NM is supported only on platforms that have the NM FW functionality loaded and enabled on the Management Engine (ME) in the SSB and that have a BMC present to support the external LAN interface to the ME. NM power limiting features requires a means for the ME to monitor input power consumption for the platform. This capability is generally provided by means of PMBus-compliant power supplies although an alternative model using a simpler SMBus power monitoring device is possible (there is potential loss in accuracy and responsiveness using non-PMBus devices). The NM SmaRT/CLST feature does specifically require PMBus-compliant power supplies as well as additional hardware on the baseboard.

6.6.2 Features

NM provides feature support for policy management, monitoring and querying, alerts and notifications, and an external interface protocol. The policy management features implement specific IT goals that can be specified as policy directives for NM. Monitoring and querying features enable tracking of power consumption. Alerts and notifications provide the foundation for automation of power management in the data center management stack. The external interface specifies the protocols that must be supported in this version of NM.

6.6.3 ME Firmware Update

On server platforms, the ME FW uses a single operational image with a limited-functionality recovery image. In order to upgrade an operational image, a boot to recovery image must be performed. Unlike on Xeon 5500/5600 based platforms, the ME FW does not support an IPMI update mechanism except for the case that the system is configured with a dual-ME (redundant) image. In order to conserve flash space, which the ME FW shares with BIOS, the systems only support a single ME image. For this case, ME update is only supported by means of BIOS performing a direct update of the flash component. The recovery image only provides the basic functionality that is required to perform the update; therefore other ME FW features are not functional therefore when the update is in progress.

6.6.4 SmaRT/CLST

The power supply optimization provided by SmaRT/CLST relies on a platform HW capability as well as ME FW support. When a PMBus-compliant power supply detects insufficient input voltage, an overcurrent condition, or an over-temperature condition, it will assert the SMBAlert# signal on the power supply SMBus (that is, the PMBus). Through the use of external gates, this results in a momentary assertion of the PROCHOT# and MEMHOT# signals to the processors, thereby throttling the processors and memory. The ME FW also sees the SMBAlert# assertion, queries the power supplies to determine the condition causing the assertion, and applies an algorithm to either release or prolong the throttling, based on the situation.

System power control modes include:

1. SmaRT: Low AC input voltage event; results in a onetime momentary throttle for each event to the maximum throttle state
2. Electrical Protection CLST: High output energy event; results in a throttling hiccup mode with fixed maximum throttle time and a fix throttle release ramp time.
3. Thermal Protection CLST: High power supply thermal event; results in a throttling hiccup mode with fixed maximum throttle time and a fix throttle release ramp time.

When the SMBAlert# signal is asserted, the fans will be gated by HW for a short period (~100ms) to reduce overall power consumption. It is expected that the interruption to the fans will be of short enough duration to avoid false lower threshold crossings for the fan tach sensors; however, this may need to be comprehended by the fan monitoring FW if it does have this side-effect.

ME FW will log an event into the SEL to indicate when the system has been throttled by the SmaRT/CLST power management feature. This is dependent on ME FW support for this sensor. Please refer ME FW EPS for SEL log details.

6.6.4.1 Dependencies on PMBus-compliant Power Supply Support

The SmaRT/CLST system feature depends on functionality present in the ME NM SKU. This feature requires power supplies that are compliant with the *PMBus Specification rev1.2*.

6.7 EU Lot 6 Mode

The European Union has set forth a stringent standby power consumption target for systems that are used as primary computing devices in office environments. Owing to the fact in office environments, pedestal servers are being used more and more as workstations and that Value servers could make their way into Home servers, this solution is being requested for some pedestal servers. HW support for EU Lot6 will only be available for specific pedestal products.

In order to meet the standby power requirements for EU Lot6 it is necessary to remove power to the BMC, along with other components, when in the S5 state. As this operational mode impacts system feature support, the user has the option of enabling and disabling this mode by the BIOS setup screen utility.

BIOS is responsible for enabling/disabling the system hardware for EU Lot6 operation. It notifies the BMC of the current state. The BMC saves the state in persistent store and uses it to control special EU Lot6 internal processing during boot, sensor monitoring, and so on as needed.

Wake-on-LAN (WOL) is not supported in EU Lot6 mode.

6.7.1 Impact to System Features

The following system features are lost or impacted when EU Lot6 mode is enabled:

- Increased boot time (~15-20s) when system is DC power cycled.
  - This is due to the fact that both the BMC and BIOS are booting at the same time when the system is powered on (to S0 state). BIOS will need to allow extra time for the BMC to initialize to the point where it can communicate with BIOS.

    Note: Even when EU Lot6 is not enabled and the system is AC cycled, this increased boot time is applicable if a user immediately attempts to power the system up (for example, pressing the power button), as in this case both the BMC and BIOS are booting at the same time

- No LAN manageability when on standby, and therefore no remote OOB power on by BMC.
- No support for SOL or KVM for monitoring the entire boot process.
  - Since BMC is initializing at the same time as BIOS, it will not be possible to have an SOL or KVM session established from the beginning of the system boot.
- FP status LED will behave differently (it will be off when on standby) rather than showing fault conditions present at the time the system was powered down.
- No beep code due to uninstalled CPU.
- No monitoring of any sensors when on standby.
- No detection/logging of any ThermTrip faults.
  - These result as the system is shutdown by HW so BMC will not be available to detect that they occurred.
- Sensor monitoring after DC power-on will be delayed by the time it takes BMC to initialize its sensor subsystem (~15 to 20s), possibly losing SEL events or failing to provide correct FP LED status LED indication.

  Note: This delay occurs on each AC cycle even when EU Lot6 mode is disabled
- Chassis intrusion not detected when in standby

7. Intel® Server Board S2600CP Connector/Header Locations and Pin-outs

7.1 Power Connectors

7.1.1 Main Power Connector

Main server board power is supplied by one 12-pin power connector. The connector is labeled as "MAIN PWR" on the left bottom of the server board. The following tables provide the pin-out for "MAIN PWR" connector.

Table 26. Main Power Connector Pin-out

Pin	Signal name	Pin	Signal name
1	P3V3	13	P3V3
2	P3V3	14	N12V
3	GND	15	GND
4	P5V	16	FM_PS_EN_PSU_N
5	GND	17	GND
6	P5V	18	GND
7	GND	19	GND
8	PWRGD_PS_PWROK_PSU_R1	20	NC_PS_RES_TP
9	P5V_STBY_PSU	21	P5V
10	P12V	22	P5V
11	P12V	23	P5V
12	P3V3	24	GND

7.1.2 CPU Power Connectors

On the server board are two white 8-pin CPU power connectors labeled "CPU_1 PWR" and "CPU_2 PWR". The following table provides the pin-out for both connectors.

Table 27. CPU_1 Power Connector Pin-out

Pin	Signal name	Pin	Signal name
1	GND	5	P12V1
2	GND	6	P12V1
3	GND	7	P12V3A
4	GND	8	P12V3A

Table 28. CPU_2 Power Connector Pin-out

Pin	Signal name	Pin	Signal name
1	GND	5	P12V2
2	GND	6	P12V2
3	GND	7	P12V3B
4	GND	8	P12V3B

7.2 Front Panel Header and Connectors

The server board includes several connectors that provide various possible front panel options. This section provides a functional description and pin-out for each connector.

7.2.1 Front Panel Header

Included on the left edge of the server board is a 30-pin header consists of a 24-pin SSI compatible front panel header and a 4-pin header to support optional NIC3/4 LEDs. The 24-pin SSI front panel header provides various front panel features including:

- Power/Sleep Button
- System ID Button
- NMI Button
- NIC Activity LEDs
- Hard Drive Activity LEDs
- System Status LED
- System ID LED

The following table provides the pin-out for this 30-pin header.

Table 29. Front Panel Header Pin-out

Pin	Signal name	Pin	Signal name
1	P3V3_AUX	2	P3V3_AUX
3	Key	4	P5V_STBY
5	FP_PWR_LED_BUF_N	6	FP_ID_LED_BUF_N
7	P3V3	8	FP_LED_STATUS_GREEN_BUF_N
9	LED_HDD_ACTIVITY_N	10	FP_LED_STATUS_AMBER_BUF_N
11	FP_PWR_BTN_N	12	LED_NIC_LINK0_ACT_BUF_N
13	GND	14	LED_NIC_LINK0_LNKUP_BUF_N
15	FP_RST_BTN_N	16	SMB_SENSOR_3V3STBY_DATA
17	GND	18	SMB_SENSOR_3V3STBY_CLK
19	FP_ID_BTN_N	20	FP_CHASSIS_INTRUSION
21	PU_FM_SIO_TEMP_SENSOR	22	LED_NIC_LINK1_ACT_BUF_N
23	FP_NMI_BTN_N	24	LED_NIC_LINK1_LNKUP_BUF_N
25	<Empty Pin>	26	<Empty Pin>
27	LED_NIC_LINK2_ACT_FP_N	28	LED_NIC_LINK3_ACT_FP_N
29	LED_NIC_LINK2_LNKUP_FP_N	30	LED_NIC_LINK3_LNKUP_FP_N

7.2.2 Front Panel USB Connector

The server board includes a 10-pin connector, that when cabled, can provide up to two USB ports to a front panel. The following table provides the connector pin-out.

Table 30. Front Panel USB Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	P5V_USB_FP	2	P5V_USB_FP
3	USB2_P13_F_DN	4	USB2_P11_F_DN
5	USB2_P13_F_DP	6	USB2_P11_F_DP
7	GND	8	GND
9	KEY	10	NA

7.2.3 Local Control Panel Connector

The server board includes a 7-pin connector that is used when the system is configured with the Intel Local Control Panel with LCD support. The following table provides the pin-out for this connector.

Table 31. Local Front Panel Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	SMB_SENSOR_3V3STBY_DATA	2	GND
3	SMB_SENSOR_3V3STBY_CLK	4	P3V3_AUX
5	FM_LCP_ENTER_N	6	FM_LCP_LEFT_N
7	FM_LCP_RIGHT_N		

7.3 On Board Storage Connectors

The server board provides connectors for support of several storage device options. This section provides a functional overview and pin-out of each connector.

7.3.1 SATA Connectors: 6Gbps

The server board includes two white single port SATA only connectors capable of transfer rates of up to 6Gb/s. The following table provides the pin-out for both connectors.

Table 32. SATA 6Gbps Connector Pin-out

Pin	Signal Name
1	GND
2	SATA_TX_P
3	SATA_TX_N
4	GND
5	SATA_RX_N
6	SATA_RX_P
7	GND

7.3.2 SATA Connectors: 3Gbps

The server board includes four black single port SATA only connectors capable of transfer rates of up to 3Gb/s. The following table provides the pin-out for both connectors.

Table 33. SATA 3Gbps Connector Pin-out

Pin	Signal Name
1	GND
2	SATA_TX_P
3	SATA_TX_N
4	GND
5	SATA_RX_N
6	SATA_RX_P
7	GND

7.3.3 SATA SGPIO Connector

SGPIO uses a 5pin header, this is to incorporate a ground conductor as an SI improvement over previous generation products and based on measurement data indicating add the ground is strongly recommended. The 5pin connector will be consistent with other HSBPs, in this way cable commonality is improved.

Table 34. SATA SGPIO Connector Pin-out

Pin	Signal Name
1	SCLK
2	SLOAD
3	GND
4	SDATAOUT0
5	SDATAOUT1

7.3.4 SAS Connectors

The server board includes eight SAS/SATA connectors. By default, only the connectors labeled from “SAS_0” to “SAS_3” are enabled and support transfer rates of up to 3Gb/s. The connectors labeled from “SAS_4” to “SAS_7” are only enabled when an optional Intel® RAID C600 Upgrade Key is installed. The following tables provide the pin-out for each connector.

Table 35. SAS/SATA Connector Pin-out

Pin	Signal Name
1	GND
2	SATA_TX_P
3	SATA_TX_N
4	GND
5	SATA_RX_N
6	SATA_RX_P
7	GND

7.3.5 SAS SGPIO Connectors

Table 36. SAS SGPIO Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	CLOCK	2	LOAD
3	GND	4	DATAOUT
5	DATAIN		

7.3.6 Intel® RAID C600 Upgrade Key Connector

The server board provides one connector to support Intel® RAID C600 Upgrade Key. The Intel® RAID C600 Upgrade Key is a small PCB board that enables different versions of RAID 5 software stack and/or upgrade from SATA to SAS storage functionality. The pin configuration of connector is identical and defined in the following table.

Table 37. Intel® RAID C600 Upgrade Key Connector Pin-out

Pin	Signal Name
1	GND
2	FM_PBG_DYN_SKU_KEY
3	GND
4	FM_SSB_SAS_SATA_RAID_KEY

7.3.7 HSBP_I2C Header

Table 38. HSBP_I2C Header Pin-out

Pin	Signal Name
1	SMB_HSBP_3V3STBY_DATA
2	GND
3	SMB_HSBP_3V3STBY_CLK

7.3.8 HDD LED Header

The server board includes a 2-pin hard drive activity LED header used with some SAS/SATA controller add-in cards. The header has the following pin-out.

Table 39. HDD LED Header Pin-out

Pin	Signal Name	Pin	Signal Name
1	LED_HDD_ACT_N	2	NA

7.3.9 Internal Type- A USB Connector

The server board includes one internal Type-A USB connector. The following table provides the pin-out for this connector.

Table 40. Type-A USB Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	P5V	2	USB2_P2_F_DN
3	USB2_P2_F_DP	4	GND

7.3.10 Internal eUSB SSD Header

The server board includes one 10-pin internal eUSB header with an intended usage of supporting USB SSD devices. The following table provides the pin-out for this connector.

Table 41. eUSB SSD Header Pin-out

Pin	Signal Name	Pin	Signal Name
1	5V	2	NC
3	USB2_PCH_P12_DN	4	NC
5	USB2_PCH_P12_DP	6	NC
7	GND	8	NC
9	Key	10	LED_HDD_ACT_ZEPHER_N

7.4 Management and Security Connectors

7.4.1 RMM4_Lite Connector

A 7-pin Intel® RMM4 Lite connector is included on the server board to support the optional Intel® Remote Management Module 4. There is no support for third-party management cards on this server board.

Table 42. RMM4_Lite Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	P3V3_AUX	2	DI
3	KEY	4	CLK
5	DO	6	GND
7	CS_N	8	GND

7.4.2 RMM4_NIC Connector

Table 43. RMM4_NIC Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	3V3_AUX	2	MDIO
3	3V3_AUX	4	MDC
5	GND	6	TXD_0
7	GND	8	TXD_1
9	GND	10	TXD_2
11	GND	12	TXD_3
13	GND	14	TX_CTL
15	GND	16	RX_CTL
17	GND	18	RXD_0
19	GND	20	RXD_1
21	GND	22	RXD_2
23	GND	24	RXD_3
25	GND	26	TX_CLK
27	GND	28	RX_CLK
29	GND	30	PRESENT#

7.4.3 TPM Connector

Table 44. TPM Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	Key	2	LPC_LAD<1>
3	LPC_LAD<0>	4	GND
5	IRQ_SERIAL	6	LPC_FRAME_N
7	P3V3	8	GND
9	RST_IBMC_NIC_N_R2	10	CLK_33M_TPM
11	LPC_LAD<3>	12	GND
13	GND	14	LPC_LAD<2>

7.4.4 PMBUS Connector

Table 45. PMBUS Connector Pin-out

Pin	Signal name
1	SMB_PMBUS_CLK_R
2	SMB_PMBUS_DATA_R
3	IRQ_SML1_PMBUS_ALERT_RC_N
4	GND

Pin	Signal name
5	P3V3

7.4.5 Chassis Intrusion Header

The server board includes a 2-pin chassis intrusion header which can be used when the chassis is configured with a chassis intrusion switch. The header has the following pin-out.

Table 46. Chassis Intrusion Header Pin-out

Header State	Description
Pins 1 and 2 closed	FM_INTRUDER_HDR_N is pulled HIGH. Chassis cover is closed.
Pins 1 and 2 open	FM_INTRUDER_HDR_N is pulled LOW. Chassis cover is removed.

7.4.6 IPMB Connector

Table 47. IPMB Connector Pin-out

Pin	Signal Name
1	SMB_IPMB_5VSTBY_DATA
2	GND
3	SMB_IPMB_5VSTBY_CLK
4	P5V_STBY

7.5 FAN Connectors

The server board provides support for nine fans. Seven of them are system cooling fans, two of them are CPU fans.

7.5.1 System FAN Connectors

The six system cooling fan connectors near the front edge of the board are 6-Pin connectors; the one system cooling fan near edge of the board is a 4-Pin connectors. Following table provides the pin-out for all system fan connectors.

Table 48. 6-pin System FAN Connector Pin-out

Pin	Signal Name
1	GND
2	12V
3	TACH
4	PWM
5	PRSNT
6	FAULT

Table 49. 4-pin System FAN Connector Pin-out

Pin	Signal Name
1	GND
2	12V
3	TACH
4	PWM

7.5.2 CPU FAN Connector

The two CPU fan connectors are 4-pin fan connectors. Following table provides the pin-out for CPU fan connectors.

Table 50. CPU FAN Connector Pin-out

Pin	Signal Name
1	GND
2	12V
3	TACH
4	PWM

7.6 Serial Port and Video Connectors

The server board includes two serial port connectors.

7.6.1 Serial Port A Connector (DB9)

Serial-A is an external RJ45 type connector and has the following pin-out configuration.

Table 51. Serial Port A Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	SPA_DCD	2	SPA_SIN
3	SPA_SOUT_N	4	SPA_DTR
5	GND	6	SPA_DSR
7	SPA_RTS	8	SPA_CTS
9	SPA_RI		

7.6.2 Serial Port B Connector

Serial-B is an internal 10-pin DH-10 connector and has the following pin-out.

Table 52. Serial Port B Connector Pin-out

Pin	Signal Name	Pin	Signal Name
1	SPA_DCD	2	SPA_DSR
3	SPA_SIN	4	SPA_RTS
5	SPA_SOUT_N	6	SPA_CTS
7	SPA_DTR	8	SPA_RI
9	GND		

7.6.3 Video Connector

The following table details the pin-out definition of the external VGA connector.

Table 53. Video Connector Pin-out details

Pin	Signal Name
1	CRT_RED
2	CRT_GREEN
3	CRT_BLUE
4	N/C
5	GND
6	GND
7	GND

8	GND
9	P5V
10	GND
11	NC
12	CRT_DDCDATA
13	CRT_HSYNC
14	CRT_VSYNC
15	CRT_DDCCLK

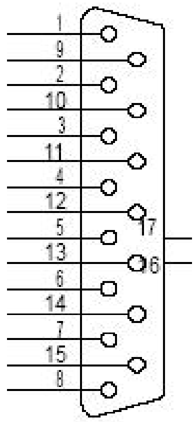


Figure 30. Video Connector Pin-out

Note: Intel Corporation server boards support peripheral components and can contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel's own chassis are designed and tested to meet the intended thermal requirements of these components when the fully integrated system is used together. It is the responsibility of the system integrator that chooses not to use Intel® developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

8. Intel® Server Board S2600CP Jumper Blocks

The server boards have several 3-pin jumper blocks that you can use to configure, protect, or recover specific features of the server boards.

The following symbol identifies Pin 1 on each jumper block on the silkscreen: ▼

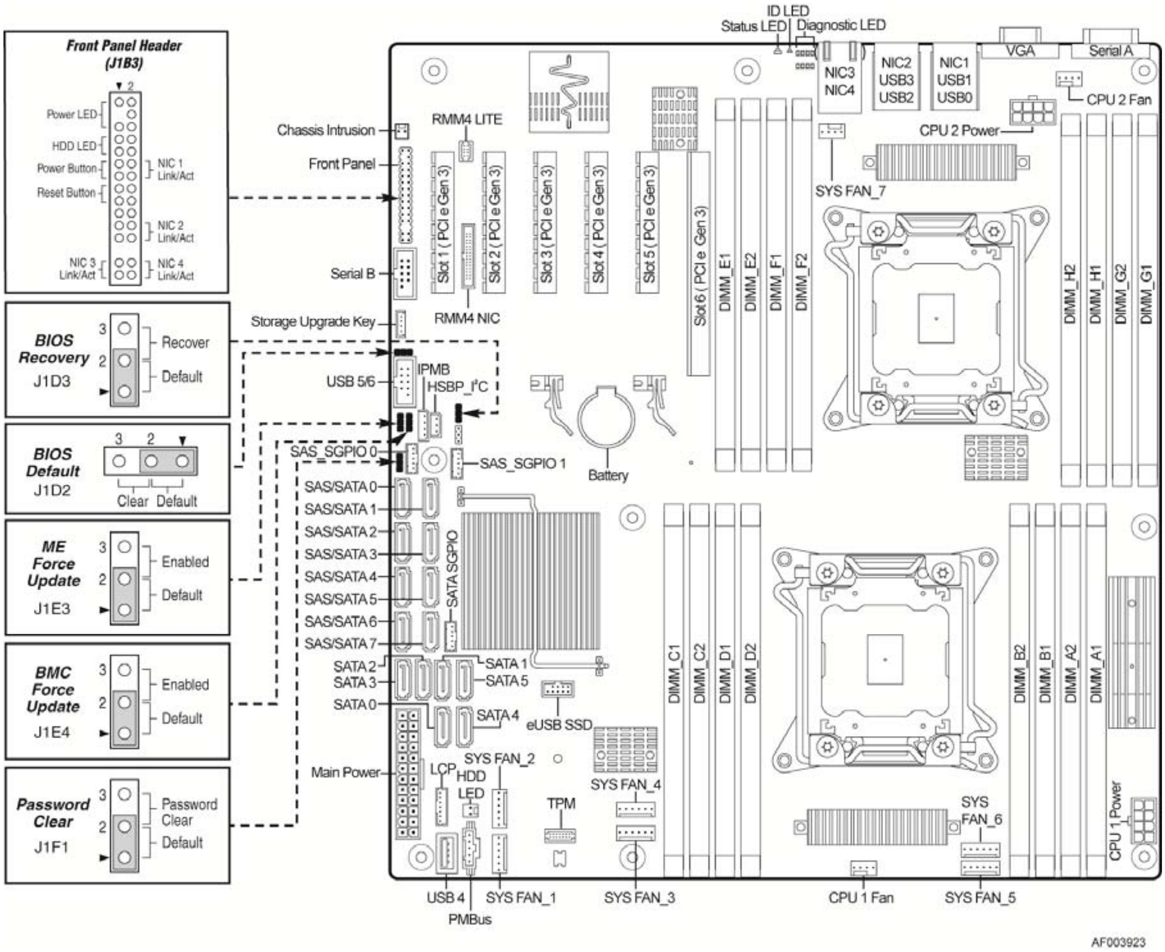


Figure 31. Jumper Blocks (J1D3, J1D2, J1E3, J1E4, J1F1)

Table 54. Server Board Jumpers (J1D3, J1D2, J1E3, J1E4, J1F1)

Jumper Name	Pins	System Results
J1D3: BIOS Recovery	1-2	Pins 1-2 should be connected for normal system operation. **(Default)**
	2-3	The main system BIOS does not boot with pins 2-3 connected. The system only boots from EFI-bootable recovery media with a recovery BIOS image present.
J1D2: BIOS Default (that is, CMOS Clear)	1-2	These pins should have a jumper in place for normal system operation. **(Default)**
	2-3	If pins 2-3 are connected when AC power unplugged, the CMOS settings clear in 5 seconds. Pins 2-3 should not be connected for normal system operation.
J1E3: ME Force Update	1-2	ME Firmware Force Update Mode – Disabled **(Default)**
	2-3	ME Firmware Force Update Mode – Enabled
J1E4: BMC	1-2	BMC Firmware Force Update Mode – Disabled **(Default)**

Jumper Name	Pins	System Results
Force Update	2-3	BMC Firmware Force Update Mode – Enabled
J1F1: Password Clear	1-2	These pins should have a jumper in place for normal system operation. **(Default)**
	2-3	To clear administrator and user passwords, power on the system with pins 2-3 connected. The administrator and user passwords clear in 5-10 seconds after power on. Pins 2-3 should not be connected for normal system operation.

8.1 BIOS Default (a.k.a CMOS Clear) and Password Reset Usage Procedure

The BIOS Default (that is, CMOS Clear) and Password Reset recovery features are designed such that the desired operation can be achieved with minimal system downtime. The usage procedure for these two features has changed from previous generation Intel server boards. The following procedure outlines the new usage model.

8.1.1 Set BIOS to default (a.k.a Clearing the CMOS)

To clear the CMOS, perform the following steps:

1. Power down the server. Do not unplug the power cord.
2. Open the server chassis. For instructions, see your server chassis documentation.
3. Move jumper from the default operating position (covering pins 1 and 2) to the reset/clear position (covering pins 2 and 3).
4. Wait five seconds.
5. Remove AC power.
6. Move the jumper back to the default position (covering pins 1 and 2).
7. Close the server chassis.
8. Power up the server.

The CMOS is now cleared and can be reset by going into the BIOS setup.

Note: Removing AC power before performing the CMOS clear operation causes the system to automatically power up and immediately power down, after the procedure is followed and AC power is re-applied. If this happens, remove the AC power cord again, wait 30 seconds, and re-install the AC power cord. Power up the system and proceed to the <F2> BIOS Setup utility to reset the preferred settings.

8.1.2 Clearing the Password

To clear the password, perform the following steps:

1. Power down the server. Do not unplug the power cord.
2. Open the chassis. For instructions, see your server chassis documentation.
3. Move jumper from the default operating position (covering pins 1 and 2) to the password clear position (covering pins 2 and 3).
4. Close the server chassis.
5. Power up the server and wait 10 seconds or until POST completes.
6. Power down the server.

7. Open the chassis and move the jumper back to the default position (covering pins 1 and 2).
8. Close the server chassis.
9. Power up the server.

The password is now cleared and can be reset by going into the BIOS setup.

8.2 Integrated BMC Force Update Procedure

When performing the standard Integrated BMC firmware update procedure, the update utility places the Integrated BMC into an update mode, allowing the firmware to load safely onto the flash device. In the unlikely event the Integrated BMC firmware update process fails due to the Integrated BMC not being in the proper update state, the server board provides an Integrated BMC Force Update jumper, which forces the Integrated BMC into the proper update state. The following procedure should be completed in the event the standard Integrated BMC firmware update process fails.

1. Power down and remove the AC power cord.
2. Open the server chassis. For instructions, see your server chassis documentation.
3. Move jumper from the default operating position (covering pins 1 and 2) to the enabled position (covering pins 2 and 3).
4. Close the server chassis.
5. Reconnect the AC cord and power up the server.
6. Perform the Integrated BMC firmware update procedure as documented in the README.TXT file that is included in the given Integrated BMC firmware update package. After successful completion of the firmware update process, the firmware update utility may generate an error stating that the Integrated BMC is still in update mode.
7. Power down and remove the AC power cord.
8. Open the server chassis.
9. Move jumper from the enabled position (covering pins 2 and 3) to the disabled position (covering pins 1 and 2).
10. Close the server chassis.
11. Reconnect the AC cord and power up the server.

Note: Normal Integrated BMC functionality is disabled with the Force Integrated BMC Update jumper set to the enabled position. The server should never be run with the Integrated BMC Force Update jumper set in this position. This jumper setting should only be used when the standard firmware update process fails. This jumper should remain in the default/disabled position when the server is running normally.

8.3 ME Force Update Jumper

When performing the standard ME force update procedure, the update utility places the ME into an update mode, allowing the ME to load safely onto the flash device. In the unlikely event ME firmware update process fails due to ME not being in the proper update state, the server board provides an Integrated BMC Force Update jumper, which forces the ME into the proper update state. The following procedure should be completed in the event the standard ME firmware update process fails.

1. Power down and remove the AC power cord.
2. Open the server chassis. For instructions, see your server chassis documentation.
3. Move jumper from the default operating position (covering pins 1 and 2) to the enabled position (covering pins 2 and 3).
4. Close the server chassis.
5. Reconnect the AC cord and power up the server.
6. Perform the ME firmware update procedure as documented in the README.TXT file that is included in the given ME firmware update package (same package as BIOS).
7. Power down and remove the AC power cord.
8. Open the server chassis.
9. Move jumper from the enabled position (covering pins 2 and 3) to the disabled position (covering pins 1 and 2).
10. Close the server chassis.
11. Reconnect the AC cord and power up the server.

8.4 BIOS Recovery Jumper

The following procedure boots the recovery BIOS and flashes the normal BIOS:

1. Turn off the system power.
2. Move the BIOS recovery jumper to the recovery state.
3. Insert a bootable BIOS recovery media containing the new BIOS image files.
4. Turn on the system power.

The BIOS POST screen will appear displaying the progress, and the system will boot to the EFI shell. The EFI shell then executes the Startup.nsh batch file to start the flash update process. The user should then switch off the power and return the recovery jumper to its normal position. The user should not interrupt the BIOS POST on the first boot after recovery.

When the flash update completes:

1. Remove the recovery media.
2. Turn off the system power.
3. Restore the jumper to its original position.
4. Turn on the system power.
5. Re-flash any custom blocks, such as user binary or language blocks.

The system should now boot using the updated system BIOS.

9. Intel® Light Guided Diagnostics

Both server boards have several onboard diagnostic LEDs to assist in troubleshooting board-level issues. This section provides a description of the location and function of each LED on the server boards.

9.1 5-volt Stand-by LED

Several server management features of these server boards require a 5-V stand-by voltage supplied from the power supply. The features and components that require this voltage must be present when the system is "power-down". The LED is illuminated when AC power is applied to the platform and 5-V stand-by voltage is supplied to the server board by the power supply.

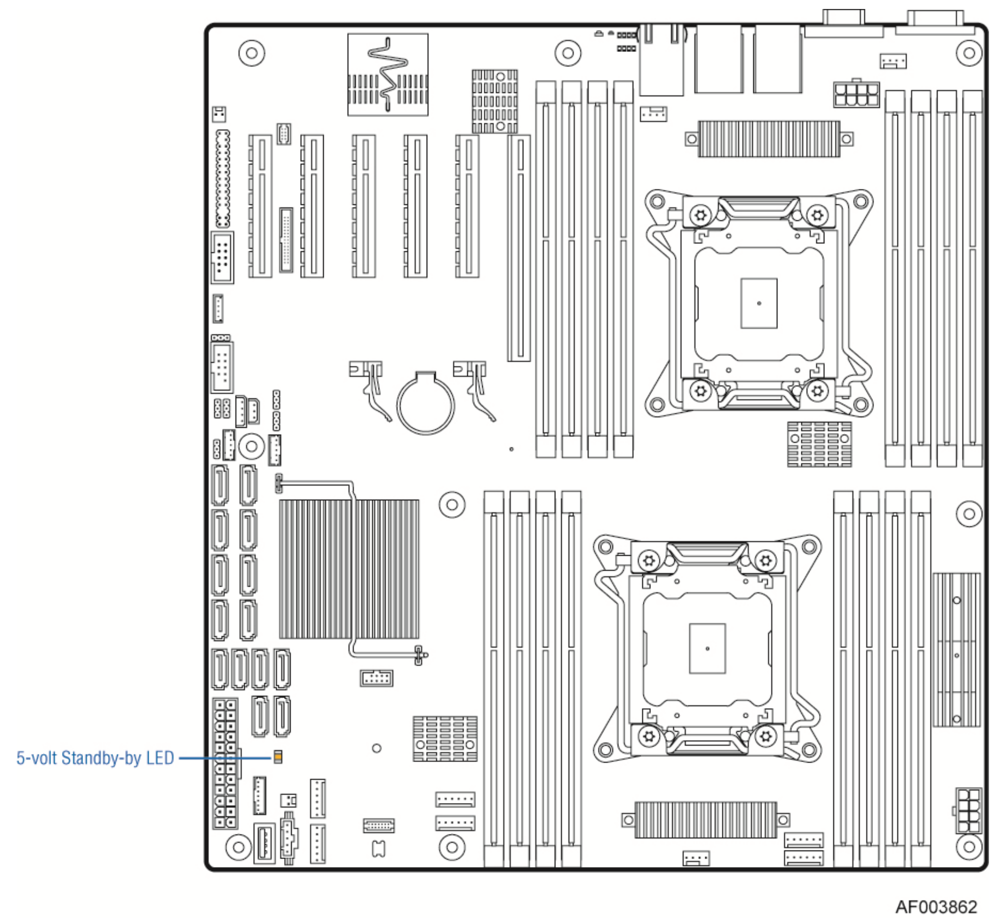


Figure 32. 5-volt Stand-by Status LED Location

9.2 Fan Fault LED's

Fan fault LEDs are present for the two CPU fans and the one rear system fan. The fan fault LEDs illuminate when the corresponding fan has fault.

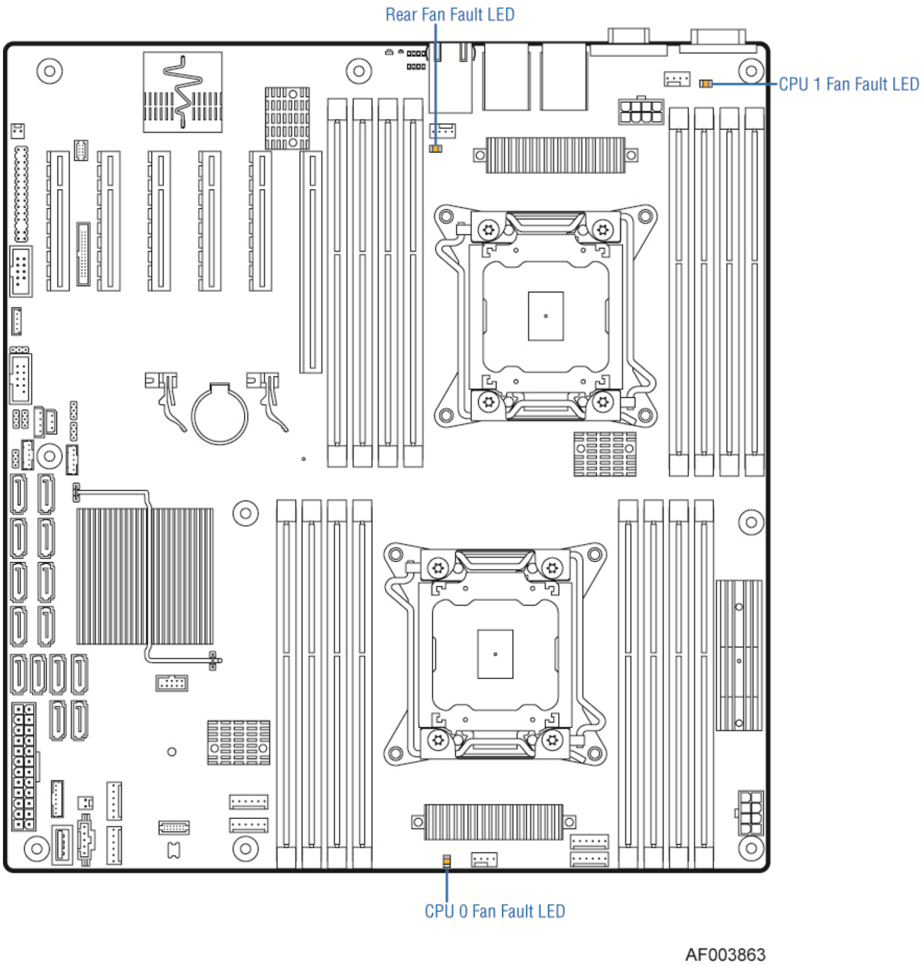


Figure 33. Fan Fault LED's Location

9.3 DIMM Fault LEDs

The server board provide memory fault LED for each DIMM socket. These LEDs are located as shown in the following figure. The DIMM fault LED illuminates when the corresponding DIMM slot has memory installed and a memory error occurs.

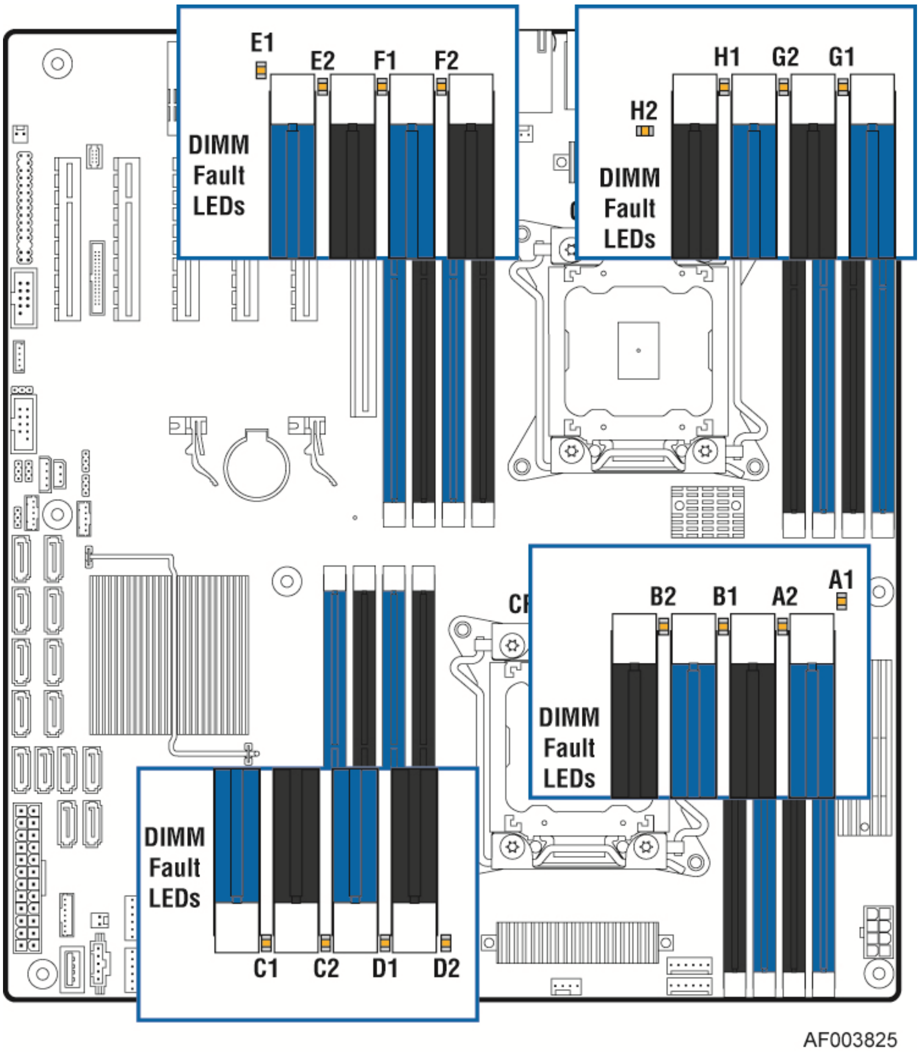
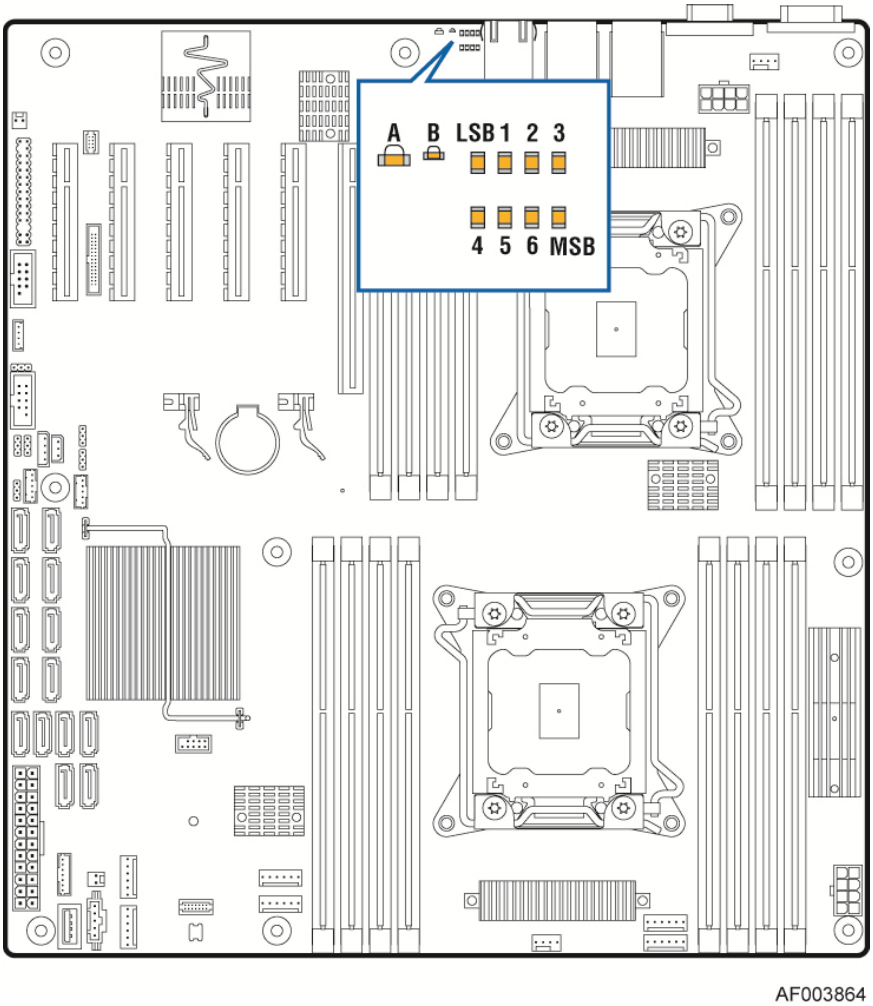


Figure 34. DIMM Fault LED's Location

9.4 System ID LED, System Status LED and POST Code Diagnostic LEDs

The server boards provide LEDs for system ID, system status and POST code. These LEDs are located in the rear I/O area of the server board as shown in the following figure.



Callout	Description
A	System Status LED
B	System ID LED
LSB 1 2 3 4 5 6 MSB	POST Code Diagnostic LEDs

Figure 35. Location of System Status, System ID and POST Code Diagnostic LEDs

9.4.1 System ID LED

- You can illuminate the blue System ID LED using either of the following two mechanisms:
  - By pressing the System ID Button on the system front control panel, the ID LED displays a solid blue color until the button is pressed again.
  - By issuing the appropriate hex IPMI "Chassis Identify" value, the ID LED will either blink blue for 15 seconds and turn off or will blink indefinitely until the appropriate hex IPMI Chassis Identify value is issue to turn it off.

9.4.2 System Status LED

The bi-color (green/amber) System Status LED operates as follows:

Table 55. System Status LED

Color	State	Criticality	Description
Green	Solid on	Ok	Indicates that the System Status is 'Healthy'. The system is not exhibiting any errors. AC power is present and BMC has booted and manageability functionality is up and running.
Green	~1 Hz blink	Degraded	System degraded: 1. Redundancy loss such as power-supply or fan. Applies only if the associated platform sub-system has redundancy capabilities. 2. Fan warning or failure when the number of fully operational fans is more than minimum number needed to cool the system. 3. Non-critical threshold crossed – Temperature (including HSBP temp), voltage, input power to power supply, output current for main power rail from power supply and Processor Thermal Control (Therm Ctrl) sensors. 4. Power supply predictive failure occurred while redundant power supply configuration was present. 5. Unable to use all of the installed memory (more than 1 DIMM installed). 6. Correctable Errors over a threshold and migrating to a spare DIMM (memory sparing). This indicates that the user no longer has spared DIMMs indicating a redundancy lost condition. Corresponding DIMM LED lit. 7. In mirrored configuration, when memory mirroring takes place and system loses memory redundancy. 8. Battery failure. 9. BMC executing in uBoot. (Indicated by Chassis ID blinking at Blinking at 3Hz). System in degraded state (no manageability). BMC uBoot is running but has not transferred control to BMC Linux. Server will be in this state 6-8 seconds after BMC reset while it pulls the Linux image into flash 10. BMC booting Linux. (Indicated by Chassis ID solid ON). System in degraded state (no manageability). Control has been passed from BMC uBoot to BMC Linux itself. It will be in this state for ~10-~20 seconds. 11. BMC Watchdog has reset the BMC. 12. Power Unit sensor offset for configuration error is asserted. 13. HDD HSC is off-line or degraded.
Amber	~1 Hz blink	Non-critical	Non-fatal alarm – system is likely to fail: 1. Critical threshold crossed – Voltage, temperature (including HSBP temp), input power to power supply, output current for main power rail from power supply and PROCHOT (Therm Ctrl) sensors. 2. VRD Hot asserted. 3. Minimum number of fans to cool the system not present or failed. 4. Hard drive fault. 5. Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies present). 6. In non-sparing and non-mirroring mode if the threshold of correctable errors is crossed within the window.

Color	State	Criticality	Description
Amber	Solid on	Critical, non-recoverable	Fatal alarm – system has failed or shutdown: 1. CPU CATERR signal asserted. 2. MSID mismatch detected (CATERR also asserts for this case). 3. CPU 1 is missing. 4. CPU ThermalTrip. 5. No power good – power fault. 6. DIMM failure when there is only 1 DIMM present and hence no good memory present. 7. Runtime memory uncorrectable error in non-redundant mode[1]. 8. DIMM Thermal Trip or equivalent. 9. SSB Thermal Trip or equivalent. 10. CPU ERR2 signal asserted. 11. BMC\Video memory test failed. (Chassis ID shows blue/solid-on for this condition). 12. Both uBoot BMC FW images are bad. (Chassis ID shows blue/solid-on for this condition). 13. 240VA fault
Off	N/A	Not ready	AC power off

Note:
* When the server is powered down (transitions to the DC-off state or S5), the BMC is still on standby power and retains the sensor and front panel status LED state established before the power-down event. If the system status is normal when the system is powered down (the LED is in a solid green state), the system status LED is off.

9.4.3 POST Code Diagnostic LEDs

During the system boot process, the BIOS executes a number of platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the given POST code to the POST code diagnostic LED's on the back edge of the server boards. To assist in troubleshooting a system hang during the POST process, you can use the diagnostic LEDs to identify the last POST process executed.

Table 56. POST Code Diagnostic LEDs

A. Diagnostic LED #7 (MSB LED)	E. Diagnostic LED #3
B. Diagnostic LED #6	F. Diagnostic LED #2
C. Diagnostic LED #5	G. Diagnostic LED #1
D. Diagnostic LED #4	H. Diagnostic LED #0 (LSB LED)

10. Intel® Server System P4000CP Front Control Panel and Back Panel

Intel® Server System P4000CP family include a Front Control Panel on the front of the system providing push button system controls, LED indicators for several system features and additional system I/O features. The front panel is identical across different options of Intel® Server System P4000CP family. Intel® Server System P4000CP family provide two different back panel, supporting 550-W fixed power supply and 750-W redundant power supply. This section describes the features and functions of the front panel and back panel.

10.1 Front Control Panel Overview

This Front Control Panel conforms to SSI specification with one exception that up to 4 LAN act/link LEDs are supported. The common front panel can support either the standard SSI 2x12 cable interconnect (2 LAN ports) or an Intel customized 2x15 cable interconnect (4 LAN ports).

The Front Control Panel has the following features:

- Power button with integrated power LED (green)
- System ID with integrated ID LED (blue)
- System Status LED (green/amber)
- System Reset button
- HDD activity LED
- 4 NIC activity/link LEDs
- NMI button
- Two USB ports

10.1.1 Front Control Panel LED/Button Functionality

The following figure shows the layout of Front Control Panel:

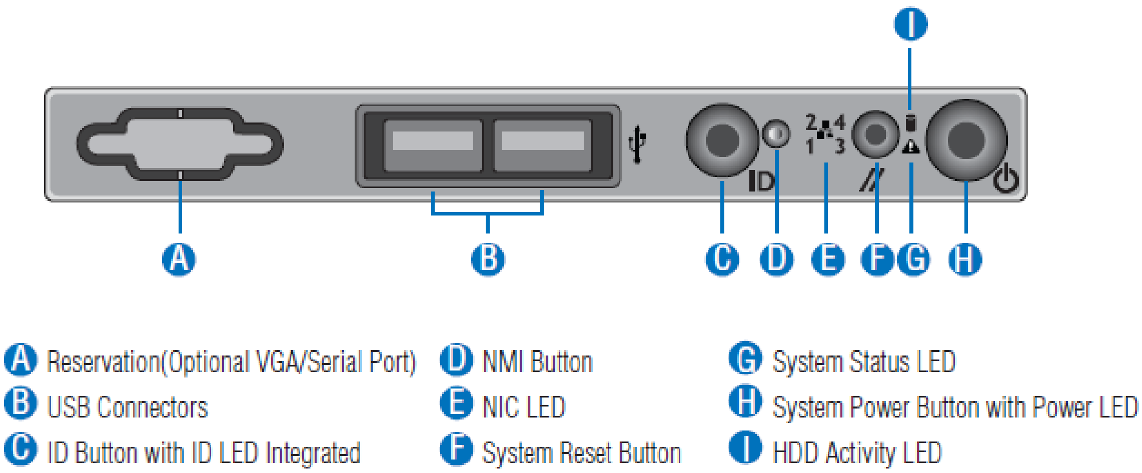


Figure 36. Front Control Panel LED/Button Arragement

ID Button with integrated ID LED – Toggles the integrated ID LED and the Blue server board ID LED on and off. The ID LED is used to identify the system for maintenance when installed in a rack of similar server systems. The ID LED can also be toggled on and off remotely using the IPMI "Chassis Identify" command which will cause the LED to blink for 15 seconds.

NMI Button – When the NMI button is pressed, it puts the server in a halt state and issues a non-maskable interrupt (NMI). This can be useful when performing diagnostics for a given issue where a memory download is necessary to help determine the cause of the problem. To prevent an inadvertent system halt, the actual NMI button is located behind the Front Control Panel faceplate where it is only accessible with the use of a small tipped tool like a pin or paper clip.

Network Activity LEDs (NIC LED) – The Front Control Panel includes an activity LED indicator for each on-board Network Interface Controller (NIC). When a network link is detected, the LED will turn on solid. The LED will blink once network activity occurs at a rate that is consistent with the amount of network activity that is occurring.

System Reset Button – When pressed, this button will reboot and re-initialize the system.

System Status LED – The System Status LED is a bi-color (Green/Amber) indicator that shows the current health of the server system. The system provides two locations for this feature; one is located on the Front Control Panel, the other is located on the back edge of the server board, viewable from the back of the system. Both LEDs are tied together and will show the same state. The System Status LED states are driven by the on-board platform management sub-system.

System Power Button with power LED – Toggles the system power on and off. This button also functions as a sleep button if enabled by an ACPI compliant operating system. Pressing this button will send a signal to the iBMC, which will either power on or power off the system. The integrated LED is a single color (Green) and is capable of supporting different indicator states as defined in the following table.

Table 57. Power/Sleep LED Functional States

State	Power Mode	LED	Description
Power-off	Non-ACPI	Off	System power is off, and the BIOS has not initialized the chipset.
Power-on	Non-ACPI	On	System power is on
S5	ACPI	Off	Mechanical is off, and the operating system has not saved any context to the hard disk.
S4	ACPI	Off	Mechanical is off. The operating system has saved context to the hard disk.
S3-S1	ACPI	Slow blink[1]	DC power is still on. The operating system has saved context and gone into a level of low-power state.
S0	ACPI	Steady on	System and the operating system are up and running.

HDD Activity LED - The drive activity LED on the front panel indicates drive activity from the on-board hard disk controllers. The server board also provides a header giving access to this LED for add-in controllers.

USB Ports – In addition, the front panel provides two USB ports. The USB ports are cabled to the 2x5 connector on the server board.

10.1.2 Front Control Panel LED Status

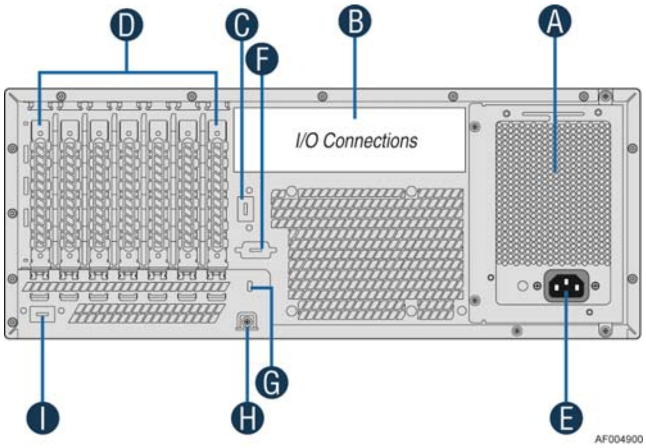
The following table provides a description of each LED status.

Table 58. Front Control Panel LED Status

LED	Color	Condition	What It Means
Power/Sleep	Green	On	Power on or S0 sleep.
	Green	Blink	S1 sleep or S3 standby only for workstation baseboards.
		Off	Off (also sleep S4/S5 modes).
Status	Green	On	System ready/No alarm.
	Green	Blink	System ready, but degraded: redundancy lost such as PS or fan failure; non-critical temp/voltage threshold; battery failure; or predictive PS failure.
	Amber	On	Critical alarm: Voltage, thermal, or power fault; CPU missing; insufficient power unit redundancy resource offset asserted.
	Amber	Blink	Non-Critical failure: Critical temp/voltage threshold; VDR hot asserted; min number fans not present or failed.
		Off	AC power off: System unplugged. AC power on: System powered off and in standby, no prior degraded/non-critical/critical state.
Global HDD Activity	Green	Blink	HDD access.
		Off	No access and no fault.
LAN 1-4 Activity/Link	Green	On	LAN link
	Green	Blink	LAN access.
		Off	Idle.
Chassis Identification	Blue	On	Front panel chassis ID button pressed.
	Blue	Blink	Unit selected for identification by software.
		Off	No identification.

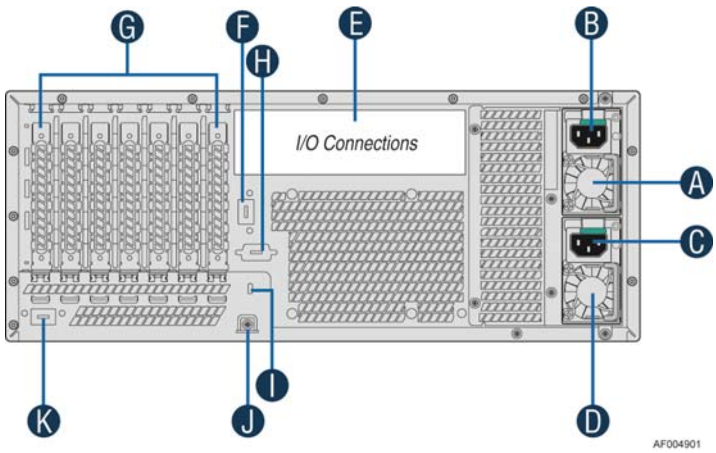
10.2 Back Panel Overview

The following figure shows the layout of Back Panel with 550-W fixed power supply and 750-W redundant power supplies.



A	Power Supply	F	Serial-B Port (Optional)
B	IO Connectors	G	Kensington* Cable Lock Mounting Hole
C	RMM4 NIC Port (Optional)	H	Padlock Loop
D	Add in PCI-e cards	I	RMM4 NIC Port (Optional)
E	Power Connector		

Figure 37. Back Panel Layout with 550-W Fixed PSU



A	Power Supply	G	Add in PCI-e cards
B	Power Connector	H	Serial-B Port (Optional)
C	Power Connector	I	Kensington* Cable Lock Mounting Hole
D	Power Supply	J	Padlock Loop
E	IO Connectors	K	RMM4 NIC Port (Optional)
F	RMM4 NIC Port (Optional)		

Figure 38. Back Panel Layout with 750-W Redundant PSUs

11. Intel® Server System P4000CP Storage and Peripheral Drive Bays

The Intel® Server System P4000CP product family has support for many storage device options, including:

- Hot Swap 2.5" Hard Disk Drives
- Hot Swap 3.5" Hard Disk Drives
- SAS Expender Option
- SATA Optical Drive
- eUSB Solid State Device (eUSB SSD)

Support for different storage and peripheral device options will vary depending on the system SKU. This section will provide an overview of each available option.

11.1 2.5" Hard Disk Drive Support

The Intel® Server System P4208CP4MHGC support 8x2.5" drive configuration. The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 2.5" hard disk drive is mounted to a drive tray, allowing for hot swap extraction and insertion. Drive trays have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.

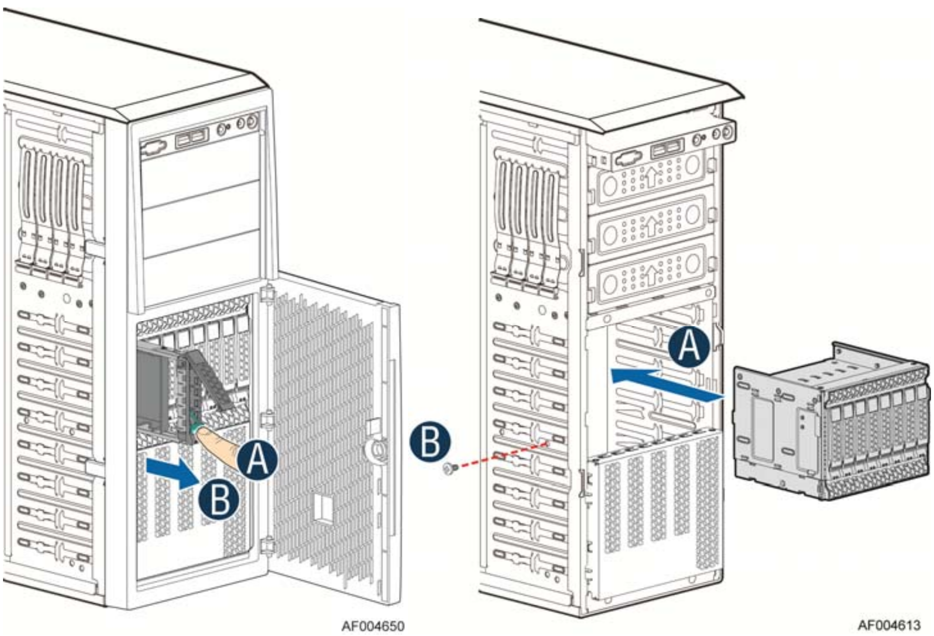


Figure 39. 2.5" Hard Disk Drive Cage

Light pipes integrated into the drive tray assembly direct light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.

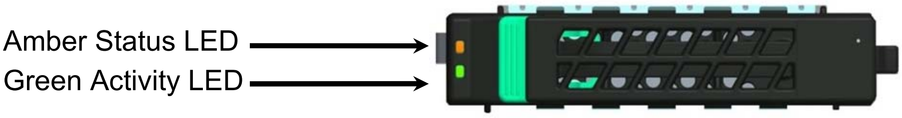


Table 59. 2.5" Hard Disk Drive Status LED States

Amber	Off	No access and no fault
	Solid On	Hard Drive Fault has occurred
	Blink	RAID rebuild in progress (1 Hz), Identify (2 Hz)

Table 60. 2.5" Hard Disk Drive Activity LED States

	Condition	Drive Type	Behavior
Green	Power on with no drive activity	SAS	LED stays on
		SATA	LED stays off
	Power on with drive activity	SAS	LED blinks off when processing a command
		SATA	LED blinks on when processing a command
	Power on and drive spun down	SAS	LED stays off
		SATA	LED stays off
	Power on and drive spinning up	SAS	LED blinks
		SATA	LED stays off

11.1.1 2.5" Drive Hot-Swap Backplane Overview

The 8x2.5" backplane is attached to the back of the 8x2.5" drive bay assembly. On the front side of each backplane are mounted eight hard disk drive interface connectors (A), each providing both power and I/O signals to attached hard disk drives.

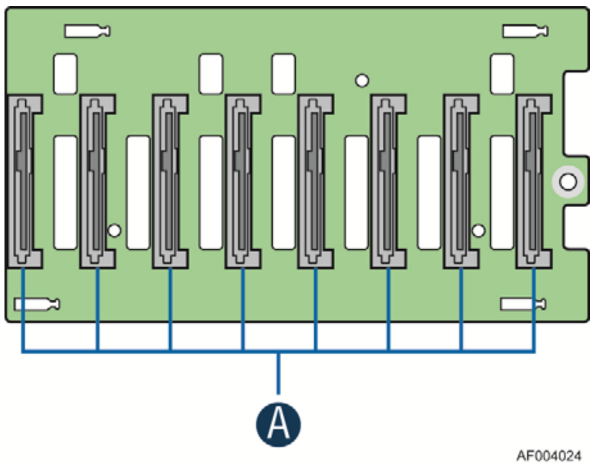
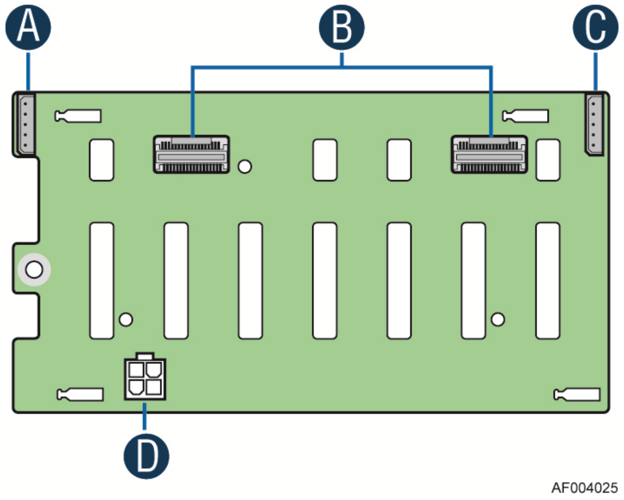


Figure 40. 2.5" Backplane, Front Side

There are several connectors on the backside of each backplane. The following illustration identifies each of them:



Label	Description
A	I2C-Out cable connector for multi-backplane support
B	4-port Mini-SAS cable connectors
C	I2C-In cable connector (From Server board or other backplane)
D	Power connector

Figure 41. 2.5" Backplane, Back Side

A, **C** – I2C Cable Connectors – The backplane includes two cable connectors used as a management interface between the server board and the installed backplanes. In systems configured with multiple backplanes, a short jumper cable is attached between backplanes, with connector B used on the first board and connector D used on the second board, extending the manageability to each installed backplane.

B – Multi-port Mini-SAS Cable Connectors – The backplane includes two multi-port mini-SAS cable connectors, each providing I/O signals for four SAS/SATA hard drives on the backplane. Cables can be routed from matching connectors on the server board, add-in SAS/SATA RAID cards, or optionally installed SAS expander cards.

D – Power Harness Connector – The backplane includes a 2x2 connector supplying power to the backplane. Power is routed to each installed backplane by a multi-connector power cable harness from the server board.

Note: The two SATA 6G connectors from ACHI (white connectors) on server board are not recommended to connect to the 8X2.5 backplane. The LED indicators on the front side of the 8X2.5" drive bay will not light up if used as such.

11.1.2 Cypress* CY8C22545 Enclosure Management Controller

The backplanes support enclosure management using a Cypress* CY8C22545 Programmable System-on-Chip (PSoC*) device. The CY8C22545 drives the hard drive activity/fault LED, hard drive present signal, and controls hard drive power-up during system power-on.

11.2 3.5" Hard Disk Drive Support

The Intel® Server System P4308CP4MHEN and P4308CP4MHGC support 8x3.5" drive configuration. The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 3.5" hard disk drive is mounted to a drive tray, allowing for hot swap extraction and insertion. Drive trays have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.

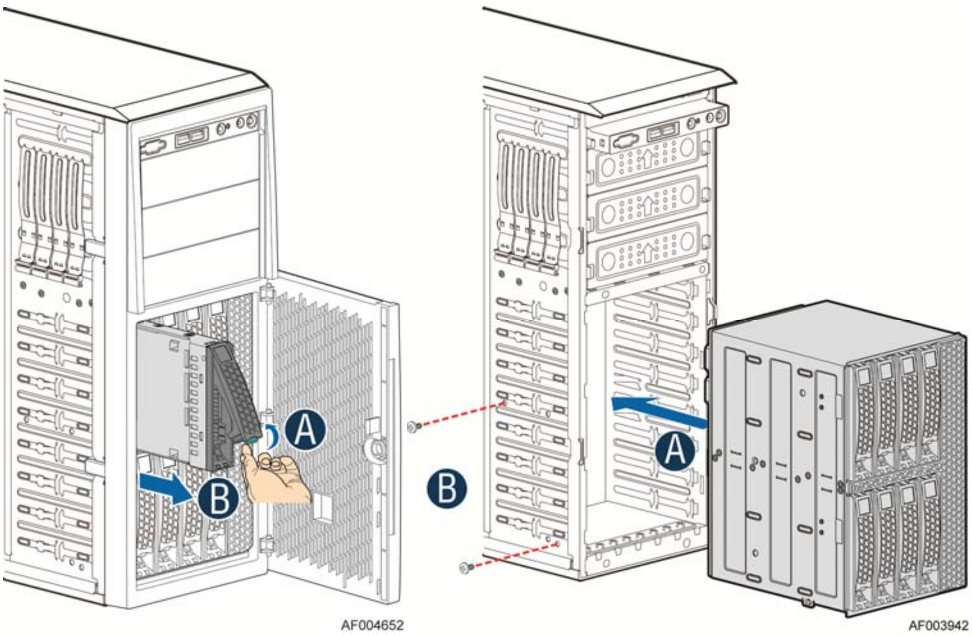


Figure 42. 3.5" Hard Disk Drive Cage

Light pipes integrated into the drive tray assembly direct light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.

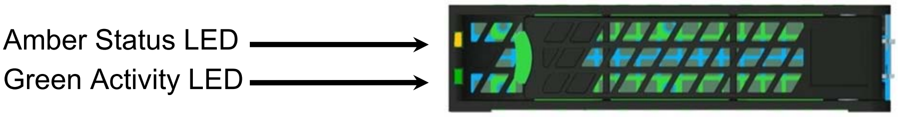


Table 61. 3.5" Hard Disk Drive Status LED States

Amber	Off	No access and no fault
	Solid On	Hard Drive Fault has occurred
	Blink	RAID rebuild in progress (1 Hz), Identify (2 Hz)

Table 62. 3.5" Hard Disk Drive Activity LED States

	Condition	Drive Type	Behavior
Green	Power on with no drive activity	SAS	LED stays on
		SATA	LED stays off
	Power on with drive activity	SAS	LED blinks off when processing a command
		SATA	LED blinks on when processing a command
	Power on and drive spun down	SAS	LED stays off
		SATA	LED stays off
	Power on and drive spinning up	SAS	LED blinks
		SATA	LED stays off

11.2.1 3.5" Drive Hot-Swap Backplane Overview

The backplane mount to the back of the drive bay assembly. On the front side the back plane are mounted eight hard disk drive interface connectors (A), each providing both power and I/O signals to the attached hard disk drives.

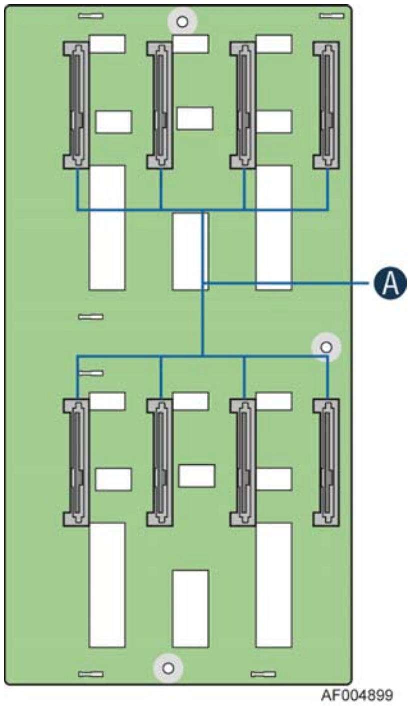
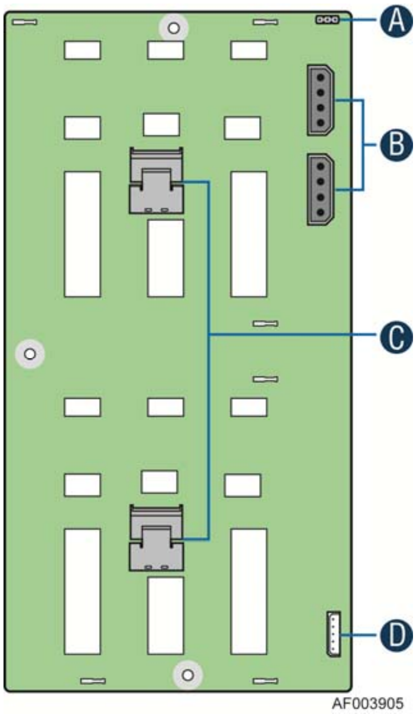


Figure 43. 3.5" Backplane, Front Side

On the backside of each backplane are several connectors. The following illustration identifies each.



Label	Description
A	Reserved
B	Power connector
C	4-port mini-SAS connectors
D	I2C connector

Figure 44. 2.5" Backplane, Back Side

A – Reserved

B – Power Harness Connector - The backplane includes a 2x2 connector supplying power to the backplane. Power is routed to the backplane by a power cable harness from the server board

C – 4-port Mini-SAS Connectors – The backplane includes two or three multi-port mini-SAS cable connectors, each providing I/O signals for four SAS/SATA hard drives on the backplane. Cables can be routed from matching connectors on the server board, add-in SAS/SATA RAID cards, or optionally installed SAS expander cards. Each mini-SAS connector will include a silk-screen identifying which drives the connector supports; Drives 0-3 and Drives 4-7.

D – I2C Cable Connectors – A cable connector used as a management interface to the server board.

Note: The two SATA 6G connectors from ACHI (white connectors) on server board are not recommended to connect to the 8X3.5 backplane. The LED indicators on the front side of the 8X2.5" drive bay will not light up if used as such.

11.2.2 Cypress* CY8C22545 Enclosure Management Controller

The backplanes support enclosure management using a Cypress* CY8C22545 Programmable System-on-Chip (PSoC*) device. The CY8C22545 drives the hard drive activity/fault LED, hard drive present signal, and controls hard drive power-up during system power-on.

11.3 SAS Expander Card Option RS2CV240

The expander card RS2CV240 is an optional accessory that can support more than eight 2.5" hard disk drives. The expander card can be mounted directly behind the drive bay assembly as shown in the following illustration.

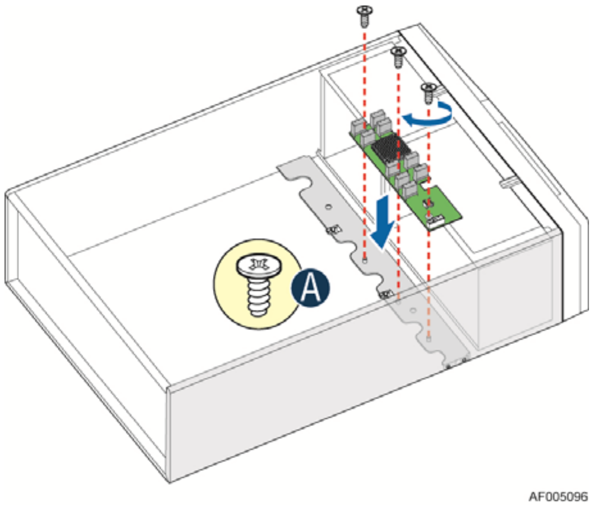


Figure 45. Internal SAS Expander Installation

The following diagrams are used to help identify the mini-SAS connectors found on the SAS expander cards. Care should be taken when connecting connectors from the SAS expander to the connectors on the backplane because each connector is pre-programmed at the factory to provide specific drive identification mapping. Improper connections may provide undesirable drive mappings.

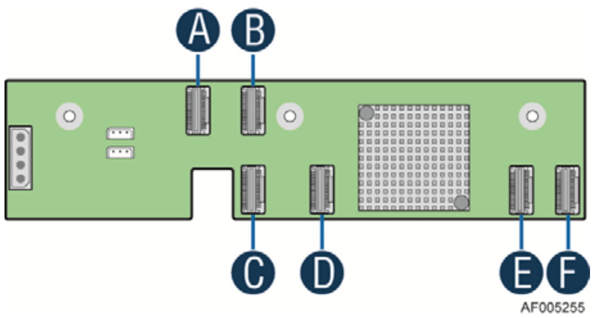


Figure 46. Internal 24-Port SAS Expander Card

Each connector on the SAS expander card can be used as a "cable in" (SAS Controller to SAS Expander) or "cable out" (SAS Expander to Hot Swap Backplane) type connector.

Note: Current SCU controller design limitations prevent any hard drive attached to a SAS expander card from being a boot device when all SCU connectors are attached to the SAS expander card.

For storage configurations that require utilizing a hard disk drive as the boot device, the system must be cabled as follows to ensure a boot device is found and for contiguous drive mapping (0-16).

- The SCU port 0-3 (labeled as "SAS 0" through "SAS 3") connector on the server board is cabled to the first mini-SAS connector on the hot swap backplane
- The SCU port 4-7 (labeled as "SAS 4" through "SAS 7") connector on the server board is cabled to Connector A on the SAS expander card.
- Cables from the SAS Expander to the hot swap backplane must be connected in order from connector B to connector F.

11.4 Optical Drive Support

The Intel® Server System P4000CP includes support three 5.25" optical drive bays. The optical drives can be installed to one of the three drive bays as illustrated below.

Note: The data cables from optical drives are recommended to connect to the two SATA 6G connectors (white connectors) on the server board.

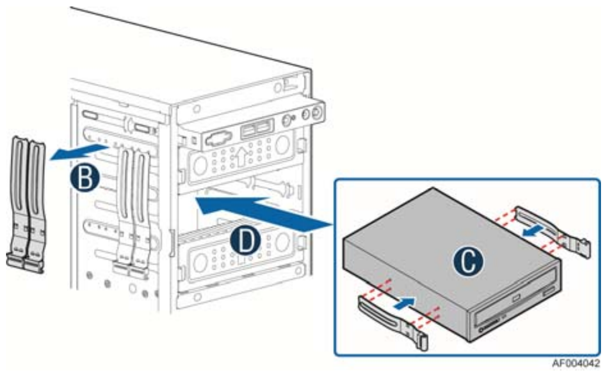


Figure 47. Optical Drive

11.5 Low Profile eUSB SSD Support

The system provides support for a low profile eUSB SSD storage device. A 2mm 2x5-pin connector labeled "eUSB SSD" is used to plug these small flash storage devices.

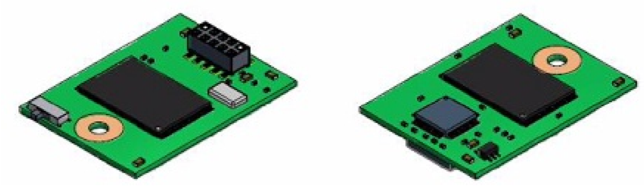


Figure 48. eUSB SSD Support

eUSB features include:

- Two wire small form factor Universal Serial Bus 2.0 (Hi-Speed USB) interface to host.
- Read Speed up to 35 MB/s and write Speed up to 24 MB/s.
- Capacity range from 256GB to 32GB.
- Support USB Mass Storage Class requirements for Boot capability.

12. Intel® Server System P4000CP Thermal Management

The Intel® Server System P4000CP is designed to operate at external ambient temperatures of between 10ºC- 35ºC. Working with integrated platform management, several features within the system are designed to move air in a front to back direction, through the system and over critical components in order to prevent them from overheating and allow the system to operate with best performance.

12.1 Thermal Operation and Configuration Requirements

To keep the system operating within supported maximum thermal limits, the system must meet the following operating and configuration guidelines:

- Ambient in-let temperature cannot exceed 35º C and should not remain at this maximum level for long periods of time. Doing so may affect long term reliability of the system.
- All hard drive bays must be populated. Hard drive carriers either can be populated with a hard drive or supplied drive blank.
- The air duct must be installed at all times.
- In single power supply configurations, the second power supply bay must have the supplied filler blank installed at all times.
- The system top-cover must be installed at all times.

12.2 Thermal Management Overview

In order to maintain the necessary airflow within the system, all of the previously listed components and top cover need to be properly installed. For best system performance, the external ambient temperature must remain below 35ºC and all system fans should be operational.

In the event that system thermals should continue to increase with the system fans operating at their maximum speed, platform management may begin to throttle performance of either the memory subsystem or the processors or both, in order to keep components from overheating and keep the system operational. Throttling of these sub-systems will continue until system thermals are reduced.

Should system thermals increase to a point beyond the maximum thermal limit as pre-programmed in platform management for this system, the system will shut down, the System Status LED will change to a solid Amber state, and the event will be logged to the system event log.

12.3 System Fans

Two cooling solutions are used in the Intel® Server Chassis P4000M series. The base non-redundant solution consists of two 120 x 38mm fixed fans to provide sufficient system cooling. The second redundant solution is designed for maximum up time by providing five 80 x 38 mm replaceable hot-swap fans. The fans can maintain proper system cooling, even with a single failed fan. Air ducts are used in both configurations.

12.3.1 Non-Redundant Cooling Solution

Non-Redundant cooling solution is used in the Intel® Server Chassis P4308XXMXXMHEN.

Two 120 x 38 mm fans provide cooling for the processors, memory, hard drives and add-in cards. The two fans draw air through the rear of each hard drive bay to provide drive, processors, and memory cooling. All system fans provide a signal for RPM detection the server board can make available for server management functions.
In addition, the power supply fan provides cooling for the power supply.

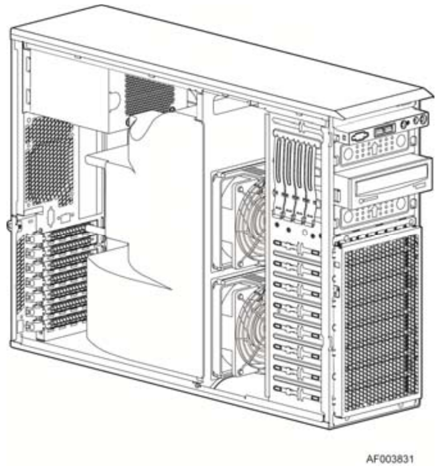


Figure 49. Fixed Fans in Intel® Server Chassis P4308XXMXXMFEN

12.3.2 Redundant Cooling Solution

Redundant cooling solution is used in the Intel® Server Chassis P4308XXMXXMHGC and P4208XXMHGC.

Five hot-swap 80x38mm fans provide cooling for the processors, hard drives, and add-in cards. When any single fan fails, the remaining fans increase in speed and maintain cooling until the failed unit is replaced. All system fans provide a signal for RPM detection that the server board can make available for server management functions.

In addition, the power supply fan provides cooling for the power supply.

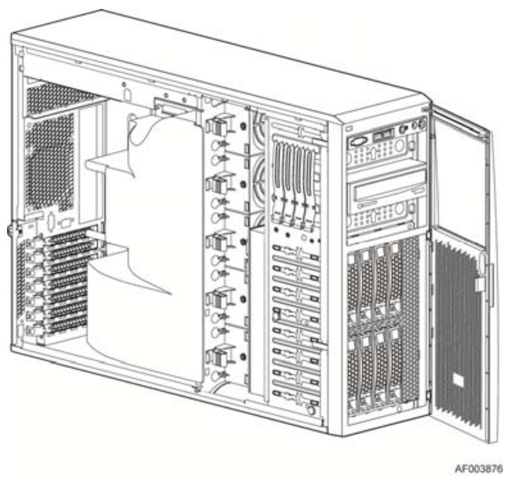


Figure 50. Hot-swap Fans in Intel® Server Chassis P4308XXMXXMHGC

12.3.3 Fan Control

The fans provided in the Intel® Server Chassis P4000M Family contains a tachometer signal that can be monitored by the server management subsystem of the Intel® Server Boards for RPM (Revolutions per Minute) detection.

The server board monitors several temperature sensors and adjusts the PWM (Pulse Width Modulated) signal to drive the fan at the appropriate speed.

The front panel of the chassis has a digital temperature sensor connected to the server board through the front panel's bus. The server board firmware adjusts the fan speed based on the front panel intake temperature and processor temperatures.

Refer to the baseboard documentation for additional details on how fan control is implementation.

12.3.4 Fan Header Connector Descriptions

All system fan headers support pulse width modulated (PWM) fans for cooling the processors in the chassis. PWM fans have an improved RPM range (20% to 100% rated fan speed) when compared to voltage controlled fans.

Fixed chassis fans are a 4-wire/4-pin style designed to plug into 4-pin or 6-pin SSI Fan headers. When plugged into a 6-pin header, only the first four signals are used (Pwr, Gnd, Tach,PWM).

Hot-swap chassis fans are a 6-wire/6-pin style designed to plug into 6-pin headers. The extra signals provide for fan redundancy and failure indications (Pwr, Gnd, Tach, PWM, Presence, and Failure).

13. Intel® Server System P4000CP Power System Options

13.1 Intel® Server System P4000CP Power System Options Overview

Intel® Server System P4308CP4MHEN is equipped with one 550-W power supply. Intel® Server System P4308CP4MHGC and P4208MHGC are equipped with two redundant 750-W power supplies and provide power to mother board through a power distribution board.

13.2 550-W Power Supply

This 550-W power supply specification defines a non-redundant power supply that supports pedestal entry server systems. The 550-W power supply has 7 outputs; 3.3V, 5V, 12V1,12V2, 12V3, -12V and 5Vsb, with no less than 550W. The power supply has an AC input and be power factor corrected.

13.2.1 Mechanical Overview

The power supply size is 98mm x 150mm x 160mm (H x W x D) and has a wire harness for the DC outputs. The AC plugs directly into the external face of the power supply.

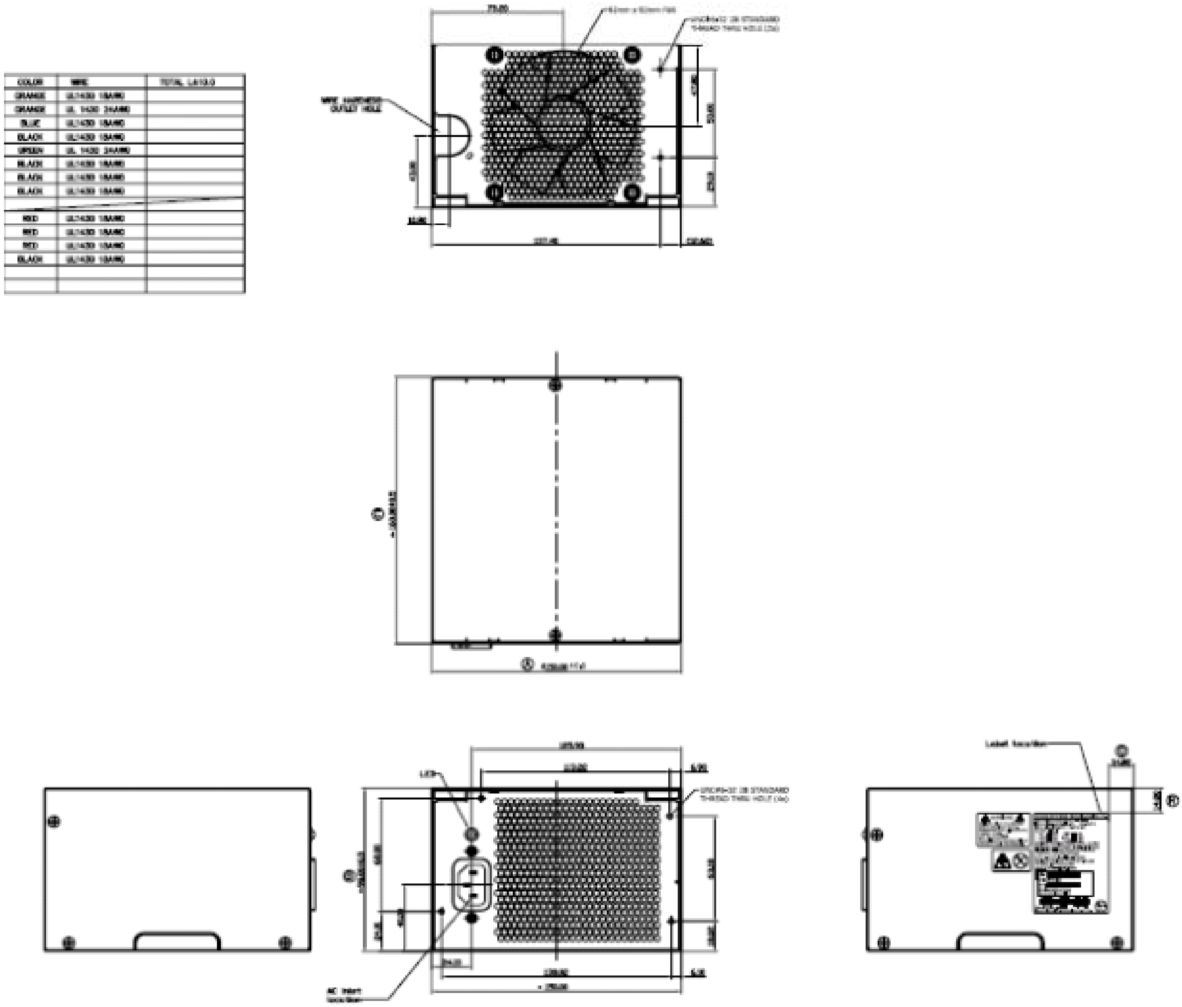


Figure 51. Mechanical Drawing for 550-W Power Supply Enclosure

13.2.1.1 550-W Power Supply Output Wire Harness

Listed or recognized component appliance wiring material (AVLV2), CN, rated min 85°C shall be used for all output wiring.

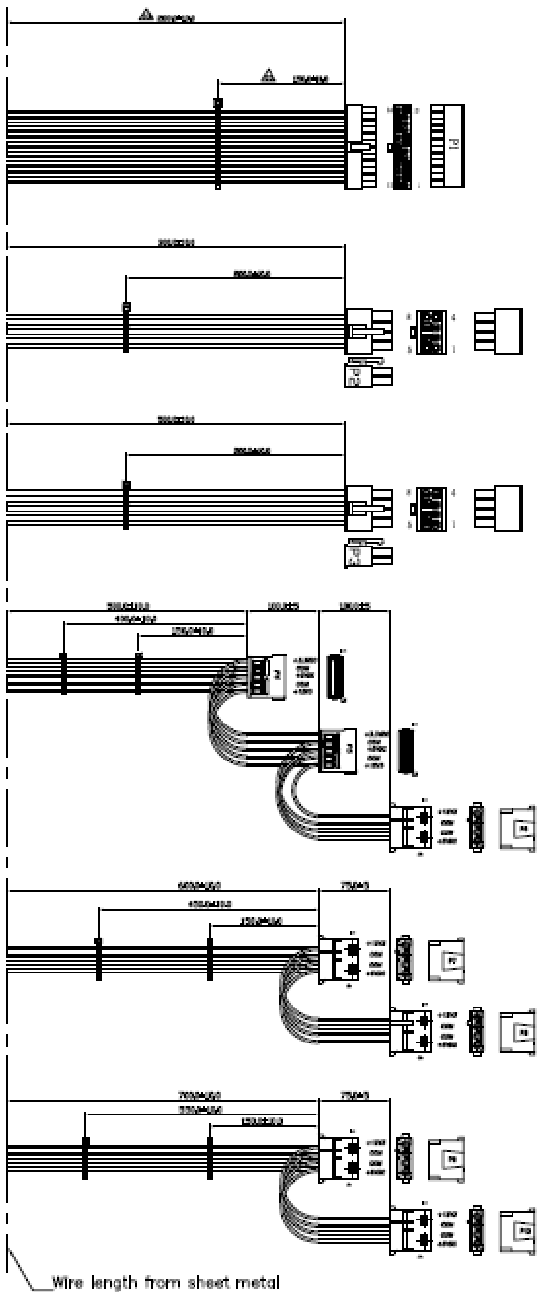


Figure 52. Output Cable Harness for 550-W Power Supply

Table 63. Power Supply Cable Lengths

From	Length (mm)	To connector #	No of pins	Description
Power Supply cover exit hole	280	P1	24	Baseboard Power Connector
Power Supply cover exit hole	300	P2	8	Processor 0 connector
Power Supply cover exit hole	500	P3	8	Processor 1 connector
Power Supply cover exit hole	500	P4	5	SATA Peripheral Power

From	Length (mm)	To connector #	No of pins	Description
				Connector for 5.25"
Extension from P4	100	P5	5	SATA Peripheral Power Connector for 5.25"
Extension from P5	100	P6	4	Peripheral Power Connector for 5.25"
Power Supply cover exit hole	600	P7	4	1x4 Legacy HSBP Power Connector
Extension from P7	75	P8	4	1x4 Legacy HSBP Power Connector
Power Supply cover exit hole	700	P9	4	1x4 Legacy HSBP Power/Fixed HDD Adapter Connection
Extension from P9	75	P10	4	1x4 Legacy HSBP Power/Fixed HDD Adapter Connection

13.2.1.1.1 Main power connector (P1)

- Connector housing: 24- Pin Molex* Mini-Fit Jr 39-01-2245 (94V2) or equivalent
- Contact: Molex* Minifit Jr, Crimp 5556 or equivalent

Table 64. P1 Main Power Connector

Pin	Signal	18 awg color	Pin	Signal	18 awg color
1	+3.3 VDC	Orange	13	+3.3 VDC	Orange
2	+3.3 VDC	Orange	14	-12 VDC	Blue
3	COM	Black	15	COM	Black
4	+5 VDC*	Red	16	PSON#	Green
5	COM	Black	17	COM	Black
6	+5 VDC	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray	20	Reserved	N.C.
9	5VSB	Purple	21	+5 VDC	Red
10	+12V2	Yellow/Black	22	+5 VDC	Red
11	+12V2	Yellow/Black	23	+5 VDC	Red
12	+3.3 VDC	Orange	24	COM	Black

Note: 3.3V remote sense shall be double crimped into pin 13 if needed to meet regulation limits.

13.2.1.1.2 Processor/Memory Power Connector (P2)

- Connector housing: 8- Pin Molex* 39-01-2085 (94V2) or equivalent
- Contact: Molex*, Mini-Fit Jr, HCS, 44476-1111 or equivalent

Table 65. P2 Processor#1 Power Connector

Pin	Signal	18 awg color	Pin	Signal	18 awg color
1	COM	Black	5	+12V1	Yellow

Pin	Signal	18 awg color	Pin	Signal	18 awg color
2	COM	Black	6	+12V1	Yellow
3	COM	Black	7	+12V1	Yellow
4	COM	Black	8	+12V1	Yellow

13.2.1.1.3 Processor/Memory Power Connector (P3)

- Connector housing: 8- Pin Molex* 39-01-2085 (94V2) or equivalent
- Contact: Molex*, Mini-Fit Jr, HCS, 44476-1111 or equivalent

Table 66. P3 Processor#1 Power Connector

Pin	Signal	18 awg color	Pin	Signal	18 awg color
1	COM	Black	5	+12V2	Yellow
2	COM	Black	6	+12V2	Yellow
3	COM	Black	7	+12V2	Yellow
4	COM	Black	8	+12V2	Yellow

13.2.1.1.4 Peripheral Power Connectors (P6,7,8,9,10)

- Connector housing: Amp 1-480424-0 or equivalent
- Contact: Amp 61314-1 contact or equivalent

Table 67. Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+12V3	Yellow/Black
2	COM	Black
3	COM	Black
4	+5 VDC	Red

13.2.1.1.5 SATA Hard Drive Power Connectors (P4, P5)

- Connector housing: JWT A3811H00-5P (94V2) or equivalent
- Contact: JWT A3811TOP-0D or equivalent

Table 68. SATA Power Connector

Pin	Signal	18 AWG Color
1	+3.3V	Orange
2	COM	Black
3	+5VDC	Red
4	COM	Black
5	+12V2	Yellow/Black

13.2.2 Temperature Requirements

The power supply shall operate within all specified limits over the T_{op} temperature range.

Table 69. Thermal Requirements

Item	Description	Min	Max	Units
T_{op}	Operating temperature range.	0	50	°C
$T_{non\text{-}op}$	Non-operating temperature range.	-40	70	° C
Altitude	Maximum operating altitude.		3000	meters

13.2.3 AC Input Requirements

13.2.3.1 Power Factor

The power supply meets the power factor requirements stated in the Energy Star® Program Requirements for Computer Servers. These requirements are stated below.

Table 70. Power Factor Requirements for Computer Servers

Output power	20% load	50% load	100% load
Power factor	0.8	0.9	0.95

Tested at 230Vac, 50Hz and 60Hz and 115VAC, 60Hz.
Tested according to Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.4.3. This is posted at http://efficientpowersupplies.epri.com/methods.asp.

13.2.3.2 AC Inlet Connector

The AC input connector is an *IEC 320 C-14* power inlet. This inlet is rated for 10A/250VAC.

13.2.3.3 AC Input Voltage Specification

The power supply operates within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage does not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC does not cause damage to the power supply, including a blown fuse.

Table 71. AC Input Voltage Range

Parameter	Min	Rated	Vmax	Start up vac	Power off vac
Voltage (110)	90 V_{rms}	100-127 V_{rms}	140 V_{rms}	85VAC +/- 4VAC	70VAC +/- 5VAC
Voltage (220)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}		
Frequency	47 Hz	50/60	63 Hz		

Notes:

1. Maximum input current at low input voltage range shall be measured at 90VAC, at max load.
2. Maximum input current at high input voltage range shall be measured at 180VAC, at max load.
3. This requirement is not to be used for determining agency input current markings.

13.2.3.4 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply meets dynamic voltage regulation requirements. An AC line dropout of any duration does not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the hold up time the power supply recovers and meets all turn on requirements. The power supply meets the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration does not cause damage to the power supply.

Table 72. AC Line Holdup time

Loading	Holdup time
75%	12msec

13.2.3.5 AC Line Fuse

The power supply has one line fused in the **single line fuse** on the line (Hot) wire of the AC input. The line fusing is acceptable for all safety agency requirements. The input fuse is a slow blow type. AC inrush current does not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply do not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions

13.2.3.6 AC Line Leakage Current

The maximum leakage current to ground for each power supply is 3.5mA when tested at 240VAC.

13.2.3.7 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions is defined as the AC line voltage dropping below nominal voltage conditions. “Surge” is defined to refer to conditions when the AC line voltage rises above nominal voltage.
The power supply meets the requirements under the following AC line sag and surge conditions.

Table 73. AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30 %	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Table 74. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

13.2.3.8 Power Recovery

The power supply recovers automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

13.2.4 Efficency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels; 100%, 50% and 20%. Output shall be load according to the proportional loading method defined by 80 Plus in Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.4.3. This is posted at http://efficientpowersupplies.epri.com/methods.asp.

Table 75. Silver Efficiency Requirement

Loading	100% of maximum	50% of maximum	20% of maximum
Minimum Efficiency	85%	88%	85%

The power supply passes with enough margins to make sure in production all power supplies meet these efficiency requirements.

13.2.4.1 Standy Efficiency

When in standby mode; the power supply draws less than 1W AC power with 100mA of 5Vstandby load. This is tested at 115VAC/60Hz and 230VAC/50Hz.

13.2.5 DC Output Specification

13.2.5.1 Output Power/Currents

The following tables define the minimum power and current ratings. The power supply meets both static and dynamic voltage regulation requirements for all conditions.

Table 76. Over Voltage Protection Limits

Parameter	Min	Max.	Peak	Unit
3.3V	0.5	18.0		A
5V	0.3	15.0		A
12V1	0.7	24.0	28.0	A
12V2	0.7	24.0	28.0	A
12V3	1.5	18.0		
3.3V	0.5	18.0		A
– 12V	0.0	0.5		A
5Vstby	0.0	3.0	3.5	A

Notes:

1. Max combined power for all output shall not exceed 550W.
2. Peak combined power for all outputs shall not exceed 630W for 20 seconds.
3. Max combined power of 12V1, 12V2 and 12V3 shall not exceed 530W.
4. Max combined power on 3.3V and 5V shall not exceed 120W.

13.2.5.2 Cross Loading

The power supply maintains voltage regulation limit when operated over the following cross loading conditions.

Table 77. Loading Conditions

	3.3V	5.0V	12V1	12V2	12V3	-12V	5.0Vstby	Total Power	12V Power	3.3V/5V Power
Load1	18	12.1	12	12	11.7	0	0.3	550	428	120
Load2	13.5	15	12	12	11.2	0.5	0.3	549	422	120
Load3	2.5	2	20	20	4.2	0	0.3	550	530	18
Load4	2.5	2	13.1	13.1	18	0	0.3	550	530	18
Load5	0.5	0.3	15	15	6.5	0.5	3	462	438	3
Load6	16	4	1	1	3.5	0	0.3	140	66	73
Load7	16	13	1	1	9	0.5	3	271	132	118

13.2.5.3 Standby Output

The 5VSB output is present when an AC input greater than the power supply turn on voltage is applied.

13.2.5.4 Voltage Regulation

The power supply output voltages stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. These shall be measured at the output connectors.

Table 78. Voltage Regulation Limits

Parameter	Tolerance	Min	Nom	Max	Units
+3.3V	- 3%/+5%	+3.20	+3.30	+3.46	Vrms
+5V	- 4%/+5%	+4.80	+5.00	+5.25	Vrms
+12V1	- 4%/+5%	+11.52	+12.00	+12.60	Vrms
+12V2	- 4%/+5%	+11.52	+12.00	+12.60	Vrms
+12V3	- 4%/+5%	+11.52	+12.00	+12.60	Vrms
- 12V	- 10%/+10%	- 13.20	-12.00	-10.80	Vrms
+5VSB	- 4%/+5%	+4.80	+5.00	+5.25	Vrms

13.2.5.5 Dynamic Loading

The output voltages remain within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate is tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 79. Transient Load Requirements

Output	Δ Step Load Size (See note 2)	Load Slew Rate	Test capacitive Load
+3.3V	6.0A	0.5 A/μsec	970 μF
+5V	4.0A	0.5 A/μsec	400 μF
12V1+12V2 +12V3	23.0A	0.5 A/μsec	2200 μF [1,2]
+5VSB	0.5A	0.5 A/μsec	20 μF

Notes:
1. Step loads on each 12V output may happen simultaneously.
2. The +12V should be tested with 2200μF evenly split between the four +12V rails.
3. This will be tested over the range of load conditions in section 13.2.5.2.

13.2.5.6 Capacitive Loading

The power supply is stable and meets all requirements with the following capacitive loading ranges.

Table 80. Capacitive Loading Conditions

Output	Min	Max	Units
+3.3V	250	5000	μF
+5V	400	5000	μF
+12V	500	8000	μF
-12V	1	350	μF
+5VSB	20	350	μF

13.2.5.7 Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins are connected to the safety ground (power supply enclosure). This grounding is well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply is provided with a reliable protective earth ground. All secondary circuits are connected to protective earth ground. Resistance of the ground returns to chassis does not exceed 1.0 mΩ. This path may be used to carry DC current.

13.2.5.8 Residual Voltage Immunity in Standby mode

The power supply is immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to **500mV**. There is neither additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also does not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition does not exceed **100mV** when AC voltage is applied and the PSON# signal is de-asserted.

13.2.5.9 Common Mode Noise

The Common Mode noise on any output does not exceed **350mV pk-pk** over the frequency band of 10Hz to 20MHz.

The measurement is made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure).
The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

13.2.5.10 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in below table 20. This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor is placed at the point of measurement.

Table 81. Ripples and Noise

+3.3V	+5V	+12V 1, 2, 3	-12V	+5VSB
50mVp-p	50mVp-p	120mVp-p	200mVp-p	50mVp-p

The test set-up shall be as shown below.

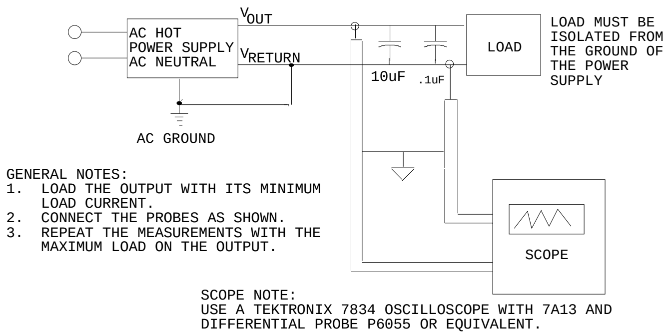


Figure 53. Differential Noise test setup

Note: When performing this test, the probe clips and capacitors should be located close to the load.

13.2.5.11 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages rise from 10% to within regulation limits (T_{vout_rise}) within 2 to 50ms, except for 5VSB - it is allowed to rise from 1 to 25ms. The +3.3V, +5V and +12V1, +12V2, +12V3 output voltages start to rise approximately at the same time**. All outputs rise monotonically**. Each output voltage reach regulation within 50ms (T_{vout_on}) of each other during turn on the power supply. Each output voltage fall out of regulation within 400ms (T_{vout_off}) of each other during turn off. Table 83. Table 83 shows the timing requirements for the power supply being turned on and off by the AC input, with PSON held low and the PSON signal, with the AC input applied. All timing requirements are met for the cross loading condition in Table 77.

Table 82. Output Voltage Timing

Item	Description	MIN	MAX	UNITS
T_{vout_rise}	Output voltage rise time from each main output.	2	50	ms
	Output rise time for the 5Vstby output.	1	25	ms
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	ms
T_{vout_off}	All main outputs must leave regulation within this time.		400	ms

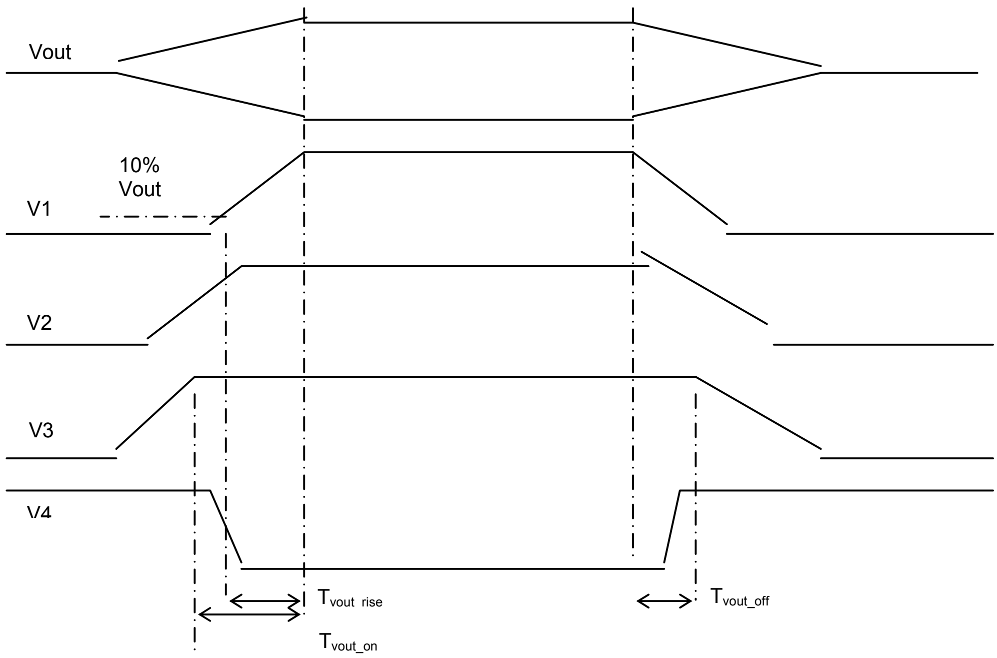


Figure 54. Output Voltage Timing

Table 83. Turn On/Off Timing

Item	Description	MIN	MAX	UNITS
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.		1500	ms
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	ms
T_{vout_holdup}	Time all output voltages stay within regulation after loss of AC. Tested at 75% of maximum load.	13		ms
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK. Tested at 75% of maximum load.	12		ms
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T_{pson_pwok}	Delay from PSON# deactivate to PWOK being de-asserted.		50	ms
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T_{pwok_off}	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		ms
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
T_{sb_vout}	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	10	1000	ms
T_{5VSB_holdup}	Time the 5VSB output voltage stays within regulation after loss of AC.	70		ms

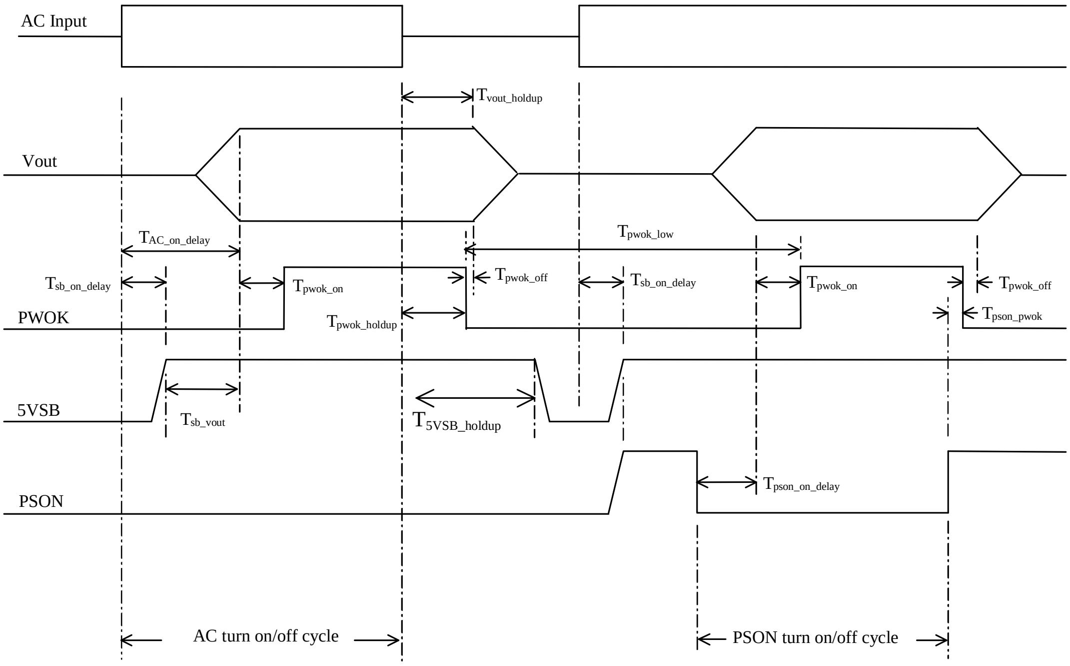


Figure 55. Turn On/Off Timing (Power Supply Signals)

13.2.6 Protection Circuits

Protection circuits inside the power supply causes only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON# cycle HIGH for 1sec able to reset the power supply.

13.2.6.1 Current Limit (OCP)

Below are over current protection limits for each output. If the current limits are exceeded the power supply shuts down and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply does not be damaged from repeated power cycling in this condition. -12V and 5VSB is protected under over current or shorted conditions so that no damage can occur to the power supply. 5Vsb will be auto-recovered after removing OCP limit.

Table 84. Over Current Limits

Output	Min OCP	Max OCP
+3.3V	19 A	30 A
+5V	16 A	30 A
+12V[1,2]	29 A	36 A
+12V[3] (240VA limited)	18.5 A	20 A
-12V	No damage	
5Vstby	No damage	

13.2.6.2 Over Voltage Protection (OVP)

The power supply over voltage protection is locally sensed. The power supply shuts down and latch off after an over voltage condition occurs. This latch is cleared by toggling the PSON#

signal or by an AC power interruption. The table below contains the over voltage limits. The values are measured at the output of the power supply's pins. The voltage shall never exceed the maximum levels when measured at the power pins of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the power supply connector. 5VSB will be auto-recovered after removing OVP limit.

Table 24. Over Voltage Protection (OVP) Limits

Output Voltage	MAX (V)
+3.3V	4.5
+5V	6.5
+12V[1,2,3]	14.5
+5VSB	6.5

13.2.6.3 Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown.

13.2.7 Control and Indicator Functions

The following sections define the input and output signals from the power supply.
Signals that can be defined as low true use the following convention: Signal# = low true

13.2.7.1 PSON# Input Signal

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +3.3V, +5V, +12V1,+12V2,+12V3 and -12V power rails. When this signal is not pulled low by the system, or left open, the outputs (except the +5VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to Figure 17 for the timing diagram.

Table 85. PSON# Signal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	5.25V
Source current, Vpson = low		4mA
Power up delay: Tpson_on_delay	5msec	400msec
PWOK delay: T pson_pwok		50msec

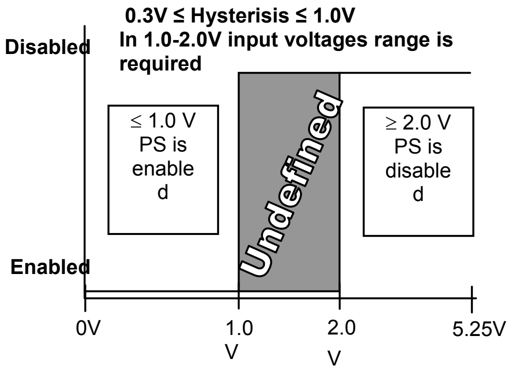


Figure 56. PSON# Required Signal Characteristic

13.2.7.2 PWOK (Power OK) Output Signal

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. Refer to Figure 55 for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

Table 86. PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in system.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	MAX
Logic level low voltage, Isink=4mA	0V	0.4V
Logic level high voltage, Isource=200µA	2.4V	5.25V
Sink current, PWOK = low		4mA
Source current, PWOK = high		2mA
PWOK delay: Tpwok_on	100ms	500ms
PWOK rise and fall time		100µsec
Power down delay: T pwok_off	1ms	

13.3 750-W Power Supply

This specification defines a 750W redundant power supply that supports server systems. This power supply has 2 outputs; 12V and 12V standby. The AC input is auto ranging and power factor corrected.

13.3.1 Mechanical Overview

The physical size of the power supply enclosure is 39/40mm x 74mm x 185mm. The power supply contains a single 40mm fan. The power supply has a card edge output that interfaces with a 2x25 card edge connector in the system. The AC plugs directly into the external face of the power supply. Refer to the following figure. All dimensions are nominal.

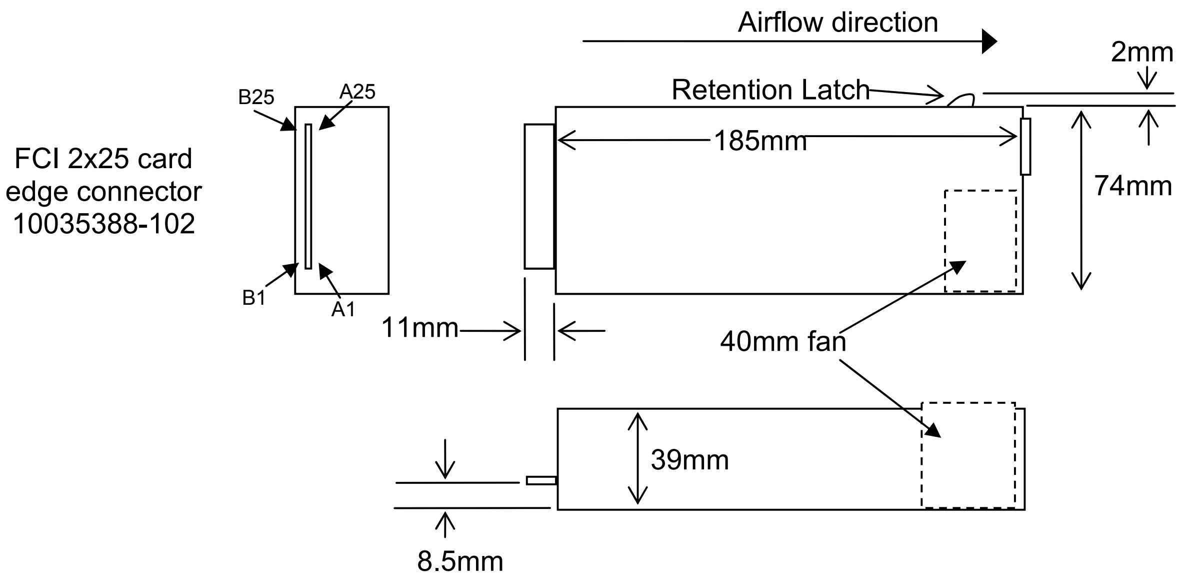


Figure 57. 750-W Power Supply Outline Drawing

13.3.1.1 DC Output Connector

The power supply uses a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector (equivalent to 2x25 pin configuration of the FCI power card connector 10035388-102LF).

Table 87. DC Output Connector

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V

Pin	Name	Pin	Name
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus SDA	B19	A0 (SMBus address)
A20	PMBus SCL	B20	A1 (SMBus address)
A21	PSON	B21	12V stby
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Return Sense	B23	12V load share bus
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	Compatibility **Check** pin

13.3.1.2 Handle Retention

The power supply has a handle to assist extraction. The module is able to be inserted and extracted without the assistance of tools. The power supply has a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply.

The handle protects the operator from any burn hazard.

13.3.1.3 LED Marking and Identification

The power supply uses a bi-color LED: Amber and Green. Below are table showing the LED states for each power supply operating state and the LED's wavelength characteristics.

Refer to the Intel LED Wavelength and Intensity specification for more details.

Table 88. LED Characteristics

	Min λd Wavelength	Nominal λd Wavelength	Max λd Wavelength	Units
Green	562	565	568	nm
Amber	607	610	613	nm

Table 89. Power Supply LED Functionality

Power Supply Condition	LED State
Output ON and OK	GREEN
No AC power to all power supplies	OFF
AC present/Only 12VSB on (PS off) or PS in Cold redundant state	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER
Power supply FW updating	2Hz Blink GREEN

13.3.1.4 Temperature Requirements

The power supply operates within all specified limits over the T_{op} temperature range. All airflow passes through the power supply and not over the exterior surfaces of the power supply.

Table 90. Environmental Requirements

Item	Description	Min	Max	Units
$T_{op\_sc\_red}$	Operating temperature range; spreadcore redundant (60% load, 3000m, spreadcore system flow impedance2)	0	60	°C
$T_{op\_sc\_nr}$	Operating temperature range; spreadcore non-redundant (100% load, 3000m, spreadcore system flow impedance2)	0	50	°C
$T_{op\_rackped\_900}$	Operating temperature range; rack/pedestal 900m (100% load, 900m, rack/pedestal system flow impedance2)	0	45	°C
$T_{op\_rackped\_3000}$	Operating temperature range; rack/pedestal 3000m (100% load, 3000m, rack/pedestal system flow impedance2)	0	40	°C
Texit	Maximum exit air temperature		68	°C
$T_{non\text{-}op}$	Non-operating temperature range.	-40	70	°C
Altitude	Maximum operating altitude 3		3050	m

Notes:

1. Under normal conditions, the exit air temperature shall be less than 65C. 68C is provided for absolute worst case conditions and is expected only to exist when the inlet ambient reaches 60C.
2. $T_{op\_rackped\_900}$ condition only requires max altitude of 900m.

The power supply meets UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side are classified as “Handle, knobs, grips, and so on held for short periods of time only”.

13.3.2 AC Input Requirements

13.3.2.1 Power Factor

The power supply meets the power factor requirements stated in the Energy Star® Program Requirements for Computer Servers. These requirements are stated below.

Table 91. Power Factor Requirements for Computer Servers

Output power	10% load	20% load	50% load	100% load
Power factor	> 0.65	> 0.80	> 0.90	> 0.95

Tested at 230Vac, 50Hz and 60Hz and 115VAC, 60Hz
Tested according to Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.4.3. This is posted at http://efficientpowersupplies.epri.com/methods.asp.

13.3.2.2 AC Inlet Connector

The AC input connector is an *IEC 320 C-14* power inlet. This inlet is rated for 10A/250VAC.

13.3.2.3 AC Input Voltage Specification

The power supply operates within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage does not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC does not cause damage to the power supply, including a blown fuse.

Table 92. AC Input Voltage Range

Parameter	MIN	Rated	V_{MAX}	Start up VAC	Power Off VAC
Voltage (110)	90 V_{rms}	100-127 V_{rms}	140 V_{rms}	85VAC +/- 4VAC	70VAC +/- 5VAC
Voltage (220)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}		
Frequency	47 Hz	50/60	63 Hz		

Notes:

1. Maximum input current at low input voltage range shall be measured at 90VAC, at max load.
2. Maximum input current at high input voltage range shall be measured at 180VAC, at max load.
3. This requirement is not to be used for determining agency input current markings.

13.3.2.4 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply meets dynamic voltage regulation requirements. An AC line dropout of any duration does not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time the power supply recovers and meets all turn on requirements. The power supply meets the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration does not cause damage to the power supply.

Table 93. AC Line Holdup Time

Loading	Holdup time
70%	12msec

13.3.2.4.1 AC Line 12VSBHoldup

The 12VSB output voltage stays in regulation under its full load (static or dynamic) during an AC dropout of **70ms min** (=12VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

13.3.2.5 AC Line Fuse

The power supply has one line fused in the **single line fuse** on the line (Hot) wire of the AC input. The line fusing is acceptable for all safety agency requirements. The input is a slow blow type. AC inrush current does not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply does not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

13.3.2.6 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions is defined as the AC line voltage dropping below nominal voltage conditions. “Surge” is defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply meets the requirements under the following AC line sag and surge conditions.

Table 94. AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Table 95. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

13.3.2.7 Power Recovery

The power supply shall recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

13.3.3 Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels; 100%, 50%, 20%, and 10%. Output shall be load according to the proportional loading method defined by 80 Plus in Generalized Internal Power Supply Efficiency Testing Protocol Rev. 6.4.3. This is posted at http://efficientpowersupplies.epri.com/methods.asp.

Table 96. Silver Efficiency Requirement

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Minimum Efficiency	91%	94%	90%	82%

The power supply passes with enough margins to make sure in production all power supplies meet these efficiency requirements.

13.3.4 DC Output Specification

13.3.4.1 Output Power/Currents

The following table defines the minimum power and current ratings. The power supply meets both static and dynamic voltage regulation requirements for all conditions.

Table 97. Minimum Load Ratings

Parameter	Min	Max.	Peak 2, 3	Unit
12V main	0.0	62.0	70.0	A
12Vstby 1	0.0	2.1	2.4	A

13.3.4.2 Standby Output

The 12VSB output is present when an AC input greater than the power supply turn on voltage is applied.

13.3.4.3 Voltage Regulation

The power supply output voltages stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. These shall be measured at the output connectors.

Table 98. Voltage Regulation Limits

Parameter	Tolerance	Min	Nom	Max	Units
+12V	- 5%/+5%	+11.40	+12.00	+12.60	V_{rms}
+12V stby	- 5%/+5%	+11.40	+12.00	+12.60	V_{rms}

13.3.4.4 Dynamic Loading

The output voltages remains within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate is tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 99. Transient Load Requirements

Output	Δ Step Load Size (See note 2)	Load Slew Rate	Test capacitive Load
+12VSB	1.0A	0.25 A/µsec	20 µF
+12V	60% of max load	0.25 A/µsec	2000 µF

Note:

For dynamic condition +12V min loading is 1A.

13.3.4.5 Capacitive Loading

The power supply is stable and meets all requirements with the following capacitive loading ranges.

Table 100. Capacitive Loading Conditions

Output	Min	Max	Units
+12VSB	20	3100	µF
+12V	500	25000	µF

13.3.4.6 Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins are connected to the safety ground (power supply enclosure). This grounding is well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply is provided with a reliable protective earth ground. All secondary circuits is connected to protective earth ground. Resistance of the ground returns to chassis does not exceed 1.0 mΩ. This path may be used to carry DC current.

13.3.4.7 Residual Voltage Immunity in Standby mode

The power supply is immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There is neither additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also does not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition does not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

13.3.4.8 Common Mode Noise

The Common Mode noise on any output does not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz.

The measurement is made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure).

The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

13.3.4.9 Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages remains within the limits with the capacitive load specified. The hot swap test is conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply uses a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

13.3.4.10 Forced Load Sharing

The +12V output will have active load sharing. The output will share within 10% at full load. The failure of a power supply does not affect the load sharing or output voltages of the other supplies still operating. The supplies are able to load share in parallel and operate in a hot-swap/redundant **1+1** configurations. The 12VSB output is not required to actively share current between power supplies (passive sharing). The 12VSB output of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

13.3.4.11 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in below Table. 41. This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor is placed at the point of measurement.

Table 101. Ripples and Noise

+12V main	+12VSB
120mVp-p	120mVp-p

The test set-up shall be as shown below.

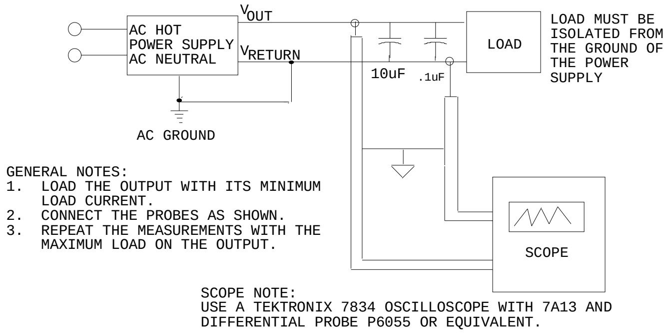


Figure 58. Differential Noise test setup

Note: When performing this test, the probe clips and capacitors should be located close to the load.

13.3.4.12 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70ms. For 12VSB, it is allowed to rise from 1.0 to 25ms. **All outputs must rise monotonically**. Table below shows the timing requirements for the power supply being turned on and off by the AC input, with PSON held low and the PSON signal, with the AC input applied.

Table 102. Timing Requirements

Item	Description	Min	Max	Units
T^{vout_rise}	Output voltage rise time	5.0 *	70 *	ms
$T_{sb\_on\_delay}$	Delay from AC being applied to 12VSBbeing within regulation.		1500	ms
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		3000	ms
T_{vout_holdup}	Time 12Vl output voltage stay within regulation after loss of AC.	13		ms
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	12		ms
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T_{pson_pwok}	Delay from PSON# deactivate to PWOK being de-asserted.		5	ms
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T_{pwok_off}	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1		ms
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
T_{sb_vout}	Delay from 12VSBbeing in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T_{12VSB_holdup}	Time the 12VSBoutput voltage stays within regulation after loss of AC.	70		ms

* The 12VSBoutput voltage rise time shall be from 1.0ms to 25ms.

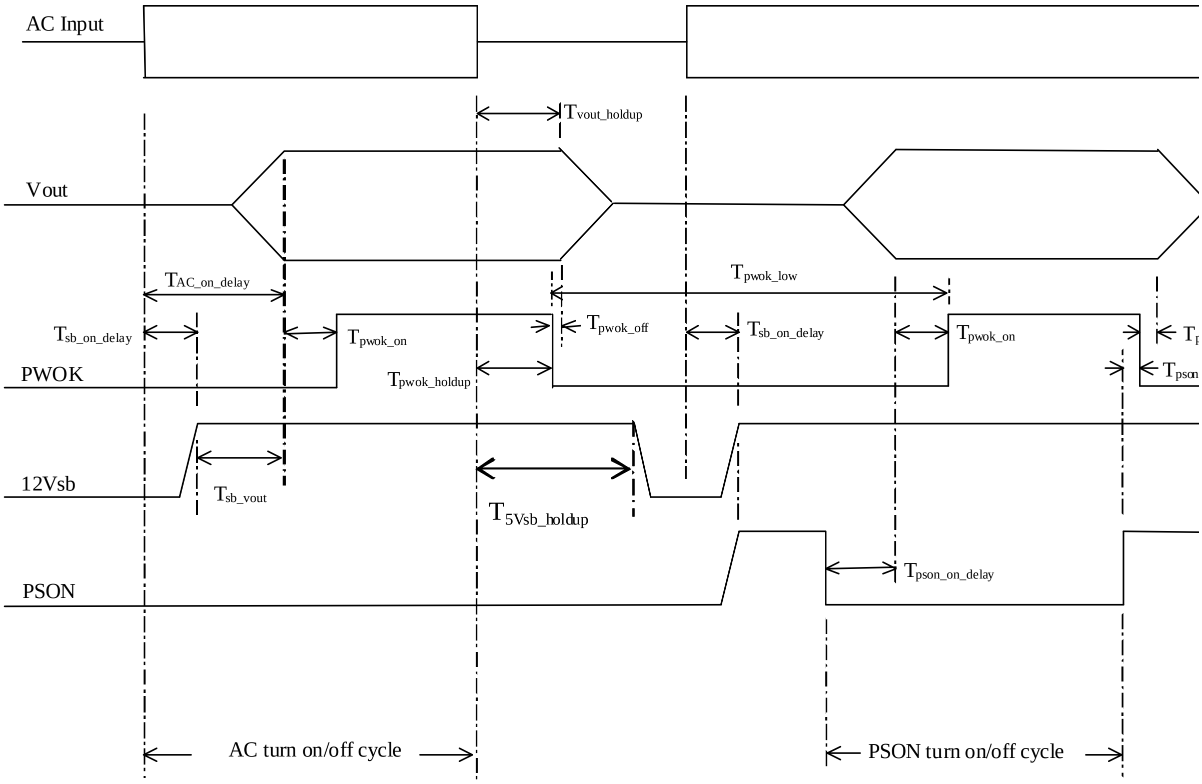


Figure 59. Turn On/Off Timing (Power Supply Signals)

13.3.5 Protection Circuits

Protection circuits inside the power supply causes only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON# cycle HIGH for 1sec is able to reset the power supply.

13.3.5.1 Current Limit (OCP)

The power supply has current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply shuts down and latchs off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply does not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

Table 103. Over Current Protection

Output VOLTAGE	Input voltage range	Over Current Limits
+12V	90 – 264VAC	72A min; 78A max
12VSB	90 – 264VAC	2.5A min; 3.5A max

13.3.5.2 Over Voltage Protection (OVP)

The power supply over voltage protection is locally sensed. The power supply shuts down and latchs off after an over voltage condition occurs. This latch is cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage does not exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage doesn't trip any lower than the minimum levels when measured at the power connector. 12VSBwill be auto-recovered after removing OVP limit.

Table 104. Over Voltage Protection (OVP) Limits

Output voltage	Min (v)	Max (v)
+12V	13.3	14.5
+12VSB	13.3	14.5

13.3.5.3 Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 4°C of ambient temperature margin.

13.3.6 Control and Indicator Functions

The following sections define the input and output signals from the power supply.

Signals that can be defined as low true use the following convention: Signal# = low true.

13.3.6.1 PSON# Input Signal

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +12V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +12VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to Table 42 for the timing diagram.

Table 105. PSON# Signal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, Vpson = low		4mA
Power up delay: $T_{pson\_on\_delay}$	5msec	400msec
PWOK delay: T_{pson_pwok}		50msec

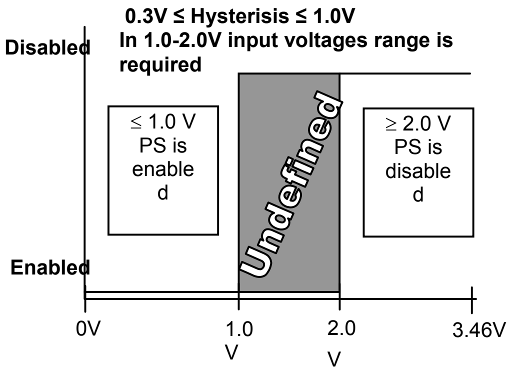


Figure 60. PSON# Required Signal Characteristic.

13.3.6.2 PWOK (Power OK) Output Signal

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See Table 46 for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

Table 106. PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in the power supply.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	MAX
Logic level low voltage, Isink=400uA	0V	0.4V
Logic level high voltage, Isource=200μA	2.4V	3.46V
Sink current, PWOK = low		400uA
Source current, PWOK = high		2mA
PWOK delay: T_{pwok_on}	100ms	1000ms
PWOK rise and fall time		100μsec
Power down delay: T_{pwok_off}	1ms	200msec

A recommended implementation of the Power Ok circuits is shown below.

Note: the Power Ok circuits should be compatible with 5V pull up resistor (>10k) and 3.3V pull up resistor (>6.8k).

13.3.6.3 SMBAlert# Signal

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold (see sec. 4.10), general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

This signal is to be asserted in parallel with LED turning solid Amber or blink Amber.

Table 107. SMBAlert# Signal Characteristics

Signal Type (Active Low)	Open collector/drain output from power supply. Pull-up to VSB located in system.	
Alert# = High	OK	
Alert# = Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 μA		3.46 V
Sink current, Alert# = low		4 mA
Sink current, Alert# = high		50 μA
Alert# rise and fall time		100 μs

13.3.7 Thermal CLST

The power supply shall assert the SMBAlert signal when a temperature sensor crosses a warning threshold. Refer to the *Intel® Common Hardware and Firmware Requirements for CRPS Power Supplier* for detailed requirements.

13.3.8 Power Supply Diagnostic "Black Box"

The power supply saves the latest PMBus data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data is accessible by the SMBus interface with an external source providing power to the 12Vstby output.

Refer to the Intel "Common Hardware and Firmware Requirements for CRPS Power Supplier" for detailed requirements.

13.3.9 Firmware Uploader

The power supply has the capability to update its firmware by the PMBus interface while it is in standby mode. This FW can be updated when in the system and in standby mode and outside the system with power applied to the 12Vstby pins.

Refer to the Intel Common Hardware and Firmware Requirements for CRPS Power Supplier for detailed requirements.

13.4 Higer Power Common Redundant Power Distribution Board (PDB)

The Power Distribution Board (PDB) for Intel® Server Chassis P4000M supports the Common Redundant power supply in a 1+1 redundant configuration. The PDB is designed to plug directly to the output connector of the PS and it contains 3 DC/DC power converters to produce other required voltages: +3.3VDC, +5VDC and 5V standby along with additional over current protection circuit for the 12V rails.

This power distribution board is intended to be used in the Intel® Server Chassis P4000M with various common redundant power supplies; 460W, 750W, 1200W, 1600W and DC input 750W.

13.4.1 Mechanical Overview

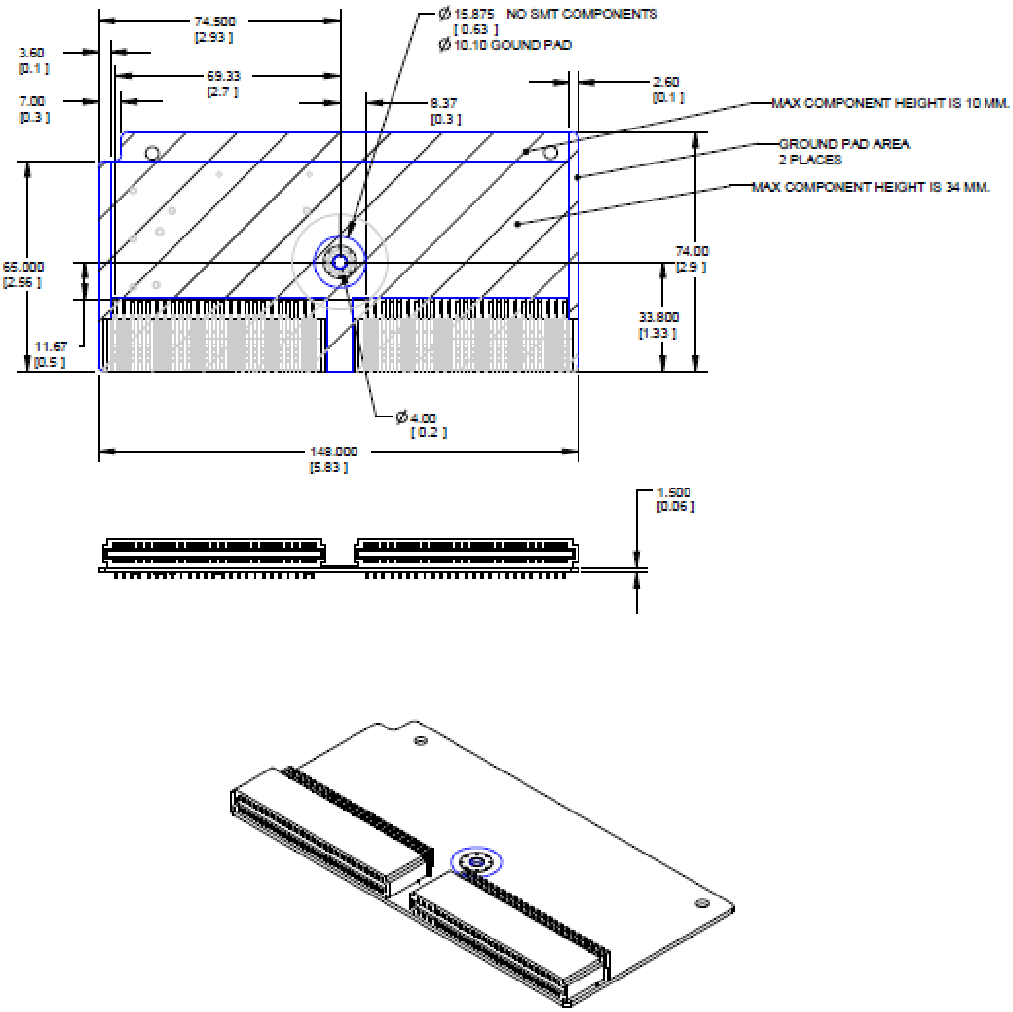


Figure 61. Outline Drawing

13.4.1.1 Airflow Requirements

The power distribution board shall get enough airflow for cooling DC/DC converters from the fans located in the Power Supply modules. Below is a basic drawing showing airflow direction.

The amount of cooling airflow that will be available to the DC/DC converters is to be no less then 1.2M/s.

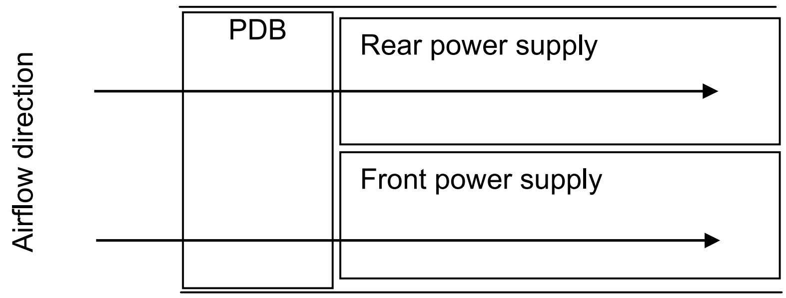


Figure 62. Airflow Diagram

13.4.1.2 DC/DC converter cooling

The dc/dc converters on the power distribution board are in series airflow path with the power supplies.

13.4.1.3 Temperature Requirements

The PDB operates within all specified limits over the Top temperature range. Some amount of airflow shall pass over the PDB.

Table 108. Thermal Requirements

Item	Description	Min	Max	Units
T_{op}	Operating temperature range.	0	50	°C
T_{non-op}	Non-operating temperature range.	-40	70	°C

13.4.1.4 Efficiency

Each DC/DC converter shall have a **minimum** efficiency of **85%** at 50% ~ 100% loads and over +12V line voltage range and over temperature and humidity range.

13.4.2 DC Output Specification

13.4.2.1 Input Connector (power distribution mating connector)

The power distribution provides 2 power pin, a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector (equivalent to 2x25 pin configuration of the FCI power card connector 10035388-102LF). The FCI power card edge connector is a new version of the PCE from FCI used to raise the card edge by 0.031” to allow for future 0.093” PCBs in the system. The card edge connector has no keying features; the keying method is accomplished by the system sheet metal.

Table 109. Input Connector and Pin Assignment Diagrams

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus SDA	B19	A0 (SMBus address)
A20	PMBus SCL	B20	A1 (SMBus address)
A21	PSON	B21	12V stby
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Return Sense	B23	12V load share
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	Compatibility Pin*

*The compatibility Pin is used for soft compatibility check. The two compatibility pins are connected directly.

13.4.2.2 Output Wire Harness

The power distribution board has a wire harness output with the following connectors.

Listed or recognized component appliance wiring material (AVLV2), CN, rated min 85°C shall be used for all output wiring.

Table 110. PDB Cable Length

From	Length, mm	To connector #	No of pins	Description
Power Supply cover exit hole	280	P1	24	Baseboard Power Connector
Power Supply cover exit hole	300	P2	8	Processor 0 connector
Power Supply cover exit hole	500	P3	8	Processor 1 connector
Power Supply cover exit hole	900	P4	5	Power FRU/PMBus connector
Power Supply cover exit hole	500	P5	5	SATA peripheral power connector for 5.25”
Extension from P5	100	P6	5	SATA peripheral power connector for 5.25”
Extension from P6	100	P7	4	Peripheral Power Connector for 5.25”/HSBP Power
Power Supply cover exit hole	600	P8	4	1x4 legacy HSBP Power Connector

From	Length, mm	To connector #	No of pins	Description
Extension from P8	75	P9	4	1x4 legacy HSBP Power Connector
Power supply cover exit hole	700	P10	4	1x4 legacy HSBP Power/Fixed HDD adaptor Connection
Extension from P10	75	P11	4	1x4 legacy HSBP Power/Fixed HDD adaptor Connection
Connector only (no cable)	N/a	P12	4	Aux baseboard power connector for PCIe slots
Connector only (no cable)	N/a	P13	4	GFX card aux connectors
Connector only (no cable)	N/a	P14	4	
Connector only (no cable)	N/a	P15	4	
Connector only (no cable)	N/a	P16	4	

13.4.2.2.1 Baseboard power connector (P1)

- Connector housing: 24-Pin Molex* Mini-Fit Jr. 39-01-2245 or equivalent
- Contact: Molex* Mini-Fit, HCS Plus, Female, Crimp 44476 or equivalent

Table 111. P1 Baseboard Power Connector

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	+3.3VDC	Orange	13	+3.3VDC	Orange
	3.3V RS	Orange (24AWG)			
2	+3.3VDC	Orange	14	-12VDC	Blue
3	COM	Black	15	COM	Black
4	+5VDC	Red	16	PSON#	Green (24AWG)
5	COM	Black	17	COM	Black
6	+5VDC	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray (24AWG)	20	Reserved	N.C.
9	5 VSB	Purple	21	+5VDC	Red
10	+12V1	Yellow	22	+5VDC	Red
11	+12V1	Yellow	23	+5VDC	Red
12	+3.3VDC	Orange	24	COM	Black

13.4.2.2.2 Processor#0 Power Connector (P2)

- Connector housing: 8-Pin Molex* 39-01-2080 or equivalent
- Contact: Molex* Mini-Fit, HCS Plus, Female, Crimp 44476 or equivalent

Table 112. P0 Processor Power Connector

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5*	+12V1	White
2	COM	Black	6	+12V1	White

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
3	COM	Black	7	+12V1	White
4	COM	Black	8	+12V1	White

13.4.2.2.3 Processor#1 Power Connector (P3)

- Connector housing: 8-Pin Molex* 39-01-2080 or equivalent
- Contact: Molex* Mini-Fit, HCS Plus, Female, Crimp 44476 or equivalent

Table 113. P1 Processor Power Connector

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5	+12V1	Brown
2	COM	Black	6	+12V1	Brown
3	COM	Black	7	+12V1	Brown
4	COM	Black	8	+12V1	Brown

13.4.2.2.4 Power Signal Connector (P4)

- Connector housing: 5-pin Molex* 50-57-9405 or equivalent
- Contacts: Molex* 16-02-0087 or equivalent

Table 114. Power Signal Connector

Pin	Signal	24 AWG Color
1	I2C Clock	White
2	I2C Data	Yellow
3	SMBAlert#	Red
4	COM	Black
5	3.3RS	Orange

13.4.2.2.5 2x2 12V connector (P12-P16)

Connector header: Foxconn p/n HM3502E-P1 or equivalent

Table 115. P12 12V connectors

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5	+12V1	Yellow
2	COM	Black	6	+12V1	Yellow

Table 116. P13 - P16 12V connectors

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5	+12V2	Yellow
2	COM	Black	6	+12V2	Yellow

13.4.2.2.6 Legacy 1x4 Peripheral Power Connectors (P7, P8, P9, P10)

- Connector housing: Molex* 0015-24-4048 or equivalent;
- Contact: Molex* 0002-08-1201 or equivalent

Table 117. P8, P9 Legacy Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+12V3	Green
2	COM	Black
3	COM	Black
4	+5 VDC	Red

Table 118. P7, P10, P11 Legacy Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+12V3	Green
2	COM	Black
3	COM	Black
4	+5 VDC	Red

13.4.2.2.7 SATA 1x5 Peripheral Power Connectors (P5, P6)

- Connector housing: Molex* 0675-82-0000 or equivalent
- Contact: Molex* 0675-81-0000 or equivalent

Table 119. SATA Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+3.3VDC	Orange
2	COM	Black
3	+5VDC	Red
4	COM	Black
5	+12V2	Yellow

13.4.2.3 Grounding

The ground of the pins of the PDB output connectors provides the power return path. The output connector ground pins is connected to safety ground (PDB enclosure). This grounding is well designed to ensure passing the max allowed Common Mode Noise levels.

13.4.2.4 Remote Sense

Below is listed the remote sense requirements and connection points for all the converters on the PDB and the main 12V output of the power supply.

Table 120. Remote Sense Connection Points

Converter	+ sense location	- sense location
Power supply main 12V	On PDB	On PDB
12V/3.3V	P20 (1x5 signal connector)	P20 (1x5 signal connector)
12V/5V	On PDB	On PDB
12V/-12V	none	none
12Vstby/5Vstby	none	none

Table 121. Remote Sense Requirements

Characteristic	Requirement
+3.3V remote sense input impedance	200Ω (measure from +3.3V on P1 2x12 connector to +3.3V sense on P20 1x5 signal connector)
+3.3V remote sense drop	200mV (remote sense must be able to regulate out 200mV drop on the +3.3V and return path; from the 2x12 connector to the remote sense points)
Max remote sense current draw	< 5mA

13.4.2.5 12V Rail Distribution

The following table shows the configuration of the 12V rails and what connectors and components in the system they are powering.

Table 122. 12V Rail Distribution

	P2		P3		P12	P1		P8	P9	P10	P11	P5,6,7	P13	P14	P15	P16	P17	P18	P19	P20				
	2x4		2x4		2x2	2x12		1x4	1x4	1x4	1x4	(2) 1x5, 1x4	GPU1		GPU2		GPU3		GPU4			OCP		
	CPU 1	Memory 1	CPU 2	Memory 2	PCIe	Fans	Misc	HDD and peripherals					2x3	2x4	2x3	2x4	2x3	2x4	2x3	2x4	Total Current	Min	Nominal	Max
12V1	17.8 A	10.5 A	17.8 A	10.5 A	21.7 A	10.0 A	3.0 A														91 A	91	95.5	100
12V2													6.3 A	12.5 A	6.3 A	12.5 A	6.3 A	12.5 A	6.3 A	12.5 A	76 A	76	88	100
12V3								18.0 A													18 A	18	19	20

Note:

+12V current to PCIe slots may be supplied from four different connectors. 12V1 on P2, 12V2 on P3, 12V3 on P1, and 12V3 on P12. P12 is reserved for board that needs 4 x GPU cards powered. P1 is the main 12V power for PCIe slot; but additional 12V power can be connected to P2 and/or P3. The motherboard MUST NOT short any of the 12V rails or connectors together.

13.4.2.6 Hard Drive 12V rail configuration options

The following table shows the hard drive configuration options using the defined power connectors. In some cases additional converter or 'Y' cables are needed.

Table 123. Hard Drive 12V rail configuration options

	P8	P9	P10	P11	P5	P6	P7
	1x4	1x4	1x4	1x4	1x5	1x5	1x4
	18						
3 x 2.5" 8xHDD BP	HDD1 8 x 2.5	HDD2 8 x 2.5	N/a	N/a	N/a	N/a	HDD3 8 x 2.5
2 x 3.5" 4xHDD BP	HDD1 4x3.5		HDD1 4x3.5		peripheral bay		

	P8	P9	P10	P11	P5	P6	P7
	1x4	1x4	1x4	1x4	1x5	1x5	1x4
	18						
1 x 3.5" 8xHDD BP	HDD1 8x3.5		N/a	N/a	peripheral bay		
8 x 3.5" fixed SATA	2xfixed	2xfixed	2xfixed	2xfixed	peripheral bay		
8 x 3.5" fixed SAS	2xfixed	2xfixed	2xfixed	2xfixed	peripheral bay		

13.4.2.7 DC/DC Converters Loading

The following table defines power and current ratings of three DC/DC converters located on the PDB, each powered from +12V rail. The 3 converters meet both static and dynamic voltage regulation requirements for the minimum and maximum loading conditions.

Table 124. DC/DC Converters Load Ratings

	+12VDC Input DC/DC Converters		
	+3.3V Converter	+5V Converter	-12V Converter
MAX Load	25A	25A	0.5A
MIN Static/Dynamic Load	0A	0A	0A
Max Output Power	3.3V x25A =82.5W	5V x25A =125W	12V x0.5A =6W

13.4.2.8 5VSB Loading

There is also one DC/DC converter that converts the 12V standby into 5V standby.

Table 125. 5VSB Loading

	12V stby/5V stby DC/DC Converters
MAX Load	8A
MIN Static/Dynamic Load	0.1
Max Output Power	5V x8A =40W

13.4.2.9 DC/DC Converters Voltage Regulation

The DC/DC converters' output voltages stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise specified in Table 145. The 3.3V and 5V outputs are measured at the remote sense point, all other voltages measured at the output harness connectors.

Table 126. Voltage Regulation Limits

Converter output	Tolerance	Min	Nom	Max	Units
+ 3.3VDC	-4%/+5%	+3.20	+3.30	+3.46	VDC
+ 5VDC	-4%/+5%	+4.80	+5.00	+5.25	VDC
5Vstby	-4%/+5%	+4.80	+5.00	+5.25	VDC

13.4.2.10 DC/DC Converters Dynamic Loading

The output voltages remains within limits specified in table above for the step loading and capacitive loading specified in the table below. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load shown in Tables 143 and 144.

Table 127. Transient Load Requirements

Output	Max Δ Step Load Size	Max Load Slew Rate	Test capacitive Load
+ 3.3VDC	5A	0.25 A/µs	250 µF
+ 5VDC	5A	0.25 A/µs	400 µF
+5Vsb	0.5A	0.25A/µs	20 µF

13.4.2.11 DC/DC Converter Capacitive Loading

The DC/DC converters is stable and meet all requirements with the following capacitive loading ranges. Minimum capacitive loading applies to static load only.

Table 128. Capacitive Loading Conditions

Converter output	Min	Max	Units
+3.3VDC	250	6800	µF
+5VDC	400	4700	µF
5Vstby	20	350	µF

13.4.2.12 DC/DC Converters Closed Loop stability

Each DC/DC converter is unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in Section 13.5.2.11. A minimum of: **45 degrees phase margin** and **-10dB-gain margin** is required. The PDB provides proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

13.4.2.13 Common Mode Noise

The Common Mode noise on any output does not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz.

- The measurement shall be made across a 100Ω resistor between each of DC outputs, including ground, at the DC power connector and chassis ground (power subsystem enclosure).
- The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

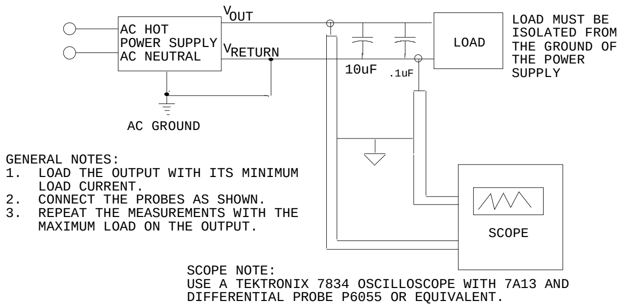
13.4.2.14 Ripple/Noise

The maximum allowed ripple/noise output of each DC/DC Converter is defined in below Table 95. This is measured over a bandwidth of 0Hz to 20MHz at the PDB output connectors. A 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor are placed at the point of measurement.

Table 129. Ripple and Noise

+3.3V	+5V	-12V	+5VSB
50mVp-p	50mVp-p	120mVp-p	50mVp-p

The test set-up shall be as shown below.



Note:

When performing this test, the probe clips and capacitors should be located close to the load.

Figure 63. Differential Noise test setup

13.4.2.15 Timing Requirements

Below are timing requirements for the power on/off of the PDB DC/DC converters. The +3.3V, +5V and +12V output voltages should start to rise approximately at the same time. All outputs must rise monotonically.

Table 130. Output Voltage Timing

Description	Min	Max	Units
Output voltage rise time for each main output; 3.3V, 5V, -12V and 5Vstby.	1.0	20	msec
The main DC/DC converters (3.3V, 5V, -12V) shall be in regulation limits within this time after the 12V input has reached 11.4V.		20	msec
The main DC/DC converters (3.3V, 5V, -12V) must drop below regulation limits within this time after the 12V input has dropped below 11.4V.		20	msec
The 5Vstby converter shall be in regulation limits within this time after the 12Vstby has reach 11.4V.		20	msec
The 5Vstby converter must power off within this time after the 12Vstby input has dropped below 11.4V.		20	msec

13.4.2.16 Residual Voltage Immunity in Standby Mode

Each DC/DC converter is immune to any residual voltage placed on its respective output (typically a leakage voltage through the system from standby output) up to 500mV. This residual voltage does not have any adverse effect on each DC/DC converter, such as: no additional power dissipation or over-stressing/over-heating any internal components or adversely affecting the turn-on performance (no protection circuits tripping during turn on).

While in Stand-by mode, at no load condition, the residual voltage on each DC/DC converter output does not exceed 100mV.

13.4.3 Protection Circuits

The PDB shall shut down all the DC/DC converters on the PDB and the power supply (by PSON) if there is a fault condition on the PDB (OVP or OCP). If the PDB DC/DC converter latches off due to a protection circuit tripping, an AC cycle OFF for 15sec min or a PSON# cycle HIGH for 1sec shall be able to reset the power supply and the PDB.

13.4.3.1 Over-Current Protection (OCP)/240VA Protection

Each DC/DC converter output on PDB has individual OCP protection circuits. The PS+PDB combo shall shutdown and latch off after an over current condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the PDB harness connectors. The DC/DC converters shall not be damaged from repeated power cycling in this condition. Also, the +12V output from the power supply is divided on the PDB into 4 channels and +12V4 is limited to 240VA of power. There are current sensors and limit circuits to shut down the entire PS+PDB combo if the limit is exceeded. The limits are listed in below table. -12V and 5VSB is protected under over current or shorted conditions so that no damage can occur to the power supply. Auto-recovery feature is a requirement on 5VSB rail.

Table 131. PDB Over Current Protection Limits/240VA Protection

Output Voltage	Min OCP Trip Limits	Max OCP Trip Limits	Usage	Connectors
+3.3V	27A	32A	PCIe, Misc	P1, P5, P6
+5V	27A	32A	PCIe, HDD, Misc	P1, P5, P6
+12V1	91A	100A	CPU1 + memory Fans, Misc	P1-P3, P12
+12V2	76A	100A	HDD and peripherals	P13-P16
+12V3	18A	20A		P5-P11

13.4.3.2 Over Voltage Protection (OVP)

Each DC/DC converter output on PDB have individual OVP protection circuits built in and it shall be locally sensed. The PS+PDB combo shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. Table 98 contains the over voltage limits. The values are measured at the PDB harness connectors. The voltage shall never exceed the maximum levels when measured at the power pins of the output harness connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the PDB connector.

Table 132. Over Voltage Protection (OVP) Limits

Output voltage	OVP min (v)	OVP max (v)
+3.3V	3.9	4.8
+5V	5.7	6.5
-12V	-13.3	-15.5
+5VSB	5.7	6.5

13.4.4 PWOK (Power OK) Signal

The PDB connects the PWOK signals from the power supply modules and the DC/DC converters to a common PWOK signal. This common PWOK signal connects to the PWOK pin on P1. The DC/DC convert PWOK signals have open collector outputs.

13.4.4.1 System PWOK requirements

The system will connect the PWOK signal to 3.3V or 5V by a pull-up resistor. The maximum sink current of the power supplies are 0.5mA. The minimum resistance of the pull-up resistor is stated below depending upon the motherboard's pull-up voltage. Refer to the CRPS power supply specification for signal details.

Table 133. System PWOK Requirements

Motherboard pull-up voltage	MIN resistance value (ohms)
5V	10K
3.3V	6.8K

13.4.5 PSON Signal

The PDB connects the power supplies PSON signals together and connect them to the PSON signal on P1.
Refer to the CRPS power supply specification for signal details.

13.4.6 PMBus

The PDB has no components on it to support PMBus. It only needs to connect the power supply PMBus signals (clock, data, SMBAlert#) and pass them to the 1x5 signal connector.

13.4.6.1 Addressing

The PDB address the power supply as follows on the PDB.
0 = open, 1 = grounded

Table 134. PDB addressing

	Power Supply Position 1	Power Supply Position 2
PDB addressing Address0/Address1	0/0	0/1
Power supply PMBus device address	B0h	B2h

14. Intel® Server System P4000CP Accessories

14.1 Intel® RAID C600 Upgrade Key

Intel® RAID C600 Upgrade Keys are used to enable additional storage features on Intel® Server Board S2600CP2/S2600CP4 and Intel® Server System P4000CP that use the Intel® C600 series chipset. Several types of Intel® RAID C600 Upgrade Keys are available. These keys are used for enabling different storage options and serve different purposes. Intel® RAID C600 Upgrade Keys do NOT work on Intel® Server Board S2600CP2J.

Table 135. Intel® RAID C600 Upgrade Key

Item	Product Code	Color of the key	Description
1	Default (No Key)	NA	Activate 4 ports (SATA only). Support software RAID which includes RSTe[1] RAID 0/1/10/5 and ESRT2[2] RAID 0/1/10.
2	RKSATA4R5	Black	Add RAID 5 support in ESRT2 based on item #1.
3	RKSATA8	Blue	Activate 4 ports (SATA only). Support software RAID which includes RSTe[1] RAID 0/1/10/5 and ESRT2[2] RAID 0/1/10.
4	RKSATA8R5	White	Add RAID 5 support in ESRT2 based on item #3.
5	RKSAS4	Green	Activate 4 ports (SAS/SATA). Support software RAID which includes RSTe[1] RAID 0/1/10 and ESRT2[2] RAID 0/1/10.
6	RKSAS4R5	Yellow	Add RAID 5 support in ESRT2 based on item #5.
7	RKSAS8	Orange	Activate 8 ports (SAS/SATA). Support software RAID which includes RSTe[1] RAID 0/1/10 and ESRT2[2] RAID 0/1/10.
8	RKSAS8R5	Purple	Add RAID 5 support in ESRT2 based on item #7.

Note[1]: RSTe - Intel® Rapid Storage Technology enterprise.
Note[2]: ESRT2 - Intel® Embedded Server RAID Technology II.

Intel® RAID C600 Upgrade keys enable software RAID, it does not require additional RAM nor does it use a backup battery. This key is the only hardware required to add additional RAID options to server boards. An Intel® RAID C600 key can be installed to Intel® Server Board S2600CP at the location as shown in the figure below.

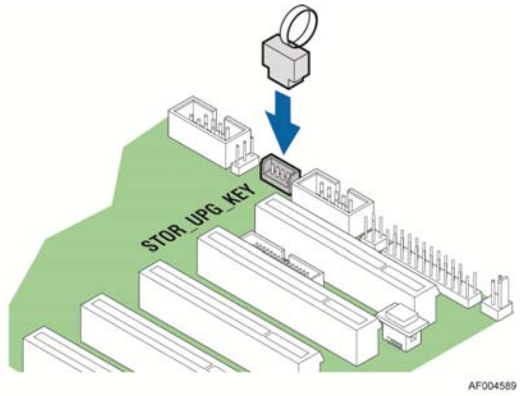


Figure 64. Intel® RAID C600 Key

14.2 Intel® Remote Management Module 4 (Intel® RMM4)

Intel® Remote Management Model 4 (RMM4) includes two components, Intel® Remote Management Module 4 Lite (RMM4 Lite) and Intel® Dedicated Server Management NIC (DMN). RMM4 Lite is the key that can enable advance features of server onboard Integrated BMC. DMN can provide a dedicated management LAN interface. This DMN is only for Integrated BMC management communication and cannot be shared with OS.

Table 136. Intel® Remote Management Module 4 (Intel® RMM4)

Intel® Product Code	Description	Kit Contents	Benefits
AXXRMM4LITE	Intel® Remote Management Module 4 Lite	RMM4 Lite Activation Key	Enables KVM and media redirection by onboard NIC
AXXRMM4	Intel® Remote Management Module 4	RMM4 Lite Activation Key Dedicated NIC Port Module	Dedicated NIC for management traffic, KVM and media Redirection.

The RMM4 can be installed in Intel® Server System P4000CP at the board and chassis locations as shown in the figure below.

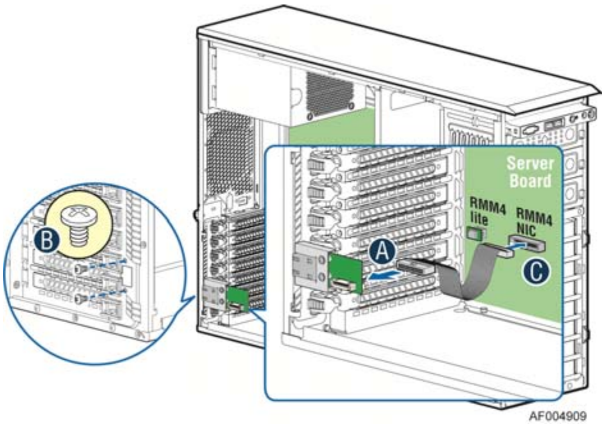


Figure 65. Intel® RMM4

For more detail information of RMM4, please refer to *Intel® Remote Management Module 4 Technical Product Specification.*

14.3 Rack Options

Intel® Server System P4308CP4MHEN, P4308CP4MHGC and P4208CP4MHGC can be converted to rack systems with the rack bezel and rack rail options.

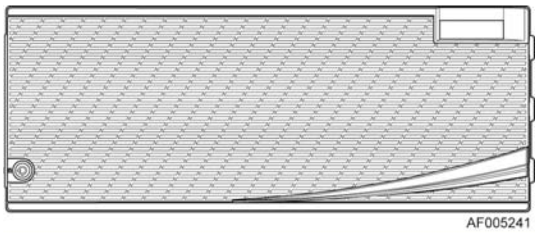


Figure 66. Intel® RMM4

Rack rail options include AXXELVRAIL and AXX3U5UPRAIL.

Table 137. AXXELVRAIL and AXX3U5UPRAIL Rack Options

AXXELVRAIL	AXX3U5UPRAIL
▪ 3U to 5U compatible ▪ 100 lbs max support weight ▪ Tool-less chassis attach (optional screws) ▪ Tools required to attach rails to rack ▪ 1/2 extension from rack	▪ 3U to 5U compatible ▪ 100 lbs max support weight ▪ Tool-less installation ▪ Full extension from rack ▪ Stab in system install ▪ Optional cable management arm support

AXX3U5UCMA

- Cable Management Arm support AXX3U5UPRAIL

15. Design and Environmental Specifications

15.1 Intel® Server Board S2600CP Design Specifications

The following table defines the Intel® Server Board S2600CP operating and non-operating environmental limits. Operation of the Intel® Server Board S2600CP at conditions beyond those shown in the following table may cause permanent damage to the system. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 138. Server Board Design Specifications

Operating Temperature	0º C to 55º C [1] (32º F to 131º F)
Non-Operating Temperature	-40º C to 70º C (-40º F to 158º F)
DC Voltage	± 5% of all nominal voltages
Shock (Unpackaged)	Trapezoidal, 35g, 170 inches/sec
Shock (Packaged) < 20 pounds 20 to < 40 pounds 40 to < 80 pounds 80 to < 100 pounds 100 to < 120 pounds 120 pounds	 36 inches 30 inches 24 inches 18 inches 12 inches 9 inches
Vibration (Unpackaged)	5 Hz to 500 Hz 3.13 g RMS random

Note:

1. Chassis design must provide proper airflow to avoid exceeding the processor maximum case temperature.

Disclaimer Note: Intel® ensures the unpackaged server board and system meet the shock requirement mentioned above through its own chassis development and system configuration. It is the responsibility of the system integrator to determine the proper shock level of the board and system if the system integrator chooses different system configuration or different chassis. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

Disclaimer Note: Intel Corporation server boards contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel® server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel® developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible, if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

15.2 Intel® Server System P4000CP Environmental Limits

The following table defines the Intel® Server System P4000CP system level operating and non-operating environmental limits. Operation of the Intel® Server System P4000CP at conditions beyond those shown in the following table may cause permanent damage to the system. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 139. System Environmental Limits Summary

Parameter		Limits
Temperature		
	Operating	10º C to 35º C (50º F to 95º F) with the maximum rate of change not to exceed 10°C per hour
	Non-Operating	-40º C to 70º C (-40º F to 158º F)
Humidity		
	Non-Operating	50% to 90%, non-condensing with a maximum wet bulb of 28° C (at temperatures from 25° C to 35° C)
Shock		
	Operating	Half sine, 2g, 11 mSec
	Unpackaged	Trapezoidal, 25 g, velocity change is based on packaged weight
	Packaged	Product Weight: ≥ 40 to < 80 Non-palletized Free Fall Height = 18 inches Palletized (single product) Free Fall Height = NA
Vibration		
	Unpackaged	5 Hz to 500 Hz 2.20 g RMS random
	Packaged	5 Hz to 500 Hz 1.09 g RMS random
AC-DC		
	Voltage	90 Hz to 132 V and 180 V to 264 V
	Frequency	47 Hz to 63 Hz
	Source Interrupt	No loss of data for power line drop-out of 12 mSec
	Surge Non-operating and operating	Unidirectional
	Line to earth Only	AC Leads 2.0 kV I/O Leads 1.0 kV DC Leads 0.5 kV
ESD		
	Air Discharged	12.0 kV
	Contact Discharge	8.0 kV
Acoustics Sound Power Measured		
	Power in Watts	<300 W ≥300 W ≥600 W ≥1000 W
	Servers/Rack Mount BA	7.0 7.0 7.0 7.0

15.3 MTBF

The following is the calculated Mean Time Between Failures (MTBF) 30°C (ambient air). These values are derived using a historical failure rate and multiplied by factors for application, electrical and/or thermal stress and for device maturity. You should view MTBF estimates as "reference numbers" only.

- Calculation Model: Telcordia* Issue 2, method I case 3
- Operating Temperature: Server in 40° C ambient air
- Operating Environment: Ground Benign, Controlled
- Duty Cycle: 100%
- Quality Level: II

Table 140. MTBF Estimate

Assembly	Failure Rate	MTBF
Mother board	4,617.71	216,557
Integrated Circuits	1,756.55	569,298
Transistor_Bipolar	6.04	165,508,840
Transistor_MOSFET	418.11	2,391,663
Diodes	20.26	49,353,370
Diodes_LED	90.09	11,099,561
Resistors	960.02	1,041,635
Capacitors	213.71	4,679,143
E-Cap	571.98	1,748,312
Inductors	109.62	9,122,408
Connections	623.35	1,604,218
Misc	73.08	13,682,860

15.4 Server Board Power Distribution

This section provides power supply design guidelines for a system using the Intel® Server Board S2600CP. The following diagram shows the power distribution implemented on these server boards. For power supply data, please refer to the chapter that describe the power system options including 550W or 750W power supply. Please note the intent of 550W/750W power supply data is to provide customers with a guide to assist in defining and/or selecting a power supply for custom server platform designs that utilize the server boards detailed in this document.

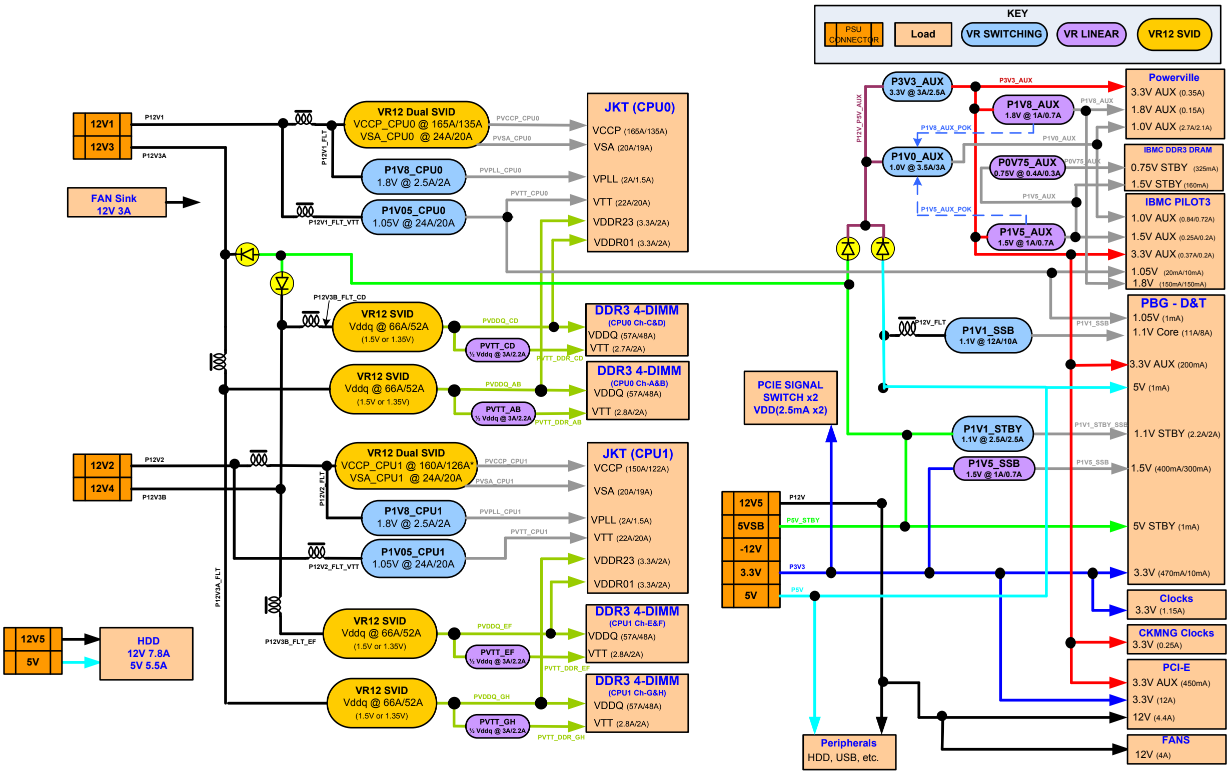


Figure 67. Power Distribution Block Diagram

Appendix A: Integration and Usage Tips

- When adding or removing components or peripherals from the server board, AC power must be removed. With AC power plugged into the server board, 5-V standby is still present even though the server board is powered off.
- This server board supports The Intel® Xeon® Processor E5-2600 product family with a Thermal Design Power (TDP) of up to and including 135 Watts. Previous generations of the Intel® Xeon® processors are not supported.
- Processors must be installed in order. CPU 1 must be populated for the server board to operate.
- On the back edge of the server board are eight diagnostic LEDs that display a sequence of amber POST codes during the boot process. If the server board hangs during POST, the LEDs display the last POST event run before the hang.
- This server board only supports registered DDR3 DIMMs (RDIMMs) and unbuffered DDR3 DIMMs (UDIMMs). Mixing of RDIMMs and UDIMMs is not supported.
- For the best performance, the number of DDR3 DIMMs installed should be balanced across both processor sockets and memory channels. For example, a two-DIMM configuration performs better than a one-DIMM configuration. In a two-DIMM configuration, DIMMs should be installed in DIMM sockets A1 and D1.
- The Intel® Remote Management Module 4 (Intel® RMM4) connector is not compatible with any previous versions of the Intel® Remote Management Module (Product Order Code – AXXRMM, AXXRMM2, and AXXRMM3).
- Clear the CMOS with AC power cord plugged. Removing the AC power before performing the CMOS clear operation causes the system to automatically power up and immediately power down after the CMOS clear procedure is followed and AC power is re-applied. If this happens, remove the AC power cord, wait 30 seconds, and then re-connect the AC power cord. Power up the system and proceed to the <F2> BIOS Setup utility to reset the desired settings.
- Normal Integrated BMC functionality is disabled with the BMC Force Update jumper set to the “enabled” position (pins 2-3). The server should never be run with the BMC Force Update jumper set in this position and should only be used when the standard firmware update process fails. This jumper should remain in the default (disabled) position (pins 1-2) when the server is running normally.
- When performing a normal BIOS update procedure, the BIOS recovery jumper must be set to its default position (pins 1-2).

Appendix B: Compatible Intel® Server Chassis

The Intel ® Server Board S2600CP can be used inside Intel ® Server Chassis P4000M family.

Table 141. Compatible Intel® Server Chassis

Chassis Name	System Fans	Storage Drives	Power Supply(s)
P4308XXMFEN	Two Fixed Fans	Eight 3.5" Fixed Drive Trays	550W Fixed PSU
P4308XXMHEN	Two Fixed Fans	Eight 3.5" Hotswap Drive Bay	550W Fixed PSU
P4308XXMFGN	Two Fixed Fans	Eight 3.5" Fixed Drive Trays	One 750W CRPS
P4308XXMHGC	Five Redundant Fans	Eight 3.5" Hotswap Drive Bay	Two 750W CRPS
P4308XXMHJC	Five Redundant Fans	Eight 3.5" Hotswap Drive Bay	Two 1200W CRPS
P4208XXMHEN	Two Fixed Fans	Eight 2.5" Hotswap Drive Bay	550W Fixed PSU
P4208XXMHDR	Two Fixed Fans	Eight 2.5" Hotswap Drive Bay	Two 460W CRPS
P4208XXMHGR	Two Fixed Fans	Eight 2.5" Hotswap Drive Bay	Two 750W CRPS
P4208XXMHGC	Five Redundant Fans	Eight 2.5" Hotswap Drive Bay	Two 750W CRPS
P4216XXMHJC	Five Redundant Fans	Sixteen 2.5" Hotswap Drive Bay	Two 1200W CRPS

Appendix C: BMC Sensor Tables

This appendix lists the sensor identification numbers and information about the sensor type, name, supported thresholds, assertion and de-assertion information, and a brief description of the sensor purpose. See the *Intelligent Platform Management Interface Specification, Version 2.0* for sensor and event/reading-type table information.

Sensor Type Codes

Sensor table given below lists the sensor identification numbers and information regarding the sensor type, name, supported thresholds, assertion and de-assertion information, and a brief description of the sensor purpose. Refer to the *Intelligent Platform Management Interface Specification, Version 2.0* for sensor and event/reading-type table information.

Sensor Type

The sensor type references the values in the Sensor Type Codes table in the *Intelligent Platform Management Interface Specification* Second Generation v2.0. It provides a context to interpret the sensor.

Event/Reading Type

The event/reading type references values from the Event/Reading Type Code Ranges and the Generic Event/Reading Type Code tables in the *Intelligent Platform Management Interface Specification Second Generation* v2.0. Digital sensors are specific type of discrete sensors that only have two states.

Event Thresholds/Triggers

The following event thresholds are supported for threshold type sensors:

[u,l][nr,c,nc] upper non-recoverable, upper critical, upper non-critical, lower non-recoverable, lower critical, lower non-critical uc, lc upper critical, lower critical

Event triggers are supported event-generating offsets for discrete type sensors. The offsets can be found in the *Generic Event/Reading Type Code* or *Sensor Type Code* tables in the *Intelligent Platform Management Interface Specification Second Generation v2.0*, depending on whether the sensor event/reading type is generic or a sensor-specific response.

Assertion/Deassertion

Assertion and de-assertion indicators reveal the type of events this sensor generates:

As: Assertion

De: De-assertion

Readable Value/Offsets

Readable value indicates the type of value returned for threshold and other non-discrete type sensors.

Readable offsets indicate the offsets for discrete sensors that are readable by means of the *Get Sensor Reading* command. Unless otherwise indicated, event triggers are readable. Readable offsets consist of the reading type offsets that do not generate events.

Event Data

Event data is the data that is included in an event message generated by the associated sensor. For threshold-based sensors, these abbreviations are used:

R: Reading value

T: Threshold value

Rearm Sensors

The rearm is a request for the event status for a sensor to be rechecked and updated upon a transition between good and bad states. Rearming the sensors can be done manually or automatically. This column indicates the type supported by the sensor. The following abbreviations are used in the comment column to describe a sensor:

A: Auto-rearm

M: Manual rearm

I: Rearm by init agent

Default Hysteresis

The hysteresis setting applies to all thresholds of the sensor. This column provides the count of hysteresis for the sensor, which can be 1 or 2 (positive or negative hysteresis).

Criticality

Criticality is a classification of the severity and nature of the condition. It also controls the behavior of the front panel status LED.

Standby

Some sensors operate on standby power. These sensors may be accessed and/or generate events when the main (system) power is off, but AC power is present.

Note: All sensors listed below may not be present on all platforms. Please check platform EPS section for platform applicability and platform chassis section for chassis specific sensors. Redundancy sensors will be only present on systems with appropriate hardware to support redundancy (for instance, fan or power supply).

Table 142. Integrated BMC Core Sensors

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Power Unit Status *(Pwr Unit Status)*	01h	All	Power Unit 09h	Sensor Specific 6Fh	00 - Power down	OK	As and De	–	Trig Offset	A	X
					02 - 240 VA power down	Fatal					
					04 - A/C lost	OK					
					05 - Soft power control failure	Fatal					
					06 - Power unit failure						
Power Unit Redundancy[1] *(Pwr Unit Redund)*	02h	Chassis-specific	Power Unit 09h	Generic 0Bh	00 - Fully Redundant	OK	As and De	–	Trig Offset	M	X
					01 - Redundancy lost	Degraded					
					02 - Redundancy degraded	Degraded					
					03 - Non-redundant: sufficient resources. Transition from full redundant state.	Degraded					
					04 – Non-redundant: sufficient resources. Transition from insufficient state.	Degraded					
					05 - Non-redundant: insufficient resources	Fatal					

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
					06 – Redundant: degraded from fully redundant state.	Degraded					
					07 – Redundant: Transition from non-redundant state.	Degraded					
IPMI Watchdog *(IPMI Watchdog)*	03h	All	Watchdog 2 23h	Sensor Specific 6Fh	00 - Timer expired, status only 01 - Hard reset 02 - Power down 03 - Power cycle 08 - Timer interrupt	OK	As	–	Trig Offset	A	X
Physical Security *(Physical Scrty)*	04h	Chassis Intrusion is chassis-specific	Physical Security 05h	Sensor Specific 6Fh	00 - Chassis intrusion 04 - LAN leash lost	Degraded OK	As and De	–	Trig Offset	A	X
FP Interrupt *(FP NMI Diag Int)*	05h	Chassis - specific	Critical Interrupt 13h	Sensor Specific 6Fh	00 - Front panel NMI/diagnostic interrupt	OK	As	–	Trig Offset	A	–
SMI Timeout *(SMI Timeout)*	06h	All	SMI Timeout F3h	Digital Discrete 03h	01 – State asserted	Fatal	As and De	–	Trig Offset	A	–
System Event Log *(System Event Log)*	07h	All	Event Logging Disabled 10h	Sensor Specific 6Fh	02 - Log area reset/cleared	OK	As	–	Trig Offset	A	X
System Event *(System Event)*	08h	All	System Event 12h	Sensor Specific 6Fh	02 - Undetermined system H/W failure 04 – PEF action	Fatal OK	As and De As	-	Trig Offset	A	X

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Button Sensor *(Button)*	09h	All	Button/Switch 14h	Sensor Specific 6Fh	00 – Power Button 02 – Reset Button	OK	AS	–	Trig Offset	A	X
BMC Watchdog	0Ah	All	Mgmt System Health 28h	Digital Discrete 03h	01 – State Asserted	Degraded	As	–	Trig Offset	A	-
Voltage Regulator Watchdog (VR Watchdog)	0Bh	All	Voltage 02h	Digital Discrete 03h	01 – State Asserted	Fatal	As and De	–	Trig Offset	M	X
Fan Redundancy[1] *(Fan Redundancy)*	0Ch	Chassis-specific	Fan 04h	Generic 0Bh	00 - Fully redundant	OK	As and De	–	Trig Offset	A	–
					01 - Redundancy lost	Degraded					
					02 - Redundancy degraded	Degraded					
					03 - Non-redundant: Sufficient resources. Transition from redundant	Degraded					
					04 - Non-redundant: Sufficient resources. Transition from insufficient.	Degraded					
					05 - Non-redundant: insufficient resources.	Non-Fatal					
					06 – Non-Redundant: degraded from fully redundant.	Degraded					
					07 - Redundant degraded from non-redundant	Degraded					
SSB Thermal Trip *(SSB Therm Trip)*	0Dh	All	Temperature 01h	Digital Discrete 03h	01 – State Asserted	Fatal	As and De	–	Trig Offset	M	X

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
IO Module Presence (IO Mod Presence)	0Eh	Platform-specific	Module/Board 15h	Digital Discrete 08h	01 – Inserted/Present	OK	As and De	–	Trig Offset	M	-
SAS Module Presence (SAS Mod Presence)	0Fh	Platform-specific	Module/Board 15h	Digital Discrete 08h	01 – Inserted/Present	OK	As and De	–	Trig Offset	M	X
BMC Firmware Health (BMC FW Health)	10h	All	Mgmt Health 28h	Sensor Specific 6Fh	04 – Sensor Failure	Degraded	As	-	Trig Offset	A	X
System Airflow (System Airflow)	11h	All	Other Units 0Bh	Threshold 01h	–	–	–	Analog	–	–	–
FW Update Status	12h	All	Version Change 2Bh	OEM defined x70h	00h→Update started 01h→Update completed successfully. 02h→Update failure	OK	As	_	Trig Offset	A	_
IO Module2 Presence (IO Mod2 Presence)	13h	Platform-specific	Module/Board 15h	Digital Discrete 08h	01 – Inserted/Present	OK	As and De	–	Trig Offset	M	-
Baseboard Temperature 5 *(Platform Specific)*	14h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Baseboard Temperature 6 *(Platform Specific)*	15h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
IO Module2 Temperature (I/O Mod2 Temp)	16h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
PCI Riser 3 Temperature (PCI Riser 5 Temp)	17h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
PCI Riser 4 Temperature (PCI Riser 4 Temp)	18h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Baseboard +1.05V Processor3 Vccp *(BB +1.05Vccp P3)*	19h	Platform-specific	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.05V Processor4 Vccp *(BB +1.05Vccp P4)*	1Ah	Platform-specific	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard Temperature 1 *(Platform Specific)*	20h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Front Panel Temperature *(Front Panel Temp)*	21h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
SSB Temperature *(SSB Temp)*	22h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Baseboard Temperature 2 *(Platform Specific)*	23h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Baseboard Temperature 3 *(Platform Specific)*	24h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Baseboard Temperature 4 *(Platform Specific)*	25h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
IO Module Temperature (I/O Mod Temp)	26h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
PCI Riser 1 Temperature (PCI Riser 1 Temp)	27h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
IO Riser Temperature (IO Riser Temp)	28h	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Hot-swap Backplane 1 Temperature (HSBP 1 Temp)	29h	Chassis-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Hot-swap Backplane 2 Temperature (HSBP 2 Temp)	2Ah	Chassis-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Hot-swap Backplane 3 Temperature (HSBP 3 Temp)	2Bh	Chassis-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
PCI Riser 2 Temperature (PCI Riser 2 Temp)	2Ch	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
SAS Module Temperature (SAS Mod Temp)	2Dh	Platform-specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Exit Air Temperature (Exit Air Temp)	2Eh	Chassis and Platform Specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Network Interface Controller Temperature (LAN NIC Temp)	2Fh	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Fan Tachometer Sensors (Chassis specific sensor names)	30h–3Fh	Chassis and Platform Specific	Fan 04h	Threshold 01h	[l] [c,nc]	nc = Degraded c = Non-fatal[2]	As and De	Analog	R, T	M	-
Fan Present Sensors *(Fan x Present)*	40h–4Fh	Chassis and Platform Specific	Fan 04h	Generic 08h	01 - Device inserted	OK	As and De	-	Triggered Offset	Auto	-
Power Supply 1 Status *(PS1 Status)*	50h	Chassis-specific	Power Supply 08h	Sensor Specific 6Fh	00 - Presence	OK	As and De	–	Trig Offset	A	X
					01 - Failure	Degraded					
					02 – Predictive Failure	Degraded					
					03 - A/C lost	Degraded					
					06 – Configuration error	OK					
Power Supply 2 Status *(PS2 Status)*	51h	Chassis-specific	Power Supply 08h	Sensor Specific 6Fh	00 - Presence	OK	As and De	–	Trig Offset	A	X
					01 - Failure	Degraded					
					02 – Predictive Failure	Degraded					
					03 - A/C lost	Degraded					
					06 – Configuration error	OK					
Power Supply 1 AC Power Input (PS1 Power In)	54h	Chassis-specific	Other Units 0Bh	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 2 AC Power Input (PS2 Power In)	55h	Chassis-specific	Other Units 0Bh	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 1 +12V % of Maximum Current Output (*PS1 Curr Out %*)	58h	Chassis-specific	Current 03h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Power Supply 2 +12V % of Maximum Current Output (*PS2 Curr Out %*)	59h	Chassis-specific	Current 03h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 1 Temperature (*PS1 Temperature*)	5Ch	Chassis-specific	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 2 Temperature (*PS2 Temperature*)	5Dh	Chassis-specific	Temperature	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Hard Disk Drive 16 - 24 Status (HDD 16 - 24 Status)	60h – 68h	Chassis-specific	Drive Slot 0Dh	Sensor Specific 6Fh	00 - Drive Presence	OK	As and De	–	Trig Offset	A	X
					01- Drive Fault	Degraded					
					07 - Rebuild/Remap in progress	Degraded					
	69h - 6Bh	Chassis-specific	Microcontroller 16h	Discrete 0Ah	04- transition to Off Line	Degraded		–	Trig Offset		X
Processor 1 Status (*P1 Status*)	70h	All	Processor 07h	Sensor Specific 6Fh	01 - Thermal trip	Fatal	As and De	–	Trig Offset	M	X
					07 - Presence	OK					
Processor 2 Status (*P2 Status*)	71h	All	Processor 07h	Sensor Specific 6Fh	01 - Thermal trip	Fatal	As and De	–	Trig Offset	M	X
					07 - Presence	OK					
Processor 3 Status (*P3 Status*)	72h	Platform-specific	Processor 07h	Sensor Specific 6Fh	01 - Thermal trip	Fatal	As and De	–	Trig Offset	M	X
					07 - Presence	OK					
Processor 4 Status (*P4 Status*)	73h	Platform-specific	Processor 07h	Sensor Specific 6Fh	01 - Thermal trip	Fatal	As and De	–	Trig Offset	M	X
					07 - Presence	OK					

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Processor 1 Thermal Margin (P1 Therm Margin)	74h	All	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Processor 2 Thermal Margin (P2 Therm Margin)	75h	All	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Processor 3 Thermal Margin (P3 Therm Margin)	76h	Platform-specific	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Processor 4 Thermal Margin (P4 Therm Margin)	77h	Platform-specific	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Processor 1 Thermal Control % (*P1 Therm Ctrl %*)	78h	All	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	Trig Offset	A	–
Processor 2 Thermal Control % (*P2 Therm Ctrl %*)	79h	All	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	Trig Offset	A	–
Processor 3 Thermal Control % (*P3 Therm Ctrl %*)	7Ah	Platform-specific	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	Trig Offset	A	–
Processor 4 Thermal Control % (*P4 Therm Ctrl %*)	7Bh	Platform-specific	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	Trig Offset	A	–
Processor 1 ERR2 Timeout (P1 ERR2)	7Ch	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	fatal	As and De	–	Trig Offset	A	–
Processor 2 ERR2 Timeout (P2 ERR2)	7Dh	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	fatal	As and De	–	Trig Offset	A	–
Processor 3 ERR2 Timeout (P3 ERR2)	7Eh	Platform-specific	Processor 07h	Digital Discrete 03h	01 – State Asserted	fatal	As and De	–	Trig Offset	A	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Processor 4 ERR2 Timeout (P4 ERR2)	7Fh	Platform-specific	Processor 07h	Digital Discrete 03h	01 – State Asserted	fatal	As and De	–	Trig Offset	A	–
Catastrophic Error *(CATERR)*	80h	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	fatal	As and De	–	Trig Offset	M	–
Processor1 MSID Mismatch *(P1 MSID Mismatch)*	81h	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	fatal	As and De	–	Trig Offset	M	–
Processor Population Fault *(CPU Missing)*	82h	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	Fatal	As and De	–	Trig Offset	M	–
Processor 1 DTS Thermal Margin (P1 DTS Therm Mgn)	83h	All	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Processor 2 DTS Thermal Margin (P2 DTS Therm Mgn)	84h	All	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Processor 3 DTS Thermal Margin (P3 DTS Therm Mgn)	85h	All	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Processor 4 DTS Thermal Margin (P4 DTS Therm Mgn)	86h	All	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Processor2 MSID Mismatch *(P2 MSID Mismatch)*	87h	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	fatal	As and De	–	Trig Offset	M	–
Processor 1 VRD Temperature (*P1 VRD Hot*)	90h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	M	–
Processor 2 VRD Temperature (*P2 VRD Hot*)	91h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	M	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Processor 3 VRD Temperature (P3 VRD Hot)	92h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	M	–
Processor 4 VRD Temperature (P4 VRD Hot)	93h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	M	–
Processor 1 Memory VRD Hot 0-1 (P1 Mem01 VRD Hot)	94h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	A	–
Processor 1 Memory VRD Hot 2-3 (P1 Mem23 VRD Hot)	95h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	A	–
Processor 2 Memory VRD Hot 0-1 (P2 Mem01 VRD Hot)	96h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	A	–
Processor 2 Memory VRD Hot 2-3 (P2 Mem23 VRD Hot)	97h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	A	–
Processor 3 Memory VRD Hot 0-1 (P3 Mem01 VRD Hot)	98h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	A	–
Processor 3 Memory VRD Hot 2-3 (P4 Mem23 VRD Hot)	99h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	A	–
Processor 4 Memory VRD Hot 0-1 (P4 Mem01 VRD Hot)	9Ah	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	A	–
Processor 4 Memory VRD Hot 2-3 (P4 Mem23 VRD Hot)	9Bh	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Non-fatal	As and De	–	Trig Offset	A	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Power Supply 1 Fan Tachometer 1 *(PS1 Fan Tach 1)*	A0h	Chassis-specific	Fan 04h	Generic – digital discrete	01 – State Asserted	Non-fatal	As and De	-	Trig Offset	M	-
Power Supply 1 Fan Tachometer 2 *(PS1 Fan Tach 2)*	A1h	Chassis-specific	Fan 04h	Generic – digital discrete	01 – State Asserted	Non-fatal	As and De	-	Trig Offset	M	-
Power Supply 2 Fan Tachometer 1 *(PS2 Fan Tach 1)*	A4h	Chassis-specific	Fan 04h	Generic – digital discrete	01 – State Asserted	Non-fatal	As and De	-	Trig Offset	M	-
Power Supply 2 Fan Tachometer 2 *(PS2 Fan Tach 2)*	A5h	Chassis-specific	Fan 04h	Generic – digital discrete	01 – State Asserted	Non-fatal	As and De	-	Trig Offset	M	-
Processor 1 DIMM Aggregate Thermal Margin 1 *(P1 DIMM Thrm Mrgn1)*	B0h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Processor 1 DIMM Aggregate Thermal Margin 2 *(P1 DIMM Thrm Mrgn2)*	B1h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Processor 2 DIMM Aggregate Thermal Margin 1 *(P2 DIMM Thrm Mrgn1)*	B2h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Processor 2 DIMM Aggregate Thermal Margin 2 *(P2 DIMM Thrm Mrgn2)*	B3h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Processor 3 DIMM Aggregate Thermal Margin 1 *(P3 DIMM Thrm Mrgn1)*	B4h	Platform Specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Processor 3 DIMM Aggregate Thermal Margin 2 *(P3 DIMM Thrm Mrgn2)*	B5h	Platform Specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Processor 4 DIMM Aggregate Thermal Margin 1 *(P4 DIMM Thrm Mrgn1)*	B6h	Platform Specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Processor 4 DIMM Aggregate Thermal Margin 2 *(P4 DIMM Thrm Mrgn2)*	B7h	Platform Specific	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Fan Tachometer Sensors (Chassis specific sensor names)	BAh–BFh	Chassis and Platform Specific	Fan 04h	Threshold 01h	[l] [c,nc]	nc = Degraded c = Non-fatal[2]	As and De	Analog	R, T	M	-
Processor 1 DIMM Thermal Trip *(P1 Mem Thrm Trip)*	C0h	All	Memory 0Ch	Digital Discrete 03h	0A- Critical overtemperature	Fatal	As and De	–	Trig Offset	M	-
Processor 2 DIMM Thermal Trip *(P2 Mem Thrm Trip)*	C1h	All	Memory 0Ch	Digital Discrete 03h	0A- Critical overtemperature	Fatal	As and De	–	Trig Offset	M	-
Processor 3 DIMM Thermal Trip (P3 Mem Thrm Trip)	C2h	All	Memory 0Ch	Digital Discrete 03h	0A- Critical overtemperature	Fatal	As and De	–	Trig Offset	M	X
Processor 4 DIMM Thermal Trip (P4 Mem Thrm Trip)	C3h	All	Memory 0Ch	Digital Discrete 03h	0A- Critical overtemperature	Fatal	As and De	–	Trig Offset	M	X
Global Aggregate Temperature Margin 1 (Agg Therm Mrgn 1)	C8h	Platform Specific	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Global Aggregate Temperature Margin 2 (Agg Therm Mrgn 2)	C9h	Platform Specific	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Global Aggregate Temperature Margin 3 (Agg Therm Mrgn 3)	CAh	Platform Specific	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Global Aggregate Temperature Margin 4 (Agg Therm Mrgn 4)	CBh	Platform Specific	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Global Aggregate Temperature Margin 5 (Agg Therm Mrgn 5)	CCh	Platform Specific	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Global Aggregate Temperature Margin 6 (Agg Therm Mrgn 6)	CDh	Platform Specific	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Global Aggregate Temperature Margin 7 (Agg Therm Mrgn 7)	CEh	Platform Specific	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Global Aggregate Temperature Margin 8 (Agg Therm Mrgn 8)	CFh	Platform Specific	Temperature 01h	Threshold 01h	-	-	-	Analog	R, T	A	–
Baseboard +12V *(BB +12.0V)*	D0h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +5V *(BB +5.0V)*	D1h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +3.3V *(BB +3.3V)*	D2h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +5V Stand-by *(BB +5.0V STBY)*	D3h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Baseboard +3.3V Auxiliary *(BB +3.3V AUX)*	D4h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Baseboard +1.05V Processor1 Vccp *(BB +1.05Vccp P1)*	D6h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.05V Processor2 Vccp *(BB +1.05Vccp P2)*	D7h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Baseboard +1.5V P1 Memory AB VDDQ *(BB +1.5 P1MEM AB)*	D8h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.5V P1 Memory CD VDDQ *(BB +1.5 P1MEM CD)*	D9h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.5V P2 Memory AB VDDQ *(BB +1.5 P2MEM AB)*	DAh	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.5V P2 Memory CD VDDQ *(BB +1.5 P2MEM CD)*	DBh	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.8V Aux (BB +1.8V AUX)	DCh	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.1V Stand-by (BB +1.1V STBY)	DDh	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard CMOS Battery *(BB +3.3V Vbat)*	DEh	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.35V P1 Low Voltage Memory AB VDDQ *(BB +1.35 P1LV AB)*	E4h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.35V P1 Low Voltage Memory CD VDDQ *(BB +1.35 P1LV CD)*	E5h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +1.35V P2 Low Voltage Memory AB VDDQ *(BB +1.35 P2LV AB)*	E6h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–

Full Sensor Name (Sensor name in SDR)	Sensor #	Platform Applicability	Sensor Type	Event/Reading Type	Event Offset Triggers	Contrib. To System Status	Assert/ De-assert	Readable Value/Offsets	Event Data	Rearm	Stand-by
Baseboard +1.35V P2 Low Voltage Memory CD VDDQ *(BB +1.35 P2LV CD)*	E7h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +3.3V Riser 1 Power Good (BB +3.3 RSR1 PGD)	EAh	Platform Specific	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard +3.3V Riser 2 Power Good (BB +3.3 RSR2 PGD)	EBh	Platform Specific	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Hard Disk Drive 1 -15 Status (HDD 1 - 15 Status)	F0h - FEh	Chassis-specific	Drive Slot 0Dh	Sensor Specific 6Fh	00 - Drive Presence	OK	As and De	–	Trig Offset	A	X
					01- Drive Fault	Degraded					
					07 - Rebuild/Remap in progress	Degraded					

Notes:

1. Redundancy sensors will be only present on systems with appropriate hardware to support redundancy (for instance, fan or power supply).
2. This is only applicable when the system doesn't support redundant fans. When fan redundancy is supported, then the contribution to system state is driven by the fan redundancy sensor.

Appendix D: Platform Specific BMC Appendix

This is an addendum document to BMC core EPS. This document describes platform and chassis specific information.

Product ID

Bytes 11:12 (product ID) of Get Device ID command response: 4Ah 00h

IPMI Channel ID Assignments

Below table provides the information of BMC channels' assignments.

Table 143. IPMI Channel ID Assignments

Channel ID	Interface	Supports Sessions
0	Primary IPMB	No
1	LAN 1	Yes
2	LAN 2	Yes
3	LAN3 [1] (Provided by the Intel® Dedicated Server Management NIC)	Yes
4	Reserved	Yes
5	USB	No
6	Secondary IPMB	No
7	SMM	No
8– 0Dh	Reserved	–
0Eh	Self [2]	–
0Fh	SMS/Receive Message Queue	No

Notes:

1. Optional HW supported by the server system.
2. Refers to the actual channel used to send the request.

ACPI S3 Sleep State Support

Not support.

Processor Support for Intel® Server Board S2600CP

- Intel® Xeon® processor E5-2600 product family up to 135 Watt
- Intel® Xeon® processor E5-2600 v2 product family up to 135 Watt

Supported Chassis

- Intel® Server Chassis P4208XXM (Fixed fans, fixed or redundant PSUs)
- Intel® Server Chassis P4308XXM (Fixed fans, fixed or redundant PSUs)
- Intel® Server Chassis P4208XXM (Redundant fans, redundant PSUs)
- Intel® Server Chassis P4308XXM (Redundant fans, redundant PSUs)
- Intel® Server Chassis P4216XXM (Redundant fans, redundant PSUs)

Chassis-specific sensors

Table 144. Chassis-specific Sensors

Intel® Server Chassis	Fan Tachometer sensors	Fan Presence sensors	Physical security (Chassis intrusion) Sensor	FP interrupt (FP NMI Diag Int)
P4208XXM/ P4308XXM (Fixed fans, fixed or redundant PSUs)	System Fan 1(30h)	NA	Physical Scrty (04h)	FP NMI Diag Int (05h)
	System Fan 2(31h)	NA	NA	NA
P4208XXM/ P4308XXM/ P4216XXM (Redundant fans, redundant PSUs)	System Fan 1 (30h)	Fan 1 Present (40h)	Physical Scrty (04h)	FP NMI Diag Int (05h)
	System Fan 2 (31h)	Fan 2 Present (41h)	NA	NA
	System Fan 3 (32h)	Fan 3 Present (42h)	NA	NA
	System Fan 4 (33h)	Fan 4 Present (43h)	NA	NA
	System Fan 5 (34h)	Fan 5 Present (44h)	NA	NA

Hot-plug fan support

Supported on

- Intel® Server Chassis P4208XXM (Redundant fans, redundant PSUs)
- Intel® Server Chassis P4308XXM (Redundant fans, redundant PSUs)
- Intel® Server Chassis P4216XXM (Redundant fans, redundant PSUs)

Fan redundancy support

Supported on

- Intel® Server Chassis P4208XXM (Redundant fans, redundant PSUs)
- Intel® Server Chassis P4308XXM (Redundant fans, redundant PSUs)
- Intel® Server Chassis P4216XXM (Redundant fans, redundant PSUs)

Fan domain definition

Table 145. Fan Domain Definition

Chassis	Fan Domain	Major Components Cooled (Temperature sensor number)	Fans (Sensor number)
P4208XXM/ P4308XXM (Fixed fans, fixed or redundant PSUs)	0	▪ Memory channels C and D(B1h) ▪ Memory channels E and F(B2h) ▪ BMC Temp(23h) ▪ Memory VR(25h) ▪ Baseboard NIC(2Fh) ▪ Server South Bridge(22h) ▪ Hot-swap backplane 1(29h) ▪ Hot-swap backplane 2(2Ah)	System Fan 1(30h)
	1	▪ P1 Therm Margin(74h) ▪ P2 Therm Margin(75h) ▪ Memory channels A and B(B0h) ▪ Memory channels C and D(B1h)	System Fan 2(31h)

Chassis	Fan Domain	Major Components Cooled (Temperature sensor number)	Fans (Sensor number)
		▪ Memory channels E and F(B2h) ▪ Memory channels G and H(B3h) ▪ BB P2 VR Temp(24h) Memory VR(25h) Hot-swap backplane 1(29h) Hot-swap backplane 2(2Ah)	
P4208XXM/ P4308XXM/ P4216XXM (Redundant fans, redundant PSUs)	0	▪ BMC Temp(23h) ▪ Memory VR(25h) ▪ Baseboard NIC(2Fh) ▪ Server South Bridge(22h) ▪ Hot-swap backplane 1(29h) ▪ Hot-swap backplane 2(2Ah)	System Fan 1 (30h)
	1	▪ P1 Therm Margin(74h) ▪ P2 Therm Margin(75h) ▪ Memory channels C and D(B1h) ▪ Memory channels E and F(B2h) ▪ BMC Temp(23h) ▪ Memory VR(25h) ▪ Baseboard NIC(2Fh) ▪ Server South Bridge(22h) ▪ Hot-swap backplane 1(29h) ▪ Hot-swap backplane 2(2Ah)	System Fan 2 (31h)
	2	▪ P1 Therm Margin(74h) ▪ P2 Therm Margin(75h) ▪ Memory channels A and B(B0h) ▪ Memory channels C and D(B1h) ▪ Memory channels E and F(B2h) ▪ Memory channels G and H(B3h) ▪ BB P2 VR Temp(24h) ▪ Memory VR(25h) ▪ Hot-swap backplane 1(29h) ▪ Hot-swap backplane 2(2Ah)	System Fan 3 (32h)
	3	▪ P1 Therm Margin(74h) ▪ P2 Therm Margin(75h) ▪ Memory channels A and B(B0h) ▪ Memory channels C and D(B1h) ▪ Memory channels E and F(B2h) ▪ Memory channels G and H(B3h) ▪ BB P2 VR Temp(24h) ▪ Memory VR(25h) ▪ Hot-swap backplane 1(29h) ▪ Hot-swap backplane 2(2Ah)	System Fan 4 (33h)
	4	▪ P2 Therm Margin(75h) ▪ Memory channels A and B(B0h) ▪ Memory channels G and H(B3h) ▪ BB P2 VR Temp(24h)	System Fan 5 (34h)

Chassis	Fan Domain	Major Components Cooled (Temperature sensor number)	Fans (Sensor number)
		▪ Hot-swap backplane 1(29h) ▪ Hot-swap backplane 2(2Ah)	

HSC Availability

- Intel® Server Chassis P4208XXM (Fixed fans, fixed or redundant PSUs)
  - 8-bay 2.5” HDD – FXX8X25HSBP
- Intel® Server Chassis P4308XXM (Fixed fans, fixed or redundant PSUs)
  - 8-bay 3.5” HDD – FUP8X35HSBP
- Intel® Server Chassis P4208XXM (Redundant fans, redundant PSUs)
  - 8-bay 2.5” HDD – FXX8X25HSBP
- Intel® Server Chassis P4308XXM (Redundant fans, redundant PSUs)
  - 8-bay 3.5” HDD – FUP8X35HSBP
- Intel® Server Chassis P4216XXM (Redundant fans, redundant PSUs)
  - 8-bay 2.5” HDD – FXX8X25HSBP

Power unit support

- Intel® Server Chassis P4208XXM/P4308XXM (Fixed fans, fixed or redundant PSUs)

Table 146. Intel® Server Chassis P4208XXM/P4308XXM (Fixed fans, fixed or redundant PSUs)

PS Module Number	PMBus	Product Name (in product area of the FRU)	PSU Redundant	Cold Redundant	Fans in each PS
550W Fixed Power Supply	Not support	No FRU	Not support	Not Support	NA

- Intel® Server Chassis P4208XXM (Fixed fans, redundant PSUs)

Table 147. Intel® Server Chassis P4208XXM (Fixed fans, redundant PSUs)

PS Module Number	PMBus	Product Name (in product area of the FRU)	PSU Redundant	Cold Redundant	Fans in each PS
460W HS Power Supply	Support	DPS-460KB A	Support	Support	1 PS fan
750W HS Power Supply	Support	DPS-750XB A	Support	Support	1 PS fan

- Intel® Server Chassis P4308XXM (Fixed fans, redundant PSUs)

Table 148. Intel® Server Chassis P4308XXM (Fixed fans, redundant PSUs)

PS Module Number	PMBus	Product Name (in product area of the FRU)	PSU Redundant	Cold Redundant	Fans in each PS
750W HS Power Supply	Support	DPS-750XB A	Not support	Not support	1 PS fan

- Intel® Server Chassis P4208XXM/P4308XXM (Redundant fans, redundant PSUs)

Table 149. Intel® Server Chassis P4208XXM/P4308XXM (Redundant fans, redundant PSUs)

PS Module Number	PMBus	Product Name (in product area of the FRU)	PSU Redundant	Cold Redundant	Fans in each PS
750W HS Power Supply	Support	DPS-750XB A	Support	Support	1 PS fan
1200W HS Power Supply	Support	DPS-1200TB A	Support	Support	2PS fan

- Intel® Server Chassis P4216XXM (Redundant fans, redundant PSUs)

Table 150. Intel® Server Chassis P4216XXM (Redundant fans, redundant PSUs)

PS Module Number	PMBus	Product Name (in product area of the FRU)	PSU Redundant	Cold Redundant	Fans in each PS
1200W HS Power Supply	Support	DPS-1200TB A	Support	Support	2 PS fan

Redundant Fans only for Intel® Server Chassis

- Intel® Server Chassis P4208XXM (Redundant fans, redundant PSUs)
- Intel® Server Chassis P4308XXM (Redundant fans, redundant PSUs)
- Intel® Server Chassis P4216XXM (Redundant fans, redundant PSUs)

Fan Fault LED support

Fan fault LEDs are available on the hot-swap redundant fans available on the on below chassis:

- Intel® Server Chassis P4208XXM (Redundant fans, redundant PSUs)
- Intel® Server Chassis P4308XXM (Redundant fans, redundant PSUs)
- Intel® Server Chassis P4216XXM (Redundant fans, redundant PSUs)

Memory Throttling support

- Baseboard supports this feature.

Appendix E: POST Code Diagnostic LED Decoder

During the system boot process, the BIOS executes a number of platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the POST code to the POST Code Diagnostic LEDs on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, the Diagnostic LEDs can be used to identify the last POST process that was executed.

Each POST code is represented by a sequence of eight amber diagnostic LEDs. The POST codes are divided into two groups of LEDs as shown in below figure.

The diagnostic LED #7 is labeled as "MSB", and the diagnostic LED #0 is labeled as "LSB".

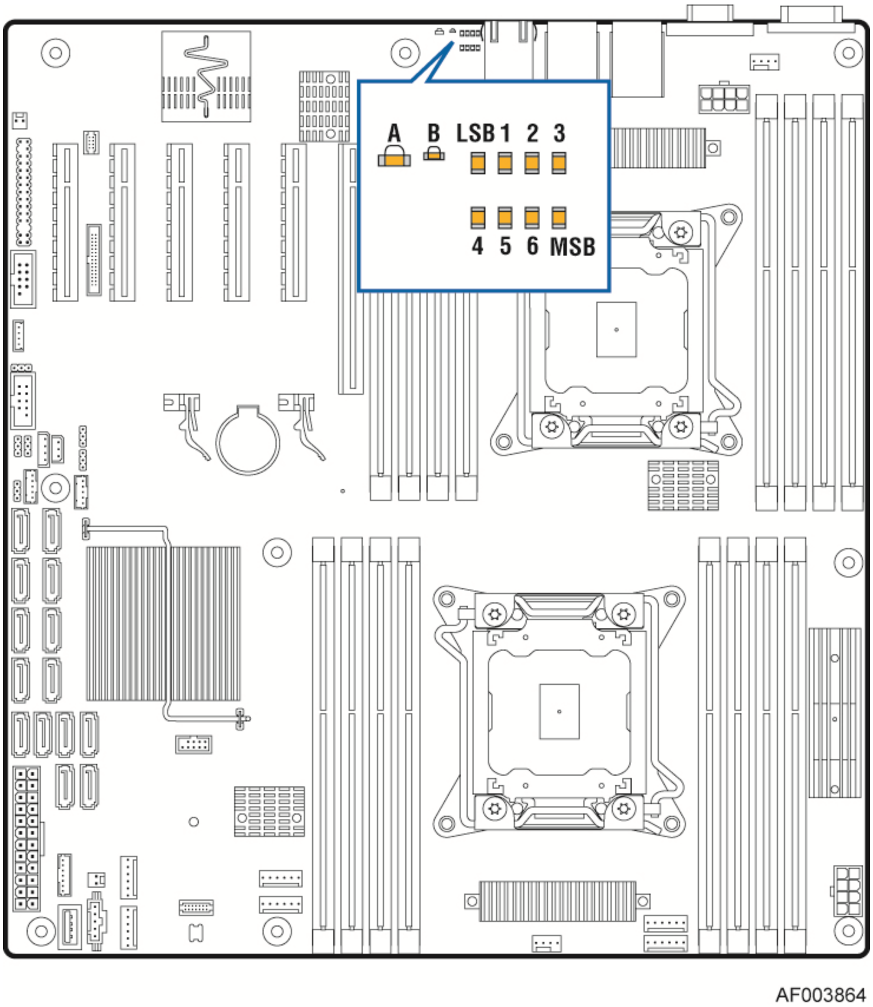


Figure 68. POST Code Diagnostic LED Decoder

A – System Status LED
B – System ID LED
LSB 1 2 3 4 5 6 MSB – Diagnostic LED

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

Table 151. POST Progress Code LED Example

LEDs	Upper Nibble AMBER LEDs				Lower Nibble GREEN LEDs			
	MSB							LSB
	LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
	8h	4h	2h	1h	8h	4h	2h	1h
Status	ON	OFF	ON	OFF	ON	ON	OFF	OFF
Results	1	0	1	0	1	1	0	0
	Ah				Ch			

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh

The following table provides a list of all POST progress codes.

Table 152. POST Progress Codes

Checkpoint	Diagnostic LED Decoder 1 = LED On, 0 = LED Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED #	#7	#6	#5	#4	#3	#2	#1	#0	
SEC Phase									
01h	0	0	0	0	0	0	0	1	First POST code after CPU reset
02h	0	0	0	0	0	0	1	0	Microcode load begin
03h	0	0	0	0	0	0	1	1	CRAM initialization begin
04h	0	0	0	0	0	1	0	0	Pei Cache When Disabled
05h	0	0	0	0	0	1	0	1	SEC Core At Power On Begin.
06h	0	0	0	0	0	1	1	0	Early CPU initialization during Sec Phase.
07h	0	0	0	0	0	1	1	1	Early SB initialization during Sec Phase.
08h	0	0	0	0	1	0	0	0	Early NB initialization during Sec Phase.
09h	0	0	0	0	1	0	0	1	End Of Sec Phase.
0Eh	0	0	0	0	1	1	1	0	Microcode Not Found.
0Fh	0	0	0	0	1	1	1	1	Microcode Not Loaded.
PEI Phase									
10h	0	0	0	1	0	0	0	0	PEI Core
11h	0	0	0	1	0	0	0	1	CPU PEIM
15h	0	0	0	1	0	1	0	1	NB PEIM
19h	0	0	0	1	1	0	0	1	SB PEIM
MRC Process Codes – MRC Progress Code Sequence is executed - See Table 63									
PEI Phase continued…									
31h	0	0	1	1	0	0	0	1	Memory Installed
32h	0	0	1	1	0	0	1	0	CPU PEIM (Cpu Init)
33h	0	0	1	1	0	0	1	1	CPU PEIM (Cache Init)
34h	0	0	1	1	0	1	0	0	CPU PEIM (BSP Select)
35h	0	0	1	1	0	1	0	1	CPU PEIM (AP Init)
36h	0	0	1	1	0	1	1	0	CPU PEIM (CPU SMM Init)
4Fh	0	1	0	0	1	1	1	1	Dxe IPL started
DXE Phase									
60h	0	1	1	0	0	0	0	0	DXE Core started
61h	0	1	1	0	0	0	0	1	DXE NVRAM Init
62h	0	1	1	0	0	0	1	0	SB RUN Init
63h	0	1	1	0	0	0	1	1	Dxe CPU Init

Checkpoint	Diagnostic LED Decoder								Description
	1 = LED On, 0 = LED Off								
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED #	#7	#6	#5	#4	#3	#2	#1	#0	
68h	0	1	1	0	1	0	0	0	DXE PCI Host Bridge Init
69h	0	1	1	0	1	0	0	1	DXE NB Init
6Ah	0	1	1	0	1	0	1	0	DXE NB SMM Init
70h	0	1	1	1	0	0	0	0	DXE SB Init
71h	0	1	1	1	0	0	0	1	DXE SB SMM Init
72h	0	1	1	1	0	0	1	0	DXE SB devices Init
78h	0	1	1	1	1	0	0	0	DXE ACPI Init
79h	0	1	1	1	1	0	0	1	DXE CSM Init
90h	1	0	0	1	0	0	0	0	DXE BDS Started
91h	1	0	0	1	0	0	0	1	DXE BDS connect drivers
92h	1	0	0	1	0	0	1	0	DXE PCI Bus begin
93h	1	0	0	1	0	0	1	1	DXE PCI Bus HPC Init
94h	1	0	0	1	0	1	0	0	DXE PCI Bus enumeration
95h	1	0	0	1	0	1	0	1	DXE PCI Bus resource requested
96h	1	0	0	1	0	1	1	0	DXE PCI Bus assign resource
97h	1	0	0	1	0	1	1	1	DXE CON_OUT connect
98h	1	0	0	1	1	0	0	0	DXE CON_IN connect
99h	1	0	0	1	1	0	0	1	DXE SIO Init
9Ah	1	0	0	1	1	0	1	0	DXE USB start
9Bh	1	0	0	1	1	0	1	1	DXE USB reset
9Ch	1	0	0	1	1	1	0	0	DXE USB detect
9Dh	1	0	0	1	1	1	0	1	DXE USB enable
A1h	1	0	1	0	0	0	0	1	DXE IDE begin
A2h	1	0	1	0	0	0	1	0	DXE IDE reset
A3h	1	0	1	0	0	0	1	1	DXE IDE detect
A4h	1	0	1	0	0	1	0	0	DXE IDE enable
A5h	1	0	1	0	0	1	0	1	DXE SCSI begin
A6h	1	0	1	0	0	1	1	0	DXE SCSI reset
A7h	1	0	1	0	0	1	1	1	DXE SCSI detect
A8h	1	0	1	0	1	0	0	0	DXE SCSI enable
A9h	1	0	1	0	1	0	0	1	DXE verifying SETUP password
ABh	1	0	1	0	1	0	1	1	DXE SETUP start
ACh	1	0	1	0	1	1	0	0	DXE SETUP input wait
ADh	1	0	1	0	1	1	0	1	DXE Ready to Boot
AEh	1	0	1	0	1	1	1	0	DXE Legacy Boot
AFh	1	0	1	0	1	1	1	1	DXE Exit Boot Services
B0h	1	0	1	1	0	0	0	0	RT Set Virtual Address Map Begin
B1h	1	0	1	1	0	0	0	1	RT Set Virtual Address Map End
B2h	1	0	1	1	0	0	1	0	DXE Legacy Option ROM init
B3h	1	0	1	1	0	0	1	1	DXE Reset system
B4h	1	0	1	1	0	1	0	0	DXE USB Hot plug
B5h	1	0	1	1	0	1	0	1	DXE PCI BUS Hot plug
B6h	1	0	1	1	0	1	1	0	DXE NVRAM cleanup
B7h	1	0	1	1	0	1	1	1	DXE Configuration Reset
00h	0	0	0	0	0	0	0	0	INT19
S3 Resume									
E0h	1	1	0	1	0	0	0	0	S3 Resume PEIM (S3 started)
E1h	1	1	0	1	0	0	0	1	S3 Resume PEIM (S3 boot script)
E2h	1	1	0	1	0	0	1	0	S3 Resume PEIM (S3 Video Repost)
E3h	1	1	0	1	0	0	1	1	S3 Resume PEIM (S3 OS wake)
BIOS Recovery									

Checkpoint	Diagnostic LED Decoder								Description
	1 = LED On, 0 = LED Off								
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED #	#7	#6	#5	#4	#3	#2	#1	#0	
F0h	1	1	1	1	0	0	0	0	PEIM which detected forced Recovery condition
F1h	1	1	1	1	0	0	0	1	PEIM which detected User Recovery condition
F2h	1	1	1	1	0	0	1	0	Recovery PEIM (Recovery started)
F3h	1	1	1	1	0	0	1	1	Recovery PEIM (Capsule found)
F4h	1	1	1	1	0	1	0	0	Recovery PEIM (Capsule loaded)

POST Memory Initialization MRC Diagnostic Codes

There are two types of POST Diagnostic Codes displayed by the MRC during memory initialization; Progress Codes and Fatal Error Codes.

The MRC Progress Codes are displays to the Diagnostic LEDs that show the execution point in the MRC operational path at each step.

Table 153. MRC Progress Codes

Checkpoint	Diagnostic LED Decoder								Description
	1 = LED On, 0 = LED Off								
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
MRC Progress Codes									
B0h	1	0	1	1	0	0	0	0	Detect DIMM population
B1h	1	0	1	1	0	0	0	1	Set DDR3 frequency
B2h	1	0	1	1	0	0	1	0	Gather remaining SPD data
B3h	1	0	1	1	0	0	1	1	Program registers on the memory controller level
B4h	1	0	1	1	0	1	0	0	Evaluate RAS modes and save rank information
B5h	1	0	1	1	0	1	0	1	Program registers on the channel level
B6h	1	0	1	1	0	1	1	0	Perform the JEDEC defined initialization sequence
B7h	1	0	1	1	0	1	1	1	Train DDR3 ranks
B8h	1	0	1	1	1	0	0	0	Initialize CLTT/OLTT
B9h	1	0	1	1	1	0	0	1	Hardware memory test and init
BAh	1	0	1	1	1	0	1	0	Execute software memory init
BBh	1	0	1	1	1	0	1	1	Program memory map and interleaving
BCh	1	0	1	1	1	1	0	0	Program RAS configuration
BFh	1	0	1	1	1	1	1	1	MRC is done

Memory Initialization at the beginning of POST includes multiple functions, including: discovery, channel training, validation that the DIMM population is acceptable and functional, initialization of the IMC and other hardware settings, and initialization of applicable RAS configurations.

When a major memory initialization error occurs and prevents the system from booting with data integrity, a beep code is generated, the MRC will display a fatal error code on the diagnostic LEDs, and a system halt command is executed. Fatal MRC error halts do NOT change the state of the System Status LED, and they do NOT get logged as SEL events. The following table lists all MRC fatal errors that are displayed to the Diagnostic LEDs.

Table 154. MRC Fatal Error Codes

Checkpoint	Diagnostic LED Decoder 1 = LED On, 0 = LED Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
MRC Fatal Error Codes									
E8h	1	1	1	0	1	0	0	0	No usable memory error
E9h	1	1	1	0	1	0	0	1	Memory is locked by Intel Trusted Execuiton Technology and is inaccessible
EAh	1	1	1	0	1	0	1	0	DDR3 channel training error
EBh	1	1	1	0	1	0	1	1	Memory test failure
EDh	1	1	1	0	1	1	0	1	DIMM configuration population error
EFh	1	1	1	0	1	1	1	1	Indicates a CLTT table structure error

Appendix F: POST Error Code

Most error conditions encountered during POST are reported using POST Error Codes. These codes represent specific failures, warnings, or informational messages that are identified with particular hardware units. These POST Error Codes may be displayed in the Error Manager display screen, and are always automatically logged to the System Event Log (SEL). Being logged to SEL means that the error information is available to System Management applications, including Remote and Out of Band (OOB) management. The table below lists the supported POST Error Codes, with a descriptive Error Message text. for each. There is also a Response listed, which classifies the error as Minor, Major, or Fatal depending on how serious the error is and what action the system should take. The Response section in the following table indicates one of these actions:

- **Minor:** The message is displayed on the screen or on the Error Manager screen, and an error is logged to the SEL. The system continues booting in a degraded state. The user may want to replace the erroneous unit. The POST Error Pause option setting in the BIOS setup does not have any effect on this error.
- **Major:** The message is displayed on the Error Manager screen, and an error is logged to the SEL. The POST Error Pause option setting in the BIOS setup determines whether the system pauses to the Error Manager for this type of error so the user can take immediate corrective action or the system continues booting.
- **Fatal:** The system halts during post at a blank screen with the text **"Unrecoverable fatal error found. System will not boot until the error is resolved"** and **"Press <F2> to enter setup"** The POST Error Pause option setting in the BIOS setup does not have any effect with this class of error.

Table 155. POST Error Codes and Messages

Error Code	Error Message	Response
0012	System RTC date/time not set	Major
0048	Password check failed	Major
0140	PCI component encountered a PERR error	Major
0141	PCI resource conflict	Major
0146	PCI out of resources error	Major
0191	Processor core/thread count mismatch detected	Fatal
0192	Processor cache size mismatch detected	Fatal
0194	Processor family mismatch detected	Fatal
0195	Processor Intel(R) QPI link frequencies unable to synchronize	Fatal
0196	Processor model mismatch detected	Fatal
0197	Processor frequencies unable to synchronize	Fatal
5220	BIOS Settings reset to default settings	Major
5221	Passwords cleared by jumper	Major
5224	Password clear jumper is Set	Major
8130	Processor 01 disabled	Major
8131	Processor 02 disabled	Major
8132	Processor 03 disabled	Major
8133	Processor 04 disabled	Major
8160	Processor 01 unable to apply microcode update	Major

Error Code	Error Message	Response
8161	Processor 02 unable to apply microcode update	Major
8162	Processor 03 unable to apply microcode update	Major
8163	Processor 04 unable to apply microcode update	Major
8170	Processor 01 failed Self Test (BIST)	Major
8171	Processor 02 failed Self Test (BIST)	Major
8172	Processor 03 failed Self Test (BIST)	Major
8173	Processor 04 failed Self Test (BIST)	Major
8180	Processor 01 microcode update not found	Minor
8181	Processor 02 microcode update not found	Minor
8182	Processor 03 microcode update not found	Minor
8183	Processor 04 microcode update not found	Minor
8190	Watchdog timer failed on last boot	Major
8198	OS boot watchdog timer failure	Major
8300	Baseboard management controller failed self-test	Major
8305	Hot Swap Controller failure	Major
83A0	Management Engine (ME) failed Selftest	Major
83A1	Management Engine (ME) Failed to respond.	Major
84F2	Baseboard management controller failed to respond	Major
84F3	Baseboard management controller in update mode	Major
84F4	Sensor data record empty	Major
84FF	System event log full	Minor
8500	Memory component could not be configured in the selected RAS mode	Major
8501	DIMM Population Error	Major
8520	DIMM_A1 failed test/initialization	Major
8521	DIMM_A2 failed test/initialization	Major
8522	DIMM_A3 failed test/initialization	Major
8523	DIMM_B1 failed test/initialization	Major
8524	DIMM_B2 failed test/initialization	Major
8525	DIMM_B3 failed test/initialization	Major
8526	DIMM_C1 failed test/initialization	Major
8527	DIMM_C2 failed test/initialization	Major
8528	DIMM_C3 failed test/initialization	Major
8529	DIMM_D1 failed test/initialization	Major
852A	DIMM_D2 failed test/initialization	Major
852B	DIMM_D3 failed test/initialization	Major
852C	DIMM_E1 failed test/initialization	Major
852D	DIMM_E2 failed test/initialization	Major
852E	DIMM_E3 failed test/initialization	Major
852F	DIMM_F1 failed test/initialization	Major
8530	DIMM_F2 failed test/initialization	Major
8531	DIMM_F3 failed test/initialization	Major
8532	DIMM_G1 failed test/initialization	Major
8533	DIMM_G2 failed test/initialization	Major
8534	DIMM_G3 failed test/initialization	Major
8535	DIMM_H1 failed test/initialization	Major
8536	DIMM_H2 failed test/initialization	Major

Error Code	Error Message	Response
8537	DIMM_H3 failed test/initialization	Major
8538	DIMM_I1 failed test/initialization	Major
8539	DIMM_I2 failed test/initialization	Major
853A	DIMM_I3 failed test/initialization	Major
853B	DIMM_J1 failed test/initialization	Major
853C	DIMM_J2 failed test/initialization	Major
853D	DIMM_J3 failed test/initialization	Major
853E	DIMM_K1 failed test/initialization	Major
853F (Go to 85C0)	DIMM_K2 failed test/initialization	Major
8540	DIMM_A1 disabled	Major
8541	DIMM_A2 disabled	Major
8542	DIMM_A3 disabled	Major
8543	DIMM_B1 disabled	Major
8544	DIMM_B2 disabled	Major
8545	DIMM_B3 disabled	Major
8546	DIMM_C1 disabled	Major
8547	DIMM_C2 disabled	Major
8548	DIMM_C3 disabled	Major
8549	DIMM_D1 disabled	Major
854A	DIMM_D2 disabled	Major
854B	DIMM_D3 disabled	Major
854C	DIMM_E1 disabled	Major
854D	DIMM_E2 disabled	Major
854E	DIMM_E3 disabled	Major
854F	DIMM_F1 disabled	Major
8550	DIMM_F2 disabled	Major
8551	DIMM_F3 disabled	Major
8552	DIMM_G1 disabled	Major
8553	DIMM_G2 disabled	Major
8554	DIMM_G3 disabled	Major
8555	DIMM_H1 disabled	Major
8556	DIMM_H2 disabled	Major
8557	DIMM_H3 disabled	Major
8558	DIMM_I1 disabled	Major
8559	DIMM_I2 disabled	Major
855A	DIMM_I3 disabled	Major
855B	DIMM_J1 disabled	Major
855C	DIMM_J2 disabled	Major
855D	DIMM_J3 disabled	Major
855E	DIMM_K1 disabled	Major
855F (Go to 85D0)	DIMM_K2 disabled	Major
8560	DIMM_A1 encountered a Serial Presence Detection (SPD) failure	Major
8561	DIMM_A2 encountered a Serial Presence Detection (SPD) failure	Major

Error Code	Error Message	Response
8562	DIMM_A3 encountered a Serial Presence Detection (SPD) failure	Major
8563	DIMM_B1 encountered a Serial Presence Detection (SPD) failure	Major
8564	DIMM_B2 encountered a Serial Presence Detection (SPD) failure	Major
8565	DIMM_B3 encountered a Serial Presence Detection (SPD) failure	Major
8566	DIMM_C1 encountered a Serial Presence Detection (SPD) failure	Major
8567	DIMM_C2 encountered a Serial Presence Detection (SPD) failure	Major
8568	DIMM_C3 encountered a Serial Presence Detection (SPD) failure	Major
8569	DIMM_D1 encountered a Serial Presence Detection (SPD) failure	Major
856A	DIMM_D2 encountered a Serial Presence Detection (SPD) failure	Major
856B	DIMM_D3 encountered a Serial Presence Detection (SPD) failure	Major
856C	DIMM_E1 encountered a Serial Presence Detection (SPD) failure	Major
856D	DIMM_E2 encountered a Serial Presence Detection (SPD) failure	Major
856E	DIMM_E3 encountered a Serial Presence Detection (SPD) failure	Major
856F	DIMM_F1 encountered a Serial Presence Detection (SPD) failure	Major
8570	DIMM_F2 encountered a Serial Presence Detection (SPD) failure	Major
8571	DIMM_F3 encountered a Serial Presence Detection (SPD) failure	Major
8572	DIMM_G1 encountered a Serial Presence Detection (SPD) failure	Major
8573	DIMM_G2 encountered a Serial Presence Detection (SPD) failure	Major
8574	DIMM_G3 encountered a Serial Presence Detection (SPD) failure	Major
8575	DIMM_H1 encountered a Serial Presence Detection (SPD) failure	Major
8576	DIMM_H2 encountered a Serial Presence Detection (SPD) failure	Major
8577	DIMM_H3 encountered a Serial Presence Detection (SPD) failure	Major
8578	DIMM_I1 encountered a Serial Presence Detection (SPD) failure	Major
8579	DIMM_I2 encountered a Serial Presence Detection (SPD) failure	Major
857A	DIMM_I3 encountered a Serial Presence Detection (SPD) failure	Major
857B	DIMM_J1 encountered a Serial Presence Detection (SPD) failure	Major
857C	DIMM_J2 encountered a Serial Presence Detection (SPD) failure	Major
857D	DIMM_J3 encountered a Serial Presence Detection (SPD) failure	Major
857E	DIMM_K1 encountered a Serial Presence Detection (SPD) failure	Major
857F (Go to 85E0)	DIMM_K2 encountered a Serial Presence Detection (SPD) failure	Major
85C0	DIMM_K3 failed test/initialization	Major
85C1	DIMM_L1 failed test/initialization	Major
85C2	DIMM_L2 failed test/initialization	Major
85C3	DIMM_L3 failed test/initialization	Major
85C4	DIMM_M1 failed test/initialization	Major
85C5	DIMM_M2 failed test/initialization	Major
85C6	DIMM_M3 failed test/initialization	Major
85C7	DIMM_N1 failed test/initialization	Major
85C8	DIMM_N2 failed test/initialization	Major
85C9	DIMM_N3 failed test/initialization	Major
85CA	DIMM_O1 failed test/initialization	Major
85CB	DIMM_O2 failed test/initialization	Major
85CC	DIMM_O3 failed test/initialization	Major
85CD	DIMM_P1 failed test/initialization	Major

Error Code	Error Message	Response
85CE	DIMM_P2 failed test/initialization	Major
85CF	DIMM_P3 failed test/initialization	Major
85D0	DIMM_K3 disabled	Major
85D1	DIMM_L1 disabled	Major
85D2	DIMM_L2 disabled	Major
85D3	DIMM_L3 disabled	Major
85D4	DIMM_M1 disabled	Major
85D5	DIMM_M2 disabled	Major
85D6	DIMM_M3 disabled	Major
85D7	DIMM_N1 disabled	Major
85D8	DIMM_N2 disabled	Major
85D9	DIMM_N3 disabled	Major
85DA	DIMM_O1 disabled	Major
85DB	DIMM_O2 disabled	Major
85DC	DIMM_O3 disabled	Major
85DD	DIMM_P1 disabled	Major
85DE	DIMM_P2 disabled	Major
85DF	DIMM_P3 disabled	Major
85E0	DIMM_K3 encountered a Serial Presence Detection (SPD) failure	Major
85E1	DIMM_L1 encountered a Serial Presence Detection (SPD) failure	Major
85E2	DIMM_L2 encountered a Serial Presence Detection (SPD) failure	Major
85E3	DIMM_L3 encountered a Serial Presence Detection (SPD) failure	Major
85E4	DIMM_M1 encountered a Serial Presence Detection (SPD) failure	Major
85E5	DIMM_M2 encountered a Serial Presence Detection (SPD) failure	Major
85E6	DIMM_M3 encountered a Serial Presence Detection (SPD) failure	Major
85E7	DIMM_N1 encountered a Serial Presence Detection (SPD) failure	Major
85E8	DIMM_N2 encountered a Serial Presence Detection (SPD) failure	Major
85E9	DIMM_N3 encountered a Serial Presence Detection (SPD) failure	Major
85EA	DIMM_O1 encountered a Serial Presence Detection (SPD) failure	Major
85EB	DIMM_O2 encountered a Serial Presence Detection (SPD) failure	Major
85EC	DIMM_O3 encountered a Serial Presence Detection (SPD) failure	Major
85ED	DIMM_P1 encountered a Serial Presence Detection (SPD) failure	Major
85EE	DIMM_P2 encountered a Serial Presence Detection (SPD) failure	Major
85EF	DIMM_P3 encountered a Serial Presence Detection (SPD) failure	Major
8604	POST Reclaim of non-critical NVRAM variables	Minor
8605	BIOS Settings are corrupted	Major
92A3	Serial port component was not detected	Major
92A9	Serial port component encountered a resource conflict error	Major
A000	TPM device not detected.	Minor
A001	TPM device missing or not responding.	Minor
A002	TPM device failure.	Minor
A003	TPM device failed self-test.	Minor
A100	BIOS ACM Error	Major
A421	PCI component encountered a SERR error	Fatal
A5A0	PCI Express component encountered a PERR error	Minor
A5A1	PCI Express component encountered an SERR error	Fatal

The following table lists the POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user-visible code on the POST Progress LEDs

Table 156. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
3	Memory error	See Table 64	System halted because a fatal error related to the memory was detected.
1 long	Intel® TXT security violation	0xAE, 0xAF	System halted because Intel® Trusted Execution Technology detected a potential violation of system security.

POST Error Beep Code

The Integrated BMC may generate beep codes upon detection of failure conditions. Beep codes are sounded each time the problem is discovered, such as on each power-up attempt, but are not sounded continuously. Codes that are common across all Intel server boards and systems that use same generation chipset are listed in the following table. Each digit in the code is represented by a sequence of beeps whose count is equal to the digit.

Table 157. Integrated BMC Beep Codes

Code	Reason for Beep	Associated Sensors
1-5-2-1	No CPUs installed or first CPU socket is empty.	CPU Missing Sensor
1-5-2-4	MSID Mismatch.	MSID Mismatch Sensor.
1-5-4-2	Power fault: DC power is unexpectedly lost (power good dropout).	Power unit – power unit failure offset.
1-5-4-4	Power control fault (power good assertion timeout).	Power unit – soft power control failure offset.
1-5-1-2	VR Watchdog Timer sensor assertion	VR Watchdog Timer
1-5-1-4	The system does not power on or unexpectedly powers off and a power supply unit (PSU) is present that is an incompatible model with one or more other PSUs in the system	PS Status

Glossary

This appendix contains important terms used in the preceding chapters. For ease of use, numeric entries are listed first (for example, 82460GX) with alpha entries following (for example, AGP 4x). Acronyms are then entered in their respective place, with non-acronyms following.

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ASIC	Application Specific Integrated Circuit
BIOS	Basic Input/Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
byte	8-bit quantity.
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMP	Emergency Management Port
EPS	External Product Specification
FMB	Flexible Mother Board
FMC	Flex Management Connector
FMM	Flex Management Module
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GB	1024MB
GPIO	General Purpose I/O
GTL	Gunning Transceiver Logic
HSC	Hot-Swap Controller
Hz	Hertz (1 cycle/second)
I2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture
IBF	Input Buffer
ICH	I/O Controller Hub
ICMB	Intelligent Chassis Management Bus
IERR	Internal Error
IFB	I/O and Firmware Bridge

Term	Definition
INTR	Interrupt
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
ITP	In-Target Probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB	1024KB
mBMC	National Semiconductor© PC87431x mini BMC
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
ms	milliseconds
MTTR	Memory Tpe Range Register
Mux	Multiplexor
NIC	Network Interface Controller
NMI	Nonmaskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm	Unit of electrical resistance
PEF	Platform Event Filtering
PEP	Platform Event Paging
PIA	Platform Information Area (This feature configures the firmware for the platform hardware)
PLD	Programmable Logic Device
PMI	Platform Management Interrupt
POST	Power-On Self Test
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board)
SDR	Sensor Data Record
SECC	Single Edge Connector Cartridge
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory
SEL	System Event Log
SIO	Server Input/Output

Term	Definition
SMI	Server Management Interrupt (SMI is the highest priority nonmaskable interrupt)
SMM	Server Management Mode
SMS	Server Management Software
SNMP	Simple Network Management Protocol
TBD	To Be Determined
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
UTC	Universal time coordinare
VID	Voltage Identification
VRD	Voltage Regulator Down
Word	16-bit quantity
ZIF	Zero Insertion Force

Reference Documents

See the following document for additional information:

- *BIOS for EPSD Platforms Based on Intel® Xeon Processor E5-4600/2600/2400/1600 Product Families External Product Specification*
- *EPSD Platforms Based On Intel Xeon® Processor E5 4600/2600/2400/1600 Product Families BMC Core Firmware External Product Specification*
- *Intel® Remote Management Module 4 Technical Product Specification*
- *Intelligent Platform Management Interface Specification*