Intel® Server System P4000SC Family

Technical Product Specification

Intel reference number G63273-001

Revision 1.1

July, 2012

Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
May 2012	1.0	Initial release.
July 2012	1.1	Updated section 1.1 and Table 1.

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1. Intel® Server System P4000SC Overview

Intel® Server System P4000SC is 4U pedestal length server chassis that is designed to support Intel® Server Board S2400SC. This chapter provides a high-level overview of the chassis features. Greater detail for each major chassis component or feature is provided in the following chapters.

1.1 Integrated System family overview

Intel® Server System P4000SC makes extensive use of tool-less hardware features and, depending on configuration and upgrade features, provides redundant power supply, redundant cooling and hot swappable hard drives capability. Intel® Server System P4000SC comes with the following configuration:

Your Intel® Server System P4304SC2SFEN ships with the following items:

- One Intel® Server Board S2400SC
- One fixed 550W power supply, installed in the chassis
- One fixed system CPU zone fan, installed in the chassis
- One fixed system PCI zone fan, installed in the chassis
- Four fixed HDD carrier tray, installed in the chassis
- Front panel, installed in the chassis
- Front Bezel for fixed hard drive, EMI shield, 5.25'' bay filler
- Pre-routing cables
- Two heat sinks
- One air duct

Your Intel® Server System P4304SC2SHDR ships with the following items:

- One Intel® Server Board S2400SC
- Two CRPS 460W power supply, installed in the chassis
- One fixed system CPU zone fan, installed in the chassis
- One fixed system PCI zone fan, installed in the chassis
- 4x3.5 hot swap HDD cage with four 3.5” HDD carrier, installed in the chassis
- One Intel® Remote Management Module 4 Lite, installed on the server board.
- Front panel, installed in the chassis
- Front Bezel for hot-swap hard drive, EMI shield, 5.25'' bay filler
- Pre-routing cables
- Two heat sinks
- One air duct

Your Intel® Server System P4308SC2MHGC ships with the following items:

- One Intel® Server Board S2400SC
- Two CRPS 750W power supply, installed in the chassis
- Five hot-swap redundant system fans, installed in the chassis
- 8x3.5'' hot-swap HDD cage with eight 3.5” HDD carrier, installed in the chassis
- One Intel® Remote Management Module 4, installed on the server board.
- Front panel, installed in the chassis
- Front Bezel for hot-swap hard drive, EMI shield, 5.25'' bay filler
- Pre-routing cables
- Two heat sinks

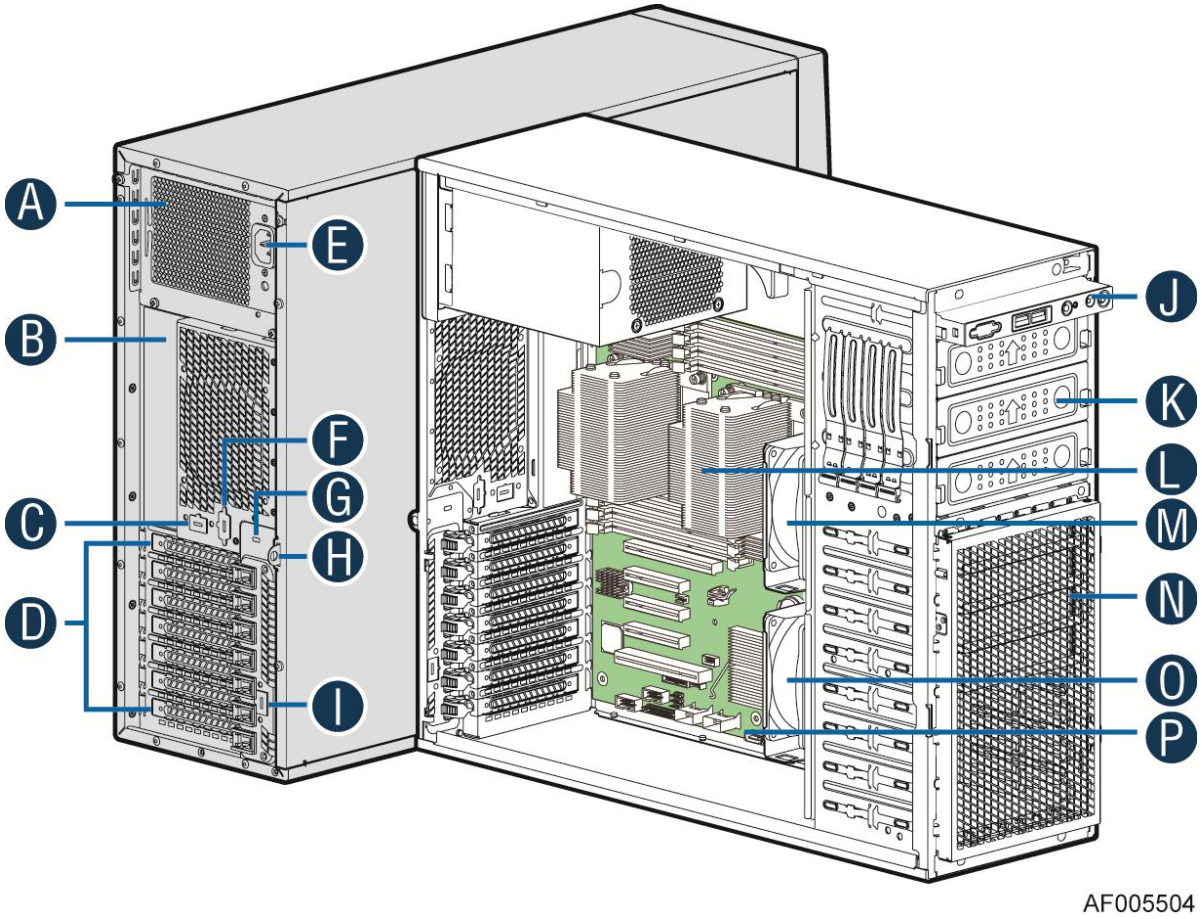
- One air duct

The following table summarizes the features for all system combinations:

Table 1. Intel® Server System P4000SC configuration base feature

Configuration	P4304SC2SFEN	P4304SC2SHDR	P4308SC2MHGC
Intel® Server Board Support	Intel® Server Board S2400SC		
Power	550W non-redundant fixed power supply	Two 460W redundant hot-swap power supplies	Two 750W redundant hot-swap power supplies
System Cooling	Two 92x32mm non-redundant fans and one air duct		Five 80x38mm redundant hot swap fans and one air duct
Peripherals Bays	Three (3) half height 5-1/4" bays for optical devices.		
Drive Bays	Includes one fixed drive bay. Supports up to four 3.5” fixed hard drives.	Includes one 4x3.5” hot-swap hard drive cage. Supports up to four 3.5” fixed hard drives.	Includes one 8x3.5” hot-swap hard drive cage. Supports up to eight 3.5” hot-swap hard drives.
Expansion Slots	Support up to six (6) full height, full length PCI form factor cards mechanically.		
Front Panel	Power Button with LED, Reset Button, NMI Button, ID Button with LED, Four NIC LEDs, Hard drive activity LED, System status LED, two USB ports, Optional front serial port/VGA port		
Appearance	Color: Cosmetic black (GE 701 or equivalent), service Intel blue, hot swap Intel green. Support for Intel standard front panel or LCD		
Dimensions Pedestal	17.24 in (438 mm) x 6.81 in (173mm) x 22.05 in (560 mm) (Height X Width X Depth)		17.24 in (438 mm) x 6.81 in (173mm) x 25 in (612 mm) (Height X Width X Depth)
Optional Accessory Kits	Zephyr flash storage, RMM4-lite modules, TPM module, dedicated NIC module, Expander Card module,		

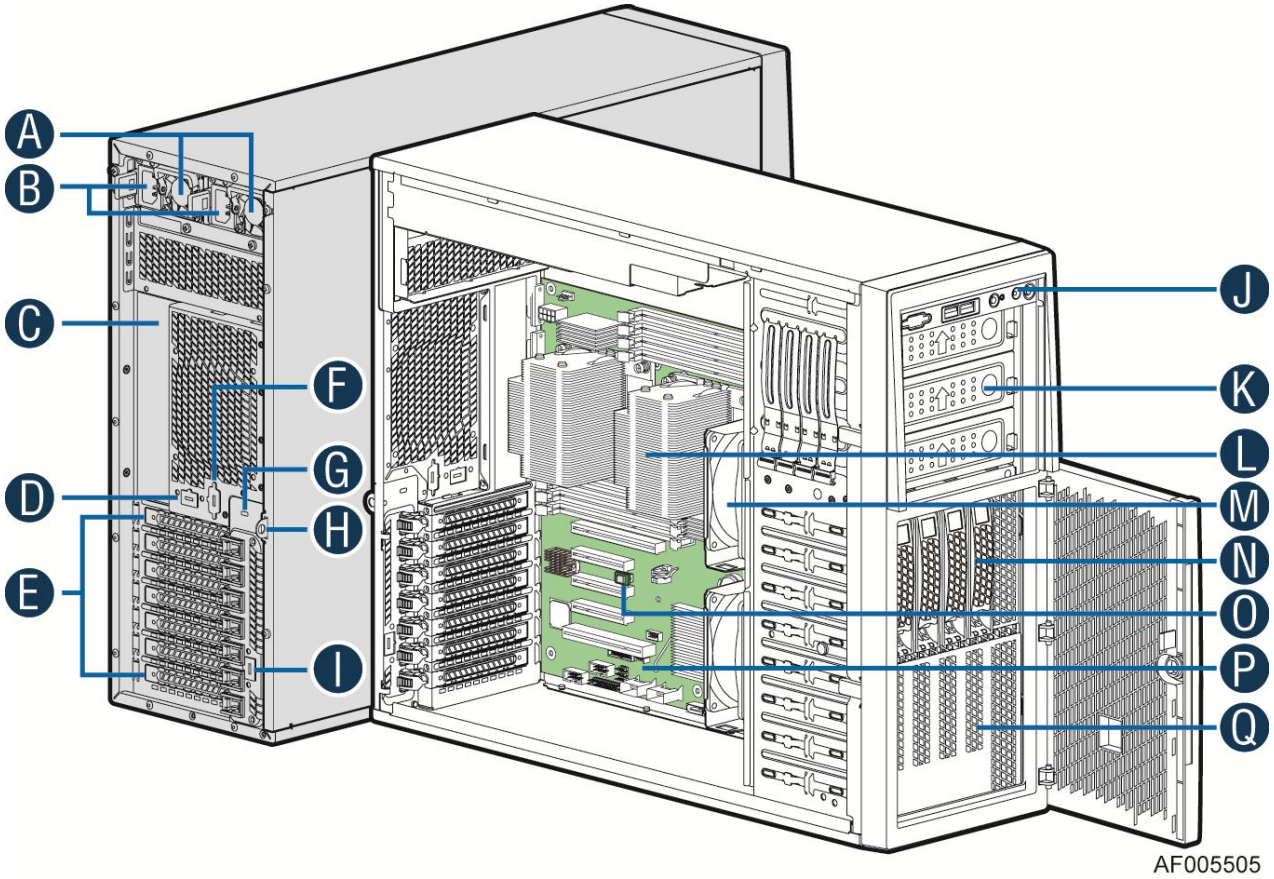
1.1.1 Intel® Server System P4304SC2SFEN View



A. 550-W Fixed Power Supply
B. I/O Ports
C. Alternate RMM4 Knockout
D. PCI Add-in Board Slot Covers
E. AC Input Power Connector
F. Serial Port Knockout
G. A Kensington* Cable Lock Mounting Hole
H. Padlock Loop
I. RMM4 Knockout
J. Front Control Panel
K. 5.25” Peripheral Bays
L. Heatsink
M. Fixed CPU Zone System Fan
N. EMI Filler
O. Fixed PCI Zone System Fan
P. Intel® Server Board S2400SC

Figure 1. Internal Chassis View of Intel® Server System P4304SC2SFEN

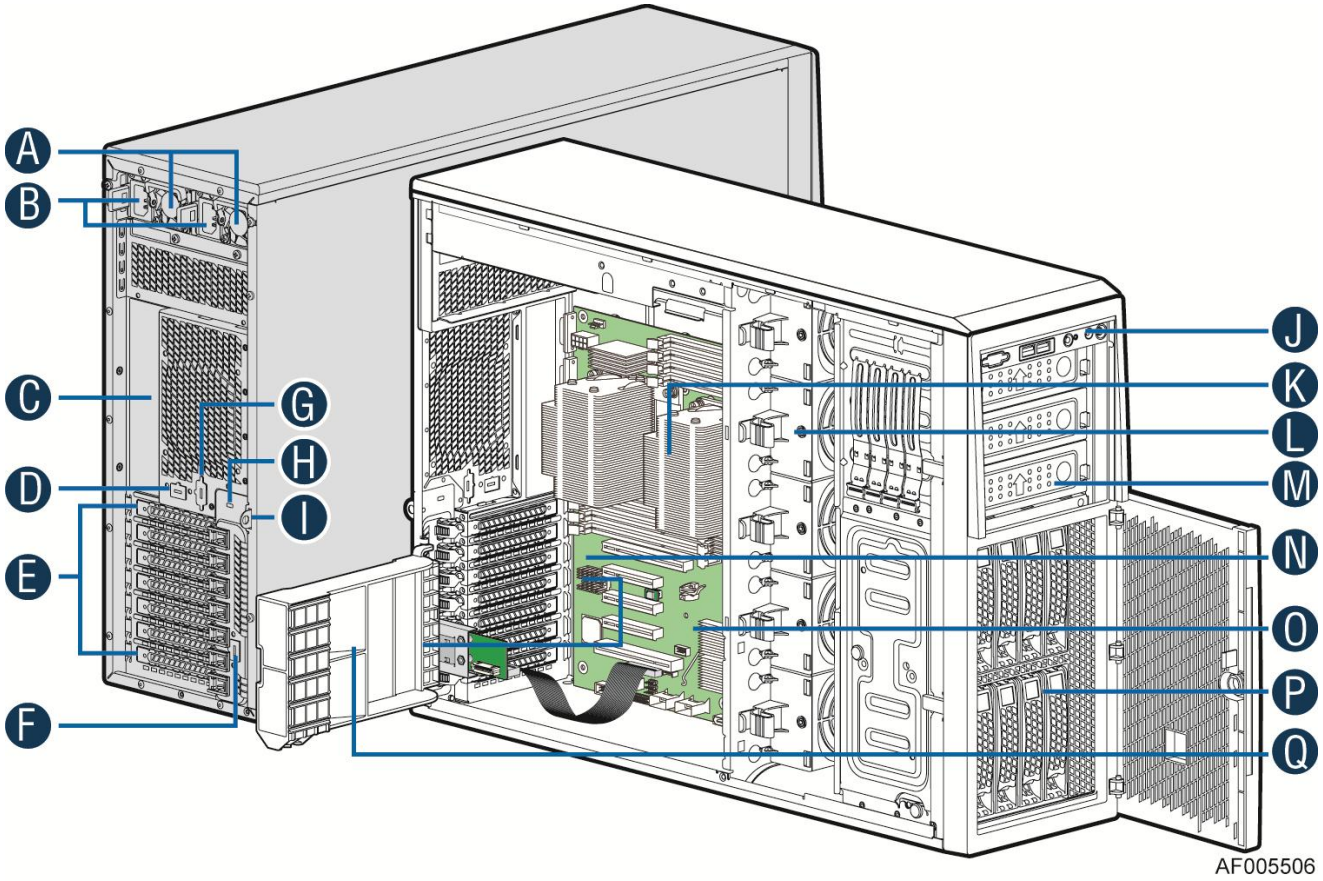
1.1.2 Intel® Server System P4304SHDR View



A. 460-W Hot Swap Power Supply (Two)
B. AC Input Power Connector
C. I/O Ports
D. Alternate RMM4 Knockout
E. PCI Add-in Board Slot Covers
F. Alternate Serial Port Knockout
G. A Kensington* Cable Lock Mounting Hole
H. Padlock Loop
I. RMM4 Knockout
J. Front Control Panel
K. 5.25" Peripheral Bays
L. Heat-sink
M. Fixed System Fan
N. 4x3.5” Hot-swap HDD Cage
O. Intel® Remote Management Module 4 Lite
P. Intel® Server Board S2400SC
Q. EMI Cover

Figure 2. Internal Chassis View of Intel® Server System P4304SC2SHDR

1.1.3 Intel® Server System P4308SC2MHGC View



A. 750-W Redundant Power Supply (Two)
B. AC Input Power Connector
C. I/O Ports
D. Alternate RMM4 Knockout
E. PCI Add-in Board Slot Covers
F. RMM4 Knockout
G. Alternate Serial Port Knockout
H. A Kensington* Cable Lock Mounting Hole
I. Padlock Loop
J. Front Control Panel
K. Heat-sink
L. Hot-swap system fan
M. 5.25” Peripheral Bays
N. Intel® Server Board S2400SC
O. Intel® Remote Management Module 4
P. 8x3.5” Hot-swap HDD Cage
Q. PCI-e Retainer

Figure 3. Internal Chassis View of Intel® Server System P4308SC2MHGC

1.2 Chassis dimensions

Length:
656 mm (without bezel)
698.3 mm (with bezel)

Height:
438 mm

Width:
173 mm

1.3 Front control panel feature Overview

This Front Control Panel conforms to *SSI Specification* with one exception that up to 4 LAN act/link LEDs are supported. The common front panel can support either the standard SSI 2x12 cable interconnect (2 LAN ports) or an Intel customized 2x15 cable interconnect (4 LAN ports).

The Front Control Panel has the following features:

- Power button with integrated power LED (green)
- System ID with integrated ID LED (blue)
- System Status LED (green/amber)
- System Reset button
- HDD activity LED
- 4 NIC activity/link LEDs
- NMI button
- Two USB ports

1.3.1 Front Control Panel LED/Button Functionality

The following figure shows the layout of Front Control Panel:

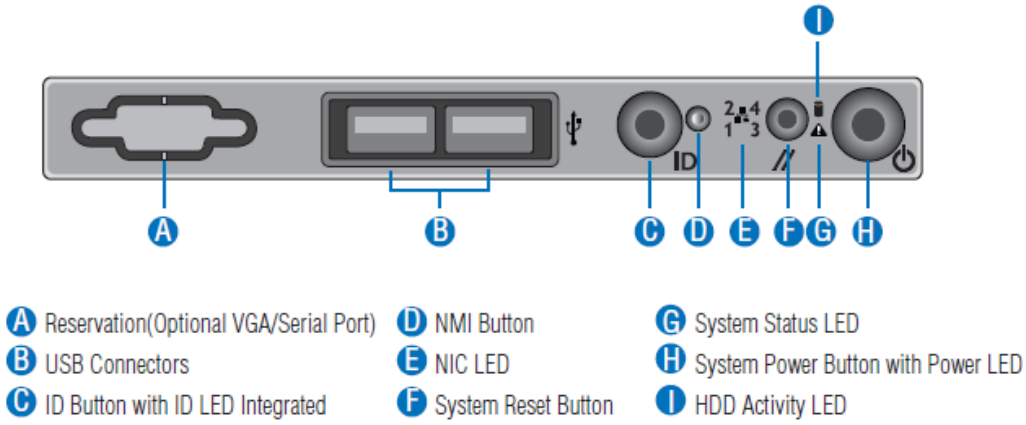


Figure 4. Front Control Panel LED/Button Arragement

ID Button with integrated ID LED – Toggles the integrated ID LED and the Blue server board ID LED on and off. The ID LED is used to identify the system for maintenance when installed in a rack of similar server systems. The ID LED can also be toggled on and off remotely using the IPMI "Chassis Identify" command which will cause the LED to blink for 15 seconds.

NMI Button – When the NMI button is pressed, it puts the server in a halt state and issues a non-maskable interrupt (NMI). This can be useful when performing diagnostics for a given issue where a memory download is necessary to help determine the cause of the problem. To prevent an inadvertent system halt, the actual NMI button is located behind the Front Control Panel faceplate where it is only accessible with the use of a small tipped tool like a pin or paper clip.

Network Activity LEDs (NIC LED) – The Front Control Panel includes an activity LED indicator for each on-board Network Interface Controller (NIC). When a network link is detected, the LED will turn on solid. The LED will blink once network activity occurs at a rate that is consistent with the amount of network activity that is occurring.

System Reset Button – When pressed, this button will reboot and re-initialize the system.

System Status LED – The System Status LED is a bi-color (Green/Amber) indicator that shows the current health of the server system. The system provides two locations for this feature; one is located on the Front Control Panel, the other is located on the back edge of the server board, viewable from the back of the system. Both LEDs are tied together and will show the same state. The System Status LED states are driven by the on-board platform management sub-system.

System Power Button with power LED – Toggles the system power on and off. This button also functions as a sleep button if enabled by an ACPI compliant operating system. Pressing this button will send a signal to the Integrated BMC, which will either power on or power off the system. The integrated LED is a single color (Green) and is capable of supporting different indicator states as defined in the following table:

Table 2. Power/Sleep LED Functional States

State	Power Mode	LED	Description
Power-off	Non-ACPI	Off	System power is off, and the BIOS has not initialized the chipset.
Power-on	Non-ACPI	On	System power is on
S5	ACPI	Off	Mechanical is off, and the operating system has not saved any context to the hard disk.
S4	ACPI	Off	Mechanical is off. The operating system has saved context to the hard disk.
S3-S1	ACPI	Slow blink[1]	DC power is still on. The operating system has saved context and gone into a level of low-power state.
S0	ACPI	Steady on	System and the operating system are up and running.

HDD Activity LED - The drive activity LED on the front panel indicates drive activity from the on-board hard disk controllers. The server board also provides a header giving access to this LED for add-in controllers.

USB Ports – In addition, the front panel provides two USB ports. The USB ports are cabled to the 2x5 connector on the server board.

1.3.2 Front Control Panel LED Status

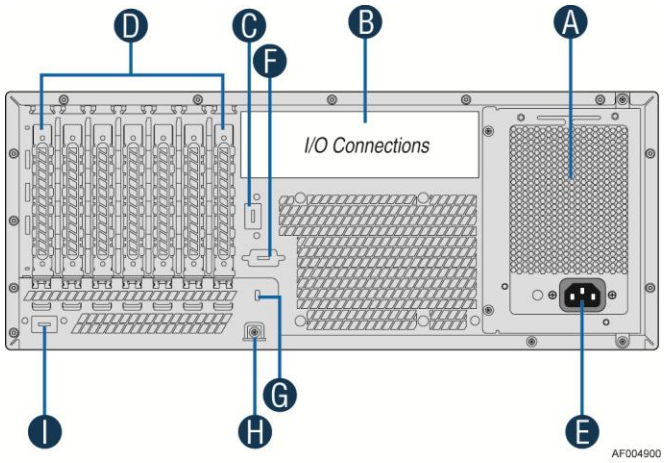
The following table provides a description of each LED status.

Table 3. Front Control Panel LED Status

LED	Color	Condition	What It Means
Power/Sleep	Green	On	Power on or S0 sleep.
	Green	Blink	S1 sleep or S3 standby only for Server baseboards.
		Off	Off (also sleep S4/S5 modes).
Status	Green	On	System ready/No alarm.
	Green	Blink	System ready, but degraded: redundancy lost such as PS or fan failure; non-critical temp/voltage threshold; battery failure; or predictive PS failure.
	Amber	On	Critical alarm: Voltage, thermal, or power fault; CPU missing; insufficient power unit redundancy resource offset asserted.
	Amber	Blink	Non-Critical failure: Critical temp/voltage threshold; VDR hot asserted; min number fans not present or failed.
		Off	AC power off: System unplugged. AC power on: System powered off and in standby, no prior degraded/non-critical/critical state.
Global HDD Activity	Green	Blink	HDD access.
		Off	No access and no fault.
LAN 1-4 Activity/Link	Green	On	LAN link
	Green	Blink	LAN access.
		Off	Idle.
Chassis Identification	Blue	On	Front panel chassis ID button pressed.
	Blue	Blink	Unit selected for identification by software.
		Off	No identification.

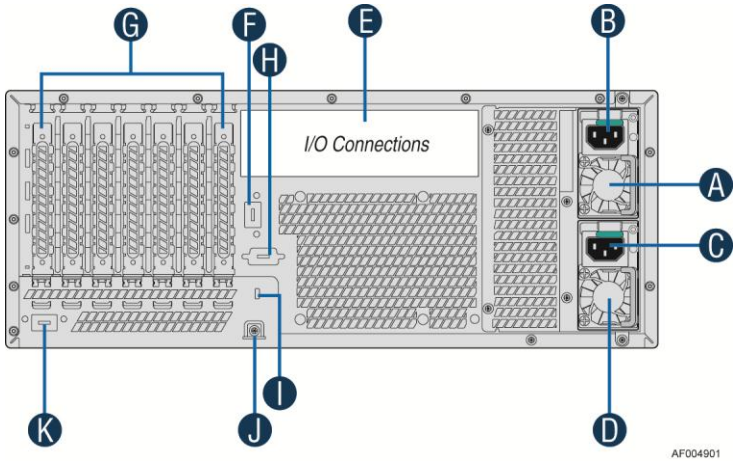
1.4 Back panel feature Overview

The following figure shows the layout of Back Panel with fixed power supply and hot-swap redundant power supplies:



A	Fixed Power Supply	F	Serial-B Port (Optional)
B	IO Connectors	G	Kensington* Cable Lock Mounting Hole
C	RMM4 NIC Port (Optional)	H	Padlock Loop
D	Add in PCI-e cards	I	RMM4 NIC Port (Optional)
E	Power Connector		

Figure 5. Back panel feature (for P4000SC2SFEN)



A	Hot-swap Power Supply	G	Add in PCI-e cards
B	Power Connector	H	Serial-B Port (Optional)
C	Power Connector	I	Kensington* Cable Lock Mounting Hole
D	Hot-swap Power Supply	J	Padlock Loop
E	IO Connectors	K	RMM4 NIC Port (Optional)
F	RMM4 NIC Port (Optional)		

Figure 13. Back panel feature (For P4000SC2SHDR and P4000SC2MHGC)

1.5 Hot swap Hard Drivers and front panel options

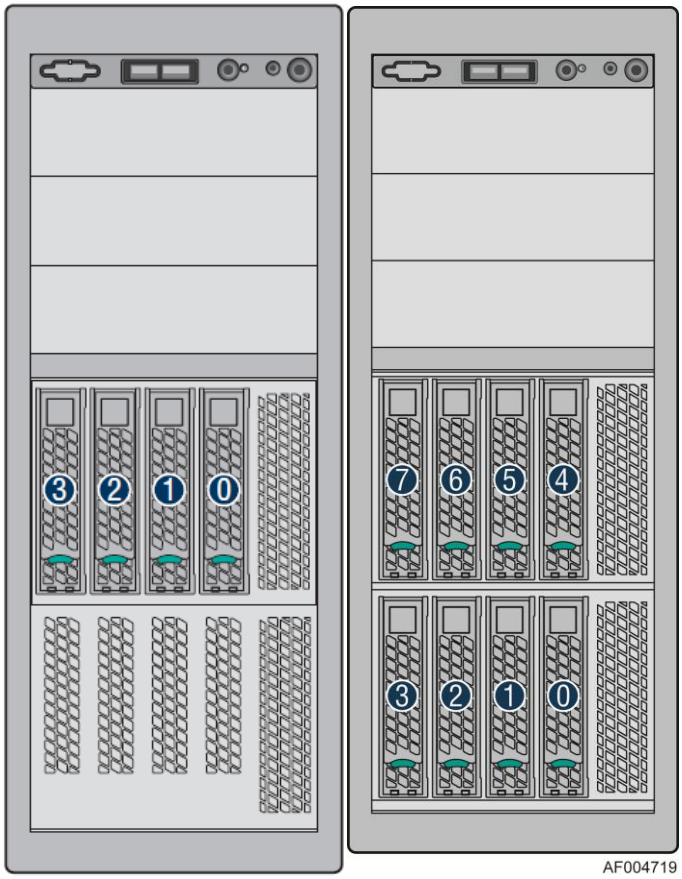


Figure 6. Hot-Swap Hard Disk Drive Cage

1.6 Chassis Security

A variety of chassis security options are provided at the system level:

- A removable padlock loop at the rear of the system access cover can be used to prevent access to the microprocessors, memory, and add-in cards. A variety of lock sizes can be accommodated by the 0.270-inch diameter loop.
- A Kensington* cable lock mounting hole is provided on the rear chassis I/O panel.
- A chassis intrusion switch is provided, allowing server management software to detect unauthorized access to the system side cover.
- In hot-swap hard drives configuration, a door lock is provided on the front bezel assembly with the door to prevent access to the hot-swap hard drives and the interior of the chassis.

Note: See the Technical Product Specificationappropriate to the server board and *System Service Guide* for a description of BIOS and management security features for each specific supported platform. Technical product specifications can be found at http://www.intel.com/support.

1.7 Front Bezel Features

There are two type of front bezel assembly.

1. Front bezel assembly for fixed hard drives configuration on Intel® Server System P4304SC2SFEN.

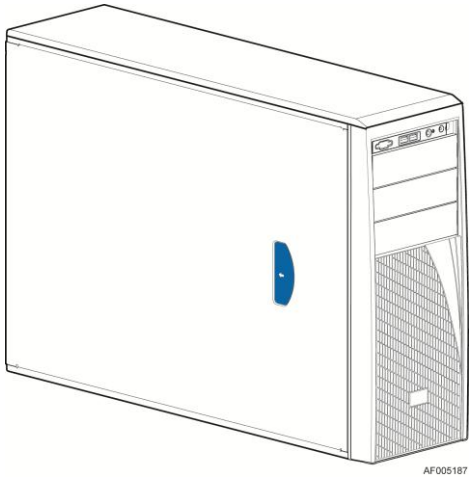
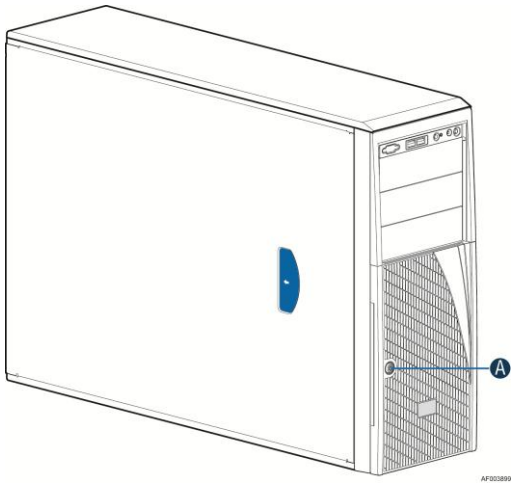


Figure 7. Front Closed Chassis View for Fixed Hard Drives Configuration

2. Front bezel assembly with the door for hot-swap hard drives configuration on Intel® Server System P4304SC2SHDR and P4308SC2MHGC.



A. Security Lock

Figure 8. Front Closed Chassis View for Hot-swap Hard Drives Configuration

Both two pedestal front bezel are constructed of molded plastic and attaches to the front of the chassis with three clips on the right side and two snaps on the left. The snaps at the left attach behind the access cover, thereby preventing accidental removal of the bezel. The bezel can

only be removed by first removing the server access cover. This provides additional security to the hard drive and peripheral bay area.

For the front bezel assembly for fixed hard drives configuration, removing the bezel, there is an EMI shield covering the fixed hard drives bay area.

For the front bezel assembly for hot-swap hard drives configuration, the bezel includes a key-locking door that covers the drive cage area and allows access to hot swap drives when a hot swap drive cage is installed.

The peripheral bays are covered with plastic snap-in cosmetic pieces that must be removed to add peripherals to the system. Front panel buttons and lights are located above the peripheral bays.

2. System Power Sub-system

2.1 550-W Power Supply

This 550W power supply specification defines a non-redundant power supply that supports pedestal entry server systems. The 550W power supply has seven outputs; 3.3V, 5V, 12V1, 12V2, 12V3, -12V, and 5Vsb, with no less than 550W. The power supply has an AC input and be power factor corrected.

2.1.1 Mechanical Overview

The power supply size is 98mm x 150mm x 160mm (H x W x D) and has a wire harness for the DC outputs. The AC plugs directly into the external face of the power supply.

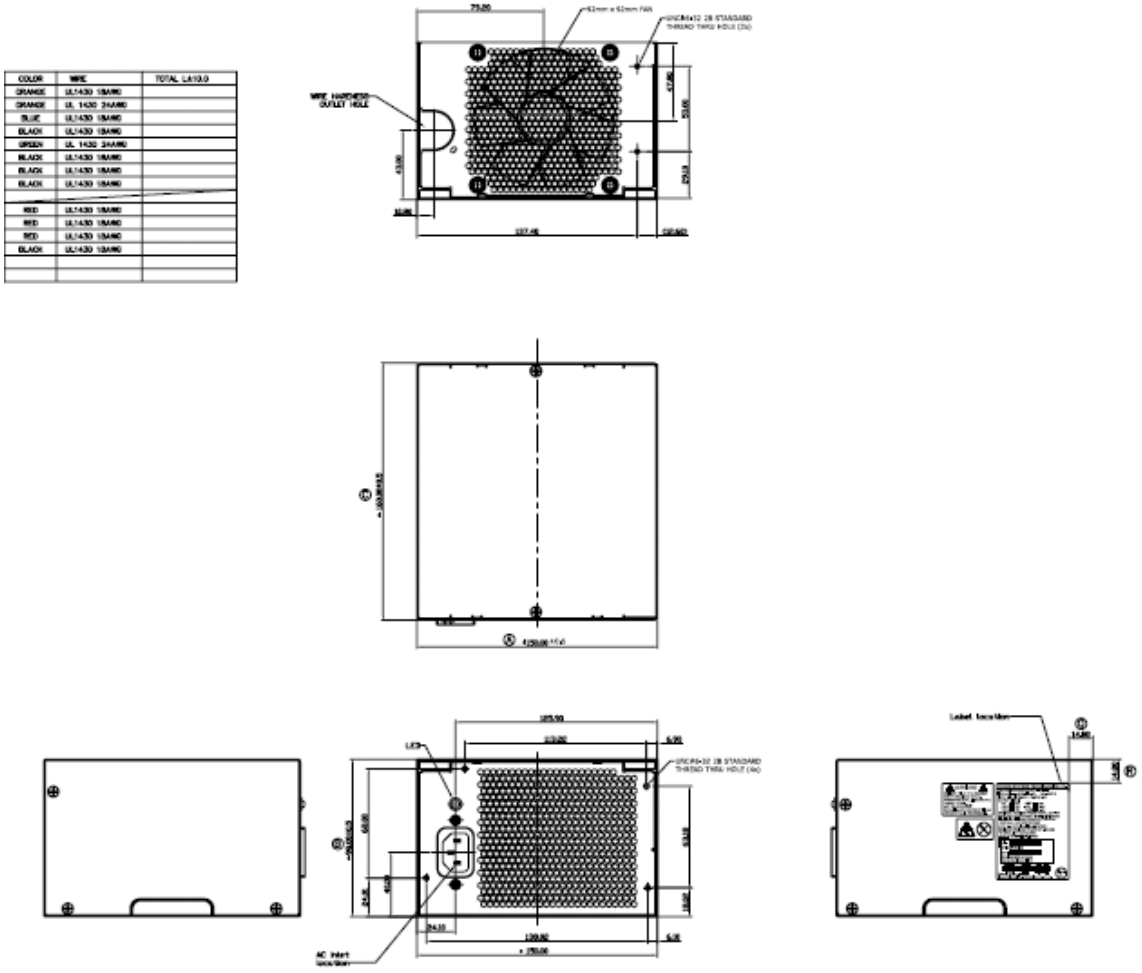


Figure 9. Mechanical Drawing for 550W Power Supply Enclosure

2.1.1.1 550W Power Supply Output Wire Harness

Listed or recognized component appliance wiring material (AVLV2), CN, rated min 85°C shall be used for all output wiring.

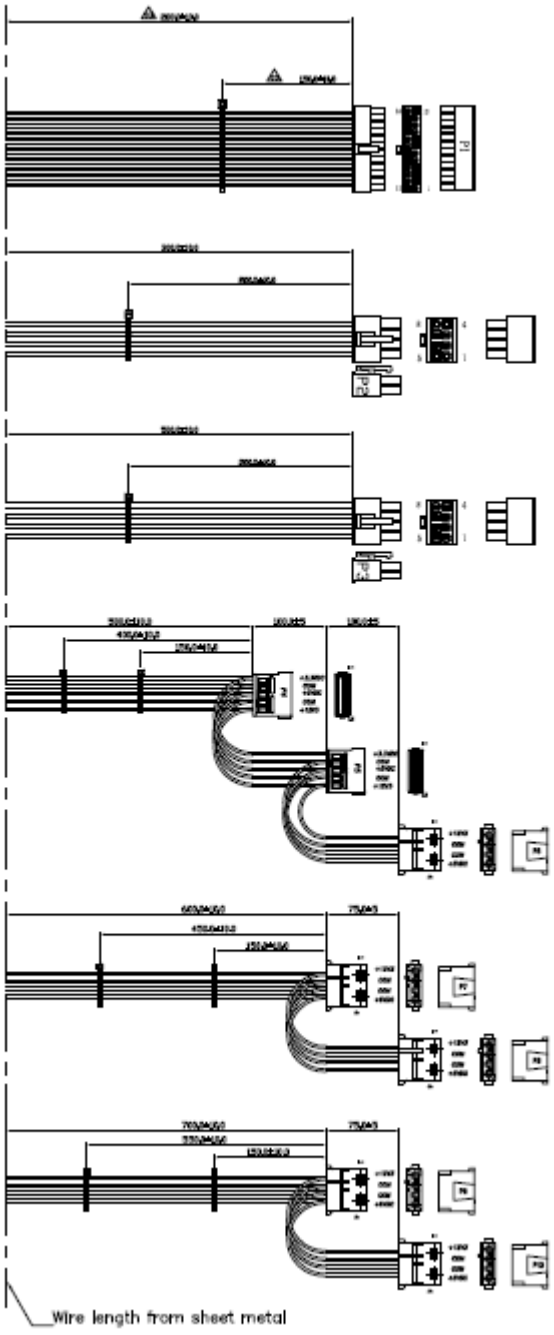


Figure 10. Output Cable Harness for 550W Power Supply

Table 4. Power Supply Cable Lengths

From	Length (mm)	To connector #	No of pins	Description
Power Supply cover exit hole	280	P1	24	Baseboard Power Connector
Power Supply cover exit hole	300	P2	8	Processor 0 connector
Power Supply cover exit hole	500	P3	8	Processor 1 connector
Power Supply cover exit hole	500	P4	5	SATA Peripheral Power Connector for 5.25"
Extension from P4	100	P5	5	SATA Peripheral Power Connector for 5.25"
Extension from P5	100	P6	4	Peripheral Power Connector for 5.25"
Power Supply cover exit hole	600	P7	4	1x4 Legacy HSBP Power Connector
Extension from P7	75	P8	4	1x4 Legacy HSBP Power Connector
Power Supply cover exit hole	700	P9	4	1x4 Legacy HSBP Power/Fixed HDD Adapter Connection
Extension from P9	75	P10	4	1x4 Legacy HSBP Power/Fixed HDD Adapter Connection

2.1.1.1.1 Main power connector (P1)

Connector housing: 24- Pin Molex Mini-Fit Jr 39-01-2245 (94V2) or equivalent
Contact: Molex Minifit Jr, Crimp 5556 or equivalent

Table 5. P1 Main Power Connector

Pin	Signal	18 awg color	Pin	Signal	18 awg color
1	+3.3 VDC	Orange	13	+3.3 VDC	Orange
2	+3.3 VDC	Orange	14	-12 VDC	Blue
3	COM	Black	15	COM	Black
4	+5 VDC*	Red	16	PSON#	Green
5	COM	Black	17	COM	Black
6	+5 VDC	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray	20	Reserved	N.C.
9	5VSB	Purple	21	+5 VDC	Red
10	+12V3	Yellow/Black	22	+5 VDC	Red
11	+12V3	Yellow/Black	23	+5 VDC	Red
12	+3.3 VDC	Orange	24	COM	Black

Note: 3.3V remote sense shall be double crimped into pin 13 if needed to meet regulation limits.

2.1.1.1.2 Processor/Memory Power Connector (P2)

Connector housing: 8- Pin Molex 39-01-2085 (94V2) or equivalent
Contact: Molex, Mini-Fit Jr, HCS, 44476-1111 or equivalent

Table 6. P2 Processor#1 Power Connector

Pin	Signal	18 awg color	Pin	Signal	18 awg color
1	COM	Black	5	+12V1	Yellow
2	COM	Black	6	+12V1	Yellow
3	COM	Black	7	+12V1	Yellow
4	COM	Black	8	+12V1	Yellow

2.1.1.1.3 Processor/Memory Power Connector (P3)

Connector housing: 8- Pin Molex 39-01-2085 (94V2) or equivalent
Contact: Molex, Mini-Fit Jr, HCS, 44476-1111 or equivalent

Table 7. P3 Processor#1 Power Connector

Pin	Signal	18 awg color	Pin	Signal	18 awg color
1	COM	Black	5	+12V2	Yellow
2	COM	Black	6	+12V2	Yellow
3	COM	Black	7	+12V2	Yellow
4	COM	Black	8	+12V2	Yellow

2.1.1.1.4 Peripheral Power Connectors (P6,7,8,9,10)

Connector housing: Amp 1-480424-0 or equivalent
Contact: Amp 61314-1 contact or equivalent

Table 8. Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+12V3	Yellow/Black
2	COM	Black
3	COM	Black
4	+5 VDC	Red

2.1.1.1.5 SATA Hard Drive Power Connectors (P4, P5)

Connector housing: JWT A3811H00-5P (94V2) or equivalent;
Contact: JWT A3811TOP-0D or equivalent

Table 9. SATA Power Connector

Pin	Signal	18 AWG Color
1	+3.3V	Orange
2	COM	Black
3	+5VDC	Red
4	COM	Black
5	+12V3	Yellow/Black

2.1.2 Temperature Requirements

The power supply shall operate within all specified limits over the T_{op} temperature range.

Table 10. Thermal Requirements

Item	Description	Min	Max	Units
T_{op}	Operating temperature range.	0	50	ºC
T_{non-op}	Non-operating temperature range.	-40	70	º C
Altitude	Maximum operating altitude.		3000	meters

2.1.3 AC Input Requirements

2.1.3.1 Power Factor

The power supply meets the power factor requirements stated in the Energy Star® Program Requirements for Computer Servers. These requirements are stated below.

Table 11. Power Factor Requirements for Computer Servers

Output power	20% load	50% load	100% load
Power factor	0.8	0.9	0.95

Tested at 230Vac, 50Hz and 60Hz and 115VAC, 60Hz.
Tested according to *Generalized Internal Power Supply Efficiency Testing Protocol*, Rev 6.4.3.
This is posted at http://efficientpowersupplies.epri.com/methods.asp.

2.1.3.2 AC Inlet Connector

The AC input connector is an *IEC 320 C-14* power inlet. This inlet is rated for 10A/250VAC.

2.1.3.3 AC Input Voltage Specification

The power supply operates within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage does not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC does not cause damage to the power supply, including a blown fuse.

Table 12. AC Input Voltage Range

Parameter	Min	Rated	Vmax	Start up vac	Power off vac
Voltage (110)	90 V_{rms}	100-127 V_{rms}	140 V_{rms}	85VAC +/- 4VAC	70VAC +/- 5VAC
Voltage (220)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}		
Frequency	47 Hz	50/60	63 Hz		

Notes:
1. Maximum input current at low input voltage range shall be measured at 90VAC, at max load.
2. Maximum input current at high input voltage range shall be measured at 180VAC, at max load.
3. This requirement is not to be used for determining agency input current markings.

2.1.3.4 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply meets dynamic voltage regulation requirements. An AC line dropout of any duration does not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time the power supply recovers and meets all turn on requirements. The power supply meets the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration does not cause damage to the power supply.

Table 13. AC Line Holdup time

Loading	Holdup time
75%	12msec

2.1.3.5 AC Line Fuse

The power supply has one line fused in the **single line fuse** on the line (Hot) wire of the AC input. The line fusing is acceptable for all safety agency requirements. The input fuse is a slow blow type. AC inrush current does not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply do not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions

2.1.3.6 AC Line Leakage Current

The maximum leakage current to ground for each power supply is 3.5mA when tested at 240VAC.

2.1.3.7 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions is defined as the AC line voltage dropping below nominal voltage conditions. “Surge” is defined to refer to conditions when the AC line voltage rises above nominal voltage.
The power supply meets the requirements under the following AC line sag and surge conditions.

Table 14. AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30 %	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Table 15. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

2.1.3.8 Power Recovery

The power supply recovers automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

2.1.4 Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels; 100%, 50% and 20%. Output shall be loaded according to the proportional loading method defined by 80 Plus in *Generalized Internal Power Supply Efficiency Testing Protocol*, Rev 6.4.3. This is posted at http://efficientpowersupplies.epri.com/methods.asp.

Table 16. Silver Efficiency Requirement

Loading	100% of maximum	50% of maximum	20% of maximum
Minimum Efficiency	85%	88%	85%

The power supply passes with enough margins to make sure in production all power supplies meet these efficiency requirements.

2.1.4.1 Standby Efficiency

When in standby mode; the power supply draws less than 1W AC power with 100mA of 5Vstandby load. This is tested at 115VAC/60Hz and 230VAC/50Hz.

2.1.5 DC Output Specification

2.1.5.1 Output Power/Currents

The following tables define the minimum power and current ratings. The power supply meets both static and dynamic voltage regulation requirements for all conditions.

Table 17. Over Voltage Protection Limits

Parameter	Min	Max.	Peak	Unit
3.3V	0.5	18.0		A
5V	0.3	15.0		A
12V1	0.7	24.0	28.0	A
12V2	0.7	24.0	28.0	A
12V3	1.5	18.0		
– 12V	0.0	0.5		A
5Vstby	0.0	3.0	3.5	A

Notes:

1. Max combined power for all output shall not exceed 550W.
2. Peak combined power for all outputs shall not exceed 630W for 20 seconds.
3. Max combined power of 12V1, 12V2 and 12V3 shall not exceed 530W.
4. Max combined power on 3.3V and 5V shall not exceed 120W.

2.1.5.2 Cross Loading

The power supply maintains voltage regulation limit when operated over the following cross loading conditions.

Table 18. Loading Conditions

	3.3V	5.0V	12V1	12V2	12V3	-12V	5.0Vstby	Total Power	12V Power	3.3V/5V Power
Load1	18	12.1	12	12	11.7	0	0.3	550	428	120
Load2	13.5	15	12	12	11.2	0.5	0.3	549	422	120
Load3	2.5	2	20	20	4.2	0	0.3	550	530	18
Load4	2.5	2	13.1	13.1	18	0	0.3	550	530	18
Load5	0.5	0.3	15	15	6.5	0.5	3	462	438	3
Load6	16	4	1	1	3.5	0	0.3	140	66	73
Load7	16	13	1	1	9	0.5	3	271	132	118

2.1.5.3 Standby Output

The 5VSB output is present when an AC input greater than the power supply turn on voltage is applied.

2.1.5.4 Voltage Regulation

The power supply output voltages stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. These shall be measured at the output connectors.

Table 19. Voltage Regulation Limits

Parameter	Tolerance	Min	Nom	Max	Units
+3.3V	- 3%/+5%	+3.20	+3.30	+3.46	Vrms
+5V	- 4%/+5%	+4.80	+5.00	+5.25	Vrms
+12V1	- 4%/+5%	+11.52	+12.00	+12.60	Vrms
+12V2	- 4%/+5%	+11.52	+12.00	+12.60	Vrms
+12V3	- 4%/+5%	+11.52	+12.00	+12.60	Vrms
- 12V	- 10%/+10%	- 13.20	-12.00	-10.80	Vrms
+5VSB	- 4%/+5%	+4.80	+5.00	+5.25	Vrms

2.1.5.5 Dynamic Loading

The output voltages remain within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate is tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 20. Transient Load Requirements

Output	Δ Step Load Size (See note 2)	Load Slew Rate	Test capacitive Load
+3.3V	6.0A	0.5 A/μsec	970 μF

Output	Δ Step Load Size (See note 2)	Load Slew Rate	Test capacitive Load
+5V	4.0A	0.5 A/μsec	400 μF
12V1+12V2 +12V3	23.0A	0.5 A/μsec	2200 μF [1,2]
+5VSB	0.5A	0.5 A/μsec	20 μF

Notes:
1. Step loads on each 12V output may happen simultaneously.
2. The +12V should be tested with 2200μF evenly split between the four +12V rails.
3. This will be tested over the range of load conditions.

2.1.5.6 Capacitive Loading

The power supply is stable and meets all requirements with the following capacitive loading ranges.

Table 21. Capacitive Loading Conditions

Output	Min	Max	Units
+3.3V	250	5000	μF
+5V	400	5000	μF
+12V	500	8000	μF
-12V	1	350	μF
+5VSB	20	350	μF

2.1.5.7 Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins are connected to the safety ground (power supply enclosure). This grounding is well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply is provided with a reliable protective earth ground. All secondary circuits are connected to protective earth ground. Resistance of the ground returns to chassis does not exceed 1.0 mΩ. This path may be used to carry DC current.

2.1.5.8 Residual Voltage Immunity in Standby mode

The power supply is immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to **500mV**. There is neither additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also does not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition does not exceed **100mV** when AC voltage is applied and the PSON# signal is de-asserted.

2.1.5.9 Common Mode Noise

The Common Mode noise on any output does not exceed **350mV pk-pk** over the frequency band of 10Hz to 20MHz.

The measurement is made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure).
The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

2.1.5.10 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in the table below. This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor is placed at the point of measurement.

Table 22. Ripples and Noise

+3.3V	+5V	+12V 1, 2, 3	-12V	+5VSB
50mVp-p	50mVp-p	120mVp-p	200mVp-p	50mVp-p

The test set-up shall be as shown below.

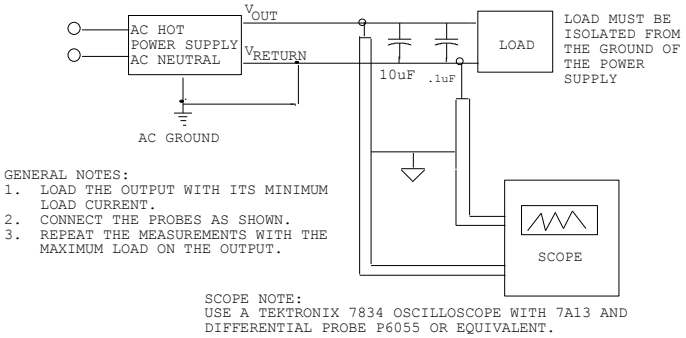


Figure 11. Differential Noise test setup

Note: When performing this test, the probe clips and capacitors should be located close to the load.

2.1.5.11 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages rise from 10% to within regulation limits (T_{vout_rise}) within 2 to 50ms, except for 5VSB - it is allowed to rise from 1 to 25ms. The +3.3V, +5V and +12V1, +12V2, +12V3 output voltages start to rise approximately at the same time**. All outputs rise monotonically**. Each output voltage reach regulation within 50ms (T_{vout_on}) of each other during turn on the power supply. Each output voltage fall out of regulation within 400ms (T_{vout_off}) of each other during turn off. Table 24 shows the timing requirements for the power supply being turned on and off by the AC input, with PSON held low and the PSON signal, with the AC input applied. All timing requirements are met for the cross loading condition in Table 18.

Table 23. Output Voltage Timing

Item	Description	MIN	MAX	UNITS
T_{vout_rise}	Output voltage rise time from each main output.	2	50	ms
	Output rise time for the 5Vstby output.	1	25	ms
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	ms
T_{vout_off}	All main outputs must leave regulation within this time.		400	ms

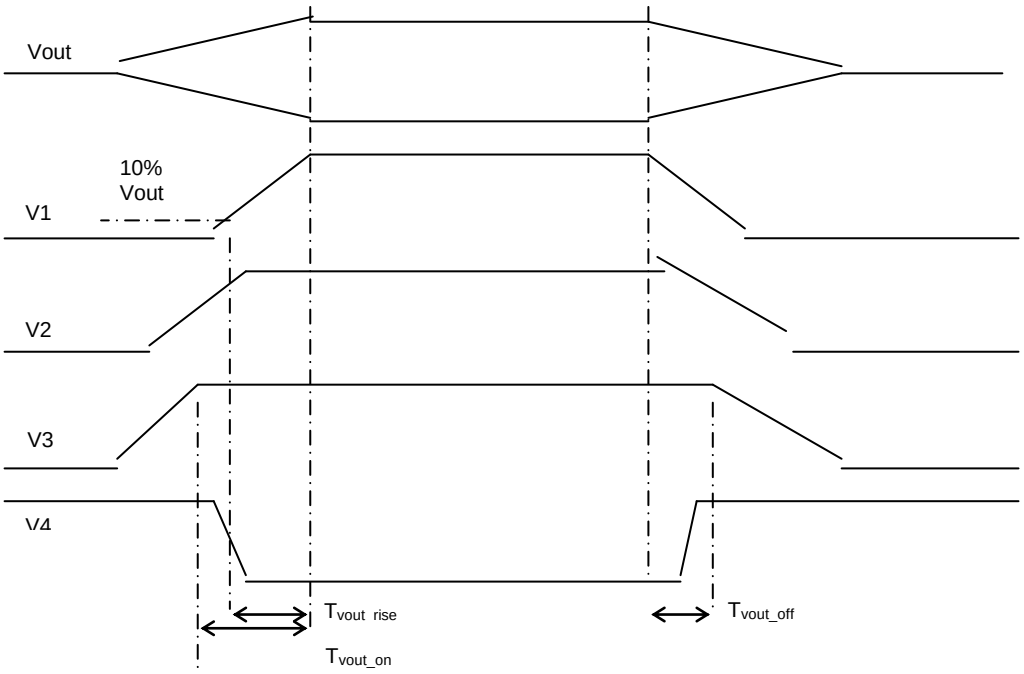


Figure 12. Output Voltage Timing

Table 24. Turn On/Off Timing

Item	Description	MIN	MAX	UNITS
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.		1500	ms
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	ms
T_{vout_holdup}	Time all output voltages stay within regulation after loss of AC. Tested at 75% of maximum load.	13		ms
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK. Tested at 75% of maximum load.	12		ms
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T_{pson_pwok}	Delay from PSON# deactivate to PWOK being de-asserted.		50	ms
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T_{pwok_off}	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		ms
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
T_{sb_vout}	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	10	1000	ms

Item	Description	MIN	MAX	UNITS
T_{5VSB_holdup}	Time the 5VSB output voltage stays within regulation after loss of AC.	70		ms

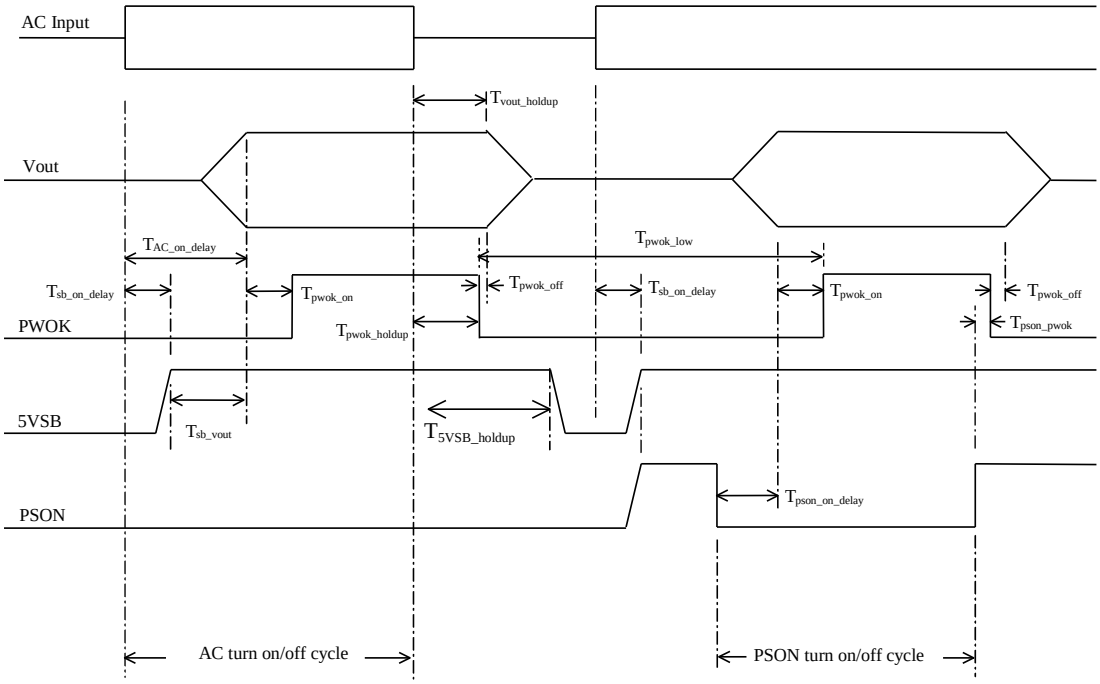


Figure 13. Turn On/Off Timing (Power Supply Signals)

2.1.6 Protection Circuits

Protection circuits inside the power supply causes only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON# cycle HIGH for 1sec able to reset the power supply.

2.1.6.1 Current Limit (OCP)

Below are over current protection limits for each output. If the current limits are exceeded the power supply shuts down and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply does not be damaged from repeated power cycling in this condition. -12V and 5VSB is protected under over current or shorted conditions so that no damage can occur to the power supply. 5Vsb will be auto-recovered after removing OCP limit.

Table 25. Over Current Limits

Output	Min OCP	Max OCP
+3.3V	22 A	Meet 240VA
+5V	16 A	30 A
+12V1,2	29 A	36 A
+12V3 (240VA limited)	18.5 A	20 A

Output	Min OCP	Max OCP
-12V	No damage	
5Vstby	No damage	

2.1.6.2 Over Voltage Protection (OVP)

The power supply over voltage protection is locally sensed. The power supply shuts down and latch off after an over voltage condition occurs. This latch is cleared by toggling the PSON# signal or by an AC power interruption. The table below contains the over voltage limits. The values are measured at the output of the power supply's pins. The voltage shall never exceed the maximum levels when measured at the power pins of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the power supply connector. 5VSB will be auto-recovered after removing OVP limit.

Table 24. Over Voltage Protection (OVP) Limits

Output Voltage	MAX (V)
+3.3V	4.5
+5V	6.5
+12V1,2,3	14.5
+5VSB	6.5

2.1.6.3 Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down.

2.1.7 Control and Indicator Functions

The following sections define the input and output signals from the power supply.
Signals that can be defined as low true use the following convention: Signal# = low true

2.1.7.1 PSON# Input Signal

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +3.3V, +5V, +12V1, +12V2, +12V3 and -12V power rails. When this signal is not pulled low by the system, or left open, the outputs (except the +5VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to Figure 27 for the timing diagram.

Table 26. PSON# Signal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	5.25V
Source current, Vpson = low		4mA
Power up delay: Tpson_on_delay	5msec	400msec
PWOK delay: T pson_pwok		50msec

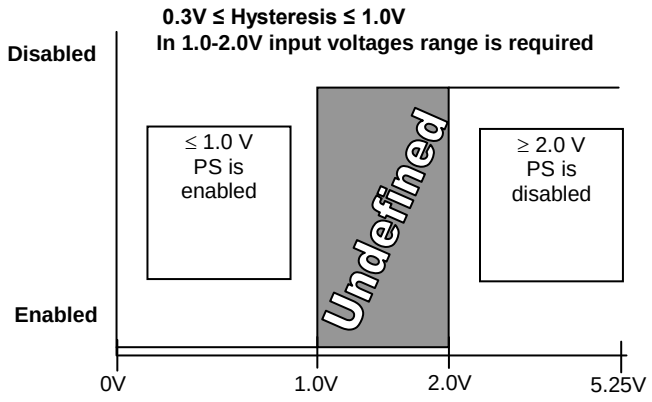


Figure 14. PSON# Required Signal Characteristic

2.1.7.2 PWOK (Power OK) Output Signal

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. Refer to Figure 13 for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

Table 27. PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in system.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	MAX
Logic level low voltage, Isink=4mA	0V	0.4V
Logic level high voltage, Isource=200μA	2.4V	5.25V
Sink current, PWOK = low		4mA
Source current, PWOK = high		2mA
PWOK delay: Tpwok_on	100ms	500ms
PWOK rise and fall time		100μsec
Power down delay: T pwok_off	1ms	

2.2 460W Power Supply

This specification defines a 460W redundant power supply that supports server systems. The parameters of this power supply are defined in this specification. This specification defines a power supply with 2 outputs; 12V and 12V standby. The AC input shall be auto ranging and power factor corrected.

2.2.1 Mechanical Overview

The physical size of the power supply enclosure is 39/40mm x 73.5mm x 185mm. The power supply contains a single 40mm fan. The power supply has a card edge output that interfaces with a 2x25 card edge connector in the system. The AC plugs directly into the external face of the power supply. Refer to the following figure. All dimensions are nominal.

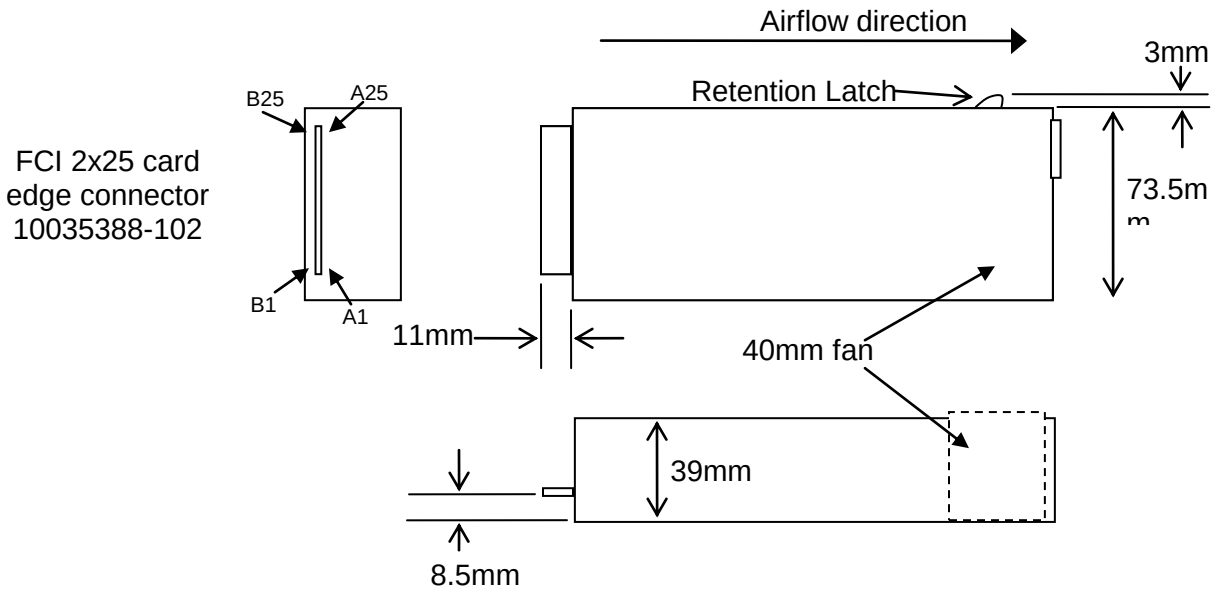


Figure 15. Power Supply Outline Drawing

2.2.1.1 DC Output Connector

The power supply shall use a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector (equivalent to 2x25 pin configuration of the FCI power card connector 10035388-102LF).

Table 28. DC Output Selector

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V

Pin	Name	Pin	Name
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus* SDA	B19	A0 (SMBus* address)
A20	PMBus* SCL	B20	A1 (SMBus* address)
A21	PSON	B21	12V stby
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Return Sense	B23	12V load share bus
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	Compatibility Check pin*

Note: Refer to the *Common Hardware and Firmware Requirements for CRPS Power Supplies Specification*.

2.2.1.2 Handle Retention

The power supply shall have a handle to assist extraction. The module shall be able to be inserted and extracted without the assistance of tools. The power supply shall have a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply.

The handle shall protect the operator from any burn hazard through the use of the Intel Corporation Industrial designed plastic handle or equivalent Intel approved material.

2.2.1.3 LED Marking and Identification

The power supply shall use a bi-color LED; Amber and Green. Below are table showing the LED states for each power supply operating state and the LED's wavelength characteristics.

Refer to the Intel LED Wavelength and Intensity specification for more details.

Table 29. LED Characteristics

	Min λd Wavelength	Nominal λd Wavelength	Max λd Wavelength	Units
Green	562	565	568	nm
Amber	607	610	613	nm

Table 30. LED Indicator States

Power Supply Condition	LED State
Output ON and OK	GREEN
No AC power to all power supplies	OFF

Power Supply Condition	LED State
AC present/Only 12VSB on (PS off) or PS in Cold redundant state	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER
Power supply FW updating	2Hz Blink GREEN

2.2.1.4 Temperature Requirements

The power supply shall operate within all specified limits over the T_{op} temperature range. All airflow shall pass through the power supply and not over the exterior surfaces of the power supply.

Table 31. Environmental Requirements

Item	Description	MIN	MAX	UNITS
$T_{op\_sc\_red}$	Operating temperature range; spreadcore redundant (60% load, 3000m, spreadcore system flow impedance)	0	60	°C
$T_{op\_sc\_nr}$	Operating temperature range; spreadcore non-redundant (100% load, 3000m, spreadcore system flow impedance)	0	50	°C
$T_{op\_rackped\_900}$	Operating temperature range; rack/pedestal 900m (100% load, 900m, rack/pedestal system flow impedance)	0	45	°C
$T_{op\_rackped\_3000}$	Operating temperature range; rack/pedestal 3000m (100% load, 3000m, rack/pedestal system flow impedance)	0	40	°C
Texit	Maximum exit air temperature		68[1]	°C
$T_{non\text{-}op}$	Non-operating temperature range.	-40	70	°C
Altitude	Maximum operating altitude		3050	m

2.2.2 AC Input Requirements

2.2.2.1 Power Factor

The power supply must meet the power factor requirements stated in the Energy Star® Program Requirements for Computer Servers. These requirements are stated below:

Output power	10% load	20% load	50% load	100% load
Power factor	> 0.65	> 0.80	> 0.90	> 0.95

Tested at 230Vac, 50Hz and 60Hz and 115VAC, 60Hz
Tested according to *Generalized Internal Power Supply Efficiency Testing Protocol*, Rev 6.4.3.
This is posted at http://efficientpowersupplies.epri.com/methods.asp.

2.2.2.2 AC Inlet Connector

The AC input connector shall be an *IEC 320 C-14* power inlet. This inlet is rated for 10A/250VAC.

2.2.2.3 AC Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC shall not cause damage to the power supply, including a blown fuse.

Table 32. AC Input Voltage Range

Parameter	MIN	Rated	V_{MAX}	Startup VAC	Power Off VAC
Voltage (110)	90 V_{rms}	100-127 V_{rms}	140 V_{rms}	85VAC +/- 4VAC	74VAC +/- 5VAC
Voltage (220)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}		
Frequency	47 Hz	50/60	63 Hz		

Notes:
1. Maximum input current at low input voltage range shall be measured at 90VAC, at max load.
2. Maximum input current at high input voltage range shall be measured at 180VAC, at max load.
3. This requirement is not to be used for determining agency input current markings.

2.2.2.4 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration shall not cause damage to the power supply.

Loading	Holdup time

70%	12msec

2.2.2.5 AC Line 12VSBHoldup

The 12VSB output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of **70ms min** (=12VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

2.2.2.6 AC Line Fuse

The power supply shall have one line fused in the **single line fuse** on the line (Hot) wire of the AC input. The line fusing shall be acceptable for all safety agency requirements. The input fuse shall be a slow blow type. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

2.2.2.7 AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”; these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.
The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 33 AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30 %	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self-recoverable

Table 34. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

2.2.2.8 Power Recovery

The power supply shall recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

2.2.3 Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels; 100%, 50%, 20%, and 10%. Output shall be loaded according to the proportional loading method defined by 80 Plus in *Generalized Internal*

Power Supply Efficiency Testing Protocol, Rev 6.4.3. This is posted at http://efficientpowersupplies.epri.com/methods.asp.

Table 35. Gold Efficiency Requirement

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Minimum Efficiency	88%	92%	88%	80%

The power supply must pass with enough margins to make sure in production all power supplies meet these efficiency requirements.

2.2.4 DC Output Specification

2.2.4.1 Output Power/Currents

The following table defines the minimum power and current ratings. The power supply must meet both static and dynamic voltage regulation requirements for all conditions.

Table 36. Minimum Load Ratings

Parameter	Min	Max.	Peak [2,3]	Unit
12V main	0.0	38.0	45.0	A
12Vstby [1]	0.0	2.1	2.4	A

Notes:
1. 12Vstby must provide 4.0A with two power supplies in parallel. The Fan may start to work when stby current >1.5A
2. Peak combined power for all outputs shall not exceed 575W.
3. Length of time peak power can be supported is based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration shall be 20 seconds without asserting the SMBAlert# signal at maximum operating temperature.

2.2.4.2 Standby Output

The 12VSB output shall be present when an AC input greater than the power supply turn on voltage is applied. There should be load sharing in the standby rail. And two PSU modules should be able to support 4A standby current.

2.2.4.3 Voltage Regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. These shall be measured at the output connectors.

Table 37. Voltage Regulation Limits

Parameter	Tolerance	MIN	NOM	MAX	UNITS
+12V	- 5%/+5%	+11.40	+12.00	+12.60	V_{rms}
+12V stby	- 5%/+5%	+11.40	+12.00	+12.60	V_{rms}

2.2.4.4 Dynamic Loading

The output voltages shall remain within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 38. Transient Load Requirements

Output	Δ Step Load Size (See note)	Load Slew Rate	Test capacitive Load
+12VSB	1.0A	0.25 A/μsec	20 μF
+12V	60% of max load	0.25 A/μsec	2000 μF

Note: For dynamic condition +12V min loading is 1A.

2.2.4.5 Capacitive Loading

The power supply shall be stable and meet all requirements with the following capacitive loading ranges.

Table 39. Capacitive Loading Conditions

Output	MIN	MAX	Units
+12VSB	20	3100	μF
+12V	500	25000	μF

2.2.4.6 Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC current.

2.2.4.7 Residual Voltage Immunity in Standby mode

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to **500mV**. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed **100mV** when AC voltage is applied and the PSON# signal is de-asserted.

2.2.4.8 Common Mode Noise

The Common Mode noise on any output shall not exceed **350mV pk-pk** over the frequency band of 10Hz to 20MHz.

1. The measurement shall be made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure).
2. The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

2.2.4.9 Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

2.2.4.10 Forced Load Sharing

The +12V output will have active load sharing. The output will share within 10% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot-swap/redundant 1+1 configurations. The 12VSBoutput is not required to actively share current between power supplies (passive sharing). The 12VSB output of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

2.2.4.11 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in the table below. This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor is placed at the point of measurement.

Table 40. Ripples and Noise

+12V main	+12VSB
120mVp-p	120mVp-p

The test set-up shall be as shown below:

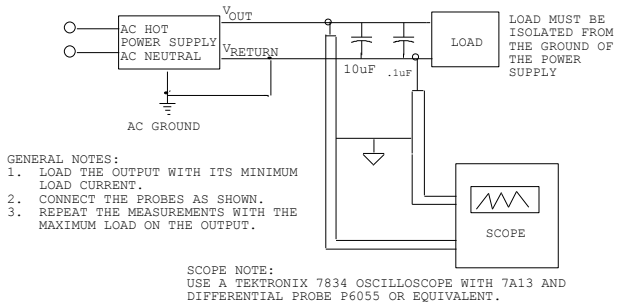


Figure 16. Differential Noise test setup

Note: When performing this test, the probe clips and capacitors should be located close to the load.

2.2.4.12 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70ms. For 12VSB, it is allowed to rise from 1.0 to 25ms. **All outputs must rise monotonically**. Table below shows the timing requirements for the power supply being turned on and off by the AC input, with PSON held low and the PSON signal, with the AC input applied.

Table 41. Timing Requirements

Item	Description	MIN	MAX	UNITS
T_{vout_rise}	Output voltage rise time	5.0 *	70 *	ms
Tsb_on_delay	Delay from AC being applied to 12VSBbeing within regulation.		1500	ms
Tac_on_delay	Delay from AC being applied to all output voltages being within regulation.		3000	ms
Tvout_holdup	Time 12V output voltage stays within regulation after loss of AC at 70% load.	13		ms
Tpwok_holdup	Delay from loss of AC to de-assertion of PWOK	12		ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
Tpson_pwok	Delay from PSON# deactivate to PWOK being de-asserted.		5	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T pwok_off	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1		ms
Tpwok_low	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
Tsb_vout	Delay from 12VSBbeing in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T12VSB_holdup	Time the 12VSBoutput voltage stays within regulation after loss of AC.	70		ms

* The 12VSBoutput voltage rise time shall be from 1.0ms to 25ms

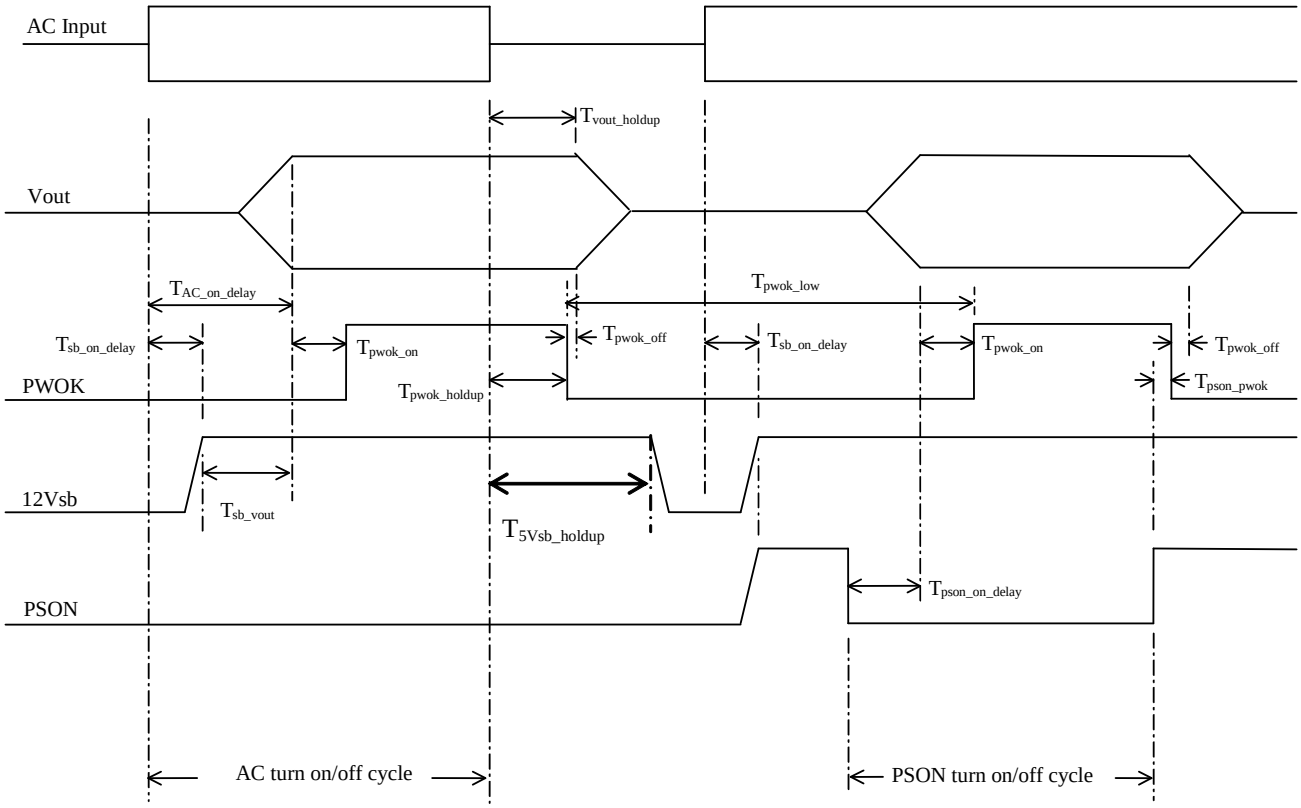


Figure 17. Turn On/Off Timing (Power Supply Signals)

2.2.5 Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

2.2.5.1 Current Limit (OCP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply shall shutdown and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

Table 42. Over Current Protection

Output VOLTAGE	Input voltage range	Over Current Limits
+12V	90 – 264VAC	47A min; 55A max
12VSB	90 – 264VAC	2A min; 2.5A max

2.2.5.2 Over Voltage Protection (OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. 12VSBwill be auto-recovered after removing OVP limit.

Table 43. Over Voltage Protection (OVP) Limits

Output Voltage	MIN (V)	MAX (V)
+12V	13.3	14.5
+12VSB	13.3	14.5

2.2.5.3 Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 4°C of ambient temperature margin.

2.2.6 Control and Indicator Functions

The following sections define the input and output signals from the power supply.
Signals that can be defined as low true use the following convention: *Signal#* = low true

2.2.6.1 PSON# Input Signal

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +12V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +5VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer Figure 17 for the timing diagram.

Table 44. PSON# Signal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.
PSON# = Low	ON
PSON# = High or Open	OFF

	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, Vpson = low		4mA
Power up delay: $T_{pson\_on\_delay}$	5msec	400msec
PWOK delay: T_{pson_pwok}		50msec

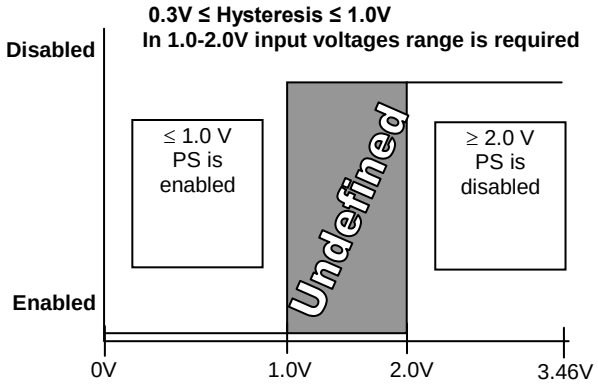


Figure 18. PSON# Required Signal Characteristic

2.2.6.2 PWOK (Power OK) Output Signal

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See the table below for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

Table 45. PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in the power supply.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	MAX
Logic level low voltage, Isink=400uA	0V	0.4V
Logic level high voltage, Isource=200μA	2.4V	3.46V
Sink current, PWOK = low		400uA

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in the power supply.	
Source current, PWOK = high		2mA
PWOK delay: T_{pwok_on}	100ms	1000ms
PWOK rise and fall time		100μsec
Power down delay: T_{pwok_off}	1ms	200msec

A recommended implementation of the Power Ok circuits is shown below.

Note: The Power Ok circuits should be compatible with 5V pull up resistor (>10k) and 3.3V pull up resistor (>6.8k).

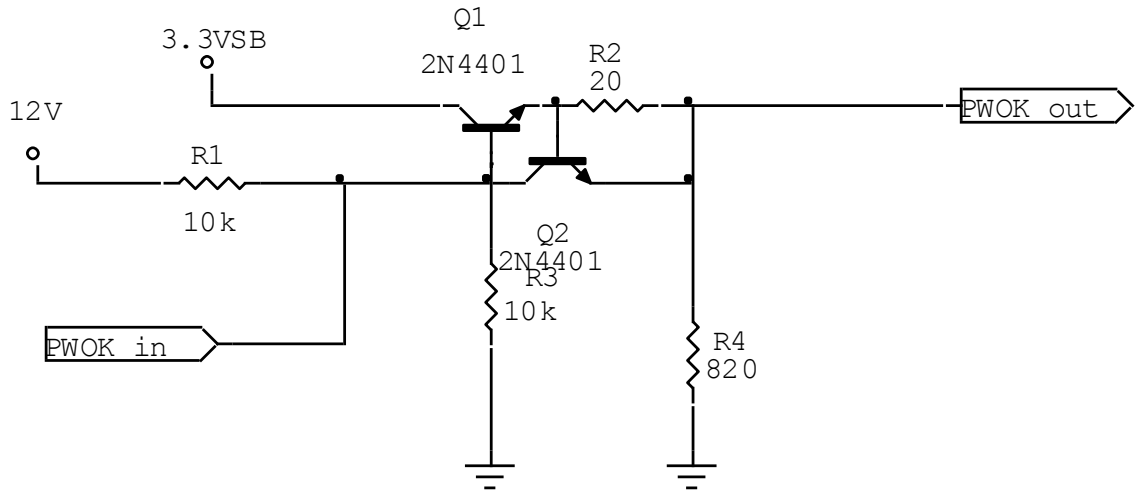


Figure 19. Implementation of the Power Ok Circuits

2.2.6.3 SMBAlert# Signal

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.
This signal is to be asserted in parallel with LED turning solid Amber or blink Amber.

Table 46. SMBAlert# Signal Characteristics

Signal Type (Active Low)	Open collector/drain output from power supply. Pull-up to VSB located in system.	
Alert# = High	OK	
Alert# = Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 μA		3.46 V
Sink current, Alert# = low		4 mA
Sink current, Alert# = high		50 μA
Alert# rise and fall time		100 μs

2.2.7 Thermal CLST

The power supply shall assert the SMBAlert signal when a temperature sensor crosses a warning threshold. Refer to the *Intel® Common Hardware and Firmware Requirements for CRPS Power Supplier* for detailed requirements.

2.2.8 Power Supply Diagnostic "Black Box"

The power supply shall save the latest PMBus* data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data shall be accessible from the SMBus* interface with an external source providing power to the 12Vstby output.

Refer to *Intel® Common Hardware and Firmware Requirements for CRPS Power Supplier* for detailed requirements.

2.2.9 Firmware Uploader

The power supply shall have the capability to update its firmware from the PMBus* interface while it is in standby mode. This FW can be updated when in the system and in standby mode and outside the system with power applied to the 12Vstby pins.
Refer to the *Intel® Common Hardware and Firmware Requirements for CRPS Power Supplier* for detailed requirements.

2.3 750-W Power Supply

This specification defines a 750W redundant power supply that supports server systems. This power supply has 2 outputs; 12V and 12V standby. The AC input is auto ranging and power factor corrected.

2.3.1 Mechanical Overview

The physical size of the power supply enclosure is 39/40mm x 73.5mm x 185mm. The power supply contains a single 40mm fan. The power supply has a card edge output that interfaces with a 2x25 card edge connector in the system. The AC plugs directly into the external face of the power supply. Refer to the figure below. All dimensions are nominal.

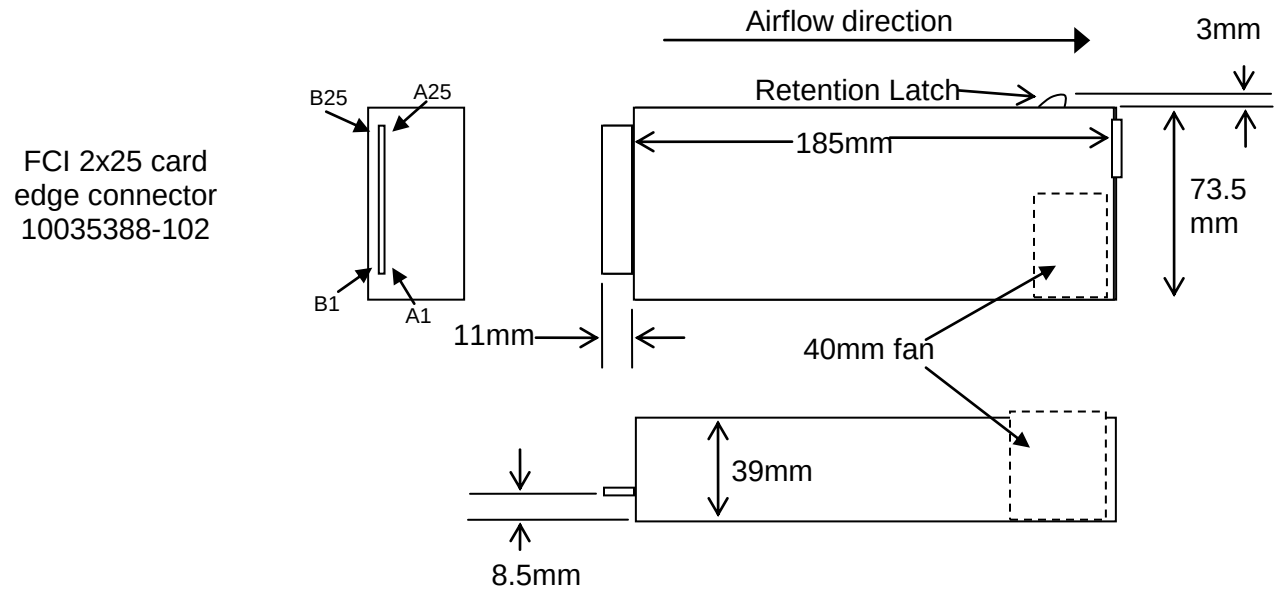


Figure 20. 750-W Power Supply Outline Drawing

2.3.1.1 DC Output Connector

The power supply uses a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector (equivalent to 2x25 pin configuration of the FCI power card connector 10035388-102LF).

Table 47. DC Output Connector

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V

Pin	Name	Pin	Name
A19	PMBus* SDA	B19	A0 (SMBus* address)
A20	PMBus* SCL	B20	A1 (SMBus* address)
A21	PSON	B21	12V stby
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Return Sense	B23	12V load share bus
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	Compatibility Check pin

2.3.1.2 Handle Retention

The power supply has a handle to assist extraction. The module is able to be inserted and extracted without the assistance of tools. The power supply has a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply.

The handle protects the operator from any burn hazard.

2.3.1.3 LED Marking and Identification

The power supply uses a bi-color LED: Amber and Green. Below are table showing the LED states for each power supply operating state and the LED's wavelength characteristics. Refer to the Intel LED Wavelength and Intensity specification for more details.

Table 48. LED Characteristics

	Min λd Wavelength	Nominal λd Wavelength	Max λd Wavelength	Units
Green	562	565	568	nm
Amber	607	610	613	nm

Table 49. Power Supply LED Functionality

Power Supply Condition	LED State
Output ON and OK	GREEN
No AC power to all power supplies	OFF
AC present/Only 12VSB on (PS off) or PS in Cold redundant state	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER
Power supply FW updating	2Hz Blink GREEN

2.3.1.4 Temperature Requirements

The power supply operates within all specified limits over the T_{op} temperature range. All airflow passes through the power supply and not over the exterior surfaces of the power supply.

Table 50. Environmental Requirements

Item	Description	Min	Max	Units
$T_{op\_sc\_red}$	Operating temperature range; spreadcore redundant (60% load, 3000m, spreadcore system flow impedance2)	0	60	°C
$T_{op\_sc\_nr}$	Operating temperature range; spreadcore non-redundant (100% load, 3000m, spreadcore system flow impedance2)	0	50	°C
$T_{op\_rackped\_900}$	Operating temperature range; rack/pedestal 900m (100% load, 900m, rack/pedestal system flow impedance2)	0	45	°C
$T_{op\_rackped\_3000}$	Operating temperature range; rack/pedestal 3000m (100% load, 3000m, rack/pedestal system flow impedance2)	0	40	°C
Texit	Maximum exit air temperature		68	°C
$T_{non\text{-}op}$	Non-operating temperature range.	-40	70	°C
Altitude	Maximum operating altitude 3		3050	m

Notes:

1. Under normal conditions, the exit air temperature shall be less than 65C. 68C is provided for absolute worst case conditions and is expected only to exist when the inlet ambient reaches 60C.
2. $T_{op\_rackped\_900}$ condition only requires max altitude of 900m.

The power supply meets UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side are classified as “Handle, knobs, grips, and so on held for short periods of time only”.

2.3.2 AC Input Requirements

2.3.2.1 Power Factor

The power supply meets the power factor requirements stated in the *Energy Star® Program Requirements for Computer Servers*. These requirements are stated below.

Table 51. Power Factor Requirements for Computer Servers

Output power	10% load	20% load	50% load	100% load
Power factor	> 0.65	> 0.80	> 0.90	> 0.95

Tested at 230Vac, 50Hz and 60Hz and 115VAC, 60Hz
Tested according to *Generalized Internal Power Supply Efficiency Testing Protocol,* Rev 6.4.3.
This is posted at http://efficientpowersupplies.epri.com/methods.asp.

2.3.2.2 AC Inlet Connector

The AC input connector is an *IEC 320 C-14* power inlet. This inlet is rated for 10A/250VAC.

2.3.2.3 AC Input Voltage Specification

The power supply operates within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage does not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC does not cause damage to the power supply, including a blown fuse.

Table 52. AC Input Voltage Range

PARAMETER	MIN	RATED	V_{MAX}	Start up VAC	Power Off VAC
Voltage (110)	90 V_{rms}	100-127 V_{rms}	140 V_{rms}	85VAC +/- 4VAC	74VAC +/- 5VAC
Voltage (220)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}		
Frequency	47 Hz	50/60	63 Hz		

Notes:

1. Maximum input current at low input voltage range shall be measured at 90VAC, at max load.
2. Maximum input current at high input voltage range shall be measured at 180VAC, at max load.
3. This requirement is not to be used for determining agency input current markings.

2.3.2.4 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply meets dynamic voltage regulation requirements. An AC line dropout of any duration does not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time the power supply recovers and meets all turn on requirements. The power supply meets the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration does not cause damage to the power supply.

Table 53. AC Line Holdup Time

Loading	Holdup time
70%	12msec

2.3.2.5 AC Line 12VSBHoldup

The 12VSB output voltage stays in regulation under its full load (static or dynamic) during an AC dropout of **70ms min** (=12VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

2.3.2.6 AC Line Fuse

The power supply has one line fused in the **single line fuse** on the line (Hot) wire of the AC input. The line fusing is acceptable for all safety agency requirements. The input is a slow blow type. AC inrush current does not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply does not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

2.3.2.7 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions is defined as the AC line voltage dropping below nominal voltage conditions. “Surge” is defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply meets the requirements under the following AC line sag and surge conditions.

Table 54. AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Table 55. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

2.3.2.8 Power Recovery

The power supply shall recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

2.3.3 Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels; 100%, 50%, 20%, and 10%. Output shall be loaded according to the proportional loading method defined by 80 Plus in *Generalized Internal Power Supply Efficiency Testing Protocol,* Rev. 6.4.3. This is posted at http://efficientpowersupplies.epri.com/methods.asp.

Table 56. Silver Efficiency Requirement

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Minimum Efficiency	91%	94%	90%	82%

The power supply passes with enough margins to make sure all power supplies in production meet these efficiency requirements.

2.3.4 DC Output Specification

2.3.4.1 Output Power/Currents

The following table defines the minimum power and current ratings. The power supply meets both static and dynamic voltage regulation requirements for all conditions.

Table 57. Minimum Load Ratings

Parameter	Min	Max.	Peak 2, 3	Unit
12V main	0.0	62.0	70.0	A
12Vstby 1	0.0	2.1	2.4	A

Notes:

1. 12Vstby must provide 4.0A with two power supplies in parallel. The Fan may work when stby current >1.5A
2. Length of time peak power can be supported is based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration shall be 20 seconds without asserting the SMBAlert# signal at maximum operating temperature.

2.3.4.2 Pmax Power support

The PSU should support 3msec peak power duration at a 50msec period; 5.7% duty cycle, Step loading from 730W to 1050W, Average power = 750W. Full AC input range; 100-127VAC/200-240VAC

2.3.4.3 Standby Output

The 12VSB output is present when an AC input greater than the power supply turn on voltage is applied.

2.3.4.4 Voltage Regulation

The power supply output voltages stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. These shall be measured at the output connectors.

Table 58. Voltage Regulation Limits

Parameter	Tolerance	Min	Nom	Max	Units
+12V	- 5%/+5%	+11.40	+12.00	+12.60	V_{rms}
+12V stby	- 5%/+5%	+11.40	+12.00	+12.60	V_{rms}

2.3.4.5 Dynamic Loading

The output voltages remains within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate is tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 59. Transient Load Requirements

Output	Δ Step Load Size (See note 2)	Load Slew Rate	Test capacitive Load

+12VSB	1.0A	0.25 A/μsec	20 μF
+12V	60% of max load	0.25 A/μsec	2000 μF

Note:
For dynamic condition +12V min loading is 1A.

2.3.4.6 Capacitive Loading

The power supply is stable and meets all requirements with the following capacitive loading ranges.

Table 60. Capacitive Loading Conditions

Output	Min	Max	Units
+12VSB	20	3100	μF
+12V	500	25000	μF

2.3.4.7 Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins are connected to the safety ground (power supply enclosure). This grounding is well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply is provided with a reliable protective earth ground. All secondary circuits are connected to protective earth ground. Resistance of the ground returns to chassis does not exceed 1.0 mΩ. This path may be used to carry DC current.

2.3.4.8 Residual Voltage Immunity in Standby mode

The power supply is immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There is neither additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also does not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition does not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

2.3.4.9 Common Mode Noise

The Common Mode noise on any output does not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz. The measurement is made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure). The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

2.3.4.10 Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages remains within the limits with the capacitive load specified. The hot swap test is conducted when the system is operating

under static, dynamic, and zero loading conditions. The power supply uses a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

2.3.4.11 Forced Load Sharing

The +12V output will have active load sharing. The output will share within 10% at full load. The failure of a power supply does not affect the load sharing or output voltages of the other supplies still operating. The supplies are able to load share in parallel and operate in a hot-swap/redundant **1+1** configurations. The 12VSB output is not required to actively share current between power supplies (passive sharing). The 12VSB output of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

2.3.4.12 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in below Table. 41. This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor is placed at the point of measurement.

Table 61. Ripples and Noise

+12V main	+12VSB
120mVp-p	120mVp-p

The test set-up shall be as shown below:

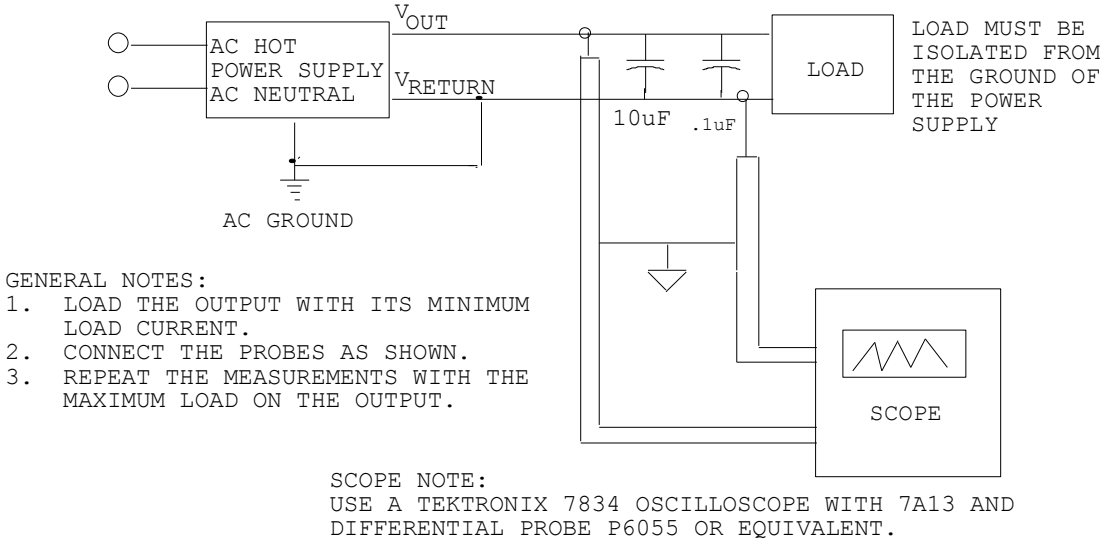


Figure 21. Differential Noise test setup

Note: When performing this test, the probe clips and capacitors should be located close to the load.

2.3.4.13 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70ms. For 12VSB, it is allowed to rise from 1.0 to 25ms. **All outputs must rise monotonically**. Table below shows the timing requirements for the power supply being turned on and off by the AC input, with PSON held low and the PSON signal, with the AC input applied.

Table 62. Timing Requirements

Item	Description	Min	Max	Units
T^{vout_rise}	Output voltage rise time	5.0 *	70 *	ms
$T_{sb\_on\_delay}$	Delay from AC being applied to 12VSBbeing within regulation.		1500	ms
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		3000	ms
T_{vout_holdup}	Time 12VI output voltage stay within regulation after loss of AC.	13		ms
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	12		ms
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T_{pson_pwok}	Delay from PSON# deactivate to PWOK being de-asserted.		5	ms
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T_{pwok_off}	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1		ms
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
T_{sb_vout}	Delay from 12VSBbeing in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T_{12VSB_holdup}	Time the 12VSBoutput voltage stays within regulation after loss of AC.	70		ms

* The 12VSBoutput voltage rise time shall be from 1.0ms to 25ms.

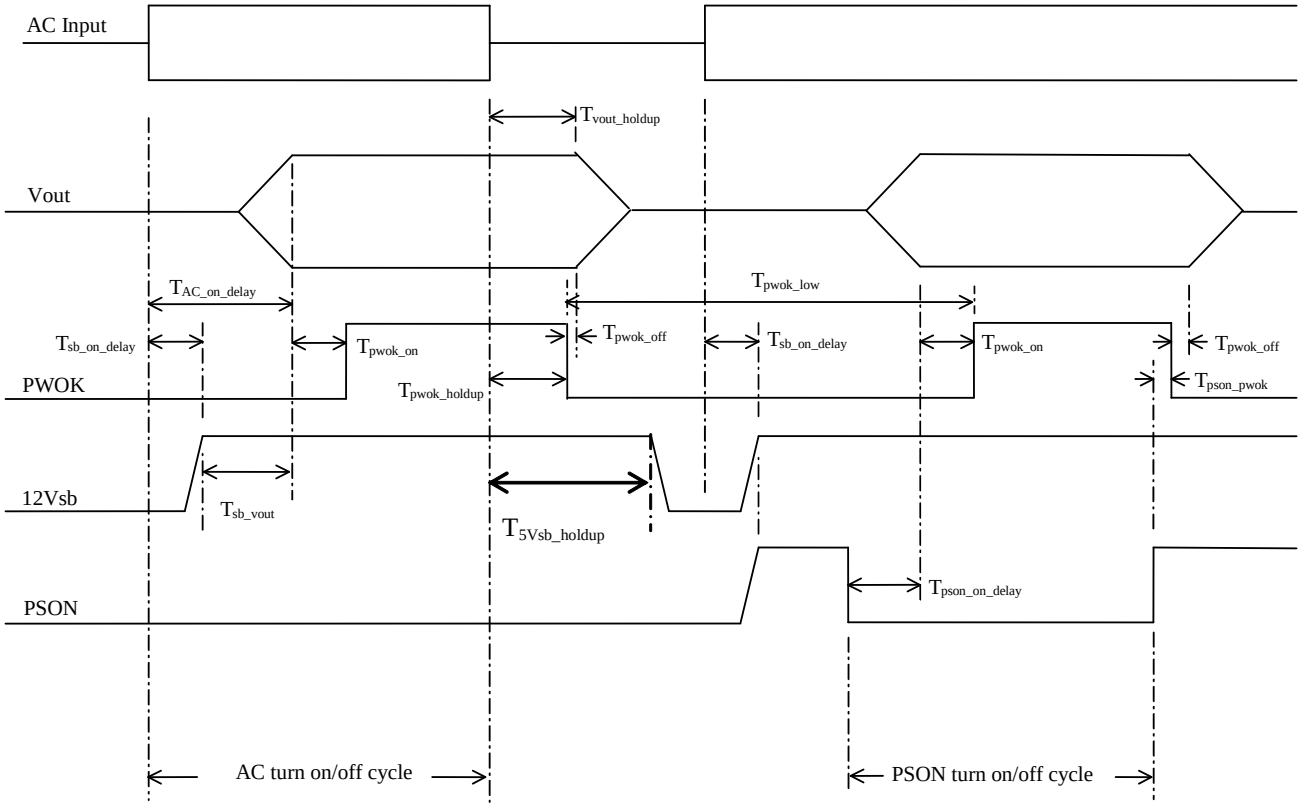


Figure 22. Turn On/Off Timing (Power Supply Signals)

2.3.5 Protection Circuits

Protection circuits inside the power supply causes only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 seconds and a PSON# cycle HIGH for one second are able to reset the power supply.

2.3.5.1 Current Limit (OCP)

The power supply has current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply shuts down and latches off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply does not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

Table 63. Over Current Protection

Output VOLTAGE	Input voltage range	Over Current Limits
+12V	90 – 264VAC	72A min; 78A max
12VSB	90 – 264VAC	2.5A min; 3.5A max

2.3.5.2 Over Voltage Protection (OVP)

The power supply over voltage protection is locally sensed. The power supply shuts down and latches off after an over voltage condition occurs. This latch is cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage does not exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage doesn't trip any lower than the minimum levels when measured at the power connector. 12VSBwill be auto-recovered after removing OVP limit.

Table 64. Over Voltage Protection (OVP) Limits for 750W PSU

Output voltage	Min (v)	Max (v)
+12V	13.0	14.5
+12VSB	13.0	14.5

2.3.5.3 Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 4°C of ambient temperature margin.

2.3.6 Control and Indicator Functions

The following sections define the input and output signals from the power supply. Signals that can be defined as low true use the following convention: Signal# = low true.

2.3.6.1 PSON# Input Signal

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +12V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +12VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply.

Table 65. PSON# Signal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, Vpson = low		4mA
Power up delay: $T_{pson\_on\_delay}$	5msec	400msec
PWOK delay: T_{pson_pwok}		50msec

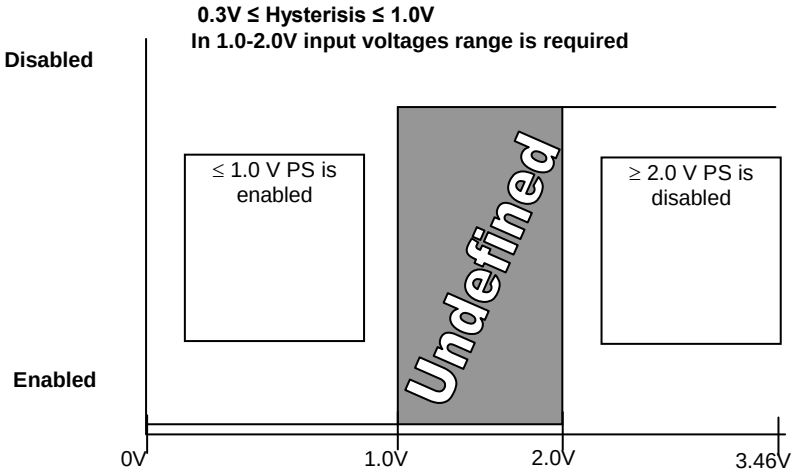


Figure 23. PSON# Required Signal Characteristic

2.3.6.2 PWOK (Power OK) Output Signal

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See Table 46 for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

Table 66. PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in the power supply.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	MAX
Logic level low voltage, Isink=400uA	0V	0.4V
Logic level high voltage, Isource=200μA	2.4V	3.46V
Sink current, PWOK = low		400uA
Source current, PWOK = high		2mA
PWOK delay: T_{pwok_on}	100ms	1000ms
PWOK rise and fall time		100μsec
Power down delay: T_{pwok_off}	1ms	200msec

A recommended implementation of the Power Ok circuits is shown below.

Note: The Power Ok circuits should be compatible with 5V pull up resistor (>10k) and 3.3V pull up resistor (>6.8k).

2.3.6.3 SMBAlert# Signal

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold (see sec. 4.10), general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

This signal is to be asserted in parallel with LED turning solid Amber or blink Amber.

Table 67. SMBAlert# Signal Characteristics

Signal Type (Active Low)	Open collector/drain output from power supply. Pull-up to VSB located in system.	
Alert# = High	OK	
Alert# = Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 μA		3.46 V
Sink current, Alert# = low		4 mA
Sink current, Alert# = high		50 μA
Alert# rise and fall time		100 μs

2.3.7 Thermal CLST

The power supply shall assert the SMBAlert signal when a temperature sensor crosses a warning threshold. Refer to the *Intel® Common Hardware and Firmware Requirements for CRPS Power Supplier* for detailed requirements.

2.3.8 Power Supply Diagnostic "Black Box"

The power supply saves the latest PMBus* data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data is accessible by the SMBus* interface with an external source providing power to the 12Vstby output.

Refer to the *Intel® Common Hardware and Firmware Requirements for CRPS Power Supplier* for detailed requirements.

2.3.9 Firmware Uploader

The power supply has the capability to update its firmware from the PMBus* interface while it is in standby mode. This FW can be updated when in the system and in standby mode and outside the system with power applied to the 12Vstby pins.

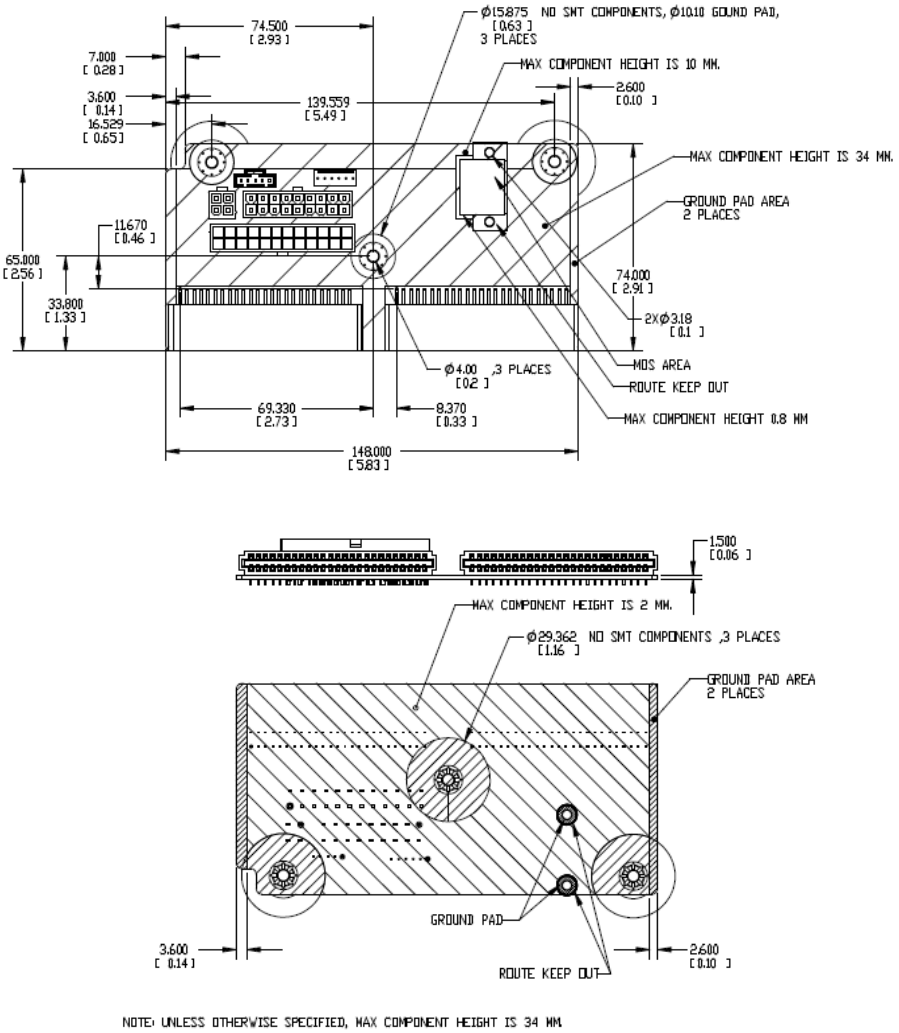
Refer to the *Intel® Common Hardware and Firmware Requirements for CRPS Power Supplier* for detailed requirements.

2.4 Lower Current Common Redundant Power Distribution Board (PDB)

The Power Distribution Board (PDB) for Intel® Server Chassis P4304SC2SHDR supports the Common Redundant power supply in a 1+1 redundant configuration. The PDB is designed to plug directly to the output connector of the PS and it contains 4 DC/DC power converters to produce other required voltages: -12V, +3.3VDC, +5VDC and 5V standby along with additional over current protection circuit for the 12V rails.

This power distribution board is intended to be used in the Intel® Server System P4304SC2SHDR with 460W common redundant power supply.

2.4.1 Mechanical Overview



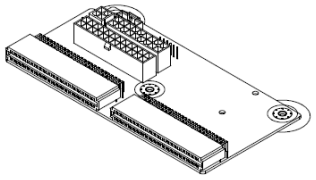


Figure 24. Outline Drawing

2.4.1.1 Airflow Requirements

The power distribution board shall get enough airflow for cooling DC/DC converters from the fans located in the Power Supply modules. Below is a basic drawing showing airflow direction.

The amount of cooling airflow that will be available to the DC/DC converters is to be no less than 1.2M/s.

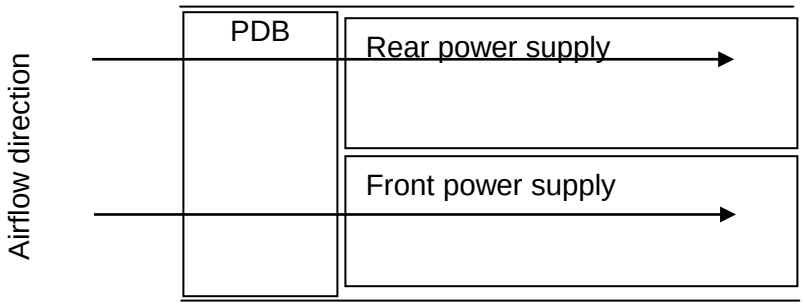


Figure 25. Airflow Diagram

2.4.1.2 DC/DC converter cooling

The dc/dc converters on the power distribution board are in series airflow path with the power supplies.

2.4.1.3 Temperature Requirements

The PDB operates within all specified limits over the Top temperature range. Some amount of airflow shall pass over the PDB.

Tabel 68. Thermal Requirements

Item	Description	Min	Max	Units
T_{op}	Operating temperature range.	0	50	°C
T_{non-op}	Non-operating temperature range.	-40	70	°C

2.4.1.4 Efficiency

Each DC/DC converter shall have a **minimum** efficiency of **85%** at 50% ~ 100% loads and over +12V line voltage range and over temperature and humidity range.

2.4.2 DC Output Specification

2.4.2.1 Input Connector (power distribution mating connector)

The power distribution provides 2 power pin, a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector (equivalent to 2x25 pin configuration of the FCI power card connector 10035388-102LF). The FCI power card edge connector is a new version of the PCE from FCI used to raise the card edge by 0.031" to allow for future 0.093" PCBs in the system. The card edge connector has no keying features; the keying method is accomplished by the system sheet metal.

Table 69. Input Connector and Pin Assignment Diagrams

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus* SDA	B19	A0 (SMBus* address)
A20	PMBus* SCL	B20	A1 (SMBus* address)
A21	PSON	B21	12V stby
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Return Sense	B23	12V load share
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	Compatibility Pin

2.4.2.2 Output Wire Harness

The power distribution board has a wire harness output with the following connectors.

Listed or recognized component appliance wiring material (AVLV2), CN, rated min 85°C shall be used for all output wiring.

Table 70. PDB Cable Length

From	Length, mm	To connector #	No. of pins	Description
Power Supply cover exit hole	470	P1	24	Baseboard Power Connector
Power Supply cover exit hole	320	P2	8	Processor 0 connector
Power Supply cover exit hole	450	P3	8	Processor 1 connector
Power Supply cover exit hole	800	P4	5	Power FRU/PMBus* connector
Power Supply cover exit hole	350	P5	5	SATA peripheral power connector for 5.25”
Extension from P5	100	P6	5	SATA peripheral power connector for 5.25”
Extension from P6	100	P7	4	Peripheral Power Connector for 5.25”/HSBP Power
Power Supply cover exit hole	400	P8	4	1x4 legacy HSBP Power Connector
Extension from P8	75	P9	4	1x4 legacy HSBP Power Connector
Power supply cover exit hole	500	P10	4	1x4 legacy HSBP Power/Fixed HDD adaptor Connection
Extension from P10	75	P11	4	1x4 legacy HSBP Power/Fixed HDD adaptor Connection
Connetor only (no cable)		P12	4	2x2 Legacy PCI Power Connector for PCIe slots

2.4.2.2.1 Baseboard power connector (P1)

- Connector housing: 24-Pin Molex Mini-Fit Jr. 39-01-2245 or equivalent
- Contact: Molex Mini-Fit, HCS Plus, Female, Crimp 44476 or equivalent

Table 71. P1 Baseboard Power Connector

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	+3.3VDC	Orange	13	+3.3VDC	Orange
	3.3V RS	Orange (24AWG)			
2	+3.3VDC	Orange	14	-12VDC	Blue
3	COM	Black	15	COM	Black
4	+5VDC	Red	16	PSON#	Green (24AWG)
5	COM	Black	17	COM	Black
6	+5VDC	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray (24AWG)	20	Reserved	N.C.
9	5 VSB	Purple	21	+5VDC	Red
10	+12V1	Yellow	22	+5VDC	Red
11	+12V1	Yellow	23	+5VDC	Red
12	+3.3VDC	Orange	24	COM	Black

2.4.2.2.2 Processor#0 Power Connector (P2)

- Connector housing: 8-Pin Molex 39-01-2080 or equivalent
- Contact: Molex Mini-Fit, HCS Plus, Female, Crimp 44476 or equivalent

Table 72. P0 Processor Power Connector

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5*	+12V1	Yellow
2	COM	Black	6	+12V1	Yellow
3	COM	Black	7	+12V1	Yellow
4	COM	Black	8	+12V1	Yellow

2.4.2.2.3 Processor#1 Power Connector (P3)

- Connector housing: 8-Pin Molex 39-01-2080 or equivalent
- Contact: Molex Mini-Fit, HCS Plus, Female, Crimp 44476 or equivalent

Table 73. P1 Processor Power Connector

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5	+12V1	Yellow
2	COM	Black	6	+12V1	Yellow
3	COM	Black	7	+12V1	Yellow
4	COM	Black	8	+12V1	Yellow

2.4.2.2.4 Power Signal Connector (P4)

- Connector housing: 5-pin Molex 50-57-9405 or equivalent
- Contacts: Molex 16-02-0087 or equivalent

Table 74. Power Signal Connector

Pin	Signal	24 AWG Color
1	I2C Clock	White
2	I2C Data	Yellow
3	SMBAlert#	Red
4	COM	Black
5	3.3RS	Orange

2.4.2.2.5 Aux baseboard power connector (P12)

Connector header: Foxconn p/n HM3502E-P1 or equivalent

Table 75. Aux baseboard power connector

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	3	+12V1	Yellow
2	COM	Black	4	+12V1	Yellow

2.4.2.2.6 Legacy 1x4 Peripheral Power Connectors (P7, P8, P9, P10, P11)

- Connector housing: Molex 0015-24-4048 or equivalent;
- Contact: Molex 0002-08-1201 or equivalent

Table 76. P8, P9, P10, P11 Legacy Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+12V3	White
2	COM	Black
3	COM	Black
4	+5 VDC	Red

Table 77. P7 Legacy Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+12V2	Brown
2	COM	Black
3	COM	Black
4	+5 VDC	Red

2.4.2.2.7 SATA 1x5 Peripheral Power Connectors (P5, P6)

- Connector housing: Molex 0675-82-0000 or equivalent;
- Contact: Molex 0675-81-0000 or equivalent

Table 78. SATA Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+3.3VDC	Orange
2	COM	Black
3	+5VDC	Red
4	COM	Black
5	+12V2	Brown

2.4.2.3 Grounding

The ground of the pins of the PDB output connectors provides the power return path. The output connector ground pins is connected to safety ground (PDB enclosure). This grounding is well designed to ensure passing the max allowed Common Mode Noise levels.

2.4.2.4 Remote Sense

Below is listed the remote sense requirements and connection points for all the converters on the PDB and the main 12V output of the power supply.

Table 79. Remote Sense Connection Points

Converter	+ sense location	- sense location
Power supply main 12V	On PDB	On PDB
12V/3.3V	P20 (1x5 signal connector)	P20 (1x5 signal connector)
12V/5V	On PDB	On PDB
12V/-12V	none	none
12Vstby/5Vstby	none	none

Table 80. Remote Sense Requirements

Characteristic	Requirement
+3.3V remote sense input impedance	200Ω (measure from +3.3V on P1 2x12 connector to +3.3V sense on P20 1x5 signal connector)
+3.3V remote sense drop	200mV (remote sense must be able to regulate out 200mV drop on the +3.3V and return path; from the 2x12 connector to the remote sense points)
Max remote sense current draw	< 5mA

2.4.2.5 12V Rail Distribution

The following table shows the configuration of the 12V rails and what connectors and components in the system they are powering.

Table 81. 12V Rail Distribution

	P2		P3		P12	P1	P8	P9	P10	P11	P5,6,7				
			2x4		2x2	2x12	1x4	1x4	1x4	1x4	(2) 1x5, 1x4		OCP		
	CPU1	Memory1	CPU2	Memory2	PCIe	Fans	Misc	HDD and peripherals				Total Current	Min	Nominal	Max
12V1	17.8 A	10.5 A	17.8	10.5	21.7	10.0 A	3.0 A					91 A	50	55	60
12V2								18.0 A (P8, 9, 10, 11)				18 A	18	19	20
12V3								18a (P5, 6, 7)				18 A	18	19	20

Note:

+12V current to PCIe slots may be supplied from four different connectors. 12V1 on P2, 12V2 on P3, 12V3 on P1, and 12V3 on P12. P12 is reserved for board that needs 4 x GPU cards powered. P1 is the main 12V power for PCIe slot; but additional 12V power can be connected to P2 and/or P3. The motherboard MUST NOT short any of the 12V rails or connectors together.

2.4.2.6 Hard Drive 12V rail configuration options

The following table shows the hard drive configuration options using the defined power connectors. In some cases additional converter or 'Y' cables are needed.

Table 82. Hard Drive 12V rail configuration options

	P8	P9	P10	P11	P5	P6	P7
	1x4	1x4	1x4	1x4	1x5	1x5	1x4
	18						
3 x 2.5" 8xHDD BP	HDD1 8 x 2.5	HDD2 8 x 2.5	na	na	na	na	HDD3 8 x 2.5
2 x 3.5" 4xHDD BP	HDD1 4x3.5		HDD1 4x3.5		peripheral bay		

1 x 3.5" 8xHDD BP	HDD1 8x3.5		na	na	peripheral bay
8 x 3.5" fixed SATA	2xfixed	2xfixed	2xfixed	2xfixed	peripheral bay
8 x 3.5" fixed SAS	2xfixed	2xfixed	2xfixed	2xfixed	peripheral bay

2.4.2.7 DC/DC Converters Loading

The following table defines power and current ratings of three DC/DC converters located on the PDB, each powered from +12V rail. The 3 converters meet both static and dynamic voltage regulation requirements for the minimum and maximum loading conditions.

Table 83. DC/DC Converters Load Ratings

	+12VDC Input DC/DC Converters		
	+3.3V Converter	+5V Converter	-12V Converter
MAX Load	15A	15A	0.5A
MIN Static/Dynamic Load	0A	0A	0A
Max Output Power	3.3V x15A =49.5W	5V x15A =75W	12V x0.5A =6W

2.4.2.8 5VSB Loading

There is also one DC/DC converter that converts the 12V standby into 5V standby.

Table 84. 5VSB Loading

	12V stby/5V stby DC/DC Converters
MAX Load	5A
MIN Static/Dynamic Load	0.1
Max Output Power	5V x5A =25W

2.4.2.9 DC/DC Converters Voltage Regulation

The DC/DC converters' output voltages stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise specified in Table 88. The 3.3V and 5V outputs are measured at the remote sense point, all other voltages measured at the output harness connectors.

Table 85. Voltage Regulation Limits

Converter output	Tolerance	Min	Nom	Max	Units
+ 3.3VDC	-5%/+5%	+3.14	+3.30	+3.46	VDC
+ 5VDC	-5%/+5%	+4.75	+5.00	+5.25	VDC
- 12VDC	- 5%/+9%	-13.08	-12.00	-11.40	VDC
5Vstby	-5%/+5%	+4.75	+5.00	+5.25	VDC

2.4.2.10 DC/DC Converters Dynamic Loading

The output voltages remains within limits specified in table above for the step loading and capacitive loading specified in Table 103 below. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load shown in Table 83 and Table 84.

Table 86. Transient Load Requirements

Output	Max Δ Step Load Size	Max Load Slew Rate	Test capacitive Load
+ 3.3VDC	5A	0.25 A/μs	250 μF
+ 5VDC	5A	0.25 A/μs	400 μF
+5Vsb	0.5A	0.25A/μs	20 μF

2.4.2.11 DC/DC Converter Capacitive Loading

The DC/DC converters are stable and meet all requirements with the following capacitive loading ranges.

Min capacitive loading applies to static load only.

Table 87. Capacitive Loading Conditions

Converter output	Min	Max	Units
+3.3VDC	250	6800	μF
+5VDC	400	4700	μF
-12VDC	1	350	μF
5Vstby	20	350	μF

2.4.2.12 DC/DC Converters Closed Loop stability

Each DC/DC converter is unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in Section 2.5.2.11. A minimum of: **45 degrees phase margin** and -**10dB-gain margin** is required. The PDB provides proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

2.4.2.13 Common Mode Noise

The Common Mode noise on any output does not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz.

- The measurement shall be made across a 100Ω resistor between each of DC outputs, including ground, at the DC power connector and chassis ground (power subsystem enclosure).
- The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

2.4.2.14 Ripple/Noise

The maximum allowed ripple/noise output of each DC/DC Converter is defined in the table below. This is measured over a bandwidth of 0Hz to 20MHz at the PDB output connectors. A 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor are placed at the point of measurement.

Table 88. Ripple and Noise

+3.3V	+5V	-12V	+5VSB
50mVp-p	50mVp-p	120mVp-p	50mVp-p

The test set-up shall be as shown below.

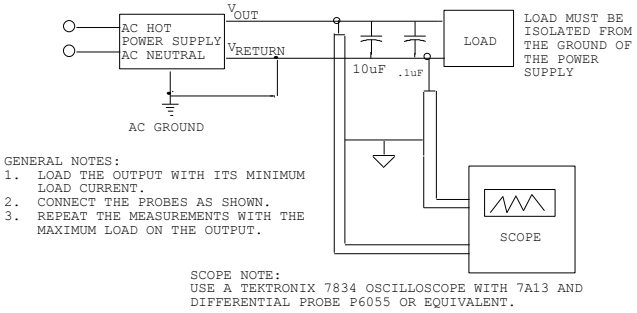


Figure 26. Differential Noise test setup

Note: When performing this test, the probe clips and capacitors should be located close to the load.

2.4.2.15 Timing Requirements

Below are timing requirements for the power on/off of the PDB DC/DC converters. The +3.3V, +5V and +12V output voltages should start to rise approximately at the same time. All outputs must rise monotonically.

Table 89. Output Voltage Timing

Description	Min	Max	Units
Output voltage rise time for each main output; 3.3V, 5V, and -12V.	5.0	70	msec
Output voltage rise time for the 5Vstby	1.0	25	msec
The main DC/DC converters (3.3V, 5V, -12V) shall be in regulation limits within this time after the 12V input has reached 11.4V.		50	msec
The main DC/DC converters (3.3V, 5V, -12V) must power off within this time after the 12V input has dropped below 11.4V.		100	msec
The 5Vstby converter shall be in regulation limits within this time after the 12Vstby has reach 11.4V.		10	msec
The 5Vstby converter must power off within this time after the 12Vstby input has dropped below 11.4V.		100	msec

2.4.2.16 Residual Voltage Immunity in Standby Mode

Each DC/DC converter is immune to any residual voltage placed on its respective output (typically a leakage voltage through the system from standby output) up to 500mV. This residual voltage does not have any adverse effect on each DC/DC converter, such as: no additional power dissipation or over-stressing/over-heating any internal components or adversely affecting the turn-on performance (no protection circuits tripping during turn on).

While in Stand-by mode, at no load condition, the residual voltage on each DC/DC converter output does not exceed 100mV.

2.4.3 Protection Circuits

The PDB shall shut down all the DC/DC converters on the PDB and the power supply (from PSON) if there is a fault condition on the PDB (OVP or OCP). If the PDB DC/DC converter latches off due to a protection circuit tripping, an AC cycle OFF for 15sec min or a PSON# cycle HIGH for 1sec shall be able to reset the power supply and the PDB.

2.4.3.1 Over-Current Protection (OCP)/240VA Protection

Each DC/DC converter output on PDB has individual OCP protection circuits. The PS+PDB combo shall shutdown and latch off after an over current condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the PDB harness connectors. The DC/DC converters shall not be damaged from repeated power cycling in this condition. Also, the +12V output from the power supply is divided on the PDB into 4 channels and +12V4 is limited to 240VA of power. There are current sensors and limit circuits to shut down the entire PS+PDB combo if the limit is exceeded. The limits are listed in below table. -12V and 5VSB is protected under over current or shorted conditions so that no damage can occur to the power supply. Auto-recovery feature is a requirement on 5VSB rail.

Table 90. PDB Over Current Protection Limits/240VA Protection

Output Voltage	Min OCP Trip Limits	Max OCP Trip Limits	Usage	Connectors
+3.3V	18A	240VA	PCIe, Misc	P1
+5V	18A	240VA	PCIe, HDD, Misc	P1, P5-11
+12V1	91A	100A	CPU1 + memory Fans, Misc	P2
+12V2	18A	20A	HDD and peripherals	P8, 9, 10, 11
+12V3	18A	20A	HDD and peripherals	P5, 6, 7

2.4.3.2 Over Voltage Protection (OVP)

Each DC/DC converter output on PDB have individual OVP protection circuits built in and it shall be locally sensed. The PS+PDB combo shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption.

Table 91 contains the over voltage limits. The values are measured at the PDB harness connectors. The voltage shall never exceed the maximum levels when measured at the power pins of the output harness connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the PDB connector.

Table 91. Over Voltage Protection (OVP) Limits

Output voltage	OVP min (v)	OVP max (v)
+3.3V	3.9	4.8
+5V	5.7	6.5
-12V	-13.3	-15.5
+5VSB	5.7	6.5

2.4.4 PWOK (Power OK) Signal

The PDB connects the PWOK signals from the power supply modules and the DC/DC converters to a common PWOK signal. This common PWOK signal connects to the PWOK pin on P1. The DC/DC convert PWOK signals have open collector outputs.

2.4.4.1 System PWOK requirements

The system will connect the PWOK signal to 3.3V or 5V from a pull-up resistor. The maximum sink current of the power supplies are 0.5mA. The minimum resistance of the pull-up resistor is stated below depending upon the motherboard's pull-up voltage. Refer to the *CRPS Power Supply Specification* for signal details.

Table 92. System PWOK Requirements

Motherboard pull-up voltage	MIN resistance value (ohms)
5V	10K
3.3V	6.8K

2.4.5 PSON Signal

The PDB connects the power supplies PSON signals together and connect them to the PSON signal on P1.
Refer to the *CRPS Power Supply Specification* for signal details.

2.4.6 PMBus*

The PDB has no components on it to support PMBus*. It only needs to connect the power supply PMBus* signals (clock, data, SMBAlert#) and pass them to the 1x5 signal connector.

2.4.6.1 Addressing

The PDB address the power supply as follows on the PDB.
0 = open, 1 = grounded

Table 93. PDB addressing

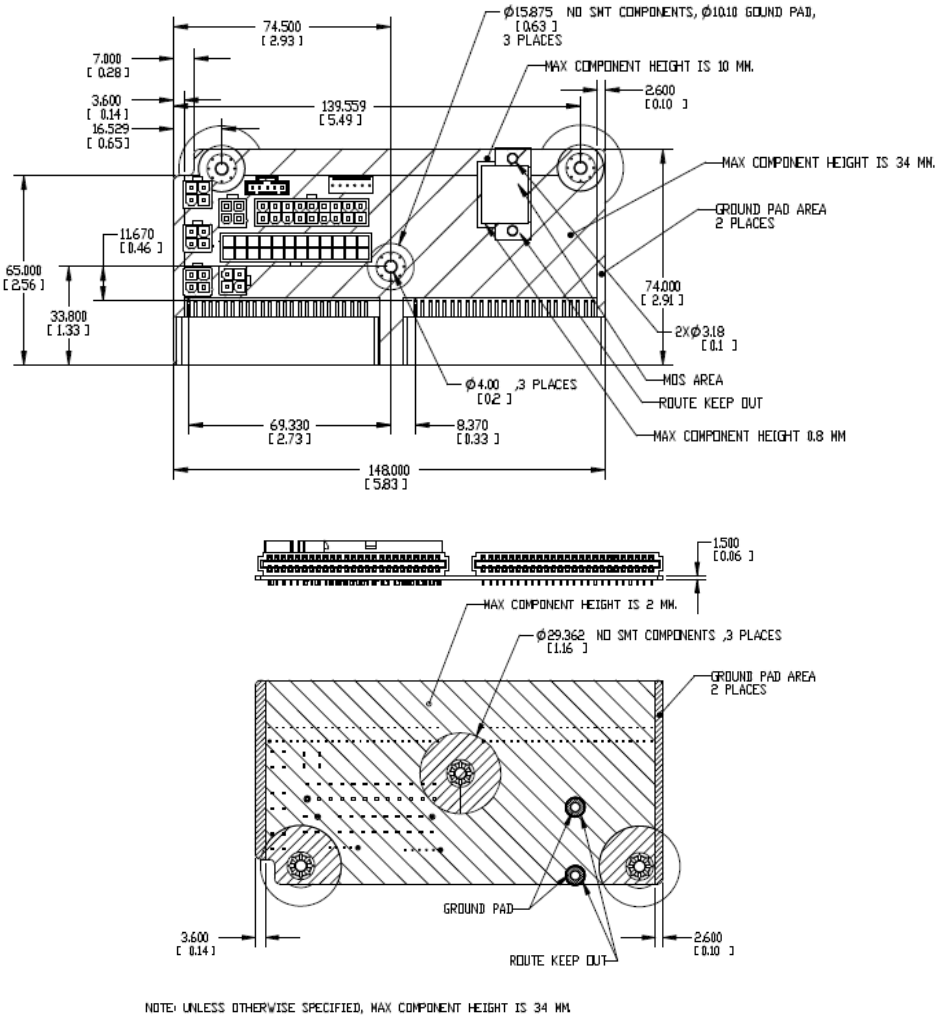
	Power Supply Position 1	Power Supply Position 2
PDB addressing Address0/Address1	0/0	0/1
Power supply PMBus* device address	B0h	B2h

2.5 Higer Current Power Common Redundant Power Distribution Board (PDB)

The Power Distribution Board (PDB) for Intel® Server System P4308SC2MHGC supports the Common Redundant power supply in a 1+1 redundant configuration. The PDB is designed to plug directly to the output connector of the PS and it contains 3 DC/DC power converters to produce other required voltages: +3.3VDC, +5VDC and 5V standby along with additional over current protection circuit for the 12V rails.

This power distribution board is intended to be used in the Intel® Server System P4308SC2MHGC with 750W common redundant power supply.

2.5.1 Mechanical Overview



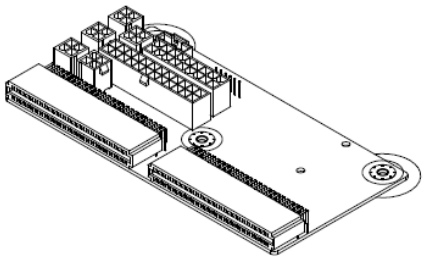


Figure 27. Outline Drawing

2.5.1.1 Airflow Requirements

The power distribution board shall get enough airflow for cooling DC/DC converters from the fans located in the Power Supply modules. Below is a basic drawing showing airflow direction. The amount of cooling airflow that will be available to the DC/DC converters is to be no less than 1.2M/s.

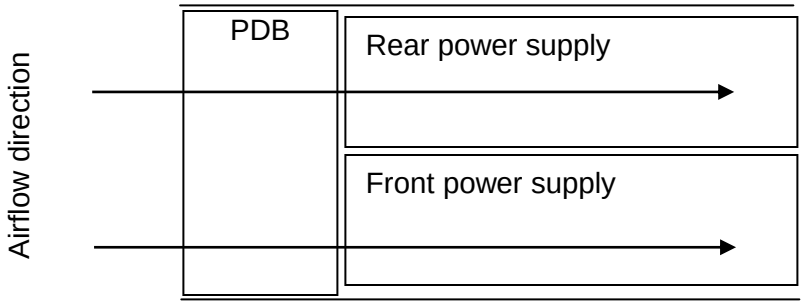


Figure 28. Airflow Diagram

2.5.1.2 DC/DC converter cooling

The dc/dc converters on the power distribution board are in series airflow path with the power supplies.

2.5.1.3 Temperature Requirements

The PDB operates within all specified limits over the Top temperature range. Some amount of airflow shall pass over the PDB.

Table 94. Thermal Requirements

Item	Description	Min	Max	Units
T_{op}	Operating temperature range.	0	50	°C
T_{non-op}	Non-operating temperature range.	-40	70	°C

2.5.1.4 Efficiency

Each DC/DC converter shall have a **minimum** efficiency of **85%** at 50% ~ 100% loads and over +12V line voltage range and over temperature and humidity range.

2.5.2 DC Output Specification

2.5.2.1 Input Connector (power distribution mating connector)

The power distribution provides two power pins, a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector (equivalent to 2x25 pin configuration of the FCI power card connector 10035388-102LF). The FCI power card edge connector is a new version of the PCE from FCI used to raise the card edge by 0.031" to allow for future 0.093" PCBs in the system. The card edge connector has no keying features; the keying method is accomplished by the system sheet metal.

Table 95. Input Connector and Pin Assignment Diagrams

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus* SDA	B19	A0 (SMBus* address)
A20	PMBus* SCL	B20	A1 (SMBus* address)
A21	PSON	B21	12V stby
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Return Sense	B23	12V load share
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	Compatibility Pin*

Note: *The compatibility Pin is used for soft compatibility check. The two compatibility pins are connected directly.

2.5.2.2 Output Wire Harness

The power distribution board has a wire harness output with the following connectors.

Listed or recognized component appliance wiring material (AVLV2), CN, rated min 85°C shall be used for all output wiring.

Table 96. PDB Cable Length

From	Length, mm	To connector #	No of pins	Description
Power Supply cover exit hole	470	P1	24	Baseboard Power Connector
Power Supply cover exit hole	320	P2	8	Processor 0 connector
Power Supply cover exit hole	450	P3	8	Processor 1 connector
Power Supply cover exit hole	800	P4	5	Power FRU/PMBus* connector
Power Supply cover exit hole	350	P5	5	SATA peripheral power connector for 5.25"
Extension from P5	100	P6	5	SATA peripheral power connector for 5.25"
Extension from P6	100	P7	4	Peripheral Power Connector for 5.25"/HSBP Power
Power Supply cover exit hole	400	P8	4	1x4 legacy HSBP Power Connector
Extension from P8	75	P9	4	1x4 legacy HSBP Power Connector
Power supply cover exit hole	500	P10	4	1x4 legacy HSBP Power/Fixed HDD adaptor Connection
Extension from P10	75	P11	4	1x4 legacy HSBP Power/Fixed HDD adaptor Connection
PCI power connector	800	P12	4	2x2 Legacy PCI Power Connector
Connector only (no cable)	na	P13	4	GFX card aux connectors
Connector only (no cable)	na	P14	4	
Connector only (no cable)	na	P15	4	
Connector only (no cable)	na	P16	4	

2.5.2.2.1 Baseboard power connector (P1)

- Connector housing: 24-Pin Molex* Mini-Fit Jr. 39-01-2245 or equivalent
- Contact: Molex* Mini-Fit, HCS Plus, Female, Crimp 44476 or equivalent

Table 97. P1 Baseboard Power Connector

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	+3.3VDC	Orange	13	+3.3VDC	Orange

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
	3.3V RS	Orange (24AWG)			
2	+3.3VDC	Orange	14	-12VDC	Blue
3	COM	Black	15	COM	Black
4	+5VDC	Red	16	PSON#	Green (24AWG)
5	COM	Black	17	COM	Black
6	+5VDC	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray (24AWG)	20	Reserved	N.C.
9	5 VSB	Purple	21	+5VDC	Red
10	+12V1	Yellow	22	+5VDC	Red
11	+12V1	Yellow	23	+5VDC	Red
12	+3.3VDC	Orange	24	COM	Black

2.5.2.2.2 Processor#0 Power Connector (P2)

- Connector housing: 8-Pin Molex* 39-01-2080 or equivalent
- Contact: Molex* Mini-Fit, HCS Plus, Female, Crimp 44476 or equivalent

Table 98. P0 Processor Power Connector

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5*	+12V1	Yellow
2	COM	Black	6	+12V1	Yellow
3	COM	Black	7	+12V1	Yellow
4	COM	Black	8	+12V1	Yellow

2.5.2.2.3 Processor#1 Power Connector (P3)

- Connector housing: 8-Pin Molex* 39-01-2080 or equivalent
- Contact: Molex* Mini-Fit, HCS Plus, Female, Crimp 44476 or equivalent

Table 99. P1 Processor Power Connector

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5	+12V1	Yellow
2	COM	Black	6	+12V1	Yellow
3	COM	Black	7	+12V1	Yellow
4	COM	Black	8	+12V1	Yellow

2.5.2.2.4 Power Signal Connector (P4)

- Connector housing: 5-pin Molex* 50-57-9405 or equivalent

- Contacts: Molex* 16-02-0087 or equivalent

Table 100. Power Signal Connector

Pin	Signal	24 AWG Color
1	I2C Clock	White
2	I2C Data	Yellow
3	SMBAlert#	Red
4	COM	Black
5	3.3RS	Orange

2.5.2.2.5 2x2 12V connector (P12-P16)

Connector header: Foxconn p/n HM3502E-P1 or equivalent

Table 101. P12 12V connectors

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5	+12V1	Yellow
2	COM	Black	6	+12V1	Yellow

Table 102. P13 - P16 12V connectors

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5	+12V2	Green
2	COM	Black	6	+12V2	Green

2.5.2.2.6 Legacy 1x4 Peripheral Power Connectors (P7, P8, P9, P10, P11)

- Connector housing: Molex* 0015-24-4048 or equivalent;
- Contact: Molex* 0002-08-1201 or equivalent

Table 103. P8, P9, P10, P11 Legacy Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+12V4	White
2	COM	Black
3	COM	Black
4	+5 VDC	Red

Table 104. P7Legacy Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+12V3	Brown
2	COM	Black
3	COM	Black
4	+5 VDC	Red

2.5.2.2.7 SATA 1x5 Peripheral Power Connectors (P5, P6)

- Connector housing: Molex* 0675-82-0000 or equivalent;
- Contact: Molex* 0675-81-0000 or equivalent

Table 105. SATA Peripheral Power Connectors

Pin	Signal	18 AWG Color
1	+3.3VDC	Orange
2	COM	Black
3	+5VDC	Red
4	COM	Black
5	+12V3	Yellow

2.5.2.3 Grounding

The ground of the pins of the PDB output connectors provides the power return path. The output connector ground pins is connected to safety ground (PDB enclosure). This grounding is well designed to ensure passing the max allowed Common Mode Noise levels.

2.5.2.4 Remote Sense

Below is listed the remote sense requirements and connection points for all the converters on the PDB and the main 12V output of the power supply.

Table 106. Remote Sense Connection Points

Converter	+ sense location	- sense location
Power supply main 12V	On PDB	On PDB
12V/3.3V	P20 (1x5 signal connector)	P20 (1x5 signal connector)
12V/5V	On PDB	On PDB
12V/-12V	none	none
12Vstby/5Vstby	none	none

Table 107. Remote Sense Requirements

Characteristic	Requirement
+3.3V remote sense input impedance	200Ω (measure from +3.3V on P1 2x12 connector to +3.3V sense on P20 1x5 signal connector)
+3.3V remote sense drop	200mV (remote sense must be able to regulate out 200mV drop on the +3.3V and return path; from the 2x12 connector to the remote sense points)
Max remote sense current draw	< 5mA

2.5.2.5 12V Rail Distribution

The following table shows the configuration of the 12V rails and what connectors and components in the system they are powering.

Table 108. 12V Rail Distribution

	P2		P3		P12	P1		P8	P9	P10	P11	P5,6,7	P13	P14	P15	P16	P17	P18	P19	P20				
	2x4		2x4		2x2	2x12		1x4	1x4	1x4	1x4	(2) 1x5, 1x4	GPU1		GPU2		GPU3		GPU4			OCP		
	CPU 1	Memory1	CPU2	Memory2	PCIe	Fans	Misc	HDD and peripherals					2x3	2x4	2x3	2x4	2x3	2x4	2x3	2x4	Total Current	Min	Nominal	Max
12V1	17.8 A	10.5 A	17.8 A	10.5 A	21.7 A	10.0 A	3.0 A														91 A	91	95.5	100
12V2													6.3 A	12.5 A	6.3 A	12.5 A	6.3 A	12.5 A	6.3 A	12.5 A	76 A	76	88	100
12V3												18.0 A									18 A	18	19	20
12V4								18.0A													18A	18	19	20

Note:

P12 is reserved for board that needs 4 x GPU cards powered. P1 is the main 12V power for PCIe slot; but additional 12V power can be connected to P2 and/or P3. The motherboard MUST NOT short any of the 12V rails or connectors together.

2.5.2.6 Hard Drive 12V rail configuration options

The following table shows the hard drive configuration options using the defined power connectors. In some cases additional converter or 'Y' cables are needed.

Table 109. Hard Drive 12V rail configuration options

	P8	P9	P10	P11	P5	P6	P7
	1x4	1x4	1x4	1x4	1x5	1x5	1x4
	18						
3 x 2.5" 8xHDD BP	HDD1 8 x 2.5	na	HDD2 8 x 2.5	na	na	na	HDD3 8 x 2.5
2 x 3.5" 4xHDD BP	HDD1 4x3.5		HDD1 4x3.5		peripheral bay		
1 x 3.5" 8xHDD BP	HDD1 8x3.5		na	na	peripheral bay		
8 x 3.5" fixed SATA	2xfixed	2xfixed	2xfixed	2xfixed	peripheral bay		
8 x 3.5" fixed SAS	2xfixed	2xfixed	2xfixed	2xfixed	peripheral bay		

2.5.2.7 DC/DC Converters Loading

The following table defines power and current ratings of three DC/DC converters located on the PDB, each powered from +12V rail. The 3 converters meet both static and dynamic voltage regulation requirements for the minimum and maximum loading conditions.

Table 110. DC/DC Converters Load Ratings

	+12VDC Input DC/DC Converters		
	+3.3V Converter	+5V Converter	-12V Converter
MAX Load	25A	15A	0.5A
MIN Static/Dynamic Load	0A	0A	0A
Max Output Power	3.3V x25A =82.5W	5V x15A =75W	12V x0.5A =6W

2.5.2.8 5VSB Loading

There is also one DC/DC converter that converts the 12V standby into 5V standby.

Table 111. 5VSB Loading

	12V stby/5V stby DC/DC Converters
MAX Load	8A
MIN Static/Dynamic Load	0.1
Max Output Power	5V x8A =40W

2.5.2.9 DC/DC Converters Voltage Regulation

The DC/DC converters' output voltages stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise specified in Table 95. The 3.3V and 5V outputs are measured at the remote sense point, all other voltages measured at the output harness connectors.

Table 112. Voltage Regulation Limits

Converter output	Tolerance	Min	Nom	Max	Units
+ 3.3VDC	-4%/+5%	+3.20	+3.30	+3.46	VDC
+ 5VDC	-4%/+5%	+4.80	+5.00	+5.25	VDC
5Vstby	-4%/+5%	+4.80	+5.00	+5.25	VDC

2.5.2.10 DC/DC Converters Dynamic Loading

The output voltages remains within limits specified in table above for the step loading and capacitive loading specified in Table 93 below. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load shown in Tables 93 and 94.

Table 113. Transient Load Requirements

Output	Max Δ Step Load Size	Max Load Slew Rate	Test capacitive Load
+ 3.3VDC	5A	0.25 A/μs	250 μF
+ 5VDC	5A	0.25 A/μs	400 μF
+5Vsb	0.5A	0.25A/μs	20 μF

2.5.2.11 DC/DC Converter Capacitive Loading

The DC/DC converters are stable and meet all requirements with the following capacitive loading ranges. Minimum capacitive loading applies to static load only.

Table 114. Capacitive Loading Conditions

Converter output	Min	Max	Units
+3.3VDC	250	6800	μF
+5VDC	400	4700	μF
5Vstby	20	350	μF

2.5.2.12 DC/DC Converters Closed Loop stability

Each DC/DC converter is unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in Section 2.4.2.11. A minimum of: **45 degrees phase margin** and -**10dB-gain margin** is required. The PDB provides proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

2.5.2.13 Common Mode Noise

The Common Mode noise on any output does not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz.

- The measurement shall be made across a 100Ω resistor between each of DC outputs, including ground, at the DC power connector and chassis ground (power subsystem enclosure).
- The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

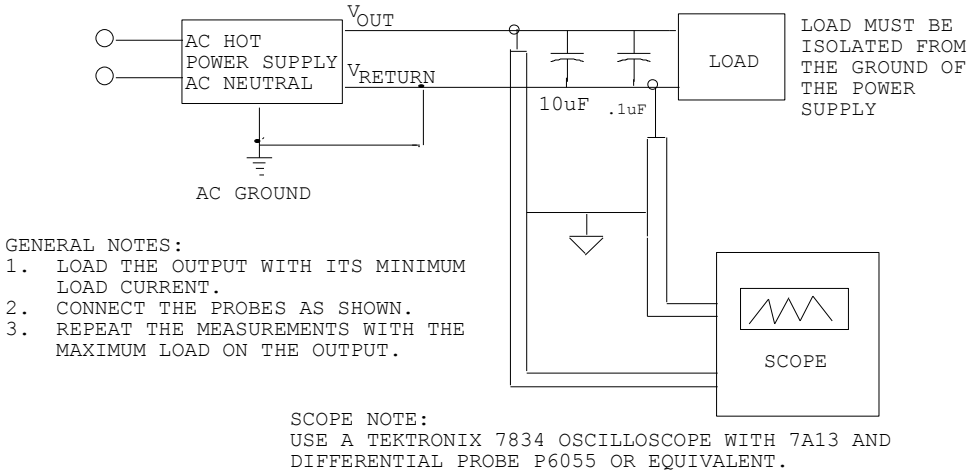
2.5.2.14 Ripple/Noise

The maximum allowed ripple/noise output of each DC/DC Converter is defined in below Table 95. This is measured over a bandwidth of 0Hz to 20MHz at the PDB output connectors. A 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor are placed at the point of measurement.

Table 115. Ripple and Noise

+3.3V	+5V	-12V	+5VSB
50mVp-p	50mVp-p	120mVp-p	50mVp-p

The test set-up shall be as shown below.



Note:

When performing this test, the probe clips and capacitors should be located close to the load.

Figure 29. Differential Noise test setup

2.5.2.15 Timing Requirements

Below are timing requirements for the power on/off of the PDB DC/DC converters. The +3.3V, +5V and +12V output voltages should start to rise approximately at the same time. All outputs must rise monotonically.

Table 116. Output Voltage Timing

Description	Min	Max	Units
Output voltage rise time for each main output; 3.3V, 5V, -12V and 5Vstby.	1.0	20	msec
The main DC/DC converters (3.3V, 5V, -12V) shall be in regulation limits within this time after the 12V input has reached 11.4V.		20	msec
The main DC/DC converters (3.3V, 5V, -12V) must drop below regulation limits within this time after the 12V input has dropped below 11.4V.		20	msec
The 5Vstby converter shall be in regulation limits within this time after the 12Vstby has reach 11.4V.		20	msec
The 5Vstby converter must power off within this time after the 12Vstby input has dropped below 11.4V.		100	msec

2.5.2.16 Residual Voltage Immunity in Standby Mode

Each DC/DC converter is immune to any residual voltage placed on its respective output (typically a leakage voltage through the system from standby output) up to 500mV. This residual voltage does not have any adverse effect on each DC/DC converter, such as: no additional power dissipation or over-stressing/over-heating any internal components or adversely affecting the turn-on performance (no protection circuits tripping during turn on).

While in Stand-by mode, at no load condition, the residual voltage on each DC/DC converter output does not exceed 100mV.

2.5.3 Protection Circuits

The PDB shall shut down all the DC/DC converters on the PDB and the power supply (from PSON) if there is a fault condition on the PDB (OVP or OCP). If the PDB DC/DC converter latches off due to a protection circuit tripping, an AC cycle OFF for 15sec min or a PSON# cycle HIGH for 1sec shall be able to reset the power supply and the PDB.

2.5.3.1 Over-Current Protection (OCP)/240VA Protection

Each DC/DC converter output on PDB has individual OCP protection circuits. The PS+PDB combo shall shutdown and latch off after an over current condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the PDB harness connectors. The DC/DC converters shall not be damaged from repeated power cycling in this condition. Also, the +12V output from the power supply is divided on the PDB into 3 channels and +12V3 is limited to 240VA of power. There are current sensors and limit circuits to shut down the entire PS+PDB combo if the limit is exceeded. The limits are listed in below table. -12V and 5VSB is protected under over current or shorted conditions so that no damage can occur to the power supply. Auto-recovery feature is a requirement on 5VSB rail.

Table 117. PDB Over Current Protection Limits/240VA Protection

Output Voltage	Min OCP Trip Limits	Max OCP Trip Limits	Usage
+3.3V	27A	Meet 240VA	PCIe, Misc
+5V	27A		PCIe, HDD, Misc
+12V1	91A	100A	CPU and memory
+12V2	76A	100A	GPU cards
+12V3	18A	20A	HDD and peripherals
+12V4	18A	20A	HDD and peripherals

2.5.3.2 Over Voltage Protection (OVP)

Each DC/DC converter output on PDB have individual OVP protection circuits built in and it shall be locally sensed. The PS+PDB combo shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. Table 135 contains the over voltage limits. The values are measured at the PDB harness connectors. The voltage shall never exceed the maximum levels when measured at the power pins of the output harness connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the PDB connector.

Table 118. Over Voltage Protection (OVP) Limits

Output voltage	OVP min (v)	OVP max (v)
+3.3V	3.9	4.8
+5V	5.7	6.5
+5VSB	5.7	6.5

2.5.4 PWOK (Power OK) Signal

The PDB connects the PWOK signals from the power supply modules and the DC/DC converters to a common PWOK signal. This common PWOK signal connects to the PWOK pin on P1. The DC/DC convert PWOK signals have open collector outputs.

2.5.4.1 System PWOK requirements

The system will connect the PWOK signal to 3.3V or 5V from a pull-up resistor. The maximum sink current of the power supplies are 0.5mA. The minimum resistance of the pull-up resistor is stated below depending upon the motherboard's pull-up voltage. Refer to the *CRPS Power Supply Specification* for signal details.

Table 119. System PWOK Requirements

Motherboard pull-up voltage	MIN resistance value (ohms)
5V	10K
3.3V	6.8K

2.5.5 PSON Signal

The PDB connects the power supplies PSON signals together and connect them to the PSON signal on P1.
Refer to the *CRPS Power Supply Specification* for signal details.

2.5.6 PMBus*

The PDB has no components on it to support PMBus*. It only needs to connect the power supply PMBus* signals (clock, data, SMBAlert#) and pass them to the 1x5 signal connector.

2.5.6.1 Addressing

The PDB address the power supply as follows on the PDB.
0 = open, 1 = grounded

Table 120. PDB addressing

	Power Supply Position 1	Power Supply Position 2
PDB addressing Address0/Address1	0/0	0/1
Power supply PMBus* device address	B0h	B2h

3. Thermal Management

The Intel® Server System P4000SC is designed to operate at external ambient temperatures of between 10ºC- 35ºC. Working with integrated platform management, several features within the system are designed to move air in a front to back direction, through the system and over critical components in order to prevent them from overheating and allow the system to operate with best performance.

3.1 Thermal Operation and Configuration Requirements

To keep the system operating within supported maximum thermal limits, the system must meet the following operating and configuration guidelines:

- Ambient in-let temperature cannot exceed 35º C and should not remain at this maximum level for long periods of time. Doing so may affect long term reliability of the system.
- All hard drive bays must be populated. Hard drive carriers either can be populated with a hard drive or supplied drive blank.
- The air duct must be installed at all times.
- In single power supply configurations, the second power supply bay must have the supplied filler blank installed at all times.
- The system top-cover must be installed at all times.

3.2 Thermal Management Overview

In order to maintain the necessary airflow within the system, all of the previously listed components and top cover need to be properly installed. For best system performance, the external ambient temperature must remain below 35ºC and all system fans should be operational.

In the event that system thermals should continue to increase with the system fans operating at their maximum speed, platform management may begin to throttle performance of either the memory subsystem or the processors or both, in order to keep components from overheating and keep the system operational. Throttling of these sub-systems will continue until system thermals are reduced.

Should system thermals increase to a point beyond the maximum thermal limit as pre-programmed in platform management for this system, the system will shut down, the System Status LED will change to a solid Amber state, and the event will be logged to the system event log.

3.3 System Fan Configuration

3.3.1 Cooling Solution for Intel® Server System P4304SC2SFEN and P4304SC2SHDR

Non-Redundant cooling solution is used in the Intel® Server System P4304SC2SFEN and P4304SC2SHDR.

Two 92 x 32 mm fans provide cooling for the processors, memory, hard drives and add-in cards. The two fans draw air through the rear of each hard drive bay to provide drive, processors, and memory cooling. All system fans provide a signal for RPM detection the server board can make available for server management functions. In addition, the power supply fan provides cooling for the power supply.
The default location of the two system fans is shown below:

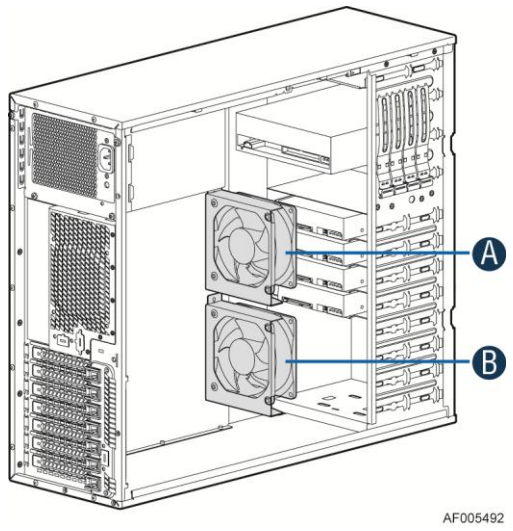


Figure 30. Chassis Fans default location in Intel® Server System P4304SC2SFEN and P4304SC2SHDR

To support full height full length PCI card, the PCI zone system fan in above figure can be reinstalled as shown below:

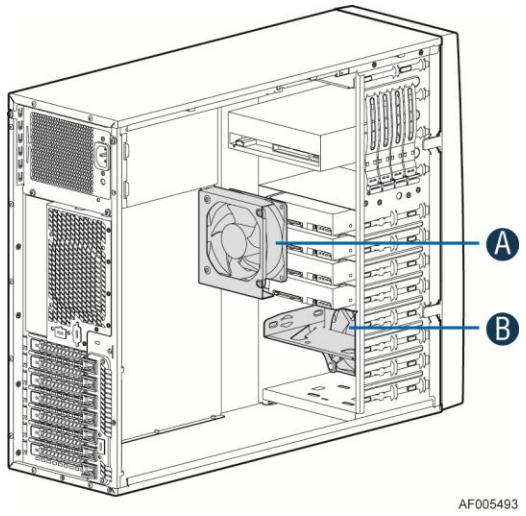


Figure 33. Chassis System Fans to support full length card in Intel® Server Chassis P4304SC2SFEN and P4304SC2SHDR

3.3.2 Redundant Cooling Solution

Redundant cooling solution is used in the Intel® Server System P4308SC2MHGC.

Five hot-swap 80x38mm fans provide cooling for the processors, hard drives, and add-in cards. When any single fan fails, the remaining fans increase in speed and maintain cooling until the failed unit is replaced. All system fans provide a signal for RPM detection that the server board can make available for server management functions.

In addition, the power supply fan provides cooling for the power supply.

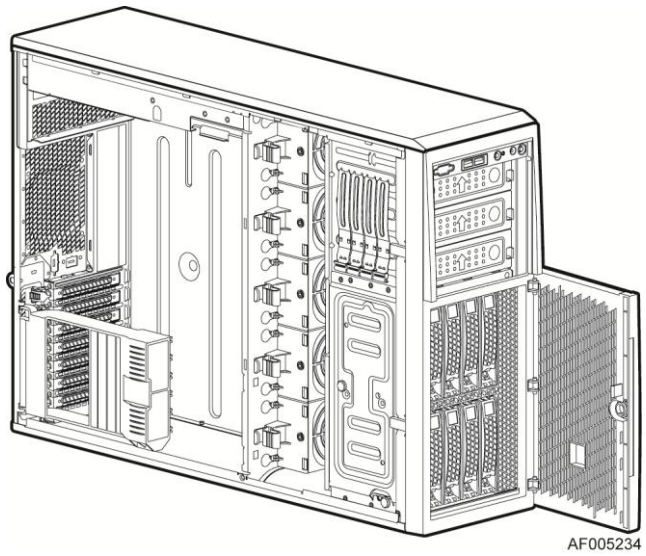


Figure 31. Hot-swap Fans in Intel® Server System P4308SC2MHGC

3.4 Fan Control

The fans provided in the Intel® Server Chassis P4000SC Family contains a tachometer signal that can be monitored by the server management subsystem of the Intel® Server Boards for RPM (Revolutions per Minute) detection.

The server board monitors several temperature sensors and adjusts the PWM (Pulse Width Modulated) signal to drive the fan at the appropriate speed.

The front panel of the chassis has a digital temperature sensor connected to the server board through the front panel's bus. The server board firmware adjusts the fan speed based on the front panel intake temperature and processor temperatures.

Refer to the baseboard documentation for additional details on how fan control is implementation.

3.5 Fan Header Connector Descriptions

All system fan headers support pulse width modulated (PWM) fans for cooling the processors in the chassis. PWM fans have an improved RPM range (20% to 100% rated fan speed) when compared to voltage controlled fans.

Fixed chassis fans are a 4-wire/4-pin style designed to plug into 4-pin or 6-pin SSI Fan headers. When plugged into a 6-pin header, only the first four signals are used (Pwr, Gnd, Tach, and PWM).

Hot-swap chassis fans are a 6-wire/6-pin style designed to plug into 6-pin headers. The extra signals provide for fan redundancy and failure indications (Pwr, Gnd, Tach, PWM, Presence, and Failure).

4. Storage and Peripheral Drive Bays

The Intel® Server System P4000SC product family has support for many storage device options, including:

- Fixed 3.5'' Hard Disk Drives
- Hot Swap 3.5'' Hard Disk Drives
- SAS Expender Option
- SATA Optical Drive
- eUSB Solid State Device (eUSB SSD)

Support for different storage and peripheral device options will vary depending on the system SKU. This section will provide an overview of each available option.

4.1 4x 3.5" Hot swap HDD support

The Intel® Server System P4304SC2SHDR supports 4x3.5" SAS/SATA backplane. The backplane provides the platform support for up to four hot-swap SAS or SATA hard drives.

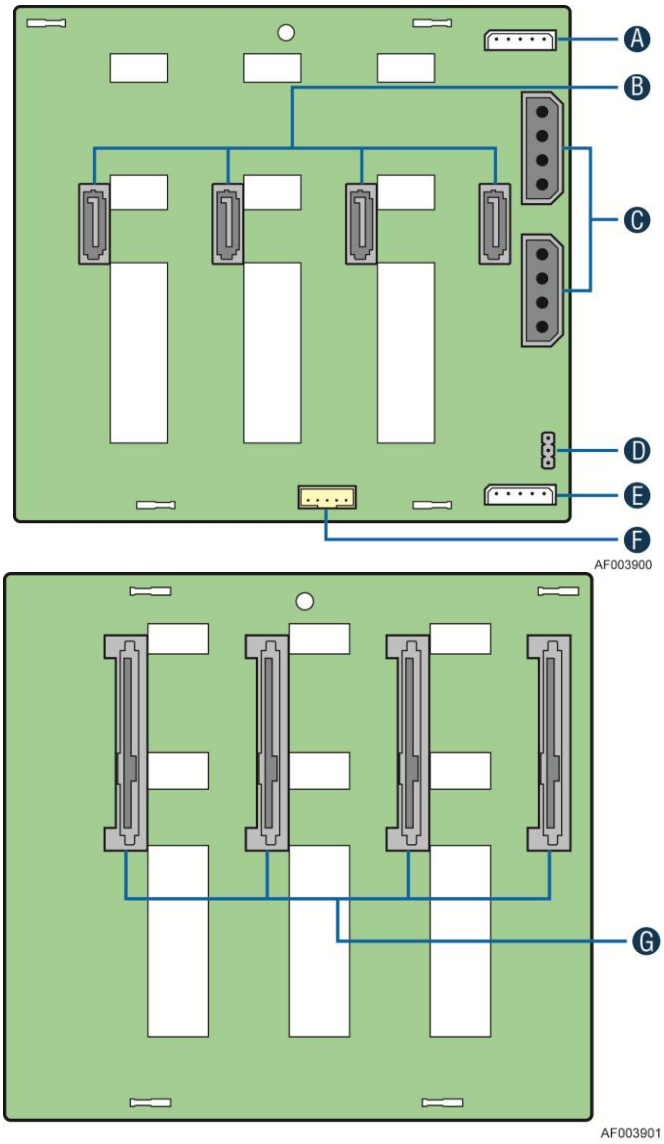
4.1.1 Key Features

The 4x3.5" HDD SAS/SATA HSBP supports the following feature set:

- 4x SAS/SATA 3.5'' hot swap hard drive at 6Gb SAS/SATA or slower speeds.
- One SGPIO SFF-8485 interface from a 5pin connector.
- One I2C interface from a 5pin connector for HDD status communication to BMC over slave SMB bus.
- Temperature sensor and FRU support.
- In-application FW updateable over I2C interfaces from the BMC. No special hardware needed for field FW upgrade with BMC onboard EPSD baseboard.
- 4 HDD status LEDs and 4 HDD activity LEDs.
- 4 HDD presence detect inputs to the microcontroller.
- 3.3V linear regulator for to power microcontroller and various other components.
- Four 7 pin shrouded latching THMT SAS/SATA input connectors.
- 29pin SAS/SATA 'hybrid' docking hotswap connectors.

4.1.2 Board Layout

The following figure shows the board layout and connectors placement of the 4HDD SAS/SATA hot-swap backplane.



A. A. I2C_In Connectors
B. B. SATA/SAS Cable Connectors
C. C. Power Connectors
D. D. SATA 6X Mode
E. E. I2C_Out Connectors
F. F. SGPIO connector
G. G. SATA/SAS Hot-swap Drive Connectors

Figure 32. 4x3.5" HSBP Board Layout

Note: Secondary side is mirrored.

4.1.3 4x3.5" HSBP Functional Description

4.1.3.1 4x3.5" HSBP Microcontroller

The microcontroller Cypress PSoC (CY8C22545-24AXI) is sized for 4x and 8x HSBP. It includes I2C interface hardware for in application updating of FW operational code from the I2C interface.

Following are the microcontroller signal names and pin numbers:

Table 121. 4x3.5" HSBP Microcontroller Pinouts

Pin	Pin Name	Signal Name
1	P2[5]	FM_HDD_PRSNT1
2	P2[3]	SGPIO_DATAOUT_0
3	P2[1]	SGPIO_DATAIN_0
4	Vdd	P3V3
5	P4[5]	TP_SATA_6X_MODE
6	P4[3]	LED_HDD_FAULT3_N
7	P4[1]	LED_HDD_FAULT1_N
8	Vss	GND
9	P3[7]	TP_SGPIO_DATAOUT_1
10	P3[5]	TP_SGPIO_DATAIN_1
11	P3[3]	TP_HDD_PRSNT_7
12	P3[1]	TP_HDD_PRSNT_5
13	P1[7]	SMB_P3V3_CLK
14	P1[5]	SMB_P3V3_DAT
15	P1[3]	TP_P1_3
16	P1[1]	SMB_ISSP_CLK
17	Vss	GND
18	P1[0]	SMB_ISSP_DAT
19	P1[2]	TP_P1_2
20	P1[4]	SMB_ADD0
21	P1[6]	SMB_ADD1
22	P3[0]	TP_HDD_PRSNT_4
23	P3[2]	TP_HDD_PRSNT_6
24	P3[4]	TP_SGPIO_CLK_1
25	P3[6]	TP_SGPIO_LOAD_1
26	XRES	FM_ISSP_XRES
27	P4[0]	LED_HDD_FAULT0_N
28	P4[2]	LED_HDD_FAULT2_N
29	P4[4]	TP_P4_4
30	Vss	GND
31	P2[0]	SGPIO_CLOCK_0
32	P2[2]	SGPIO_LOAD_0
33	P2[4]	FM_HDD_PRSNT0
34	P2[6]	FM_HDD_PRSNT2

Pin	Pin Name	Signal Name
35	P0[0]	Therm_P0
36	P0[2]	TP_THERM_N
37	P0[4]	TP_LED_HDD_FAULT4_N
38	P0[6]	TP_LED_HDD_FAULT6_N
39	Vdd	P3V3
40	P0[7]	TP_LED_HDD_FAULT7_N
41	P0[5]	TP_LED_HDD_FAULT5_N
42	P0[3]	TP_P0_3
43	P0[1]	TP_P0_1
44	P2[7]	FM_HDD_PRSNT3

4.1.3.2 SGPIO Functionality

The 4x 3.5" HSBP supports a SFF-8485 compliant SGPIO interface. It is used to activate the HDD status LED as well is monitored by the microcontroller for generating fault, identify, and rebuild registers that in turn are monitored by the baseboard BMC for generating corresponding SEL events.

SGPIO uses a 5pin header; this is to incorporate a ground conductor as an SI improvement over previous generation products and based on measurement data indicating add the ground is strongly recommended. The 5pin connector will be consistent with other HSBPs, in this way cable commonality is improved.

4.1.3.3 I2C Functionality

The microcontroller has a master/slave I2C connection to the baseboard BMC. The microcontroller is not an IPMB compliant device. The BMC will generate SEL events by monitoring registers on the HSBP microcontroller for drive presence, fault, and RAID rebuild in progress.

I2C uses a 5pin connector; this is to add two additional address bits. This connector is keyed differently than the 5pin SGPIO connector. The 4x3.5” HSBP architecture is setup to support up to 3 HSBPs even though the 4x 3.5" HSBP is currently only indented to support up to two of them in the Intel® Server Chassis P4000S, P4000M and P4000L family. Two pins on the I2C header are used to indicate HSBP address. Below is a figure on how the addressing is recommended for up to three HSBPs.

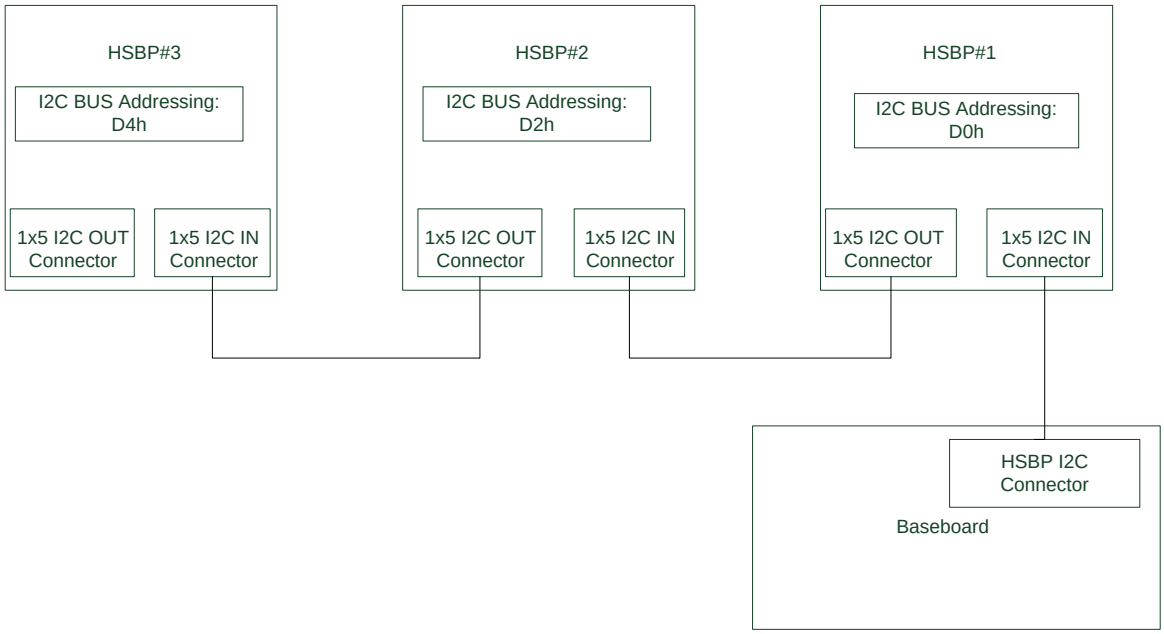


Figure 33. 4x 3.5" HSBP I2C Connectivity

4.1.3.4 SATA 6X Mode Jumper Functionality

The SATA 6X Mode jumper is used to enable baseboard AHCI SATA ports SGPIO function. Only when SATA 6X Mode jumper is enabled, and the SGPIO on backplane is connected to the SGPIO connector for the AHCI SATA ports on the baseboard, the AHCI SATA ports SGPIO function will be enabled. The following table is the SATA 6X Mode Jumper Block function:

Table 122. 4x3.5" HSBP SATA 6X Mode Host Jumper Block

Function	Pins	Operation
SATA 6X Mode	1-2	Enable SATA 6x Mode
	2-3	Disable SATA 6x Mode

4.1.3.5 HSBP LED Functionality

Below is a table for EPSD LED functionality for HSBP board.

Table 123. Romley LED Functionality

HDD	Green	Blink	HDD access or spin up/down (see note below)
	Amber	On	HDD fault
	Amber	Blink	RAID rebuild in progress (1Hz), identify (2Hz)
		Off	No access and no fault

The HSBP does not route HDD activity signal to the front panel so is not subject to the LED being continuously on when running SAS HDDs. Any HDD activity (really bus activity) driven

from SATA/SAS host on baseboard or HBA card hosts that cable HDD activity to baseboard 2pin header would still result in the FP LED blinking. Below is a table showing HDD activity LED differences between with SATA and SAS HDDs.

Table 124. HDD Activity LED Functionality

Condition	Drive Type	Behavior
Power On with no drive activity	SAS	Ready LED stays On.
	SATA	Ready LED stays Off.
Power On with drive activity	SAS	Ready LED blinks Off when processing a command.
	SATA	Ready LED blinks On when processing a command.
Power On and drive spun down	SAS	Ready LED stays Off.
	SATA	Ready LED stays Off.
Power On and drive spun down	SAS	Ready LED blinks*.
	SATA	Ready LED stays Off.

HSBP does not need to route HDD fault LED function to front panel fan board. This function is already lumped with system fault LED already on the FP.

4.1.4 4x3.5" HSBP Connector List and Pinouts

Below is a list of the connectors needed for this board.

Table 125. 4x3.5" HSBP Connector List

Function	Color	Qty
29Pin Hot Swap Docking Connector	Black	4
7Pin Input SAS/SATA Connector	Black	4
1x4Pin Power Connector	White	2
1x5Pin I2C Connector (In)	White	1
1x5Pin I2C Connector (Out)	Blue	1
1x5Pin SGPIO Connector	White	1

4.1.5 Pinouts

Table 126. 4x3.5" HSBP SGPIO Connector Pinouts

	Description
-	1x5pin SATA SGPIO
Pin	Signal Description
1	SGPIO_CLOCK_0
2	SGPIO_LOAD_0
3	GND
4	SGPIO_DATAOUT_0
5	SGPIO_DATAIN_0

Table 127. 4x3.5" HSBP I2C(In) Connector Pinouts

	Description
-	1x5Pin I2C Connector (In)
Pin	Signal Description
1	SMB_3V3SB_DAT
2	GND
3	SMB_3V3SB_CLK
4	SMB_ADD0
5	SMB_ADD1

Table 128. 4x3.5" HSBP I2C (Out) Connector List

	Description
-	1x5Pin I2C Connector (Out)
Pin	Signal Description
1	SMB_3V3SB_DAT
2	GND
3	SMB_3V3SB_CLK
4	SMB_ADD0
5	SMB_ADD1

Table 129. 4x3.5" HSBP Power Connector Pinouts

	Description
	1x4Pin Power Connector
Pin	Signal Description
1	P12V
2	GND
3	GND
4	P5V

Note: See SAS/SATA specs for pinout of 29pin and 7pin connectors.

4.1.6 4x3.5" HSBP Cabling Requirements

The 4x 3.5" HSBP requires the following cables:

1. Ganged 4x SATA/SAS data cable.
2. I2C cable - 5pin on HSBP side to 3pin on baseboard side
3. SGPIO cable - 5pin on HSBP side to 5pin on host controller side.

4.2 8x3.5" Hot Swap HDD support

The Intel® Server System P4308SC2MHGC support 8x3.5" drive configuration. The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 3.5" hard disk drive is mounted to a drive tray, allowing for hot swap extraction and insertion. Drive trays have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.

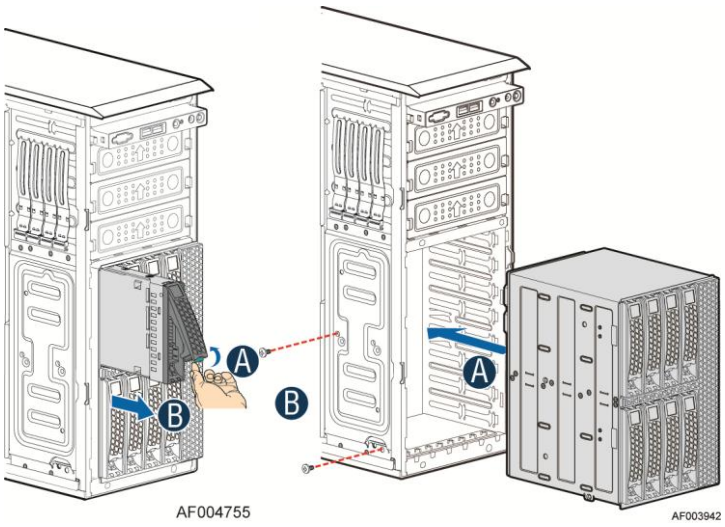


Figure 34. 3.5'' Hard Disk Drive Cage

Light pipes integrated into the drive tray assembly direct light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.

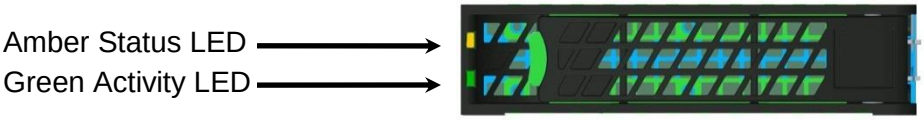


Figure 35. 3.5'' Hard Disk Drive Support - LED Status

Table 130. 3.5'' Hard Disk Drive Status LED States

Amber	Off	No access and no fault
	Solid On	Hard Drive Fault has occurred
	Blink	RAID rebuild in progress (1 Hz), Identify (2 Hz)

Table 131. 3.5'' Hard Disk Drive Activity LED States

	Condition	Drive Type	Behavior
Green	Power on with no drive activity	SAS	LED stays on
		SATA	LED stays off
	Power on with drive activity	SAS	LED blinks off when processing a command
		SATA	LED blinks on when processing a command
	Power on and drive spun down	SAS	LED stays off
		SATA	LED stays off
	Power on and drive spinning up	SAS	LED blinks
		SATA	LED stays off

4.2.1 3.5" Drive Hot-Swap Backplane Overview

4.2.1 Overview

The chassis supports 8x3.5" SAS/SATA backplane. The backplane provide the platform support for up to eight hot-swap SAS or SATA hard drives.

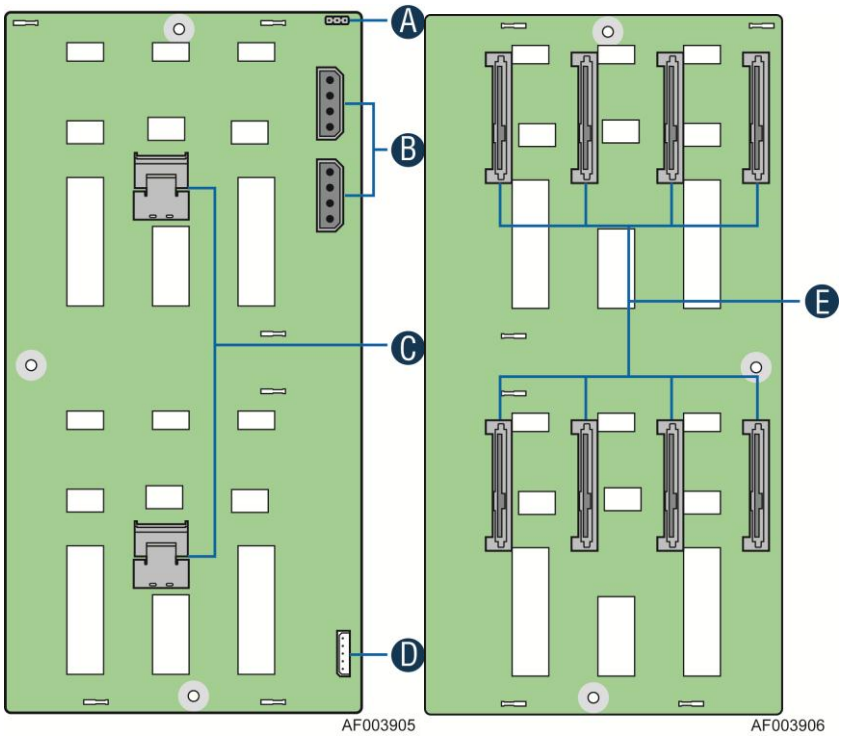
4.2.1.1 Key Features

The 8HDD 3.5" SAS/SATA HSBP supports the following feature set:

- 8x SAS/SATA 3.5'' hot swap hard drives.
- Two SGPIO SFF-8485 interfaces in sideband of mini-SAS connectors.
- One I2C interface from a 5pin connector for HDD status communication to BMC over slave SMB bus.
- Temperature sensor and FRU support
- In-application FW updateable over I2C interface from BMC. No special hardware needed for field FW upgrade with BMC onboard EPSD baseboard
- 8 HDD status LEDs and 8 HDD activity LEDs
- 8 HDD presence detect inputs to the microcontroller
- 3.3V linear regulator for to power microcontroller and various other components
- Two mini-SAS SAS/SATA input connectors
- Eight 29pin SAS/SATA 'hybrid' docking hot-swap connectors
- Mount board using one loose screw

4.2.1.2 Board Layout

The following figure shows the board layout and connectors placement of the 8HDD SAS/SATA hot-swap backplane.



A. A. SATA 6X Mode
B. B. Power Connectors
C. C. MINI_SAS Connectors
D. D. I2C Connector
E. E. SATA/SAS Hot-swap Drive Connectors
F.

Figure 36. 8x3.5" HSBP Board Layout

4.2.2 8x 3.5" HSBP Functional Description

4.2.2.1 8x3.5" HSBP Microcontroller

The microcontroller Cypress PSoC (CY8C22545-24AXI) is sized for 4x and 8x HSBP. It includes I2C interface hardware for in application updating of FW operational code from I2C interface. The following table displays the microcontroller signal names and pin numbers:

Table 132. 8x3.5" HSBP Microcontroller Pinouts

Pin	Pin Name	Signal Name
1	P2[5]	FM_HDD_PRSNT1
2	P2[3]	SGPIO_DATAOUT_0
3	P2[1]	SGPIO_DATAIN_0
4	Vdd	P3V3
5	P4[5]	TP_SATA_6X_MODE
6	P4[3]	LED_HDD_FAULT3_N

Pin	Pin Name	Signal Name
7	P4[1]	LED_HDD_FAULT1_N
8	Vss	GND
9	P3[7]	TP_SGPIO_DATAOUT_1
10	P3[5]	TP_SGPIO_DATAIN_1
11	P3[3]	TP_HDD_PRSNT_7
12	P3[1]	TP_HDD_PRSNT_5
13	P1[7]	SMB_P3V3_CLK
14	P1[5]	SMB_P3V3_DAT
15	P1[3]	TP_P1_3
16	P1[1]	SMB_ISSP_CLK
17	Vss	GND
18	P1[0]	SMB_ISSP_DAT
19	P1[2]	TP_P1_2
20	P1[4]	SMB_ADD0
21	P1[6]	SMB_ADD1
22	P3[0]	TP_HDD_PRSNT_4
23	P3[2]	TP_HDD_PRSNT_6
24	P3[4]	TP_SGPIO_CLK_1
25	P3[6]	TP_SGPIO_LOAD_1
26	XRES	FM_ISSP_XRES
27	P4[0]	LED_HDD_FAULT0_N
28	P4[2]	LED_HDD_FAULT2_N
29	P4[4]	TP_P4_4
30	Vss	GND
31	P2[0]	SGPIO_CLOCK_0
32	P2[2]	SGPIO_LOAD_0
33	P2[4]	FM_HDD_PRSNT0
34	P2[6]	FM_HDD_PRSNT2
35	P0[0]	Therm_P0
36	P0[2]	TP_THERM_N
37	P0[4]	TP_LED_HDD_FAULT4_N
38	P0[6]	TP_LED_HDD_FAULT6_N
39	Vdd	P3V3
40	P0[7]	TP_LED_HDD_FAULT7_N
41	P0[5]	TP_LED_HDD_FAULT5_N
42	P0[3]	TP_P0_3
43	P0[1]	TP_P0_1
44	P2[7]	FM_HDD_PRSNT3

4.2.2.2 SGPIO Functionality

The 8x 3.5" HSBP supports two SFF-8485 compliant SGPIO interfaces. The two SGPIO interfaces are included in sideband of mini-SAS connectors. They are used to activate the HDD status LED as well is monitored by the microcontroller for generating fault, identify, and rebuild

registers that in turn are monitored by the baseboard BMC for generating corresponding SEL events.

4.2.2.3 I2C Functionality

The microcontroller has a master/slave I2C connection to the baseboard BMC. The microcontroller is not an IPMB compliant device. The BMC will generate SEL events by monitoring registers on the HSBP microcontroller for drive presence, fault, and RAID rebuild in progress.

I2C uses a 5pin connector; this is to add two additional address bits. The 4U 8x 3.5" HSBP doesn't really need these extra two address bits, they should be hardwired. However 5pin will make it consistent with other HSBPs, in this way cable commonality is improved.

4.2.2.4 SATA 6X Mode Jumper Functionality

The SATA 6X Mode jumper is used for enable baseboard AHCI SATA ports SGPIO function. Only when SATA 6X Mode jumper is set enabled, and the SGPIO on backplane is connected to the SGPIO connector for the AHCI SATA ports on the baseboard, the AHCI SATA ports SGPIO function will be enabled.

The table below displays the SATA 6X Mode Jumper Block function:

Table 133. 8x3.5" HSBP SATA 6X Mode Host Jumper Block

Function	Pins	Operation
SATA 6X Mode	1-2	Enable SATA 6x Mode
	2-3	Disable SATA 6x Mode

4.2.2.5 HSBP LED Functionality

Below is a table for EPSD LED functionality for HSBP board.

Table 134. LED Functionality

HDD	Green	Blink	HDD access or spin up/down (see note below)
	Amber	On	HDD fault
	Amber	Blink	RAID rebuild in progress (1Hz), identify (2Hz)
		Off	No access and no fault

The HSBP does not route HDD activity signal to the front panel so is not subject to the LED being continuously on when running SAS HDDs. Any HDD activity (really bus activity) driven from SATA/SAS host on baseboard or HBA card hosts that cable HDD activity to baseboard 2pin header would still result in the FP LED blinking. Below is a table showing HDD activity LED differences between with SATA and SAS HDDs.

Table 135. BP HDD Activity LED Functionality

Condition	Drive Type	Behavior
Power on with no drive activity	SAS	Ready LED stays on
	SATA	Ready LED stays off
Power on with drive activity	SAS	Ready LED blinks off when processing a command
	SATA	Ready LED blinks on when processing a command
Power on and drive spun down	SAS	Ready LED stays off
	SATA	Ready LED stays off
Power on and drive spinning up	SAS	Ready LED blinks*
	SATA	Ready LED stays off

HSBP does not need to route HDD fault LED function to front panel fan board. This function is already lumped with system fault LED already on the FP.

4.2.3 8x3.5" HSBP Connector List and Pinouts

Below is a list of the connectors needed for this board.

Table 136. 8x3.5" HSBP Connector List and Pinouts

Function	Color	Qty
29Pin Hot Swap Docking Connector	Black	8
36Pin Input RA Mini-SAS Connector	Metal	2
1x4Pin Power Connector	Black	2
1x5Pin I2C Connector (In)	White	1
1x3 SATA 6X Host Jumper Header	Black	1

4.2.3.1 Pinouts

Table 137. 1x5 Pin I2C Connector (In)

	Description
-	1x5Pin I2C Connector (In)
Pin	Signal Name
1	SMB_3V3SB_DAT
2	GND
3	SMB_3V3SB_CLK
4	SMB_ADD0
5	SMB_ADD1

Table 138.1x4 Pin Power Connector

	Description
	1x4Pin Power Connector
Pin	Signal Name
1	P12V

	Description
2	GND
3	GND
4	P5V

Table 139. 36Pin Input RA Mini-SAS Connector

	Description	
	36Pin Input RA Mini-SAS Connector	
Pin	Signal Name	
A1	GND1	GND
A2	RX0_P	SAS_P0_TX_P
A3	RX0_N	SAS_P0_TX_N
A4	GND2	GND
A5	RX1_P	SAS_P1_TX_P
A6	RX1_N	SAS_P1_TX_N
A7	GND3	GND
A8	SIDEBAND7	SGPIO_CLOCK_0_R
A9	SIDEBAND3	SGPIO_LOAD_0_R
A10	SIDEBAND4	GND
A11	SIDEBAND5	TP_PORTA_SIDEBAND6
A12	GND4	GND
A13	RX2_P	SAS_P2_TX_P
A14	RX2_N	SAS_P2_TX_N
A15	GND5	GND
A16	RX3_P	SAS_P3_TX_P
A17	RX3_N	SAS_PE_TX_N
A18	GND6	GND
B1	GND7	GND
B2	TX0_P	SAS_P0_RX_P
B3	TX0_N	SAS_P0_RX_N
B4	GND8	GND
B5	TX1_P	SAS_P1_RX_P
B6	TX1_N	SAS_P1_RX_N
B7	GND9	GND
B8	SIDEBAND0	PD_PORTA_SIDEBAND7
B9	SIDEBAND1	TP_PORTA_B9
B10	SIDEBAND2	SGPIO_DATAOUT_0_R
B11	SIDEBAND6	SGPIO_DATAIN_0_R
B12	GND10	GND
B13	TX2_P	SAS_P2_RX_P
B14	TX2_N	SAS_P2_RX_N
B15	GND11	GND
B16	TX3_P	SAS_P3_RX_P
B17	TX3_N	SAS_P3_RX_N
B18	GND12	GND
MTH1	GND13	GND

	Description	
MTH2	GND14	GND
MTH3	GND15	GND
MTH4	GND16	GND
MTH5	GND17	GND
MTH6	GND18	GND

Table 140.1x3 SATA 6X Host Jumper

	Description
-	1x3 SATA 6X Host Jumper Header
Pin	Signal Name
1	P3V3
2	SATA_6X_MODE
3	TP_PIN3

4.2.4 8x3.5" HSBP Cabling Requirements

The 8x 3.5" HSBP requires the following cables:

1. Up to two Ganged Mini SAS to 4pcs 7Pin SATA cable with SGPIO Cable.
2. I2C cable - 5pin on HSBP side to 3pin on baseboard side.

4.3 SAS Expander Card Option

The 24-port SAS expander card and 36-port expander card is an optional accessory that can support up to 16 Hard drivers and 24 Hard drivers 2.5" hard disk drives. The expander card can be mounted directly behind the drive bay assembly as shown in the following illustration.

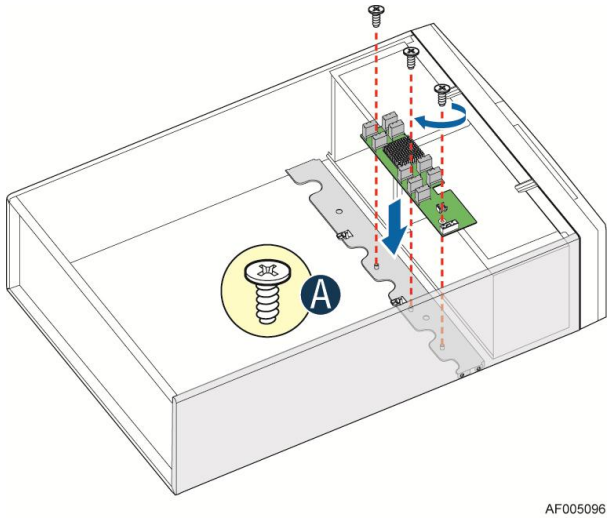


Figure 37. Internal SAS Expander Installation

The following diagrams are used to help identify the mini-SAS connectors found on the SAS expander cards. Care should be taken when connecting connectors from the SAS expander to the connectors on the backplane because each connector is pre-programmed at the factory to provide specific drive identification mapping. Improper connections may provide undesirable drive mappings.

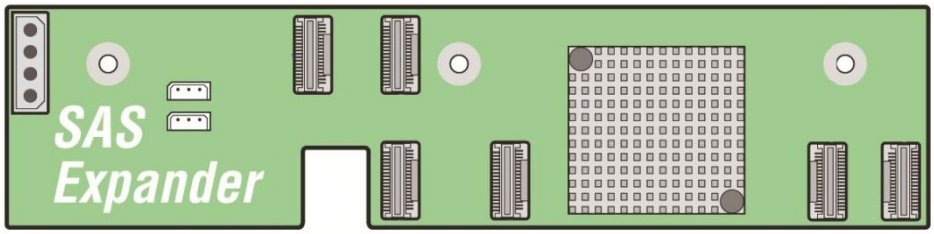


Figure 38. Internal 24-Port SAS Expander Card

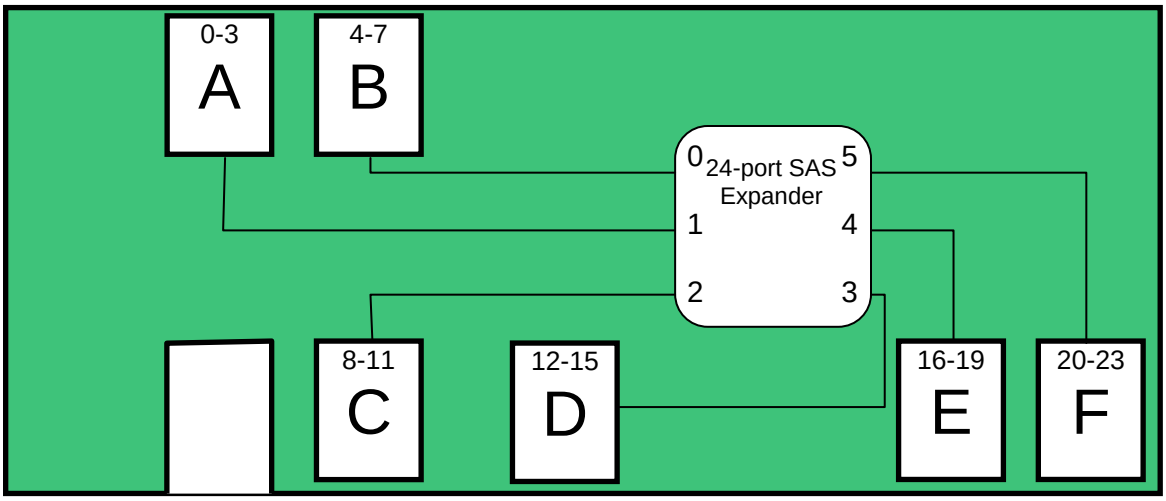


Figure 39. 24-Port Expander SAS Connector/Drive Identification Block Diagram

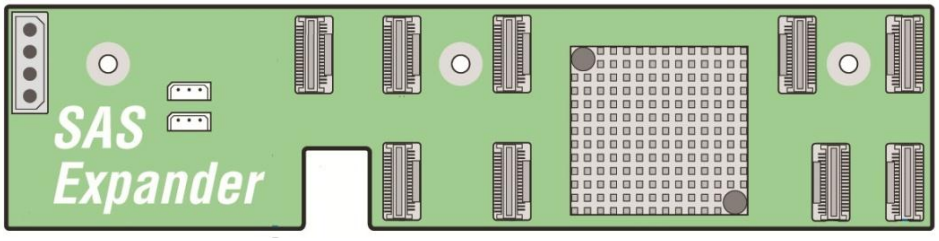


Figure 40. Internal 36-Port SAS Expander Card

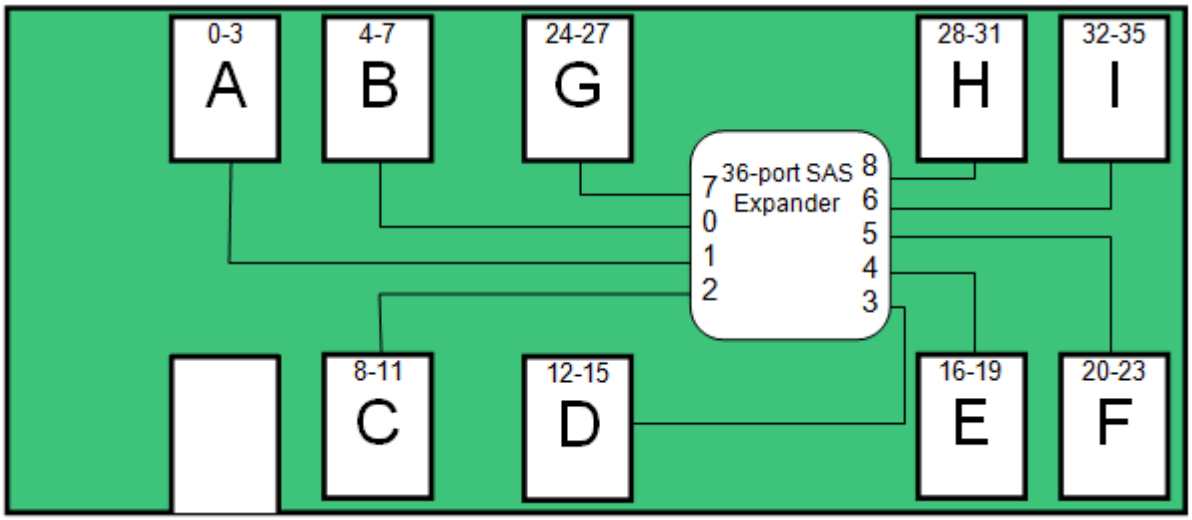


Figure 41. 36-Port Expander SAS Connector/Drive Identification Block Diagram

Each connector on the SAS expander card can be used as a “cable in” (SAS Controller to SAS Expander) or “cable out” (SAS Expander to Hot Swap Backplane) type connector. However, for contiguous drive mapping (0 – 16 or 0 – 24), cable routing differs when using a x8 wide-port capable 6 Gb SAS/SAS RAID Controller and using the embedded SCU ports.

Note: The 2.5” HDD support requires separate 16x 2.5 or 24x2.5 HDD drive cages.

4.3.1.1 Cable Routing using a x8 wide-port capable 6 Gb SAS/SAS RAID Controller

To ensure contiguous drive mapping when using x8 wide-port capable 6 Gb SAS/SAS RAID Controller with a SAS expander card, the system must be cabled as follows:

- Cables from the SAS Expander to the hot swap backplane must be connected in order: A – D for 16-drive configurations, and A – F for 24 drive configurations.
- The cables from the SAS controller can be attached to any of the remaining connectors on the SAS expander card.

4.3.1.2 Cable Routing using the embedded SCU ports

Note: The following may also be applied when using any 3 Gb SAS/SAS RAID Controller.

For storage configurations that utilize up to 16 or 24 hard disk drives for storage only and an internally mounted SSD as a boot device, the system must be configured as follows to ensure contiguous drive mapping (0 – 16 or 0-24):

- At least one internally mounted SSD device must be attached to the AHCI controller (SATA_0 or SATA_1 on the server board) and used as a boot device.
- Cables from the SAS Expander to the hot swap backplane must be connected in order**:** **B – E** for 16-drive configurations, and **B – G** for 24 drive configurations.

- The **SCU_0 or 3G SAS/SAS RAID (0-3**) connector is cabled to the first mini-SAS connector on the hot swap backplane
- The **SCU_1 or 3G SAS/SAS RAID (4-7)** connector is cable to **Connector A** on the SAS expander card.

For storage configurations that require utilizing a hard disk drive as the boot device, the system must be cabled as follows to ensure a boot device is found and for contiguous drive mapping (0-16 or 0-24).

- The **SCU_0 (0-3**) connector on the server board is cabled to the first mini-SAS connector on the hot swap backplane
- The **SCU_1 (4-7)** connector on the server board is cable to **Connector_A** on either the 24-port or 36-port SAS expander card.
- **Cables from the SAS Expander to the hot swap backplane must be connected in order**: B – F on the 24-port expander card, and B – G on the 36-port expander card.

Note: Current SCU controller design limitations prevent any hard drive attached to a SAS expander card from being a boot device when both SCU connectors are attached to the SAS expander card.

Please reference the *Intel® Server System P4000SC Product Family Service Guide* for cable routing diagrams illustrating a variety of different storage configurations.

4.3.2 Protocol Support

Each port on the expander cards support SAS devices, SATA II devices, or both using SSP, SMP, STP, and SATA II as follows:

- Serial SCSI Protocol (SSP) to enable communication with other SAS devices.
- SATA II Protocol to enable communication with other SATA II devices.
- Serial Management Protocol (SMP) to share topology management information with expanders.
- Serial Tunneling Protocol (STP) support for SATA II through expander interfaces.
- SAS protocol, described in the Serial Attached SCSI (SAS) Standard, version 2.0
- SFF-8485 protocol, using the Serial GPIO (SGPIO) interface provided by the expander.

4.3.3 SAS Expander Features

- Supports both Serial Attached SCSI and Serial ATA devices
- 6.0 Gbit/s, 3.0 Gbit/s, and 1.5 Gbit/s data transfer rate
- SFF-8087 mini-SAS connectors
- Output mini-SAS connectors support sideband SGPIO as per SFF-8485 specification
- Provides a low-latency connection to create and maintain transparent access to each connected SAS/SATA physical drive
- Staggered spin-up
- Hot Plug
- Native Command Queuing

- Allows multiple initiators to address a single target (in a fail-over configuration)

4.4 Optical Drive Support

The Intel® Server System P4000SC includes support three 5.25" optical drive bays. The optical drives can be installed to one of the three drive bays as illustrated below. The data cable from optical drive is recommended to connect to the white SATA 6G connectors on the server board.

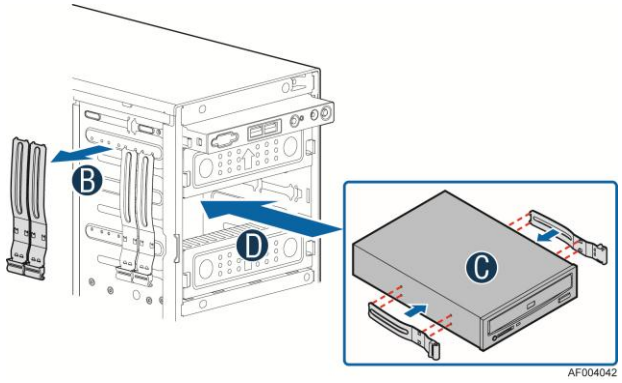


Figure 42. Optical Drive

4.5 Low Profile eUSB SSD Support

The system provides support for a low profile eUSB SSD storage device. A 2mm 2x5-pin connector labeled “eUSB SSD” near the rear I/O section of the server board is used to plug these small flash storage devices.

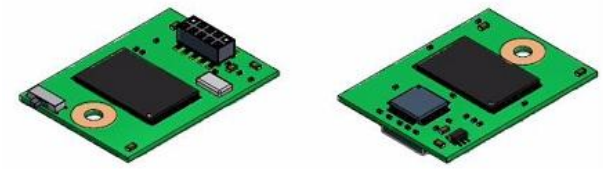


Figure 43. eUSB SSD Support

The eUSB features include:

- Two wire small form factor Universal Serial Bus 2.0 (Hi-Speed USB) interface to host.
- Read Speed up to 35 MB/s and write Speed up to 24 MB/s.
- Capacity range from 256GB to 32GB.
- Support USB Mass Storage Class requirements for Boot capability.

5. Reliability and Availability

5.1 Mean Time between Failure

The following is the calculated Mean Time Between Failures (MTBF) at maximum configuration at 40°C (ambient air). These values are derived using a historical failure rate and multiplied by factors for application, electrical and/or thermal stress and for device maturity. MTBF estimates should be viewed as “reference numbers” only.

- Telcordia SR_332 Issue II: Reliability Prediction Procedure
- Method 1: Parts Count Prediction
- Case III: Generic Value + Quality + Stress + Temperature
- Confidence Level: 90%
- Quality Level: II
- Temperature: Customer Specified (default 40°C)
- Duty Cycle: Continuous, 100%
- Operating Environment: Ground Benign, Fixed, Controlled

Table 141. Calculated Mean Time Between Failure P4304SC2SFEN

Subassembly (Server in 40°C ambient air)	Intel® Server System P4304SC2SFEN	
	MTBF	FIT
	(Hours)	(Failures/10^9 hrs)
S2400SC Baseboard	168,035	5,951
Power Supply (550 W Non Redundant)	474,910	2,106
Cooling fans (Non-redundant)	196,687	5,084
Backplane board -4x3.5”	NA	NA
Front Panel board	8,272,282	121
Totals with motherboard=	136700	7,311
Totals with motherboard	75400	13,262

Table 142. Calculated Mean Time Between Failure P4304SC2SHDR

Subassembly (Server in 40°C ambient air)	Intel® Server Chassis P4304XXSFDR	
	MTBF	FIT
	(Hours)	(Failures/10^9 hrs)
S2400SC Baseboard	168,035	5,951
Power Supply (Two 460 W Redundant)	1,186,122	843
Low Current PDB Board	1,726,969	579
Cooling fans (Non-redundant)	196,687	5,084
Backplane board -4x3.5”	NA	NA

Subassembly (Server in 40°C ambient air)	Intel® Server Chassis P4304XXSFDR	
	MTBF	FIT
	(Hours)	(Failures/10^9 hrs)
Front Panel board	8,272,282	121
Totals with motherboard=	150800	6,627
Totals with motherboard	79500	12,578

Table 143. Calculated Mean Time Between Failure P4308SC2MHGC

Subassembly (Server in 40°C ambient air)	Intel® Server Chassis P4308SC2MHGC	
	MTBF	FIT
	(Hours)	(Failures/10^9 hrs)
S2400SC Baseboard	168,035	5,951
Power Supply (Two 750 W)	806,373	1,240
High Current PDB	1,726,969	579
Redundant Cooling Fan (x5)	108,708	9,199
8x3.5" HSBP	712,161	1,404
Front Panel board	8,272,282	121
RMM4	10,960,687	91
Totals withoutmotherboard=	79,100	12,634
Totals with motherboard =	53,800	18,586

6. Environmental Limits

6.1 System Environment Limits

The following table defines the Intel® Server System P4000SC system level operating and non-operating environmental limits. Operation of the Intel® Server System P4000SC at conditions beyond those shown in the following table may cause permanent damage to the system. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 144. System Environment Limits Summary

Parameter		Limits
Temperature		
	Operating	10º C to 35º C [1] (50ºF to 95ºF) with the maximum rate of change not to exceed 10°C per hour
	Non-Operating	-40º C to 70º C (-40ºF to 158ºF)
Humidity		
	Non-Operating	50% to 90%, non-condensing with a maximum wet bulb of 28° C (at temperatures from 25°C to 35°C)
Shock		
	Operating	Half sine, 2g , 11 mSec
	Unpackaged	Trapezoidal, 25g , velocity change is based on packaged weight
	Packaged	Product Weight: ≥ 40 to < 80 Non-palletized Free Fall Height = 18 inches Palletized (single product) Free Fall Height = NA
Vibration		
	Unpackaged	5 Hz to 500 Hz 2.20 g RMS random
	Packaged	5 Hz to 500 Hz 1.09 g RMS random
AC-DC		
	Voltage	90 Hz to 132 V and 180 V to 264 V
	Frequency	47 Hz to 63 Hz
	Source Interrupt	No loss of data for power line drop-out of 12 mSec
	Surge Non-operating and operating	Unidirectional
	Line to earth Only	AC Leads 2.0 kV I/O Leads 1.0 kV DC Leads 0.5 kV
ESD		
	Air Discharged	12.0 kV
	Contact Discharge	8.0 kV
Acoustics Sound Power Measured		
	Power in Watts	<300 W ≥300 W ≥600 W ≥1000 W
	Servers/Rack Mount BA	7.0 7.0 7.0 7.0

Note:

1. Intel Corporation server boards contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel® server building blocks are used together, the fully integrated system will

meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel® developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

Disclaimer Note: Intel® ensures the unpackaged server board and system meet the shock requirement mentioned above through its own chassis development and system configuration. It is the responsibility of the system integrator to determine the proper shock level of the board and system if the system integrator chooses different system configuration or different chassis. Intel Corporation cannot be held responsible, if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

6.2 System Environmental Testing

The system will be tested per the *Environmental Standards Handbook*, Intel Doc 25-GS0009. These tests shall include:

- Acoustic Sound Power
- Temperature operating and non-operating
- Humidity non-operating
- Shock Operating, Shock Packaged and Shock unpackaged
- Vibration Packaged and Vibration Unpackaged
- AC, DC, and I/O Surge
- AC voltage, frequency, and source interrupt
- Conducted Immunity
- DC Voltage and Source Interrupt
- Electrical Fast Transient (EFT)
- Electrostatic discharge (ESD)
- Flicker and Voltage Fluctuation
- Power Frequency Magnetic Fields
- Power Line Harmonics
- Radiated Emissions
- Radiated Immunity
- Telecom Power Line Conducted Emissions
- Voltage Dip and Dropout
- Reliability Test

Appendix A: Integration and Usage Tips

This appendix provides a list of useful information that is unique to the Intel® Server Chassis P4000 family and should be kept in mind while integrating and configuring your server.

The Intel® Local Control Panel can only be used with systems configured with an Intel® Management Module.

Make sure the latest system software is loaded on the server. This includes system BIOS, FRU/SDR, BMC firmware, and hot-swap controller firmware. The latest system software can be downloaded from http://www.intel.com/support/motherboards/server/.

Glossary

Word/Acronym	Definition
ACA	Australian Communication Authority
ANSI	American National Standards Institute
ATA	Advanced Technology Attachment
ATX	Advanced Technology Extended
Auto-Ranging	Power supply that automatically senses and adjust itself to the proper input voltage range (110 VAC or 220 VAC). No manual switches or manual adjustments are needed.
BMC	Baseboard Management Controller
CFM	Cubic Feet per Minute (airflow)
CMOS	Complementary Metal Oxide Silicon
Dropout	A condition that allows the line voltage input to the power supply to drop to below the minimum operating voltage.
EEB	Entry-level Electronics Bay
EM	Expander Management
EMC	Electromagnetic compatibility
EMI	Electromagnetic Interference
EMP	Emergency Management Port
ESD	Electrostatic Discharge
FIT	Failures In Time
FP	Front Panel
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
GPIO	General Purpose Input and Output
HSBP	Hot-swap Backplane
I/O	Input/Output
I2C	Inter-Integrated Circuit
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
Latch Off	A power supply, after detecting a fault condition, shuts itself off. Even if the fault condition disappears, the supply does not restart unless manual or electronic intervention occurs. Manual intervention commonly includes briefly removing and then reconnecting the supply, or using a switch. Electronic intervention can be completed by electronic signals in the Server System.
LCD	Liquid Crystal Display
LCP	Local Control Panel
LPC	Low-Pin Count
LQFP	Lower Profile Quad Flat Pack
Monotonically	A waveform changes from one level to another in a steady fashion, without intermediate retrenchment or oscillation.
MTBF	Mean Time Between Failure
MTTR	Mean Time to Repair
Noise	The periodic or random signals over frequency band of 10 Hz to 20 MHz.

Word/Acronym	Definition
OCP	Over Current Protection
OTP	Over Temperature Protection
Over-current	A condition in which a supply attempts to provide more output current than the amount for which it is rated. This commonly occurs if there is a 'short circuit' condition in the load attached to the supply.
OVP	Over Voltage Protection
PDB	Power Distribution Board
PFC	Power Factor Correction
PMBus*	Power Management Bus
PSU	Power Supply Unit
PWM	Pulse Width Modulate
ppm	Parts per million
PWOK	A typical logic level output signal provided by the supply that signals the Server System that all DC output voltages are within their specified range.
RI	Ring Indicate
Ripple	The periodic or random signals over frequency band of 10 Hz to 20 MHz.
Rise Time	The time it takes any output voltage to rise from 10% to 95% of its nominal voltage.
Sag	The condition where the AC line voltage drops below the nominal voltage conditions.
SAS	Serial Attached SCSI
SATA	Serial ATA
SCA	Single Connector Attachment
SCSI	Small Computer System Interface
SDK	Software Development Kit
SDR	Sensor Data Record
SE	Single-Ended
SES	SCSI Enclosure Service
SGPIO	Serial General Purpose Input/Output
SMBUS*	System Management Bus
SSI	Server System Infrastructure
Surge	AC line voltage rises above nominal voltage
TACH	Tachometer
THD	Total Harmonic Distortion
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VCCI	Voluntary Control Council for Interference
VSB or Stand By	An output voltage that is present whenever AC power is applied to the AC inputs of the supply.

Reference Documents

See the following documents for additional information:

- *Intel® Server Board S2400SC Technical Product Specification*
- *Intel® Server System P4000SC Service Guide*
- *Intel® Server System P4000SC Quick Installation Guide*
- *BIOS for EPSD Platforms Based on Intel® Xeon Processor E5-4600/2600/2400/1600 Product Families External Product Specification*
- *EPSD Platforms Based On Intel Xeon® Processor E5 4600/2600/2400/1600 Product Families BMC Core Firmware External Product Specification*
- *Intel Integrated RAID Module RMS25PB080, RMS25PB040, RMS25CB080, and RMS25CB040 Hardware User's Guide*
- *Intel® Remote Management Module 4 Technical Product Specification*
- *Intel® Remote Management Module 4 and Integrated BMC Web Console User's Guide*