Intel® Server System R1000JP Family

Technical Product Specification

Intel order number: G71652-007

Revision 1.5

November, 2013

Enterprise Platforms and Services Division

Revision History

Date	Revision Number	Modifications
November, 2012	0.5	Initial release.
December, 2012	1.0	Updated assembly information of the optical drive.
May, 2013	1.1	Update pin-out table for Power Distribution Board
July, 2013	1.2	Update LED Indications table for 450W AC and 750W AC PSU
Sep, 2013	1.3	Add E5-2600 and E5-1600 V2 CPU support.
October, 2013	1.4	Remove the note “Note: Suggest you do not use the 2.5” hard drive in the 3.5” carrier” in 5.2
November, 2013	1.5	Update chassis air flow specification.

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1. Introduction

This *Technical Product Specification (TPS)* provides system specific information detailing the features, functionality, and high-level architecture of the Intel® Server System R1000JP family. You should also reference the *Intel® Server Board S1600JP Family Technical Product Specification* to obtain greater detail of functionality and architecture of the server board integrated in this server system.

In addition, you can obtain design-level information for specific sub-systems by ordering the *External Product Specifications (EPS)* or *External Design Specifications (EDS)* for a given sub-system. EPS and EDS documents are not publicly available. They are only made available under NDA with Intel® and must be ordered through your local Intel® representative. For a complete list of available documents, refer to the *Reference Documents* section at the end of this document.

The Intel® Server System R1000JP may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Refer to the *Intel® Server Board S1600JP/Intel® Server System R1000JP Specification Update* for published errata.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Product Overview
- Chapter 3 – Power Sub-System
- Chapter 4 – Thermal Management
- Chapter 5 – System Storage and Peripheral Options
- Chapter 6 – Storage Controller Options Overview
- Chapter 7 – Front Control Panel and I/O Panel Overview
- Chapter 8 – Intel® Local Control Panel
- Chapter 9 – PCI Riser Card Support
- Appendix A – Integration and Usage Tips
- Appendix B – POST Code LED Decoder
- Appendix C – POST Code Errors
- Glossary
- Reference Documents

1.2 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel® ensures through its own chassis development and testing that when Intel® server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel® developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board

does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Overview

This generation of Intel® 1U server platforms offers a variety of system options to meet the varied configuration requirements of high-density high-performance computing environments. The Intel® Server System R1000JP product family is comprised of several available 1U rack mount server systems that are all integrated with an Intel® Server Board S1600JP4.

This chapter provides a high-level overview of the system features. The following chapters provide greater detail for each major system component or feature.

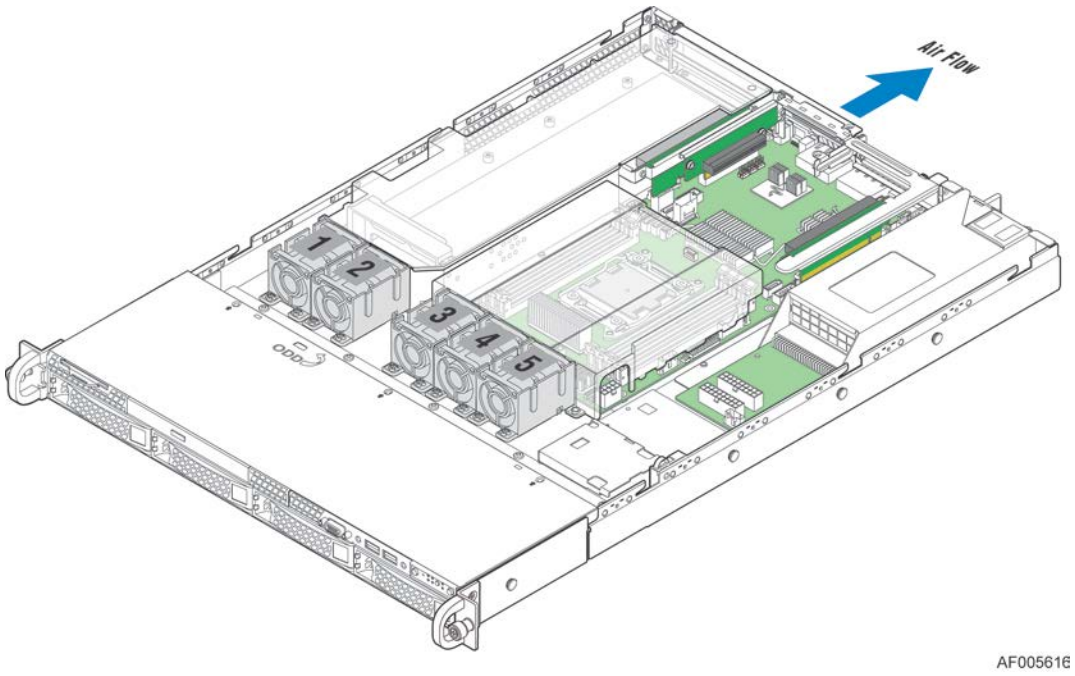


Figure 1. Product Drawing

Table 1. System Feature Set

Feature	Description
Processor	▪ Support for one Intel® Xeon® processor E5-2600 / E5-2600 V2 series with a Thermal Design Power (TDP) of up to 135W (Heatsink product code: FXXEA84X106HS, FXXCA84X106HS for Intel® Xeon® E5-2690/2643). ▪ Support for one Intel® Xeon® processor E5-1600 / E5-1600 V2 series with a Thermal Design Power (TDP) of up to 130W (Heatsink product code: FXXCA84X106HS). It can support to 25C and 900m. **Note:** The heatsink which the system integrates can only support 130W (Intel® Xeon® E5-2643 130W 4 core excluded) or below Intel® Xeon® Processor E5-2600 series.
Memory	▪ Maximum DIMM Capacity: 32GB DIMMs. ▪ Unbuffered DDRIII, Registered DDRIII, and Load Reduced DDRIII. ▪ Memory DDRIII data transfer rate of 1066/1333/1600MT/s. ▪ Four memory channels, Two DIMM slots per channel. ▪ DDR3 standard I/O voltage of 1.5V and DDR3 Low Voltage of 1.35V
Chipset	Intel® C600 Platform Controller Hub (PCH) with support for optional Storage Upgrade Key
System Connectors	External I/O connectors: ▪ DB-15 Video connectors

Feature	Description
/Headers	▪ Four RJ-45 Network Interface for 10/100/1000 LAN ▪ Two USB 2.0 connectors Internal connectors/headers: ▪ One Type A USB connector ▪ Two 2 x 5 USB connectors ▪ One 2 x 5 serial port connector ▪ One internal video connector for the front video ▪ Six SATA connectors ▪ One mini SAS connector
System Fan Support	Four fans for R1208JP4OC, R1304JP4OC, R1208JP4TC, and R1304JP4TC. Five fans for R1208JP4GS, R1304JP4GS.
Add-in Adapter Support	R1304JP4OC/R1208JP4OC and R1304JP4TC/R1208JP4TC: ▪ Riser slot 1 supports PCIe Gen III x16 Riser with LP PCIe add-in card. ▪ Riser slot 2 supports PCIe Gen III x 8 Riser (for Intel® rIOM and RMM4 NIC port). This riser and the carrier board are not integrated in the system. Please refer to the product order code A1UJPRMM4IOM. ▪ Riser slot 3 supports two slots Riser (PCIe Gen III x16 + x8) with full length and full height PCIe add-in card. R1304JP4GS and R1208JP4GS: ▪ Riser slot 1 supports PCIe Gen III x16 Riser with LP PCIe add-in card. ▪ Riser slot 2 supports PCIe Gen III x 8 Riser (for Intel® rIOM and RMM4 NIC port). This riser and the carrier board are not integrated in the system. Please refer to the product order code A1UJPRMM4IOM. ▪ Riser slot 3 supports PCIe Gen III x16 Riser with full length and full height, double width PCIe add-in card. **Notes:** 1. The system can support third-party double width card with TDP up to 225W for Passive Card and 300W for Active Card for A2 Class. 2. The system can support Intel® MIC Card with TDP up to 245W for Passive Card for A2 Class. 3. Inlet ambient temperature needs derating to 25°C and 900m Altitude if Intel® MIC Card with TDP higher than 245W is installed. 4. The system cannot support Active Intel® MIC Card.
On-board Video	On-board Emulex* LLC Pilot III Controller ▪ Integrated 2D Video Controller ▪ 128 MB DDR2 Memory
Hard Disk Drive Supported	4x 3.5-inch SATA/SAS HDD bays (SKU: R1304JP) 8x 2.5-inch SATA/SAS HDD bays (SKU: R1208JP)
RAID Support	▪ Intel® RSTe SW RAID 0/1/10/5 for SATA mode ▪ LSI* SW RAID 0/1/10/5
LAN	▪ Four Gigabit Ethernet device i350 connectors
System Power	450W AC (SKU: R1304JP4OC, R1208JP4OC) 450W DC (SKU: R1304JP4TC, R1208JP4TC) 750W AC (SKU: R1304JP4GS, R1208JP4GS)
Server Management	▪ Onboard Emulex* LLC Pilot III* Controller ▪ Support for Intel® Remote Management Module 4 Lite solutions ▪ Intel® Light-Guided Diagnostics on field replaceable units ▪ Support for Intel® System Management Software ▪ Support for Intel® Intelligent Power Node Manager (Need PMBus*-compliant power supply)

Table 2. System SKU matrix

Board SKU vs Chassis	450W AC	450W DC	750W AC
3.5" HDD	R1304JP4OC	R1304JP4TC	R1304JP4GS
2.5" HDD	R1208JP4OC	R1208JP4TC	R1208JP4GS

The Intel® Server System R1000JP family are supporting all Intel® Xeon® processor E5-2600 series with TDP 135W (8-core, 6-core), or 80W (4-core) and below. You can find a full list of supported processors at the Intel® Support website: https://serverconfigurator.intel.com/sct_private/sct_app.aspx.

Note: The processor with TDP 150W in Intel® Xeon® processor E5-2600 Series is not supported.

2.1 System Views

Figure 2. System Photo

2.2 System Dimensions

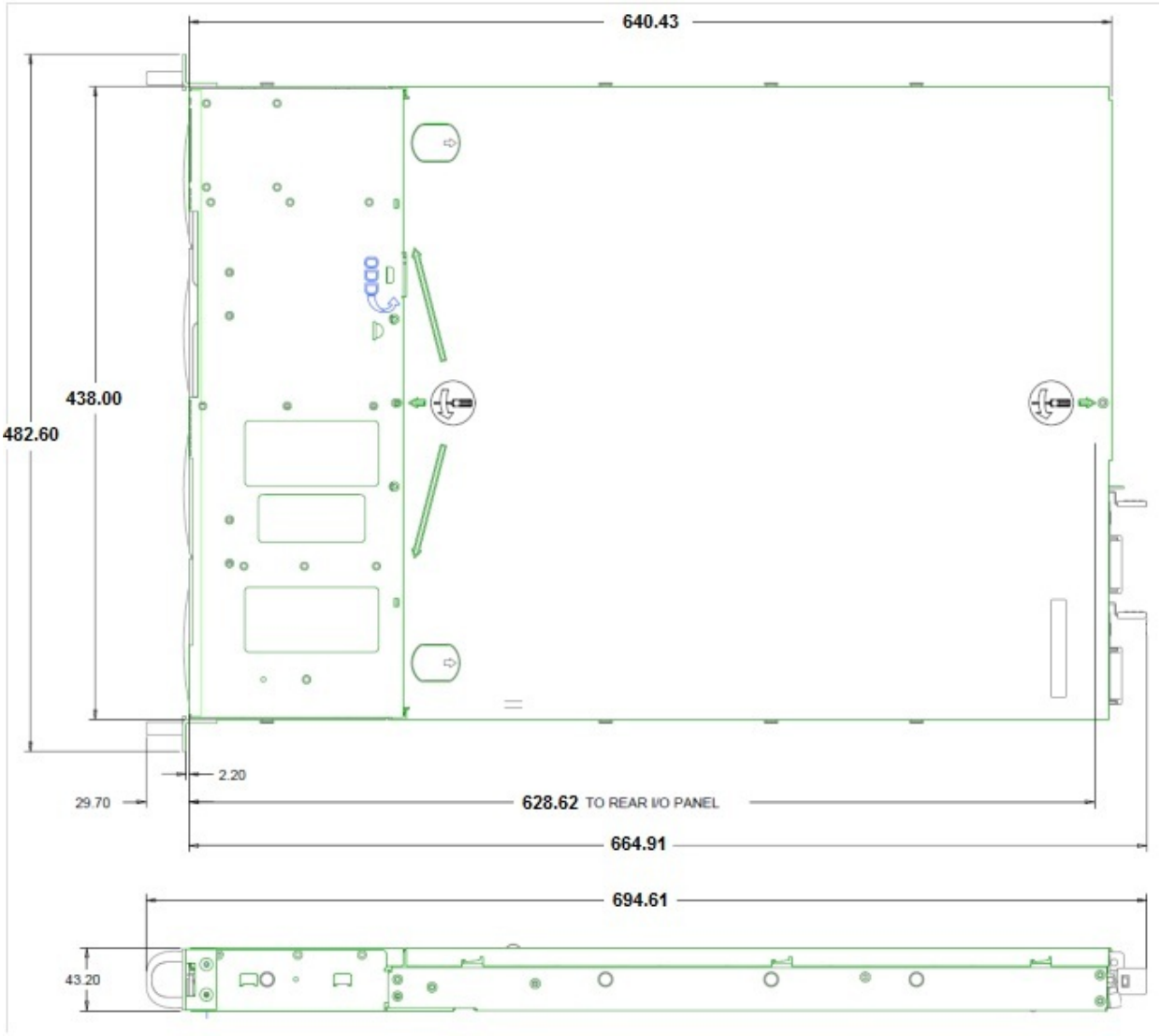


Figure 3. Chassis Dimension

2.3 System Level Environmental Limits

The following table defines the system level operating and non-operating environmental limits.

Table 3. System Environmental Limits Summary

Parameter		Limits
Temperature		
	Operating	ASHRAE Class A2 – Continuous Operation. 10ºC to 35ºC (50ºF to 95ºF) with the maximum rate of change not to exceed 10°C per hour.
	Shipping	-40ºC to 70ºC (-40ºF to 158ºF).
Altitude		
	Operating	Support operation up to 3050m with ASHRAE class deratings.

Parameter		Limits
Humidity		
	Shipping	50% to 90%, non-condensing with a maximum wet bulb of 28°C (at temperatures from 25°C to 35°C).
Shock		
	Operating	Half sine, 2g, 11 mSec.
	Unpackaged	Trapezoidal, 25 g, velocity change is based on packaged weight.
	Packaged	Product Weight: ≥ 40 to < 80. Non-palletized Free Fall Height = 18 inches. Palletized (single product) Free Fall Height = NA.
Vibration		
	Unpackaged	5 Hz to 500 Hz 2.20 g RMS random.
	Packaged	5 Hz to 500 Hz 1.09 g RMS random.
AC-DC		
	Voltage	90 V to 132 V and 180 V to 264 V.
	Frequency	47 Hz to 63 Hz.
	Source Interrupt	No loss of data for power line drop-out of 12 mSec.
	Surge Non-operating and operating	Unidirectional
	Line to earth Only	AC Leads 2.0 kV I/O Leads 1.0 kV DC Leads 0.5 kV
ESD		
	Air Discharged	12.0 kV
	Contact Discharge	8.0 kV
Acoustics Sound Power Measured		
Air Flow	Operation	11 to 80 CFM
	Power in Watts	<300 W ≥300 W ≥600 W ≥1000 W
	Servers/Rack Mount BA	7.0 7.0 7.0 7.0

Note:

See the *Intel® S1600JP Product Family Power Budget and Thermal Configuration Tool* for system configuration requirements and limitations.

2.4 System Features and Options Overview

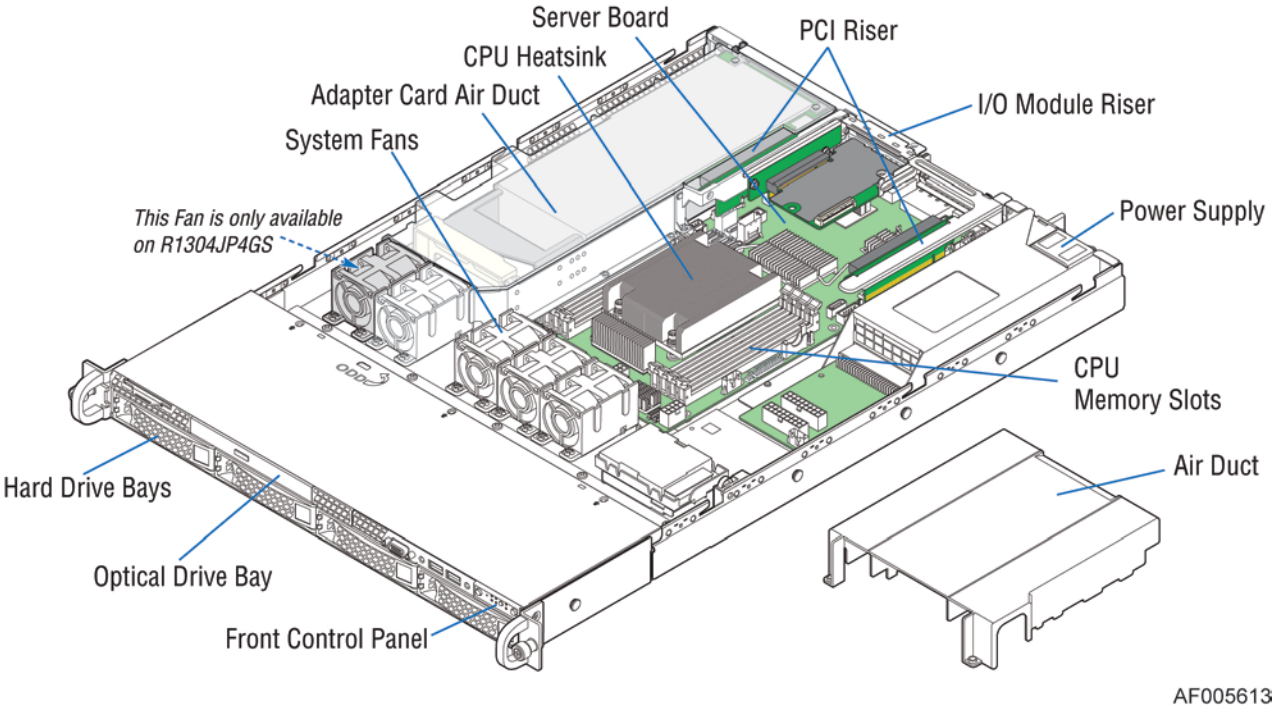


Figure 4. System Components Overview

2.4.1 Hot Swap Hard Drive Bay and Front Panel Options

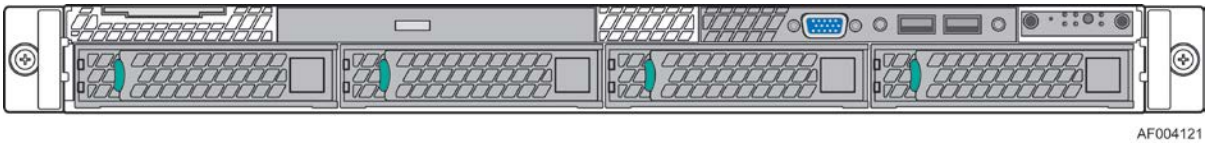


Figure 5. 3.5" Hard Drive Bay - 4 Drive Configuration

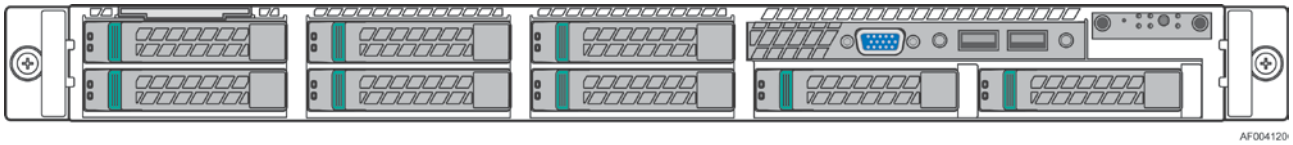


Figure 6. 2.5" Hard Drive Bay - 8 Drive Configuration

2.4.2 Back Panel Features

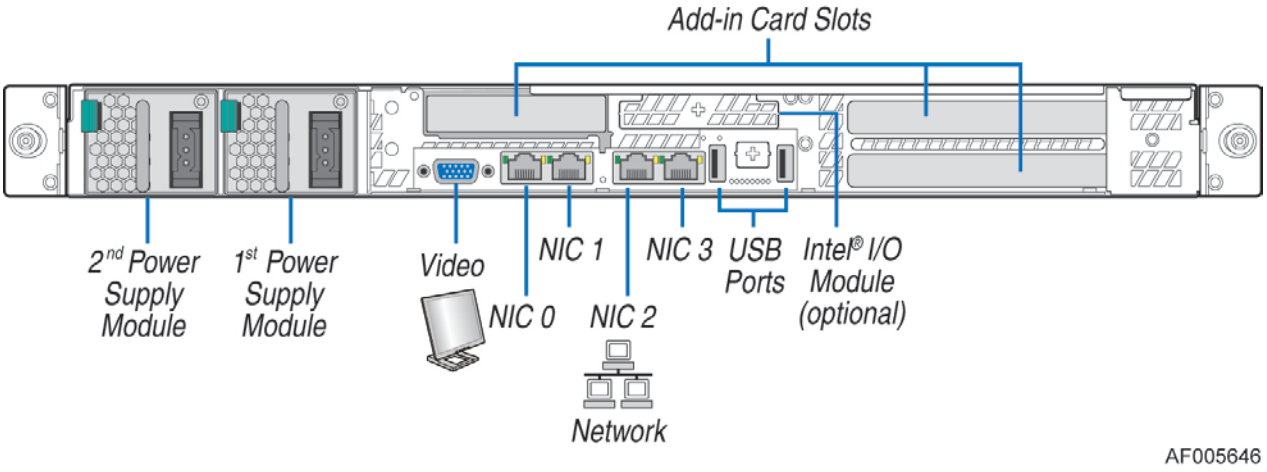
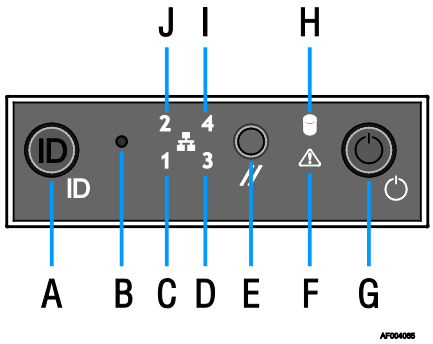


Figure 7. Back Panel Feature Identification (Redundant Power Supply as shown)

2.4.3 Front Control Panel Options



Label	Description	Label	Description
A	System ID Button w/Integrated LED	F	System Status LED
B	NMI Button (recessed, tool required for use)	G	Power Button w/Integrated LED
C	NIC-1 Activity LED	H	Hard Drive Activity LED
D	NIC-3 Activity LED	I	NIC-4 Activity LED
E	System Cold Reset Button	J	NIC-2 Activity LED

Figure 8. Front Control Panel Options

2.5 Server Board Overview

The chassis is mechanically and functionally designed to the standard form factor and half width server board, including Intel® Server Board S1600JP4. The following sections provide an overview of the server board feature sets.

The following figure shows the layout of the server board. Each connector and major component is identified. The description is given below in Figure 9.

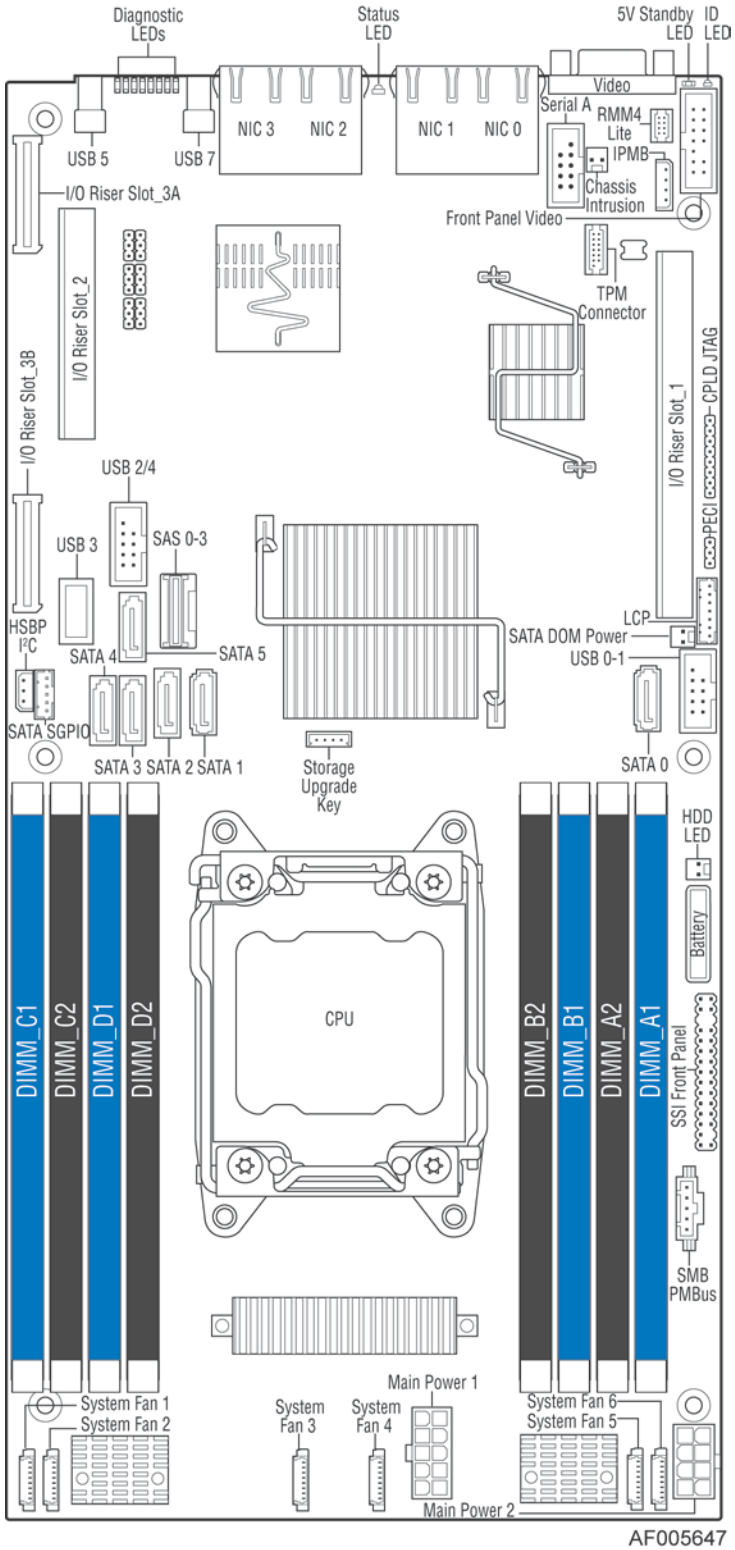
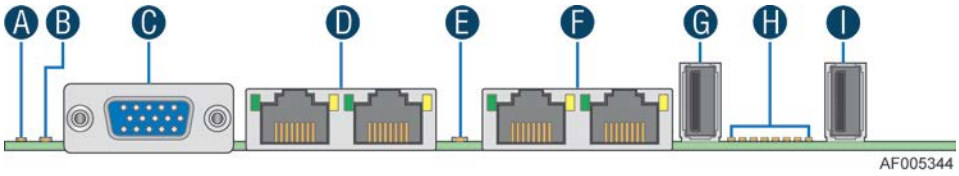


Figure 9. Intel® Server Board S1600JP4

2.5.1 Rear Component View

The following figure shows the layout of the server board. Each connector and major component is identified. The description is given below in the figure.



	Description		Description
A	ID LED	F	Two NIC ports (RJ45)
B	5V standby LED	G	USB connector
C	DB15 Video out	H	Diagnostic LED
D	Two NIC ports (RJ45)	I	USB connector
E	System status LED		

Figure 10. Intel® Server Board S1600JP Components

2.6 Available Front Bezel Support (Optional)

The optional front bezel is made of molded plastic and uses a snap-on design. When installed, its design allows for maximum airflow to maintain system cooling requirements. The face of the bezel assembly includes optional snap-in identification badge and wave (shown) features to allow for customization.
(Intel® Product Order Code – A1UBEZEL)

Figure 11. Optional Front Bezel

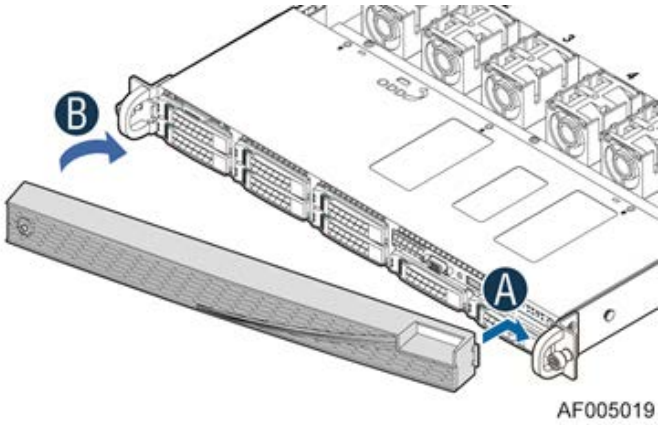


Figure 12. Installing Front Bezel

2.7 Available Rack and Cabinet Mounting Kit Options

- Tool-less rack mount rail kit – Intel® Product Code – AXXPRAIL
  - 1U and 4U compatible
  - 65 lbs maximum support weight
  - Tool-less installation
  - Full extension from rack
  - Optional cable management arm support

- Value rack mount rail kit – Intel® Product Code – AXXELVRAIL
  - 1U to 4U compatible
  - 110 lbs maximum support weight
  - Tool-less chassis attach
  - Tools required to attach rails to rack
  - 2/3 extension from rack

- Cable Management Arm – Intel® Product Code – AXX1U2UCMA (*supported with AXXPRAIL only)
- 2-Post Fixed mount bracket kit – Intel® Product Code - AXX2POSTBRCKT

3. Power Sub-System

This chapter will provide a high level overview of the power management features and specification data for the power supply options available for this server product. Specification variations will be identified for each supported power supply. There are three power supply options available in Intel® Server System R1000JP Family: 450W AC, 450W DC, and 750W AC. The server system supports redundant 450W AC power supply and redundant 450W DC power supply. The server system which integrates the 750W AC power supply is a single power supply system.

The redudant power supply platform can have up to two power supply modules installed, supporting the following power supply configurations: 1+0 (single power supply), 1+1 Redundant Power, and 2+0 Combined Power (non-redundant). 1+1 redundant power and 2+0 combined power configurations are automatically configured depending on the total power draw of the system. If the total system power draw exceeds the power capacity of a single power supply module, then power from the second power supply module will be utilized. Should this occur, power redundancy is lost. In a 2+0 power configuration, total power available may be less than twice the rated power of the installed power supply modules due to the amount of heat produced with both supplies providing peak power. Should system thermals exceed the programmed limits, platform management will attempt to keep the system operational. See *Closed Loop System Throttling (CLST)* later in this chapter, and Chapter 4 for details.

In the event of a power supply failure, redundant 1+1 power supply configurations (for 450W AC and 450W DC platforms) have support for hot-swap extraction and insertion.

3.1 450W AC Power Supply and Power Distribution Board

The 450W AC power supply with two outputs: +12V DC and +5V Standby. There is one Power Distribution Board (PDB) for 450W AC 1+1 redundant power supply. The PDB is designed to plug directly to the output connector of the power supply and it contains two DC/DC power converters to produce other required voltages: +3.3V and +5V. The PDB is integrated in the power supply cage.

3.1.1 Mechnical Overview

The following drawing is the cage which integrates the power supply units and the PDB.

Figure 13. 450W AC PSU with PDB

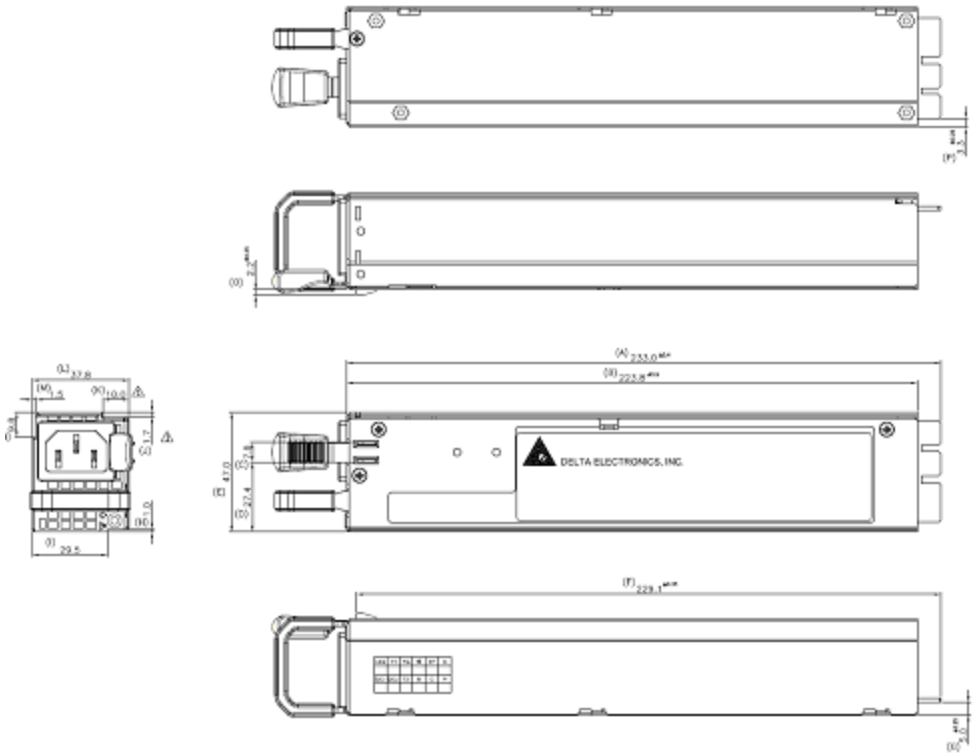


Figure 14. 450W AC Power Supply Unit Dimension Overview

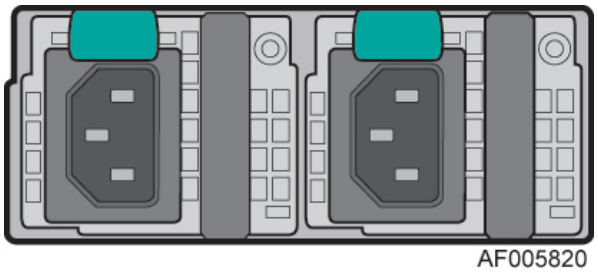


Figure 15. 450W AC Power Supply – Connector View

3.1.2 Power Supply Output Connectors

This 450W AC power supply module has 2x14 card edge output connection that plugs directly into a matching slot connector on power distribution board. The connector provides both power and communication signals. The following Table 4 defines the connector pin-out.

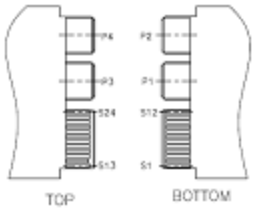


Figure 16. 450W Power Supply Module Output Power Connector

Table 4. 450W Power Supply Module Output Power Connector Pin-out

Pin	Definition	Pin	Definition
S1	NA	S2	NA
S3	L_MON	S4	ALERT
S5	SDA	S6	SCL
S7	PS_KILL	S8	PSON
S9	PSOK	S10	SGND
S11	+5VSB	S12	+5VSB
S13	FAN_PLSE2	S14	PRESENT
S15	AO	S16	VCC2
S17	FAN_GND	S18	FAN_PWR
S19	FAN_PLSE	S20	FAN_VS
S21	RS+	S22	RS-
S23	+5VSB	S24	+5VSB
P1	+12V	P2	+12V
P3	SGND	P4	SGND

3.1.3 Power Supply Module Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels: 100%, 50%, and 20%.

Table 5. 450WAC Power Supply Efficiency

Loading	100% of maximum	50% of maximum	20% of maximum
Minimum Efficiency	88%	92%	88%

3.1.4 Power Supply LED Indications

The power supply uses a bi-color LED, Amber & Green. LED states are shown as below

Table 6. 450W AC PSU LED Indications

Power Supply Condition	LED State
Output ON and OK	GREEN
No AC power to all power supplies	OFF

AC present / Only 5VSB on (PS off)	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER

3.1.5 Power Cord Specification Requirements

Power cords used must meet the specification requirements listed in the following table.

Table 7. AC Power Cord Specifications

Cable Type	SJT
Wire Size	16 AWG
Temperature Rating	105ºC
Amperage Rating	13 A
Voltage Rating	125 V

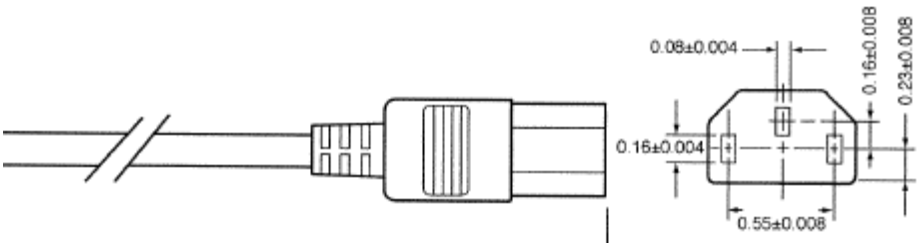


Figure 17. AC Power Cord

3.1.6 AC Input Requirement

3.1.6.1 Power Factor

The power supply must meet the power factor requirements stated in the *Energy Star® Program Requirements for Computer Servers*. These requirements are stated below.

Output power	20% load	50% load	100% load
Power factor	0.8	0.9	0.95

Tested at 230Vac, 50Hz and 60Hz, and 115VAC, 60Hz.

3.1.6.2 AC Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC should not cause damage to the power supply, including a blown fuse.

Table 8. AC Input Voltage Range

PARAMETER	MIN	RATED	VMAX	Start up VAC	Power Off VAC
Voltage (110)	90 Vrms	100-127 Vrms	140 Vrms	85VAC +/- 4VAC	70VAC +/- 5VAC
Voltage (220)	180 Vrms	200-240 Vrms	264 Vrms		
Frequency	47 Hz	50/60	63 Hz		

Notes:

1. Maximum input current at low input voltage range shall be measured at 90VAC, at maximum load.
2. Maximum input current at high input voltage range shall be measured at 180VAC, at maximum load.
3. This requirement is not to be used for determining agency input current markings.

3.1.6.3 AC Line Isolation Requirements

The power supply shall meet all safety agency requirements for dielectric strength. Additionally, power supply vendor must provide Intel® with written confirmation of dielectric withstand test which includes: voltage level, duration of test, and identification detailing how each power supply is marked to indicate that the dielectric withstand test had been completed successfully. Transformers' isolation between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage, the highest test voltage should be used. In addition, the insulation system must comply with reinforced insulation as per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements.

3.1.6.4 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout, the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration should not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time, the power supply should recover and meet all turn on requirements. The power supply should meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration should not cause damage to the power supply.

Loading	Holdup time
75%	12msec
100%	10msec

3.1.6.5 AC Line Fuse

The power supply should have one line fused in the single line fuse on the line (Hot) wire of the AC input. The line fusing must be acceptable for all safety agency requirements. The input fuse should be a slow blow type. AC inrush current must not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply should not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.1.6.6 AC Inrush

Peak inrush current must not damage the PSU, or the input fuse must not blow under any conditions of load, temperature, and input voltage, including repeated, rapid cycling of the power

line. Half cycle peak inrush current, peak repetitive input current, and worse case power factor must be provided by the vendor to assist with the UPS and line conditioning, sizing, and selection. No component will be stressed over its Max Specification (I 2·t). This must be demonstrated through measurements of the critical component specifications.

3.1.6.7 AC Line Leakage Current

The maximum leakage current to ground for each power supply shall be 3.5mA when tested at 240VAC.

3.1.6.8 AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”. These conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply must meet the requirements under the following AC line sag and surge conditions.

Table 9. AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Table 10. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

3.1.6.9 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter which meets the criteria defined in the *SSI document EPS Power Supply Specification*. For further information on Intel® standards, please request a copy of the *Intel® Environmental Standards Handbook*.

Table 11. Performance Criteria

Level	Description

A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.1.6.10 Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.1.6.11 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-4: Second edition: 2004-07 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.1.6.12 Radiated Immunity

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-3: Edition 2.1: 2002-09 test standard and performance criteria A defined in *Annex B of CISPR 24*.

3.1.6.13 Surge Immunity

The power supply shall be tested with the system for immunity to AC Unidirectional wave; 2kV line to ground and 1kV line to line, per EN 55024: 1998/A1: 2001/A2: 2003, EN 61000-4-5: Edition 1.1:2001-04.
The pass criteria include:

- No unsafe operation is allowed under any condition;
- All power supply output voltage levels to stay within proper spec levels;
- No change in operating state or loss of data during and after the test profile;
- No component damage under any condition.

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-5: Edition 1.1:2001-04 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.1.6.14 Power Recovery

The power supply should recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

3.1.6.15 Voltage Interruptions

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-11: Second Edition: 2004-03 test standard and performance criteria C defined in *Annex B of CISPR 24*.

3.1.7 DC Output Specification

3.1.7.1 Output Power/Currents

The following table defines the output current ratings. Each output has a maximum and minimum current rating shown in table 7. The power supply shall meet both static and dynamic voltage regulation requirements for the minimum dynamic load conditions. The power supply

must meet only the static load voltage regulation requirements for the minimum static load conditions.

Table 12. Load Ratings

	+12V	+5VSB
MAX	36.26A	3A
MIN DYNAMIC	2A	0.5A
MIN STATIC	0.5A	0.1A

*The combined output power of all outputs shall not exceed 405W @100~127VAC.

3.1.7.2 Standby Output

The 5VSB output should be present when an AC input greater than the power supply turn on voltage is applied.

3.1.8 Protection Circuits

Protection circuits inside the power supply should cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

3.1.8.1 Current Limit (OCP)

Following are the over current protection limits for each output. For testing purposes, the overload currents of each tested output rail should be ramped at a minimum rate of 10 A/sec starting from full load. If the current limits are exceeded, the power supply should shut down and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply should not be damaged from repeated power cycling in this condition. 5VSB must be protected under over current or shorted conditions, so that no damage can occur to the power supply. 5Vsb will be auto-recovered after removing OCP limit.

Table 13. Over Current Limits

Output	Min OCP	Max OCP
+12V	40 A	54 A
5Vstby	3.6A~8A	

3.1.8.2 Over Voltage Protection (OVP)

The power supply over voltage protection should be locally sensed. The power supply must shut down and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. Table 28 contains the over voltage limits. The values are measured at the output of the power supply's pins. The voltage should never exceed the maximum levels when measured at the power pins of the power supply connector during any single point of fail. The voltage should never trip any lower than the minimum levels when measured at the power pins of the power supply connector. 5VSB will be auto-recovered after removing the OVP limit.

Table 14. Over Voltage Protection (OVP) Limits

OUTPUT VOLTAGE	PROTECTION POINT [V]

+12 V	13.6V ~ 15.0V
5VSB	5.6V ~ 6.5V

3.1.8.3 Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition, the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply will restore power automatically, while the 12VSB remains always on. The OTP circuit must have a built in margin, such that the power supply will not oscillate ON and OFF due to the temperature recovering condition. The OTP trip level should have a minimum of 4°C of ambient temperature margin.

3.2 450W DC Power Supply

This paragraph describes the performance characteristic of a 450W power supply module with a +12V main DC output and a +5V standby output.

3.2.1 Mechnical Overview

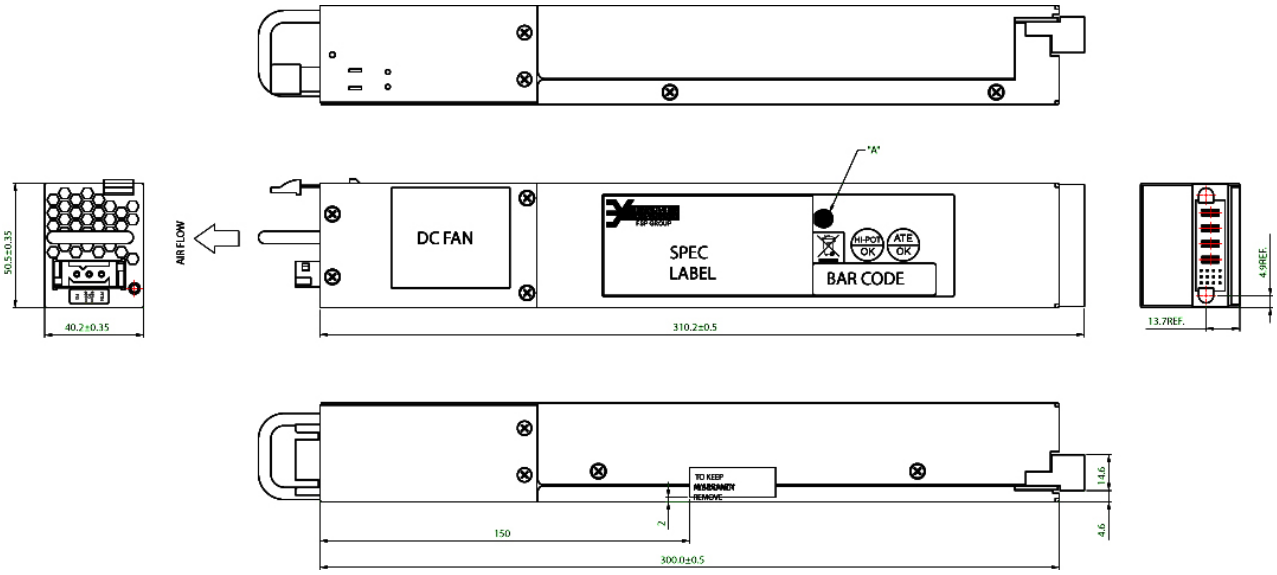


Figure 18. 450W DC Power Supply Unit Dimension Overview

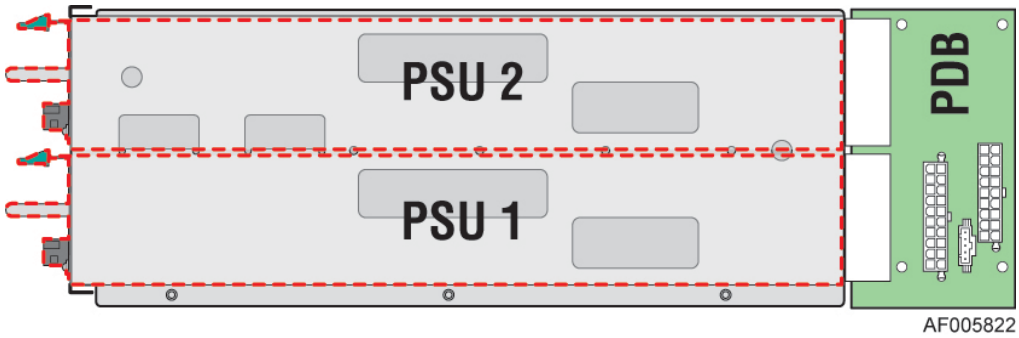


Figure 19. 450W DC Power Supply Module with PDB

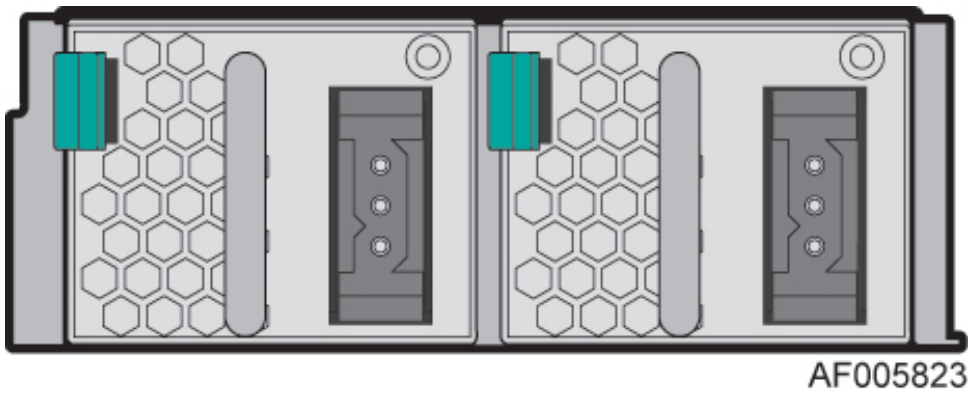
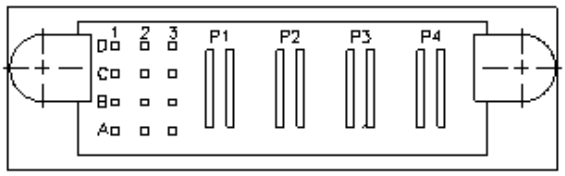


Figure 20. 450W DC Power Supply – Connector View

3.2.2 Power Connectors

3.2.2.1 Connectors on Power Distribution Board



SIGNAL PINS				POWER BLADE			
	1	2	3	P1	P2	P3	P4
D	AD	PWOK	+5VSB	RTN	RTN	+12V	+12V
C	12VLS	+15Vcc	+12VR				
B	PS-ON	SCL	B/P FAIL				
A	PS-KILL	SDA	+5VSB				

Figure 21. Power Supply Module Card Edge Connector

The DC connector has the pin-out illustrated in Figure 21. The DC power connector is the FCI#51731-042LF or equivalent.

Note: Signals that can be defined as low true or high true use the following convention: signal# = low true.

Table 15. Power Supply Module Card Edge Connector Signal Descriptions

Signal	Description	Signal	Description	Signal	Description
12VLS	+12V load share bus	PWOK	Power OK output	SCL	I^2C clock signal
5VSB	5 standby output	12VR	12V Sense	A0	I^2C address bit 0
PSON#	Power enable input	PSKILL#	Supply fast shutdown	SDA	I^2C data signal
B/P-FAIL	B/P fail input				

Table 16. Putput Power Connector 1 J4B1 Pin-out

Pin	Name	Pin	Name
10	+12V1	11	GND
9	+12V1	12	GND
8	+12V1	13	GND
7	+12V1	14	GND
6	+12V1	15	GND
5	+12V1	16	GND
4	+5V	17	GND
3	+5V	18	GND
2	+3.3V	19	GND
1	+12V2	20	+12V2

Table 17. Output Power Connector 2 J4A1 Pin-out

Pin	Name	Pin	Name
1	PSON#	10	+5V stby
2	GND	11	PWOK
3	GND	12	+3.3V
4	GND	13	+3.3V
5	+5V	14	reserved
6	+5V	15	5V_RS
7	GND	16	GND
8	GND	17	+3.3V
9	+12V1	18	+12V1

Table 18. Power Management Connector J4A2 Pin-out

Pin	Signal	24 AWG Color
1	I2C Clock	White
2	I2C Data	Yellow
3	SMBAlert#	Red
4	COM	Black
5	3.3RS	Orange

3.2.3 Power Supply Module Efficiency

This power supply supports 85% minimum at -36V to -72V for the 100% loading.

3.2.4 DC Power Input

3.2.4.1 Input voltage

	Minimum	Nominal	Maximum	Peak
Range 1	-36V	-48V	-72V	-75V

Peak Input DC voltage -75Vdc should be accepted for 1sec. without damage.

3.2.4.2 Input current

The maximum input current should be 20A for each input voltage range of Table 2.

Table 19. Maximum Input Current

Input voltage	Maximum input current	Max power
-36 to -72VAC	20-10A	100A 2u second

3.2.4.3 DC Line Fuse

The power supply should incorporate one input fuse on the return side for input over-current protection to prevent damage to the power supply and meet product safety requirements. Fuses should be slow blow type or equivalent to prevent nuisance trips. DC inrush current must not cause the DC line fuse to blow under any conditions. All protection circuits in the power supply must not cause the DC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

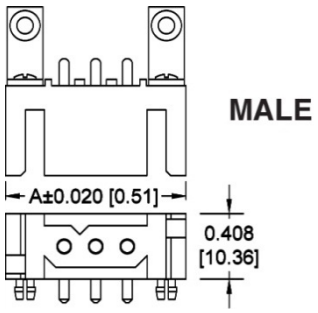
3.2.4.4 DC line inrush

The maximum DC line inrush current shall be 100A peak at an input voltage of -48VDC. Inrush current shall be measured at an ambient temperature of 25°C after the input voltage has been removed from the power supply for a minimum of 10 minutes.

3.2.4.5 DC Input connector

The power supply has an internal Positronic* Industries PLA03M4BN0A1/AA DC inlet. (Picture 1)
The mating female connector is Positronic* Industries PLA03F7000/AA. (Picture 2)

Picture 1



Picture 2

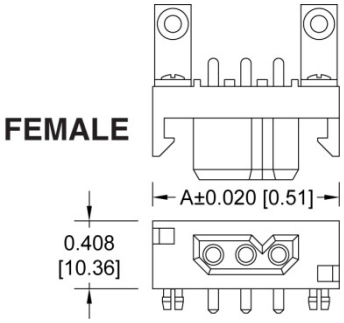


Figure 22. DC Connector

Table 20. Signal Descriptions

Signal	Description	Signal	Description	Signal	Description
12VLS	+12V load share bus	PWOK	Power OK output	SCL	I^2C clock signal
5VSB	5 standby output	12VR	12V Sense	A0	I^2C address bit 0
PSON#	Power enable input	PSKILL#	Supply fast shutdown	SDA	I^2C data signal
B/P-FAIL	B/P fail input				

3.2.5 Control and indicator functions

Signals that can be defined as low true or high true should adopt the following convention: signal# = low true.

3.2.5.1 PSON# (Power supply enable)

The PSON# signal is required to remotely turn ON/OFF the +12 V output in the power supply. When the power supply is in standby mode, the power supply fan shall be OFF. PSON# is pulled to a standby voltage by a pull-up resistor internal to the power supply. See below table for the PSON# signal characteristics.

Table 21. PS ON# Signal Characteristics

Signal Type	Pull-up to housekeeping voltage in power supply	
PSON# = Low, PSKILL = Low	ON	
PSON# = Open, PSKILL = Low or Open	OFF	
PSON# = Low, PSKILL = Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	5.25V
Source current, Vpson = low		1mA

3.2.5.2 PSKILL

The purpose of the PSKILL pin is to allow for hot swapping of the power supply. The PSKILL pin on the power supply is shorter than the other signal pins. The mating pin of this signal in the system should be tied to the ground. Internal to the power supply, the PSKILL pin should be connected to a standby voltage through a pull-up resistor. Upon receiving a LOW state at the PSKILL pin, a PSON# signal shall enable the power supply to turn on. See below table for the PSKILL signal characteristics.

Table 22. PSKILL Signal Characteristics

Signal Type (Input Signal to Supply)	Accepts a ground input from the system. Pull- up to VSB located in the power supply

PSKILL = Low, PSON# = Low	ON	
PSKILL = Low or Open, PSON# = Open	OFF	
PSKILL = Open , PSON# = Low	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	5.25V
Source current, Vpskill = low		4mA

3.2.5.3 PWOK (Power Good)

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are above their respective lower regulation limits. See the following table.

Table 23. PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located power supply	
PWOK=High	Power Good	
PWOK=Low	Power Not Good	
	MIN	MAX
Logic level low voltage, Isink=4mA	0V	0.4V
Logic level high voltage, Isource = 200uA	2.4V	5.25V
Sink current, PWOK=low		4mA
Source current, PWOK=high		2mA

3.2.5.4 B/P Fail function

This pin senses the backplane fail signal; when the backplane outputs causes OCP, OVP, or any other fail, the B/P fail signal pin goes HIGH, the module will shut down and the LED will indicate “red”.

3.2.5.5 LED indicators

These will be a bi-color LED to indicate power supply status.

Table 24. 450W DC PSU LED Indicator

Power supply condition	Power supply LED
No DC power to all PSU	OFF
No DC power to this PSU only	Flashing Red
DC present/only standby output on	Flashing BLUE
Power supply DC output ON and OK	BLUE
Power supply failure	RED

3.2.6 DC output voltages

3.2.6.1 Output rating at different input voltage ranges

Each DC output shall be capable of supplying the output current shown in Table 25. Total output power for +12V and +5VSB combined shall be ≤ 450 W @ 50om.

Table 25. Output rating

Output	Min	Max

+12V	2A	36.25A
+5VSB	0	3A

3.2.6.2 No load operation

The power supply must meet all requirements except for the transient loading requirements when operated at no load on all outputs.

3.2.6.3 Regulation, ripple, and noise

The power supply must meet the regulation, ripple, and noise limit under all operating conditions (AC line, transient loading, and output loading).

Table 26. Output voltage regulation

	Output voltage limits (Vdc)			
Output	Minimum	Nominal	Maximum	REG
+12V	11.64V	12V	12.36V	+/-3%
+5VSB	4.75V	5V	5.25V	+/-5%

3.2.6.4 Ripple and noise

Ripple and noise should be measured with 0.1uF of ceramic capacitance and 10uF of tantalum capacitance on each of the power supply output connector terminal. The ripple and noise should be met over all load ranges and AC line voltages with 1 to 2 power supplies in parallel operation. The output noise requirements shall apply over a 0Hz to 20MHz bandwidth.

Output	+12V	5VSB
Maximum ripple/noise	150mVp-p	50mVp-p

3.2.6.5 Transient loading

The power supply must operate within the specified limits and meet regulation requirements over the following transient loading conditions anywhere within the specified load range of the power supply. This shall be tested with no additional bulk capacitance added to the load.

Output	Step size	Slew rate	Capacitive Load
+12V	60% OF MAX.	0.5A/usec	2200uF
+5VSB	25% OF MAX.	0.5A/usec	1uF

3.2.6.6 Capacitive load

The power supply shall operate within specifications over the capacitive load range defined.

Output	Min	Max
+12V	10uF	11,000uF
+5VSB	1uF	350uF

3.2.6.7 Maximum load change

The power supply shall continue to operate normally when there is a step change ≤ 1 A/uS between the minimum load and the maximum load.

3.2.6.8 Load sharing control

3.2.6.8.1 +12V load sharing

The +12 V output shall have active load sharing. When operating at 50% of full load, the output current of any two power supplies must be within (+/-6.5%). For example, if power supply #1 is operating at 20A, then all other power supplies within the system shall be operating between 18.7A to 21.3A (+/- 6.5% of 20A). All current sharing functions should be implemented internally to the power supply by making use of the 12VLS signal. The 1+1 power supply system must connect the 12VLS signals between the power supplies together. The power supply should be able to share with up to two power supplies in parallel.

If the load sharing is disabled by shorting the load share bus to ground, the power supply should continue to operate within regulation limits for loads less than or equal to the rating of one power supply.

Table 27. Load Share Bus Output Characteristics

Item	Description	Min	Nominal	Max	Units
V_{share};I_{out}=Max.	Voltage of load share bus at specified max output current		6		V
$\triangle V_{share}/\triangle I_{out}$; I_{out}>1A	Slope of load share bus voltage with changing load		6/Ioutmax		V/A
I_{share}SINK; V_{share}=4.35V	Amount of current the load share bus output from each power supply is allowed to sink		1.5		mA
I_{share}SOURCE; V_{share}=4.35V	Amount of current the load share bus output form each power supply needs to source		1.5		mA
T_{share}; I_{out}=Max.	Delay from output voltages in regulation to load sharing active with maximum load of one power supply and two power supplies in parallel. (remote on/off only)			100	msec

The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The power supplies must be able to load share with 100mV of drop between different power supply's outputs.

3.2.6.9 Output voltage rise time

The turn on waveform for the +12V output shall be monotonic with less than 5% of overshoot. The rise time from 10% (1.2V) to 90% (10.8V) shall be less than 50msec for a single power supply.

3.2.6.10 Output voltage hold-up time

Upon loss of input voltage (at nominal), the output voltages shall remain in regulation for at least 10 msec.

3.2.6.11 Timing requirements

The timing requirements for the power supply's +12V, +5VSB, and PWOK signal are defined for turn on and turn off of the power supply. Also presented is the requirement for the timing of power supply shutdown under a current limit condition.

The timing of signals and power are specified in Table 28 and illustrated in Figure 23.

Table 28. Turn On/Off Timing

Turn on	Description	Min	Max	Units
Tvout rise	Output voltage rise time from each main output	5	50	msec
Tsb_on_delay	Delay from DC being applied to 5VSB being within regulation		1500	msec
Tac_on_delay	Delay from DC being applied to all output voltage being within regulation		2500	msec
Tvout_holdup	Time all output voltages, including +12V, stay within regulation after loss of DC	11		msec
Tpwok_holdup	Delay from loss of DC to deassertion of PWOK	10		msec
Tpson_on_delay	Delay from PSON# Active to output voltages within regulation limits	5	400	msec
Tpwok_on	Delay from output voltage(12V) within regulation limits to PWOK asserted at turn on	100	500	msec
Tpwok_off	Delay from PWOK deasserted to 12VDC or 12VSB dropping out of regulation limits	1		msec
Tpwok_low	Duration of PWOK being in the deasserted state during an off/on cycle using DC or the PSON signal	100		msec
Tsb_vout	Delay from 5Vsb being in regulation to 12VDC being in regulation at DC turn on	50	1000	msec

3.2.6.12 Timing requirements

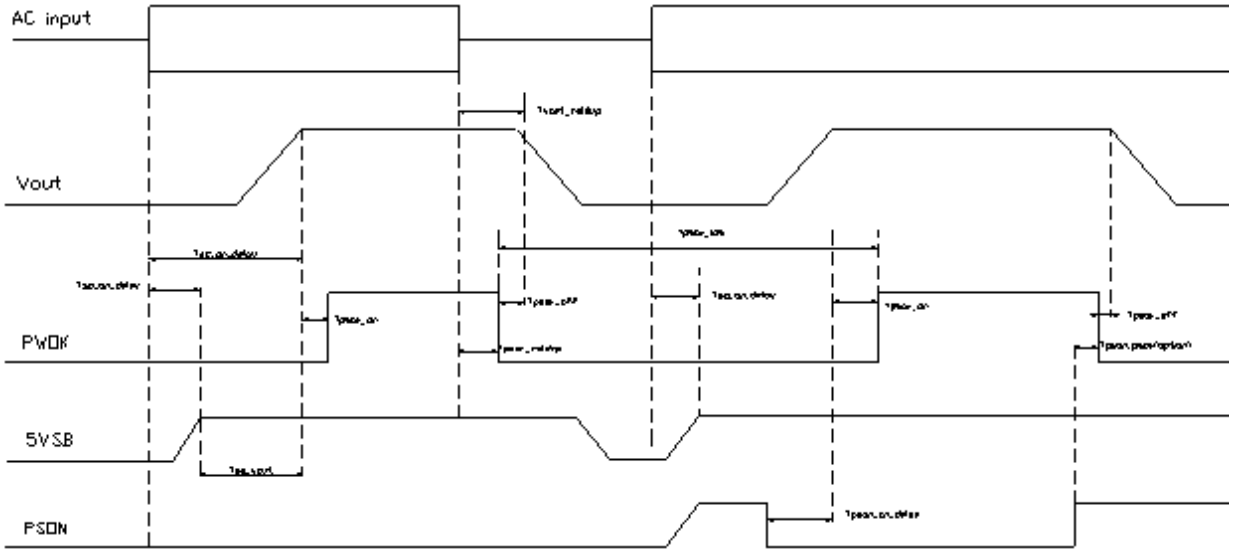


Figure 23. Turn On/Off Timing

3.2.6.13 Overshoot

Any output overshoot at turn on shall be less than 10% of the nominal output value. Any overshoot shall recover to within the specified regulation in less than 0.5mS.

3.2.6.14 Temperature coefficient

After operating for 30 minutes or longer at 25°C ambient temperature, the output voltages shall not change by more than ± 0.05 % per degree C for any given line and load conditions.

3.3 750W AC Power Supply

In Intel® Server System R1304JP4GS and R1208JP4GS, there is a single 750W power supply integrated. The parameters of this power supply are defined in below paragraph.

3.3.1 Mechanical Overview

The physical size of the power supply enclosure is 39/40mm x 73.5mm x 185mm. The power supply contains a single 40mm fan. The power supply has a card edge output that interfaces with a 2x25 card edge connector in the system. The AC plugs directly into the external face of the power supply. Refer to the following figure:

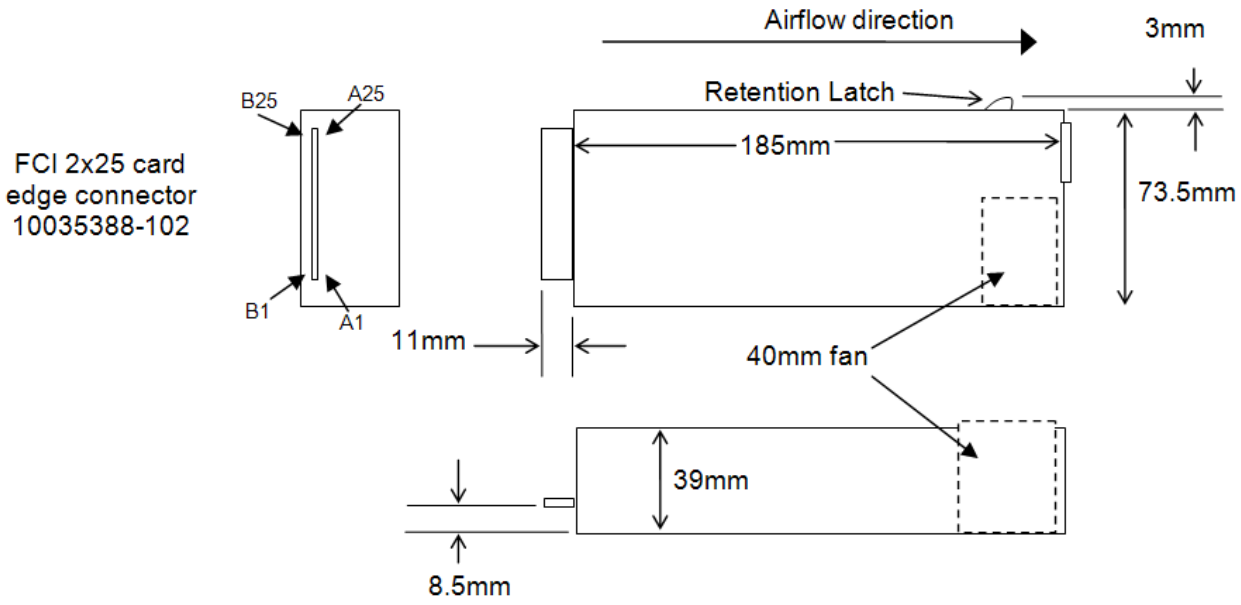


Figure 24. 750WAC Power Supply Unit Dimension Overview

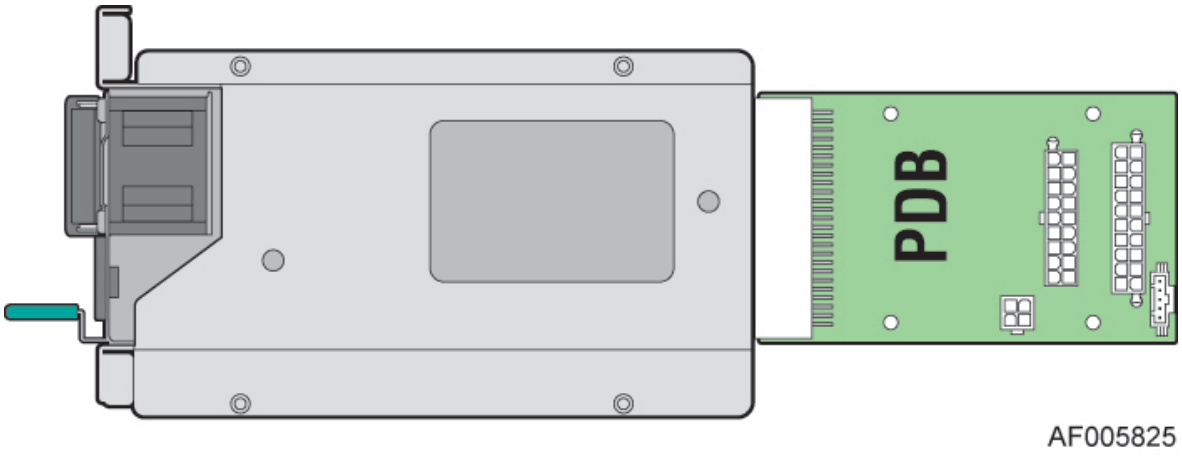


Figure 25. 750W AC Power Supply Module with PDB

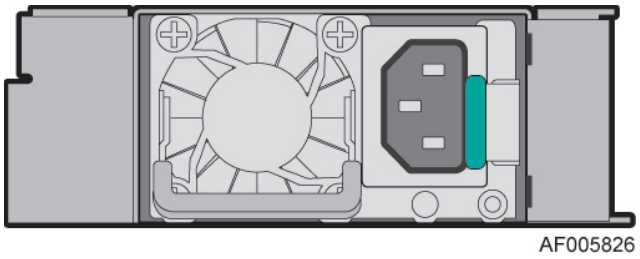


Figure 26. 750W AC Power Supply – Connector View

3.3.2 Connectors on Power Distribution Board

The power supply shall use a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector.

Table 29. Power Supply Module Output Power Connector J1D1 Pin-out

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus* SDA	B19	A0 (SMBus* address)
A20	PMBus* SCL	B20	A1 (SMBus* address)
A21	PSON	B21	12V stby
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Return Sense	B23	12V load share bus
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	Compatibility Check pin*

Table 30. Output Power Connector 1 J2A2 Pin-out

Pin	Name	Pin	Name
10	+12V1	11	GND
9	+12V1	12	GND
8	+12V1	13	GND
7	+12V1	14	GND
6	+12V1	15	GND
5	+12V1	16	GND
4	+5V	17	GND
3	+5V	18	GND
2	+3.3V	19	GND
1	+12V2	20	+12V2

Table 31. Output Power Connector 2 J1B1 Pin-out

Pin	Name	Pin	Name
1	PSON#	10	+5V stby
2	GND	11	PWOK
3	GND	12	+3.3V
4	GND	13	+3.3V
5	+5V	14	reserved
6	+5V	15	5V_RS
7	GND	16	GND
8	GND	17	+3.3V
9	+12V1	18	+12V1

Table 32. Output Power Connector 3 J2B1 Pin-out

Pin	Name	Pin	Name
1	+12V1	3	GND
2	+12V1	4	GND

Table 33. Power Management Connector J2A1 Pin-out

Pin	Signal	24 AWG Color
1	I2C Clock	White
2	I2C Data	Yellow
3	SMBAlert#	Red
4	COM	Black
5	3.3RS	Orange

3.3.3 Power Supply Module Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels: 100%, 50%, 20%, and 10%.

Table 34. 750 Watt AC Power Supply Efficiency

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximun
Minimum Efficiency	91%	94%	90%	82%

3.3.4 Power Cord Specification Requirements

Power cords used must meet the specification requirements listed in the following table:

Table 35. AC Power Cord Specifications

Cable Type	SJT
Wire Size	16 AWG
Temperature Rating	105ºC
Amperage Rating	13 A
Voltage Rating	125 V

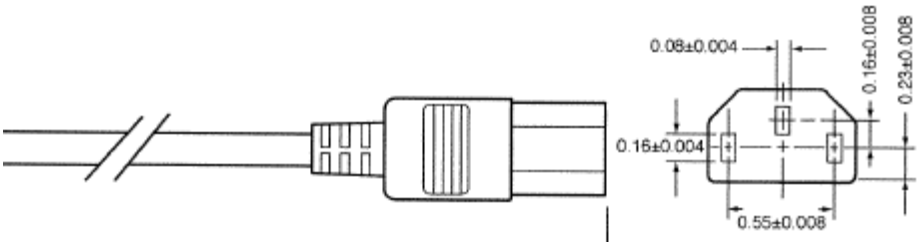


Figure 27. AC Power Cord

3.3.5 Power Supply LED Indications

The power supply uses a bi-color LED, Amber & Green. LED states are shown as below.

Table 36. 750W AC PSU LED Indications

Power Supply Condition	LED State
Output ON and OK	GREEN
No AC power to all power supplies	OFF
AC present / Only 12VSB on (PS off) or PS in Cold redundant state	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER
Power supply FW updating	2Hz Blink GREEN

3.3.6 AC Input Requirement

3.3.6.1 Power Factor

The power supply must meet the power factor requirements stated in the *Energy Star® Program Requirements for Computer Servers*. These requirements are stated below:

Output power	10% load	20% load	50% load	100% load
Power factor	> 0.65	> 0.80	> 0.90	> 0.95

Note:

Tested at 230Vac, 50Hz and 60Hz, and 115VAC, 60Hz.

Tested according to *Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.4.3*. This is posted at http://efficientpowersupplies.epri.com/methods.asp.

3.3.6.2 AC Inlet Connector

The AC input connector shall be an IEC 320 C-14 power inlet. This inlet is rated for 10A/250VAC.

3.3.6.3 AC Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC should not cause damage to the power supply, including a blown fuse.

Table 37. AC Input Voltage Range

PARAMETER	MIN	RATED	VMAX	Start up VAC	Power Off VAC
Voltage (110)	90 Vrms	100-127 Vrms	140 Vrms	85VAC +/- 4VAC	74VAC +/- 5VAC
Voltage (220)	180 Vrms	200-240 Vrms	264 Vrms		
Frequency	47 Hz	50/60	63 Hz		

Notes:

1. Maximum input current at low input voltage range shall be measured at 90VAC, at maximum load.
2. Maximum input current at high input voltage range shall be measured at 180VAC, at maximum load.
3. This requirement is not to be used for determining agency input current markings.

3.3.6.4 AC Line Isolation Requirements

The power supply should meet all safety agency requirements for dielectric strength. Additionally, power supply vendor must provide Intel® with written confirmation of dielectric withstand test which includes: voltage level, duration of test, and identification detailing how each power supply is marked to indicate dielectric withstand test had been completed successfully. Transformers' isolation between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage, the highest test voltage should be used. In addition, the insulation system must comply with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements.

3.3.6.5 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout, the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time, the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration should not cause damage to the power supply.

Loading	Holdup time
70%	12msec

3.3.6.6 AC Line 12VSB Holdup

The 12VSB output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of 70ms min (=12VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

3.3.6.7 AC Line Fuse

The power supply shall have one line fused in the single line fuse on the line (Hot) wire of the AC input. The line fusing must be acceptable for all safety agency requirements. The input fuse should be a slow blow type. AC inrush current should not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply must not cause the AC fuse to blow, unless a component in the power supply has failed. This includes DC output load short conditions.

3.3.6.8 AC Inrush

AC line inrush current should not exceed 55A peak, for up to one-quarter of the AC cycle, after which, the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (T_{op}).

3.3.6.9 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”; these conditions are defined as the AC line voltage dropping below nominal voltage conditions. “Surge” is defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply must meet the requirements under the following AC line sag and surge conditions.

Table 38. AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria

0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30 %	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Table 39. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

3.3.6.10 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter which meets the criteria defined in the *SSI document EPS Power Supply Specification*. For further information on Intel® standards, please request a copy of the *Intel® Environmental Standards Handbook*.

Table 40. Performance Criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.3.6.11 Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.3.6.12 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-4: Second edition: 2004-07 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.3.6.13 Radiated Immunity

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-3: Edition 2.1: 2002-09 test standard and performance criteria A defined in *Annex B of CISPR 24*.

3.3.6.14 Surge Immunity

The power supply shall be tested with the system for immunity to AC Unidirectional wave; 2kV line to ground and 1kV line to line, per EN 55024: 1998/A1: 2001/A2: 2003, EN 61000-4-5: Edition 1.1:2001-04 .

The pass criteria include:

- No unsafe operation is allowed under any condition
- All power supply output voltage levels to stay within proper spec levels
- No change in operating state or loss of data during and after the test profile
- No component damage under any condition

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-5: Edition 1.1:2001-04 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.3.6.15 Power Recovery

The power supply must recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

3.3.6.16 Voltage Interruptions

The power supply must comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-11: Second Edition: 2004-03 test standard and performance criteria C defined in *Annex B of CISPR 24*.

3.3.6.17 Power Factor

The power supply must meet the power factor requirements stated in the *Energy Star® Program Requirements for Computer Servers*. These requirements are stated below.

Output power	20% load	50% load	100% load
Power factor	0.8	0.9	0.95

Tested at 230Vac, 50Hz and 60Hz, and 115VAC, 60Hz.

Tested according to *Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.4.3*. This is posted at http://efficientpowersupplies.epri.com/methods.asp.

3.3.6.18 AC Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC shall not cause damage to the power supply, including a blown fuse.

Table 41. AC Input Voltage Range

PARAMETER	MIN	RATED	VMAX	Start up VAC	Power Off VAC
Voltage (110)	90 Vrms	100-127 Vrms	140 Vrms	85VAC +/- 4VAC	70VAC +/- 5VAC
Voltage (220)	180 Vrms	200-240 Vrms	264 Vrms		
Frequency	47 Hz	50/60	63 Hz		

Notes:
Maximum input current at low input voltage range shall be measured at 90VAC, at maximum load.
Maximum input current at high input voltage range shall be measured at 180VAC, at maximum load.
This requirement is not to be used for determining agency input current markings.

3.3.6.19 AC Line Isolation Requirements

The power supply shall meet all safety agency requirements for dielectric strength. Additionally, power supply vendor must provide Intel® with written confirmation of dielectric withstand test which includes: voltage level, duration of test, and identification detailing how each power supply is marked to indicate dielectric withstand test had been completed successfully. Transformers' isolation between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage, the highest test voltage should be used. In addition, the insulation system must comply with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements.

3.3.6.20 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout, the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time, the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration shall not cause damage to the power supply.

Loading	Holdup time
75%	12msec
100%	10msec

3.3.6.21 AC Line Fuse

The power supply shall have one line fused in the single line fuse on the line (Hot) wire of the AC input. The line fusing shall be acceptable for all safety agency requirements. The input fuse should be a slow blow type. AC inrush current must not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply must not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.3.6.22 AC Inrush

Peak inrush current shall not damage the PSU or the input fuse shall not blow under any conditions of load, temperature, and input voltage including repeated, rapid cycling of the power line. Half cycle peak inrush current, peak repetitive input current and worse case power factor shall be provided by the vendor to assist with the UPS and line conditioning, sizing, and selection. No component will be stressed over its Max Specification (I 2·t). This must be demonstrated through measurements of the critical component specifications.

3.3.6.23 AC Line Leakage Current

The maximum leakage current to ground for each power supply shall be 3.5mA when tested at 240VAC.

3.3.6.24 AC Line Transient Specification

AC line transient conditions shall be defined as "sag" and "surge" conditions. "Sag" conditions are also commonly referred to as "brownout", these conditions will be defined as the AC line

voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 42. AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Table 43. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

3.3.6.25 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter which meets the criteria defined in the *SSI document EPS Power Supply Specification*. For further information on Intel® standards, please request a copy of the *Intel® Environmental Standards Handbook*.

Table 44. Performance Criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.3.7 DC Output Specification

3.3.7.1 Output Power/Currents

The following table defines the minimum power and current ratings. The power supply must meet both static and dynamic voltage regulation requirements for all conditions.

Table 45. Minimum Load Ratings

Parameter	Min	Max.	Peak 2	Unit
12V main	0.0	62.0	70.0	A
12Vstby 1	0.0	2.1	2.4	A

Notes:

1. 12Vstby must provide 4.0A with two power supplies in parallel. The fan may work when stby current >1.5A
2. Length of time peak power can be supported is based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration shall be 20 seconds without asserting the SMBAlert# signal at maximum operating temperature.

3.3.7.2 Pmax Power support

The PSU should support 3msec peak power duration at a 50msec period; 5.7% duty cycle, Step loading from 730W to 990W. Full AC input range; 100-127VAC/200-240VAC

The PSU should support one time 8ms duration 990W peak power without leading to PSU shutdown.

3.3.7.3 Standby Output

The 12VSB output shall be present when an AC input greater than the power supply turn on voltage is applied.

There should be load sharing in the standby rail. And two PSU modules should be able to support 4A standby current.

3.3.8 Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

3.3.8.1 Current Limit (OCP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply shall shut down and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

Table 46 Over Current Protection

Output VOLTAGE	Input voltage range	OVER CURRENT LIMITs
+12V	90 – 264VAC	72A min; 78A max
12VSB	90 – 264VAC	2.5A min; 3.5A max

3.3.8.2 Over Voltage Protection (OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shut down and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage should never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage should never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing OVP limit.

Table 47. Over Voltage Protection (OVP) Limits

Output Voltage	MIN (V)	MAX (V)
+12V	13.0	14.5
+12VSB	13.3	14.5

3.3.8.3 Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 4°C of ambient temperature margin.

4 Thermal Management

The fully integrated system is designed to operate at external ambient temperatures of between 10ºC- 35ºC with limited excursion based operation up to 35ºC, as specified in Table 3.. Working with integrated platform management, several features within the system are designed to move air in a front to back direction, through the system and over critical components in order to prevent them from overheating and allow the system to operate with best performance.

The Intel® Server System R1000JP product family supports short-term, excursion-based, operation up to 35°C (ASHRAE A2) with limited performance impact. The configuration requirements and limitations are described in the configuration matrix found in the Intel® S1600JP Product Family Power Budget and Thermal Configuration Tool, available to download online at http://www.intel.com/p/en_US/support.

The installation and functionality of several system components are used to maintain system thermals.

Note: To support Intel® Xeon Processor E5-2690 and E5-2643, the system must change to the processor heatsink product order code FXXCA84X106HS.

4.1 Thermal Operation and Configuration Requirements

To keep the system operating within supported maximum thermal limits, the system must meet the following operating and configuration guidelines:

- The system operating ambient is designed for sustained operation up to 35ºC (ASHRAE Class A2).
  - When operating within the extended operating temperature range, then the system performance may be impacted.
  - There is no long term system reliability impact when operating at the extended temperature range within the approved limits.
- Specific configuration requirements and limitations are documented in the configuration matrix found in the *Intel® Server Board S1600JP product family Power Budget and Thermal Configuration Guidelines Tool,* available to download online at http://www.intel.com/p/en_US/support
- The processor and the CPU heatsink must be installed first.
- **Memory Slot population requirements –**

  Note: Specified memory slots can be populated with a DIMM or supplied DIMM Blank. Memory population rules apply when installing DIMMs. Install DIMMs in the order; Channels A, B, C, and D. Start with the first DIMM (Blue Slot) on each channel, then slot 2. Only remove factory installed DIMM blanks when populating the slot with an actual memory module.
- All hard drive bays must be populated. Hard drive carriers can be populated with a hard drive or supplied drive blank.
- The air duct must be installed at all times.
- In single power supply configurations, the second power supply bay must have the supplied filler blank installed at all times.
- The system top-cover must be installed at all times.

4.2 Thermal Management Overview

In order to maintain the necessary airflow within the system, all of the previously listed components and top cover need to be properly installed. For best system performance, the external ambient temperature should remain below 35ºC and all system fans should be operational. The system is designed for fan redundancy when the system is configured with two power supplies. Should a single system fan fail (System fan or Power Supply Fan), integrated platform management will: change the state of the System Status LED to flashing Green, report an error to the system event log, and automatically adjust fan speeds as needed to maintain system temperatures below maximum thermal limits.

Note: All system fans are controlled independent of each other. The fan control system may adjust fan speeds for different fans based on increasing/decreasing temperatures in different thermal zones within the chassis.

In the event that system thermals should continue to increase with the system fans operating at their maximum speed, platform management may begin to throttle bandwidth of either the memory subsystem or the processors or both, in order to keep components from overheating and keep the system operational. Throttling of these sub-systems will continue until system thermals are reduced below preprogrammed limits.

Should system temperatures increase to a point beyond the maximum thermal limits, the system will shut down, the System Status LED will change to a solid Amber state, and the event will be logged to the system event log.

Note: Sensor data records (SDRs) for any given system configuration must be loaded by the system integrator for proper thermal management of the system. SDRs are loaded using the FRUSDR utility.

An intelligent Fan Speed Control (FSC) and thermal management technology (mechanism) is used to maintain comprehensive thermal protection, deliver the best system acoustics, and fan power efficiency. Options in <**F2**> BIOS Setup (**BIOS** > **Advanced** > **System Acoustic and Performance Configuration**) allow for parameter adjustments based on the actual system configuration and usage. Refer to the following sections for a description of each setting.

4.2.1 Set Throttling Mode

This option is used to select the desired memory thermal throttling mechanism. Available settings include:

[Auto], [DCLTT], [SCLTT], and [SOLTT].

[Auto] – Factory Default Setting - BIOS automatically detects and identifies the appropriate thermal throttling mechanism based on the DIMM type, airflow input, and DIMM sensor availability.

[DCLTT] – Dynamic Closed Loop Thermal Throttling: for the SOD DIMM with system airflow input.

[SCLTT] – Static Close Loop Thermal Throttling: for the SOD DIMM without system airflow input.

[SOLTT] – Static Open Loop Thermal Throttling: for the DIMMs without sensor on DIMM (SOD).

4.2.2 Altitude

This option is used to select the proper altitude that the system will be used in. Available settings include: [300m or less], [301m-900m], [901m-1500m], [Above 1500m].

Selecting an altitude range that is lower than the actual altitude the system will be operating at, can cause the fan control system to operate less efficiently, leading to higher system thermals and lower system performance. If the altitude range selected is higher than the actual altitude the system will be operating at, the fan control system may provide better cooling but with higher acoustics and higher fan power consumption. If the altitude is not known, selecting a higher altitude is recommended in order to provide sufficient cooling.

4.2.3 Set Fan Profile

This option is used to set the desired Fan Profile. Available settings include:

[Performance] and [Acoustic]

The Acoustic mode offers the best acoustic experience and appropriate cooling capability supporting the majority of the add-in cards used. Performance mode is designed to provide sufficient cooling capability covering all kinds of add-in cards on the market.

4.2.4 Fan PWM Offset

This option is reserved for manual adjustment to the minimum fan speed curves. The valid range is from [0 to 100] which stands for 0% to 100% PWM adding to the minimum fan speed. This feature is valid when Quiet Fan Idle Mode is at Enabled state. The default setting is [0].

4.2.5 Quiet Fan Idle Mode

This feature can be [Enabled] or [Disabled]. If enabled, the fans will either shift to a lower speed or stop when the aggregate sensor temperatures are satisfied, indicating the system is at ideal thermal/light loading conditions. When the aggregate sensor temperatures are not satisfied, the fans will shift back to normal control curves. If disabled, the fans will never shift into lower fan speeds or stop, regardless of whether the aggregate sensor temperatures are satisfied. The default setting is [Disabled].

Note: The above feature may or may not be in effect and depends on the actual thermal characteristics of the specified system.

4.2.6 Thermal Sensor Input for Fan Speed Control

The BMC uses various IPMI sensors as inputs to control fan speed. Some of the sensors are actual physical sensors and some are “virtual” sensors derived from calculations.

The following IPMI thermal sensors are used as input to control fan speed:

- Front Panel Temperature Sensor[1]
- CPU Margin Sensors[2, 4, 5]
- DIMM Thermal Margin Sensors[2, 4]
- PCH Temperature Sensor[3,5]

- On-board Ethernet Controller Temperature Sensors[3, 5]
- Add-In Intel® SAS/IO Module Temperature Sensors[3, 5]
- PSU Thermal Sensor[3, 8]
- CPU VR Temperature Sensors[3, 6]
- DIMM VR Temperature Sensors[3, 6]
- BMC Temperature Sensor[3, 6]
- Global Aggregate Thermal Margin Sensors [7]
- I/O module Temperature Sensor (With option installed)
- Intel® ROC Module (With option installed)

Notes:
1. For fan speed control in Intel® chassis
2. Temperature margin from throttling threshold
3. Absolute temperature
4. PECI value or margin value
5. On-die sensor
6. On-board sensor
7. Virtual sensor
8. Available only when PSU has PMBus*
9. Calculated estimate

The following diagram illustrates the fan speed control structure:

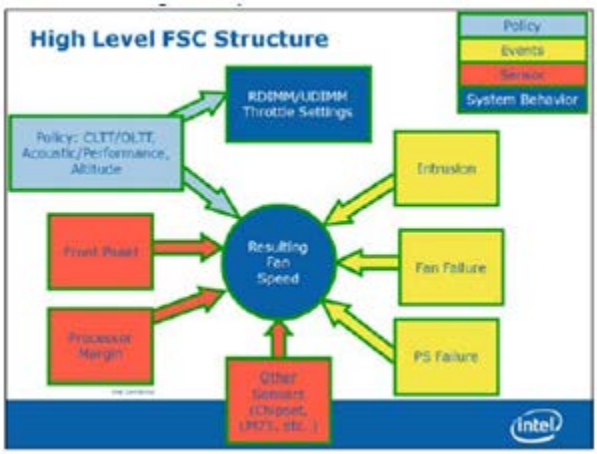


Figure 28. Fan Control Model

4.3 System Fans

Four managed dual rotor 40mm x 56mm system fans and an embedded fan for each installed power supply, provide the primary airflow for the system (five fans for R1304JP4GS and R1208JP4GS).

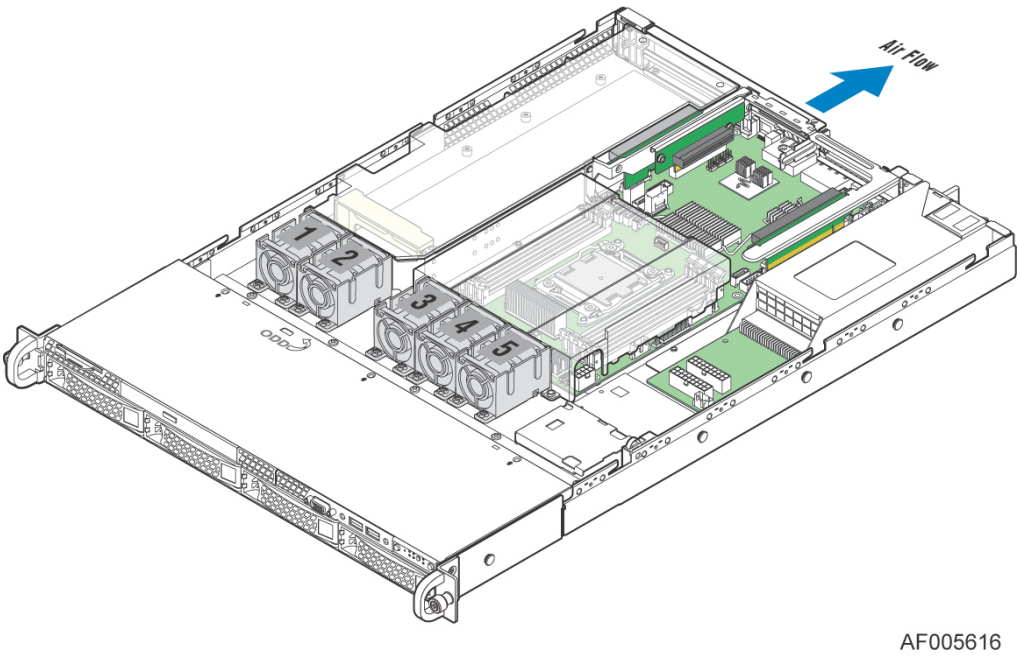


Figure 29. System Fan Identification

Each system fan is mounted inside its own plastic fan housing which include rotational vibration dampening features. The fan assemblies are held in place by fitting them over mounting pins coming up from the chassis base.

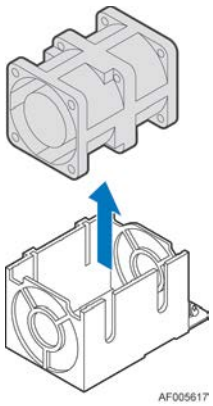


Figure 30. Removing a System Fan

The system fan assembly is designed for ease of use and supports several features.

System fans are NOT hot-swappable.

Each fan and fan assembly is designed for tool-less insertion and extraction from the system. For instructions on fan replacement, see the *Intel® Server System R1000JP Service Guide*.

Fan speed for each fan is controlled by integrated platform management as controlled by the integrated BMC on the server board. As system thermals fluctuate high and low, the integrated BMC firmware will increase and decrease the speeds to specific fans to regulate system thermals.

Each fan has a tachometer signal that allows the integrated BMC to monitor its status.

Each fan has a10-pin wire harness that connects to a matching connector on the server board.

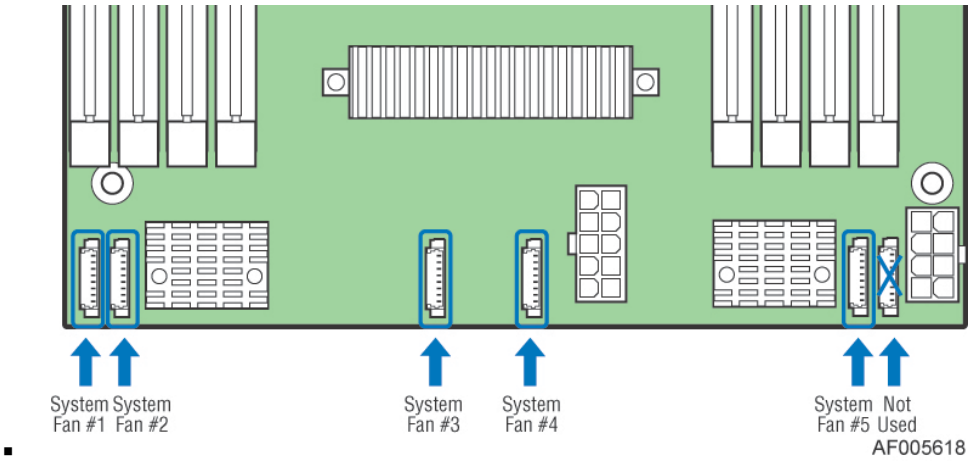


Figure 31. Server Board System Fan Connector Locations

Table 48. System Fan Connector Pin-out

SYS_FAN 1		SYS_FAN 2		SYS_FAN 3	
Signal Description	Pin#	Signal Description	Pin#	Signal Description	Pin#
FAN_TACH1_IN	1	FAN_TACH3_IN	1	FAN_TACH5_IN	1
FAN_IBMC_PWM0_R_BUF	2	FAN_IBMC_PWM1_R_BUF	2	FAN_IBMC_PWM2_R_BUF	2
P12V_FAN	3	P12V_FAN	3	P12V_FAN	3
P12V_FAN	4	P12V_FAN	4	P12V_FAN	4
FAN_TACH0_IN	5	FAN_TACH2_IN	5	FAN_TACH4_IN	5
GROUND	6	GROUND	6	GROUND	6
GROUND	7	GROUND	7	GROUND	7
FAN_SYS0_PRSNT_N	8	FAN_SYS1_PRSNT_N	8	FAN_SYS2_PRSNT_N	8
LED_FAN_FAULT0_R	9	LED_FAN_FAULT1_R	9	LED_FAN_FAULT2_R	9
LED_FAN0	10	LED_FAN1	10	LED_FAN2	10
SYS_FAN 4		SYS_FAN 5		SYS_Fan 6 (not used)	
Signal Description	Pin#	Signal Description	Pin#	Signal Description	Pin#
FAN_TACH7_IN	1	FAN_TACH9_IN	1	FAN_TACH11_IN	1
FAN_IBMC_PWM3_R_BUF	2	FAN_IBMC_PWM4_R_BUF	2	FAN_IBMC_PWM5_R_BUF	2
P12V_FAN	3	P12V_FAN	3	P12V_FAN	3
P12V_FAN	4	P12V_FAN	4	P12V_FAN	4
FAN_TACH6_IN	5	FAN_TACH8_IN	5	FAN_TACH10_IN	5
GROUND	6	GROUND	6	GROUND	6
GROUND	7	GROUND	7	GROUND	7
FAN_SYS3_PRSNT_N	8	FAN_SYS4_PRSNT_N	8	FAN_SYS5_PRSNT_N	8
LED_FAN_FAULT3_R	9	LED_FAN_FAULT4_R	9	LED_FAN_FAULT5_R	9
LED_FAN3	10	LED_FAN4	10	LED_FAN5	10

4.4 FRUSDR Utility

The purpose of the embedded platform management and fan control systems is to monitor and control various system features, and to maintain an efficient operating environment. Platform management is also used to communicate system health to supported platform management software and support mechanisms. The FRUSDR utility is used to program the server board with platform specific environmental limits, configuration data, and the appropriate sensor data records (SDRs), for use by these management features.

The FRUSDR utility must be run as part of the initial platform integration process before it is deployed into a live operating environment. It must be run with the system fully configured and each time the system configuration changes.

The FRUSDR utility for the given server platform can be run as part of the Intel® Server Deployment Toolkit and Management DVD that ships with each Intel® server, or can be downloaded from http://www.intel.com/p/en_US/support.

Note: The embedded platform management system may not operate as expected if the platform is not updated with accurate system configuration data. The FRUSDR utility must be run with the system fully configured and each time the system configuration changes, for accurate system monitoring and event reporting.

5 System Storage and Peripheral Options

The Intel® Server System R1000JP product family has support for many storage device options, including:

- Hot Swap 2.5” Hard Disk Drives
- Hot Swap 3.5” Hard Disk Drives
- SATA Optical Drive

Support for different storage and peripheral device options will vary depending on the system SKU. This section will provide an overview of each available option.

5.1 2.5” Hard Disk Drive Support

The server is available with support for eight 2.5” hard disk drives as illustrated below:

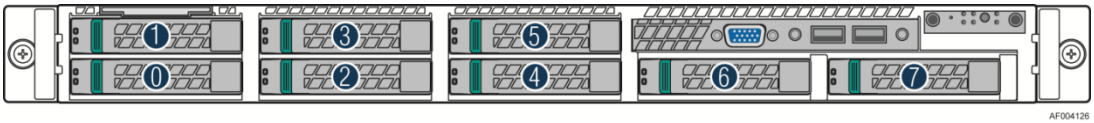


Figure 32. 2.5" Hard Drive Bay Drive Configuration

The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 2.5” hard disk drive is mounted to a drive carrier, allowing for hot swap extraction and insertion. Drive carriers have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.

Light pipes integrated into the drive tray assembly direct the light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.

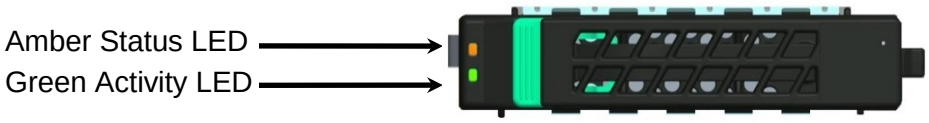


Figure 33. LED of HDD Carrier

Table 49. Drive Status LED States

Amber	Off	No access and no fault
	Solid On	Hard Drive Fault has occured
	Blink	RAID rebuild in progress (1 Hz), Identify (2 Hz)

Table 50. Drive Activity LED States

	Condition	Drive Type	Behavior
Green	Power on with no drive activity	SAS	LED stays on
		SATA	LED stays off
	Power on with drive activity	SAS	LED blinks off when processing a command
		SATA	LED blinks on when processing a command
	Power on and drive spun down	SAS	LED stays off
		SATA	LED stays off
	Power on and drive spinning up	SAS	LED blinks
		SATA	LED stays off

5.1.1 2.5" Drive Hot-Swap Backplane Overview

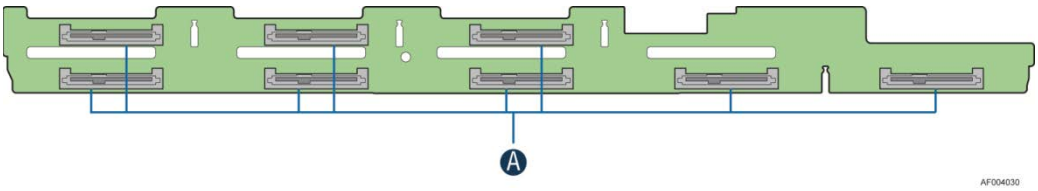
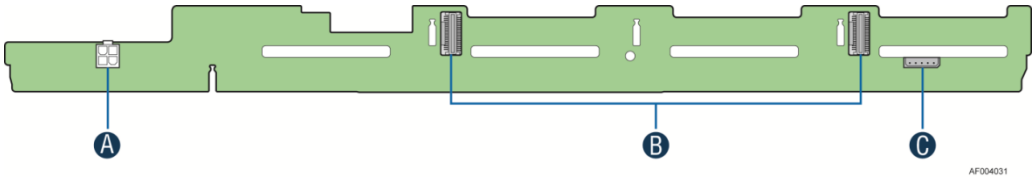


Figure 34. The Front side of 8 X 2.5" Hotswap Backplane

On the backside of each backplane are several connectors. The following illustration identifies each.



Label	Description
A	Power connector
B	4-port Mini-SAS cable connectors
C	SMBus*-In cable connector – From Server board

Figure 35. The Back Side of 8 X 2.5" Hotswap Backplane

A – Power Harness Connector – The backplane includes a 2x2 connector supplying power to the backplane. Power is routed to the backplane through a power cable harness from the server board.

B – Multi-port Mini-SAS Cable Connectors – The backplane includes two multi-port mini-SAS cable connectors, each providing I/O signals for four SAS/SATA hard drives on the backplane. Cables can be routed from matching connectors on the server board, add-in SAS/SATA RAID cards, or optionally installed SAS expander cards.

C – SMBus* Cable Connectors – The backplane includes a 1x5 cable connector used as a management interface to the server board.

5.1.2 Cypress* CY8C22545 Enclosure Management Controller

The backplane supports enclosure management using a Cypress* CY8C22545 Programmable System-on-Chip (PSoC*) device. The CY8C22545 drives the hard drive activity/fault LED, hard drive present signal, and controls hard drive power-up during system power-on.

5.2 3.5" Hard Disk Drive Support

The server is available with support for four 3.5" hard disk drives as illustrated below.

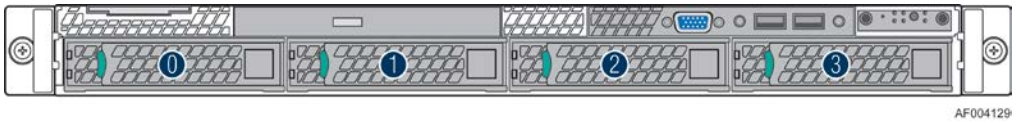
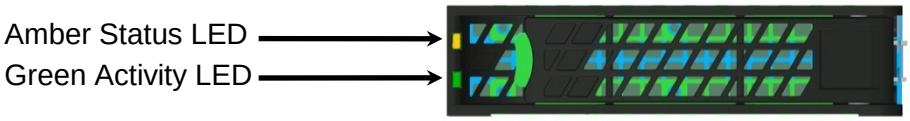


Figure 36. 3.5" Hard Drive Bay Configuration

The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 3.5" hard disk drive is mounted to a drive tray, allowing for hot swap extraction and insertion. Drive trays have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.

The hard drive carrier can also support 2.5" SSD. Light pipes integrated into the drive tray assembly direct the light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.



Amber	Off	No access and no fault
	Solid On	Hard Drive Fault has occured
	Blink	RAID rebuild in progress (1 Hz), Identify (2 Hz)

	Condition	Drive Type	Behavior
Green	Power on with no drive activity	SAS	LED stays on
		SATA	LED stays off
	Power on with drive activity	SAS	LED blinks off when processing a command
		SATA	LED blinks on when processing a command
	Power on and drive spun down	SAS	LED stays off
		SATA	LED stays off
	Power on and drive spinning up	SAS	LED blinks
		SATA	LED stays off

Figure 37. LED of HDD Carrier

5.2.1 3.5" Drive Hot-Swap Backplane Overview

On the front side of each back plane are mounted four hard disk drive interface connectors (A), each providing both power and I/O signals to attached hard disk drives.

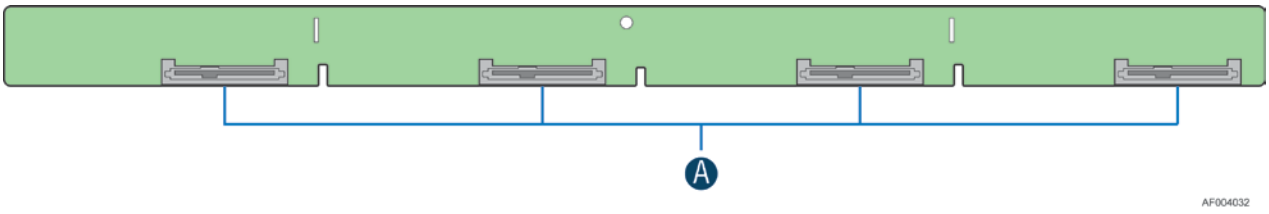
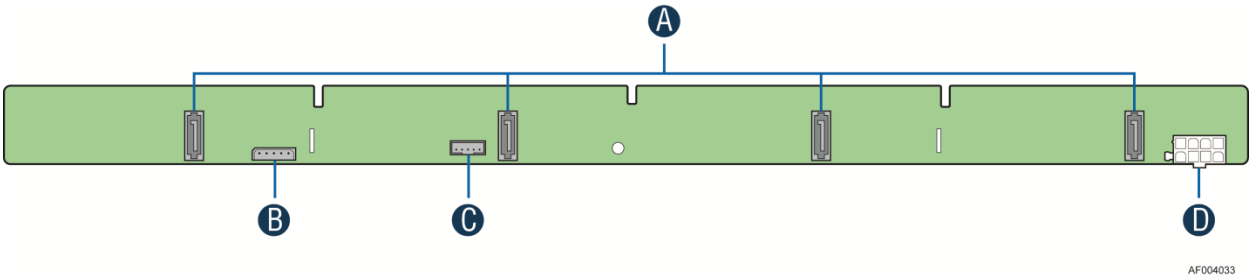


Figure 38. The front side of 4 x 3.5" Hotswap Backplane

On the backside of each backplane are several connectors. The following illustration identifies each.



Label	Description
A	7-pin SATA/SAS I/O connectors
B	SMBus*-In cable connector – From Server board
C	SGPIO connector
D	Power connector

Figure 39. The back side of 4 x 3.5" Hotswap Backplane

A – 7-pin SATA I/O Connectors – The backplane has four 7-pin SATA/SAS I/O connectors, one for each hard drive. A single multi-connector cable is routed from the backplane to a four port mini-SAS connector on the server board or other optionally installed SATA/SAS host bus adapter.

B – SMBus* Cable Connectors – The backplane includes a 1x5 cable connector used as a management interface to the server board.

C – SGPIO Cable Connector – The SGPIO connector is a management interface used to control the hard drive fault LEDs on the backplane. The SGPIO signals are routed through a multi-connectors cable that is routed to a four port mini-SAS connector on the server board or other optionally installed SATA/SAS host bus adapter.

D – Power Harness Connector - The backplane includes a 2x2 connector supplying power to the backplane. Power is routed to the backplane through a power cable harness from the server board.

5.2.2 Cypress* CY8C22545 Enclosure Management Controller

The backplanes support enclosure management using a Cypress* CY8C22545 Programmable System-on-Chip (PSoC*) device. The CY8C22545 drives the hard drive activity/fault LED, hard drive present signal, and controls hard drive power-up during the system power-on.

5.3 SATA DOM Support

The system has support for a vertical low profile InnoDisk* SATA Disk-on-Module (DOM) device. The SATA DOM plugs directly into the 7-pin AHCI SATA port on the server board, which provides both power and I/O signals.

Figure 40. InnoDisk* Low Profile SATA DOM

SATA DOM features include:

- Ultra Low Profile
- High speed and capacity
- Built-in VCC at pin 7

Note: Visit http://www.intel.com/p/en_US/support for a list of supported InnoDisk* SATA DOM parts.

Only SATA port0 can support SATA DOM.

6 Storage Controller Options Overview

The server platform supports many different embedded and add-in SATA/SAS controller to provide a large number of possible storage configurations. This section will provide an overview of the different options available.

6.1 Embedded SATA/SAS Controller support

Integrated on the server board is an Intel® C600 chipset that provides embedded storage support through two integrated controllers: AHCI and SCU.

The standard server board (with no additional storage options installed) will support up to six SATA ports:

- Two 6 Gb/sec SATA port routed from the AHCI controller SATA on board connectors
- Four 3 Gb/sec SATA ports routed from the AHCI controller to SATA on board connectors
- One mini-SAS connector labeled “SAS_0-3” to support SCU0.

With the addition of one of several available Intel® RAID C600 Upgrade Keys, the system is capable of supporting additional embedded SATA, SAS, and software RAID options. Upgrade keys install onto a 4-pin connector on the server board labeled “STOR_UPG_KEY”.

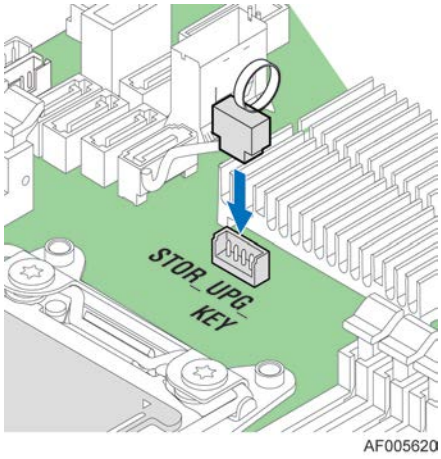


Figure 41. Insert a Caption

The following table identifies available upgrade key options and their supported features.

Table 51. Intel® RAID C600 Upgrade Key Options

Intel® RAID C600 Upgrade Key Options (Intel® Product Codes)	Key Color	Description
Default – No option key installed	**N/A**	4 Port SATA with Intel® ESRT RAID 0, 1, 10 and Intel® RSTe RAID 0, 1, 5, 10
RKSAS4	**Green**	4 Port SAS with Intel® ESRT2 RAID 0, 1, 10 and Intel® RSTe RAID 0, 1, 10
RKSAS4R5	**Yellow**	4 Port SAS with Intel® ESRT2 RAID 0, 1, 5, 10 and Intel® RSTe RAID 0, 1, 10

Additional information for the on-board RAID features and functionality can be found in the *Intel® RAID Software User's Guide* (Intel® document number D29305-020).

6.2 Embedded Software RAID Support

The system includes support for two embedded software RAID options:

- Intel® Embedded Server RAID Technology 2 (ESRT2) based on LSI* MegaRAID SW RAID technology
- Intel® Rapid Storage Technology (RSTe)

Using the <**F2**> BIOS Setup Utility, accessed during system POST, options are available to enable/disable SW RAID, and select which embedded software RAID option to use.

6.2.1 Intel® Embedded Server RAID Technology 2 (ESRT2)[1]

Features of the embedded software RAID option Intel® Embedded Server RAID Technology 2 (ESRT2) include the following:

- Based on LSI* MegaRAID Software Stack.
- Software RAID, with system providing memory and CPU utilization.
- Supported RAID Levels – 0, 1, 5, 10.
  - 4 and 8 Port SATA RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key.
  - 4 and 8 Port SAS RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key.
- Maximum drive support = 8.
  - **Note:** ESRT2 has no SAS Expander Support.
- Open Source Compliance = Binary Driver (includes Partial Source files).
  - Meta data is also recognized by MDRAID layer in Linux* (No direct Intel® support, not validated by Intel®)
- OS Support = Microsoft Windows 7*, Microsoft Windows 2008*, Microsoft Windows 2003*, RHEL*, SLES*, other Linux* variants using partial source builds.
- Utilities = Windows* GUI and CLI, Linux* GUI and CLI, DOS CLI, and EFI CLI.

6.2.2 Intel® Rapid Storage Technology (RSTe)[1]

Features of the embedded software RAID option Intel® Rapid Storage Technology (RSTe) include the following:

- Software RAID with system providing memory and CPU utilization.
- Supported RAID Levels – 0, 1, 5, 10.
  - 4-Port SATA RAID 5 available standard (no option key required).
  - 8-Port SATA RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key.
  - No SAS RAID 5 support.
- Maximum drive support = 32 (in arrays with 8 port SAS), 16 (in arrays with 4 port SAS), 128 (JBOD).
- Open Source Compliance = Yes (uses MDRAID).
- OS Support = Microsoft Windows 7*, Microsoft Windows 2008*, Microsoft Windows 2003*, RHEL* 1 and later, SLES*1, VMware* 5.x.
- Utilities = Microsoft Windows* GUI and CLI, Linux* CLI, DOS CLI, and EFI CLI.

  Note: No boot drive support to targets attached through SAS expander card.

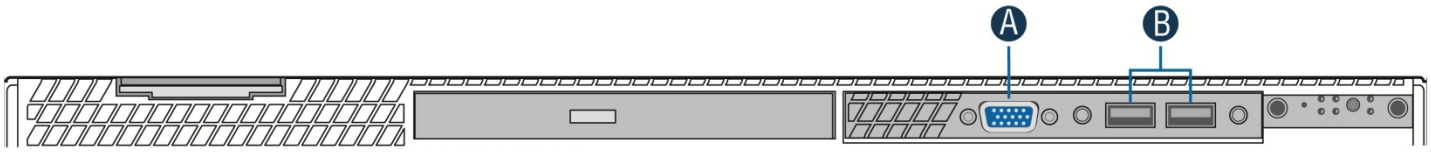
Note: See latest *Product Errata list* for support status. Product Errata are documented in the *Intel® Server Board S1600JP, Intel® Server System R1000JP, Monthly Specification Update* which can be downloaded from http://www.intel.com/p/en_US/support.

Visit http://www.intel.com/p/en_US/support for a list of supported operating systems.

7 Front Control Panel and I/O Panel Overview

On the front panel of all system configurations is a Control Panel providing push button system controls and LED indicators for several system features, and an I/O Panel providing USB ports and a video connector. This section describes the features and functions of both front panel options.

7.1 I/O Panel Features



Label	Description
A	Video connector
B	USB ports

Figure 42. Front I/O Panel Features

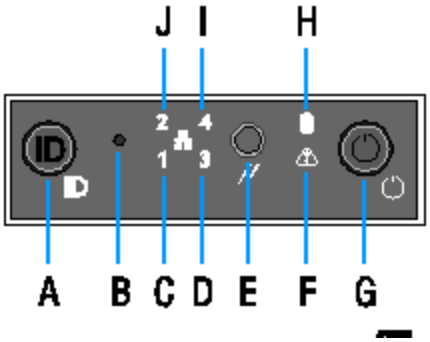
A – Video connector – The front I/O Panel video connector gives the option of attaching a monitor to the front of the system. When BIOS detects that a monitor is attached to the front video connector, it disables the video signals routed to the on-board video connector on the back of the system. Video resolutions from the front video connector may be lower than that of the rear on-board video connector. A short video cable should be used for best resolution. The front video connector is cabled to a 2x7 header on the server board labeled “FP Video”.

B – USB Ports – The front I/O panel includes two USB ports. The USB ports are cabled to a 2x5 connector on the server board labeled “FP USB”.

Note: On systems that support 8x2.5” hard drives, the I/O Panel can be replaced with a SATA optical drive.

7.2 Control Panel Features

The system includes a control panel that provides push button system controls and LED indicators for several system features. Depending on the hard drive configuration, the front control panel may come in either of two formats; however, both provide the same functionality. This section will provide a description for each front control panel feature.



Label	Description	Label	Description
A	System ID Button with Integrated LED	F	System Status LED
B	NMI Button (recessed, tool required for use)	G	Power/Sleep Button with Integrated LED
C	NIC-1 Activity LED	H	Hard Drive Activity LED
D	NIC-3 Activity LED	I	NIC-4 Activity LED
E	System Cold Reset Button	J	NIC-2 Activity LED

Figure 43. Front Control Panel Features

A – System ID Button w/Integrated LED – Toggles the integrated ID LED and the Blue server board ID LED on and off. The System ID LED is used to identify the system for maintenance when installed in a rack of similar server systems. The System ID LED can also be toggled on and off remotely using the *IPMI "Chassis Identify"* command which will cause the LED to blink for 15 seconds.

B – NMI Button – When the NMI button is pressed, it puts the server in a halt state and issues a non-maskable interrupt (NMI). This can be useful when performing diagnostics for a given issue where a memory download is necessary to help determine the cause of the problem. To prevent an inadvertent system halt, the actual NMI button is located behind the Front Control Panel faceplate where it is only accessible with the use of a small tipped tool like a pin or paper clip.

C, D, I, and J – Network Activity LEDs – The Front Control Panel includes an activity LED indicator for each on-board Network Interface Controller (NIC). When a network link is detected, the LED will turn on solid. The LED will blink once network activity occurs at a rate that is consistent with the amount of network activity that is occurring.

E – System Cold Reset Button – When pressed, this button will reboot and re-initialize the system.

F – System Status LED – The System Status LED is a bi-color (Green/Amber) indicator that shows the current health of the server system. The system provides two locations for this feature; one is located on the Front Control Panel, the other is located on the back edge of the server board, viewable from the back of the system. Both LEDs are tied together and will show the same state. The System Status LED states are driven by the on-board platform management sub-system. The following table provides a description of each supported LED state.

Table 52. System Status LED State Definitions

Color	State	Criticality	Description
Off	System is not operating	Not ready	1. System is powered off (AC and/or DC). 2. System is in EuP Lot6 Off Mode. 3. System is in S5 Soft-Off State. 4. System is in S4 Hibernate Sleep State.
Green	Solid on	Ok	Indicates that the System is running (in S0 State) and its status is 'Healthy'. The system is not exhibiting any errors. AC power is present and BMC has booted and manageability functionality is up and running.
Green	~1 Hz blink	Degraded - system is operating in a degraded state although still functional, or system is operating in a redundant state but with an impending failure warning	System degraded: 1. Redundancy loss, such as power-supply or fan. Applies only if the associated platform sub-system has redundancy capabilities. 2. Fan warning or failure when the number of fully operational fans is more than minimum number needed to cool the system. 3. Non-critical threshold crossed – Temperature (including HSBP temp), voltage, input power to power supply, output current for main power rail from power supply and Processor Thermal Control (Therm Ctrl) sensors. 4. Power supply predictive failure occurred while redundant power supply configuration was present. 5. Unable to use all of the installed memory (one or more DIMMs failed/disabled but functional memory remains available). 6. Correctable Errors over a threshold and migrating to a spare DIMM (memory sparing). This indicates that the user no longer has spared DIMMs indicating a redundancy lost condition. Corresponding DIMM LED lit. 7. Uncorrectable memory error has occurred in memory Mirroring Mode, causing Loss of Redundancy. 8. Correctable memory error threshold has been reached for a failing DDR3 DIMM when the system is operating in fully redundant RAS Mirroring Mode. 9. Battery failure. 10. BMC executing in uBoot. (Indicated by Chassis ID blinking at Blinking at 3Hz). System in degraded state (no manageability). BMC uBoot is running but has not transferred control to BMC Linux*. Server will be in this state 6-8 seconds after BMC reset while it pulls the Linux* image into flash 11. BMC booting Linux*. (Indicated by Chassis ID solid ON). System in degraded state (no manageability). Control has been passed from BMC uBoot to BMC Linux* itself. It will be in this state for ~10-~20 seconds. 12. BMC Watchdog has reset the BMC. 13. Power Unit sensor offset for configuration error is asserted. 14. HDD HSC is off-line or degraded.

Color	State	Criticality	Description
Amber	~1 Hz blink	Non-critical - System is operating in a degraded state with an impending failure warning, although still functioning	Non-fatal alarm – system is likely to fail: 1. Critical threshold crossed – Voltage, temperature (including HSBP temp), input power to power supply, output current for main power rail from power supply, and PROCHOT (Therm Ctrl) sensors. 2. VRD Hot asserted. 3. Minimum number of fans to cool the system not present or failed. 4. Hard drive fault. 5. Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies present). 6. In non-sparing and non-mirroring mode if the threshold of correctable errors is crossed within the window. 7. Correctable memory error threshold has been reached for a failing DDR3 DIMM when the system is operating in a non-redundant mode.
Amber	Solid on	Critical, non-recoverable – System is halted	Fatal alarm – system has failed or shutdown: 1. CPU CATERR signal asserted. 2. MSID mismatch detected (CATERR also asserts for this case). 3. CPU 1 is missing. 4. CPU Thermal Trip. 5. No power good – power fault. 6. DIMM failure when there is only 1 DIMM present and hence no good memory present[1]. 7. Runtime memory uncorrectable error in non-redundant mode. 8. DIMM Thermal Trip or equivalent. 9. SSB Thermal Trip or equivalent. 10. CPU ERR2 signal asserted. 11. BMC\Video memory test failed. (Chassis ID shows blue/solid-on for this condition). 12. Both uBoot BMC FW images are bad. (Chassis ID shows blue/solid-on for this condition). 13. 240VA fault. 14. Fatal Error in processor initialization: a. Processor family not identical. b. Processor model not identical. c. Processor core/thread counts not identical. d. Processor cache size not identical. e. Unable to synchronize processor frequency. f. Unable to synchronize QPI link frequency.

G – Power/Sleep Button – Toggles the system power on and off. This button also functions as a sleep button if enabled by an ACPI compliant operating system. Pressing this button will send a signal to the Integrated BMC, which will either power on or power off the system. The integrated LED is a single color (Green) and is capable of supporting different indicator states as defined in Table 53.

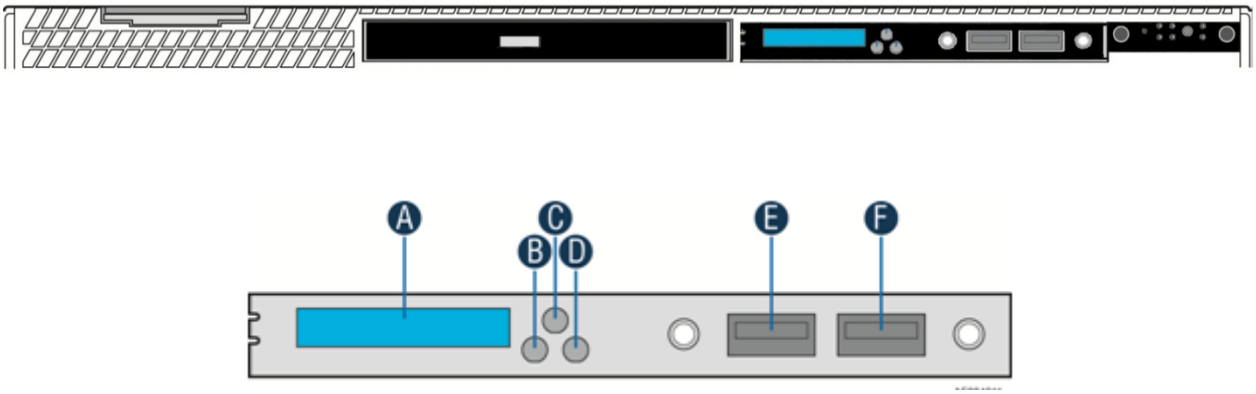
Table 53. Power/Sleep LED Functional States

State	Power Mode	LED	Description
Power-off	Non-ACPI	Off	System power is off, and the BIOS has not initialized the chipset.
Power-on	Non-ACPI	On	System power is on.
S5	ACPI	Off	Mechanical is off, and the operating system has not saved any context to the hard disk.
S4	ACPI	Off	Mechanical is off. The operating system has saved context to the hard disk.
S3-S1	ACPI	Slow blink1	DC power is still on. The operating system has saved context and gone into a level of low-power state.
S0	ACPI	Steady on	System and the operating system are up and running.

H – Drive Activity LED – The drive activity LED on the front panel indicates drive activity from the on-board hard disk controllers. The server board also provides a header giving access to this LED for add-in controllers.

8 Intel® Local Control Panel

The Intel® Local Control Panel option (Intel® Product Order Code – **AXXLCPANEL**) utilizes a combination of control buttons and LCD display to provide system accessibility and monitoring.



Label	Description	Functionality
A	LCD Display	one line 18 character display
B	Left Control Button	moves the cursor backward one step or one character
C	“Enter” Button	selects the menu item highlighted by the cursor
D	Right Control Button	moves the cursor forward one step or one character
E	USB 2.0 Port	
F	USB 2.0 Port	

Figure 44. Intel® Local Control Panel Option

The LCD (Local Control Display) is a one line character display that resides on the front panel of the chassis. It can display a maximum of 18 characters at a time. This device also contains three buttons (Left, Right, and Enter). The user can select the content that needs to be displayed on the LCD screen by operating these buttons.

8.1 LCD Functionality

The LCD device provides the following features:

- Displays a banner when the system is healthy. The default banner is the server name.
- Displays active error messages when the system is not healthy.
- Provides basic server management configuration.
- Provides the ability to see asset information without having to open the chassis.

The LCD display is menu driven. Based on the user’s selection, respective menu items are displayed. As soon as AC Power is applied to the system, the LCD panel displays faults detected while the system is on standby power prior to the DC power on. If there are no faults, a banner is displayed. By default, the banner is a text string which displays the “**Server Name**”. The “**Server Name**” is the value specified as the product name in the product FRU information in the BMC FRU. Users can set any of the parameters under the banner configuration menu as a banner string.

When the system's status is degraded, the corresponding active event will be displayed in place of the banner. During an error, the background color will be light amber in color. The LCD panel displays the event with the highest severity that is most recent and is currently active (that is, in an asserted state). For the case that there are multiple active events with the same severity, the most recent event will be displayed. The LCD panel returns to a light blue background when there are no longer any degraded, non-fatal, or fatal events active. The LCD panel shall operate in lock-step with the system status LED. For example, if the system is operating normally and an event occurs that results in the system status LED to blink green, then the LCD shall display the degraded event that triggered the systems status LED to blink.

Figure 45. LCP Background color during normal operation

Figure 46. LCP Background color during an error

If the user presses any button after the system is powered on, then the main menu will be displayed. The main menu contains "**Error**", "**View**", and "**Config**" items. Based on the user's selection, respective sub menu items will be displayed. At any point of time, if there is no user intervention for more than 10 minutes, a default banner (if there is no active error event in the system) or an error event will be displayed.

The following sections discuss the individual menu items. In the following sections, it is assumed that no active event exists during the LCD display. If any event (fatal or non-fatal) occurs that degrades the system's performance, the color of the LCD background turns into light amber. Even though all the contents (full text) are shown in the example screen shots in the following sections, by default, only the first 18 characters are displayed when a particular menu item is selected. The remaining text can be viewed by using right or left buttons.

8.2 Main Menu

If the user presses any button, when the Banner/Error screen is displayed, the following main menu will get displayed. Using left and right scroll buttons, the curser can be moved under any one of the following four menu items.

Figure 47. LCP Main Menu

If the user selects menu item, "**^**", then the LCD displays the previous screen, that is, Banner/Error string. Selecting the menu item means, moving the cursor under that item using left or right buttons and pressing enter button subsequently. In all the following sections (or for any screen shot), if the user presses "Enter" button, when the curser is under the symbol, "**^**", it takes to the previous screen. Selection of any of the menu items; "**Event**", "**View**", or "**Config**", leads the display to their corresponding screen shots and the details of these screen shots are given in the following sections.

8.3 Event Menu

In the "**Event**" menu, the LCD displays the following items. It displays all active error events in human readable text in chronological order. Informational events will not be displayed. There is no upper limit on the number of active events which can be displayed. The severity of the event will be indicated as either "**Degraded**", "**Non Fatal**", or "**Fatal**".

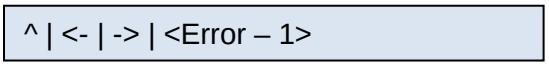


Figure 48. LCP Event Menu

The menu items, "**<-**"and "**->**" are used to traverse among the events. Selection of the menu item, "**<-**", displays the previous event and the item, "**->**", displays the next event in human readable format. By default, the first event after the last power on will be displayed. If there are no events after the last power on, then the fourth field is empty on the LCD screen.

By default, each error event scrolls automatically so that the entire error message can be read without pressing either the left or right scroll buttons. To stop auto scrolling, cursor has to be brought under the event message and the right button has to be pressed. Then the screen freezes. To start scrolling again right button has to be pressed when the cursor is under the event message. So, when the cursor is under event message, the right button decides whether to scroll or freeze the display of event message on the screen. When the cursor is under the event message, pressing enter button displays the failing FRU (if any) in an easily human readable format for that error event. Pressing enter button alternatively switches the display between error message and the failing FRU (if any) information of that error message alternatively. If there is no FRU device associated with that error, then enter button has no effect when the cursor is under the error message. Left button moves the cursor under the previous token or menu item that is "**->**".

8.4 View Menu

The following screen is displayed when "**View**" is selected from the main menu.

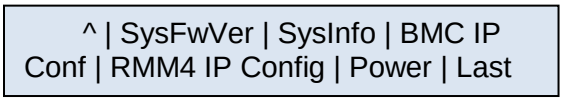


Figure 49. LCP View Menu

Based on the user's selection, details of the specific item will be displayed. The following sub sections explain the above menu items in detail.

8.4.1 System FW Version (SysFwVer)

Selecting "**SysFwVer**" item in the "View" menu displays the current firmware versions of the system as shown below:

Figure 50. System Firmware Versions Menu

This is a leaf node and there is no further traversal below this menu. User can only go to the previous screen by selecting the item, "**^**". This applies to all the items of "**View**" menu.

8.4.2 System Information (SysInfo)

Selecting "**SysInfo**" item in the "View" menu displays the Server's name, model, GUID, asset tag, and custom string. It is also a leaf node like above menu. The blanks in the following display will be replaced by their values.

^ | Server Name: ……. | Server Model: ….. | Asset Tag: ….. | Server GUID: …. | Custom String: ……..

Figure 51. System Information Menu

Each of the above fields is explained below:

a. **Server Name**: Value specified in the product name in the product FRU information in the main board BMC FRU.
b. **Server Model**: Value specified in the product part number in the product FRU information in the main board BMC FRU.
c. **Asset Tag**: Value specified in the product asset tag in the product FRU information in the main board BMC FRU.
d. **Server GUID**: System UUID stored by BIOS.
e. **Custom String**: Custom string placed by the OEM\end user.

8.4.3 BMC IP Configuration

Selecting "**BMC IP Conf**" item in the "**View**" menu displays the RMM4 IP configuration details. These details show whether the IP is configured using DHCP or Static, IP Address, Subnet Mask, and Gateway.

^ | DHCP (or Static) | IP Address: xxx.xxx.xxx.xxx | Subnet Mask: xxx.xxx.xxx.xxx | Gateway: xxx.xxx.xxx.xxx

Figure 52. LCP – BMC IP Configuration

8.4.4 RMM4 IP Configuration

Selecting "**RMM4 IP Conf**" item in the "**View**" menu displays the BMC IP configuration details. These details show whether the IP is configured using DHCP or Static, IP Address, Subnet Mask, and Gateway.

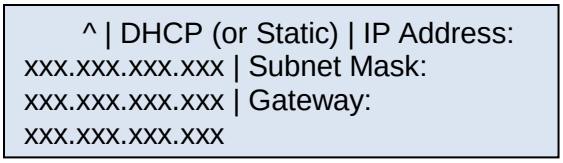


Figure 53. LCP – RMM4 IP Configuration

8.4.5 Power

Selecting "**Power**" item in the "**View**" menu displays the amount of AC power drawn by the system in Watts.

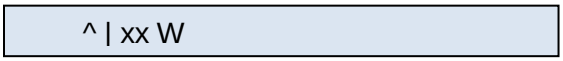


Figure 54. LCP – Power consumed by the System currently

8.4.6 Last Post Code (Last PC)

Selecting "**Last PC**" item in the "**View**" menu displays the last BIOS POST code in hexadecimal.

Figure 55. LCP – Last BIOS Post Code

8.5 Config Menu

If the user selects "**Config**" item in the main menu, then the following options will be displayed to configure.

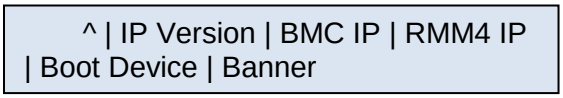


Figure 56. LCP – Configure Menu Items

The following sub-sections will explain individual items of the configuration menu.

8.5.1 IP Version

If the user selects "**IP Version**" in the "**Config**" menu, the following options will be displayed. Based the user's selection, firmware will set the IP Version as either IPv4 or IPv6.

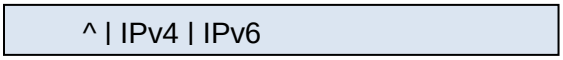


Figure 57. LCP – IP Version Configuration Screen

8.5.2 BMC IP

If the user selects "**BMC IP**" item in the "**Config**" menu, then the following options will be displayed.

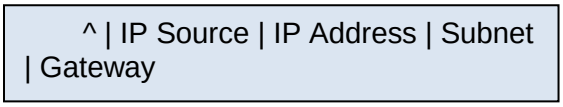


Figure 58. LCP – BMC IP Configuration Menu

Selection of the "**IP Source**" in the above menu, leads to the following screen. Based on the user's selection in the following menu, the firmware sets the BMC IP source as either DHCP or Static.

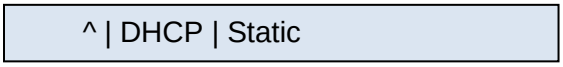


Figure 59. LCP – BMC IP Source Configuration Menu

If the user selects DHCP or if the existing IP source is DHCP, then the other menu items, that is, **IP Address**, **Subnet**, and **Gateway** are not configurable. If the user selects "**Static**" or if the existing setting is static for IP source, then the user is allowed to change the other menu items and the screen shot looks as follows:

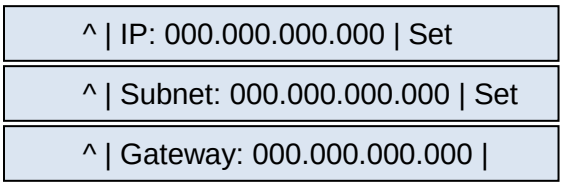


Figure 60. Screen shot for Configuring IP Address, Subnet Mask, and Gateway

By default, the cursor will be under the symbol, "**^**" and the IP address is displayed as 000.000.000.000. A right button will take the cursor to the first position (first 0) of the IP address. When the cursor is under the second menu item, the functionality of Left, Right, and Enter buttons is different from the previous screens. The second token consists of twelve 0 s' separated by '.' character in IP address format. The behaviors of these buttons are as follows when the cursor is under this item.

1. Left and Right buttons inside the second menu item traverses among the 0 positions within the same item.
2. If the cursor is under last position inside the second menu item, then a right button will move the cursor to the next item, that is, "**Set**".
3. If the cursor is under first position inside the second menu item, then a left button moves the cursor to the previous item, that is, "**^**".
4. First Enter button at any "0" position makes that position to be selected to increment or decrement the value at that position. The values allowed are between and including 0 and 9.

5. Any further Left or Right buttons will decrement or increment the value at that position.
6. Second Enter button at that position makes the cursor to be ready for moving left or right. Any further Left or Right moves the cursor to previous or next position respectively.
7. So, the Enter button is used to select a position at the first time and to leave the position at the second time.

The following state transition diagram explains the above steps pictorially, while setting an IP address using the LCD device. After entering an IP address, the user has to select "**Set**" item to set the entered IP address to the corresponding parameter (IP Address, Subnet Mask, or Gateway).

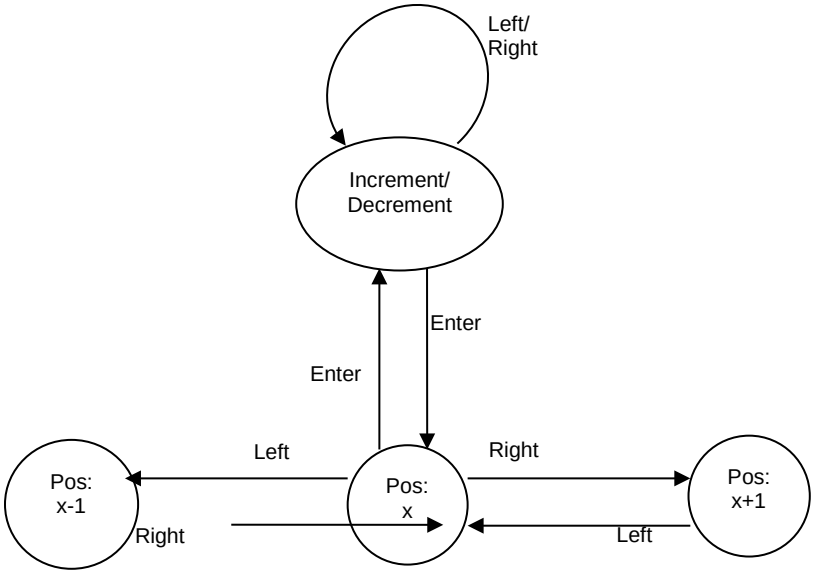


Figure 61. State transition diagram for setting IP Address

8.5.3 RMM4 IP

Same screen shots and the same description as that of the previous section ("**BMC IP**") are applicable for "**RMM4 IP**" configuration menu also.

8.5.4 Boot Device

If the user selects "**Boot Device**" in the "**Config**" menu, then the following options will be displayed. The selected item will be set as the next boot option and it will not be a permanent change.

```
     ^ | CD\DVD | Hard Drive | Network
Boot | EFI Shell
```

Figure 62. Boot options Configuration Menu

8.5.5 Banner

When the user selects "**Banner**" in the "**Config**" menu, the following options will be displayed. The selected item will be set as banner and the same will be displayed from next banner screen onwards.

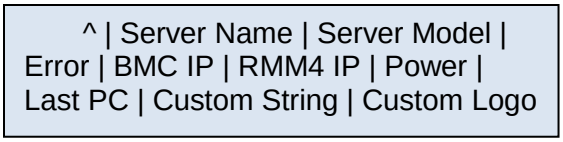


Figure 63. Banner Configuration Menu

Each of the menu items are explained below:

- **Server Name:** Displays the value specified in the product name in the product FRU information in the main board BMC FRU. The "**Server Name**" is the default banner.
- **Server Model:** Displays the value specified in the product part number in the product FRU information in the main board BMC FRU.
- **Error:** Displays the last active system event. The last active event may be degraded, non-critical, or critical only. It will not display an informational message. If the system is healthy, then it displays "**System Health Ok**".
- **BMC IP:** Displays the IPv4 or IPv6 address of BMC IP. If the BMC IP address is not configured, then nothing is displayed.
- **RMM4 IP:** Displays the IPv4 or IPv6 address of RMM4 dedicated LAN IP. If the RMM4 IP is not set or not present, then nothing is displayed.
- **Power:** Displays the current system power consumption in watts. The power consumed will be refreshed every minute.
- **Last PC:** Displays last BIOS post code.
- **Custom string:** Displays a customizable text string. The custom text string is modifiable through BIOS setup.
- **Custom Logo:** Displays a customizable bitmap logo. The OEM customized logo is programmed by the OEM and will be maintained during subsequent firmware updates.

9 PCI Riser Card Support

Intel® Server System R1304JP4OC, R1208JP4OC, R1208JP4TC, and R1304JP4TC include two riser cards on the server board (Intel® Product Order code- F1UJP1X16RISER and F1UJP2X8RISER). Intel® Server System R1208JP4GS and R1304JP4GS include two riser cards too (Intel® Product Order code- F1UJP2X8RISER and F1UJPGPURISER). Riser cards for the server are NOT interchangeable between riser slots. Another optional Intel® rIOM riser and carrier board kit is supported on Intel® Server System R1000JP family (Intel® Product order code- A1UJPRMM4IOM). This section will provide an overview of each available riser card and describe the server board features and architecture supporting them.

9.1 Architectural Overview of the Server Board Riser Slots

The server board includes three riser card slots labeled “PCIe Riser SLOT1”, “PCIe Riser Slot2”, and “PCIe Riser Slot3”. The following diagrams illustrate the general server board architecture supporting these three slots.

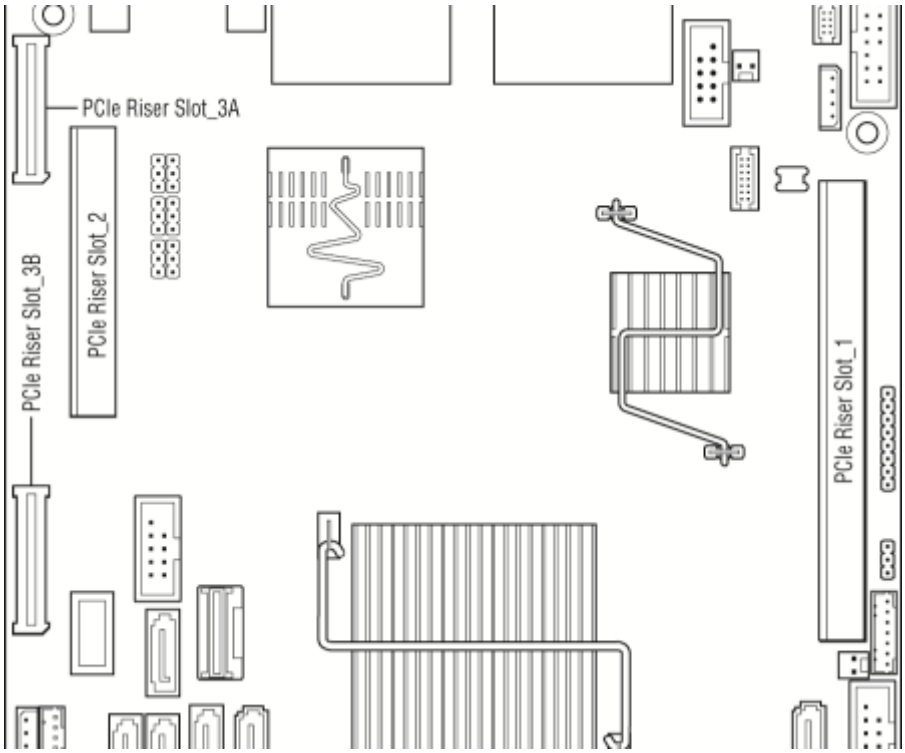


Figure 64. PCIe SLOT drawing

- SLOT1 on the board provides PCIe GenIII x16 mechanical with x16 from the processor.
- SLOT2 on the board provides PCI-e GenIII x8 mechanical.
- SLOT3 labeled “SLOT_3A” and “SLOT_3B” need to be used together to provide PCIe GenIII x16 mechanical and x16.

9.2 Riser Card Options – Riser Slot #1

All x16 PCIe bus lanes for Riser Slot #1 on the server board are routed from the processor. The riser card designed for Riser Slot #1 includes a single PCIe x16 (x16 lanes, x16 slot) add-in slot that can support a single low profile card. This card with Intel® Order product code - F1UJP1X16RISER) is integrated in all of the Intel® Server System R1000JP family.

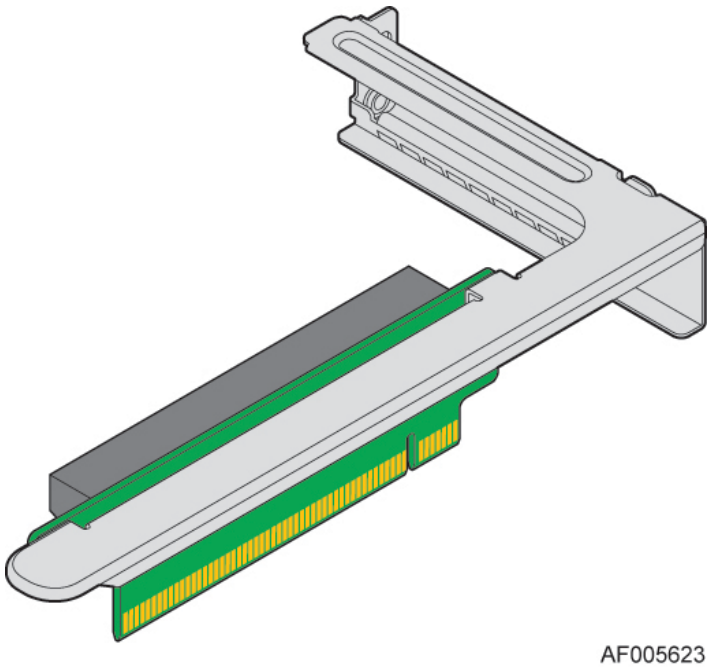


Figure 65. 1U Riser Card #1 drawing

9.3 Riser Card Options – Riser Slot #2

All x8 PCIe bus lanes for Riser Slot #2 on the server board are routed from the processor. The riser card designed for Riser Slot #2 includes a single PCIe x8 (x8 lanes, x8 slot) add-in slot that can support. The Riser with IOM carrier is provided as an accessory to the server system (Intel® Product Order Code- A1UJPRMM4IOM). The kit is not integrated in the system. It is combined with below functions:

- Provide PCI Express* x8 Gen 3 signals from riser
- Integrated 1GbE management port for Intel® Remote Management Module 4
- Support PCI-E* x4 based Intel® IO Module

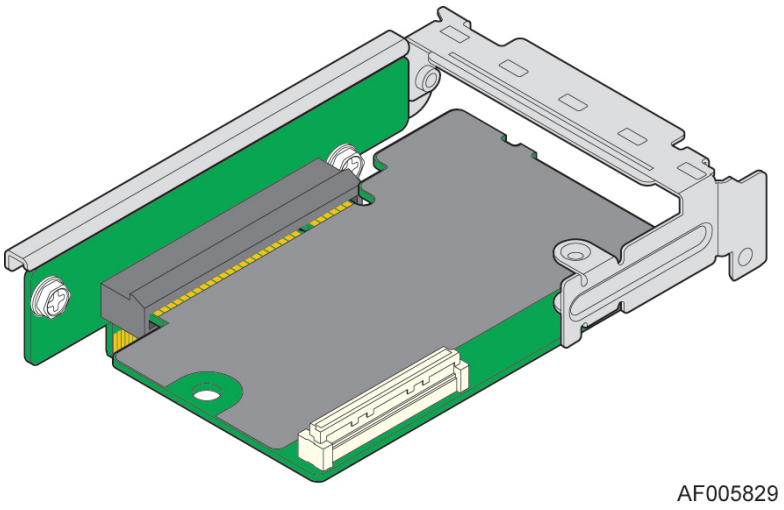


Figure 66. PCI Express* Riser with bracket and carrier board for Riser Slot 2

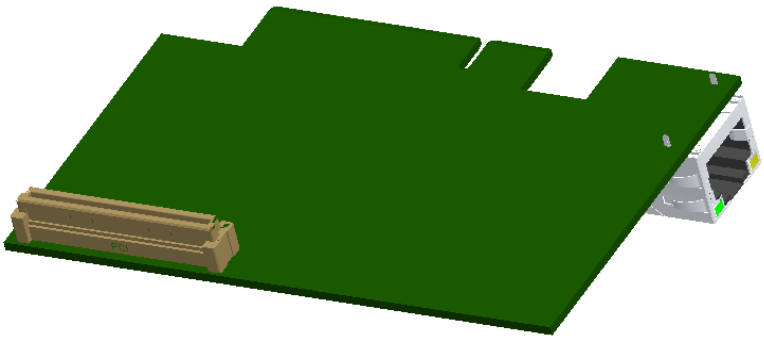


Figure 67. IOM Carrier

The 1GbE port is dedicated NIC port for RMM4 Lite module. It only works once the RMM4 Lite module is installed in the system. The LED of dedicated NIC port is following the below definition:

Table 54. Dedicated NIC Port LED Functionality

LED	Color	Condition	Functionality
Dedicated NIC Speed	Green	On	1Gbps mode
	Amber	On	100Mbps mode
		Off	10Mbps mode
Dedicated NIC Activity	Green	On	LAN link and no access
	Green	Blink	LAN access
		Off	Idle

Please get the installation steps from the *Intel® Server System R1000JP Family Service Guide* to assemble the riser, IOM carrier board, and IOM module.

9.4 Riser Card Options – Riser Slot #3

All x16 PCIe bus lanes for Riser Slot #3 on the server board are routed from the processor. There are two options for Riser Slot #3.

One option is to provide two slots in the riser with Intel® Product Order Code - F1UJP2X8RISER. The two slots in this riser provide one slot with x8 lanes x16 mechanical and one slot with x8 lanes and x8 mechanical. This riser card is included in the Intel® Server System R1304JP4OC, R1208JP4OC, R1208JP4TC, and R1304JP4TC.

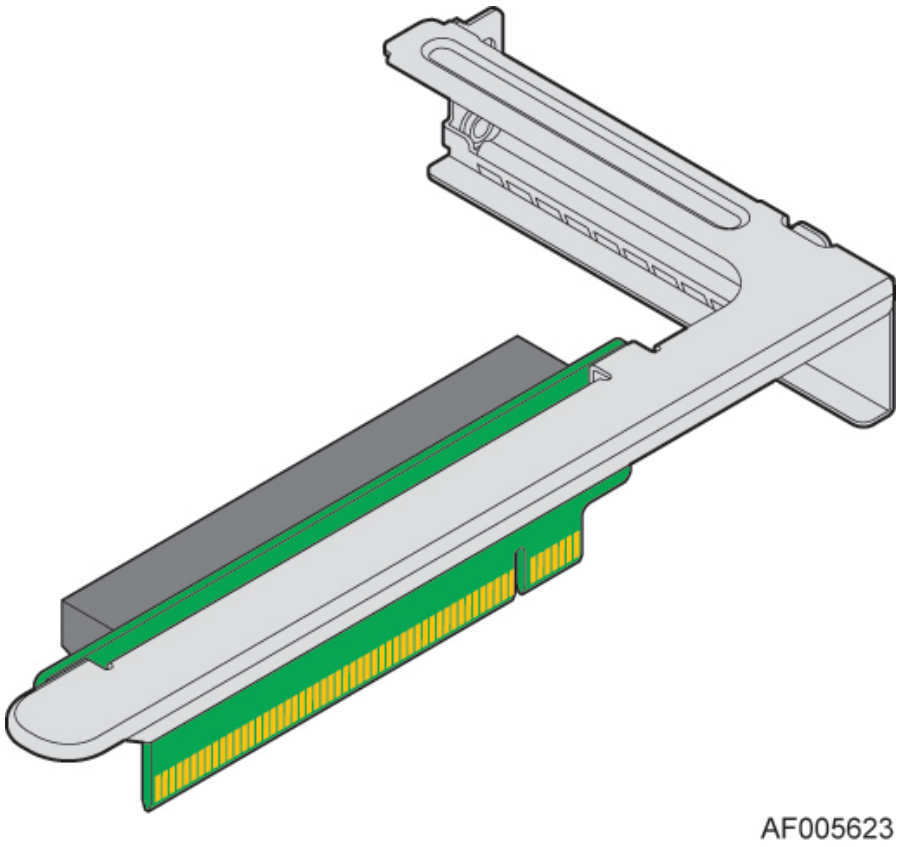


Figure 68. 1U 1SLOT Riser drawing

Another option is to provide one slot in the riser with x16 lanes x16 mechanical (Intel® Product Order Code - F1UJPMICRISER). This riser card provides the support to double width card. This riser card is included in the Intel® Server System R1208JP4GS and R1304JP4GS.

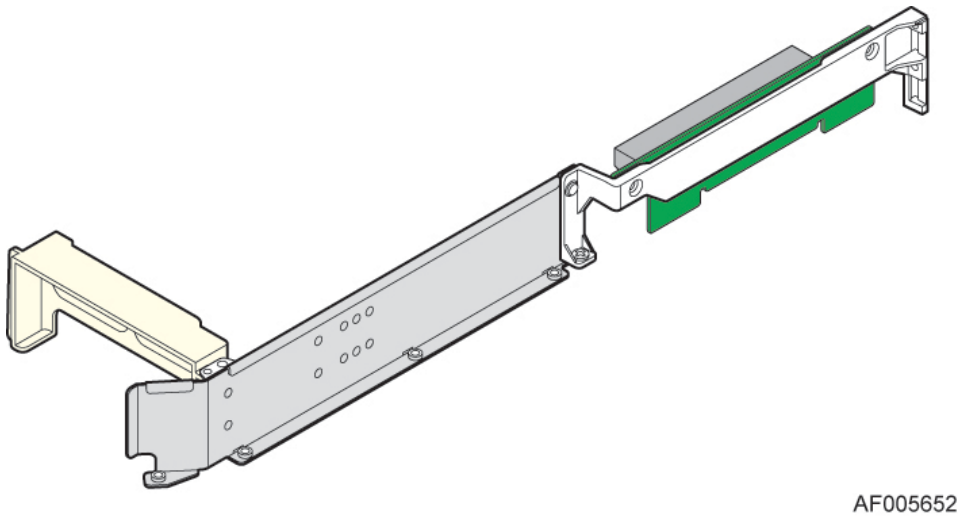


Figure 69. 1U Riser drawing with bracket

Please get the installation steps from the *Intel® Server System R1000JP Family Service Guide* to assemble the add-in video card.

Appendix A: Integration and Usage Tips

Before attempting to integrate and configure your system, you should reference this section, which provides a list of useful information.

- After the system is integrated with processors, memory, and peripheral devices, the FRUSDR utility **must** be run to load the proper Sensor Data Record data to the integrated Server Management subsystem. Failure to run this utility may prevent Server Management from accurately monitoring system health and may affect system performance. The FRUSDR utility for this server system can either be run from the Intel® Deployment CDROM that came with your system, or can be downloaded from the Intel® website referenced at the bottom of this page.
- To ensure the highest system reliability, make sure the latest system software is loaded on the server before deploying the system onto a live networking environment. This includes system BIOS, FRUSDR, BMC firmware, and hot-swap controller firmware. The system software can be updated using the Intel® Deployment CDROM that came with your system or can be downloaded from the Intel® website referenced at the bottom of this page.
- System fans are not hot-swappable.
- Only supported memory validated by Intel® should be used in this server system. A list of supported memory can be found in the *Intel® Server Board S1600JP Tested Memory List* which can be downloaded from the Intel® website referenced at the bottom of this page.
- This system supports the Intel® Xeon® processor E5-2600 / E5-2600 V2 series. You cannot use Intel® Xeon® processors not referenced on the supported processor list in this server system.
- You must use the CPU/memory air duct to maintain system thermals.
- To maintain system thermals, you must populate all hard drive bays with either a hard drive or drive blank.
- You must remove AC power from the system prior to opening the chassis for service.

You can download the latest system documentation, drivers, and system software from the Intel® Support website at http://www.intel.com/p/en_US/support/highlights/server/R1000JP.

Appendix B: POST Code LED Decoder

During the system boot process, the BIOS executes a number of platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the POST code to the POST Code Diagnostic LEDs on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, you can use the diagnostic LEDs to identify the last POST process executed.

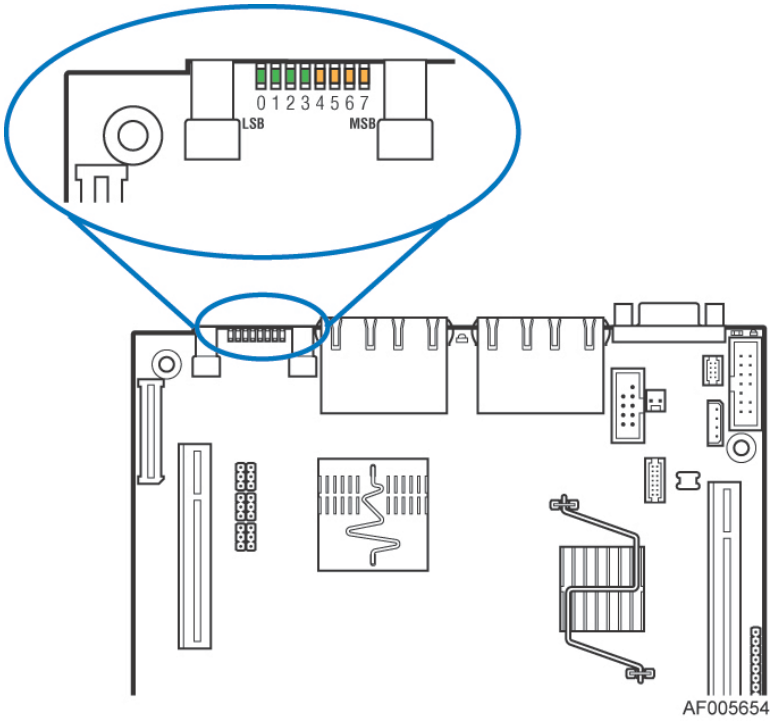


Figure 70. Diagnostic LED location

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

Table 55. POST Progress Code LED Example

LEDs	Upper Nibble AMBER LEDs				Lower Nibble GREEN LEDs			
	MSB							LSB
	LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
	8h	4h	2h	1h	8h	4h	2h	1h
Status	ON	OFF	ON	OFF	ON	ON	OFF	OFF
Results	1	0	1	0	1	1	0	0
	Ah				Ch			

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh.

Table 56. Diagnostic LED POST Code Decoder

Checkpoint	Diagnostic LED Decoder 1 = LED On, 0 = LED Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED #	#7	#6	#5	#4	#3	#2	#1	#0	
SEC Phase									
01h	0	0	0	0	0	0	0	1	First POST code after CPU reset.
02h	0	0	0	0	0	0	1	0	Microcode load begins.
03h	0	0	0	0	0	0	1	1	CRAM initialization begins.
04h	0	0	0	0	0	1	0	0	Pei Cache When Disabled.
05h	0	0	0	0	0	1	0	1	SEC Core At Power On Begin.
06h	0	0	0	0	0	1	1	0	Early CPU initialization during Sec Phase.
07h	0	0	0	0	0	1	1	1	Early SB initialization during Sec Phase.
08h	0	0	0	0	1	0	0	0	Early NB initialization during Sec Phase.
09h	0	0	0	0	1	0	0	1	End Of Sec Phase.
0Eh	0	0	0	0	1	1	1	0	Microcode Not Found.
0Fh	0	0	0	0	1	1	1	1	Microcode Not Loaded.
PEI Phase									
10h	0	0	0	1	0	0	0	0	PEI Core
11h	0	0	0	1	0	0	0	1	CPU PEIM
15h	0	0	0	1	0	1	0	1	NB PEIM
19h	0	0	0	1	1	0	0	1	SB PEIM
MRC Process Codes – MRC Progress Code Sequence is executed - See Table 63									
PEI Phase continued…									
31h	0	0	1	1	0	0	0	1	Memory Installed
32h	0	0	1	1	0	0	1	0	CPU PEIM (Cpu Init)
33h	0	0	1	1	0	0	1	1	CPU PEIM (Cache Init)
34h	0	0	1	1	0	1	0	0	CPU PEIM (BSP Select)
35h	0	0	1	1	0	1	0	1	CPU PEIM (AP Init)
36h	0	0	1	1	0	1	1	0	CPU PEIM (CPU SMM Init)
4Fh	0	1	0	0	1	1	1	1	Dxe IPL started
DXE Phase									
60h	0	1	1	0	0	0	0	0	DXE Core started
61h	0	1	1	0	0	0	0	1	DXE NVRAM Init
62h	0	1	1	0	0	0	1	0	SB RUN Init
63h	0	1	1	0	0	0	1	1	Dxe CPU Init
68h	0	1	1	0	1	0	0	0	DXE PCI Host Bridge Init
69h	0	1	1	0	1	0	0	1	DXE NB Init
6Ah	0	1	1	0	1	0	1	0	DXE NB SMM Init
70h	0	1	1	1	0	0	0	0	DXE SB Init
71h	0	1	1	1	0	0	0	1	DXE SB SMM Init
72h	0	1	1	1	0	0	1	0	DXE SB devices Init
78h	0	1	1	1	1	0	0	0	DXE ACPI Init
79h	0	1	1	1	1	0	0	1	DXE CSM Init
90h	1	0	0	1	0	0	0	0	DXE BDS Started
91h	1	0	0	1	0	0	0	1	DXE BDS connect drivers
92h	1	0	0	1	0	0	1	0	DXE PCI Bus begin
93h	1	0	0	1	0	0	1	1	DXE PCI Bus HPC Init
94h	1	0	0	1	0	1	0	0	DXE PCI Bus enumeration
95h	1	0	0	1	0	1	0	1	DXE PCI Bus resource requested
96h	1	0	0	1	0	1	1	0	DXE PCI Bus assign resource
97h	1	0	0	1	0	1	1	1	DXE CON_OUT connect
98h	1	0	0	1	1	0	0	0	DXE CON_IN connect
99h	1	0	0	1	1	0	0	1	DXE SIO Init
9Ah	1	0	0	1	1	0	1	0	DXE USB start

Checkpoint	Diagnostic LED Decoder 1 = LED On, 0 = LED Off								
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED #	#7	#6	#5	#4	#3	#2	#1	#0	Description
9Bh	1	0	0	1	1	0	1	1	DXE USB reset
9Ch	1	0	0	1	1	1	0	0	DXE USB detect
9Dh	1	0	0	1	1	1	0	1	DXE USB enable
A1h	1	0	1	0	0	0	0	1	DXE IDE begin
A2h	1	0	1	0	0	0	1	0	DXE IDE reset
A3h	1	0	1	0	0	0	1	1	DXE IDE detect
A4h	1	0	1	0	0	1	0	0	DXE IDE enable
A5h	1	0	1	0	0	1	0	1	DXE SCSI begin
A6h	1	0	1	0	0	1	1	0	DXE SCSI reset
A7h	1	0	1	0	0	1	1	1	DXE SCSI detect
A8h	1	0	1	0	1	0	0	0	DXE SCSI enable
A9h	1	0	1	0	1	0	0	1	DXE verifying SETUP password
ABh	1	0	1	0	1	0	1	1	DXE SETUP start
ACh	1	0	1	0	1	1	0	0	DXE SETUP input wait
ADh	1	0	1	0	1	1	0	1	DXE Ready to Boot
AEh	1	0	1	0	1	1	1	0	DXE Legacy Boot
AFh	1	0	1	0	1	1	1	1	DXE Exit Boot Services
B0h	1	0	1	1	0	0	0	0	RT Set Virtual Address Map Begin
B1h	1	0	1	1	0	0	0	1	RT Set Virtual Address Map End
B2h	1	0	1	1	0	0	1	0	DXE Legacy Option ROM init
B3h	1	0	1	1	0	0	1	1	DXE Reset system
B4h	1	0	1	1	0	1	0	0	DXE USB Hot plug
B5h	1	0	1	1	0	1	0	1	DXE PCI BUS Hot plug
B6h	1	0	1	1	0	1	1	0	DXE NVRAM cleanup
B7h	1	0	1	1	0	1	1	1	DXE Configuration Reset
00h	0	0	0	0	0	0	0	0	INT19
S3 Resume									
E0h	1	1	0	1	0	0	0	0	S3 Resume PEIM (S3 started)
E1h	1	1	0	1	0	0	0	1	S3 Resume PEIM (S3 boot script)
E2h	1	1	0	1	0	0	1	0	S3 Resume PEIM (S3 Video Repost)
E3h	1	1	0	1	0	0	1	1	S3 Resume PEIM (S3 OS wake)
BIOS Recovery									
F0h	1	1	1	1	0	0	0	0	PEIM which detected forced Recovery condition
F1h	1	1	1	1	0	0	0	1	PEIM which detected User Recovery condition
F2h	1	1	1	1	0	0	1	0	Recovery PEIM (Recovery started)
F3h	1	1	1	1	0	0	1	1	Recovery PEIM (Capsule found)
F4h	1	1	1	1	0	1	0	0	Recovery PEIM (Capsule loaded)

POST Memory Initialization MRC Diagnostic Codes

There are two types of POST Diagnostic Codes displayed by the MRC during memory initialization; Progress Codes and Fatal Error Codes.

The MRC Progress Codes are displays to the Diagnostic LEDs that show the execution point in the MRC operational path at each step.

Table 57. MRC Progress Codes

Diagnostic LED Decoder 1 = LED On, 0 = LED Off Upper Nibble MSB 8h	Lower Nibble 4h	2h	1h	8h	4h	2h	LSB 1h		Description
#7	#6	#5	#4	#3	#2	#1	#0		
MRC Progress Codes									
B0h	1	0	1	1	0	0	0	0	Detect DIMM population
B1h	1	0	1	1	0	0	0	1	Set DDR3 frequency
B2h	1	0	1	1	0	0	1	0	Gather remaining SPD data
B3h	1	0	1	1	0	0	1	1	Program registers on the memory controller level
B4h	1	0	1	1	0	1	0	0	Evaluate RAS modes and save rank information
B5h	1	0	1	1	0	1	0	1	Program registers on the channel level
B6h	1	0	1	1	0	1	1	0	Perform the JEDEC defined initialization sequence
B7h	1	0	1	1	0	1	1	1	Train DDR3 ranks
B8h	1	0	1	1	1	0	0	0	Initialize CLTT/OLTT
B9h	1	0	1	1	1	0	0	1	Hardware memory test and init
BAh	1	0	1	1	1	0	1	0	Execute software memory init
BBh	1	0	1	1	1	0	1	1	Program memory map and interleaving
BCh	1	0	1	1	1	1	0	0	Program RAS configuration
BFh	1	0	1	1	1	1	1	1	MRC is done

Memory Initialization at the beginning of POST includes multiple functions, including: discovery, channel training, validation that the DIMM population is acceptable and functional, initialization of the IMC and other hardware settings, and initialization of applicable RAS configurations.

When a major memory initialization error occurs and prevents the system from booting with data integrity, a beep code is generated, the MRC will display a fatal error code on the diagnostic LEDs, and a system halt command is executed. Fatal MRC error halts do NOT change the state of the System Status LED, and they do NOT get logged as SEL events. The following table lists all MRC fatal errors that are displayed to the Diagnostic LEDs.

Table 58. MRC Fatal Error Codes

Checkpoint	Diagnostic LED Decoder 1 = LED On, 0 = LED Off Upper Nibble MSB 8h	4h	2h	1h	Lower Nibble 8h	4h	2h	LSB 1h	Description
LED	#7	#6	#5	#4	#3	#2	#1	#0	
MRC Fatal Error Codes									
E8h	1	1	1	0	1	0	0	0	No usable memory error 01h = No memory was detected through SPD read, or invalid config that causes no operable memory. 02h = Memory DIMMs on all channels of all sockets are disabled due to hardware memtest error.

Checkpoint	Diagnostic LED Decoder								Description
	1 = LED On, 0 = LED Off								
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
									3h = No memory installed. All channels are disabled.
E9h	1	1	1	0	1	0	0	1	Memory is locked by Intel® Trusted Execution Technology and is inaccessible
EAh	1	1	1	0	1	0	1	0	DDR3 channel training error 01h = Error on read DQ/DQS (Data/Data Strobe) init 02h = Error on Receive Enable 3h = Error on Write Leveling 04h = Error on write DQ/DQS (Data/Data Strobe
EBh	1	1	1	0	1	0	1	1	Memory test failure 01h = Software memtest failure. 02h = Hardware memtest failed. 03h = Hardware Memtest failure in Lockstep Channel mode requiring a channel to be disabled. *This is a fatal error which requires a reset and calling MRC with a different RAS mode to retry.*
EDh	1	1	1	0	1	1	0	1	DIMM configuration population error 01h = Different DIMM types (UDIMM, RDIMM, LRDIMM) are detected installed in the system. 02h = Violation of DIMM population rules. 03h = The third DIMM slot cannot be populated when QR DIMMs are installed. 04h = UDIMMs are not supported in the third DIMM slot. 05h = Unsupported DIMM Voltage.
EFh	1	1	1	0	1	1	1	1	Indicates a CLTT table structure error

Appendix C: POST Code Errors

Whenever possible, the BIOS outputs the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The Response section in the following table is divided into three types:

- **No Pause:** The message is displayed on the local Video screen during POST or in the Error Manager. The system continues booting with a degraded state. The user may want to replace the erroneous unit. The setup POST error Pause setting does not have any effect with this error.
- **Pause:** The message is displayed on the Error Manager screen, and an error is logged to the SEL. The setup POST error Pause setting determines whether the system pauses to the Error Manager for this type of error, where the user can take immediate corrective action or choose to continue booting.
- **Halt:** The message is displayed on the Error Manager screen, an error is logged to the SEL, and the system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system. The setup POST error Pause setting does not have any effect with this error.

Table 59. POST Error Message and Handling

Error Code	Error Message	Response
0012	System RTC date/time not set	Major
0048	Password check failed	Major
113	Fixed media not detected	Major
0140	PCI component encountered a PERR error	Major
0141	PCI resource conflict	Major
0146	PCI out of resources error	Major
0191	Processor core/thread count mismatch detected	Fatal
0192	Processor cache size mismatch detected	Fatal
0194	Processor family mismatch detected	Fatal
0195	Processor Intel(R) QPI link frequencies unable to synchronize	Fatal
0196	Processor model mismatch detected	Fatal
0197	Processor frequencies unable to synchronize	Fatal
5220	BIOS Settings reset to default settings	Major
5221	Passwords cleared by jumper	Major
5224	Password clear jumper is Set	Major
8130	Processor 01 disabled	Major
8131	Processor 02 disabled	Major
8132	Processor 03 disabled	Major

Error Code	Error Message	Response
8133	Processor 04 disabled	Major
8160	Processor 01 unable to apply microcode update	Major
8161	Processor 02 unable to apply microcode update	Major
8162	Processor 03 unable to apply microcode update	Major
8163	Processor 04 unable to apply microcode update	Major
8170	Processor 01 failed Self Test (BIST)	Major
8171	Processor 02 failed Self Test (BIST)	Major
8172	Processor 03 failed Self Test (BIST)	Major
8173	Processor 04 failed Self Test (BIST)	Major
8180	Processor 01 microcode update not found	Minor
8181	Processor 02 microcode update not found	Minor
8182	Processor 03 microcode update not found	Minor
8183	Processor 04 microcode update not found	Minor
8190	Watchdog timer failed on last boot	Major
8198	OS boot watchdog timer failure	Major
8300	Baseboard management controller failed self test	Major
8305	Hot Swap Controller failure	Major
83A0	Management Engine (ME) failed self test	Major
83A1	Management Engine (ME) Failed to respond.	Major
84F2	Baseboard management controller failed to respond	Major
84F3	Baseboard management controller in update mode	Major
84F4	Sensor data record empty	Major
84FF	System event log full	Minor
8500	Memory component could not be configured in the selected RAS mode	Major
8501	DIMM Population Error	Major
8520	DIMM_A1 failed test/initialization	Major
8521	DIMM_A2 failed test/initialization	Major
8522	DIMM_A3 failed test/initialization	Major
8523	DIMM_B1 failed test/initialization	Major
8524	DIMM_B2 failed test/initialization	Major
8525	DIMM_B3 failed test/initialization	Major
8526	DIMM_C1 failed test/initialization	Major
8527	DIMM_C2 failed test/initialization	Major
8528	DIMM_C3 failed test/initialization	Major
8529	DIMM_D1 failed test/initialization	Major
852A	DIMM_D2 failed test/initialization	Major
852B	DIMM_D3 failed test/initialization	Major
852C	DIMM_E1 failed test/initialization	Major
852D	DIMM_E2 failed test/initialization	Major
852E	DIMM_E3 failed test/initialization	Major
852F	DIMM_F1 failed test/initialization	Major

Error Code	Error Message	Response
8530	DIMM_F2 failed test/initialization	Major
8531	DIMM_F3 failed test/initialization	Major
8532	DIMM_G1 failed test/initialization	Major
8533	DIMM_G2 failed test/initialization	Major
8534	DIMM_G3 failed test/initialization	Major
8535	DIMM_H1 failed test/initialization	Major
8536	DIMM_H2 failed test/initialization	Major
8537	DIMM_H3 failed test/initialization	Major
8538	DIMM_J1 failed test/initialization	Major
8539	DIMM_J2 failed test/initialization	Major
853A	DIMM_J3 failed test/initialization	Major
853B	DIMM_K1 failed test/initialization	Major
853C	DIMM_K2 failed test/initialization	Major
853D	DIMM_K3 failed test/initialization	Major
853E	DIMM_L1 failed test/initialization	Major
853F (Go to 85C0)	DIMM_L2 failed test/initialization	Major
8540	DIMM_A1 disabled	Major
8541	DIMM_A2 disabled	Major
8542	DIMM_A3 disabled	Major
8543	DIMM_B1 disabled	Major
8544	DIMM_B2 disabled	Major
8545	DIMM_B3 disabled	Major
8546	DIMM_C1 disabled	Major
8547	DIMM_C2 disabled	Major
8548	DIMM_C3 disabled	Major
8549	DIMM_D1 disabled	Major
854A	DIMM_D2 disabled	Major
854B	DIMM_D3 disabled	Major
854C	DIMM_E1 disabled	Major
854D	DIMM_E2 disabled	Major
854E	DIMM_E3 disabled	Major
854F	DIMM_F1 disabled	Major
8550	DIMM_F2 disabled	Major
8551	DIMM_F3 disabled	Major
8552	DIMM_G1 disabled	Major
8553	DIMM_G2 disabled	Major
8554	DIMM_G3 disabled	Major
8555	DIMM_H1 disabled	Major
8556	DIMM_H2 disabled	Major
8557	DIMM_H3 disabled	Major

Error Code	Error Message	Response
8558	DIMM_J1 disabled	Major
8559	DIMM_J2 disabled	Major
855A	DIMM_J3 disabled	Major
855B	DIMM_K1 disabled	Major
855C	DIMM_K2 disabled	Major
855D	DIMM_K3 disabled	Major
855E	DIMM_L1 disabled	Major
855F (Go to 85D0)	DIMM_L2 disabled	Major
8560	DIMM_A1 encountered a Serial Presence Detection (SPD) failure	Major
8561	DIMM_A2 encountered a Serial Presence Detection (SPD) failure	Major
8562	DIMM_A3 encountered a Serial Presence Detection (SPD) failure	Major
8563	DIMM_B1 encountered a Serial Presence Detection (SPD) failure	Major
8564	DIMM_B2 encountered a Serial Presence Detection (SPD) failure	Major
8565	DIMM_B3 encountered a Serial Presence Detection (SPD) failure	Major
8566	DIMM_C1 encountered a Serial Presence Detection (SPD) failure	Major
8567	DIMM_C2 encountered a Serial Presence Detection (SPD) failure	Major
8568	DIMM_C3 encountered a Serial Presence Detection (SPD) failure	Major
8569	DIMM_D1 encountered a Serial Presence Detection (SPD) failure	Major
856A	DIMM_D2 encountered a Serial Presence Detection (SPD) failure	Major
856B	DIMM_D3 encountered a Serial Presence Detection (SPD) failure	Major
856C	DIMM_E1 encountered a Serial Presence Detection (SPD) failure	Major
856D	DIMM_E2 encountered a Serial Presence Detection (SPD) failure	Major
856E	DIMM_E3 encountered a Serial Presence Detection (SPD) failure	Major
856F	DIMM_F1 encountered a Serial Presence Detection (SPD) failure	Major
8570	DIMM_F2 encountered a Serial Presence Detection (SPD) failure	Major
8571	DIMM_F3 encountered a Serial Presence Detection (SPD) failure	Major
8572	DIMM_G1 encountered a Serial Presence Detection (SPD) failure	Major
8573	DIMM_G2 encountered a Serial Presence Detection (SPD) failure	Major
8574	DIMM_G3 encountered a Serial Presence Detection (SPD) failure	Major
8575	DIMM_H1 encountered a Serial Presence Detection (SPD) failure	Major
8576	DIMM_H2 encountered a Serial Presence Detection (SPD) failure	Major
8577	DIMM_H3 encountered a Serial Presence Detection (SPD) failure	Major
8578	DIMM_J1 encountered a Serial Presence Detection (SPD) failure	Major
8579	DIMM_J2 encountered a Serial Presence Detection (SPD) failure	Major
857A	DIMM_J3 encountered a Serial Presence Detection (SPD) failure	Major
857B	DIMM_K1 encountered a Serial Presence Detection (SPD) failure	Major
857C	DIMM_K2 encountered a Serial Presence Detection (SPD) failure	Major
857D	DIMM_K3 encountered a Serial Presence Detection (SPD) failure	Major
857E	DIMM_L1 encountered a Serial Presence Detection (SPD) failure	Major
857F (Go to 85E0)	DIMM_L2 encountered a Serial Presence Detection (SPD) failure	Major

Error Code	Error Message	Response
85C0	DIMM_L3 failed test/initialization	Major
85C1	DIMM_M1 failed test/initialization	Major
85C2	DIMM_M2 failed test/initialization	Major
85C3	DIMM_M3 failed test/initialization	Major
85C4	DIMM_N1 failed test/initialization	Major
85C5	DIMM_N2 failed test/initialization	Major
85C6	DIMM_N3 failed test/initialization	Major
85C7	DIMM_P1 failed test/initialization	Major
85C8	DIMM_P2 failed test/initialization	Major
85C9	DIMM_P3 failed test/initialization	Major
85CA	DIMM_R1 failed test/initialization	Major
85CB	DIMM_R2 failed test/initialization	Major
85CC	DIMM_R3 failed test/initialization	Major
85CD	DIMM_T1 failed test/initialization	Major
85CE	DIMM_T2 failed test/initialization	Major
85CF	DIMM_T3 failed test/initialization	Major
85D0	DIMM_L3 disabled	Major
85D1	DIMM_M1 disabled	Major
85D2	DIMM_M2 disabled	Major
85D3	DIMM_M3 disabled	Major
85D4	DIMM_N1 disabled	Major
85D5	DIMM_N2 disabled	Major
85D6	DIMM_N3 disabled	Major
85D7	DIMM_P1 disabled	Major
85D8	DIMM_P2 disabled	Major
85D9	DIMM_P3 disabled	Major
85DA	DIMM_R1 disabled	Major
85DB	DIMM_R2 disabled	Major
85DC	DIMM_R3 disabled	Major
85DD	DIMM_T1 disabled	Major
85DE	DIMM_T2 disabled	Major
85DF	DIMM_T3 disabled	Major
85E0	DIMM_L3 encountered a Serial Presence Detection (SPD) failure	Major
85E1	DIMM_M1 encountered a Serial Presence Detection (SPD) failure	Major
85E2	DIMM_M2 encountered a Serial Presence Detection (SPD) failure	Major
85E3	DIMM_M3 encountered a Serial Presence Detection (SPD) failure	Major
85E4	DIMM_N1 encountered a Serial Presence Detection (SPD) failure	Major
85E5	DIMM_N2 encountered a Serial Presence Detection (SPD) failure	Major
85E6	DIMM_N3 encountered a Serial Presence Detection (SPD) failure	Major
85E7	DIMM_P1 encountered a Serial Presence Detection (SPD) failure	Major
85E8	DIMM_P2 encountered a Serial Presence Detection (SPD) failure	Major

Error Code	Error Message	Response
85E9	DIMM_P3 encountered a Serial Presence Detection (SPD) failure	Major
85EA	DIMM_R1 encountered a Serial Presence Detection (SPD) failure	Major
85EB	DIMM_R2 encountered a Serial Presence Detection (SPD) failure	Major
85EC	DIMM_R3 encountered a Serial Presence Detection (SPD) failure	Major
85ED	DIMM_T1 encountered a Serial Presence Detection (SPD) failure	Major
85EE	DIMM_T2 encountered a Serial Presence Detection (SPD) failure	Major
85EF	DIMM_T3 encountered a Serial Presence Detection (SPD) failure	Major
8604	POST Reclaim of non-critical NVRAM variables	Minor
8605	BIOS Settings are corrupted	Major
8606	NVRAM variable space was corrupted and has been reinitialized	Major
92A3	Serial port component was not detected	Major
92A9	Serial port component encountered a resource conflict error	Major
9505	ATA/ATAPI interface error	Major
A000	TPM device not detected.	Minor
A001	TPM device missing or not responding.	Minor
A002	TPM device failure.	Minor
A003	TPM device failed self test.	Minor
A100	BIOS ACM Error	Major
A421	PCI component encountered a SERR error	Fatal
A5A0	PCI Express component encountered a PERR error	Minor
A5A1	PCI Express component encountered an SERR error	Fatal
A6A0	DXE Boot Services driver: Not enough memory available to shadow a Legacy Option ROM.	Minor

POST Error Beep Codes

The following table lists POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user-visible code on POST Progress LEDs.

Table 60. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
3	Memory error	Multiple	System halted because a fatal error related to the memory was detected.

USB Device Beeps When POST

Intel® Server Boards of the S3420 family are designed to indicate USB readiness by a series of beep codes early during POST, just before video becomes available. These four to five beeps mean that the USB is powered and initialized, in order for the USB devices such as the keyboard and the mouse to become operational.

If a USB device such as a pen drive or a USB CD/DVD ROM drive is attached to any external USB port, a beep code means that the device is recognized, powered, and initialized. Each USB port will issue a beep once an external device is ready for use.

These beep codes do not signal any errors. They are designed to advise the user of USB readiness during POST and while attaching external devices.

This USB Beep is OS independent.

Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ASIC	Application Specific Integrated Circuit
ASMI	Advanced Server Management Interface
BIOS	Basic Input/Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
Byte	8-bit quantity
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.)
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMP	Emergency Management Port
EPS	External Product Specification
ESB2-E	Enterprise South Bridge 2
FBD	Fully Buffered DIMM
FMB	Flexible Mother Board
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GB	1024MB
GPIO	General Purpose I/O
GTL	Gunning Transceiver Logic
HSC	Hot-Swap Controller
Hz	Hertz (1 cycle/second)
I^2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture
IBF	Input Buffer
ICH	I/O Controller Hub
ICMB	Intelligent Chassis Management Bus
IERR	Internal Error
IFB	I/O and Firmware Bridge
INTR	Interrupt

Term	Definition
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
ITP	In-Target Probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB	1024KB
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
ms	milliseconds
MTTR	Memory Type Range Register
Mux	Multiplexor
NIC	Network Interface Controller
NMI	Nonmaskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm	Unit of electrical resistance
PEF	Platform Event Filtering
PEP	Platform Event Paging
PIA	Platform Information Area (This feature configures the firmware for the platform hardware.)
PLD	Programmable Logic Device
PMI	Platform Management Interrupt
POST	Power-On Self Test
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
RMM3	Remote Management Module – 3rd generation
RMM3 NIC	Remote Management Module – 3rd generation dedicated management NIC
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board.)
SDR	Sensor Data Record
SECC	Single Edge Connector Cartridge
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory

Term	Definition
SEL	System Event Log
SIO	Server Input/Output
SMI	Server Management Interrupt (SMI is the highest priority nonmaskable interrupt.)
SMM	Server Management Mode
SMS	Server Management Software
SNMP	Simple Network Management Protocol
SSI	Server System Infrastructure
TBD	To Be Determined
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
UTC	Universal time coordinate
VID	Voltage Identification
VRD	Voltage Regulator Down
Word	16-bit quantity
ZIF	Zero Insertion Force

Reference Documents

Refer to the following documents for additional information:

- *Intel® Server Board S1600JP Technical Product Specification*
- *ACPI 3.0:* http://www.acpi.info/spec.htm
- *IPMI 2.0*
- *Data Center Management Interface Specification v1.0*, May 1, 2008: www.intel.com/go/dcmi
- *PCI Bus Power Management Interface Specification 1.1*: http://www.pcisig.com/
- *PCI Express* Base Specification Rev 2.0,* Dec 06: http://www.pcisig.com/
- *PCI Express* Card Electromechanical Specification, Rev 2.0*: http://www.pcisig.com/
- *PMBus*:* http://pmbus.org
- *SATA 2.6:* http://www.sata-io.org/
- *SMBIOS 2.4*
- *SSI-EEB 3.0:* http://www.ssiforum.org/
- *USB 1.1:* http://www.usb.org
- *USB 2.0:* http://www.usb.org
- *Windows* Logo/SDG 3.0*
- *Intel® Dynamic Power Technology Node Manager 1.5 External Interface Specification using IPMI, 2007*. Intel Corporation.
- *Node Power and Thermal Management Architecture Specification v1.5, rev.0.79*. *2007*, Intel Corporation.
- *Intel® Server System Integrated Baseboard Management Controller Core External Product Specification, 2007* Intel Corporation.
- *Intel® Thurley Server Platform Services IPMI Commands Specification, 2007.* Intel Corporation.
- *Intel® Server Safety and Regulatory, 2011.* Intel Corporation. (*Intel® Order Code: G23122*)
- *Intelligent Platform Management Bus Communications Protocol Specification, Version 1.0,* 1998. Intel Corporation, Hewlett-Packard* Company, NEC* Corporation, Dell* Computer Corporation.
- *Platform Environmental Control Interface (PECI) Specification, Version 2.0*. Intel Corporation.

- *Platform Management FRU Information Storage Definition, Version 1.0, Revision 1.2,* 2002. Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation: http://developer.intel.com/design/servers/ipmi/spec.htm.