

Intel® Server System H2000WP Family

Technical Product Specification

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November, 2013

Enterprise Platforms and Services Division

Revision History

| Date | Revision Number | Modifications |
|-----------------|-----------------|---|
| January, 2012 | 1.0 | Initial release. |
| April, 2012 | 1.1 | <ul style="list-style-type: none">▪ Updated Table 66 PCI Express* Slot Pinout on Riser Card.▪ Updated System Level Environmental Limits.▪ Updated node cooling fan redundancy features.▪ Updated system Power Supply redundancy features. |
| June, 2012 | 1.2 | <ul style="list-style-type: none">▪ Updated environmental specifications with ASHRAE specification.▪ Updated Processor TDP to conditional support 135W.▪ Added new bridge board for 6G SAS support.▪ Added riser support for non-transparent bridge. |
| September, 2012 | 1.3 | <ul style="list-style-type: none">▪ Added System behavior with one Power Supply AC lost or failed. |
| August, 2013 | 1.4 | <ul style="list-style-type: none">▪ Updated E5-2600 v2 processor support.▪ Updated Post Code LED decoder.▪ Updated POST Error Messages and Handling. |
| November, 2014 | 1.5 | <ul style="list-style-type: none">▪ Updated chassis air flow specification. |

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Table of Contents

| | |
|--|-----------|
| 1. Introduction | 1 |
| 1.1 Chapter Outline | 1 |
| 1.2 Server Board Use Disclaimer | 2 |
| 2. Product Overview | 3 |
| 2.1 System Views..... | 5 |
| 2.2 System Dimensions..... | 5 |
| 2.3 System Level Environmental Limits..... | 6 |
| 2.3.1 High Temperature Ambience (HTA) Support..... | 7 |
| 2.3.2 Set Throttling Mode..... | 10 |
| 2.3.3 Altitude..... | 11 |
| 2.3.4 Set Fan Profile | 11 |
| 2.3.5 Fan PWM Offset..... | 11 |
| 2.3.6 Quiet Fan Idle Mode..... | 11 |
| 2.3.7 Thermal Sensor Input for Fan Speed Control | 11 |
| 2.4 Hard Drive and Peripheral Bays | 12 |
| 2.5 Server Board Overview | 13 |
| 2.6 Front Bezel Support | 16 |
| 2.7 Rack and Cabinet Mounting Options | 16 |
| 3. Power Sub-System | 17 |
| 3.1 Mechanical Overview | 17 |
| 3.1.1 AC Power Supply Unit Dimension Overview | 17 |
| 3.1.2 AC Power Supply Unit General Data..... | 17 |
| 3.1.3 AC input connector..... | 18 |
| 3.1.4 AC Power Cord Specification Requirements | 18 |
| 3.1.5 Power Supply Unit DC Output Connector..... | 18 |
| 3.1.6 Handle Retention | 19 |
| 3.1.7 LED Marking and Identification..... | 19 |
| 3.1.8 Power Cage with Power Distribution Board | 19 |
| 3.1.9 Power Cage Output Pin Assignment | 20 |
| 3.2 AC Input Specification..... | 22 |
| 3.2.1 Input Voltage and Frequency | 22 |
| 3.2.2 AC input Power Factor | 22 |
| 3.2.3 Efficiency..... | 22 |
| 3.2.4 AC Line Fuse | 23 |
| 3.2.5 AC Line Inrush | 23 |
| 3.2.6 AC Line Dropout/Holdup | 23 |
| 3.2.7 AC Line Fast Transient (EFT) Specification..... | 23 |
| 3.2.8 Hot Plug..... | 24 |
| 3.2.9 Susceptibility Requirements | 24 |

| | | |
|--------|--|----|
| 3.2.10 | ElectroStatic Discharge Susceptibility | 24 |
| 3.2.11 | Fast Transient/Burst..... | 24 |
| 3.2.12 | Radiated Immunity | 24 |
| 3.2.13 | Surge Immunity | 24 |
| 3.2.14 | AC Line Transient Specification | 25 |
| 3.2.15 | Power recovery | 25 |
| 3.2.16 | Voltage Interruptions | 25 |
| 3.2.17 | AC Line Isolation | 25 |
| 3.2.18 | AC Power Inlet | 25 |
| 3.3 | DC Output Specification | 26 |
| 3.3.1 | Output Power/Currents..... | 26 |
| 3.3.2 | Standby Output | 26 |
| 3.3.3 | Voltage Regulation | 26 |
| 3.3.4 | Dynamic Loading | 27 |
| 3.3.5 | Capacitive Loading..... | 27 |
| 3.3.6 | Ripple/Noise..... | 27 |
| 3.3.7 | Grounding | 27 |
| 3.3.8 | Closed Loop Stability..... | 28 |
| 3.3.9 | Residual Voltage Immunity in Standby Mode | 28 |
| 3.3.10 | Common Mode Noise..... | 28 |
| 3.3.11 | Soft Starting | 28 |
| 3.3.12 | Zero Load Stability Requirement | 28 |
| 3.3.13 | Hot Swap Requirement | 28 |
| 3.3.14 | Forced Load Sharing..... | 29 |
| 3.3.15 | Timing Requirement..... | 29 |
| 3.4 | Power Supply Cold Redundancy Support..... | 30 |
| 3.4.1 | 1200W CRPS Cold Redundancy..... | 31 |
| 3.4.2 | 1600W CRPS Cold Redundancy..... | 31 |
| 3.4.3 | System behavior with one Power Supply AC lost or failed..... | 31 |
| 3.5 | Control And Indicator Functions | 31 |
| 3.5.1 | PSON# Input Signal | 32 |
| 3.5.2 | PWOK (power good) Output Signal..... | 32 |
| 3.5.3 | SMBAlert# Signal | 32 |
| 3.6 | Protection circuits..... | 33 |
| 3.6.1 | Current Limit (OCP)..... | 33 |
| 3.6.2 | Over Voltage Protection (OVP) | 33 |
| 3.6.3 | Over Thermal protection..... | 33 |
| 3.7 | PMBus* | 34 |
| 3.7.1 | PSU Address Lines A0..... | 34 |
| 3.7.2 | Accuracy | 35 |
| 3.8 | Power Management Policy..... | 35 |

| | |
|---|-----------|
| 4. Cooling Sub-System | 36 |
| 4.1 Processor Heatsink | 36 |
| 4.2 Node cooling Fans | 37 |
| 4.3 Power Supply Fan | 39 |
| 4.4 Air Duct Module..... | 39 |
| 4.5 Drive Bay Population Requirement..... | 39 |
| 5. System Boards in the Node Tray | 41 |
| 5.1 Node Docking Board | 41 |
| 5.1.1 Overview of Node Docking Board..... | 41 |
| 5.1.2 Pinout definition on Node Docking Board | 42 |
| 5.2 Bridge Board | 43 |
| 5.2.1 Overview of Bridge Board | 43 |
| 5.2.2 Pinout definition on Bridge Board | 44 |
| 5.3 Spare Bridge Board to support 6Gbs SAS..... | 46 |
| 5.3.1 Overview of Bridge Board | 46 |
| 5.3.2 Pinout definition on SAS 6Gbs Bridge Board..... | 48 |
| 6. Hard Disk Drive Support | 50 |
| 6.1 Hard Disk Drive Bays scheme | 50 |
| 6.2 Hard Drive Carrier | 51 |
| 6.3 Hot Swap Hard Drive Support | 51 |
| 6.3.1 Backplane Feature set: | 52 |
| 6.3.2 Backplane Block Diagram | 53 |
| 6.3.3 3.5" Hot Swap Backplane Connector scheme | 53 |
| 6.3.4 2.5" Hot Swap Backplane Connector scheme | 54 |
| 6.3.5 Backplane LED Support | 56 |
| 6.3.6 Backplane Connector Definition | 56 |
| 7. Front Panel Control and Indicators | 60 |
| 7.1 Control Panel Button | 61 |
| 7.2 Control Panel LED Indicators | 61 |
| 7.2.1 Power/Sleep LED | 62 |
| 7.2.2 System Status LED | 62 |
| 7.2.3 System Status LED – BMC Initialization | 63 |
| 8. Configuration Jumpers | 64 |
| 8.1 Force Integrated BMC Update (J6B1) | 65 |
| 8.2 Force ME Update (J1E2)..... | 66 |
| 8.3 Password Clear (J1E3) | 66 |
| 8.4 BIOS Recovery Mode (J1E1) | 67 |
| 8.5 Reset BIOS Settings (J1D5)..... | 68 |
| 9. PCI Express* Riser Card and Assembly | 70 |
| 9.1 PCI Express* Riser for Slot 1 | 70 |
| 9.1.1 Overview of PCI-Express Riser | 70 |

| | | |
|---|---|-----------|
| 9.1.2 | Pinout definition on Slot 1 Riser | 70 |
| 9.2 | PCI Express* Riser with IOM Carrier for Slot 2 (Optional) | 74 |
| 9.2.1 | Overview of PCI-E Riser with IOM Carrier..... | 74 |
| 9.2.2 | Pinout definition on Slot 2 Riser and IOM Carrier | 76 |
| Appendix A: Integration and Usage Tips | | 82 |
| Appendix B: POST Code LED Decoder | | 83 |
| Appendix C: Video POST Code Errors | | 89 |
| Glossary | | 95 |
| Reference Documents | | 98 |

List of Figures

| | |
|--|----|
| Figure 1. System Overview (Air Duct is removed) | 5 |
| Figure 2. Compute Node Scheme (Rear View) | 5 |
| Figure 3. Fan Speed Control Structure..... | 12 |
| Figure 4. Intel® Server System H2312WP Drive Bay Overview | 13 |
| Figure 5. Intel® Server System H2216WP Drive Bay Overview | 13 |
| Figure 6. Intel® Server Board S2600WP..... | 13 |
| Figure 7. Intel® Server Board S2600WPQ/F Components..... | 14 |
| Figure 8. Back Panel Feature Overview | 14 |
| Figure 9. Light-Guided Diagnostic LED Locations | 15 |
| Figure 10. System Bezel Front View | 16 |
| Figure 11. AC Power Supply Unit Dimension Overview | 17 |
| Figure 12. Power Cage Overview..... | 20 |
| Figure 13. Power distribution board..... | 21 |
| Figure 14. AC Power Cord Specification | 26 |
| Figure 15. Turn On/Off Timing (Power Supply Signals)..... | 30 |
| Figure 16. Power Supply Device Address | 34 |
| Figure 17. PMBus* Monitoring Accuracy | 35 |
| Figure 18. Processor Heatsink Overview | 37 |
| Figure 19. Node Fan Set and power/control Connection | 38 |
| Figure 20. Compute Node Air Duct | 39 |
| Figure 21. Compute Node Tray Overview | 41 |
| Figure 22. Node Docking Board | 41 |
| Figure 23. Bridge Board Overview | 43 |
| Figure 24. Connectors on Bridge Board..... | 44 |
| Figure 25. SAS 6Gbps Bridge Board Overview | 47 |
| Figure 26. Connectors and components on Spare Bridge Board..... | 48 |
| Figure 27. HDD Scheme for H2312WPGR..... | 50 |
| Figure 28. HDD Scheme for H2216WPGR..... | 50 |
| Figure 29. 3.5-inch HDD Assembly Overview..... | 51 |
| Figure 30. 2.5-inch HDD Assembly Overview..... | 51 |
| Figure 31. Passive Backplane Block Diagram (for one node)..... | 53 |
| Figure 32. 3.5" Backplane Component and Connectors (Front View)..... | 53 |
| Figure 33. 3.5" Backplane Component and Connectors (Back View) | 54 |
| Figure 34. 2.5" Backplane Component and Connectors (Front View)..... | 55 |
| Figure 35. 2.5" Backplane Component and Connectors (Back View) | 55 |
| Figure 36. Hard Drive Carrier LED | 56 |
| Figure 37. Front Control Panel | 60 |
| Figure 38. Jumper Locations and Functions..... | 64 |
| Figure 39. PCI Express* Riser for Riser Slot 1 | 70 |

Figure 40. PCI Express* Riser with bracket for Riser Slot 275
Figure 41. IOM Carrier75
Figure 42. Diagnostic LED location83

List of Tables

| | |
|--|----|
| Table 1. System Feature Set..... | 3 |
| Table 2. System SKU matrix | 4 |
| Table 3. Chassis Dimension (SKU: H2312WPJR)..... | 5 |
| Table 4. Chassis Dimension (SKU: H2216WPJR)..... | 6 |
| Table 5. System Environmental Limits Summary | 6 |
| Table 6. Ambient Temperature Versus System Configuration | 9 |
| Table 7. Intel® Server System H2312WP and H2216WP Drive Support Matrix | 12 |
| Table 8. Specification Data for AC Power Supply Unit | 18 |
| Table 9. AC power cord specification | 18 |
| Table 10. DC Output Power Connector..... | 18 |
| Table 11. Power Supply Status LED | 19 |
| Table 12. Pin assignment of power output connector | 21 |
| Table 13. Pin assignment of control signal connector..... | 21 |
| Table 14. AC input rating. | 22 |
| Table 15. Typical power factor | 22 |
| Table 16. Platinum Efficiency Requirement..... | 23 |
| Table 17. AC Power Holdup Requirement..... | 23 |
| Table 18. Performance Criteria | 24 |
| Table 19. AC Line Sag Transient Performance | 25 |
| Table 20. AC Line Surge Transient Performance | 25 |
| Table 21. Load Ratings for single power supply unit | 26 |
| Table 22. Voltage Regulation Limits..... | 26 |
| Table 23. Transient Load Requirements | 27 |
| Table 24. Capacitive Loading Conditions | 27 |
| Table 25. Ripple and Noise | 27 |
| Table 26. Timing Requirement | 29 |
| Table 27. 1200W CRPS Cold Redundancy Threshold | 31 |
| Table 28. 1600W CRPS Cold Redundancy Threshold | 31 |
| Table 29. System behavior with one Power Supply AC lost or failed..... | 31 |
| Table 30. PSON# Signal Characteristics..... | 32 |
| Table 31. PWOK Signal Characteristics | 32 |
| Table 32. SMBAlert# Signal Characteristics | 33 |
| Table 33. Over Current Protection..... | 33 |
| Table 34. Over Voltage Protection (OVP) Limits | 33 |
| Table 35. PSU addressing | 34 |
| Table 36. PMBus* Accuracy..... | 35 |
| Table 37. 8-pin Connector Pin-Out for Node Dual Rotor Fans..... | 39 |
| Table 38. Main Power Input Connector | 42 |
| Table 39. Fan Control Signal Connector | 42 |

| | |
|---|----|
| Table 40. Node Fan Connector | 42 |
| Table 41. Main Power Output Connector | 43 |
| Table 42. Card Edge Connector Pinout..... | 44 |
| Table 43. AHCI SATA0 DOM Connector Pinout..... | 45 |
| Table 44. USB 2.0 Type-A Connector Pinout | 46 |
| Table 45. 5V_AUX Power Connector Pinout | 46 |
| Table 46. Pinout of Card Edge to BaseBoard..... | 48 |
| Table 47. Pinout of Card Edge to Hot Swap Back Plane | 48 |
| Table 48. Pinout of Mini SAS Connector | 49 |
| Table 49. Hard Drive Carrier Status LED Functions | 56 |
| Table 50. Hard Drive Carrier Activity LED Functions | 56 |
| Table 51. Backplane Input Power Connector Pin-out | 57 |
| Table 52. 2-blade Compute Node Power Connector Pin-out..... | 57 |
| Table 53. 2x40 Pin Connector Pin-out for Node Bridge Board..... | 57 |
| Table 54. Front Panel Connector Pin-out | 58 |
| Table 55. Power Supply Control Connector Pin-out | 59 |
| Table 56. Front Control Button Function..... | 61 |
| Table 57. Front LED Indicator Functions | 61 |
| Table 58. Power LED Operation | 62 |
| Table 59. System Status LED Operation..... | 62 |
| Table 60. Force Integrated BMC Update Jumper | 65 |
| Table 61. Force Integrated BMC Update Jumper | 65 |
| Table 62. Force ME Update Jumper | 66 |
| Table 63. BIOS Password Clear Jumper..... | 66 |
| Table 64. BIOS Recovery Mode Jumper | 67 |
| Table 65. Reset BIOS Jumper | 68 |
| Table 66. Riser Card Edge Pinout..... | 70 |
| Table 67. PCI Express* Slot Pinout on Riser Card | 72 |
| Table 68. Dedicated NIC Port LED Functionality | 75 |
| Table 69. Riser Card Edge Pinout..... | 76 |
| Table 70. PCI Express* Slot Pinout on Riser Card | 78 |
| Table 71. IO Module Slot on Carrier..... | 80 |
| Table 72. POST Code Diagnostic LED Location | 83 |
| Table 73. POST Progress Code LED Example | 84 |
| Table 74. MRC Fatal Error Codes..... | 84 |
| Table 75. MRC Progress Codes..... | 85 |
| Table 76. POST Progress Codes | 85 |
| Table 77. POST Error Message and Handling | 89 |
| Table 78. POST Error Beep Codes | 94 |

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1. Introduction

This Technical Product Specification (TPS) provides system specific information detailing the features, functionality, and high-level architecture of the Intel® Server System H2000WP family. You should also reference the *Intel® Server Board S2600WP Family Technical Product Specification* to obtain greater detail of functionality and architecture of the server board integrated in this server system.

In addition, you can obtain design-level information for specific sub-systems by ordering the *External Product Specifications (EPS)* or *External Design Specifications (EDS)* for a given sub-system. EPS and EDS documents are not publicly available. They are only made available under NDA with Intel® and must be ordered through your local Intel® representative. For a complete list of available documents, refer to the *Reference Documents* section at the end of this document.

The Intel® Server System H2000WP may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Refer to the *Intel® Server Board S2600WP/Intel® Server System H2000WP Specification Update* for published errata.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Product Overview
- Chapter 3 – Power Sub-System
- Chapter 4 – Cooling Sub-System
- Chapter 5 – System Boards in the Node Tray
- Chapter 6 – Hard Disk Drive Support
- Chapter 7 – Front Panel Control and Indicators
- Chapter 8 – Configuration Jumpers
- Chapter 9 – PCI Express* Riser Card and Assembly
- Appendix A – Integration and Usage Tips
- Appendix B – POST Code LED Decoder
- Appendix C – Video POST Code Errors
- Glossary
- Reference Documents

1.2 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel® ensures through its own chassis development and testing that when Intel® server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel® developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Overview

The Intel® Server System H2000WP family includes two major SKUs: H2312WP and H2216WP, which are rack mount 2U 4-node server systems, purpose-built for high-density and lowest total cost of ownership in dense computing applications, such as HPC and IPDC. The system is integrated with four units of Intel® Server Board S2600WP or S2600WPQ/S2600WPF, supports up to twelve 3.5" or sixteen 2.5" hot-swap SAS or SATA hard drives, with Common Redundant Power Supply (CRPS) capability.

This chapter provides a high-level overview of the system features. The following chapters provide greater detail for each major system component or feature.

Table 1. System Feature Set

| Feature | Description |
|----------------------------|---|
| Processor | Support Intel® Xeon® Processor E5-2600 and E5-2600 v2 series processors. <ul style="list-style-type: none"> ▪ Up to 8 GT/s Intel® QuickPath Interconnect (Intel® QPI). ▪ LGA 2011 Socket R. ▪ Thermal Design Power (TDP) up to 135W with conditional ambient temperature, 130 Watt (6-core or 8-core) and below, or 80 Watt (4-core) and below. |
| Memory | <ul style="list-style-type: none"> ▪ Unbuffered DDR3 and registered DDR3 with ECC DIMMs. ▪ Memory DDR3 data transfer rates of 800/1066/1333/1600 MT/s. ▪ Load Reduced DDR3 DIMM. ▪ DDR3 standard I/O voltage of 1.5V (all speed) and DDR3 Low Voltage of 1.35V (1333MT/s or below) |
| Chipset | Intel® C600-A Platform Controller Hub (PCH) with support for optional Storage Upgrade Key |
| System Connectors /Headers | External I/O connectors: <ul style="list-style-type: none"> ▪ DB-15 Video connectors. ▪ Two RJ-45 Network Interface for 10/100/1000 LAN. ▪ One stacked two port USB 2.0 (Port 0/1) connectors. ▪ One dedicated 1GbE management port on rIOM carrier (Optional). ▪ One InfiniBand* QDR QSFP port (Board SKU: S2600WPQ) or One InfiniBand* FDR QSFP port (Board SKU: S2600WPF) Internal connectors/headers: <ul style="list-style-type: none"> ▪ Bridge Slot to extend board I/O <ul style="list-style-type: none"> - SCU0 (Four SAS 3Gb/s ports) to backplane - Front control panel signals - One SATA (Port 0) 6Gb/s port for DOM ▪ Bridge Slot to extend board I/O with spare bridge board <ul style="list-style-type: none"> - Mini SAS port (Four SAS 6Gb/s ports) from add-in RAID card to backplane - Front control panel signals ▪ One Type-A USB 2.0 connector (USB port 2) ▪ One 2x7pin header for system FAN module ▪ One DH-10 serial Port A connector ▪ One SATA 6Gb/s (Port 1) ▪ One 2x4 pin header for Intel® RMM4 Lite ▪ One 1x4 pin header for Storage Upgrade Key |
| System Fan Support | Three sets of dual rotor fan for each node. |
| Add-in Adapter Support | Four PCIe Gen III x16 riser slots: <ul style="list-style-type: none"> ▪ Riser slot 1 support PCIe Gen III x16 Riser with LP PCIe add-in card ▪ Riser slot 2 supports PCIe Gen III x8 Riser (Intel® rIOM) ▪ Riser slot 3 and slot 4 cannot be used with bridge board covered One Bridge Slot for board I/O expansion. |

| Feature | Description |
|---------------------------|--|
| On-board Video | On-board Server Engines* LLC Pilot III Controller <ul style="list-style-type: none"> Integrated 2D Video Controller 128 MB DDR3 Memory |
| Hard Disk Drive supported | 12x 3.5-inch SATA/SAS HDD bays (SKU: H2312WP) 16x 2.5-inch SATA/SAS HDD bays (SKU: H2216WP) |
| RAID Support | <ul style="list-style-type: none"> Intel® RSTe SoftWare RAID 0/1/10/5 for SATA mode LSI® ESRT2 SoftWare RAID 0/1/10/5 for SAS/SATA mode |
| LAN | For each node: <ul style="list-style-type: none"> One Gigabit Ethernet device i350 connect to PCI-E x4 interfaces on the PCH, providing 2 GbE ports for each node. One QSFP port from Mellanox* ConnectX3 to support QDR/FDR Infiniband* based on board SKUs. One dedicated 1GbE management port with RMM4 Lite and rIOM carrier installed. |
| System Power | <ul style="list-style-type: none"> 1200W AC Common Redundant Power Supply (CRPS), 80 plus Platinum with PFC, supporting CRPS configuration. Chassis SKU: H2312WPJR, H2216WPJR <ul style="list-style-type: none"> 1600W AC Common Redundant Power Supply (CRPS), 80 plus Platinum with PFC, supporting CRPS configuration. Chassis SKU: H2312WPKR, H2216WPKR |
| Server Management | <ul style="list-style-type: none"> Onboard ServerEngines* LLC Pilot III* Controller. Support for Intel® Remote Management Module 4 Lite solutions. Intel® Light-Guided Diagnostics on field replaceable units. Support for Intel® System Management Software. Support for Intel® Intelligent Power Node Manager (Need PMBus*-compliant power supply). |

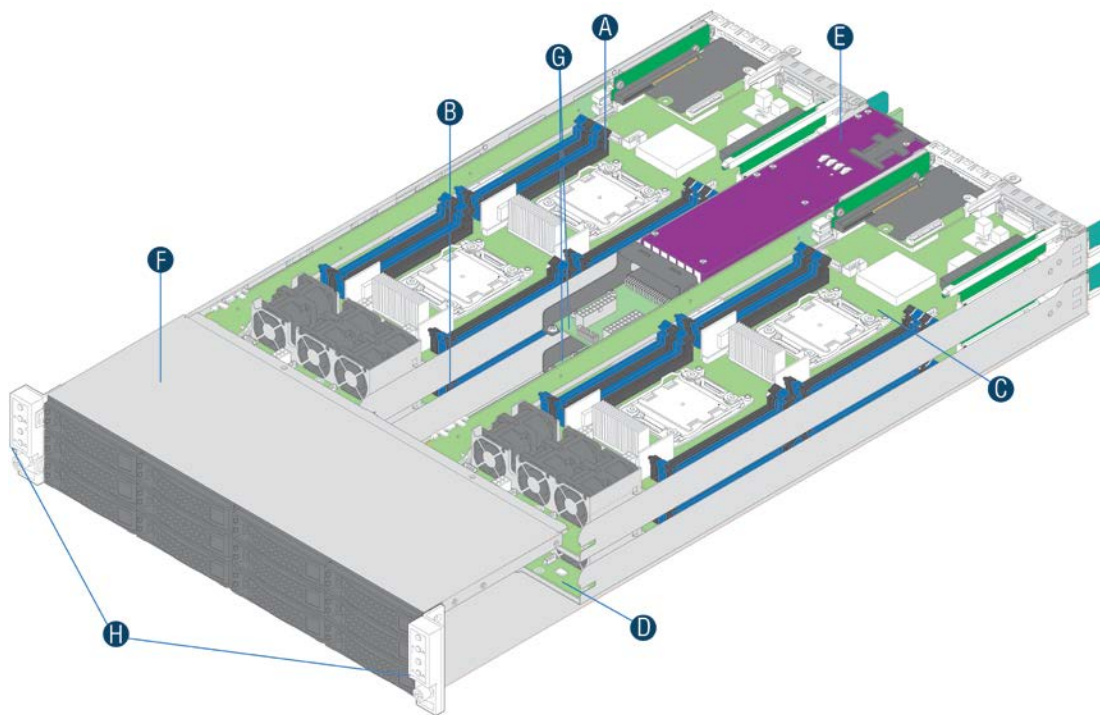
Table 2. System SKU matrix

| Board SKU vs. Chassis | 3.5" HDD with 1200W CRPS | 2.5" HDD with 1200W CRPS | 3.5" HDD with 1600W CRPS | 2.5" HDD with 1600W CRPS |
|-----------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| S2600WP | H2312WPJR | H2216WPJR | H2312WPKR | H2216WPKR |
| S2600WPQ | H2312WPQJR | H2216WPQJR | H2312WPQKR | H2216WPQKR |
| S2600WPF | H2312WPFJR | H2216WPFJR | H2312WPFKR | H2216WPFKR |

The Intel® Server System H2000WP family supports all Intel® Xeon® processor E5-2600 and E5-2600 v2 series with TDP 130W (8-core, 6-core), or 80W (4-core) and below. You can find a full list of supported processors at the Intel® support website:

http://www.intel.com/p/en_US/support/highlights/server/sb-s2600wp.

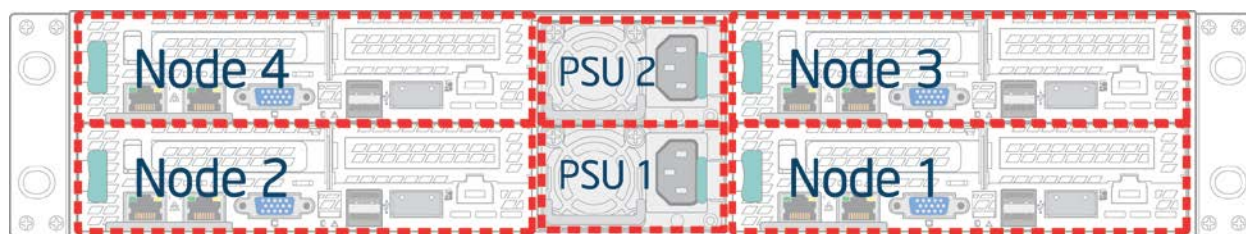
2.1 System Views



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| | | | |
|----------|-----------------------------------|----------|---|
| A | Compute Node 3 Tray (upper left) | E | Common Redundant Power Supply |
| B | Compute Node 1 Tray (lower left) | F | HDD bays with Hot Swap Backplane |
| C | Compute Node 4 Tray (upper right) | G | Upper and Lower Power Distribution Boards |
| D | Compute Node 2 Tray (lower right) | H | Front Control Panel |

Figure 1. System Overview (Air Duct is removed)



AF004513

Figure 2. Compute Node Scheme (Rear View)

2.2 System Dimensions

Table 3. Chassis Dimension (SKU: H2312WPJR)

| | | |
|---|------------|-------------|
| Height | 87.9mm | 3.46" |
| Width | 438mm | 17.24" |
| Depth | 771mm | 30.35" |
| Weight | Kg. | Lbs. |
| Chassis – basic configured (Two PSU, Zero drives) | 30 | 66.14 |
| Chassis – fully configured (Two PSU, 12 drives) | 38 | 83.78 |

Table 4. Chassis Dimension (SKU: H2216WPJR)

| | | |
|---|------------|-------------|
| Height | 87.9mm | 3.46" |
| Width | 438mm | 17.24" |
| Depth | 733mm | 28.86" |
| Weight | Kg. | Lbs. |
| Chassis – basic configured (2 PSU, 0 drives) | 29 | 63.93 |
| Chassis – fully configured (2 PSU, 16 drives) | 32 | 70.55 |

2.3 System Level Environmental Limits

The following table defines the Intel® Server Board S2600WP operating and non-operating environmental limits. Operation of the Intel® Server Board S2600WP at conditions beyond those shown in the following table may cause permanent damage to the system. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 5. System Environmental Limits Summary

| Parameter | | Limits |
|-------------|-----------------------------------|--|
| Temperature | | |
| | Operating | ASHRAE Class A2 – Continuous Operation. 10°C to 35°C (50°F to 95°F) with the maximum rate of change not to exceed 10°C per hour |
| | | ASHRAE Class A3 – Includes operation up to 40°C for up to 900 hrs. per year. |
| | | ASHRAE Class A4 – Includes operation up to 45°C for up to 90 hrs. per year. |
| | Shipping | -40°C to 70°C (-40°F to 158°F) |
| Humidity | | |
| | Non-Operating | 50% to 90%, non-condensing with a maximum wet bulb of 28°C (at temperatures from 25°C to 35°C) |
| Shock | | |
| | Operating | Half sine, 2g , 11 mSec |
| | Unpackaged | Trapezoidal, 25g , velocity change is based on packaged weight |
| | Packaged | Product Weight: ≥ 40 to < 80 Non-palletized Free Fall Height = 18 inches Palletized (single product) Free Fall Height = NA |
| Vibration | | |
| | Unpackaged | 5 Hz to 500 Hz 2.20 g RMS random |
| | Packaged | 5 Hz to 500 Hz 1.09 g RMS random |
| AC-DC | | |
| | Voltage | 90V to 132V and 180V to 264 |
| | Frequency | 47Hz to 63Hz |
| | Source Interrupt | No loss of data for power line drop-out of 12 mSec |
| | Surge Non-operating and operating | Unidirectional |
| | Line to earth Only | AC Leads 2.0 kV I/O Leads 1.0 kV DC Leads 0.5 kV |
| ESD | | |

| Parameter | | Limits |
|--------------------------------|-----------------------|--|
| | Air Discharged | 8.0 kV |
| | Contact Discharge | 8.0 kV |
| Altitude | | |
| | Operating | -16 to 3048 m (-50 to 10,000 ft) Note: For altitudes above 2950 feet, the maximum operating temperature is derated 1°F/550 ft. |
| | Storage | -16 to 10,600 m (-50 to 35,000 ft) |
| Acoustics Sound Power Measured | – | – |
| Air Flow | Operation | H2312xxKR: 8 to 41 CFM per node H2216xxKR: 8 to 61 CFM per node |
| | Power in Watts | All range |
| | Servers/Rack Mount BA | - 3.5" HDD SKU: 6.9BA at idle and 7.4BA at active mode. - 2.5" HDD SKU: 6.5BA at idle and 7.07BA at active mode. |

Note:

1. Intel Corporation server boards contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel® ensures through its own chassis development and testing that when Intel® server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel® developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible, if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

Disclaimer Note: Intel® ensures the unpackaged server board and system meet the shock requirement mentioned above through its own chassis development and system configuration. It is the responsibility of the system integrator to determine the proper shock level of the board and system if the system integrator chooses different system configuration or different chassis. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

In order to maintain comprehensive thermal protection, deliver the best system acoustics, and fan power efficiency, an intelligent Fan Speed Control (FSC) and thermal management technology (mechanism) is used. **Options** in <F2> **BIOS Setup (BIOS > Advanced > System Acoustic and Performance Configuration)** allow for parameter adjustments based on the actual system configuration and usage. Refer to the following sections for a description of each setting.

2.3.1 High Temperature Ambience (HTA) Support

To keep the system operating within supported maximum thermal limits, the system must meet the following operating and configuration guidelines:

- The system operating ambient is designed for sustained operation up to 35°C (ASHRAE Class A2) with short term excursion based operation up to 45°C (ASHRAE Class A4).

- The system can operate up to 40°C (ASHRAE Class A3) for up to 900 hours per year
- The system can operate up to 45°C (ASHRAE Class A4) for up to 90 hours per year
- System performance may be impacted when operating within the extended operating temperature range
- There is no long term system reliability impact when operating at the extended temperature range within the approved limits
- Specific configuration requirements and limitations are documented in the configuration matrix found in the *Intel® Server Board S2600WP product family Power Budget and Thermal Configuration Guidelines Tool*, available as a download tool online at Intel.com.
- The CPU-1 processor + CPU heatsink must be installed first. The CPU-2 heatsink must be installed at all times, with or without a processor installed.
- Memory Slot population requirements:

Note: Specified memory slots can be populated with a DIMM or supplied DIMM Blank. Memory population rules apply when installing DIMMs.

- **DIMM Population Rules on CPU-1** – Install DIMMs in order; Channels A, B, C, and D.
- **DIMM Population on CPU-2** – Install DIMMs in order; Channels E, F, G, and H.
- The following system configurations require that specific memory slots be populated at all times using either a DIMM or supplied DIMM blank.
- System Configuration – 16 x 2.5" hard drive bay or 12 x 3.5" hard drive bay configuration and Intel® Server Board S2600WP (16-DIMM server board).
- All hard drive bays must be populated. Hard drive carriers can be populated with a hard drive or supplied drive blank.
- With the system operating, the air duct must be installed at all times.
- In single power supply configurations, the second power supply bay must have the supplied filler blank installed at all times.
- Thermally, the system can support the following PCI add-in cards:
 - Add-in cards with a minimum 100 LFM (0.5 m/s) air flow requirement can be installed in any available add-in card slot in both Riser Card #1 and Riser Card for IO Module carrier.
 - Add-in cards with a >200 LFM air flow requirement cannot be supported.

Note: Most PCI add-in cards have minimum air flow requirements of 100 LFM (0.5m/s). Some high power add-in cards have minimum air flow requirements of 200 LFM (1 m/s). System integrators should verify PCI add-in card air flow requirements from vendor specifications when integrating add-in cards into the system.

- The system top-cover must be installed at all times when the system is in operation.
- Supported ambient temperature versus processor TDP is as follows:

Table 6. Ambient Temperature Versus System Configuration

| | | | | | | | | | |
|---|---|-------------------------------------|------|------|-------------------------------------|------|------|------|----------------|
| Notes: 1. 25°C is limited to elevations of 900m or less 2. Quad Port IO Modules cannot be installed simultaneously with PCI Cards. 3. Processor - 130W-4C and 135W-8C may have some performance impact. 4. Processors - There may be some performance impact during fan failures. 5. For A3/A4 individual PS selection: i. For dual power supply configuration, power budget must fit within single power supply rated load and be installed in dual configuration, or ii. For single power supply configuration, power budget must be sized with 30% margin to single power supply rated load. 6. LV refers to low voltage DIMMs (1.35V) 7. When identifying memory in the table, only Rank and Width are required. Capacity is not required. 8. Fan fail of dual-rotor fans refers to one rotor fail. "Fan Fail Support" indicates if fan fail can be supported with specified configuration in each column. | | Base System SKUs: H2216WP | | | Base System SKUs: H2312WP | | | | |
| ASHRAE (See note 1) | Classifications | A2 | A3 | A4 | 25 C | A2 | A3 | A4 | |
| | Max Ambient | 35 C | 40 C | 45 C | 25 C | 35 C | 40 C | 45 C | <-- See note 1 |
| Cooling (See note 8) | Redundant Fan Configuration | • | • | • | • | • | • | • | |
| | Fan Fail Support | • | | | • | • | | | |
| PS (See note 5) | Power Supplies | See Power Budget Tool | | | See Power Budget Tool | | | | <-- See note 5 |
| EP Processors (See notes 3 and 4) | Intel® Xeon® processor E5-2630L, 60w, 6C | • | • | | • | • | • | | <-- see note 4 |
| | Intel® Xeon® processor E5-2650L, 70w, 8C | • | • | • | • | • | • | | <-- see note 4 |
| | Intel® Xeon® processor E5-2620, E5-2630, E5-2640, 95w, 6C | • | • | • | • | • | • | • | <-- see note 4 |
| | Intel® Xeon® processor E5-2650, E5-2660, 95w, 8C | • | • | • | • | • | • | • | <-- see note 4 |
| | Intel® Xeon® processor E5-2665, E5-2670, 115w, 8C | • | • | • | • | • | • | | <-- see note 4 |
| | Intel® Xeon® processor E5-2667, 130w, 6C | • | • | • | • | • | | | <-- see note 4 |
| | Intel® Xeon® processor E5-2680, 130w, 8C | • | | | • | • | | | <-- see note 4 |

| | | | | | | | | | |
|-----------------------------------|--|---|---|---|---|---|---|---|----------------|
| | Intel® Xeon® processor E5-2690, 135w, 8C | • | | | • | | | | |
| | Intel® Xeon® processor E5-2637, 80w, 2C | • | • | • | • | • | • | • | <-- see note 4 |
| | Intel® Xeon® processor E5-2603, E5-2609, 80w, 4C | • | • | • | • | • | • | • | <-- see note 4 |
| | Intel® Xeon® processor E5-2643, 130w, 4C | • | | | • | | | | |
| Memory Type (See note 6 and 7) | Dual Rank x8 | • | • | • | • | • | • | • | |
| | Dual Rank x4 | • | • | | • | • | • | | |
| | Quad Rank x8 | • | • | | • | • | • | | |
| | Quad Rank x4 | • | | | • | • | | | |
| | Load Reduced DIMM | • | | | • | • | | | |
| Add-in Cards (See note 2) | PCI Cards | • | • | • | • | • | • | • | <-- See note 2 |
| Module (See note 2) | AXX10GBTWLIOM - Dual 10GBASE-T IO Module | • | • | • | • | • | • | • | |
| | AXX10GBNIAIOM - Dual SFP+ port 10GbE IO Module | • | • | • | • | • | • | • | |
| | AXX1FDRIBIOM - Single Port FDR Infiniband* IO Module | • | • | • | • | • | • | • | |
| | AXX2FDRIBIOM - Dual Port FDR Infiniband* IO Module | • | • | • | • | • | • | • | |
| | AXX4P1GBPWLIOIM - Quad Port 1GbE IO Module | • | • | • | • | • | • | • | <-- See note 2 |

2.3.2 Set Throttling Mode

This option is used to select the desired memory thermal throttling mechanism. Available settings include:

[Auto] – [DCLTT], [SCLTT], and [SOLTT].

[Auto] – Factory Default Setting - BIOS automatically detects and identifies the appropriate thermal throttling mechanism based on DIMM type, airflow input, and DIMM sensor availability.

[DCLTT] – Dynamic Closed Loop Thermal Throttling: for the SOD DIMM with system airflow input.

[SCLTT] – Static Close Loop Thermal Throttling: for the SOD DIMM without system airflow input.

[SOLTT] – Static Open Loop Thermal Throttling: for the DIMMs without sensor on DIMM (SOD).

2.3.3 Altitude

This option is used to select the proper altitude that the system will be used in. Available settings include: [300m or less], **[301m-900m]**, [901m-1500m], [Above 1500m].

Selecting an altitude range that is lower than the actual altitude the system will be operating at, can cause the fan control system to operate less efficiently, leading to higher system thermals and lower system performance. If the altitude range selected is higher than the actual altitude the system will be operating at, the fan control system may provide better cooling but with higher acoustics and higher fan power consumption. If the altitude is not known, selecting a higher altitude is recommended in order to provide sufficient cooling.

2.3.4 Set Fan Profile

This option is used to set the desired Fan Profile. Available settings include: **[Performance]** and **[Acoustic]**.

The Acoustic mode offers the best acoustic experience and appropriate cooling capability covering the mainstream and the majority of the add-in cards used. Performance mode is designed to provide sufficient cooling capability covering all kinds of add-in cards on the market.

2.3.5 Fan PWM Offset

This option is reserved for manual adjustment to the minimum fan speed curves. The valid range is from **[0 to 100]** which stands for 0% to 100% PWM adding to the minimum fan speed. This feature is valid when Quiet Fan Idle Mode is at Enabled state. The default setting is **[0]**.

2.3.6 Quiet Fan Idle Mode

This feature can be **[Enabled]** or **[Disabled]**. If enabled, the fans will either shift to a lower speed or stop when the aggregate sensor temperatures are satisfied, indicating the system is at ideal thermal/light loading conditions. When the aggregate sensor temperatures are not satisfied, the fans will shift back to normal control curves. If fans are disabled, they will never shift into lower fan speeds or stop, regardless of whether the aggregate sensor temperatures are satisfied or not. The default setting is **[Disabled]**.

Note: The above feature may or may not be in effect and depends on the actual thermal characteristics of the specified system.

2.3.7 Thermal Sensor Input for Fan Speed Control

The BMC uses various IPMI sensors as inputs to fan speed control. Some of the sensors are actual physical sensors and some are virtual sensors derived from calculations.

The following IPMI thermal sensors are used as input to fan speed control:

- Front Panel Temperature Sensor ¹
- Server board Temperature Sensor ²
- Processor Margin Sensors ^{3, 5, 6}
- DIMM Thermal Margin Sensors ^{3, 5}
- Exit Air Temperature Sensor ^{1, 4, 8}

- Chipset Temperature Sensor ^{4, 6}
- On-board Ethernet Controller Temperature Sensors ^{4, 6}
- Add-In Intel® SAS/IO Module Temperature Sensors ^{4, 6}
- Power Supply Thermal Sensor ^{4, 9}
- Processor VR Temperature Sensors ^{4, 7}
- DIMM VR Temperature Sensors ^{4, 7}
- BMC Temperature Sensor ^{4, 7}
- Global Aggregate Thermal Margin Sensors ⁸

Notes:

1. For fan speed control in Intel® chassis
2. For fan speed control in third party chassis
3. Temperature margin from throttling threshold
4. Absolute temperature
5. PECEI value or margin value
6. On-die sensor
7. On-board sensor
8. Virtual sensor
9. Available only when PSU has PMBus*

The following diagram illustrates the fan speed control structure:

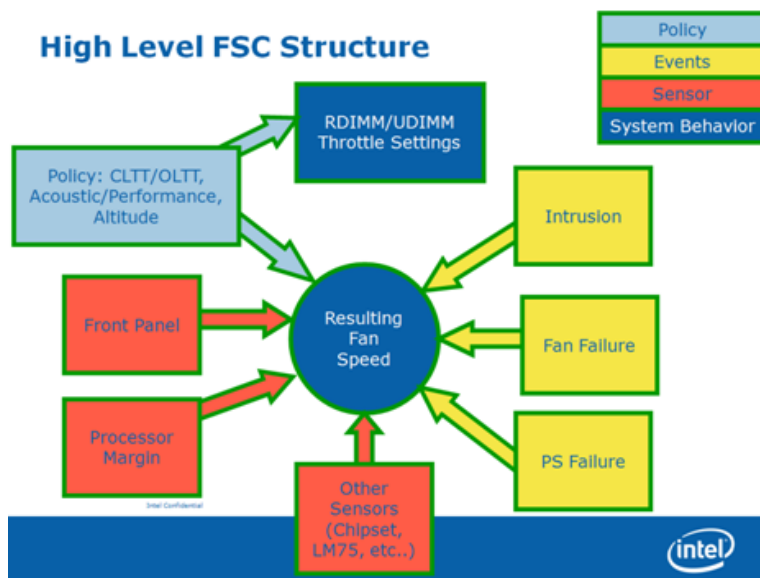
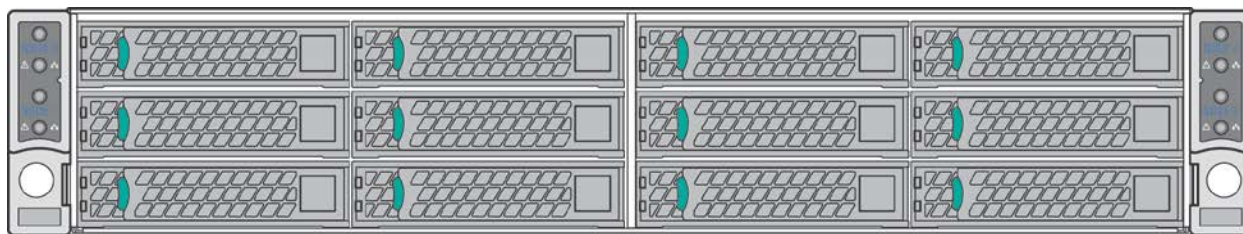


Figure 3. Fan Speed Control Structure

2.4 Hard Drive and Peripheral Bays

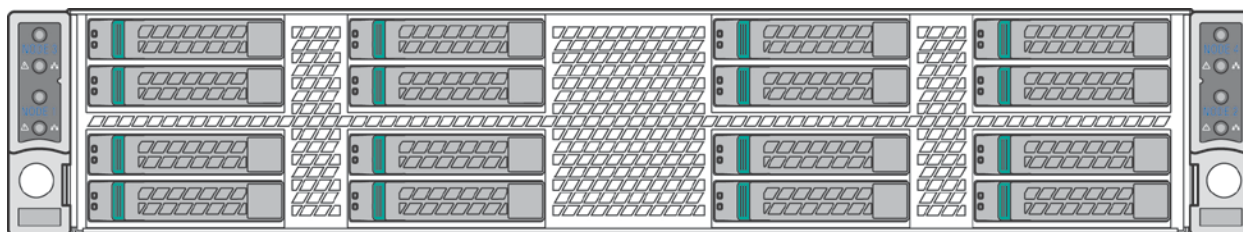
Table 7. Intel® Server System H2312WP and H2216WP Drive Support Matrix

| | Intel® Server System H2312WP | Intel® Server System H2216WP |
|----------------------------------|------------------------------|------------------------------|
| Slim-line SATA Optical Drive | Not Supported | Not Supported |
| Internal USB Floppy Drive | Not Supported | Not Supported |
| SATA/SAS Hard Disk Drives (3.5") | Up to Twelve | Not Supported |
| SATA/SAS Hard Disk Drives (2.5") | Not Supported | Up to Sixteen |
| SATA DOM | Support | Support |



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Figure 4. Intel® Server System H2312WP Drive Bay Overview



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Figure 5. Intel® Server System H2216WP Drive Bay Overview

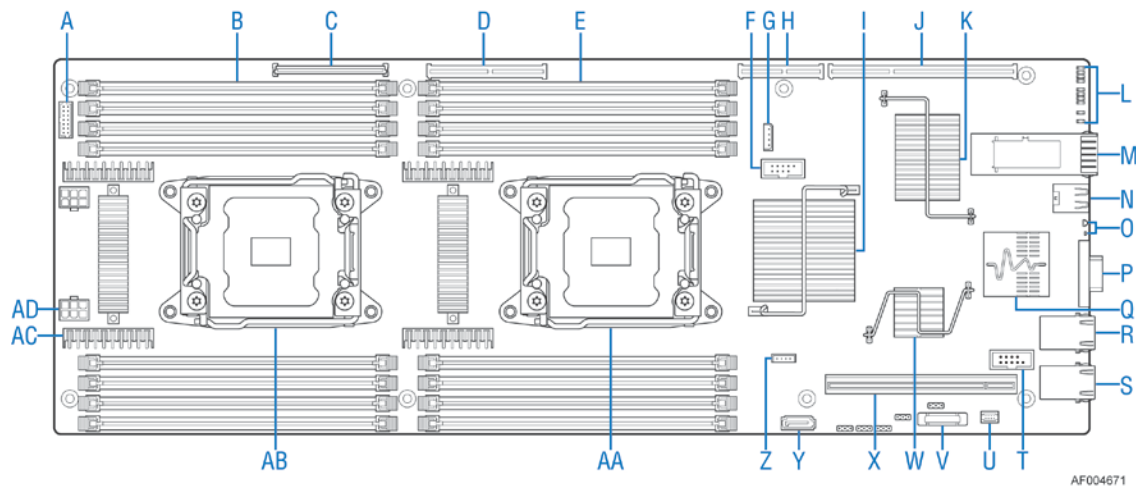
2.5 Server Board Overview

The chassis is mechanically and functionally designed to support half-width server board, including Intel® Server Board S2600WP. The following sections provide an overview of the server board feature sets.



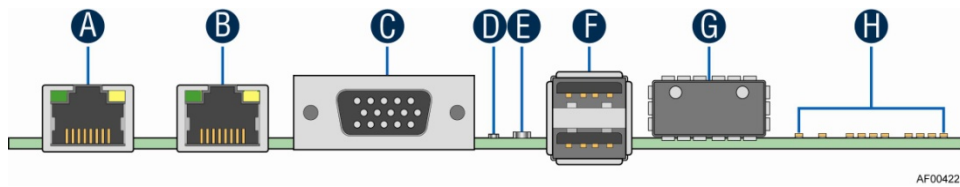
Figure 6. Intel® Server Board S2600WP

The following figure shows the layout of the server board. Each connector and major component is identified by a number or letter, and a description is given below the figure.



| | Description | | Description | | Description | | Description |
|----------|-----------------------------|----------|---------------------------------------|----------|-----------------------------|-----------|-----------------------------|
| A | 2x7 fan control connector | I | PCH C600-A | Q | Dual port 1GbE NIC chip | Y | SATA port 1 |
| B | CPU2 DIMM slots (8 total) | J | Riser Slot 2 (PCIe Gen3x16) | R | NIC port 2 | Z | Storage Upgrade key |
| C | Riser Slot 4 (PCIe Gen3x16) | K | Infiniband* QDR | S | NIC Port 1 | AA | CPU 1 |
| D | Riser Slot 3 (PCIe Gen3x16) | L | InfiniBand* status and Diagnostic LED | T | Serial Port A | AB | CPU 2 |
| E | CPU1 DIMM slots (8 total) | M | QSFP | U | RMM4 lite | AC | VRS (4 total) |
| F | 2x5 USB | N | USB x2 | V | CMOS battery | AD | 2x3 PWR connector (2 total) |
| G | IPMB connector | O | Status and ID LED | W | Integrated BMC | | |
| H | Bridge board connector | P | VGA out | X | Riser Slot 1 (PCIe Gen3x16) | | |

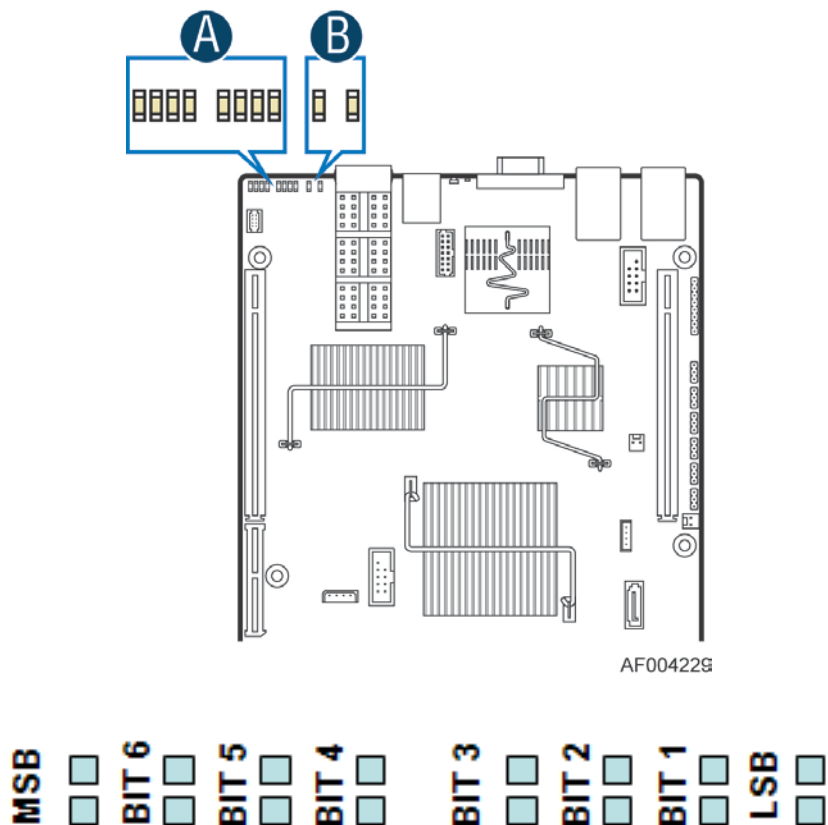
Figure 7. Intel® Server Board S2600WPQ/F Components



| | Description | | Description |
|----------|-------------------|----------|--------------------------------|
| A | NIC port 1 (RJ45) | E | Status LED |
| B | NIC port 2 (RJ45) | F | Dual port USB connector |
| C | DB15 video out | G | QSFP Connector |
| D | ID LED | H | QSFP status and Diagnostic LED |

Figure 8. Back Panel Feature Overview

Note: The Intel® Server System H2312WP and H2216WP requires the use of shielded LAN cable to comply with Emission/Immunity regulatory requirements. Use of non-shield cables **may result in** product non-compliance.



| | | | |
|---|----------------------|---|------------------------|
| A | Diagnostic LED Group | B | QSFP Link/Activity LED |
|---|----------------------|---|------------------------|

Figure 9. Light-Guided Diagnostic LED Locations

2.6 Front Bezel Support

Intel® Server System H2000WP family provides front panel bezel. The bezel provides protection to system HDD bays with a lock to chassis. The front view of the bezel is shown as below.

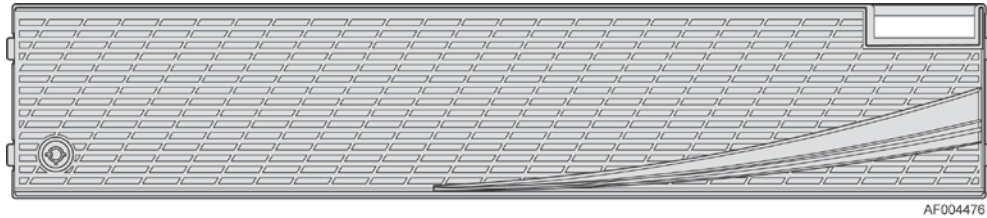


Figure 10. System Bezel Front View

2.7 Rack and Cabinet Mounting Options

The chassis was designed to support 19 inches wide by up to 30 inches deep server cabinets. The system bundles with the following Intel® rack mount option.

A basic slide rail kit (Product order code – **AXXELVRAIL**) is designed to mount the chassis into a standard (19 inches by up to 30 inches deep) EIA-310D compatible server cabinet.

CAUTION: THE MAXIMUM RECOMMENDED SERVER WEIGHT FOR THE RACK RAILS CAN BE FOUND at <http://www.intel.com/support/motherboards/server/sb/CS-033655.htm>. EXCEEDING THE MAXIMUM RECOMMENDED WEIGHT OR MISALIGNMENT OF THE SERVER MAY RESULT IN FAILURE OF THE RACK RAILS HOLDING THE SERVER. Use of a mechanical assist to install and align server into the rack rails is recommended.

3. Power Sub-System

The system supports AC 1+1 hot swap power supply module and two power distribution board which can support 2U rack high density server system. Two different power supply units are supported: 1200W and 1600W. The single power supply module has Platinum level energy efficiency, demonstrating climate saver with silver rating.

3.1 Mechanical Overview

The power supply module has a simple retention mechanism to retain the module self once it is inserted. This mechanism must withstand the specified mechanical shock and vibration requirements. The power distribution board is fixed in the chassis with screws. This specification defines a 1+1 hot swap redundancy power supply that supports 2U server system. Using existing power supply module provided by vendor with updated PMBus* and custom-made power connector board to support four nodes of Intel® Server Board S2600WP. The power supply should have two outputs: 12V and 12VSB. The input should be auto ranging and power factor corrected. The PMBus* features included in this specification are requirements for AC silver rated box power supply for use in server systems based on Intel® Server System H2000WP Family. This specification is based on the *PMBus* Specifications part I and II, revision 1.1*.

3.1.1 AC Power Supply Unit Dimension Overview

The casing dimension is W 73.5mm x L 265.0mm x H 39/40mm. The power supply contains a single 40mm fan. The power supply has a card edge output that interfaces with a 2x25 card edge connector in the system. The AC plugs directly into the external face of the power supply.

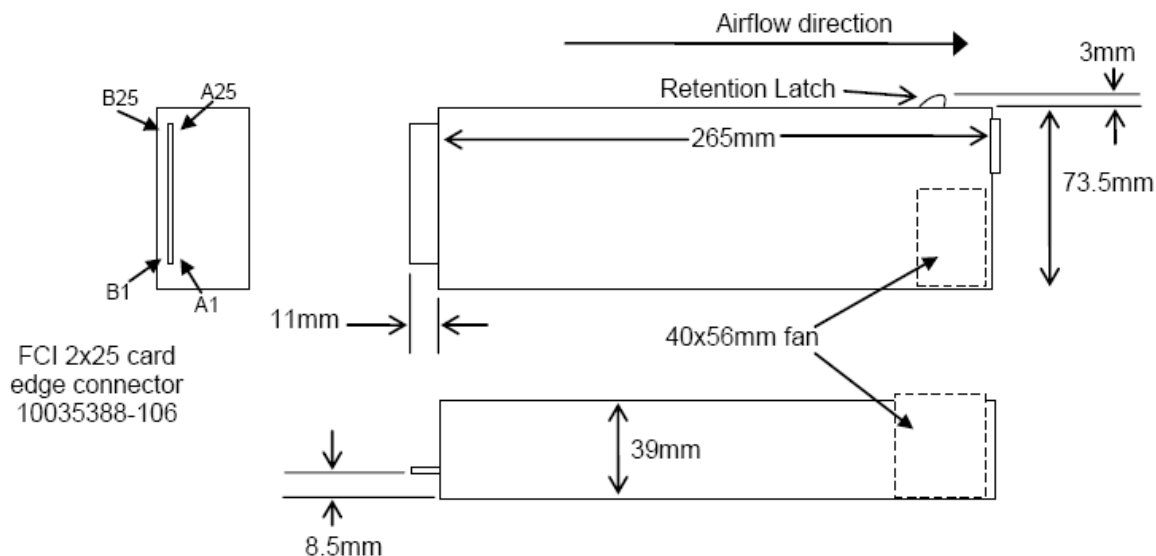


Figure 11. AC Power Supply Unit Dimension Overview

3.1.2 AC Power Supply Unit General Data

Below is general specification data for AC Power Supply Unit.

Table 8. Specification Data for AC Power Supply Unit

| | |
|---------------------------|---|
| Wattage | 1200W/1600W (Energy Smart) |
| Voltage | 90 – 264 VAC, auto-ranging, 47 Hz-63 Hz |
| Heat Dissipation | 2560 BTU/hr |
| Maximum Inrush Current | Under typical line conditions and over the entire system ambient operating range, the inrush current may reach 65 A per power supply for 5 ms |
| 80 Plus rating | Platinum |
| Climate Saver (CS) rating | Platinum |

3.1.3 AC input connector

The power supply has an internal IEC320 C14 power inlet. The inlet is rated for a minimum of 10A at 250VAC.

3.1.4 AC Power Cord Specification Requirements

The AC power cord used must meet the following specification requirements:

Table 9. AC power cord specification

| | |
|--------------------|--------|
| Cable Type | SJT |
| Wire Size | 16 AWG |
| Temperature Rating | 105 °C |
| Amperage Rating | 13A |
| Cable Type | SJT |

3.1.5 Power Supply Unit DC Output Connector

The DC output connector pin-out is defined as follows:

Table 10. DC Output Power Connector

| PSU Output Connector | | | |
|----------------------|------|-----|------|
| A1 | GND | B1 | GND |
| A2 | GND | B2 | GND |
| A3 | GND | B3 | GND |
| A4 | GND | B4 | GND |
| A5 | GND | B5 | GND |
| A6 | GND | B6 | GND |
| A7 | GND | B7 | GND |
| A8 | GND | B8 | GND |
| A9 | GND | B9 | GND |
| A10 | +12V | B10 | +12V |
| A11 | +12V | B11 | +12V |
| A12 | +12V | B12 | +12V |
| A13 | +12V | B13 | +12V |
| A14 | +12V | B14 | +12V |
| A15 | +12V | B15 | +12V |
| A16 | +12V | B16 | +12V |
| A17 | +12V | B17 | +12V |

| PSU Output Connector | | | |
|----------------------|-------------------|-----|-------------------------------|
| A18 | +12V | B18 | +12V |
| A19 | PMBus* SDA | B19 | A0* (SMBus* address) |
| A20 | PMBus* SCL | B20 | A1* (SMBus* address) |
| A21 | PSON | B21 | 12V STBY |
| A22 | SMBAAlert# | B22 | Cold Redundancy Bus* |
| A23 | Return Sense | B23 | 12V load share bus |
| A24 | +12V Remote Sense | B24 | No Connect |
| A25 | PWOK | B25 | CRPS Compatibility Check pin* |

*: Refer to the spec of CRPS: *Common Requirements Specification*.

3.1.6 Handle Retention

The power supply has a handle to assist extraction. The module is able to be inserted and extracted without the assistance of tools. The power supply also has a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply.

The handle protects the operator from any burn hazard through the use of industrial designed plastic handle or equivalent material.

3.1.7 LED Marking and Identification

The power supply is using a bi-color LED: Amber and Green for status indication. Below are table showing the LED states for each power supply operating state.

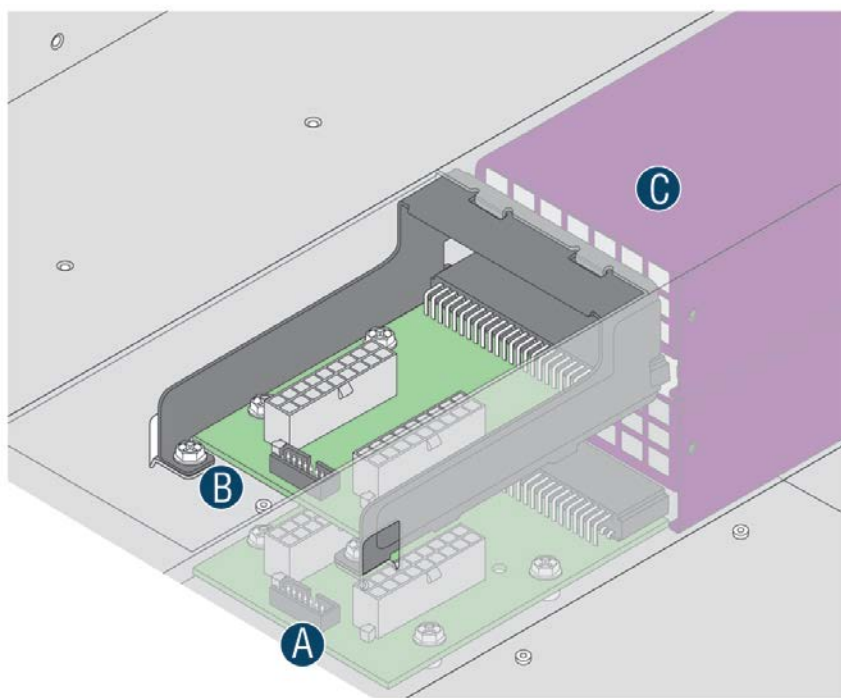
Table 11. Power Supply Status LED

| Power Supply Condition | LED State |
|---|-----------------|
| Output ON and OK | Solid GREEN |
| No AC power to all power supplies | OFF |
| AC present/Only 12VSB on (PS off) or PS in Cold redundant state | 1Hz Blink GREEN |
| AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power. | Solid AMBER |
| Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan. | 1Hz Blink Amber |
| Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail | Solid AMBER |
| Power supply FW updating | 2Hz Blink GREEN |

3.1.8 Power Cage with Power Distribution Board

The power cage is at the middle of the chassis, consists of two Power Distribution Boards (PDB) to support Common Redundant Power Supplies (CRPS).

The power system overview is shown below:



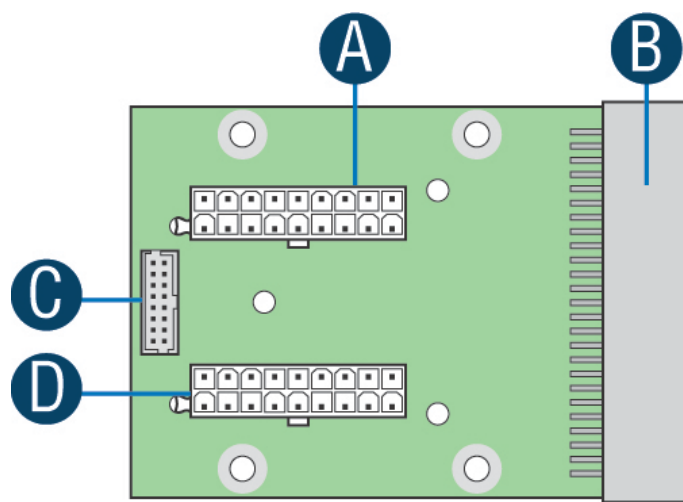
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| | |
|----------|---|
| A | Power Distribution Board 1 |
| B | Power Distribution Board 2 |
| C | Power Supply Unit #2 (upper) and #1 (lower) |

Figure 12. Power Cage Overview

3.1.9 Power Cage Output Pin Assignment

The power cage provides +12V and +12V_{STB} output to the system. Each PDB has two 2x9 power output cable to system backplane, together with one 2x8 signal control cable for power management. Refer to below table for PDB pin assignment.



AF004432

| | |
|----------|--------------------------------|
| A | Main Power Output Connector P1 |
| B | Power Supply Unit Connector |
| C | Control Signal Connector |
| D | Main Power Output Connector P2 |

Figure 13. Power distribution board

Table 12. Pin assignment of power output connector

| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 1 | GND | 2 | +12V |
| 3 | GND | 4 | +12V |
| 5 | GND | 6 | +12V |
| 7 | GND | 8 | +12V |
| 9 | GND | 10 | +12V |
| 11 | GND | 12 | +12V |
| 13 | GND | 14 | +12V |
| 15 | GND | 16 | +12V |
| 17 | GND | 18 | +12V |

Table 13. Pin assignment of control signal connector

| Pin | Description | Pin | Description |
|-----|-------------|-----|---------------------|
| 1 | PMBus* SDA | 2 | A0 (SMBus* Address) |
| 3 | PMBus* SCL | 4 | A1 (SMBus* Address) |

| Pin | Description | Pin | Description |
|-----|-------------------|-----|---------------------|
| 5 | PSO# | 6 | 12V Load Share Bus |
| 7 | SMBAlert# | 8 | Cold Redundancy Bus |
| 9 | Return Sense | 10 | PWOK |
| 11 | +12V Remote Sense | 12 | Compatibility Bus |
| 13 | Reserved | 14 | +12VSB |
| 15 | +12VSB | 16 | Key Pin (removed) |

3.2 AC Input Specification

3.2.1 Input Voltage and Frequency

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% THD must not cause the power supply to go out of specific limits. The power supply must be capable of start-up (power-on) with full rated power load, at line voltage as low as 90VAC.

Table 14. AC input rating.

| Parameter | Min | Rated | Max | Start up VAC | Power Off VAC |
|--------------------|----------------------|--------------------------|----------------------|---------------------------------------|-------------------------------------|
| 110V _{AC} | 90 V _{rms} | 100-127 V _{rms} | 140 V _{rms} | 85 V _{AC} ± 4V _{AC} | 70V _{AC} ±5V _{AC} |
| 220V _{AC} | 180 V _{rms} | 200-240 V _{rms} | 264 V _{rms} | | |
| Frequency | 47 Hz | 50/60 Hz | 63 Hz | | |

Notes:

1. Maximum input current at low input voltage range should be measured at 90VAC, at max load.
2. Maximum input current at high input voltage range should be measured at 180VAC, at max load.
3. This requirement is not to be used for determining agency input current markings.

3.2.2 AC input Power Factor

The power supply must meet the power factor requirements stated in the Energy Star® Program Requirements for Computer Servers. These requirements are stated below.

Table 15. Typical power factor

| Output power | 10% load | 20% load | 50% load | 100% load |
|--------------|----------|----------|----------|-----------|
| Power factor | > 0.80 | > 0.90 | > 0.90 | > 0.95 |

Note: Tested at 230Vac, 50Hz and 60Hz and 115VAC, 60Hz. Tested according to *Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.4.3*. This is posted at <http://efficientpowersupplies.epri.com/methods.asp>.

3.2.3 Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels; 100%, 50%, 20%, and 10%. Output should be loaded according to the proportional loading method defined by 80 Plus in *Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.4.3*. This is posted at: <http://efficientpowersupplies.epri.com/methods.asp>.

Table 16. Platinum Efficiency Requirement

| Loading | 100% of maximum | 50% of maximum | 20% of maximum | 10% of maximum |
|--------------------|-----------------|----------------|----------------|----------------|
| Minimum Efficiency | 91% | 94% | 90% | 82% |

3.2.4 AC Line Fuse

The power supply should have one line fused in the single line fuse on the line (Hot) wire of the AC input. The line fusing should be acceptable for all safety agency requirements. The input fuse should be a slow blow type. AC inrush current must not cause the AC line fuse to blow under any conditions. All the protection circuits in the power supply must not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.2.5 AC Line Inrush

AC line inrush current should not exceed **65A peak**, for up to one-quarter of the AC cycle, after which, the input current should be no more than the specified maximum input current. The peak inrush current must be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (T_{op}).

3.2.6 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration must not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time, the power supply should recover and meet all turn on requirements. The power supply should meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration must not cause damage to the power supply.

Table 17. AC Power Holdup Requirement

| Loading | Holdup time |
|---------|-------------|
| 70% | 10.6msec |

The $12V_{STB}$ output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of **70ms min** (=12VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

3.2.7 AC Line Fast Transient (EFT) Specification

The power supply should meet the EN61000-4-5 directive and any additional requirements in IEC1000-4-5: 1995 and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.

- The surge-withstand test must not produce damage to the power supply.

The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

3.2.8 Hot Plug

Power supply must be designed to allow connection into and removal from the system without removing power to the system. During any phase of insertion, start-up, shutdown, or removal, the power supply must not cause any other like modules in the system to deviate outside of their specifications. When AC power is applied, the auxiliary supply should turn on, providing bias power internal to the supply and the 5VSB standby output.

3.2.9 Susceptibility Requirements

The power supply should meet the following electrical immunity requirements when connected to a cage with an external EMI filter, which meets the criteria, defined in the SSI document *EPS Power Supply Specification*. For further information on customer standards, please request a copy of the customer *Environmental Standards Handbook*.

Table 18. Performance Criteria

| Level | Description |
|-------|--|
| A | The apparatus should continue to operate as intended. No degradation of performance. |
| B | The apparatus should continue to operate as intended. No degradation of performance beyond spec limits. |
| C | Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls. |

3.2.10 ElectroStatic Discharge Susceptibility

The power supply must comply with the limits defined in EN 55024: 1998 using the IEC 61000-4-2:1995 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.2.11 Fast Transient/Burst

The power supply must comply with the limits defined in EN 55024: 1998 using the IEC 61000-4-4:1995 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.2.12 Radiated Immunity

The power supply must comply with the limits defined in EN 55024: 1998 using the IEC 61000-4-3:1995 test standard and performance criteria A defined in *Annex B of CISPR 24*.

3.2.13 Surge Immunity

The power supply must be tested with the system for immunity to AC Ring wave and AC Unidirectional wave, both up to 2kV, per EN 55024:1998, EN 61000-4-5:1995 and ANSI C62.45: 1992.

The pass criteria include:

- No unsafe operation is allowed under any condition;
- All power supply output voltage levels to stay within proper spec levels;
- No change in operating state or loss of data during and after the test profile;
- No component damage under any condition.

The power supply must comply with the limits defined in EN 55024: 1998 using the IEC 61000-4-5:1995 test standard and performance criteria B defined in *Annex B of CISPR 24*.

3.2.14 AC Line Transient Specification

AC line transient conditions should be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”; these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply must meet the requirements under the following AC line sag and surge conditions.

Table 19. AC Line Sag Transient Performance

| AC Line Sag (10 sec interval between each sagging) | | | | |
|--|------|---------------------------|----------------|--|
| Duration | Sag | Operating AC Voltage | Line Frequency | Performance Criteria |
| 0 to ½ AC cycle | 95% | Nominal AC Voltage ranges | 50/60Hz | No loss of function or performance. |
| > 1 AC cycle | >30% | Nominal AC Voltage ranges | 50/60Hz | Loss of function acceptable, self-recoverable. |

Table 20. AC Line Surge Transient Performance

| AC Line Surge | | | | |
|-----------------|-------|----------------------------------|----------------|------------------------------------|
| Duration | Surge | Operating AC Voltage | Line Frequency | Performance Criteria |
| Continuous | 10% | Nominal AC Voltages | 50/60Hz | No loss of function or performance |
| 0 to ½ AC cycle | 30% | Mid-point of nominal AC Voltages | 50/60Hz | No loss of function or performance |

3.2.15 Power recovery

The power supply should recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

3.2.16 Voltage Interruptions

The power supply must comply with the limits defined in EN 55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-11: Second Edition: 2004-03 test standard and performance criteria C defined in *Annex B of CISPR 24*.

3.2.17 AC Line Isolation

The power supply must meet all safety agency requirements for dielectric strength. Transformers' isolation between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage the highest test voltage should be used. In addition the insulation system must comply with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements.

3.2.18 AC Power Inlet

The AC input connector should be an *IEC 320 C-14* power inlet. This inlet is rated for 10A/250 VAC.

The AC power cord must meet the following specification requirements:

| | |
|--------------------|--------|
| Cable Type | SJT |
| Wire Size | 16 AWG |
| Temperature Rating | 105°C |
| Amperage Rating | 13 A |
| Voltage Rating | 125 V |

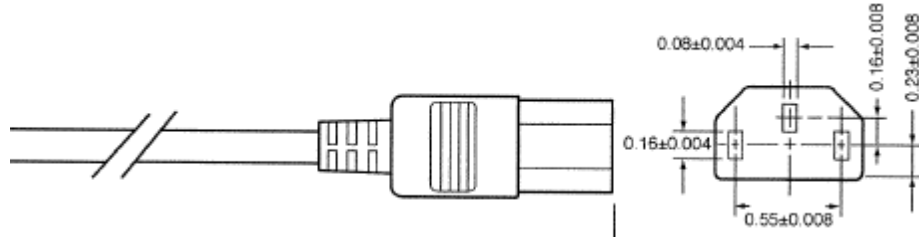


Figure 14. AC Power Cord Specification

3.3 DC Output Specification

3.3.1 Output Power/Currents

The following table defines the minimum power and current ratings. The power supply must meet both static and dynamic voltage regulation requirements for all conditions.

Table 21. Load Ratings for single power supply unit

| Parameter | Min | Max | | Peak ^{2,3} | | Unit |
|------------------------|-----|-------|-------|---------------------|-------|------|
| | | 1200W | 1600W | 1200W | 1600W | |
| PSU SKU | | 1200W | 1600W | 1200W | 1600W | |
| +12V main (200-240VAC) | 0.0 | 100 | 133 | 133 | 175 | A |
| +12V main (100-127VAC) | 0.0 | 83 | 83 | 110 | 110 | A |
| +12V _{STB} | 0.0 | 3.0 | 3.5 | 3.5 | 4.0 | A |

Notes:

- 12V_{STB} must provide 4.0A with two power supplies in parallel. The power supply fan is allowed to run in standby mode for loads > 1.5A.
- Peak combined power for all outputs must not exceed 1600W (for 1200W PSU) and 2100W (for 1600W PSU).
- Length of time peak power can be supported is based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration should be 20 seconds without asserting the SMBAlert# signal.

3.3.2 Standby Output

The 12VSB output should be present when an AC input greater than the power supply turn on voltage is applied.

3.3.3 Voltage Regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. These should be measured at the output connectors.

Table 22. Voltage Regulation Limits

| Parameter | Min | Nom | Max | Unit | Tolerance |
|-----------|-----|-----|-----|------|-----------|
|-----------|-----|-----|-----|------|-----------|

| Parameter | Min | Nom | Max | Unit | Tolerance |
|---------------------|---------|----------|---------|------|-----------|
| +12V _{STB} | +11.40V | +12.000V | +12.60V | Vrms | ±5% |
| +12V | +11.40V | +12.000V | +12.60V | Vrms | ±5% |

The combined output continuous power of all outputs should not exceed 3200W (1600W from each power supply unit). Each output has a maximum and minimum current rating shown in below table. The power supply must meet both static and dynamic voltage regulation requirements for the minimum dynamic loading conditions. The power supply must meet only the static load voltage regulation requirements for the minimum static load conditions.

3.3.4 Dynamic Loading

The output voltages should remain within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate should be tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The μ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 23. Transient Load Requirements

| Output | μ Step Load Size | Load Slew Rate | Test capacitive Load |
|---------------------|----------------------|-------------------|----------------------|
| +12V _{STB} | 1.0A | 0.25 A/ μ sec | 20 μ F |
| +12V | 60% of max load | 0.25 A/ μ sec | 2000 μ F |

Note: For dynamic condition +12V min loading is 1A.

3.3.5 Capacitive Loading

The power supply must be stable and meet all requirements, with the following capacitive loading conditions.

Table 24. Capacitive Loading Conditions

| Output | Min | Max | Units |
|---------------------|-----|--------|---------|
| +12V | 500 | 25,000 | μ F |
| +12V _{STB} | 20 | 3100 | μ F |

3.3.6 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in the following table. This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A 10 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor is placed at the point of measurement.

Table 25. Ripple and Noise

| | |
|----------|---------------------|
| +12V | +12V _{STB} |
| 120mVp-p | 120mVp-p |

3.3.7 Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins should be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply must be provided with a reliable protective earth ground. All secondary circuits should be connected to protective earth ground. Resistance of the ground returns to chassis must not exceed 1.0 mΩ. This path may be used to carry DC current.

3.3.8 Closed Loop Stability

The power supply must be unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in Section 4.6. A minimum of: **45 degrees phase margin** and **-10dB-gain margin** is required. The power supply manufacturer should provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

3.3.9 Residual Voltage Immunity in Standby Mode

The power supply should be immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500mV. There should be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition should not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

3.3.10 Common Mode Noise

The Common Mode noise on any output must not exceed **350mVp-p** over the frequency band of 10Hz to 20MHz.

1. The measurement should be made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure).
2. The test set-up must use a FET probe such as Tektronix* model P6046 or equivalent.

3.3.11 Soft Starting

The Power Supply should contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions.

3.3.12 Zero Load Stability Requirement

When the power subsystem operates in a no load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

3.3.13 Hot Swap Requirement

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages should remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply should use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

3.3.14 Forced Load Sharing

The +12V output will have active load sharing. The output will share within 10% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot-swap/redundant **1+1** configurations. The 12VSBoutput is not required to actively share current between power supplies (passive sharing). The 12VSBoutput of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

3.3.15 Timing Requirement

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70ms. For 12VSB, it is allowed to rise from 1.0 to 25ms. **All outputs must rise monotonically.** The following table shows the timing requirements for the power supply being turned on and off through the AC input, with PSON held low and the PSON signal, with the AC input applied.

Table 26. Timing Requirement

| Item | Description | MIN | MAX | UNITS |
|-----------------------|--|-------|------|-------|
| T_{vout_rise} | Output voltage rise time | 5.0 * | 70 * | ms |
| $T_{sb_on_delay}$ | Delay from AC being applied to 12VSB being within regulation. | | 1500 | ms |
| $T_{ac_on_delay}$ | Delay from AC being applied to all output voltages being within regulation | | 3000 | ms |
| T_{vout_holdup} | Time 12VI output voltage stay within regulation after loss of AC | 13 | | ms |
| T_{pwok_holdup} | Delay from loss of AC to de-assertion of PWOK | 10.6 | | ms |
| $T_{pson_on_delay}$ | Delay from PSON# active to output voltages within regulation limits | 5 | 400 | ms |
| T_{pson_pwok} | Delay from PSON# deactivate to PWOK being de-asserted | | 5 | ms |
| T_{pwok_on} | Delay from output voltages within regulation limits to PWOK asserted at turn on | 100 | 500 | ms |
| T_{pwok_off} | Delay from PWOK de-asserted to output voltages dropping out of regulation limits | 1 | | ms |
| T_{pwok_low} | Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal | 100 | | ms |
| T_{sb_vout} | Delay from 12VSBbeing in regulation to O/Ps being in regulation at AC turn on | 50 | 1000 | ms |
| T_{12VSB_holdup} | Time the 12VSBoutput voltage stays within regulation after loss of AC | 70 | | ms |

Note: * The 12V_{STB} output voltage rise time should be from 1.0ms to 25ms.

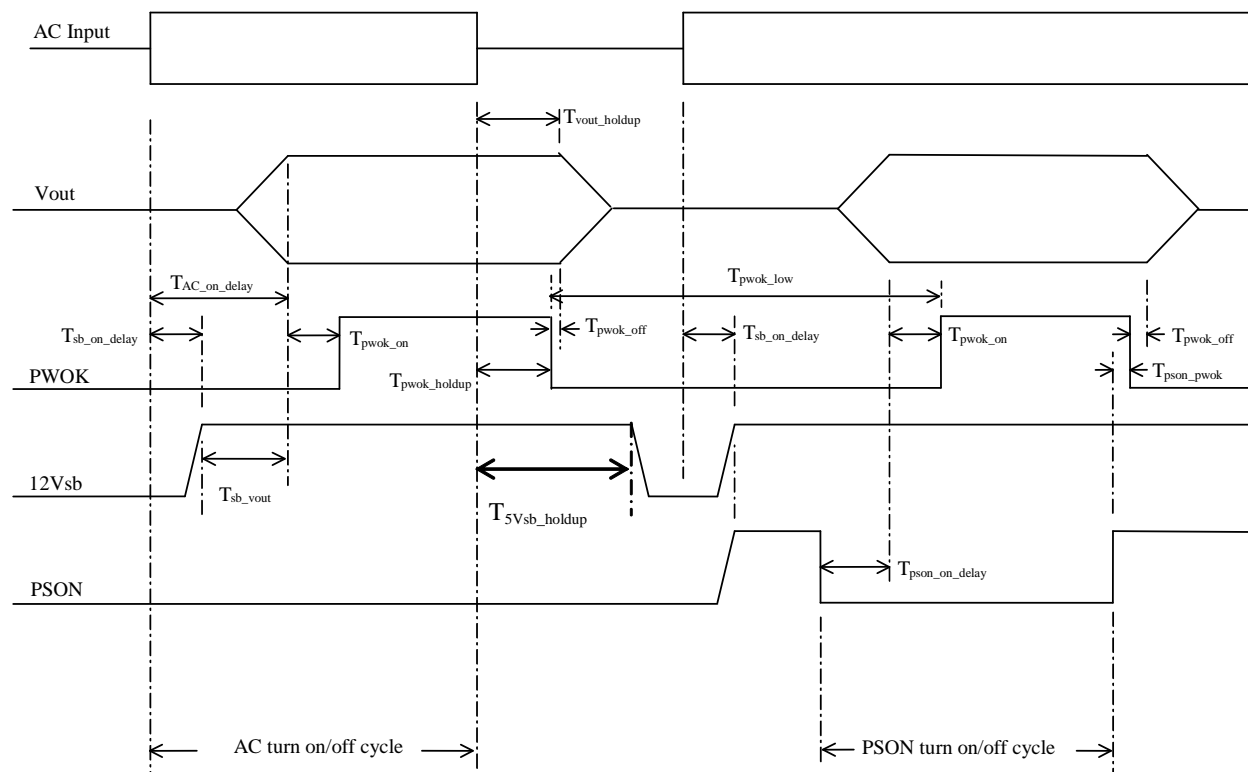


Figure 15. Turn On/Off Timing (Power Supply Signals)

3.4 Power Supply Cold Redundancy Support

Power supplies that support cold redundancy can be enabled to go into a low-power state (that is, cold redundant state) in order to provide increased power usage efficiency when system loads are such that both power supplies are not needed. When the power subsystem is in Cold Redundant mode, only the needed power supply to support the best power delivery efficiency is ON. Any additional power supplies, including the redundant power supply, is in Cold Standby state.

Each power supply has an additional signal that is dedicated to supporting Cold Redundancy; CR_BUS. This signal is a common bus between all power supplies in the system. CR_BUS is asserted when there is a fault in any power supply OR the power supplies output voltage falls below the V_{fault} threshold. Asserting the CR_BUS signal causes all power supplies in Cold Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level through a PMBus* command.

Whenever there is no active power supply on the Cold Redundancy bus driving a HIGH level on the bus all power supplies are ON no matter their defined Cold Redundant roll (active or Cold Standby). This guarantees that incorrect programming of the Cold Redundant states of the power supply will never cause the power subsystem to shut down or become over loaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in Cold Redundant Active state or Standard Redundant state to allow the Cold Standby state power supplies to go into Cold Standby state.

3.4.1 1200W CRPS Cold Redundancy

If the output power is less than 480W (40%), the Cold redundant function is enabled. You will see one PSU working normally. The second PSU will be in CR mode. The Power Supply LED will be blinking green.

Table 27. 1200W CRPS Cold Redundancy Threshold

| | Enable (V) | Percent | Power (W) | Disable (V) | Percent | Power (W) |
|----------------------|------------|---------|-----------|-------------|---------|-----------|
| Cold Standby 1 (02h) | 3.2 | 40.00% | 480 (±5%) | 1.44 | 18.00% | 432 (±5%) |

3.4.2 1600W CRPS Cold Redundancy

If the output power is less than 640W (40%), the Cold redundant function is enabled. You will see one PSU working normal. The second PSU will be in CR mode. The Power Supply LED will be blinking green.

Table 28. 1600W CRPS Cold Redundancy Threshold

| | Enable (V) | Percent | Power (W) | Disable (V) | Percent | Power (W) |
|----------------------|------------|---------|-----------|-------------|---------|-----------|
| Cold Standby 1 (02h) | 3.2 | 40.00% | 640 (±5%) | 1.44 | 18.00% | 576 (±5%) |

3.4.3 System behavior with one Power Supply AC lost or failed

Table 29. System behavior with one Power Supply AC lost or failed

| Intel® Server System H2000 Load with 2x 1200W supplies | Intel® Server System H2000 Load with 2x 1600W supplies | System Power Redundancy Mode | System behavior with one PSU AC lost or failed |
|--|--|------------------------------|--|
| <1200W | <1600W | Unconstrained Redundant Mode | No system throttling. All 4 nodes work normally. |
| 1200W < current load < 1800W | 1600W < current load < 2160W | Optimal Redundant Mode | 1. With BIOS setting “server management - shutdown policy” set to “disable”, all nodes in the system may be throttled to maintain power. This may cause lower performance. 2. With BIOS “server management - shutdown policy” set to “enable”, Nodes 3 and 4 will shut down while Nodes 1 and 2 keep running without throttling. Node 1 and Node 2 will have no performance loss. |
| >1800W | >2160W | Non Redundant Mode | All nodes in the system may shutdown. |

3.5 Control And Indicator Functions

The following sections define the input and output signals from the power supply.

Signals that can be defined as low true use the following convention: **Signal[#]** = low true

3.5.1 PSON# Input Signal

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +12V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +12VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to the following table for the timing diagram.

Table 30. PSON# Signal Characteristics.

| Signal Type | Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply. | |
|---|--|---------|
| PSON# = Low | ON | |
| PSON# = High or Open | OFF | |
| | MIN | MAX |
| Logic level low (power supply ON) | 0V | 1.0V |
| Logic level high (power supply OFF) | 2.0V | 3.46V |
| Source current, $V_{pson} = \text{low}$ | | 4mA |
| Power up delay: $T_{pson_on_delay}$ | 5msec | 400msec |
| PWOK delay: T_{pson_pwok} | | 50msec |

3.5.2 PWOK (power good) Output Signal

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See the table below for a representation of the timing characteristics of PWOK. The start of the PWOK delay time should be inhibited as long as any power supply output is in current limit.

Table 31. PWOK Signal Characteristics

| Signal Type | | |
|---|--------------|------------------------|
| PWOK = High | Power OK | |
| PWOK = Low | Power Not OK | |
| | MIN | MAX |
| Logic level low voltage, $I_{sink}=400\mu\text{A}$ | 0V | 0.4V |
| Logic level high voltage, $I_{source}=200\mu\text{A}$ | 2.4V | 3.46V |
| Sink current, PWOK = low | | 400 μA |
| Source current, PWOK = high | | 2mA |
| PWOK delay: T_{pwok_on} | 100ms | 1000ms |
| PWOK rise and fall time | | 100 Ωsec |
| Power down delay: T_{pwok_off} | 1ms | 200msec |

3.5.3 SMBAlert# Signal

This signal indicates that the power supply is experiencing a problem that the user should investigate. This should be asserted due to Critical events or Warning events. The signal should activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

This signal is to be asserted in parallel with LED turning solid Amber or blink Amber.

Table 32. SMBAlert# Signal Characteristics

| | | |
|--|--|-------------|
| Signal Type (Active Low) | Open collector/drain output from power supply. Pull-up to VSB located in system. | |
| Alert# = High | OK | |
| Alert# = Low | Power Alert to system | |
| | MIN | MAX |
| Logic level low voltage, Isink=4 mA | 0 V | 0.4 V |
| Logic level high voltage, Isink=50 μ A | | 3.46 V |
| Sink current, Alert# = low | | 4 mA |
| Sink current, Alert# = high | | 50 μ A |
| Alert# rise and fall time | | 100 μ s |

3.6 Protection circuits

Protection circuits inside the power supply must cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON# cycle HIGH for 1sec should be able to reset the power supply.

3.6.1 Current Limit (OCP)

The power supply must have current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply must shutdown and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply should not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

Table 33. Over Current Protection

| Output VOLTAGE | Input voltage range | OVER CURRENT LIMITS | |
|---------------------|---------------------|---------------------|--------------------|
| PSU SKU | | 1200W | 1600W |
| +12V | 90 – 264VAC | 140A min; 170A max | 180A min; 200A max |
| +12V _{STB} | 90 – 264VAC | 2.5A min; 3A max | 2.5A min; 3A max |

3.6.2 Over Voltage Protection (OVP)

The power supply over voltage protection should be locally sensed. The power supply must shutdown and latch off after an over voltage condition occurs. This latch should be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage must never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage must never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing OVP limit.

Table 34. Over Voltage Protection (OVP) Limits

| Output Voltage | MIN (V) | MAX (V) |
|----------------|---------|---------|
| +12V | 13.3 | 14.5 |
| +12VSB | 13.3 | 14.5 |

3.6.3 Over Thermal protection

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition, the PSU will shut down. When

the power supply temperature drops to within specified limits, the power supply should restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin, such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level must have a minimum of 4°C of ambient temperature margin.

3.7 PMBus*

The PMBus* features are requirements for power supply unit for use in server systems. This specification is based on the *PMBus* Specifications part I and II, revision 1.1*. The power supply device address locations are shown below:

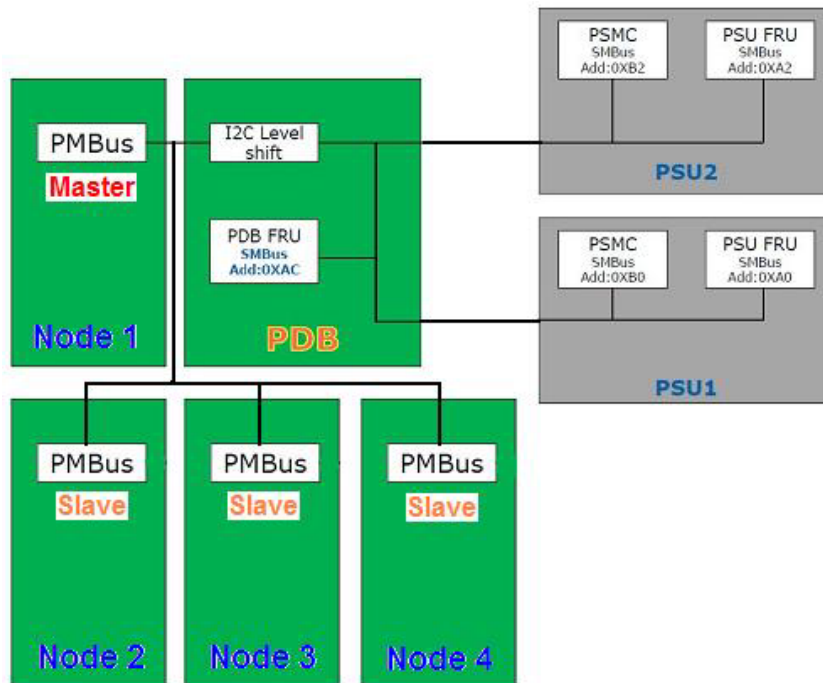


Figure 16. Power Supply Device Address

The PMBus* from PDB is connected to BMC of all four nodes. Only one board BMC is assigned to be the master BMC and communicate with PSU as single point. Other board BMCs get the PSU data from the master BMC. In case the master BMC is down, one of the slave board BMC will be promoted automatically as the master BMC and maintain the communication.

3.7.1 PSU Address Lines A0

Address pins A0 is used by end use system to allocate unit address to a power supply in particular slot position.

For redundant systems, there are two signals to set the address location of the power supply once it is installed in the system; Address0 and Address1. For non-redundant systems, the power supply device address locations should align with the Address0 / Address1 location of 0/0.

Table 35. PSU addressing

| | | |
|----------------------------|-----|-----|
| PDB addressing Address0 | 0 | 1 |
| Power supply PMBus* device | B0h | B2h |

3.7.2 Accuracy

The sensor commands must meet the following accuracy requirements. The accuracies must be met over the specified ambient temperature and the full range of rated input voltage.

Table 36. PMBus* Accuracy

| Output Loading | 10% - 20% | > 20% - 50% | > 50% - 100% |
|-----------------------|------------------|-------------|--------------|
| READ_PIN and READ_EIN | See graphs below | | |
| READ_FAN | +/-500 RPM | | |
| READ_IOUT | +/-5% | +/-2% | +/-2% |
| READ_TEMPERATURE | +/- 3°C | | |

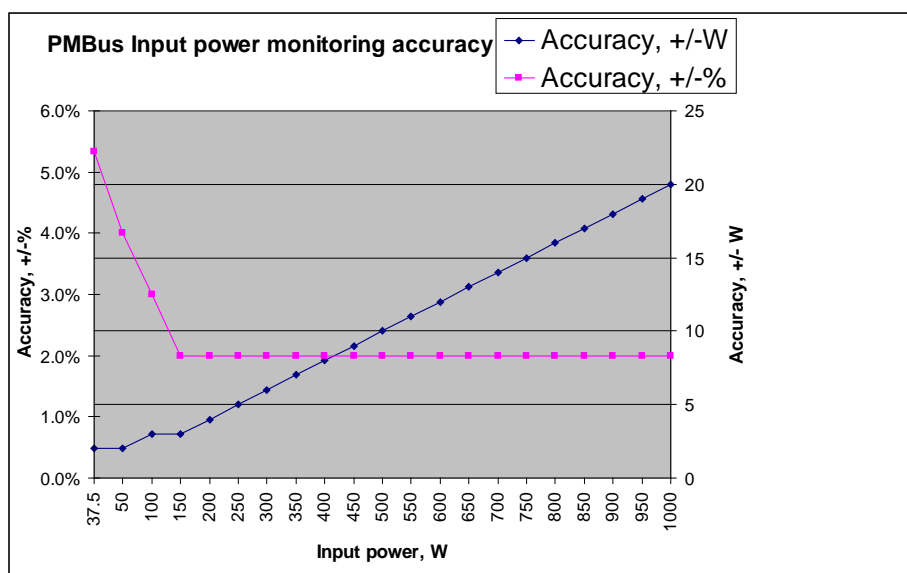


Figure 17. PMBus* Monitoring Accuracy

3.8 Power Management Policy

When working with Intel® Server Board S2600WP, the BMC on each node will monitor its fans and temperature for critical failures. When there is a fan failure and a critical temperature event at the same time the node will be powered down. When this occurs, the node will need to be manually powered back on.

Additionally on Intel® Server Board S2600WP, the BMC on node 3 and node 4 will monitor for a power supply over current condition or power supply over temperature condition. If either of these occurs and the Shutdown Policy has been enabled, then the node will be powered down. When this occurs, the node will need to be manually powered back on; but if the over current or over temperature event is detected again, the node will be powered back off.

The Shutdown Policy setting is only shown on Node 3 and Node 4, and is disabled by default, but can be enabled or disabled in the BIOS setup Server Management page or by using the *Set Shutdown Policy* command.

4. Cooling Sub-System

The chassis cooling system contains the fan cooling sub-system of each node and common fan cooling in the power supply units. Both node fans and PSU fans work together as thermal solution to the chassis.

For each node, several components and configuration requirements make up the cooling sub-system. These include processor heatsinks, chipset heatsinks, VR heatsinks, system fan module, CPU air duct, and drive bay population. All are necessary to provide and regulate the air flow and air pressure needed to maintain the system's thermals when operating at or below the maximum specified thermal limits.

In order to maintain the necessary airflow within the system, you must properly install the air duct, HDD dummy carrier, PSU dummy filler, and the top cover.

Each node uses a variable fan speed control engine to provide adequate cooling for the node and whole system at various ambient temperature conditions, under various server workloads, and with the least amount of acoustic noise possible. The fans operate at the lowest speed for any given condition to minimize acoustics.

Note: The server system does not support redundant cooling fans. If any of the node fans fail, you must power down the respective node as soon as possible to replace the fan.

4.1 Processor Heatsink

Both processor heatsinks are included in the system package. Each heatsink is designed for optimal cooling and performance in the H2600WP system. To achieve better cooling performance, you must properly attach the heatsink bottom base with TIM (thermal interface material). ShinEtsu* G-751 or ShinEtsu* 7783D or Honeywell* PCM45F TIM is recommended. The mechanical performance of the heatsink must satisfy mechanical requirement of Intel® Xeon® E5-2600 and E5-2600 v2 series processors. To keep chipsets and VR temperature at or below maximum temperature limit, the heatsink is required even if no processor is installed.

Note: The processor heatsink for CPU1 and CPU2 are different. FXXCA84X106HS (Cu base-Al fin Heatsink) is for CPU1, while FXXEA84X106HS (Al-extruded Heatsink) is for CPU2. Mis-locating the heatsink will cause serious thermal damage!

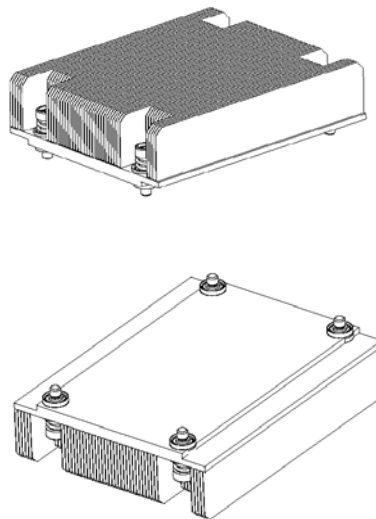
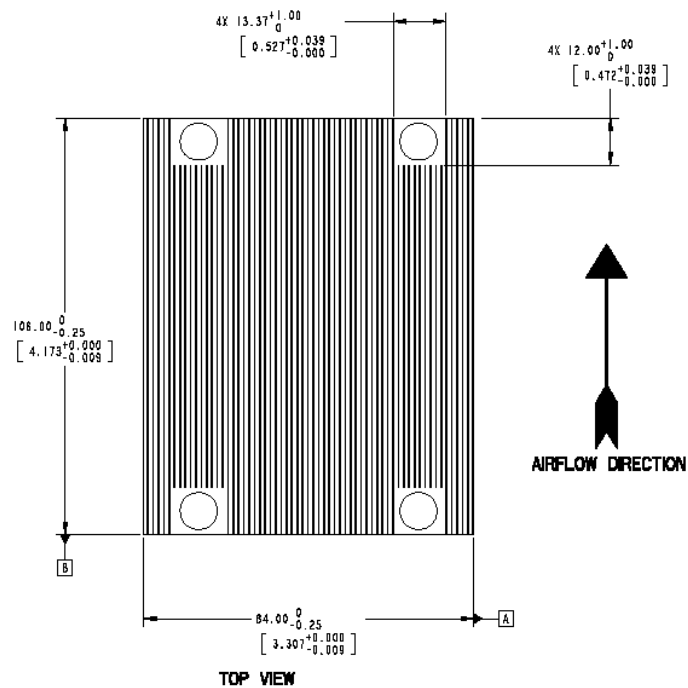


Figure 18. Processor Heatsink Overview

Note: The passive heatsink is Intel® standard thermal solution for 1U/2U rack chassis.

4.2 Node cooling Fans

The cooling subsystem for each node consists of three 40 x 40 x 56 dual rotor fan, and CPU air duct. These components provide the necessary cooling and airflow to the system node.

To maintain the necessary airflow within the system, the air duct and the top cover must be properly installed.

Note: The Intel® Server System H2312WP Family which supports up to 12 units of 3.5" storage drives does not support redundant cooling. If one of the node fan fails, it is recommended to

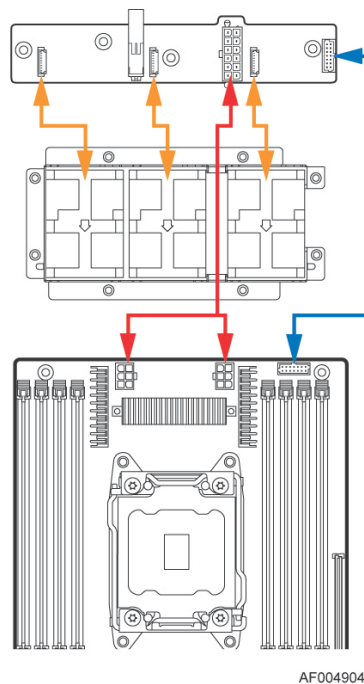
replace the failed fan as soon as possible. However, the system design still reserves limited thermal margin to fan failure.

The Intel® Server System H2216WP Family which supports up to 16 units of 2.5" storage drives does support optimal redundant cooling. Certain level of CPU throttling will occur during fan fail but the percent is below 1% which is considered to be acceptable from thermal perspective. For TDP 130W CPU configuration, the confidence level of system exit air temperature to meet 70°C is 98% which is acceptable. For TDP 95W CPU configuration, the system exit air temperature can meet 70°C spec. All other system components are within the thermal specification.

Each fan within the node is capable of supporting multiple speeds. Fan speed changes automatically when internal ambient temperature of the system or processor temperature changes. The fan speed control algorithm is programmed into the server board's BMC software.

Each fan connector within the module supplies a tachometer signal that allows the BMC to monitor the status of each fan. If one of the fans should fail, the system fault LED on front panel will light.

The fan control signal is from BMC on mother board to Node Docking Board and then distribute to three sets of dual rotor fans. See the following figure for detail.



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| |
|---|
| Yellow Lines: Fan cable connection |
| Red line: Base board power cable connection |
| Blue line: Fan control signal cable connection |

Figure 19. Node Fan Set and power/control Connection

The fan connector pin-out definition is as follows:

Table 37. 8-pin Connector Pin-Out for Node Dual Rotor Fans

| Pin | Signal Name | Description |
|-----|-------------|-------------------------|
| 1 | GND | Ground |
| 2 | P12V | Power Supply +12 V |
| 3 | Tach1 Out | FAN_TACH1 signal output |
| 4 | PWM1 In | PWM1 signal input |
| 5 | GND | Ground |
| 6 | P12V | Power Supply +12 V |
| 7 | Tach2 Out | FAN_TACH2 signal output |
| 8 | PWM1 In | PWM1 signal input |

4.3 Power Supply Fan

Each power supply module supports one non-redundant dual rotor 40 mm fan. The fans control the cooling of the power supply and some drive bays. These fans are not replaceable. Therefore, if a power supply fan fails, you must replace the power supply module.

4.4 Air Duct Module

Each node requires the use of an air duct module to direct airflow over critical areas within the node. Before slide the node tray into chassis, make sure the air duct is installed properly.

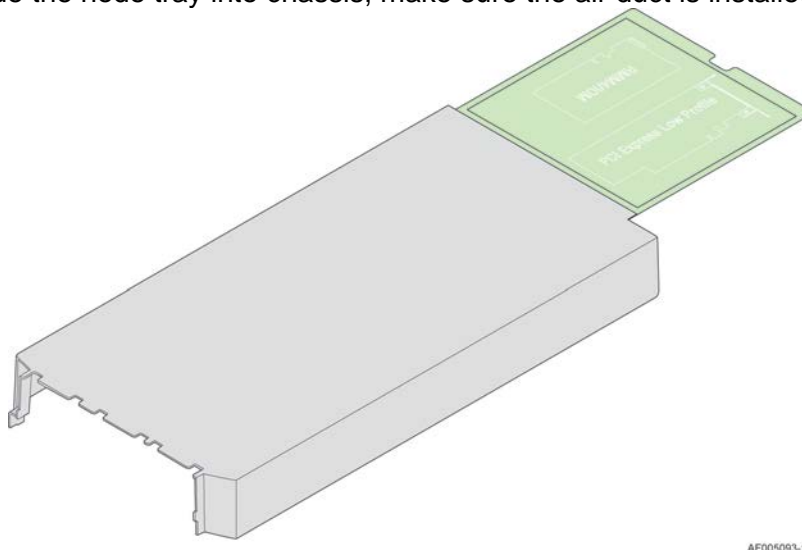


Figure 20. Compute Node Air Duct

4.5 Drive Bay Population Requirement

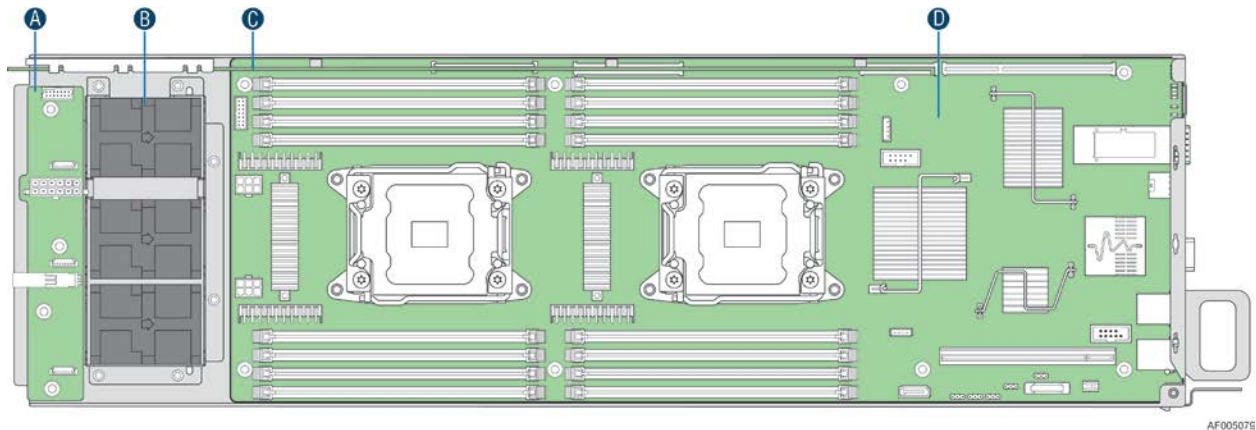
In order to maintain system thermal requirements, you must fully populate all hard drive bays. Hard drive trays used for hot-swap drives must either have a hard drive installed or not have a hard drive installed.

If only one power supply unit is used, a PSU dummy filler must be used to match the airflow requirement.

IMPORTANT NOTE: If the drive bay is missing or not fully populated, the system will not meet the thermal cooling requirements of the processor, which will most likely result in degraded performance as a result of throttling or thermal shutdown of the system. It is recommended to keep/apply the dummy plastic blocker (as shipped with HDD carrier) on any blank HDD carrier.

5. System Boards in the Node Tray

The Node tray includes mother board, node docking board, bridge board, and node fan set.



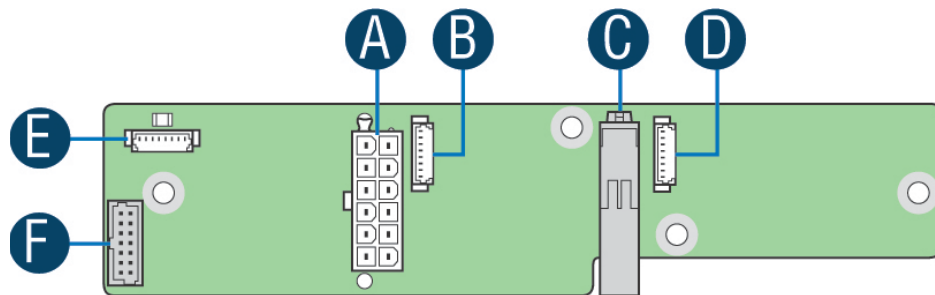
| | |
|----------|--------------------|
| A | Node Docking Board |
| B | Node Fan Set |
| C | Bridge Board |
| D | Baseboard |

Figure 21. Compute Node Tray Overview

5.1 Node Docking Board

5.1.1 Overview of Node Docking Board

The Node Docking Board provides hot swap docking of 12V main power between the compute node and the server. It supports three dual rotor fan connections, 12V main power hot swap controller, and current sensing.



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| | |
|----------|--|
| A | 2x6 pin Minit Jr main power output connector |
| B | 8 pin connector for node fan 2 |
| C | 12 pin connector for main power input |
| D | 8 pin connector for node fan 3 |
| E | 8 pin connector for node fan 1 |
| F | 2x7 pin fan control connector |

Figure 22. Node Docking Board

The Node Docking Board implements the below features:

- Main 12V hot swap connectivity between compute node and chassis power.
- Current sensing of 12V main power for use with node manager.
- One 2x6pin mini-fit jr high current connectors for cabling to either the HW baseboard or a GPGPU card. Different cable lengths will be needed for the different depth HW baseboards.
- 2x7pin fan single connector, discrete cabled to the HW baseboard.
- Three 8pin dual rotor fan connectors.
- Four loose screws used to secure board to the compute node.

5.1.2 Pinout definition on Node Docking Board

Below is a list of connector type and pin definition on Node Docking Board.

Table 38. Main Power Input Connector

| Pin | Signal Description | Pin | Signal Description |
|-------------------------|--------------------|-----|--------------------|
| Lower Blade (Circuit 1) | | | |
| 1 | GND | 2 | GND |
| 3 | GND | 4 | GND |
| 5 | GND | 6 | GND |
| Upper Blade (Circuit 2) | | | |
| 7 | P12V | 8 | P12V |
| 9 | P12V | 10 | P12V |
| 11 | P12V | 12 | P12V |

Table 39. Fan Control Signal Connector

| Pin | Signal Description | Pin | Signal Description |
|-----|--------------------|-----|--------------------|
| 1 | PWM1 | 2 | Reserved |
| 3 | Tach0 | 4 | Tach1 |
| 5 | Tach2 | 6 | Tach3 |
| 7 | Tach4 | 8 | Tach5 |
| 9 | NODE_ON | 10 | GND |
| 11 | SMBUS_R4 CLK | 12 | SMBUS_R4 DAT |
| 13 | NODE_ADR0 | 14 | NODE_PWRGD |

Table 40. Node Fan Connector

| Pin | Signal Description |
|-----|--------------------|
| 1 | GND |
| 2 | P12V |
| 3 | TACH1 |
| 4 | PWM1 |
| 5 | GND |
| 6 | P12V |
| 7 | TACH2 |
| 8 | PWM1 |

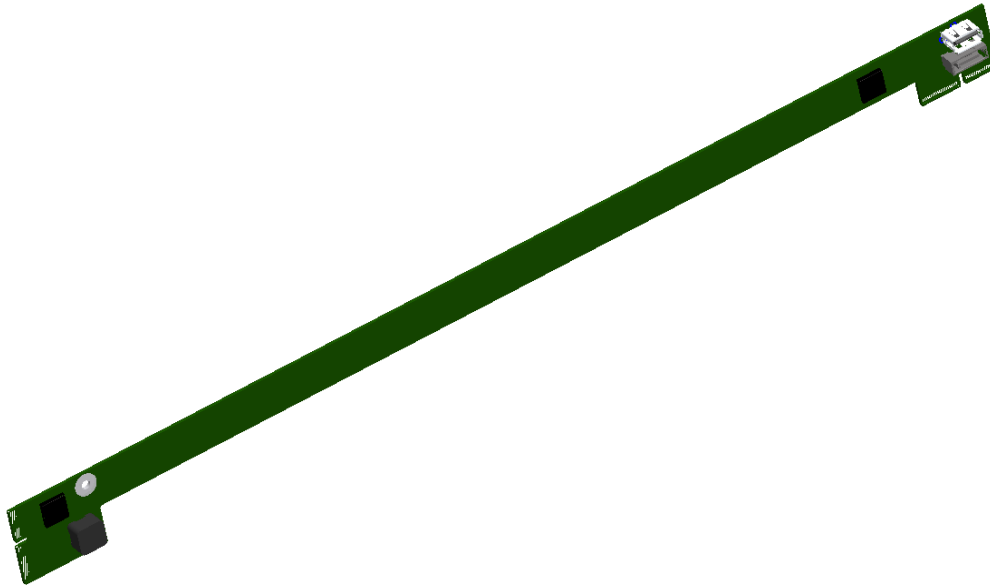
Table 41. Main Power Output Connector

| Pin | Signal Description | Pin | Signal Description |
|-----|--------------------|-----|--------------------|
| 1 | GND | 7 | P12V_HS |
| 2 | GND | 8 | P12V_HS |
| 3 | GND | 9 | P12V_HS |
| 4 | GND | 10 | P12V_HS |
| 5 | GND | 11 | P12V_HS |
| 6 | GND | 12 | P12V_HS |

5.2 Bridge Board

5.2.1 Overview of Bridge Board

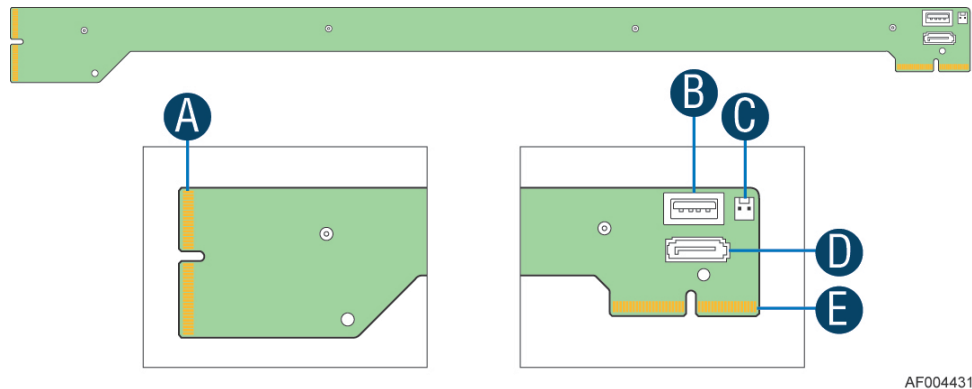
The Bridge Board provides hot swap interconnect of all electrical signals to the backplane of the server chassis (except for main 12V power). It supports up to 4x lanes of SAS/SATA, a 7-pin SATA connector for SATA DOM devices, and type-A USB connector for USB flash device. One Bridge Board is used per one compute node. The Bridge Board is secured with three loose screws to the compute node tray.

**Figure 23. Bridge Board Overview**

Bridge board passes all electrical connectivity through a 2x40pin card edge hot swap interconnect between compute node and chassis backplane. The bridge board passes the follow features (per compute node) to the backplane of the server:

- 4x 6Gb SAS/SATA ports for HSBP drives. (Intel® Server Board S2600WP and S2600WPQ family on board SCU supports 3Gb SAS/SATA while the bridge board and the HSBP of Intel® Server System H2000WP family support 6Gb SAS/SATA drives.)
- Two x4 lane 6Gb SAS/SATA re-drivers.
- Four chassis ID signals to determine the physical location of the compute node.
- One SGPIO SFF-8485 interface to the HSBP microcontroller.

- 5V_AUX power generated on HSBP and provided to the compute node.
- 3.3V power generated on HSBP and provided to bridge board to run SAS/SATA re-drivers.
- Global PMBus* alert signal for CLST support.
- Four SMBus interfaces:
 - SMBUS* R1 - For chassis temp sensor and chassis FRU EEPROM device.
 - SMBUS* R5 - Connectivity for up to two HSBP controllers and one shared 12V current monitoring device.
 - SMBUS* R7 - Connectivity for up to two common redundant power supply (CRPS) module PMBus*.
 - IPMB - For OEM requirement not used on EPSD HW servers.
 - Front panel button signals: Power, reset, NMI, and ID.
 - Front panel LEDs signals: Power, fault, status, fabric activity, ID, HDD activity.
- One 7-pin 6Gb SATA port connector for DOM device docking to the bridge board.
- USB2.0 interface to a 4-pin type-A connector for flash device docking to bridge board.
- 2-Pin 5V_AUX power for the SATA DOM in need of cabling power.
- Power connector for SATA DOM.



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| | |
|----------|--|
| A | 2x40 pin card edge connector (to backplane) |
| B | USB 2.0 Type-A connector |
| C | 2-pin 5V_AUX power |
| D | AHCI SATA0 DOM port connector |
| E | 2x40 pin card edge connector (to baseboard slot) |

Figure 24. Connectors on Bridge Board

5.2.2 Pinout definition on Bridge Board

The table below lists the connector type and pin definition for a Bridge Board.

Table 42. Card Edge Connector Pinout

| Pin | Signal Description | Pin | Signal Description |
|-----|--------------------|-----|--------------------|
| 1 | 5V Aux | 2 | 5V Aux |
| 3 | SATA0_TXN | 4 | USB2_OC |

| Pin | Signal Description | Pin | Signal Description |
|-----|--|-----|---|
| 5 | SATA0_TXP | 6 | GND |
| 7 | GND | 8 | SATA0_RXN |
| 9 | NODE_PRESENT_N (GND) | 10 | SATA0_RXP |
| 11 | ALL_NODE_OFF | 12 | GND |
| 13 | spare | 14 | USB2_P0P |
| 15 | GND | 16 | USB2_P0N |
| 17 | IPMB-Data | 18 | GND |
| 19 | IPMB-Clk | 20 | FP HDD_ACT_LED_N |
| 21 | GND | 22 | FP Activity LED_N |
| 23 | SMBUS_R1 DATA | 24 | FP Health LEDA_N |
| 25 | SMBUS_R1 CLK | 26 | FP Health LEDG_N |
| 27 | GND | 28 | FP PWR LED_N |
| 29 | SMBUS_R5 DATA | 30 | FP ID LED_N |
| 31 | SMBUS_R5 CLK | 32 | FP ID BTN_N |
| 33 | GND | 34 | FP RST BTN_N |
| 35 | SMBUS_R7 DATA | 36 | FP PWR BTN_N |
| 37 | SMBUS_R7 CLK | 38 | FP NMI BTN_N |
| 39 | GND | 40 | SPA_SOUT_N |
| 41 | PMBUS Alert_N | 42 | SPA_SIN_N |
| 43 | NODEx_ON_N | 44 | ID3 |
| 45 | SGPIO DATA IN | 46 | ID2 |
| 47 | SGPIO Data Out | 48 | ID1 |
| 49 | SGPIO LD | 50 | ID0 |
| 51 | SPKR | 52 | SGPIO CLK |
| 53 | GND | 54 | GND |
| 55 | SAS3_RX | 56 | SAS3_TX |
| 57 | SAS3_RX | 58 | SAS3_TX |
| 59 | GND | 60 | GND |
| 61 | SAS2_TX | 62 | SAS2_RX |
| 63 | SAS2_TX | 64 | SAS2_RX |
| 65 | GND | 66 | GND |
| 67 | SAS1_RX | 68 | SAS1_TX |
| 69 | SAS1_RX | 70 | SAS1_TX |
| 71 | GND | 72 | GND |
| 73 | SAS0_TX | 74 | SAS0_RX |
| 75 | SAS0_TX | 76 | SAS0_RX |
| 77 | GND | 78 | GND |
| 79 | P3V3 (HSBP Side) and GND (HW Baseboard Side) | 80 | P3V3 (HSBP Side) and SATA_SAS_N (HW Baseboard Side) |

The SATA DOM used on SATA0 port can be either powered by the SATA port, or using external power from 5V-AUX connector.

Table 43. AHCI SATA0 DOM Connector Pinout

| Pin | Signal Description |
|-----|--------------------|
| 1 | GND |

| Pin | Signal Description |
|-----|--------------------|
| 2 | SATA0_TXP |
| 3 | SATA0_TXN |
| 4 | GND |
| 5 | SATA0_RXN |
| 6 | SATA0_RXP |
| 7 | P5V_SATA/GND |

Table 44. USB 2.0 Type-A Connector Pinout

| Pin | Signal Description |
|-----|--------------------|
| 1 | P5V_USB |
| 2 | USB2_P0N |
| 3 | USB2_P0P |
| 4 | GND |

Table 45. 5V_AUX Power Connector Pinout

| Pin | Signal Description |
|-----|--------------------|
| 1 | GND |
| 2 | P5V |

5.3 Spare Bridge Board to support 6Gbs SAS

This bridge board is designed support 6Gbs SAS signal from internal SAS RAID card or SAS ROC. This bridge board will not connect to SCU ports from baseboard but make all other power and control signals available to backplane. It will ship together with a dedicated SAS cable as a spare of the system.

5.3.1 Overview of Bridge Board

The Bridge Board is a spare board across all baseboards going into the H2000WP serials server chassis, to upgrade the system for 6Gbs SAS support. The Bridge Board provides hot swap interconnect of all electrical signals to the backplane of the server chassis (except for main 12V power). It supports up to 4x lanes of SAS/SATA and one mini SAS connector for cable connection to PCIe based RAID card or SAS ROC. One Bridge Board is used per one compute node. The Bridge Board is secured with several loose screws to the compute node tray.

A dedicated mini SAS cable is shipped together with the bridge board, which is mechanically fitted into the node tray.

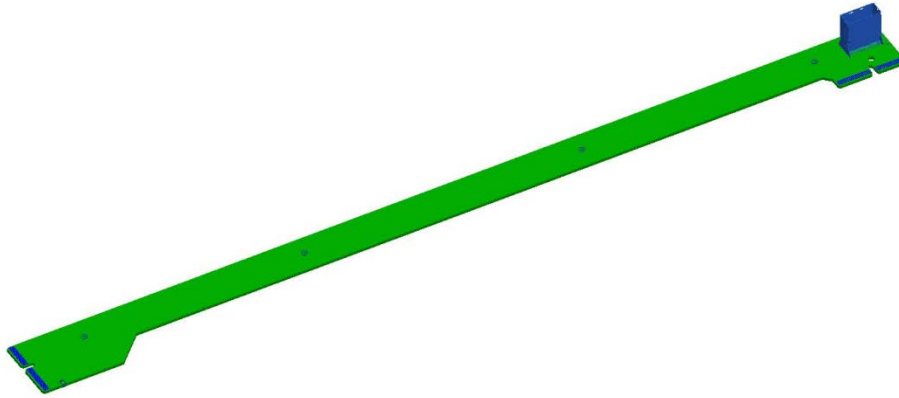
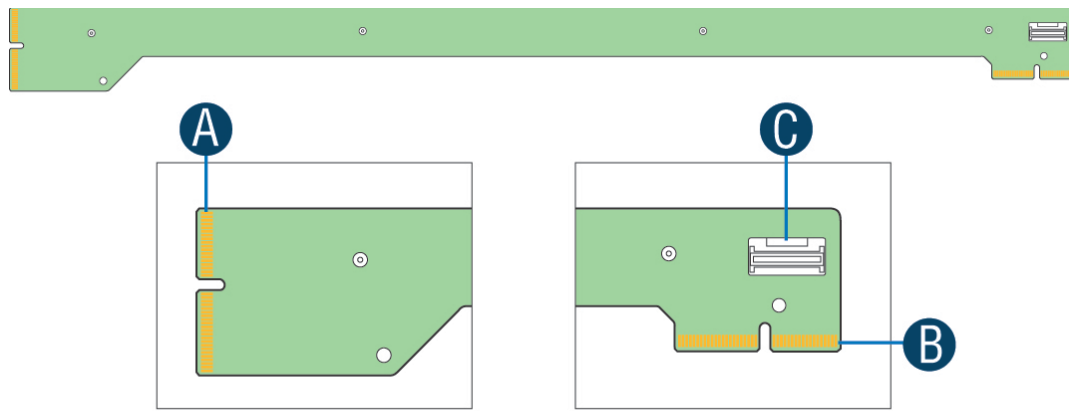


Figure 25. SAS 6Gbps Bridge Board Overview

This bridge board passes all electrical connectivity through a 2x40pin card edge hot swap interconnect between compute node/SAS RAID card and chassis backplane. The bridge board passes the follow features (per compute node) to the backplane of the server:

- 4x 6Gb SAS/SATA signals through Mini SAS port to HSBP drives.
- Two x4 lane 6Gb SAS/SATA re-drivers.
- Four chassis ID signals to determine the physical location of the compute node.
- One SGPIO SFF-8485 interface to the HSBP microcontroller.
- 5V_AUX power generated on HSBP and provided to the compute node.
- 3.3V power generated on HSBP and provided to bridge board to run SAS/SATA re-drivers.
- Global PMBus* alert signal for CLST support.
- Four SMBus* interfaces:
 - SMBUS R1 - For chassis temp sensor and chassis FRU EEPROM device.
 - SMBUS R5 - Connectivity for up to two HSBP controllers and one shared 12V current monitoring device.
 - SMBUS R7 - Connectivity to up to two common redundant power supply (CRPS) module PMBus*.
 - IPMB - For OEM requirement not used on EPSD HW servers.
 - Front panel button signals: Power, reset, NMI, and ID.
 - Front panel LEDs signals: Power, fault, status, fabric activity, ID, HDD activity.



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| | |
|----------|---|
| A | 2x40 pin card edge connector (to backplane) |
| B | 2x40 pin card edge connector (to baseboard bridge slot) |
| C | 4-port Mini SAS Connector |

Figure 26. Connectors and components on Spare Bridge Board

5.3.2 Pinout definition on SAS 6Gbps Bridge Board

The table below lists the connector pin definition on the Bridge Board.

Table 46. Pinout of Card Edge to BaseBoard

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|-----|--------------------|-----|---------------|-----|----------------|-----|----------------|
| 1 | 5V_AUX | 2 | 5V_AUX | 41 | PMBUS_ALERT_N | 42 | SPA_SIN |
| 3 | N/C | 4 | USB2_OC | 43 | NODE_ON_N | 44 | IBMC_NODEID_3 |
| 5 | N/C | 6 | GND | 45 | SGPIO_DATA_IN | 46 | IBMC_NODEID_2 |
| 7 | GND | 8 | N/C | 47 | SGPIO_DATA_OUT | 48 | IBMC_NODEID_1 |
| 9 | NODE_PRESENT_N | 10 | N/C | 49 | SGPIO_LOAD | 50 | IBMC_NODEID_0 |
| 11 | ALL_NODE_OFF | 12 | GND | 51 | SPEAKER_IN | 52 | N/C |
| 13 | N/C | 14 | N/C | 53 | GND | 54 | GND |
| 15 | GND | 16 | N/C | 55 | N/C | 56 | N/C |
| 17 | IPMB_DATA | 18 | GND | 57 | N/C | 58 | N/C |
| 19 | IPMB_CLK | 20 | LED_HDD_ACT_N | 59 | GND | 60 | GND |
| 21 | GND | 22 | FP_ACT_LED_N | 61 | N/C | 62 | N/C |
| 23 | SMB_SNSR_DATA | 24 | FP_LED_STSA_N | 63 | N/C | 64 | N/C |
| 25 | SMB_SNSR_CLK | 26 | FP_LED_STSG_N | 65 | GND | 66 | GND |
| 27 | GND | 28 | FP_PWR_LED_N | 67 | N/C | 68 | N/C |
| 29 | SMB_HSBP_DATA | 30 | FP_ID_LED_N | 69 | N/C | 70 | N/C |
| 31 | SMB_HSBP_CLK | 32 | FP_ID_BTN_N | 71 | GND | 72 | GND |
| 33 | GND | 34 | FP_RST_BTN_N | 73 | N/C | 74 | N/C |
| 35 | SMB_PMBUS_DAT A | 36 | FP_PWR_BTN_N | 75 | N/C | 76 | N/C |
| 37 | SMB_PMBUS_CLK | 38 | FP_NMI_BTN_N | 77 | GND | 78 | GND |
| 39 | GND | 40 | SPA_SOUT | 79 | GND | 80 | SAS_SATA_SET_N |

Table 47. Pinout of Card Edge to Hot Swap Back Plane

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|-----|----------------|-----|---------------|
| 1 | 5V_AUX | 2 | 5V_AUX | 41 | PMBUS_ALERT_N | 42 | SPA_SIN |
| 3 | N/C | 4 | N/C | 43 | NODE_ON_N | 44 | IBMC_NODEID_3 |
| 5 | N/C | 6 | GND | 45 | SGPIO_DATA_IN | 46 | IBMC_NODEID_2 |
| 7 | GND | 8 | N/C | 47 | SGPIO_DATA_OUT | 48 | IBMC_NODEID_1 |

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|-----|----------------|-----|---------------|-----|--------------|-----|---------------|
| 9 | NODE_PRESENT_N | 10 | N/C | 49 | SGPIO_LOAD | 50 | IBMC_NODEID_0 |
| 11 | ALL_NODE_OFF | 12 | GND | 51 | SPEAKER_IN | 52 | SGPIO_CLOCK |
| 13 | 3V3_AUX | 14 | N/C | 53 | GND | 54 | GND |
| 15 | GND | 16 | N/C | 55 | SAS3_RX_BP_N | 56 | SAS3_TX_BP_N |
| 17 | IPMB_DATA | 18 | GND | 57 | SAS3_RX_BP_P | 58 | SAS3_TX_BP_P |
| 19 | IPMB_CLK | 20 | LED_HDD_ACT_N | 59 | GND | 60 | GND |
| 21 | GND | 22 | FP_ACT_LED_N | 61 | SAS2_TX_BP_N | 62 | SAS2_RX_BP_N |
| 23 | SMB_R1_DATA | 24 | FP_LED_STSA_N | 63 | SAS2_TX_BP_P | 64 | SAS2_RX_BP_P |
| 25 | SMB_R1_CLK | 26 | FP_LED_STSG_N | 65 | GND | 66 | GND |
| 27 | GND | 28 | FP_PWR_LED_N | 67 | SAS1_RX_BP_N | 68 | SAS1_TX_BP_N |
| 29 | SMB_HSBP_DATA | 30 | FP_ID_LED_N | 69 | SAS1_RX_BP_P | 70 | SAS1_TX_BP_P |
| 31 | SMB_HSBP_CLK | 32 | FP_ID_BTN_R_N | 71 | GND | 72 | GND |
| 33 | GND | 34 | FP_RST_BTN_N | 73 | SAS0_TX_BP_N | 74 | SAS0_RX_BP_N |
| 35 | SMB_PMBUS_DATA | 36 | FP_PWR_BTN_N | 75 | SAS0_TX_BP_P | 76 | SAS0_RX_BP_P |
| 37 | SMB_PMBUS_CLK | 38 | FP_NMI_BTN_N | 77 | GND | 78 | GND |
| 39 | GND | 40 | SPA_SOUT | 79 | 3V3 | 80 | 3V3 |

Table 48. Pinout of Mini SAS Connector

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|-----|-------------|-----|----------------|
| A1 | GND | A10 | GND | B1 | GND | B10 | SGPIO_DATA_OUT |
| A2 | SAS0_TX_P | A11 | N/C | B2 | SAS0_RX_P | B11 | SGPIO_DATA_IN |
| A3 | SAS0_TX_N | A12 | GND | B3 | SAS0_RX_N | B12 | GND |
| A4 | GND | A13 | SAS2_TX_P | B4 | GND | B13 | SAS2_RX_P |
| A5 | SAS1_TX_P | A14 | SAS2_TX_N | B5 | SAS1_RX_P | B14 | SAS2_RX_N |
| A6 | SAS1_TX_N | A15 | GND | B6 | SAS1_RX_N | B15 | GND |
| A7 | GND | A16 | SAS3_TX_P | B7 | GND | B16 | SAS3_RX_P |
| A8 | SGPIO_CLOCK | A17 | SAS3_TX_N | B8 | SAS_BP_TYPE | B17 | SAS3_RX_N |
| A9 | SGPIO_LOAD | A18 | GND | B9 | N/C | B18 | GND |

6. Hard Disk Drive Support

The server system provides two SKUs to support different types of Hard Disk Drives (HDD):

- H2312WP: Supports 12x 3.5" HDD
- H2216WP: Supports 16x 2.5" HDD

6.1 Hard Disk Drive Bays scheme

The server system H2000 chassis can support up to twelve carrier-mounted SATA/SAS 3.5-inch hard disk drives, or sixteen carrier-mounted SATA/SAS 2.5-inch hard disk drives. The drives may be “electrically” hot-swapped while the system power is applied, but you must take caution before hot-swapping while the system is functioning under operating system / application control or data may be lost.

Below are hard disk drive distribution schemes on different SKUs of H2000 chassis family.

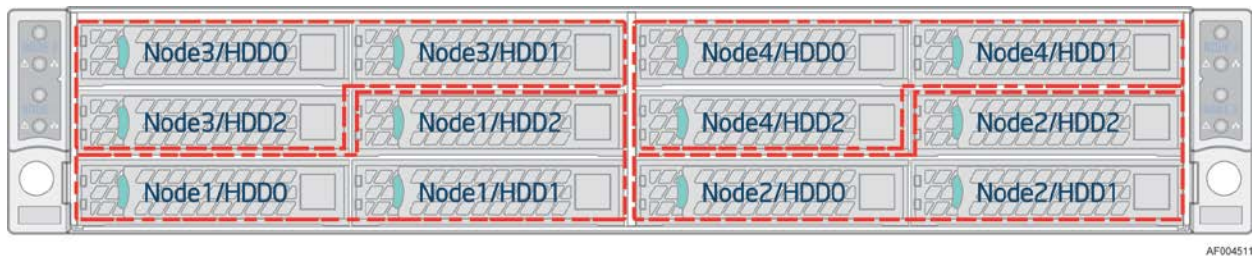


Figure 27. HDD Scheme for H2312WPGR

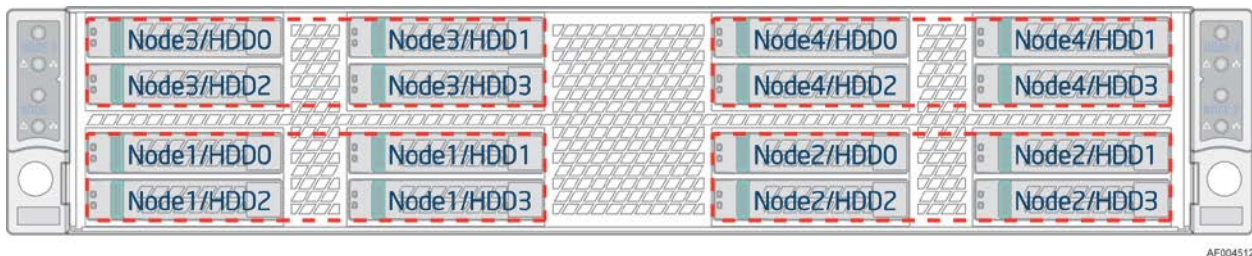


Figure 28. HDD Scheme for H2216WPGR

Note: If a failed drive needs replacing, it is recommended you replace it with the same manufacturer, model, and capacity.

6.2 Hard Drive Carrier

There are two types of HDD carriers for two chassis SKUs respectively:

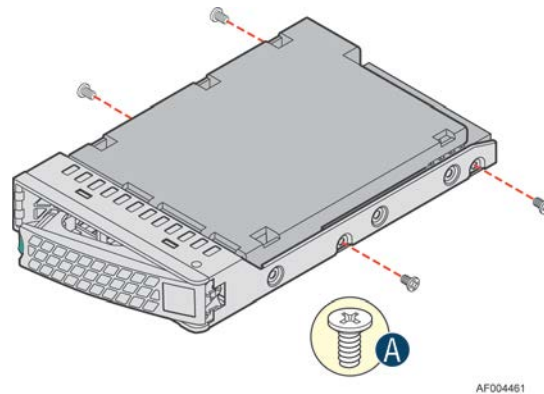


Figure 29. 3.5-inch HDD Assembly Overview

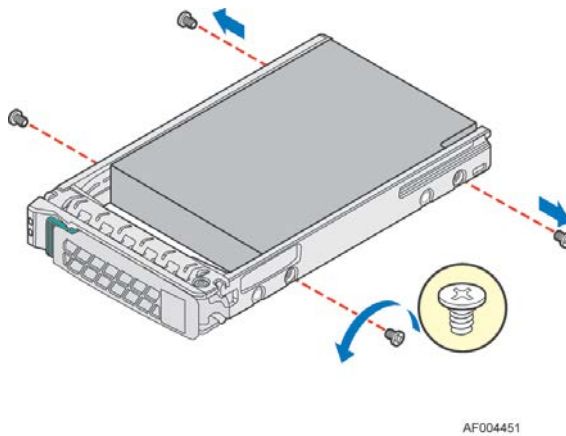


Figure 30. 2.5-inch HDD Assembly Overview

Hot-swap drive carriers make insertion and extraction of the drive from the system very simple. Each type of drive carrier has its own latching mechanism, which is used to both insert and extract drives from the chassis and lock the carrier in place. Each type of drive carrier supports two light pipes to direct light from the drive status LEDs on the backplane to the carrier's face allowing it to be viewable from the front of the system.

6.3 Hot Swap Hard Drive Support

The Intel® Server System H2000WP family can support hot-swap SATA/SAS hard drives. Hard drives interface with the passive backplane through a blind mate connection when drives are installed into a hard drive bay using hot-swap drive carriers.

The passive backplane acts as an intermediate pass-through interface board, where SATA/SAS ports of SCU0 from server board are hard wired to the backplane. The on board Intel® C600 Chipset (PCH) provides the necessary drive interface.

Each compute node in the system has dedicated Hot Swap Controller (HSC) to manage three or four HDDs. There are totally four sets of independent Programmable System On Chip (PSOC) on the backplane, to function as HSC respectively to four compute nodes.

The following sections describe the feature and connections between the backplane and server board.

6.3.1 Backplane Feature set:

- Common HSBP Microcontroller Cypress* PSoC 1 part
- **H2312WP Family:** 12x SAS/SATA 3.5" HDDs at 6Gb/s SAS/SATA or slower speeds, divided into four groups of three hot swap hard drives. Each HDD group is associated with one of the four compute nodes respectively in the 2U chassis.
- **H2216WP Family:** 16x SAS/SATA 2.5" HDDs at 6Gb/s SAS/SATA or slower speeds, divided into four groups of four hot swap hard drives. Each HDD group is associated with one of the four compute nodes respectively in the 2U chassis.
- One SGPIO SFF-8485 interface per compute node, total of four SGPIO on the backplane.
- Three SMB interfaces supported on the HSBP:
 - SMBUS* R1 - For chassis temp sensor and chassis FRU EEPROM device.
 - SMBUS* R5 - Connectivity to up to two HSBP controllers and one shared 12V current monitoring device.
 - SMBUS* R7 - Connectivity to up to two common redundant power supply (CRPS) module PMBus*.
- Integrated front panel control connectors.
- Status LED and Activity LED for each hard disk drive.
- 5V_AUX switcher regulator (from 12V and 12VSB) for HDD power and for compute nodes.
- Each grouping of HDD slots has switches for 5V and 12V power; only when corresponding compute node is plugged in and operating, will power be provided to the HDDs.
- 3.3V switcher regulator (from 12V) to power microcontroller, SAS/SATA re-drivers on the bridge board and various other components.
- 3.3V_AUX linear regulator (from 5V_AUX) for temp sensor, and chassis FRU EEPROM located on the HSBP.
- Four 80-pin bridge board connectors, one per compute node.
- Four compute node main power connectors, one per compute node.
- Four 2x9pin power cable connections and one 2x9pin power control cable connections. These cables are routing to two power distribution boards (PDB).
- Shared speaker for all compute nodes.

6.3.2 Backplane Block Diagram

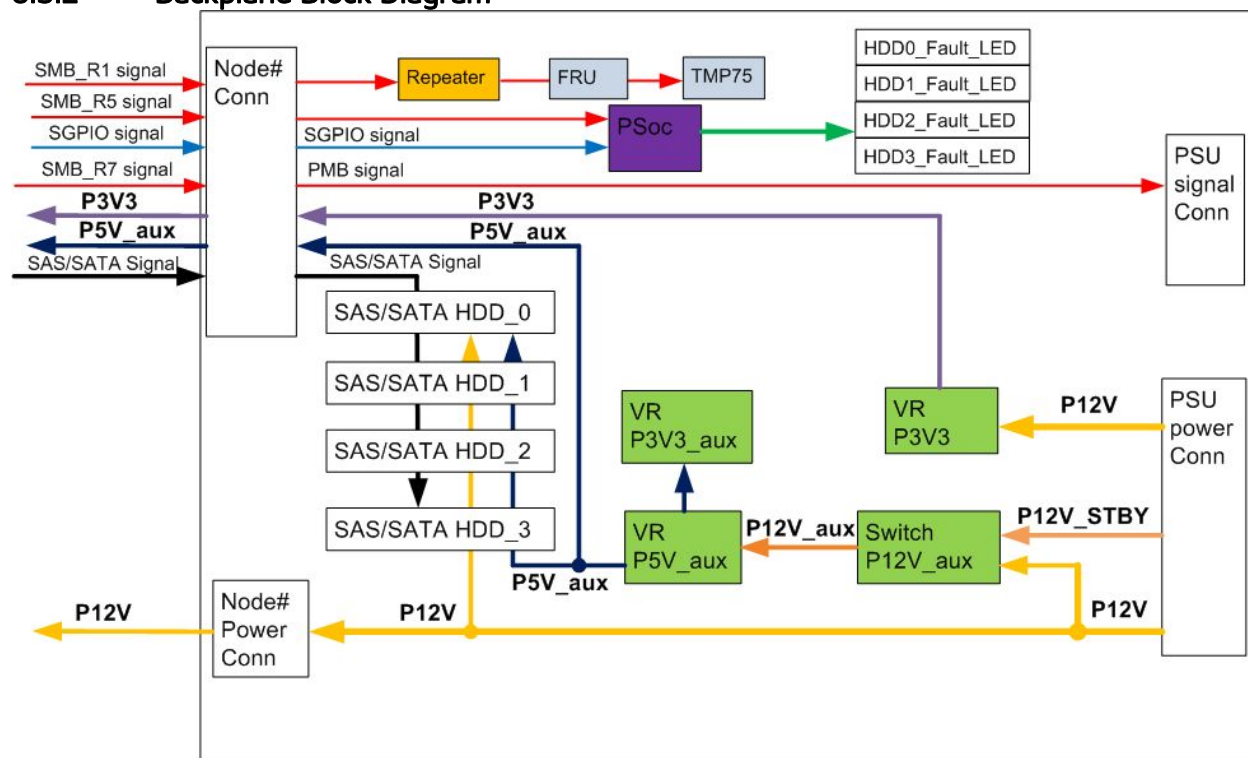
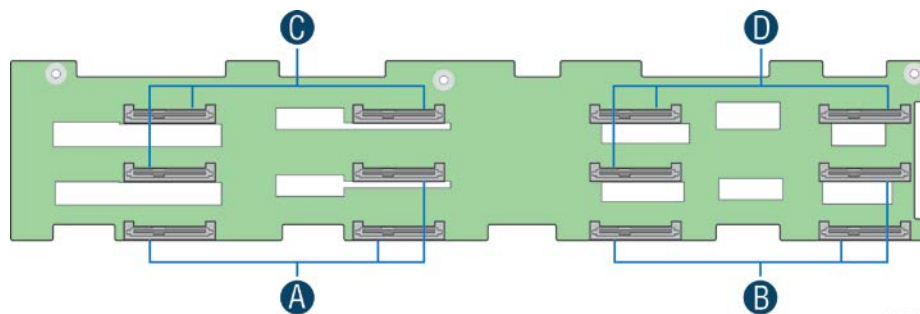


Figure 31. Passive Backplane Block Diagram (for one node)

6.3.3 3.5" Hot Swap Backplane Connector scheme

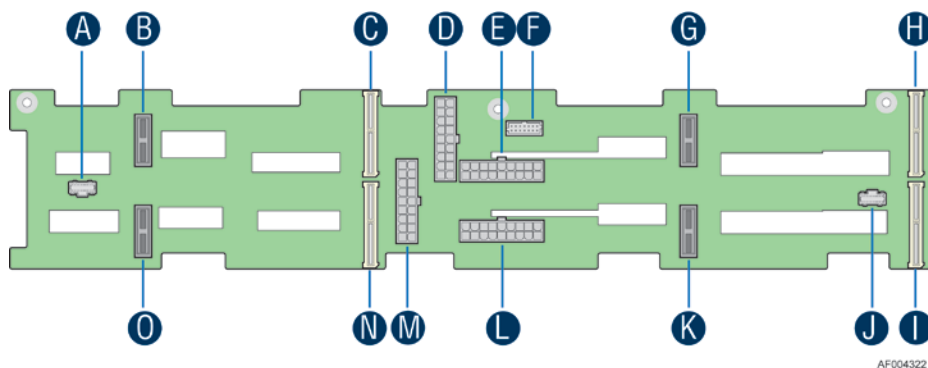
The following diagrams show the layout of major components and connectors for 3.5" Hot Swap backplane.



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| | |
|----------|--------------------------------|
| A | SATA/SAS connectors for Node 1 |
| B | SATA/SAS connectors for Node 2 |
| C | SATA/SAS connectors for Node 3 |
| D | SATA/SAS connectors for Node 4 |

Figure 32. 3.5" Backplane Component and Connectors (Front View)

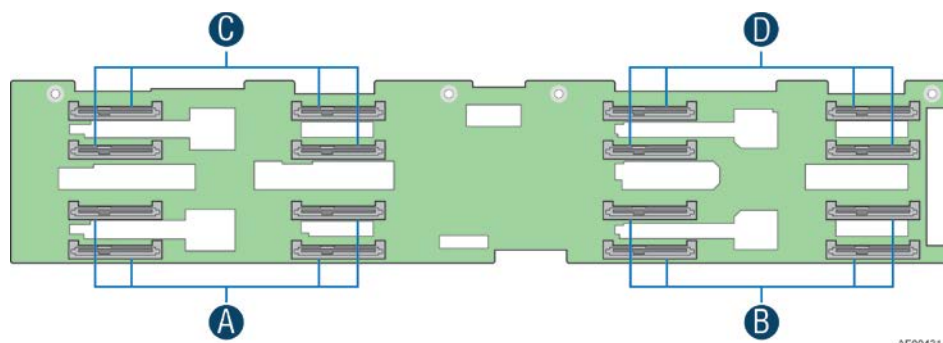


| | |
|---|--|
| A | 20-pin Front Panel cable connector for Node 2, 4 |
| B | 2-blade Compute Node Power connector for Node 4 |
| C | 2x40 pin Bridge Board connector for Node 4 |
| D | 2x9 pin Power supply input connector |
| E | 2x9 pin Power supply input connector |
| F | 2x7 pin Power Control cable connector |
| G | 2-blade Compute Node Power connector for Node 3 |
| H | 2x40 pin Bridge Board connector for Node 3 |
| I | 2x40 pin Bridge Board connector for Node 1 |
| J | 20-pin Front Panel cable connector for Node 1, 3 |
| K | 2-blade Compute Node Power connector for Node 1 |
| L | 2x9 pin Power supply input connector |
| M | 2x9 pin Power supply input connector |
| N | 2x40 pin Bridge Board connector for Node 2 |
| O | 2-blade Compute Node Power connector for Node 2 |

Figure 33. 3.5" Backplane Component and Connectors (Back View)

6.3.4 2.5" Hot Swap Backplane Connector scheme

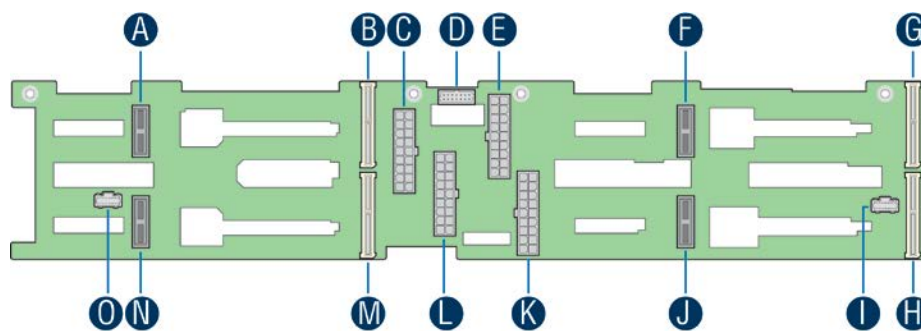
The following diagrams show the layout of major components and connectors for 2.5" Hot Swap backplane.



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| | |
|----------|--------------------------------|
| A | SATA/SAS connectors for Node 1 |
| B | SATA/SAS connectors for Node 2 |
| C | SATA/SAS connectors for Node 3 |
| D | SATA/SAS connectors for Node 4 |

Figure 34. 2.5" Backplane Component and Connectors (Front View)



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| | |
|----------|--|
| A | 2-blade Compute Node Power connector for Node 4 |
| B | 2x40 pin Bridge Board connector for Node 4 |
| C | 2x9 pin Power supply input connector |
| D | 2x7 pin Power Control cable connector |
| E | 2x9 pin Power supply input connector |
| F | 2-blade Compute Node Power connector for Node 3 |
| G | 2x40 pin Bridge Board connector for Node 3 |
| H | 2x40 pin Bridge Board connector for Node 1 |
| I | 20-pin Front Panel cable connector for Node 1, 3 |
| J | 2-blade Compute Node Power connector for Node 1 |
| K | 2x9 pin Power supply input connector |
| L | 2x9 pin Power supply input connector |
| M | 2x40 pin Bridge Board connector for Node 2 |
| N | 2-blade Compute Node Power connector for Node 2 |
| O | 20-pin Front Panel cable connector for Node 2, 4 |

Figure 35. 2.5" Backplane Component and Connectors (Back View)

6.3.5 Backplane LED Support

The backplanes support both HDD online and activity/fault LEDs for each of the hard drive connectors. A light duct in HDD tray is used to conduct LED light to front panel. General HDD LED functionality is displayed below:

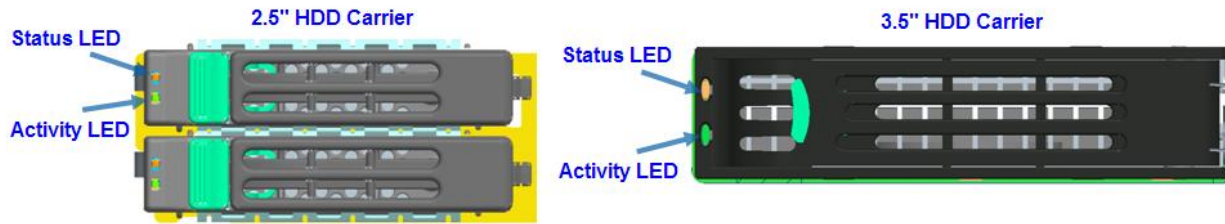


Figure 36. Hard Drive Carrier LED

The following tables list the LED functionality:

Table 49. Hard Drive Carrier Status LED Functions

| | | |
|--------------|----------|---|
| Amber | Off | No access and no fault |
| | Solid On | Hard Drive Fault has occurred |
| | Blink | Raid rebuild in progress (1hz) Identify (2hz) |

Table 50. Hard Drive Carrier Activity LED Functions

| | Condition | Drive Type | Behavior |
|--------------|----------------------------------|------------|--|
| Green | Power on with no drive activity. | SAS | LED stays on |
| | | SATA | LED stays off |
| | Power on with drive activity. | SAS | LED blinks off when processing a command |
| | | SATA | LED blinks off when processing a command |
| | Power on and drive spun down. | SAS | LED stays off |
| | | SATA | LED stays off |
| | Power on and drive spinning up. | SAS | LED blinks |
| | | SATA | LED stays off |

6.3.6 Backplane Connector Definition

The backplanes include several different connectors. This section defines the purpose and pin out associated with each.

1. 2x9 Pin Power Input Connector

The backplane is powered by +12V and +12V_{STB} from PDB of CRPS. The input power is distributed by backplane to all four nodes.

Table 51. Backplane Input Power Connector Pin-out

| Pin | Signal Description | Pin | Signal Description |
|-----|--------------------|-----|--------------------|
| 2 | P12V | 1 | GND |
| 4 | P12V | 3 | GND |
| 6 | P12V | 5 | GND |
| 8 | P12V | 7 | GND |
| 10 | P12V | 9 | GND |
| 12 | P12V | 11 | GND |
| 14 | P12V | 13 | GND |
| 16 | P12V | 15 | GND |
| 18 | P12V | 17 | GND |

2. 2-Blade Compute Node Power Connector

The backplane provides main power to compute node through 2-blade power connector.

Table 52. 2-blade Compute Node Power Connector Pin-out

| Pin | Signal Description | Pin | Signal Description |
|-------------------------|--------------------|-----|--------------------|
| Lower Blade (Circuit 1) | | | |
| 1 | GND | 2 | GND |
| 3 | GND | 4 | GND |
| 5 | GND | 6 | GND |
| 7 | GND | 8 | GND |
| Upper Blade (Circuit 2) | | | |
| 9 | P12V | 10 | P12V |
| 11 | P12V | 12 | P12V |
| 13 | P12V | 14 | P12V |
| 15 | P12V | 16 | P12V |

3. 2x40 Pin Bridge Board Connector

The Compute Node provides four SATA/SAS ports (in SCU0) to backplane, together with front panel control signals and SMBus*.

Table 53. 2x40 Pin Connector Pin-out for Node Bridge Board

| Pin | Signal Description | Pin | Signal Description |
|-----|----------------------|-----|--------------------|
| 1 | 5V_AUX | 2 | 5V_AUX |
| 3 | SATA0_TXN | 4 | USB2_OC |
| 5 | SATA0_TXP | 6 | GND |
| 7 | GND | 8 | SATA0_RXN |
| 9 | NODE_Present_N (GND) | 10 | SATA0_RXP |
| 11 | ALL_NODE_OFF | 12 | GND |
| 13 | spare | 14 | USB2_P0P |
| 15 | GND | 16 | USB2_P0N |
| 17 | IPMB-Data | 18 | GND |
| 19 | IPMB-Clk | 20 | FP HDD_ACT_LED_N |
| 21 | GND | 22 | FP Activity LED_N |

| Pin | Signal Description | Pin | Signal Description |
|-----|--------------------|-----|--------------------|
| 23 | SMBUS_R1 DATA | 24 | FP Health LEDA_N |
| 25 | SMBUS_R1 CLK | 26 | FP Health LEDG_N |
| 27 | GND | 28 | FP PWR LED_N |
| 29 | SMBUS_R5 DATA | 30 | FP ID LED_N |
| 31 | SMBUS_R5 CLK | 32 | FP ID BTN_N |
| 33 | GND | 34 | FP RST BTN_N |
| 35 | SMBUS_R7 DATA | 36 | FP PWR BTN_N |
| 37 | SMBUS_R7 CLK | 38 | FP NMI BTN_N |
| 39 | GND | 40 | SPA_SOUT_N |
| 41 | PMBUS Alert_N | 42 | SPA_SIN_N |
| 43 | NODEx_ON_N | 44 | ID3 |
| 45 | SGPIO DATA IN | 46 | ID2 |
| 47 | SGPIO Data Out | 48 | ID1 |
| 49 | SGPIO LD | 50 | ID0 |
| 51 | SPKR | 52 | SGPIO CLK |
| 53 | GND | 54 | GND |
| 55 | SAS3_RX | 56 | SAS3_TX |
| 57 | SAS3_RX | 58 | SAS3_TX |
| 59 | GND | 60 | GND |
| 61 | SAS2_TX | 62 | SAS2_RX |
| 63 | SAS2_TX | 64 | SAS2_RX |
| 65 | GND | 66 | GND |
| 67 | SAS1_RX | 68 | SAS1_TX |
| 69 | SAS1_RX | 70 | SAS1_TX |
| 71 | GND | 72 | GND |
| 73 | SAS0_TX | 74 | SAS0_RX |
| 75 | SAS0_TX | 76 | SAS0_RX |
| 77 | GND | 78 | GND |
| 79 | 3.3V | 80 | 3.3V |

4. 20-Pin Front Panel Connector

The backplanes provide connectors for front panel control signals. Each connector integrates the control signals of two compute nodes.

Table 54. Front Panel Connector Pin-out

| Pin | Signal Description |
|-----|--------------------|
| 1 | GND |
| 2 | FP1_PWR_BTN_N |
| 3 | FP1_RST_BTN_N |
| 4 | FP1_ID_BTN_N |
| 5 | P5VSB |
| 6 | FP1_PWR_LED_N |
| 7 | FP1_HEALTH_LEDG_N |
| 8 | FP1_HEALTH_LEDA_N |
| 9 | FP1_ACTIVITY_LED_N |
| 10 | FP1_ID_LED_N |
| 11 | GND |

| Pin | Signal Description |
|-----|--------------------|
| 12 | FP2_PWR_BTN_N |
| 13 | FP2_RST_BTN_N |
| 14 | FP2_ID_BTN_N |
| 15 | P3V3SB |
| 16 | FP2_PWR_LED_N |
| 17 | FP2_HEALTH_LEDG_N |
| 18 | FP2_HEALTH_LED_A_N |
| 19 | FP2_ACTIVITY_LED_N |
| 20 | FP2_ID_LED_N |

5. 2x7 Pin Power Supply Control Signal Connector

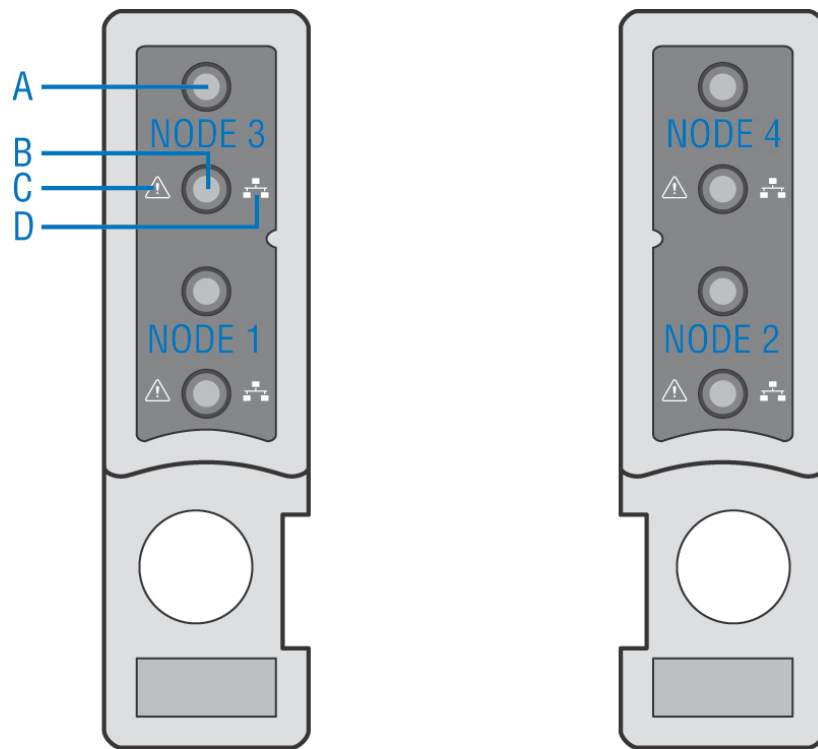
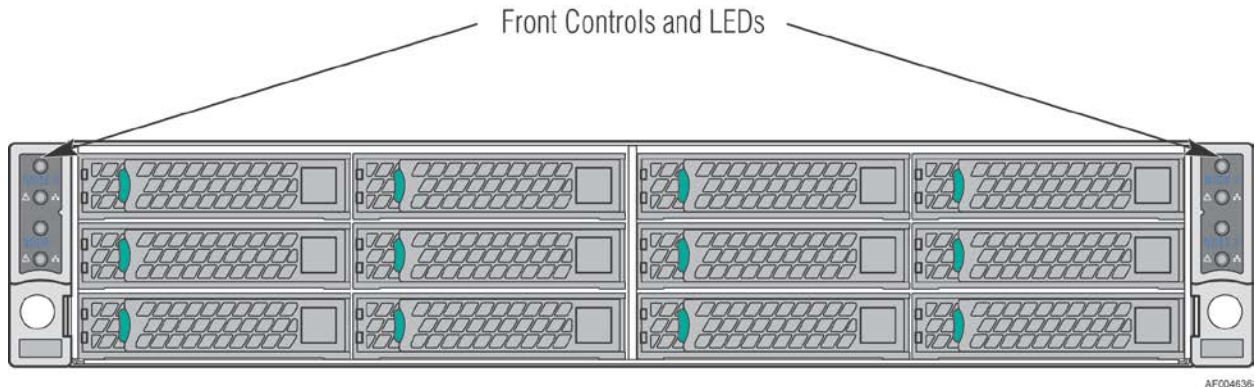
The backplanes provide power supply control signals, together with PMBus* functionality integrated.

Table 55. Power Supply Control Connector Pin-out

| Pin | Signal Description | Pin | Signal Description |
|-----|--------------------|-----|--------------------|
| 1 | SMBUS_R7_DATA | 2 | A0 |
| 3 | SMBUS_R7_CLK | 4 | PSON_N |
| 5 | PMBUS_ALERT_N | 6 | 12V RS_RTN |
| 7 | PWROK | 8 | 12V RS |
| 9 | Reserved | 10 | PDU1-12VSB |
| 11 | PDU1-12VSB | 12 | PDU2-12VSB |
| 13 | PDU2-12VSB | 14 | Reserved |

7. Front Panel Control and Indicators

The Intel® Server System H2000WP family Front Control Panel is integrated with rack handles at the both sides of the chassis. Each control panel contains two sets of node control buttons and status LEDs. The control panel assembly is pre-assembled and fixed with the rack handles.



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| | |
|----------|------------------------------|
| A | System Power Button with LED |
| B | System ID LED Button |
| C | System Status LED |
| D | Network Link/Activity LED |

Figure 37. Front Control Panel

7.1 Control Panel Button

The following table lists the control panel features and functions. The control panels features a system power button.

Table 56. Front Control Button Function

| Feature | Function |
|------------------------------|---|
| Power Button with Power LED | Toggles the system power on/off. This button also integrates the power LED. |
| System ID Button with ID LED | Toggles between ID LED on and off. |

7.2 Control Panel LED Indicators

The control panel houses independent two LEDs and two button integrated LEDs for each node, which are viewable to display the system's operating status. The following table identifies each LED and describes their functionality.

Table 57. Front LED Indicator Functions

| LED Indicator | Color | Condition | What it describes |
|---------------------|-------|-----------|--|
| Power | Green | On | Power On/ACPI S0 state |
| | Green | Blink | Sleep /ACPI S1 state |
| | - | Off | Power Off /ACPI S5 state |
| LAN (i350 Dual NIC) | Green | On | LAN Link no Access |
| | Green | Blink | LAN Activity |
| | - | Off | No Link |
| System Status | Green | On | System Ready/No Alarm |
| | Green | Blink | System ready, but degraded: redundancy lost such as the power supply or fan failure; non-critical temp/voltage threshold; battery failure; or predictive power supply failure. |
| | Amber | On | Critical Alarm: Critical power modules failure, critical fans failure, voltage (power supply), critical temperature, and voltage |
| | Amber | Blink | Non-Critical Alarm: Redundant fan failure, redundant power module failure, non-critical temperature, and voltage |
| | - | Off | Power off: System unplugged Power on: System powered off and in standby, no prior degraded\non-critical\critical state |

Notes:

1. Blink rate is ~1 Hz at 50% duty cycle.
2. It is also off when the system is powered off (S5) or in a sleep state (S1).
3. The power LED sleep indication is maintained on standby by the chipset. If the system is powered down without going through the BIOS, the LED state in effect at the time of power off is restored when the system is powered on until the BIOS clear it.
4. If the system is not powered down normally, it is possible the Power LED will blink at the same time the system status LED is off due to a failure or configuration change that prevents the BIOS from running.

7.2.1 Power/Sleep LED

Table 58. Power LED Operation

| State | Power Mode | LED | Description |
|-----------|------------|----------|--|
| Power Off | Non-ACPI | Off | System power is off and the BIOS has not initialized the chipset. |
| Power On | Non-ACPI | Solid On | System power is on but the BIOS has not yet initialized the chipset. |
| S5 | ACPI | Off | Mechanical is off and the operating system has not saved any context to the hard disk. |
| S1 Sleep | ACPI | Blink | DC power is still on. The operating system has saved context and gone into a level of low-power state. |
| S0 | ACPI | Solid On | System and the operating system are up and running. |

Note: Blink rate is ~ 1Hz at 50% duty cycle.

7.2.2 System Status LED

Table 59. System Status LED Operation

| Color | State | Criticality | Description |
|-----------------|------------------|--------------|---|
| Off | N/A | Not ready | Power off or BMC initialization completes if no degraded, non-critical, critical, or non-recoverable conditions exist after power cable plug in. |
| Green/ Amber | Both Solid On | Not ready | Pre DC Power On – 15-20 second BMC Initialization when AC is applied to the server. The system will not POST until BMC initialization completes. |
| Green | Solid on | Ok | System ready. |
| Green | Blink | Degraded | <p>BIOS detected.</p> <ol style="list-style-type: none"> Unable to use all of the installed memory (more than one DIMM installed).¹ In a mirrored configuration, when memory mirroring takes place and system loses memory redundancy. This is not covered by (2).¹ PCI Express* correctable link errors. <p>Integrated BMC detected.</p> <ol style="list-style-type: none"> One of redundant power supplies not present. CPU disabled – if there are two CPUs and one CPU is disabled. Fan alarm – Fan failure. Number of operational fans should be more than minimum number needed to cool the system. Non-critical threshold crossed – Temperature, voltage, power nozzle, power gauge, and PROCHOT2 (Therm Ctrl) sensors. Battery failure. Predictive failure when the system has redundant power supplies. |
| Amber | Blink | Non-critical | <p>Non-fatal alarm – system is likely to fail.</p> <p>BIOS Detected</p> <ol style="list-style-type: none"> In non-mirroring mode, if the threshold of ten correctable errors is crossed within the window.¹ PCI Express* uncorrectable link errors. <p>Integrated BMC Detected</p> <ol style="list-style-type: none"> Critical threshold crossed – Voltage, temperature, power nozzle, power gauge, and PROCHOT (Therm Ctrl) sensors. VRD Hot asserted. One of the redundant power supplies failed. |

| Color | State | Criticality | Description |
|-------|----------|---------------------------|---|
| | | | 4. Minimum number of fans to cool the system are not present or have failed. |
| Amber | Solid on | Critical, non-recoverable | <p>Fatal alarm – system has failed or shutdown.</p> <p>BIOS Detected</p> <ol style="list-style-type: none"> DIMM failure when there is one DIMM present and no good memory is present.¹ Run-time memory uncorrectable error in non-redundant mode.¹ CPU configuration error (for instance, processor stepping mismatch). <p>Integrated BMC Detected</p> <ol style="list-style-type: none"> CPU CATERR signal asserted. CPU 1 is missing. CPU THERMTRIP. System cooling fan failure. No power good – redundant power fault. <ul style="list-style-type: none"> Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies are present). |

Notes:

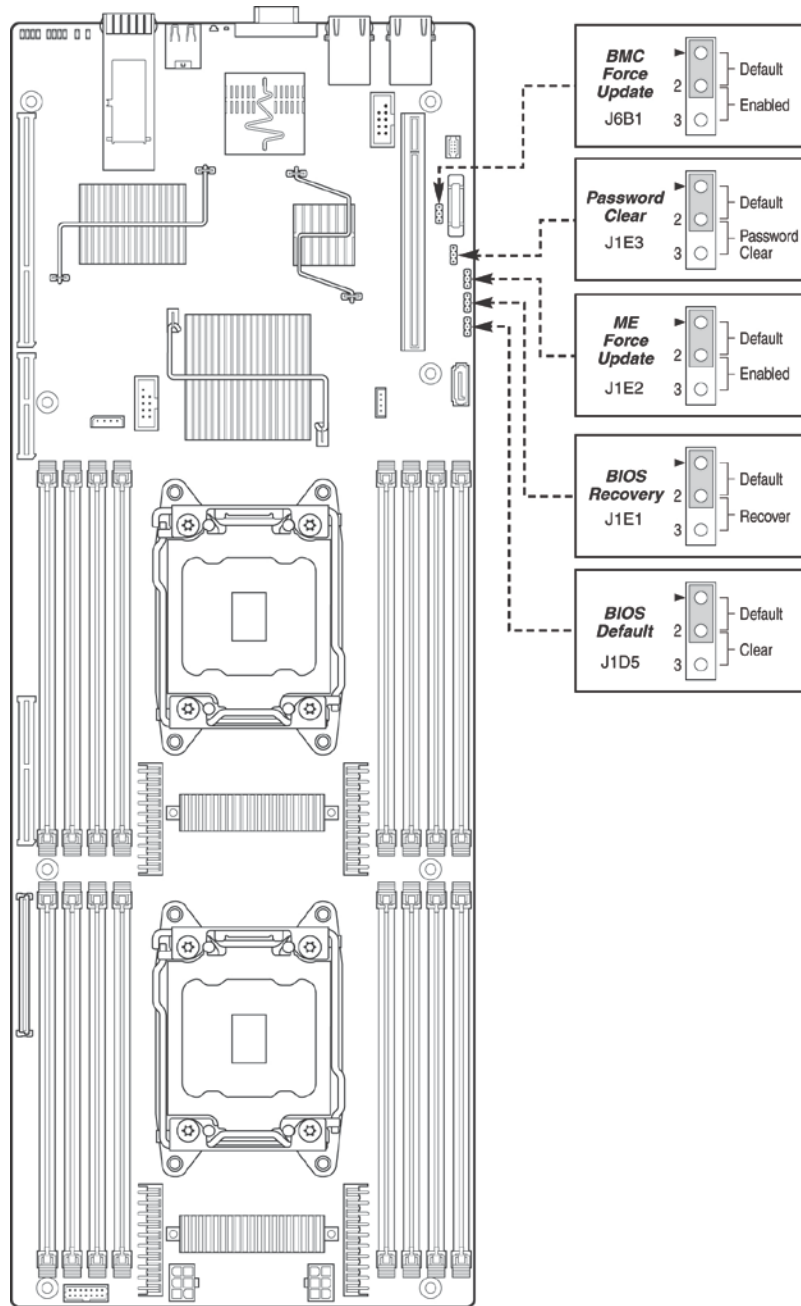
- The BIOS detects these conditions and sends a *Set Fault Indication* command to the Integrated BMC to provide the contribution to the system status LED.
- Blink rate is ~ 1Hz at 50% duty cycle.

7.2.3 System Status LED – BMC Initialization

When power is first applied to the system and 5V-STBY is present, the BMC controller on the server board requires 15-20 seconds to initialize. During this time, the system status LED will be solid on, both amber and green. Once BMC initialization has completed, the status LED will stay green solid on. If power button is pressed before BMC initialization completes, the system will not boot to POST.

8. Configuration Jumpers

The following table provides a summary and description of configuration, test, and debug jumpers on the Intel® Server Board S2600WP, which is used in Intel® Server System H2000WP Family as Compute Node.



AF004672

Figure 38. Jumper Locations and Functions

Table 60. Force Integrated BMC Update Jumper

| Jumper Name | Jumper Position | Mode of Operation | Note |
|-------------------------------|-----------------|---------------------|--|
| J6B1: BMC Force Update jumper | 1-2 | Normal | Normal mode |
| | 2-3 | Update | BMC in force update mode |
| J1E2: ME Force Update | 1-2 | Normal | Normal mode |
| | 2-3 | Update | ME in force update mode |
| J1E3: Password Clear | 1-2 | Normal | Normal mode, password in protection |
| | 2-3 | Clear Password | BIOS password is cleared |
| J1E1: BIOS Recovery Mode | 1-2 | Normal | Normal mode |
| | 2-3 | Recovery | BIOS in recovery mode |
| J1D5: BIOS Default | 1-2 | Normal | Normal mode |
| | 2-3 | Clear BIOS Settings | BIOS settings are reset to factory default |

8.1 Force Integrated BMC Update (J6B1)

When performing a standard BMC firmware update procedure, the update utility places the BMC into an update mode, allowing the firmware to load safely onto the flash device. In the unlikely event the BMC firmware update process fails due to the BMC not being in the proper update state, the server board provides a BMC Force Update jumper (J6B1) which will force the BMC into the proper update state. The following procedure should be followed in the event the standard BMC firmware update process fails.

Table 61. Force Integrated BMC Update Jumper

| Jumper Position | Mode of Operation | Note |
|-----------------|-------------------|--------------------------|
| 1-2 | Normal | Normal Operation |
| 2-3 | Update | BMC in force update mode |

Steps to perform the Force Integrated BMC Update:

1. Power down and remove the AC power cord.
2. Open the server chassis. See your server chassis documentation for instructions.
3. Move jumper from the default operating position, covering pins 1 and 2, to the enabled position, covering pins 2 and 3.
4. Close the server chassis.
5. Reconnect the AC cord and power up the server.
6. Perform the BMC firmware update procedure as documented in the *ReleaseNote.TXT* file included in the given BMC firmware update package. After successful completion of the firmware update process, the firmware update utility may generate an error stating the BMC is still in update mode.
7. Power down and remove the AC power cord.
8. Open the server chassis.
9. Move the jumper from the enabled position, covering pins 2 and 3 to the disabled position, covering pins 1 and 2.
10. Close the server chassis.
11. Reconnect the AC cord and power up the server.

Note: Normal BMC functionality is disabled with the Force BMC Update jumper is set to the enabled position. You should never run the server with the BMC Force Update jumper set in this

position. You should only use this jumper setting when the standard firmware update process fails. This jumper should remain in the default/disabled position when the server is running normally.

The server board has several 3-pin jumper blocks that can be used to configure, protect, or recover specific features of the server board.

8.2 Force ME Update (J1E2)

When this three-pin jumper is set, it manually puts the ME firmware in update mode, which enables the user to update ME firmware code when necessary.

Table 62. Force ME Update Jumper

| Jumper Position | Mode of Operation | Note |
|-----------------|-------------------|-------------------------|
| 1-2 | Normal | Normal operation |
| 2-3 | Update | ME in force update mode |

Note: Normal ME functionality is disabled with the Force ME Update jumper is set to the enabled position. You should never run the server with the ME Force Update jumper set in this position. You should only use this jumper setting when the standard firmware update process fails. This jumper should remain in the default/disabled position when the server is running normally.

Steps to perform the Force ME Update:

1. Power down and remove the AC power cord.
2. Open the server chassis. For instructions, see your server chassis documentation.
3. Move jumper from the default operating position (covering pins 1 and 2) to the enabled position (covering pins 2 and 3).
4. Close the server chassis.
5. Reconnect the AC cord and power up the server.
6. Perform the ME firmware update procedure as documented in the *README.TXT* file that is included in the given ME firmware update package (same package as BIOS).
7. Power down and remove the AC power cord.
8. Open the server chassis.
9. Move jumper from the enabled position (covering pins 2 and 3) to the disabled position (covering pins 1 and 2).
10. Close the server chassis.

8.3 Password Clear (J1E3)

This three-pin jumper is used to clear the BIOS password.

Table 63. BIOS Password Clear Jumper

| Jumper Position | Mode of Operation | Note |
|-----------------|-------------------|-------------------------------------|
| 1-2 | Normal | Normal mode. Password in protection |
| 2-3 | Clear Password | BIOS password is cleared |

Steps to perform the password clear:

1. Power down server. Do not unplug the power cord.
2. Open the chassis. For instructions, refer to your server chassis documentation.
3. Move the jumper (J1F2) from the default operating position, covering pins 1 and 2, to the password clear position, covering pins 2 and 3.
4. Close the server chassis.
5. Power up the server, wait 10 seconds or until POST completes.
6. Power down the server.
7. Open the chassis and move the jumper back to default position, covering pins 1 and 2.
8. Close the server chassis.
9. Power up the server. The password is now cleared and you can reset it by going into the BIOS setup. The BIOS password is now cleared.

8.4 BIOS Recovery Mode (J1E1)

The Intel® Server Board S2600WP uses BIOS recovery to repair the system BIOS from flash corruption in the main BIOS and Boot Block. This 3-pin jumper is used to reload the BIOS when the image is suspected to be corrupted. For directions on how to recover the BIOS, refer to the specific *BIOS release notes*.

Table 64. BIOS Recovery Mode Jumper

| Jumper Position | Mode of Operation | Note |
|-----------------|-------------------|-----------------------|
| 1-2 | Normal | Normal mode |
| 2-3 | Recovery | BIOS in recovery mode |

You can accomplish a BIOS recovery from the SATA CD and USB Mass Storage device. Please note that this platform does not support recovery from a USB floppy.

The recovery media must contain the following files under the root directory:

1. RML.ROM
2. UEFI iFlash32 11.0 Build 2 (including iFlash32.efi and ipmi.efi)
3. *Rec.CAP
4. Startup.nsh (update accordingly to use proper *Rec.CAP file)

The BIOS starts the recovery process by first loading and booting to the recovery image file (RML.ROM) on the root directory of the recovery media (USB disk). This process takes place before any video or console is available. Once the system boots to this recovery image file (FVMAIN.FV), it boots automatically into the EFI Shell to invoke the Startup.nsh script and start the flash update application (iFlash32.efi). iFlash32.efi requires the supporting BIOS Capsule image file (*Rec.CAP).

After the update is complete, a message displays stating, "BIOS has been updated successfully". This indicates the recovery process is finished.

The user should then switch the recovery jumper back to normal operation and restart the system by performing a power cycle.

The following steps demonstrate this recovery process:

1. Power OFF the system.
2. Insert recovery media.
3. Switch the recovery jumper. Details regarding the jumper ID and location can be obtained from the board EPS for that platform.
4. Power ON the system.
5. The BIOS POST screen will appear displaying the progress, and the system automatically boots to the EFI SHELL.
6. The Startup.nsh file executes, and initiates the flash update (IFlash32.efi) with a new capsule file (*Rec.CAP). The regular iFlash message displays at the end of the process—once the flash update succeeds.
7. Power OFF the system, and revert the recovery jumper position to "normal operation".
8. Power ON the system.
9. Do NOT interrupt the BIOS POST during the first boot.

8.5 Reset BIOS Settings (J1D5)

This jumper used to be the CMOS Clear jumper. The BIOS has moved CMOS data to the NVRAM region of the BIOS flash since the previous generation. The BIOS checks during boot to determine if the data in the NVRAM must be set to default.

Table 65. Reset BIOS Jumper

| Jumper Position | Mode of Operation | Note |
|-----------------|--------------------------|--|
| 1-2 | Normal | These pins should have a jumper in place for normal system operation. (Default) |
| 2-3 | Reset BIOS Configuration | If these pins 2-3 are connected with AC power plugged, the CMOS settings are cleared within five seconds. These pins should not be connected for normal operation. |

Steps to reset the BIOS settings to default:

1. Power down server. Do not unplug the power cord.
2. Open the server chassis. For instructions, see your server chassis documentation.
3. Move jumper (J1D5) from the default operating position, covering pins 1 and 2, to the reset/clear position, covering pins 2 and 3.
4. Wait five seconds.
5. Remove AC power.
6. Move the jumper back to default position, covering pins 1 and 2.
7. Close the server chassis.
8. Power up the server.

The BIOS settings are now cleared and you can reset it by going into the BIOS setup.

Note: Removing AC Power before performing the BIOS settings Clear operation causes the system to automatically power up and immediately power down, after the procedure is followed and AC power is re-applied. If this happens, remove the AC power cord again, wait 30 seconds, and re-install the AC power cord. Power-up the system and proceed to the <F2> BIOS Setup Utility to reset the desired settings.

9. PCI Express* Riser Card and Assembly

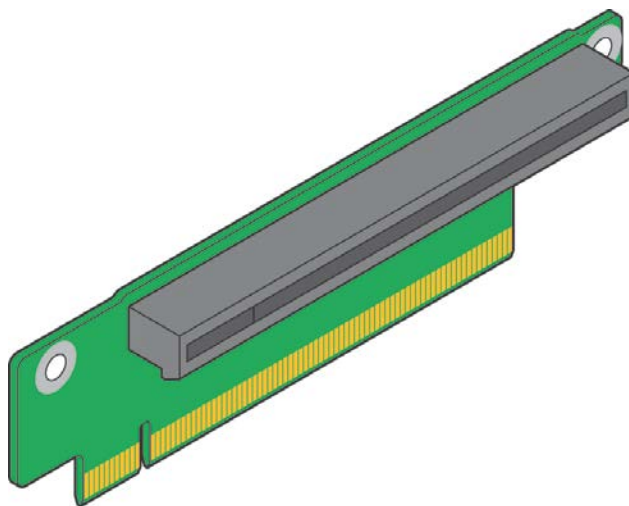
Each compute node in Intel® Server System H2000WP Family includes four PCI Express* riser slots that accept dedicated PCI Express* x16 Gen3 Risers to support low profile add-in card and Intel® IO module. Only Riser Slot 1 and Riser Slot 2 are available for risers. Riser Slot 3 and 4 are hidden by bridge board. The PCI Express* slot on riser also accommodates PCI Express* x8, x4, and x1 adapters.

9.1 PCI Express* Riser for Slot 1

9.1.1 Overview of PCI-Express Riser

Riser slot 1 on baseboard provides standard PCI Express* x16 Gen3 signals, together with specific power pins to support high-power Graphic/GPGPU add-in card.

Note: Riser Slot 1 on baseboard only supports Intel® 1U/2U Risers. It will cause damage to any PCI-E based add-in card, which is directly plugged into the Riser Slot 1 on baseboard.



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Figure 39. PCI Express* Riser for Riser Slot 1

9.1.2 Pinout definition on Slot 1 Riser

The following lists the pin definition on Slot 1 Riser.

Table 66. Riser Card Edge Pinout

| Pin | Pin Name | Description | Pin | Pin Name | Description |
|-----|----------|-----------------------------|-----|----------|-----------------------------|
| B1 | 12V | 20W 3.3V generated on riser | A1 | 12V | 20W 3.3V generated on riser |
| B2 | 12V | 66W for GPU | A2 | 12V | 66W for GPU |
| B3 | 12V | 66W for GPU | A3 | 12V | 66W for GPU |
| B4 | 12V | 66W for GPU | A4 | SMDATA | |
| B5 | SMCLK | | A5 | 3.3VAUX | For wake on LAN |

| Pin | Pin Name | Description | Pin | Pin Name | Description |
|------------|--------------|-----------------|-----|-------------|--------------------------|
| B6 | 3.3VAUX | For wake on LAN | A6 | GPU_NODE_ON | can turn of 2U GPU power |
| B7 | GND | | A7 | GPU_PWRGD | |
| B8 | Tach9 | | A8 | Tach11 | |
| B9 | Tach8 | | A9 | Tach10 | |
| B10 | Tach7 | | A10 | Tach6 | |
| B11 | Spare | | A11 | Spare | |
| KEY | | | | | |
| B12 | Spare | | A12 | PWM2 | GPU Fan speed control |
| B13 | Spare | | A13 | GND | |
| B14 | GND | | A14 | PERST# | |
| B15 | SMBUS_R4 CLK | | A15 | WAKE# | |
| B16 | SMBUS_R4 DAT | | A16 | GND | |
| B17 | GND | | A17 | REFCLK+ | Clock pair 1 |
| B18 | PETxP0 | Tx Lane 0+ | A18 | REFCLK- | Clock pair 1 |
| B19 | PETxN0 | Tx Lane 0- | A19 | GND | |
| B20 | GND | | A20 | PERxP0 | Rx Lane 0+ |
| B21 | GND | | A21 | PERxN0 | Rx Lane 0- |
| B22 | PETxP1 | Tx Lane 1+ | A22 | GND | |
| B23 | PETxN1 | Tx Lane 1- | A23 | GND | |
| B24 | GND | | A24 | PERxP1 | Rx Lane 1+ |
| B25 | GND | | A25 | PERxN1 | Rx Lane 1- |
| B26 | PETxP2 | Tx Lane 2+ | A26 | GND | |
| B27 | PETxN2 | Tx Lane 2- | A27 | GND | |
| B28 | GND | | A28 | PERxP2 | Rx Lane 2+ |
| B29 | GND | | A29 | PERxN2 | Rx Lane 2- |
| B30 | PETxP3 | Tx Lane 3+ | A30 | GND | |
| B31 | PETxN3 | Tx Lane 3- | A31 | GND | |
| B32 | GND | | A32 | PERxP3 | Rx Lane 3+ |
| B33 | GND | | A33 | PERxN3 | Rx Lane 3- |
| B34 | PETxP4 | Tx Lane 4+ | A34 | GND | |
| B35 | PETxN4 | Tx Lane 4- | A35 | GND | |
| B36 | GND | | A36 | PERxP4 | Rx Lane 4+ |
| B37 | GND | | A37 | PERxN4 | Rx Lane 4- |
| B38 | PETxP5 | Tx Lane 5+ | A38 | GND | |
| B39 | PETxN5 | Tx Lane 5- | A39 | GND | |
| B40 | GND | | A40 | PERxP5 | Rx Lane 5+ |
| B41 | GND | | A41 | PERxN5 | Rx Lane 5- |
| B42 | PETxP6 | Tx Lane 6+ | A42 | GND | |
| B43 | PETxN6 | Tx Lane 6- | A43 | GND | |
| B44 | GND | | A44 | PERxP6 | Rx Lane 6+ |
| B45 | GND | | A45 | PERxN6 | Rx Lane 6- |
| B46 | PETxP7 | Tx Lane 7+ | A46 | GND | |
| B47 | PETxN7 | Tx Lane 7- | A47 | GND | |

| Pin | Pin Name | Description | Pin | Pin Name | Description |
|-----|----------|--------------|-----|----------|-----------------------|
| B48 | GND | | A48 | PERxP7 | Rx Lane 7+ |
| B49 | GND | | A49 | PERxN7 | Rx Lane 7- |
| B50 | PETxP8 | Tx Lane 8+ | A50 | GND | |
| B51 | PETxN8 | Tx Lane 8- | A51 | GND | |
| B52 | GND | | A52 | PERxP8 | Rx Lane 8+ |
| B53 | GND | | A53 | PERxN8 | Rx Lane 8- |
| B54 | PETxP9 | Tx Lane 9+ | A54 | GND | |
| B55 | PETxN9 | Tx Lane 9- | A55 | GND | |
| B56 | GND | | A56 | PERxP9 | Rx Lane 9+ |
| B57 | GND | | A57 | PERxN9 | Rx Lane 9- |
| B58 | PETxP10 | Tx Lane 10+ | A58 | GND | |
| B59 | PETxN10 | Tx Lane 10- | A59 | GND | |
| B60 | GND | | A60 | PERxP10 | Rx Lane 10+ |
| B61 | GND | | A61 | PERxN10 | Rx Lane 10- |
| B62 | PETxP11 | Tx Lane 11+ | A62 | GND | |
| B63 | PETxN11 | Tx Lane 11- | A63 | GND | |
| B64 | GND | | A64 | PERxP11 | Rx Lane 11+ |
| B65 | GND | | A65 | PERxN11 | Rx Lane 11- |
| B66 | PETxP12 | Tx Lane 12+ | A66 | GND | |
| B67 | PETxN12 | Tx Lane 12- | A67 | GND | |
| B68 | GND | | A68 | PERxP12 | Rx Lane 12+ |
| B69 | GND | | A69 | PERxN12 | Rx Lane 12- |
| B70 | PETxP13 | Tx Lane 13+ | A70 | GND | |
| B71 | PETxN13 | Tx Lane 13- | A71 | GND | |
| B72 | GND | | A72 | PERxP13 | Rx Lane 13+ |
| B73 | GND | | A73 | PERxN13 | Rx Lane 13- |
| B74 | PETxP14 | Tx Lane 14+ | A74 | GND | |
| B75 | PETxN14 | Tx Lane 14- | A75 | GND | |
| B76 | GND | | A76 | PERxP14 | Rx Lane 14+ |
| B77 | REFCLK+ | Clock pair 2 | A77 | PERxN14 | Rx Lane 14- |
| B78 | REFCLK- | Clock pair 2 | A78 | GND | |
| B79 | GND | | A79 | PERxP15 | Rx Lane 15+ |
| B80 | PETxP15 | Tx Lane 15+ | A80 | PERxN15 | Rx Lane 15- |
| B81 | PETxN15 | Tx Lane 15- | A81 | GND | |
| B82 | GND | | A82 | Riser ID | Fix to High: PCIe x16 |

There is a standard PCI Express* Gen 3x16 slot on riser card for PCIe based add-in card. The pin definitions for the slot are as follows:

Table 67. PCI Express* Slot Pinout on Riser Card

| Pin-Side B | PCI Spec Signal | Pin-Side A | PCI Spec Signal |
|------------|-----------------|------------|-----------------|
| 82 | RSVD | 82 | GND |
| 81 | PRSNT2# | 81 | HSIN15 |
| 80 | GND | 80 | HSIP15 |

| Pin-Side B | PCI Spec Signal | Pin-Side A | PCI Spec Signal |
|------------|-----------------|------------|-----------------|
| 79 | HSO15 | 79 | GND |
| 78 | HSOP15 | 78 | GND |
| 77 | GND | 77 | HSIN14 |
| 76 | GND | 76 | HSIP14 |
| 75 | HSO14 | 75 | GND |
| 74 | HSOP14 | 74 | GND |
| 73 | GND | 73 | HSIN13 |
| 72 | GND | 72 | HSIP13 |
| 71 | HSO13 | 71 | GND |
| 70 | HSOP13 | 70 | GND |
| 69 | GND | 69 | HSIN12 |
| 68 | GND | 68 | HSIP12 |
| 67 | HSO12 | 67 | GND |
| 66 | HSOP12 | 66 | GND |
| 65 | GND | 65 | HSIN11 |
| 64 | GND | 64 | HSIP11 |
| 63 | HSO11 | 63 | GND |
| 62 | HSOP11 | 62 | GND |
| 61 | GND | 61 | HSIN10 |
| 60 | GND | 60 | HSIP10 |
| 59 | HSO10 | 59 | GND |
| 58 | HSOP10 | 58 | GND |
| 57 | GND | 57 | HSIN9 |
| 56 | GND | 56 | HSIP9 |
| 55 | HSO9 | 55 | GND |
| 54 | HSOP9 | 54 | GND |
| 53 | GND | 53 | HSIN8 |
| 52 | GND | 52 | HSIP8 |
| 51 | HSO8 | 51 | GND |
| 50 | HSOP8 | 50 | RSVD |
| 49 | GND | 49 | GND |
| 48 | PRSNT2# | 48 | HSIN7 |
| 47 | GND | 47 | HSIP7 |
| 46 | HSO7 | 46 | GND |
| 45 | HSOP7 | 45 | GND |
| 44 | GND | 44 | HSIN6 |
| 43 | GND | 43 | HSIP6 |
| 42 | HSO6 | 42 | GND |
| 41 | HSOP6 | 41 | GND |
| 40 | GND | 40 | HSIN5 |
| 39 | GND | 39 | HSIP5 |
| 38 | HSO5 | 38 | GND |
| 37 | HSOP5 | 37 | GND |
| 36 | GND | 36 | HSIN4 |
| 35 | GND | 35 | HSIP4 |
| 34 | HSO4 | 34 | GND |

| Pin-Side B | PCI Spec Signal | Pin-Side A | PCI Spec Signal |
|------------|-----------------|------------|-----------------|
| 33 | HSOP4 | 33 | RSVD |
| 32 | GND | 32 | RSVD |
| 31 | PRSNT2# | 31 | GND |
| 30 | RSVD | 30 | HSIN3 |
| 29 | GND | 29 | HSIP3 |
| 28 | HSO3 | 28 | GND |
| 27 | HSOP3 | 27 | GND |
| 26 | GND | 26 | HSIN2 |
| 25 | GND | 25 | HSIP2 |
| 24 | HSO2 | 24 | GND |
| 23 | HSOP2 | 23 | GND |
| 22 | GND | 22 | HSIN1 |
| 21 | GND | 21 | HSIP1 |
| 20 | HSO1 | 20 | GND |
| 19 | HSOP1 | 19 | RSVD |
| 18 | GND | 18 | GND |
| 17 | PRSNT2# | 17 | HSIN0 |
| 16 | GND | 16 | HSIP0 |
| 15 | HSO0 | 15 | GND |
| 14 | HSOP0 | 14 | REFCLK- |
| 13 | GND | 13 | REFCLK+ |
| 12 | RSVD | 12 | GND |
| KEY | | KEY | |
| KEY | | KEY | |
| 11 | WAKE# | 11 | PWRGD |
| 10 | 3.3V AUX | 10 | 3.3V |
| 9 | JTAG1 | 9 | 3.3V |
| 8 | 3.3V | 8 | JTAG5 |
| 7 | GND | 7 | JTAG4 |
| 6 | SMDAT | 6 | JTAG3 |
| 5 | SMCLK | 5 | JTAG2 |
| 4 | GND | 4 | GND |
| 3 | RSVD | 3 | 12V |
| 2 | 12V | 2 | 12V |
| 1 | 12V | 1 | PRSNT1# |

9.2 PCI Express* Riser with IOM Carrier for Slot 2 (Optional)

9.2.1 Overview of PCI-E Riser with IOM Carrier

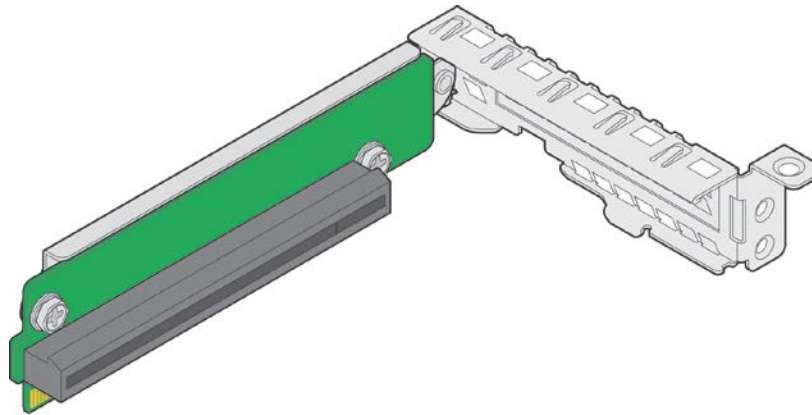
The Riser with IOM carrier is provided as accessory to the server system. It is combined with the following functions:

- Provide PCI Express* x8 Gen 3 signals from riser.
- Integrated 1GbE management port for Intel® Remote Management Module 4.
- Support PCI-E x4 based Intel® IO Module.

Riser slot 2 on baseboard provides standard PCI Express* x16 Gen3 signals, together with specific power pins to support high-power Graphic/GPGPU add-in card.

Note: Riser Slot 2 on baseboard only supports Intel® 1U/2U Risers. It will cause damage to any PCI-E based add-in card, which is directly plugged into the Riser Slot 2.

The PCI-E slot on Riser is x16 mechanically with x8 electrically. The IOM carrier is using PCI-E x8 card edge with PCI-E x4 IO module slot.



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Figure 40. PCI Express* Riser with bracket for Riser Slot 2

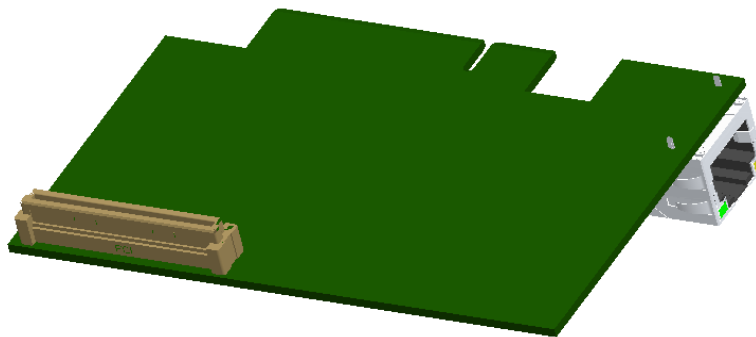


Figure 41. IOM Carrier

The 1GbE port is dedicated NIC port for RMM4 Lite module. It only works once the RMM4 Lite module is installed in the system. The LED of dedicated NIC port is following the below definition:

Table 68. Dedicated NIC Port LED Functionality

| LED | Color | Condition | Functionality |
|---------------------|-------|-----------|---------------|
| Dedicated NIC Speed | Green | On | 1Gbps mode |
| | Amber | On | 100Mbps mode |
| | | Off | 10Mbps mode |

| LED | Color | Condition | Functionality |
|------------------------|-------|-----------|------------------------|
| Dedicated NIC Activity | Green | On | LAN link and no access |
| | Green | Blink | LAN access |
| | | Off | Idle |

9.2.2 Pinout definition on Slot 2 Riser and IOM Carrier

Below is a list of pin definition for Slot 2 Riser and IOM Carrier.

Table 69. Riser Card Edge Pinout

| Side Even | Signal | | Side Odd | Signal | |
|-----------|----------|-----------------------------|----------|-----------|-----------------------------|
| 200 | 12V | 20W 3.3V generated on riser | 199 | 12V | For IOM |
| 198 | 12V | 66W for GPU | 197 | 12V | 66W for GPU |
| 196 | 12V | 66W for GPU | 195 | spare | |
| 194 | spare | | 193 | spare | |
| 192 | spare | | 191 | GND | |
| 190 | spare | | 189 | SMDATA | For rIOM temp sensor |
| 188 | GND | | 187 | 5VAUX | For DNM and IOM wake on LAN |
| 186 | SMCLK | For rIOM temp sensor | 185 | PRESENT# | rIOM function present |
| 184 | 3.3V Aux | For DNM and IOM wake on LAN | 183 | RIOM_ACT# | |
| 182 | GND | | 181 | RXD_3 | RGMIi receive data |
| 180 | TXD_0 | RGMIi txmit data | 179 | RXD_2 | RGMIi receive data |
| 178 | TXD_1 | RGMIi txmit data | 177 | RXD_1 | RGMIi receive data |
| 176 | TXD_2 | RGMIi txmit data | 175 | RXD_0 | RGMIi receive data |
| 174 | TXD_3 | RGMIi txmit data | 173 | GND | |
| 172 | GND | | 171 | RX_CTL | RGMIi receive Cntrl |
| 170 | TX_CLK | RGMIi txmit Clock | 169 | GND | |
| 168 | TX_CTL | RGMIi txmit Cntrl | 167 | RX_CLK | RGMIi receive Clock |
| 166 | MDIO | | 165 | MDC | |
| 164 | spare | | 163 | GND | |
| 162 | GND | | 161 | IB_CLK3+ | |
| 160 | PERST# | | 159 | IB_CLK3- | |
| 158 | WAKE# | | 157 | GND | |
| 156 | GND | | 155 | CLK1+ | |
| 154 | CLK2+ | | 153 | CLK1- | |
| 152 | CLK2- | | 151 | GND | |
| 150 | GND | | 149 | R00+ | |
| 148 | T00+ | | 147 | R00- | |
| 146 | T00- | | 145 | GND | |
| 144 | GND | | 143 | R01+ | |
| 142 | T01+ | | 141 | R01- | |
| 140 | T01- | | 139 | GND | |
| 138 | GND | | 137 | R02+ | |
| 136 | T02+ | | 135 | R02- | |
| 134 | T02- | | 133 | GND | |
| 132 | GND | | 131 | R03+ | |
| 130 | T03+ | | 129 | R03- | |
| 128 | T03- | | 127 | GND | |

| Side Even | Signal | | Side Odd | Signal | |
|-----------|---------|--|----------|---------|--|
| 126 | GND | | 125 | R04+ | |
| 124 | T04+ | | 123 | R04- | |
| 122 | T04- | | 121 | GND | |
| 120 | GND | | 119 | R05+ | |
| 118 | T05+ | | 117 | R05- | |
| 116 | T05- | | 115 | GND | |
| 114 | GND | | 113 | R06+ | |
| 112 | T06+ | | 111 | R06- | |
| 110 | T06- | | 109 | GND | |
| 108 | GND | | 107 | R07+ | |
| 106 | T07+ | | 105 | R07- | |
| 104 | T07- | | 103 | GND | |
| 102 | GND | | 101 | IB_R00+ | |
| 100 | IB_T00+ | | 99 | IB_R00- | |
| 98 | IB_T00- | | 97 | GND | |
| 96 | GND | | 95 | IB_R01+ | |
| 94 | IB_T01+ | | 93 | IB_R01- | |
| 92 | IB_T01- | | 91 | GND | |
| 90 | GND | | 89 | IB_R02+ | |
| 88 | IB_T02+ | | 87 | IB_R02- | |
| 86 | IB_T02- | | 85 | GND | |
| 84 | GND | | 83 | IB_R03+ | |
| 82 | IB_T03+ | | 81 | IB_R03- | |
| 80 | IB_T03- | | 79 | GND | |
| 78 | GND | | 77 | IB_R04+ | |
| 76 | IB_T04+ | | 75 | IB_R04- | |
| 74 | IB_T04- | | 73 | GND | |
| 72 | GND | | 71 | IB_R05+ | |
| 70 | IB_T05+ | | 69 | IB_R05- | |
| 68 | IB_T05- | | 67 | GND | |
| 66 | GND | | 65 | GND | |
| | | | | | |
| 64 | GND | | 63 | GND | |
| 62 | GND | | 61 | IB_R06+ | |
| 60 | IB_T06+ | | 59 | IB_R06- | |
| 58 | IB_T06- | | 57 | GND | |
| 56 | GND | | 55 | IB_R07+ | |
| 54 | IB_T07+ | | 53 | IB_R07- | |
| 52 | IB_T07- | | 51 | GND | |
| 50 | GND | | 49 | R08+ | |
| 48 | T08+ | | 47 | R08- | |
| 46 | T08- | | 45 | GND | |
| 44 | GND | | 43 | R09+ | |
| 42 | T09+ | | 41 | R09- | |
| 40 | T09- | | 39 | GND | |
| 38 | GND | | 37 | R10+ | |
| 36 | T10+ | | 35 | R10- | |
| 34 | T10- | | 33 | GND | |
| 32 | GND | | 31 | R11+ | |

| Side Even | Signal | | Side Odd | Signal | |
|-----------|--------|--|----------|----------|----------|
| 30 | T11+ | | 29 | R11- | |
| 28 | T11- | | 27 | GND | |
| 26 | GND | | 25 | R12+ | |
| 24 | T12+ | | 23 | R12- | |
| 22 | T12- | | 21 | GND | |
| 20 | GND | | 19 | R13+ | |
| 18 | T13+ | | 17 | R13- | |
| 16 | T13- | | 15 | GND | |
| 14 | GND | | 13 | R14+ | |
| 12 | T14+ | | 11 | R14- | |
| 10 | T14- | | 9 | GND | |
| 8 | GND | | 7 | R15+ | |
| 6 | T15+ | | 5 | R15- | |
| 4 | T15- | | 3 | GND | |
| 2 | GND | | 1 | Riser ID | Riser ID |

Table 70. PCI Express* Slot Pinout on Riser Card

| Pin | Pin Name | Description | Pin | Pin Name | Description |
|-----|----------|-----------------------------|-----|-----------|-----------------------------|
| B1 | 12V | 20W 3.3V generated on riser | A1 | 12V | 20W 3.3V generated on riser |
| B2 | 12V | 66W for GPU | A2 | 12V | 66W for GPU |
| B3 | 12V | 66W for GPU | A3 | 12V | 66W for GPU |
| B4 | 12V | 66W for GPU | A4 | SMDATA | for rIOM temp sensor |
| B5 | SMCLK | for rIOM temp sensor | A5 | 5VAUX | For DNM and IOM wake on LAN |
| B6 | 3.3V Aux | For DNM and IOM wake on LAN | A6 | PRESENT# | DNM function present |
| B7 | GND | | A7 | RIOM_ACT# | |
| B8 | TXD_0 | RGMII txmit data | A8 | RXD_3 | RGMII receive data |
| B9 | TXD_1 | RGMII txmit data | A9 | RXD_2 | RGMII receive data |
| B10 | TXD_2 | RGMII txmit data | A10 | RXD_1 | RGMII receive data |
| B11 | TXD_3 | RGMII txmit data | A11 | RXD_0 | RGMII receive data |
| KEY | | | | | |
| B12 | GND | | A12 | RX_CTL | RGMII receive Cntrl |
| B13 | TX_CLK | RGMII txmit Clock | A13 | GND | |
| B14 | TX_CTL | RGMII txmit Cntrl | A14 | RX_CLK | RGMII receive Clock |
| B15 | MDIO | | A15 | MDC | |
| B16 | PERST# | | A16 | GND | |
| B17 | WAKE# | | A17 | REFCLK+ | Clock pair 1 |
| B18 | PETxP0 | Tx Lane 0+ | A18 | REFCLK- | Clock pair 1 |
| B19 | PETxN0 | Tx Lane 0- | A19 | GND | |
| B20 | GND | | A20 | PERxP0 | Rx Lane 0+ |
| B21 | GND | | A21 | PERxN0 | Rx Lane 0- |
| B22 | PETxP1 | Tx Lane 1+ | A22 | GND | |
| B23 | PETxN1 | Tx Lane 1- | A23 | GND | |
| B24 | GND | | A24 | PERxP1 | Rx Lane 1+ |

| Pin | Pin Name | Description | Pin | Pin Name | Description |
|-----|----------|-------------|-----|----------|-------------|
| B25 | GND | | A25 | PERxN1 | Rx Lane 1- |
| B26 | PETxP2 | Tx Lane 2+ | A26 | GND | |
| B27 | PETxN2 | Tx Lane 2- | A27 | GND | |
| B28 | GND | | A28 | PERxP2 | Rx Lane 2+ |
| B29 | GND | | A29 | PERxN2 | Rx Lane 2- |
| B30 | PETxP3 | Tx Lane 3+ | A30 | GND | |
| B31 | PETxN3 | Tx Lane 3- | A31 | GND | |
| B32 | GND | | A32 | PERxP3 | Rx Lane 3+ |
| B33 | GND | | A33 | PERxN3 | Rx Lane 3- |
| B34 | PETxP4 | Tx Lane 4+ | A34 | GND | |
| B35 | PETxN4 | Tx Lane 4- | A35 | GND | |
| B36 | GND | | A36 | PERxP4 | Rx Lane 4+ |
| B37 | GND | | A37 | PERxN4 | Rx Lane 4- |
| B38 | PETxP5 | Tx Lane 5+ | A38 | GND | |
| B39 | PETxN5 | Tx Lane 5- | A39 | GND | |
| B40 | GND | | A40 | PERxP5 | Rx Lane 5+ |
| B41 | GND | | A41 | PERxN5 | Rx Lane 5- |
| B42 | PETxP6 | Tx Lane 6+ | A42 | GND | |
| B43 | PETxN6 | Tx Lane 6- | A43 | GND | |
| B44 | GND | | A44 | PERxP6 | Rx Lane 6+ |
| B45 | GND | | A45 | PERxN6 | Rx Lane 6- |
| B46 | PETxP7 | Tx Lane 7+ | A46 | GND | |
| B47 | PETxN7 | Tx Lane 7- | A47 | GND | |
| B48 | GND | | A48 | PERxP7 | Rx Lane 7+ |
| B49 | GND | | A49 | PERxN7 | Rx Lane 7- |
| B50 | PETxP8 | Tx Lane 8+ | A50 | GND | |
| B51 | PETxN8 | Tx Lane 8- | A51 | GND | |
| B52 | GND | | A52 | PERxP8 | Rx Lane 8+ |
| B53 | GND | | A53 | PERxN8 | Rx Lane 8- |
| B54 | PETxP9 | Tx Lane 9+ | A54 | GND | |
| B55 | PETxN9 | Tx Lane 9- | A55 | GND | |
| B56 | GND | | A56 | PERxP9 | Rx Lane 9+ |
| B57 | GND | | A57 | PERxN9 | Rx Lane 9- |
| B58 | PETxP10 | Tx Lane 10+ | A58 | GND | |
| B59 | PETxN10 | Tx Lane 10- | A59 | GND | |
| B60 | GND | | A60 | PERxP10 | Rx Lane 10+ |
| B61 | GND | | A61 | PERxN10 | Rx Lane 10- |
| B62 | PETxP11 | Tx Lane 11+ | A62 | GND | |
| B63 | PETxN11 | Tx Lane 11- | A63 | GND | |
| B64 | GND | | A64 | PERxP11 | Rx Lane 11+ |
| B65 | GND | | A65 | PERxN11 | Rx Lane 11- |
| B66 | PETxP12 | Tx Lane 12+ | A66 | GND | |
| B67 | PETxN12 | Tx Lane 12- | A67 | GND | |

| Pin | Pin Name | Description | Pin | Pin Name | Description |
|-----|----------|--------------|-----|----------|-------------|
| B68 | GND | | A68 | PERxP12 | Rx Lane 12+ |
| B69 | GND | | A69 | PERxN12 | Rx Lane 12- |
| B70 | PETxP13 | Tx Lane 13+ | A70 | GND | |
| B71 | PETxN13 | Tx Lane 13- | A71 | GND | |
| B72 | GND | | A72 | PERxP13 | Rx Lane 13+ |
| B73 | GND | | A73 | PERxN13 | Rx Lane 13- |
| B74 | PETxP14 | Tx Lane 14+ | A74 | GND | |
| B75 | PETxN14 | Tx Lane 14- | A75 | GND | |
| B76 | GND | | A76 | PERxP14 | Rx Lane 14+ |
| B77 | REFCLK+ | Clock pair 2 | A77 | PERxN14 | Rx Lane 14- |
| B78 | REFCLK- | Clock pair 2 | A78 | GND | |
| B79 | GND | | A79 | PERxP15 | Rx Lane 15+ |
| B80 | PETxP15 | Tx Lane 15+ | A80 | PERxN15 | Rx Lane 15- |
| B81 | PETxN15 | Tx Lane 15- | A81 | GND | |
| B82 | GND | | A82 | Riser ID | |

Table 71. IO Module Slot on Carrier

| Pin | Signal | Pin | Signal |
|-----|------------------|-----|-------------------|
| 1 | 3.3V | 2 | 12V |
| 3 | 3.3V | 4 | 12V |
| 5 | 3.3V | 6 | 12V |
| 7 | 3.3V | 8 | 12V |
| 9 | RSVD | 10 | FRU/TEMP ADDR [I] |
| 11 | GND | 12 | 5VSB |
| 13 | RSVD+ | 14 | FM_IO_MODULE_EN |
| 15 | RSVD- | 16 | 3.3VSTBY |
| 17 | GND | 18 | LED_GLOBAL_ACT# |
| 19 | RSVD | 20 | FM_IOM_PRESENT_N |
| 21 | RSVD | 22 | WAKE# |
| 23 | GND | 24 | PERST# |
| 25 | SMB_CLK | 26 | GND |
| 27 | SMB_DAT | 28 | rIOM REFCLK+ [0] |
| 29 | GND | 30 | rIOM REFCLK- [0] |
| 31 | PCIe Gen3 Tn [7] | 32 | GND |
| 33 | PCIe Gen3 Tp [7] | 34 | PCIe Gen3 Rn [7] |
| 35 | GND | 36 | PCIe Gen3 Rp [7] |
| 37 | PCIe Gen3 Tn [6] | 38 | GND |
| 39 | PCIe Gen3 Tp [6] | 40 | PCIe Gen3 Rn [6] |
| 41 | GND | 42 | PCIe Gen3 Rp [6] |
| 43 | PCIe Gen3 Tn [5] | 44 | GND |

| Pin | Signal | Pin | Signal |
|-----|------------------|-----|------------------|
| 45 | PCIe Gen3 Tp [5] | 46 | PCIe Gen3 Rn [5] |
| 47 | GND | 48 | PCIe Gen3 Rp [5] |
| 49 | PCIe Gen3 Tn [4] | 50 | GND |
| 51 | PCIe Gen3 Tp [4] | 52 | PCIe Gen3 Rn [4] |
| 53 | GND | 54 | PCIe Gen3 Rp [4] |
| 55 | PCIe Gen3 Tn [3] | 56 | GND |
| 57 | PCIe Gen3 Tp [3] | 58 | PCIe Gen3 Rn [3] |
| 59 | GND | 60 | PCIe Gen3 Rp [3] |
| 61 | PCIe Gen3 Tn [2] | 62 | GND |
| 63 | PCIe Gen3 Tp [2] | 64 | PCIe Gen3 Rn [2] |
| 65 | GND | 66 | PCIe Gen3 Rp [2] |
| 67 | PCIe Gen3 Tn [1] | 68 | GND |
| 69 | PCIe Gen3 Tp [1] | 70 | PCIe Gen3 Rn [1] |
| 71 | GND | 72 | PCIe Gen3 Rp [1] |
| 73 | PCIe Gen3 Tn [0] | 74 | GND |
| 75 | PCIe Gen3 Tp [0] | 76 | PCIe Gen3 Rn [0] |
| 77 | GND | 78 | PCIe Gen3 Rp [0] |
| 79 | RSVD | 80 | GND |

Appendix A: Integration and Usage Tips

Before attempting to integrate and configure your system, you should reference this section, which provides a list of useful information.

- After the system is integrated with processors, memory, and peripheral devices, the FRUSDR utility **must** be run to load the proper Sensor Data Record data to the integrated Server Management subsystem. Failure to run this utility may prevent Server Management from accurately monitoring system health and may affect system performance. The FRUSDR utility for this server system can either be run from the Intel® Deployment CDROM that came with your system, or can be downloaded from the Intel® website referenced at the bottom of this page.
- To ensure the highest system reliability, make sure the latest system software is loaded on the server before deploying the system onto a live networking environment. This includes system BIOS, FRUSDR, BMC firmware, and hot-swap controller firmware. The system software can be updated using the Intel® Deployment CDROM that came with your system or can be downloaded from the Intel® website referenced at the bottom of this page.
- System fans are not hot-swappable.
- Only supported memory validated by Intel® should be used in this server system. A list of supported memory can be found in the Intel® Server Board S2600WP Tested Memory List which can be downloaded from the Intel® website referenced at the bottom of this page.
- This system supports the Intel® Xeon® processor E5-2600 and E5-2600 v2 sequence. You cannot use Intel® Xeon® processors not referenced on the supported processor list in this server system.
- You must use the CPU/memory air duct to maintain system thermals.
- To maintain system thermals, you must populate all hard drive bays with either a hard drive or drive blank.
- You must remove AC power from the system prior to opening the chassis for service.

You can download the latest system documentation, drivers, and system software from the Intel® Support website at

http://www.intel.com/p/en_US/support/highlights/server/sb-s2600wp.

Appendix B: POST Code LED Decoder

During the system boot process, the BIOS executes a number of platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the POST code to the POST Code Diagnostic LEDs on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, you can use the diagnostic LEDs to identify the last POST process executed.

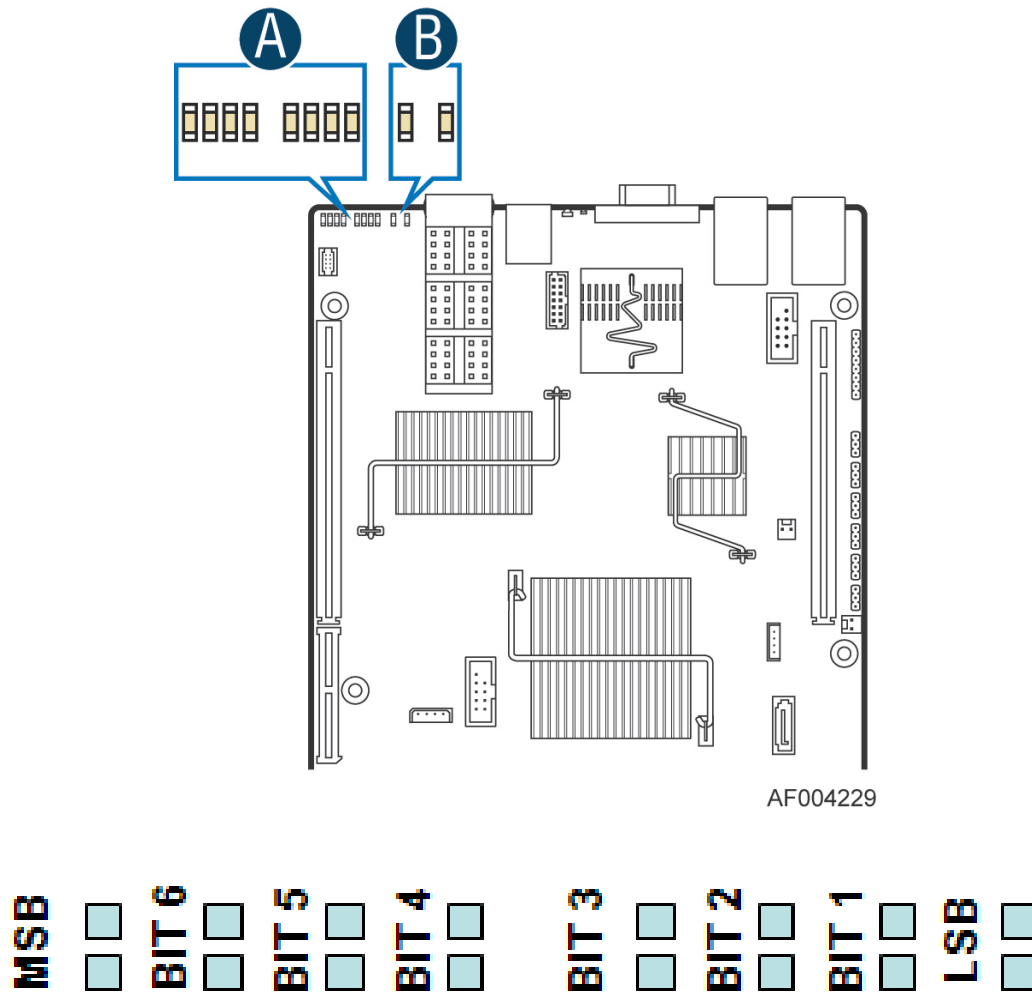


Figure 42. Diagnostic LED location

Table 72. POST Code Diagnostic LED Location

| | | | |
|----------|-----------------------|----------|-----------------------|
| A | ID LED | B | Status LED |
| C | Diagnostic LED #7 MSB | G | Diagnostic LED #3 |
| D | Diagnostic LED #6 | H | Diagnostic LED #2 |
| E | Diagnostic LED #5 | I | Diagnostic LED #1 |
| F | Diagnostic LED #4 | J | Diagnostic LED #0 LSB |

Each POST code is represented by the eight amber diagnostic LEDs. The POST codes are divided into two nibbles, an upper nibble and a lower nibble. The upper nibble bits are represented by diagnostic LEDs #4, #5, #6, and #7. The lower nibble bits are represented by diagnostics LEDs #0, #1, #2, and #3. If the bit is set in the upper and lower nibbles, then the corresponding LED is lit. If the bit is clear, then the corresponding LED is off.

The diagnostic LED #7 is labeled as “MSB” (Most Significant Bit), and the diagnostic LED #0 is labeled as “LSB” (Least Significant Bit).

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

Table 73. POST Progress Code LED Example

| LEDs | Upper Nibble LEDs | | | | Lower Nibble LEDs | | | |
|----------------|-------------------|--------|--------|--------|-------------------|--------|--------|---------------|
| | MSB LED #7 | LED #6 | LED #5 | LED #4 | LED #3 | LED #2 | LED #1 | LSB LED #0 |
| | 8h | 4h | 2h | 1h | 8h | 4h | 2h | 1h |
| Status | ON | OFF | ON | OFF | ON | ON | OFF | OFF |
| Results | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| | Ah | | | | Ch | | | |

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh.

Table 74. MRC Fatal Error Codes

| Error Code | Fatal Error Code Explanation (with MRC Internal Minor Code) |
|------------|---|
| 0xE8 | <u>No Usable Memory Error:</u> 01h = No memory was detected via SPD read, or invalid config that causes no operable memory. 02h = Memory DIMMs on all channels of all sockets are disabled due to hardware memtest error. 03h = No memory installed. All channels are disabled. |
| 0xE9 | <u>Memory is locked by Intel® Trusted Execution Technology and is inaccessible.</u> |
| 0xEA | <u>DDR3 Channel Training Error:</u> 01h = Error on read DQ/DQS (Data/Data Strobe) init 02h = Error on Receive Enable 03h = Error on Write Leveling 04h = Error on write DQ/DQS (Data/Data Strobe) |
| 0xEB | <u>Memory Test Failure:</u> 01h = Software memtest failure. 02h = Hardware memtest failed. 03h = Hardware Memtest failure in Lockstep Channel mode requiring a channel to be disabled. <i>This is a fatal error which requires a reset and calling MRC with a different RAS mode to retry.</i> |
| 0xED | <u>DIMM Configuration/Population Error:</u> 01h = Different DIMM types (UDIMM, RDIMM, LRDIMM) are detected installed in the system. 02h = Violation of DIMM population rules. 03h = The 3rd DIMM slot can not be populated when QR DIMMs are installed. 04h = UDIMMs are not supported in the 3rd DIMM slot. 05h = Unsupported DIMM Voltage. |
| 0xEF | <u>Indicates a CLTT table structure error.</u> |

Table 75. MRC Progress Codes

| Progress Code | Main Sequence | Subsequences/Subfunctions |
|---------------|---|---------------------------|
| 0xB0 | Detect DIMM population | —n/a— |
| 0xB1 | Set DDR3 frequency | —n/a— |
| 0xB2 | Gather remaining SPD data | —n/a— |
| 0xB3 | Program registers on the memory controller level | —n/a— |
| 0xB4 | Evaluate RAS modes and save rank information | —n/a— |
| 0xB5 | Program registers on the channel level | —n/a— |
| 0xB6 | Perform the JEDEC defined initialization sequence | —n/a— |
| 0xB7 | Train DDR3 ranks | —n/a— |
| 0x01 | ↓ | Read DQ/DQS training |
| 0x02 | ↓ | Receive Enable training |
| 0x03 | ↓ | Write Leveling training |
| 0x04 | ↓ | Write DQ/DQS training |
| 0x05 | ↓ | DDR channel training done |
| 0xB8 | Initialize CLTT/OLTT | —n/a— |
| 0xB9 | Hardware memory test and init | —n/a— |
| 0xBA | Execute software memory init | —n/a— |
| 0xBB | Program memory map and interleaving | —n/a— |
| 0xBC | Program RAS configuration | —n/a— |
| 0xBF | MRC is done | —n/a— |

Table 76. POST Progress Codes

| Progress Code | Description |
|------------------|---|
| SEC Phase | |
| 0x01 | First POST code after CPU reset |
| 0x02 | Microcode load begin |
| 0x03 | CRAM initialization begin |
| 0x04 | Pei Cache When Disabled |
| 0x05 | SEC Core At Power On Begin |
| 0x06 | Early CPU initialization during Sec Phase |

| Progress Code | Description |
|--|--|
| 0x07 | Early SB initialization during Sec Phase |
| 0x08 | Early NB initialization during Sec Phase |
| 0x09 | End Of Sec Phase |
| 0x0E | Microcode Not Found |
| 0x0F | Microcode Not Loaded |
| PEI Phase | |
| 0x10 | PEI Core |
| 0x11 | CPU PEIM |
| 0x15 | NB PEIM |
| 0x19 | SB PEIM |
| MRC Progress Codes <i>At this point the MRC Progress Code sequence is executed See Table 75.</i> | |
| 0x31 | Memory Installed |
| 0x32 | CPU PEIM (CPU Init) |
| 0x33 | CPU PEIM (Cache Init) |
| 0x34 | CPU PEIM (BSP Select) |
| 0x35 | CPU PEIM (AP Init) |
| 0x36 | CPU PEIM (CPU SMM Init) |
| 0x4F | Dxe IPL started |
| DXE Phase | |
| 0x60 | DXE Core started |
| 0x61 | DXE NVRAM Init |
| 0x62 | SB RUN Init |
| 0x63 | DXE CPU Init |
| 0x68 | DXE PCI Host Bridge Init |
| 0x69 | DXE NB Init |
| 0x6A | DXE NB SMM Init |
| 0x70 | DXE SB Init |
| 0x71 | DXE SB SMM Init |
| 0x72 | DXE SB devices Init |
| 0x78 | DXE ACPI Init |

| Progress Code | Description |
|---------------|----------------------------------|
| 0x79 | DXE CSM Init |
| 0x90 | DXE BDS Started |
| 0x91 | DXE BDS connect drivers |
| 0x92 | DXE PCI Bus begin |
| 0x93 | DXE PCI Bus HPC Init |
| 0x94 | DXE PCI Bus enumeration |
| 0x95 | DXE PCI Bus resource requested |
| 0x96 | DXE PCI Bus assign resource |
| 0x97 | DXE CON_OUT connect |
| 0x98 | DXE CON_IN connect |
| 0x99 | DXE SIO Init |
| 0x9A | DXE USB start |
| 0x9B | DXE USB reset |
| 0x9C | DXE USB detect |
| 0x9D | DXE USB enable |
| 0xA1 | DXE IDE begin |
| 0xA2 | DXE IDE reset |
| 0xA3 | DXE IDE detect |
| 0xA4 | DXE IDE enable |
| 0xA5 | DXE SCSI begin |
| 0xA6 | DXE SCSI reset |
| 0xA7 | DXE SCSI detect |
| 0xA8 | DXE SCSI enable |
| 0xA9 | DXE verifying SETUP password |
| 0xAB | DXE SETUP start |
| 0xAC | DXE SETUP input wait |
| 0xAD | DXE Ready to Boot |
| 0xAE | DXE Legacy Boot |
| 0xAF | DXE Exit Boot Services |
| 0xB0 | RT Set Virtual Address Map Begin |
| 0xB1 | RT Set Virtual Address Map End |

| Progress Code | Description |
|----------------------|---|
| 0xB2 | DXE Legacy Option ROM init |
| 0xB3 | DXE Reset system |
| 0xB4 | DXE USB Hot plug |
| 0xB5 | DXE PCI BUS Hot plug |
| 0xB6 | DXE NVRAM cleanup |
| 0xB7 | DXE Configuration Reset |
| 0x00 | INT19 |
| S3 Resume | |
| 0xE0 | S3 Resume PEIM (S3 started) |
| 0xE1 | S3 Resume PEIM (S3 boot script) |
| 0xE2 | S3 Resume PEIM (S3 Video Repost) |
| 0xE3 | S3 Resume PEIM (S3 OS wake) |
| BIOS Recovery | |
| 0xF0 | PEIM which detected forced Recovery condition |
| 0xF1 | PEIM which detected User Recovery condition |
| 0xF2 | Recovery PEIM (Recovery started) |
| 0xF3 | Recovery PEIM (Capsule found) |
| 0xF4 | Recovery PEIM (Capsule loaded) |

Appendix C: Video POST Code Errors

Whenever possible, the BIOS outputs the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The Response section in the following table is divided into three types:

- **No Pause:** The message is displayed on the local Video screen during POST or in the Error Manager. The system continues booting with a degraded state. The user may want to replace the erroneous unit. The setup POST error Pause setting does not have any effect with this error.
- **Pause:** The message is displayed on the Error Manager screen, and an error is logged to the SEL. The setup POST error Pause setting determines whether the system pauses to the Error Manager for this type of error, where the user can take immediate corrective action or choose to continue booting.
- **Halt:** The message is displayed on the Error Manager screen, an error is logged to the SEL, and the system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system. The setup POST error Pause setting does not have any effect with this error.

Table 77. POST Error Message and Handling

| Error Code | Error Message | Response |
|------------|---|----------|
| 0012 | System RTC date/time not set | Major |
| 0048 | Password check failed | Major |
| 113 | Fixed media not detected | Major |
| 0140 | PCI component encountered a PERR error | Major |
| 0141 | PCI resource conflict | Major |
| 0146 | PCI out of resources error | Major |
| 0191 | Processor core/thread count mismatch detected | Fatal |
| 0192 | Processor cache size mismatch detected | Fatal |
| 0194 | Processor family mismatch detected | Fatal |
| 0195 | Processor Intel(R) QPI link frequencies unable to synchronize | Fatal |
| 0196 | Processor model mismatch detected | Fatal |
| 0197 | Processor frequencies unable to synchronize | Fatal |
| 5220 | BIOS Settings reset to default settings | Major |
| 5221 | Passwords cleared by jumper | Major |
| 5224 | Password clear jumper is Set | Major |
| 8130 | Processor 01 disabled | Major |
| 8131 | Processor 02 disabled | Major |
| 8132 | Processor 03 disabled | Major |
| 8133 | Processor 04 disabled | Major |
| 8160 | Processor 01 unable to apply microcode update | Major |

| Error Code | Error Message | Response |
|------------|---|----------|
| 8161 | Processor 02 unable to apply microcode update | Major |
| 8162 | Processor 03 unable to apply microcode update | Major |
| 8163 | Processor 04 unable to apply microcode update | Major |
| 8170 | Processor 01 failed Self Test (BIST) | Major |
| 8171 | Processor 02 failed Self Test (BIST) | Major |
| 8172 | Processor 03 failed Self Test (BIST) | Major |
| 8173 | Processor 04 failed Self Test (BIST) | Major |
| 8180 | Processor 01 microcode update not found | Minor |
| 8181 | Processor 02 microcode update not found | Minor |
| 8182 | Processor 03 microcode update not found | Minor |
| 8183 | Processor 04 microcode update not found | Minor |
| 8190 | Watchdog timer failed on last boot | Major |
| 8198 | OS boot watchdog timer failure | Major |
| 8300 | Baseboard management controller failed self test | Major |
| 8305 | Hot Swap Controller failure | Major |
| 83A0 | Management Engine (ME) failed self test | Major |
| 83A1 | Management Engine (ME) Failed to respond. | Major |
| 84F2 | Baseboard management controller failed to respond | Major |
| 84F3 | Baseboard management controller in update mode | Major |
| 84F4 | Sensor data record empty | Major |
| 84FF | System event log full | Minor |
| 8500 | Memory component could not be configured in the selected RAS mode | Major |
| 8501 | DIMM Population Error | Major |
| 8520 | DIMM_A1 failed test/initialization | Major |
| 8521 | DIMM_A2 failed test/initialization | Major |
| 8522 | DIMM_A3 failed test/initialization | Major |
| 8523 | DIMM_B1 failed test/initialization | Major |
| 8524 | DIMM_B2 failed test/initialization | Major |
| 8525 | DIMM_B3 failed test/initialization | Major |
| 8526 | DIMM_C1 failed test/initialization | Major |
| 8527 | DIMM_C2 failed test/initialization | Major |
| 8528 | DIMM_C3 failed test/initialization | Major |
| 8529 | DIMM_D1 failed test/initialization | Major |
| 852A | DIMM_D2 failed test/initialization | Major |
| 852B | DIMM_D3 failed test/initialization | Major |
| 852C | DIMM_E1 failed test/initialization | Major |
| 852D | DIMM_E2 failed test/initialization | Major |
| 852E | DIMM_E3 failed test/initialization | Major |
| 852F | DIMM_F1 failed test/initialization | Major |
| 8530 | DIMM_F2 failed test/initialization | Major |
| 8531 | DIMM_F3 failed test/initialization | Major |
| 8532 | DIMM_G1 failed test/initialization | Major |
| 8533 | DIMM_G2 failed test/initialization | Major |
| 8534 | DIMM_G3 failed test/initialization | Major |
| 8535 | DIMM_H1 failed test/initialization | Major |

| Error Code | Error Message | Response |
|----------------------|---|----------|
| 8536 | DIMM_H2 failed test/initialization | Major |
| 8537 | DIMM_H3 failed test/initialization | Major |
| 8538 | DIMM_J1 failed test/initialization | Major |
| 8539 | DIMM_J2 failed test/initialization | Major |
| 853A | DIMM_J3 failed test/initialization | Major |
| 853B | DIMM_K1 failed test/initialization | Major |
| 853C | DIMM_K2 failed test/initialization | Major |
| 853D | DIMM_K3 failed test/initialization | Major |
| 853E | DIMM_L1 failed test/initialization | Major |
| 853F (Go to 85C0) | DIMM_L2 failed test/initialization | Major |
| 8540 | DIMM_A1 disabled | Major |
| 8541 | DIMM_A2 disabled | Major |
| 8542 | DIMM_A3 disabled | Major |
| 8543 | DIMM_B1 disabled | Major |
| 8544 | DIMM_B2 disabled | Major |
| 8545 | DIMM_B3 disabled | Major |
| 8546 | DIMM_C1 disabled | Major |
| 8547 | DIMM_C2 disabled | Major |
| 8548 | DIMM_C3 disabled | Major |
| 8549 | DIMM_D1 disabled | Major |
| 854A | DIMM_D2 disabled | Major |
| 854B | DIMM_D3 disabled | Major |
| 854C | DIMM_E1 disabled | Major |
| 854D | DIMM_E2 disabled | Major |
| 854E | DIMM_E3 disabled | Major |
| 854F | DIMM_F1 disabled | Major |
| 8550 | DIMM_F2 disabled | Major |
| 8551 | DIMM_F3 disabled | Major |
| 8552 | DIMM_G1 disabled | Major |
| 8553 | DIMM_G2 disabled | Major |
| 8554 | DIMM_G3 disabled | Major |
| 8555 | DIMM_H1 disabled | Major |
| 8556 | DIMM_H2 disabled | Major |
| 8557 | DIMM_H3 disabled | Major |
| 8558 | DIMM_J1 disabled | Major |
| 8559 | DIMM_J2 disabled | Major |
| 855A | DIMM_J3 disabled | Major |
| 855B | DIMM_K1 disabled | Major |
| 855C | DIMM_K2 disabled | Major |
| 855D | DIMM_K3 disabled | Major |
| 855E | DIMM_L1 disabled | Major |
| 855F (Go to 85D0) | DIMM_L2 disabled | Major |
| 8560 | DIMM_A1 encountered a Serial Presence Detection (SPD) failure | Major |

| Error Code | Error Message | Response |
|----------------------|---|----------|
| 8561 | DIMM_A2 encountered a Serial Presence Detection (SPD) failure | Major |
| 8562 | DIMM_A3 encountered a Serial Presence Detection (SPD) failure | Major |
| 8563 | DIMM_B1 encountered a Serial Presence Detection (SPD) failure | Major |
| 8564 | DIMM_B2 encountered a Serial Presence Detection (SPD) failure | Major |
| 8565 | DIMM_B3 encountered a Serial Presence Detection (SPD) failure | Major |
| 8566 | DIMM_C1 encountered a Serial Presence Detection (SPD) failure | Major |
| 8567 | DIMM_C2 encountered a Serial Presence Detection (SPD) failure | Major |
| 8568 | DIMM_C3 encountered a Serial Presence Detection (SPD) failure | Major |
| 8569 | DIMM_D1 encountered a Serial Presence Detection (SPD) failure | Major |
| 856A | DIMM_D2 encountered a Serial Presence Detection (SPD) failure | Major |
| 856B | DIMM_D3 encountered a Serial Presence Detection (SPD) failure | Major |
| 856C | DIMM_E1 encountered a Serial Presence Detection (SPD) failure | Major |
| 856D | DIMM_E2 encountered a Serial Presence Detection (SPD) failure | Major |
| 856E | DIMM_E3 encountered a Serial Presence Detection (SPD) failure | Major |
| 856F | DIMM_F1 encountered a Serial Presence Detection (SPD) failure | Major |
| 8570 | DIMM_F2 encountered a Serial Presence Detection (SPD) failure | Major |
| 8571 | DIMM_F3 encountered a Serial Presence Detection (SPD) failure | Major |
| 8572 | DIMM_G1 encountered a Serial Presence Detection (SPD) failure | Major |
| 8573 | DIMM_G2 encountered a Serial Presence Detection (SPD) failure | Major |
| 8574 | DIMM_G3 encountered a Serial Presence Detection (SPD) failure | Major |
| 8575 | DIMM_H1 encountered a Serial Presence Detection (SPD) failure | Major |
| 8576 | DIMM_H2 encountered a Serial Presence Detection (SPD) failure | Major |
| 8577 | DIMM_H3 encountered a Serial Presence Detection (SPD) failure | Major |
| 8578 | DIMM_J1 encountered a Serial Presence Detection (SPD) failure | Major |
| 8579 | DIMM_J2 encountered a Serial Presence Detection (SPD) failure | Major |
| 857A | DIMM_J3 encountered a Serial Presence Detection (SPD) failure | Major |
| 857B | DIMM_K1 encountered a Serial Presence Detection (SPD) failure | Major |
| 857C | DIMM_K2 encountered a Serial Presence Detection (SPD) failure | Major |
| 857D | DIMM_K3 encountered a Serial Presence Detection (SPD) failure | Major |
| 857E | DIMM_L1 encountered a Serial Presence Detection (SPD) failure | Major |
| 857F (Go to 85E0) | DIMM_L2 encountered a Serial Presence Detection (SPD) failure | Major |
| 85C0 | DIMM_L3 failed test/initialization | Major |
| 85C1 | DIMM_M1 failed test/initialization | Major |
| 85C2 | DIMM_M2 failed test/initialization | Major |
| 85C3 | DIMM_M3 failed test/initialization | Major |
| 85C4 | DIMM_N1 failed test/initialization | Major |
| 85C5 | DIMM_N2 failed test/initialization | Major |
| 85C6 | DIMM_N3 failed test/initialization | Major |
| 85C7 | DIMM_P1 failed test/initialization | Major |
| 85C8 | DIMM_P2 failed test/initialization | Major |
| 85C9 | DIMM_P3 failed test/initialization | Major |
| 85CA | DIMM_R1 failed test/initialization | Major |
| 85CB | DIMM_R2 failed test/initialization | Major |
| 85CC | DIMM_R3 failed test/initialization | Major |

| Error Code | Error Message | Response |
|------------|---|----------|
| 85CD | DIMM_T1 failed test/initialization | Major |
| 85CE | DIMM_T2 failed test/initialization | Major |
| 85CF | DIMM_T3 failed test/initialization | Major |
| 85D0 | DIMM_L3 disabled | Major |
| 85D1 | DIMM_M1 disabled | Major |
| 85D2 | DIMM_M2 disabled | Major |
| 85D3 | DIMM_M3 disabled | Major |
| 85D4 | DIMM_N1 disabled | Major |
| 85D5 | DIMM_N2 disabled | Major |
| 85D6 | DIMM_N3 disabled | Major |
| 85D7 | DIMM_P1 disabled | Major |
| 85D8 | DIMM_P2 disabled | Major |
| 85D9 | DIMM_P3 disabled | Major |
| 85DA | DIMM_R1 disabled | Major |
| 85DB | DIMM_R2 disabled | Major |
| 85DC | DIMM_R3 disabled | Major |
| 85DD | DIMM_T1 disabled | Major |
| 85DE | DIMM_T2 disabled | Major |
| 85DF | DIMM_T3 disabled | Major |
| 85E0 | DIMM_L3 encountered a Serial Presence Detection (SPD) failure | Major |
| 85E1 | DIMM_M1 encountered a Serial Presence Detection (SPD) failure | Major |
| 85E2 | DIMM_M2 encountered a Serial Presence Detection (SPD) failure | Major |
| 85E3 | DIMM_M3 encountered a Serial Presence Detection (SPD) failure | Major |
| 85E4 | DIMM_N1 encountered a Serial Presence Detection (SPD) failure | Major |
| 85E5 | DIMM_N2 encountered a Serial Presence Detection (SPD) failure | Major |
| 85E6 | DIMM_N3 encountered a Serial Presence Detection (SPD) failure | Major |
| 85E7 | DIMM_P1 encountered a Serial Presence Detection (SPD) failure | Major |
| 85E8 | DIMM_P2 encountered a Serial Presence Detection (SPD) failure | Major |
| 85E9 | DIMM_P3 encountered a Serial Presence Detection (SPD) failure | Major |
| 85EA | DIMM_R1 encountered a Serial Presence Detection (SPD) failure | Major |
| 85EB | DIMM_R2 encountered a Serial Presence Detection (SPD) failure | Major |
| 85EC | DIMM_R3 encountered a Serial Presence Detection (SPD) failure | Major |
| 85ED | DIMM_T1 encountered a Serial Presence Detection (SPD) failure | Major |
| 85EE | DIMM_T2 encountered a Serial Presence Detection (SPD) failure | Major |
| 85EF | DIMM_T3 encountered a Serial Presence Detection (SPD) failure | Major |
| 8604 | POST Reclaim of non-critical NVRAM variables | Minor |
| 8605 | BIOS Settings are corrupted | Major |
| 8606 | NVRAM variable space was corrupted and has been reinitialized | Major |
| 92A3 | Serial port component was not detected | Major |
| 92A9 | Serial port component encountered a resource conflict error | Major |
| 9505 | ATA/ATAPI interface error | Major |
| A000 | TPM device not detected. | Minor |
| A001 | TPM device missing or not responding. | Minor |
| A002 | TPM device failure. | Minor |
| A003 | TPM device failed self test. | Minor |

| Error Code | Error Message | Response |
|------------|--|----------|
| A100 | BIOS ACM Error | Major |
| A421 | PCI component encountered a SERR error | Fatal |
| A5A0 | PCI Express component encountered a PERR error | Minor |
| A5A1 | PCI Express component encountered an SERR error | Fatal |
| A6A0 | DXE Boot Services driver: Not enough memory available to shadow a Legacy Option ROM. | Minor |

POST Error Beep Codes

The following table lists POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user-visible code on POST Progress LEDs.

Table 78. POST Error Beep Codes

| Beeps | Error Message | POST Progress Code | Description |
|-------|---------------|--------------------|---|
| 3 | Memory error | Multiple | System halted because a fatal error related to the memory was detected. |

USB Device Beeps when POST

Intel® Server Boards of the H2600 family are designed to indicate USB readiness by a series of beep codes early during POST, just before video becomes available. These four to five beeps mean that the USB is powered and initialized, in order for USB devices such as keyboard and mouse to become operational.

If a USB device such as a pen drive or USB CD/DVD ROM drive is attached to any external USB port, a beep code means that the device is recognized, powered and initialized. Each USB port will issue a beep once an external device is ready for use.

These beep codes do not signal any errors. They are designed to advise the user of USB readiness during POST and while attaching external devices.

This USB Beep is OS independent.

Glossary

| Term | Definition |
|------------------|--|
| ACPI | Advanced Configuration and Power Interface |
| AP | Application Processor |
| APIC | Advanced Programmable Interrupt Control |
| ASIC | Application Specific Integrated Circuit |
| ASMI | Advanced Server Management Interface |
| BIOS | Basic Input/Output System |
| BIST | Built-In Self Test |
| BMC | Baseboard Management Controller |
| Bridge | Circuitry connecting one computer bus to another, allowing an agent on one to access the other |
| BSP | Bootstrap Processor |
| Byte | 8-bit quantity |
| CBC | Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.) |
| CEK | Common Enabling Kit |
| CHAP | Challenge Handshake Authentication Protocol |
| CMOS | In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board |
| DPC | Direct Platform Control |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| EHCI | Enhanced Host Controller Interface |
| EMP | Emergency Management Port |
| EPS | External Product Specification |
| ESB2-E | Enterprise South Bridge 2 |
| FBD | Fully Buffered DIMM |
| FMB | Flexible Mother Board |
| FRB | Fault Resilient Booting |
| FRU | Field Replaceable Unit |
| FSB | Front Side Bus |
| GB | 1024MB |
| GPIO | General Purpose I/O |
| GTL | Gunning Transceiver Logic |
| HSC | Hot-Swap Controller |
| Hz | Hertz (1 cycle/second) |
| I ² C | Inter-Integrated Circuit Bus |
| IA | Intel® Architecture |
| IBF | Input Buffer |
| ICH | I/O Controller Hub |
| ICMB | Intelligent Chassis Management Bus |
| IERR | Internal Error |
| IFB | I/O and Firmware Bridge |
| INTR | Interrupt |
| IP | Internet Protocol |

| Term | Definition |
|----------|---|
| IPMB | Intelligent Platform Management Bus |
| IPMI | Intelligent Platform Management Interface |
| IR | Infrared |
| ITP | In-Target Probe |
| KB | 1024 bytes |
| KCS | Keyboard Controller Style |
| LAN | Local Area Network |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diode |
| LPC | Low Pin Count |
| LUN | Logical Unit Number |
| MAC | Media Access Control |
| MB | 1024KB |
| MCH | Memory Controller Hub |
| MD2 | Message Digest 2 – Hashing Algorithm |
| MD5 | Message Digest 5 – Hashing Algorithm – Higher Security |
| ms | milliseconds |
| MTTR | Memory Type Range Register |
| Mux | Multiplexor |
| NIC | Network Interface Controller |
| NMI | Non-Maskable Interrupt |
| OBF | Output Buffer |
| OEM | Original Equipment Manufacturer |
| Ohm | Unit of electrical resistance |
| PEF | Platform Event Filtering |
| PEP | Platform Event Paging |
| PIA | Platform Information Area (This feature configures the firmware for the platform hardware.) |
| PLD | Programmable Logic Device |
| PMI | Platform Management Interrupt |
| POST | Power-On Self Test |
| PSMI | Power Supply Management Interface |
| PWM | Pulse-Width Modulation |
| RAM | Random Access Memory |
| RASUM | Reliability, Availability, Serviceability, Usability, and Manageability |
| RISC | Reduced Instruction Set Computing |
| RMM3 | Remote Management Module – Third generation |
| RMM3 NIC | Remote Management Module – Third generation dedicated management NIC |
| ROM | Read Only Memory |
| RTC | Real-Time Clock (Component of ICH peripheral chip on the server board.) |
| SDR | Sensor Data Record |
| SECC | Single Edge Connector Cartridge |
| EEPROM | Serial Electrically Erasable Programmable Read-Only Memory |
| SEL | System Event Log |
| SIO | Server Input/Output |

| Term | Definition |
|------|---|
| SMI | Server Management Interrupt (SMI is the highest priority non-maskable interrupt.) |
| SMM | Server Management Mode |
| SMS | Server Management Software |
| SNMP | Simple Network Management Protocol |
| SSI | Server System Infrastructure |
| TBD | To Be Determined |
| TIM | Thermal Interface Material |
| UART | Universal Asynchronous Receiver/Transmitter |
| UDP | User Datagram Protocol |
| UHCI | Universal Host Controller Interface |
| UTC | Universal time coordinate |
| VID | Voltage Identification |
| VRD | Voltage Regulator Down |
| Word | 16-bit quantity |
| ZIF | Zero Insertion Force |

Reference Documents

Refer to the following documents for additional information:

- *Intel® Server Board S2600WP Technical Product Specification (Intel® Order Code: G31608)*
- *ACPI 3.0*: <http://www.acpi.info/spec.htm>
- *IPMI 2.0*
- *Data Center Management Interface Specification v1.0*, May 1, 2008: www.intel.com/go/dcmi
- *PCI Bus Power Management Interface Specification 1.1*: <http://www.pcisig.com/>
- *PCI Express* Base Specification Rev 2.0 Dec 06*: <http://www.pcisig.com/>
- *PCI Express* Card Electromechanical Specification Rev 2.0*: <http://www.pcisig.com/>
- *PMBus**: <http://pmbus.org>
- *SATA 2.6*: <http://www.sata-io.org/>
- *SMBIOS 2.4*
- *SSI-EEB 3.0*: <http://www.ssiforum.org>
- *USB 1.1*: <http://www.usb.org>
- *USB 2.0*: <http://www.usb.org>
- *Windows Logo/SDG 3.0*
- *Intel® Dynamic Power Technology Node Manager 1.5 External Interface Specification using IPMI, 2007*. Intel Corporation.
- *Node Power and Thermal Management Architecture Specification v1.5, rev.0.79*. 2007, Intel Corporation.
- *Intel® Server System Integrated Baseboard Management Controller Core External Product Specification, 2007*. Intel Corporation.
- *Intel® Thurlay Server Platform Services IPMI Commands Specification, 2007*. Intel Corporation.
- *Intel® Server Safety and Regulatory, 2011*. Intel Corporation. (Intel® Order Code: G23122)
- *Intelligent Platform Management Bus Communications Protocol Specification, Version 1.0, 1998*. Intel Corporation, Hewlett-Packard* Company, NEC* Corporation, Dell* Computer Corporation.
- *Platform Environmental Control Interface (PECI) Specification, Version 2.0*. Intel Corporation.
- *Platform Management FRU Information Storage Definition, Version 1.0, Revision 1.2, 2002*. Intel Corporation, Hewlett-Packard* Company, NEC* Corporation, Dell* Computer Corporation: <http://developer.intel.com/design/servers/ipmi/spec.htm>.