

Intel® Server System R1000BB Product Family

Technical Product Specification

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Enterprise Platforms and Services Division

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April 2012	1.0	1 st Production Release

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1. Introduction

This Technical Product Specification (TPS) provides system level information for the Intel[®] Server System R1000BB product family. It describes the functions and features of the integrated server system which includes the chassis layout, system boards, power sub-system, cooling sub-system, storage sub-system options, and available installable options. Server board specific detail can be obtained by referencing the *Intel[®] Server Board S2400BB Technical Product Specification*.

In addition, design-level information related to specific server board components / subsystems can be obtained by ordering External Product Specifications (EPS) or External Design Specifications (EDS) related to this server generation. EPS and EDS documents are made available under NDA with Intel and must be ordered through your local Intel representative. See the Reference Documents section at the end of this document for a complete list of available documents.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 Introduction
- Chapter 2 Product Family Overview
- Chapter 3 Power Subsystem
- Chapter 4 Thermal Management
- Chapter 5 System Storage and Peripherals Drive Bay Overview
- Chapter 6 Storage Controller Options Overview
- Chapter 7 Front Control Panel and I/O Panel Overview
- Chapter 8 Intel[®] Local Control Panel
- Chapter 9 PCI Riser Card Support
- Chapter 10 Mezzanine Module Support
- Appendix A Integration and Usage Tips
- Appendix B POST Code Diagnostic LED Decoder
- Appendix C Post Code Errors
- Glossary
- Reference Documents

1.2 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel[®] ensures through its own chassis development and testing that when Intel[®] server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel[®]-developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

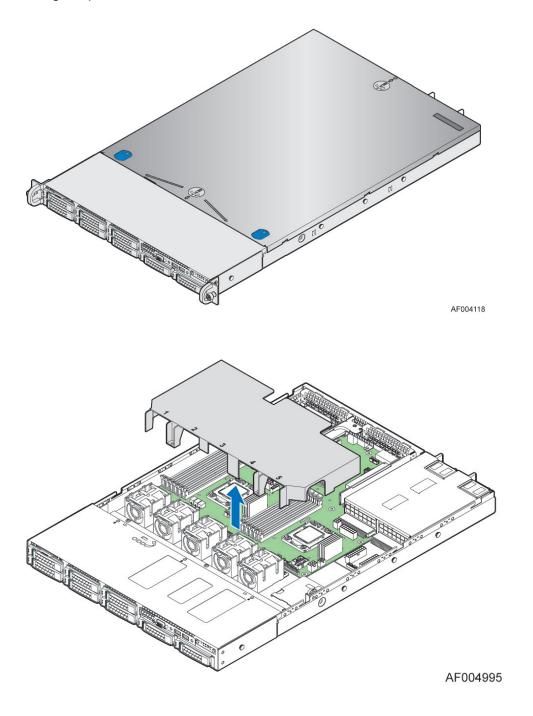
1.3 Product Errata

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Product Errata are documented in the *Intel*[®] *Server Board S2400BB, Intel*[®] *Server System R1000BB, Intel*[®] *Server System R2000BB Monthly Specification Update* which can be downloaded from http://www.intel.com/support.

2. Product Family Overview

This generation of Intel 1U server platforms offers a variety of system options to meet the varied configuration requirements of high-density high-performance computing environments. The Intel® Server System R1000BB product family is comprised of several available 1U rack mount server systems that are all integrated with an Intel® Server Board S2400BB.

This chapter provides a high-level overview of the system features and available options as supported in different platform SKUs within this server family. Greater detail for each major system component or feature is provided in the following chapters.



Intel® Server System R1000BB Product Family TPS

Table 1. System Feature Set

Server System	Integrated Server Board
Intel® Server System R1000BB product family	Intel® Server Board S2400BB

Feature	Description		
Processor Support	 Support for one or two Intel[®] Xeon[®] processors E5-2400 product family with a Thermal Design Power (TDP) of up to 95 Watts. 		
	■ 12 DIMM slots – 2 DIMMs / Channel – 3 memory channels per processor		
	■ Unbuffered DDR3 (UDIMM), registered DDR3 (RDIMM), and Load Reduced DDR3 (LRDIMM)		
Memory	Memory DDR3 data transfer rates of 800, 1066, 1333, and 1600 MT/s		
	■ DDR3 standard I/O voltage of 1.5V and DDR3 Low Voltage of 1.35V		
Chipset	Intel® C602 chipset with support for optional Intel® RAID C600 Upgrade keys		
	■ Video (back and front video connectors)		
External I/O	RJ-45 Serial- A Port		
connections	■ Four RJ-45 Network Interface Connectors supporting 10/100/1000Mb		
	■ USB 2.0 connectors - 3 on back panel + 2 on front panel		
Internal I/O	One Type-A USB 2.0 connector		
connectors / headers	One DH-10 Serial-B port connector		
I/O Module	The following I/O modules utilize a single proprietary on-board connector. An installed I/O module can be supported in addition to standard on-board features and any add-in expansion cards. • Quad port 1 GbE based on Intel® Ethernet Controller I350 – RMS25CB0080		
Accessory Options	 Dual port 10GBase-T Ethernet module based on Intel[®] Ethernet Controller I350 – AXX10GBTWLIOM 		
	■ Dual SFP+ port 10GbE module based on Intel® 82500 10 GbE controller – AXX10GBNIAIOM		
	Single Port FDR speed InfiniBand module with QSFP connector – AXX1FDRIBIOM AXX16 A AX		
	■ Intel® Quick Assist Accelerator Card - AXXQAAIOMOD		
System Fans	Five dual rotor managed system fans		
	One power supply fan for each installed power supply module		
	Support for two PCIe riser cards. Riser cards for Riser #1 and Riser #2 are not the same.		
	Riser Slot #1 (PCle x16): Single add-in card slot – PCle x16 lanes, x16 slot Ricer Slot #2 (PCle x24): Supported ricer cards for this slot include:		
	 Riser Slot #2 (PCle x24): Supported riser cards for this slot include: Single add-in card slot – PCle x8 lanes, x16 slot 		
Riser Cards	0:		
	 Single add-in card slot – PCIe x16 lanes, x16 slot (dual CPU configurations only) Butterfly Riser Card (Accessory Option) -: Two add-in card slots: one PCIe x16 lanes, x16 slot and one PCIe x8 lanes, x8 slot. Note: The PCIe x8 add-in card slot is designed specifically for an Intel® Integrated RAID Module. 		
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	■ Integrated 2D Video Controller		
Video	■ 16 MB DDR3 Memory		
	One eUSB 2x5 pin connector to support 2mm low-profile eUSB solid state devices		
	One mSATA SSD connector		
On-board storage	■ One 7-pin single port AHCI SATA connectors capable of supporting up to 6 Gb/sec		
controllers and	■ Two SCU 4-port mini-SAS connectors capable of supporting up to 3 Gb/sec SAS/SATA		
options	o SCU 0 Port (Enabled standard)		
	o SCU 1 Port (Requires Intel RAID C600 Upgrade Key)		
	■ Intel® RAID C600 Upgrade Key support providing optional expanded SATA / SAS RAID capabilities		
Security	Intel® Trusted Platform Module (TPM) - AXXTPME5 (Accessory Option)		
	■ Integrated Baseboard Management Controller, IPMI 2.0 compliant		
Sonior Managamant	Support for Intel® Server Management Software		
Server Management	■ Intel® Remote Management Module 4 Lite — Accessory option		
	■ Intel [®] Remote Management Module 4 Management NIC – Accessory option		

	■ The server system can have up to two power supply modules installed, providing support for the following power configurations: 1+0, 1+1 Redundant Power, and 2+0 Combined Power	
Power Supply	■ Three power supply options:	
Options	o AC 460W Gold	
	o AC 750W Platinum	
	o DC 750W	
Otana a Day Ontiona	■ 4x – 3.5" SATA/SAS Hot Swap Hard Drive Bays + Optical Drive support	
Storage Bay Options	■ 8x – 2.5" SATA/SAS Hot Swap Hard Drive Bays + Optical Drive support (capable)	
Supported Rack	■ Tool-less rack mount rail kit – Intel Product Code – AXXPRAIL	
Mount Kit Accessory	■ Value rack mount rail kit – Intel Product Code – AXXVRAIL	
Options	■ Cable Management Arm – Intel Product Code – AXX1U2UCMA (*supported with AXXPRAIL only)	
	■ 2-post fixed mount bracket kit – Intel Product Code – AXX2POSTBRCKT	

2.1 Chassis Dimensions

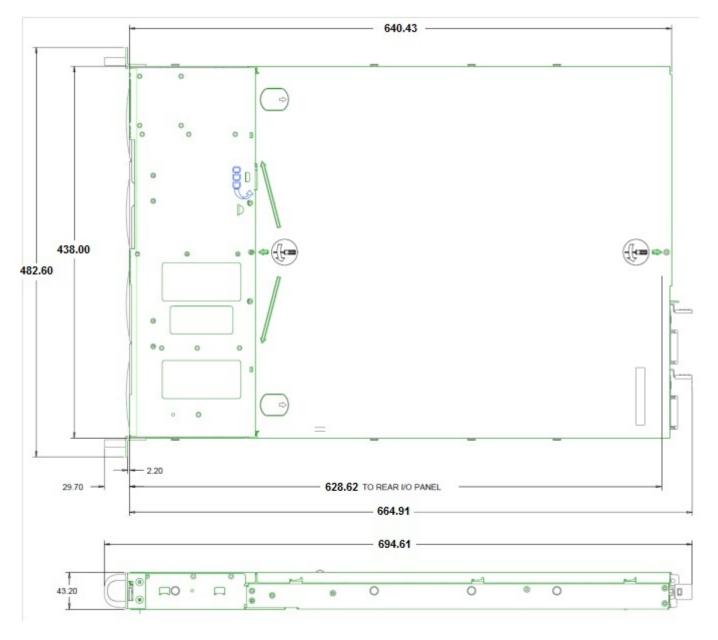


Figure 1. Chassis Dimensions

2.2 System Level Environmental Limits

The following table defines the system level operating and non-operating environmental limits.

Table 2. System Environmental Limits Summary

Parameter		Limits	
Temperature			
	Operating	ASHRAE Class A2 – Continuous Operation. 10° C to 35° C (50° F to 95° F) with the maximum rate of change not to exceed 10°C per hour	
		ASHRAE Class A3 – Includes operation up to 40C for up to 900 hrs per year.	
		ASHRAE Class A4 – Includes operation up to 45C for up to 90 hrs per year.	
	Shipping	-40° C to 70° C (-40° F to 158° F)	
Altitude			
	Operating	Support operation up to 3050m with ASHRAE class deratings.	
Humidity			
	Shipping	50% to 90%, non-condensing with a maximum wet bulb of 28° C (at temperatures from 25° C to 35° C)	
Shock			
	Operating	Half sine, 2g, 11 mSec	
	Unpackaged	Trapezoidal, 25 g, velocity change is based on packaged weight	
	Packaged	Product Weight: ≥ 40 to < 80	
		Non-palletized Free Fall Height = 18 inches	
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		Palletized (single product) Free Fall Height = NA	
Vibration		F.H. tv F00 H 0 00 v DMO v v d v	
	Unpackaged	5 Hz to 500 Hz 2.20 g RMS random	
10.00	Packaged	5 Hz to 500 Hz 1.09 g RMS random	
AC-DC	N/ 1/		
	Voltage	90 Hz to 132 V and 180 V to 264 V	
	Frequency	47 Hz to 63 Hz	
	Source Interrupt	No loss of data for power line drop-out of 12 mSec	
	Surge Non- operating and operating	Unidirectional	
	Line to earth Only	AC Leads 2.0 kV	
		I/O Leads 1.0 kV	
		DC Leads 0.5 kV	
ESD			
	Air Discharged	12.0 kV	
	Contact Discharge	8.0 kV	
Acoustics Sound Power Measured			
	Power in Watts	<300 W ≥300 W ≥600 W ≥1000 W	
	Servers/Rack Mount BA	7.0 7.0 7.0 7.0	

See the *Intel*[®] *S2400BB Product Family Power Budget and Thermal Configuration Tool* for system configuration requirements and limitations.

2.3 System Features and Options Overview

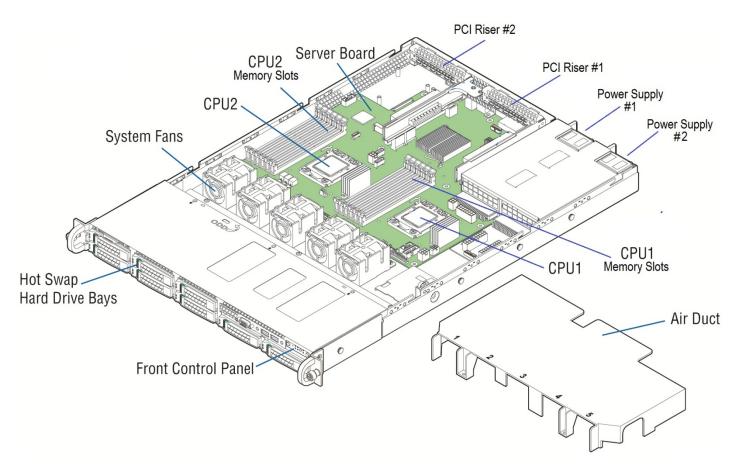


Figure 2. System Components Overview

2.3.1 Hot Swap Hard Drive Bay and Front Panel Options

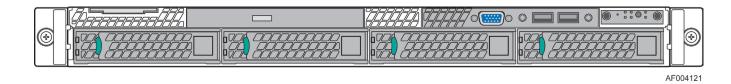


Figure 3. 3.5" Hard Drive Bay - 4 Drive Configuration

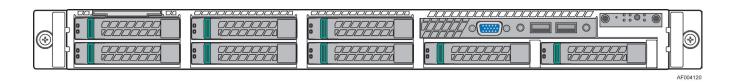


Figure 4. 2.5" Hard Drive Bay - 8 Drive Configuration

2.3.2 Back Panel Features

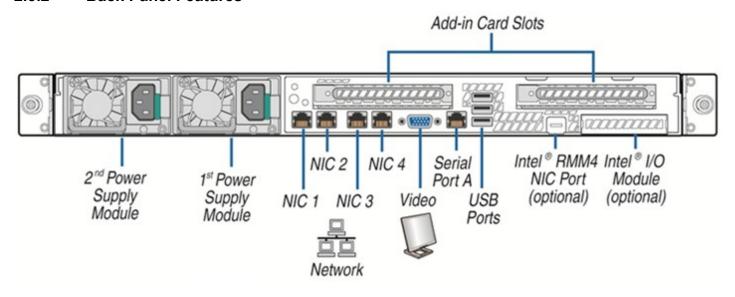
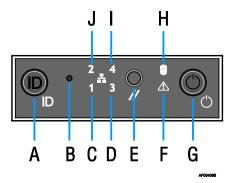


Figure 5. Back Panel Feature Identification

2.3.3 Front Control Panel Options



Label	Description		Description
Α	System ID Button w/Integrated LED		System Status LED
В	NMI Button (recessed, tool required for use)	G	Power Button w/Integrated LED
С	NIC-1 Activity LED	Н	Hard Drive Activity LED
D	NIC-3 Activity LED	I	NIC-4 Activity LED
Е	System Cold Reset Button	J	NIC-2 Activity LED

Figure 6. Front Control Panel Options

2.4 Server Board Features Overview

The following illustration provides a general overview of the server board, identifying key feature and component locations.

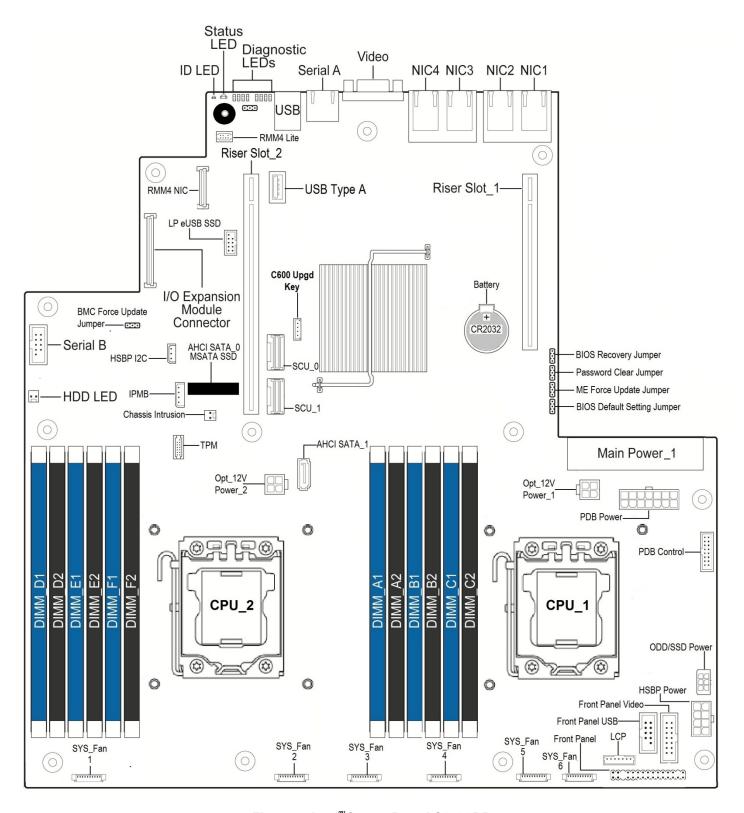


Figure 7. Intel® Server Board S2400BB

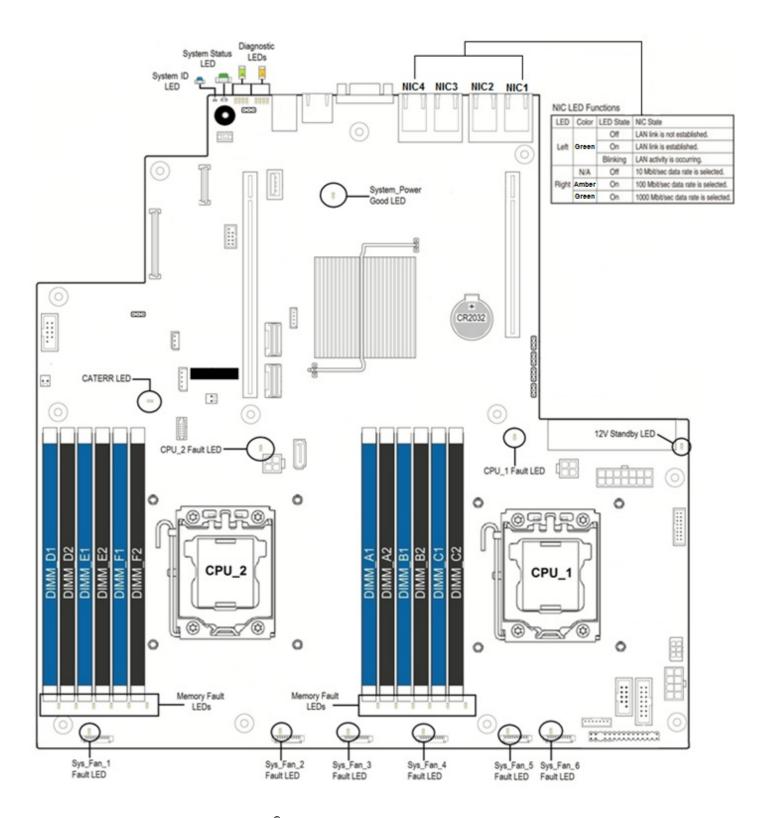


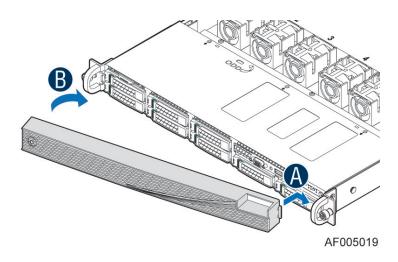
Figure 8. Intel[®] Light-Guided Diagnostic LEDs - Server Board

2.5 Available Front Bezel Support

The optional front bezel is made of molded plastic and uses a snap-on design. When installed, its design allows for maximum airflow to maintain system cooling requirements. The face of the bezel assembly includes optional snap-in identification badge and wave (shown) features to allow for customization. (Intel Product Order Code – A1UBEZEL)



Figure 9. Optional Front Bezel



2.6 Available Rack and Cabinet Mounting Kit Options

- Tool-less rack mount rail kit Intel Product Code AXXPRAIL
 - o 1U and 2U compatible
 - 65 lbs max support weight
 - Tool-less installation
 - Full extension from rack
 - Drop in system install
 - Optional cable management arm support
- Value rack mount rail kit Intel Product Code AXXVRAIL
 - o 1U to 4U compatible
 - o 130 lbs max support weight
 - o Tool-less chassis attach
 - Tools required to attach to rails to rack
 - o 2/3 extension from rack
- Cable Management Arm Intel Product Code AXX1U2UCMA (*supported with AXXPRAIL only)
- 2-Post Fixed mount bracket kit Intel Product Code AXX2POSTBRCKT

3. Power Subsystem

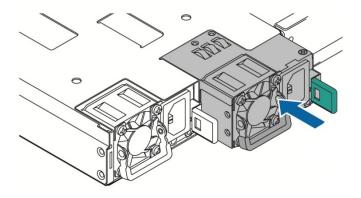
This chapter will provide a high level overview of the power management features and specification data for the power supply options available for this server product. Specification variations will be identified for each supported power supply.

The server system can have upto two power supply modules installed, supporting the following power supply configurations: 1+0 (single power supply), 1+1 Redundant Power, and 2+0 Combined Power (non-redundant). 1+1 redundant power and 2+0 combined power configurations are automatically configured depending on the total power draw of the system. If the total system power draw exceeds the power capacity of a single power supply module, then power from the 2nd power supply module will be utilized. Should this occur, power redundancy is lost. In a 2+0 power configuration, total power available maybe less then twice the rated power of the installed power supply modules due to the amount of heat produced with both supplies providing peak power. Should system thermals exceed programmed limits, platform management will attempt to keep the system operational. See *Closed Loop System Throttling (CLST)* later in this chapter, and Chapter 4 *Thermal Management*, for details.

There are three power supply options available for this server product: 460W AC, 750W AC, 750W DC.

The power supplies are modular, allowing for tool-less insertion and extraction from a bay in the back of the chassis. When inserted, the card edge connector of the power supply mates blindly to a matching slot connector on the server board (PS#1) or Power Distribution Board (PS#2)..

In the event of a power supply failure, redundant 1+1 power supply configurations have support for hot-swap extraction and insertion.



The AC input is auto-ranging and power factor corrected

3.1 Mechanical Overview

The physical size of the power supply enclosure is 39/40mm x 74mm x 185mm. The power supply contains a single 40mm fan. The power supply has a card edge output that interfaces with a 2x25 card edge connector in the system.

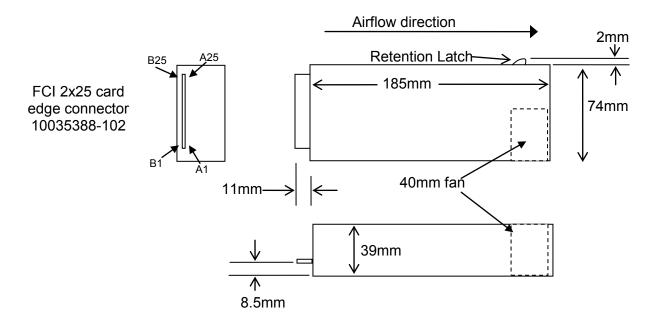


Figure 10. Power Supply Module Mechanical Drawing

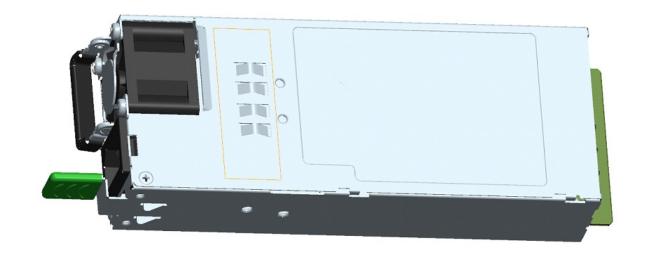


Figure 11. Power Supply Module





Figure 12. AC and DC Power Supplies - Connector View

3.2 Main Power Inter-Connect Layout

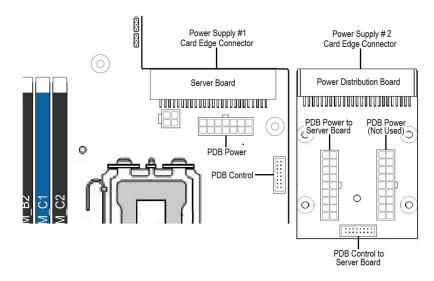


Figure 13. Main Power Connector Identification

3.3 Power Connectors

3.3.1 Power Supply Module Card Edge Connector

Each power supply module has a single 2x25 card edge output connection that plugs directly into a matching slot connector on the server board (PSU#1) and power distribution board (PSU#2). The connector provides both power and communication signals. The following table defines the connector pin-out.

Table 3. Power Supply Module Output Power Connector Pin-out

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	В3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus SDA	B19	A0 (SMBus address)
A20	PMBus SCL	B20	A1 (SMBus address)
A21	PSON	B21	12V stby
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Return Sense	B23	12V load share bus
A24	+12V remote Sense	B24	No Connect
A25	PWOK	B25	Compatibility Check pin*

The server board provides several connectors to provide power to various system options. The following subsections will identify the location; provide the pin-out definition; and provide a brief usage description for each.

3.3.2 Riser Card Power Connectors

The server board includes two white 2x2-pin power connectors that provide supplemental power to high power PCIe x16 add-in cards (GPU) that have power requirements that exceed the 75W maximum power supplied by the PCIe x16 riser slot. A cable from this connector may be routed to a power connector on the given add-in card. Maximum power draw for each connector is 225W, but is also limited by available power provided by the power supply and the total power draw of the rest of the system. A power budget for the complete system should be performed to determine how much supplemental power is available to support any high power add-in cards.

Note: GPU add-in cards cannot be supported in a 1U server system.

Each connector is labeled as "OPT_12V_PWR_1" and "OPT_12V_PWR_2" on the server board. The following table provides the pin-out for both connectors.

Table 4. Riser Slot Power Pin-out ("OPT_12V_PWR_#")

Signal Description	Pin#	Pin#	Signal Description
P12V	3	1	GROUND
P12V	4	2	GROUND

3.3.3 Hot Swap Backplane Power Connector

The server board includes one white 2x4-pin power connector that is cabled to the hot swap backplane. On the server board, this connector is labeled as "HSBP PWR". The following table provides the pin-out for this connector.

Table 5. Hot Swap Backplane Power Connector Pin-out ("HSBP PWR")

Signal Description	Pin#	Pin#	Signal Description
P12V_240VA	5	1	GROUND
P12V_240VA	6	2	GROUND
P12V_240VA	7	3	GROUND
P12V_240VA	8	4	GROUND

3.3.4 Optical Drive Power Connector

The server board includes one brown 2x3-pin power connector intended to provide power to an optionally installed optical drive. On the server board this connector is labeled as "ODD/SSD PWR". The following table provides the pin-out for this connector.

Table 6. Peripheral Drive Power Connector Pin-out ("ODD/SSD PWR")

Signal Description	Pin#	Pin#	Signal Description
P12V	4	1	P5V
P3V3	5	2	P5V
GROUND	6	3	GROUND

3.4 Power Supply Module Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels: 100%, 50% and 20%. Efficiency is tested over an AC input voltage range of 115 VAC to 220 VAC.

Table 7. 460 Watt AC Power Supply Efficiency

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Minimum Efficiency	88%	92%	88%	80%

Table 8. 750 Watt AC Power Supply Efficiency

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Minimum Efficiency	91%	94%	90%	82%

3.5 Power Cord Specification Requirements

Power cords used must meet the specification requirements listed in the following table.

Table 9. AC Power Cord Specifications

Cable Type	SJT
Wire Size	16 AWG
Temperature Rating	105°C
Amperage Rating	13 A
Voltage Rating	125 V

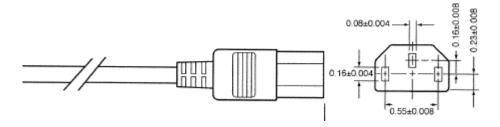


Figure 14. AC Power Cord

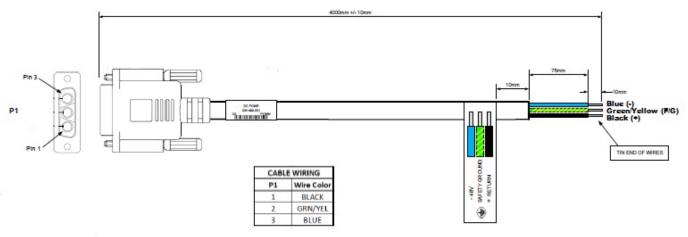


Figure 15. DC Power Cord

3.6 AC Input Requirement

3.6.1 Power Factor

The power supply must meet the power factor requirements stated in the Energy Star[®] Program Requirements for Computer Servers. These requirements are stated below.

Output power	10% load	20% load	50% load	100% load
Power factor	> 0.65	> 0.80	> 0.90	> 0.95

Tested at 230Vac, 50Hz and 60Hz and 115VAC, 60Hz

3.6.2 AC Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC shall not cause damage to the power supply, including a blown fuse.

PARAMETER	MIN	RATED	VMAX	Start up VAC	Power Off VAC
Voltage (110)	90 Vrms	100-127 Vrms	140 Vrms	85VAC +/- 4VAC	70VAC +/- 5VAC
Voltage (220)	180 Vrms	200-240 Vrms	264 Vrms		
Frequency	17 Hz	50/60	63 Hz		

Table 10. AC Input Voltage Range

- 1. Maximum input current at low input voltage range shall be measured at 90VAC, at max load.
- 2. Maximum input current at high input voltage range shall be measured at 180VAC, at max load.
- 3. This requirement is not to be used for determining agency input current markings.

3.6.3 AC Line Isolation Requirements

The power supply shall meet all safety agency requirements for dielectric strength. Transformers' isolation between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage the highest test voltage should be used. In addition the insulation system must comply with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements.

3.6.4 AC Line Dropout / Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the hold up time the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration shall not cause damage to the power supply.

Loading	Holdup time	
70%	12msec	

3.6.4.1 AC Line 12VSBHoldup

The 12VSB output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of **70ms min** (=12VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or deasserted).

3.6.5 AC Line Fuse

The power supply shall have one line fused in the **single line fuse** on the line (Hot) wire of the AC input. The line fusing shall be acceptable for all safety agency requirements. The input fuse shall be a slow blow type. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.6.6 AC Inrush

AC line inrush current shall not exceed **55A peak**, for up to one-quarter of the AC cycle, after which, the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (T_{op}).

3.6.7 AC Line Transient Specification

AC line transient conditions shall be defined as "sag" and "surge" conditions. "Sag" conditions are also commonly referred to as "brownout", these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. "Surge" will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 11. AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)					
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria	
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance	
> 1 AC cycle	>30%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable	

Table 12. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

3.6.8 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter which meets the criteria defined in the SSI document EPS Power Supply Specification. For further information on Intel standards please request a copy of the Intel Environmental Standards Handbook

Table 13. Performance Criteria

Level	Description
Α	The apparatus shall continue to operate as intended. No degradation of performance.
В	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
С	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.6.9 Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria B defined in Annex B of CISPR 24.

3.6.10 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-4: Second edition: 2004-07 test standard and performance criteria B defined in Annex B of CISPR 24.

3.6.11 Radiated Immunity

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-3: Edition 2.1: 2002-09 test standard and performance criteria A defined in Annex B of CISPR 24.

3.6.12 Surge Immunity

The power supply shall be tested with the system for immunity to AC Unidirectional wave; 2kV line to ground and 1kV line to line, per EN 55024: 1998/A1: 2001/A2: 2003, EN 61000-4-5: Edition 1.1:2001-04. The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-5: Edition 1.1:2001-04 test standard and performance criteria B defined in Annex B of CISPR 24.

3.6.13 Power Recovery

The power supply shall recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

3.6.14 Voltage Interruptions

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-11: Second Edition: 2004-03 test standard and performance criteria C defined in Annex B of CISPR 24.

3.6.15 Protection Circuits

Protection circuits inside the power supply cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 seconds and a PSON[#] cycle HIGH for one second reset the power supply.

3.6.16 Over-current Protection (OCP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply shall shutdown and latch off. The latch will be cleared by toggling the PSON[#] signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

Table 14. 460 Watt Power Supply Over Current Protection

Output Voltage	Input voltage range	Over Current Limits
+12V	90 – 264VAC	47A min; 55A max
12VSB	90 – 264VAC	2A min; 2.5A max

Table 15. 750 Watt Power Supply Over Current Protection

Output Voltage	Input voltage range	Over Current Limits
+12V	90 – 264VAC	72A min; 78A max
12VSB	90 – 264VAC	2.5A min; 3.5A max

3.6.17 Over-voltage Protection (OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON[#] signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing OVP limit.

Table 16. Over Voltage Protection (OVP) Limits

Output Voltage	MIN (V)	MAX (V)
+12V	13.3	14.5
+12VSB	13.3	14.5

3.6.18 Over-temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 4°C of ambient temperature margin.

3.7 Cold Redundancy Support

Power supplies that support cold redundancy can be enabled to go into a low-power state (that is, cold redundant state) in order to provide increased power usage efficiency when system loads are such that both power supplies are not needed. When the power subsystem is in Cold Redundant mode, only the needed power supply to support the best power delivery efficiency is ON. Any additional power supplies; including the redundant power supply, is in Cold Standby state

Each power supply has an additional signal that is dedicated to supporting Cold Redundancy; CR_BUS. This signal is a common bus between all power supplies in the system. CR_BUS is asserted when there is a fault in any power supply OR the power supplies output voltage falls below the Vfault threshold. Asserting the CR_BUS signal causes all power supplies in Cold Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level via a PMBus command.

Whenever there is no active power supply on the Cold Redundancy bus driving a HIGH level on the bus all power supplies are ON no matter their defined Cold Redundant roll (active or Cold Standby). This guarantees that incorrect programming of the Cold Redundancy states of the power supply will never cause the power subsystem to shutdown or become over loaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in Cold Redundant Active state or Standard Redundant state to allow the Cold Standby state power supplies to go into Cold Standby state.

3.7.1 Powering on Cold Standby supplies to maintain best efficiency

Power supplies in Cold Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines that power supply to be in the cold standby configuration; will slightly change the load share threshold that the power supply shall power on at.

Table 17. Example Load Share Threshold for Activating Supplies

	Enable Threshold for V _{CR_ON_EN}	Disable Threshold for V _{CR_ON_DIS}	CR_BUS De-asserted / Asserted States
Standard Redundancy	NA; Ignore dc/dc_ active# signal;	power supply is always ON	OK = High Fault = Low
Cold Redundant Active	NA; Ignore dc/dc_ active# signal;	power supply is always ON	OK = High Fault = Low
Cold Standby 1 (02h)	3.2V (40% of max)	3.2V x 0.5 x 0.9 = 1.44V	OK = Open Fault = Low
Cold Standby 2 (03h)	5.0V (62% of max)	5.0V x 0.67 x 0.9 = 3.01V	OK = Open Fault = Low
Cold Standby 3 (04h)	6.7V (84% of max)	6.7V x 0.75 x 0.9 = 4.52V	OK = Open Fault = Low

Notes:

Maximum load share voltage = 8.0V at 100% of rated output power

These are example load share bus thresholds; for a given power supply, these shall be customized to maintain the best efficiency curve for that specific model.

3.7.2 Powering on Cold Standby supplies during a fault or over current condition

When an active power supply asserts its CR_BUS signal (pulling it low), all parallel power supplies in cold standby mode shall power on within 100µsec

3.7.3 BMC Requirements

The BMC uses the Cold_Redundancy_Config command to define/configure the power supply's roll in cold redundancy and to turn on/off cold redundancy.

The BMC shall schedule a rolling change for which PSU is the Active, Cold Stby1, Cold Stby 2, and Cold Stby 3 power supply. This allows for equal loading across power supply over their life.

Events that trigger a re-configuration of the power supplies using the Cold Redundancy Config command.

- AC power ON
- PSON power ON
- Power Supply Failure
- Power supply inserted into system

3.7.4 Power Supply Turn On Function

Powering on and off of the cold standby power supplies is only controlled by each PSU sensing the Vshare bus. Once a power supply turns on after crossing the enable threshold; it lowers its threshold to the disable threshold. The system defines the 'position' of each power supply in the Cold Redundant operation. It will do this each time the system is powered on, a power supply fails, or a power supply is added to the system.

The system is relied upon to tell each power supply where it resides in the Cold Redundancy scheme.

3.8 Closed Loop System Throttling (CLST)

The server system has support for Closed Loop System Throttling (CLST). This feature prevents the system from crashing if a power supply module is overloaded. Should system power reach a pre-programmed power limit, CLST will throttle system memory and/or processors to reduce power. System performance will be impacted should this occur. For more in depth information about CLST implementation, please refer to the SmaRT & CLST Architecture on "Romley" Systems and Power Supplies Specification (IBL Reference # 461024).

3.9 Smart Ride Through Throttling (SmaRT)

The server system has support for Smart Ride Through Throttling (SmaRT). This feature increases the reliability for a system operating in a heavy power load condition, to remain operational during an AC line dropout event. See section 3.5.4 AC Line Dropout / Holdup for power supply hold up time requirements for AC Line dropout events.

When AC voltage is too low, a fast AC loss detection circuit inside each installed power supply asserts an SMBALERT# signal to initiate a throttle condition in the system. System throttling reduces the bandwidth to both system memory and CPUs, which in turn reduces the power load during the AC line drop out event.

3.10 Power Supply Status LED

There is a single bi-color LED to indicate power supply status. The LED operation is defined in the following table.

Table 18. LED Indicators

Power Supply Condition	LED State
Output ON and OK	GREEN
No AC power to all power supplies	OFF
AC present / Only 12VSB on (PS off) or PS in Cold redundant state	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER
Power supply FW updating	2Hz Blink GREEN

4. Thermal Management

The fully integrated system is designed to operate at external ambient temperatures of between 10°C- 35°C with limited excursion based operation up to 45°C, as specified in *Table 3. System Environmental Limits Summary.* Working with integrated platform management, several features within the system are designed to move air in a front to back direction, through the system and over critical components in order to prevent them from overheating and allow the system to operate with best performance.

The Intel® Server System R1000BB product family supports short-term, excursion-based, operation up to 45°C (ASHRAE A4) with limited performance impact. The configuration requirements and limitations are described in the configuration matrix found in the *Intel® S2400BB Product Family Power Budget and Thermal Configuration Tool*, available as a download online at http://www.intel.com/support.

The installation and functionality of several system components are used to maintain system thermals. They include six managed dual rotor 40mm x 56mm system fans, one integrated 40mm fan for each installed power supply module, an air duct, populated hard drive carriers, and installed CPU heats sinks. Hard drive carriers can be populated with a hard drive or supplied drive blank. In addition, it may be necessary to have specific DIMM slots populated with DIMMs or supplied DIMM blanks.

4.1 Thermal Operation and Configuration Requirements

To keep the system operating within supported maximum thermal limits, the system must meet the following operating and configuration guidelines:

- The system operating ambient is designed for sustained operation up to 35°C (ASHRAE Class A2) with short term excursion based operation up to 45°C (ASHRAE Class A4).
 - o The system can operate up to 40°C (ASHRAE Class A3) for up to 900 hours per year
 - The system can operate up to 45°C (ASHRAE Class A4) for up to 90 hours per year
 - When operating within the extended operating temperature range, then system performance may be impacted.
 - There is no long term system reliability impact when operating at the extended temperature range within the approved limits.
- Specific configuration requirements and limitations are documented in the configuration matrix found in the Intel® Server Board S2400BB product family Power Budget and Thermal Configuration Guidelines Tool, available as a download online at Http://www.intel.com/support..
- The CPU-1 processor + CPU heat sink must be installed first. The CPU-2 heat sink must be installed at all times, with or without a processor installed.
- Memory Slot population requirements -
 - NOTE: Specified memory slots can be populated with a DIMM or supplied DIMM Blank. Memory population rules apply when installing DIMMs.
 - DIMM Population Rules on CPU-1 Install DIMMs in order; Channels A, B, and C, Start with1st DIMM (Blue Slot) on each channel, then slot 2. Only remove factory installed DIMM blanks when populating the slot with an actual memory module.
 - DIMM Population Rules on CPU-2 Install DIMMs in order; Channels D, E, and F. Start with1st DIMM (Blue Slot) on each channel, then slot 2. Only remove factory installed DIMM blanks when populating the slot with an actual memory module.
- All hard drive bays must be populated. Hard drive carriers can be populated with a hard drive or supplied drive blank.
- The air duct must be installed at all times
- In single power supply configurations, the 2nd power supply bay must have the supplied filler blank installed at all times.
- The system top-cover must be installed at all times

4.2 Thermal Management Overview

In order to maintain the necessary airflow within the system, all of the previously listed components and top cover need to be properly installed. For best system performance, the external ambient temperature should remain below 35°C and all system fans should be operational. The system is designed for fan redundancy when the system is configured with two power supplies. Should a single system fan fail (System fan or Power Supply Fan), integrated platform management will: change the state of the System Status LED to flashing Green, report an error to the system event log, and automatically adjust fan speeds as needed to maintain system temperatures below maximum thermal limits.

Note: All system fans are controlled independent of each other. The fan control system may adjust fan speeds for different fans based on increasing/decreasing temperatures in different thermal zones within the chassis.

In the event that system thermals should continue to increase with the system fans operating at their maximum speed, platform management may begin to throttle bandwidth of either the memory subsystem or the processors or both, in order to keep components from overheating and keep the system operational. Throttling of these sub-systems will continue until system thermals are reduced below preprogrammed limits.

Should system temperatures increase to a point beyond the maximum thermal limits, the system will shut down, the System Status LED will change to a solid Amber state, and the event will be logged to the system event log.

<u>Note:</u> Sensor data records (SDRs) for any given system configuration must be loaded by the system integrator for proper thermal management of the system. SDRs are loaded using the FRUSDR utility.

An intelligent Fan Speed Control (FSC) and thermal management technology (mechanism) is used to maintain comprehensive thermal protection, deliver the best system acoustics, and fan power efficiency. Options in <F2> BIOS Setup (BIOS>Advanced>System Acoustic and Performance Configuration) allow for parameter adjustments based on the actual system configuration and usage. Refer to the following sections for a description of each setting.

4.2.1 Set Throttling Mode

This option is used to select the desired memory thermal throttling mechanism. Available settings include: **[Auto]**, [DCLTT], [SCLTT] and [SOLTT].

[Auto] – Factory Default Setting - BIOS automatically detects and identifies the appropriate thermal throttling mechanism based on DIMM type, airflow input, and DIMM sensor availability.

[DCLTT] – Dynamic Closed Loop Thermal Throttling: for the SOD DIMM with system airflow input

[SCLTT] – Static Close Loop Thermal Throttling: for the SOD DIMM without system airflow input

[SOLTT] – Static Open Loop Thermal Throttling: for the DIMMs without sensor on dimm (SOD)

4.2.2 Altitude

This option is used to select the proper altitude that the system will be used in. Available settings include: [300m or less], **[301m-900m]**, [901m-1500m], [Above 1500m].

Selecting an altitude range that is lower than the actual altitude the system will be operating at, can cause the fan control system to operate less efficiently, leading to higher system thermals and lower system performance. If the altitude range selected is higher than the actual altitude the system will be operating at, the fan control system may provide better cooling but with higher acoustics and higher fan power consumption. If the altitude is not known, selecting a higher altitude is recommended in order to provide sufficient cooling

4.2.3 Set Fan Profile

This option is used to set the desired Fan Profile. Available settings include: **[Performance]** and [Acoustic].

The Acoustic mode offers the best acoustic experience and appropriate cooling capability supporting the majority of the add-in cards used. Performance mode is designed to provide sufficient cooling capability covering all kinds of add-in cards on the market.

4.2.4 Fan PWM Offset

This option is reserved for manual adjustment to the minimum fan speed curves. The valid range is from [0 to 100] which stands for 0% to 100% PWM adding to the minimum fan speed. This feature is valid when Quiet Fan Idle Mode is at Enabled state. The default setting is [0]

4.2.5 Quiet Fan Idle Mode

This feature can be [Enabled] or **[Disabled]**. If enabled, the fans will either shift to a lower speed or stop when the aggregate sensor temperatures are satisfied, indicating the system is at ideal thermal/light loading conditions. When the aggregate sensor temperatures are not satisfied, the fans will shift back to normal control curves. If disabled, the fans will never shift into lower fan speeds or stop, regardless of whether the aggregate sensor temperatures are satisfied or not. The default setting is [Disabled]

Note: The above feature may or may not be in effect and depends on the actual thermal characteristics of the specified system.

4.2.6 Thermal Sensor Input for Fan Speed Control

The BMC uses various IPMI sensors as inputs to fan speed control. Some of the sensors are actual physical sensors and some are "virtual" sensors derived from calculations.

The following IPMI thermal sensors are used as input to fan speed control:

- Front Panel Temperature Sensor¹
- CPU Margin Sensors^{2,4,5}
- DIMM Thermal Margin Sensors^{2,4}
- Exit Air Temperature Sensor^{1, 7, 9}
- PCH Temperature Sensor^{3,5}
- On-board Ethernet Controller Temperature Sensors^{3, 5}
- Add-In Intel SAS/IO Module Temperature Sensors^{3, 5}
- PSU Thermal Sensor^{3, 8}
- CPU VR Temperature Sensors^{3, 6}
- DIMM VR Temperature Sensors^{3, 6}
- BMC Temperature Sensor^{3, 6}
- Global Aggregate Thermal Margin Sensors ¹
- Hot Swap Backplane Temperature Sensors
- I/O module Temperature Sensor (With option installed)
- Intel[®] ROC Module (With option installed)

Notes:

- 1. For fan speed control in Intel chassis
- 2. Temperature margin from throttling threshold
- 3. Absolute temperature
- 4. PECI value or margin value
- 5. On-die sensor
- 6. On-board sensor
- 7. Virtual sensor
- 8. Available only when PSU has PMBus
- 9. Calculated estimate

The following diagram illustrates the fan speed control structure

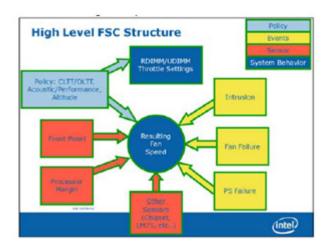


Figure 16. Fan Control Model

4.3 System Fans

Five managed dual rotor 40mm x 56mm system fans and an embedded fan for each installed power supply, provide the primary airflow for the system. The system is designed for fan redundancy when configured with two power supply modules. Should a single fan fail (system fan or power supply fan), platform management will adjust air flow of the remaining fans and manage other platform features to maintain system thermals. Fan redundancy is lost if more than one fan is in a failed state

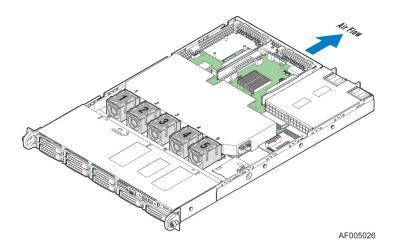
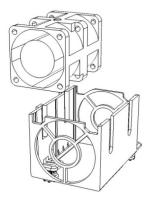


Figure 17. System Fan Identification

Each system fan is mounted inside its own plastic fan housing which include rotational vibration dampening features. The fan assemblies are held in place by fitting them over mounting pins coming up from the chassis base.



The system fan assembly is designed for ease of use and supports several features.

- System fans are NOT hot-swappable.
- Each fan and fan assembly is designed for tool-less insertion and extraction from the system. For instructions on fan replacement, see the *Intel*[®] *Server System R1000BB Service Guide*.
- Fan speed for each fan is controlled by integrated platform management as controlled by the integrated BMC on the server board. As system thermals fluctuate high and low, the integrated BMC firmware will increase and decrease the speeds to specific fans to regulate system thermals.
- Each fan has a tachometer signal that allows the integrated BMC to monitor its status.
- Each fan has a10-pin wire harness that connects to a matching connector on the server board.

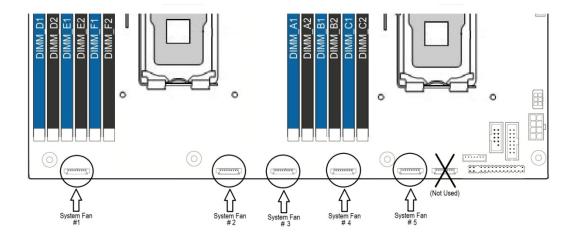


Figure 18. Server Board System Fan Connector Locations

Table 19. System Fan Connector Pin-out

SYS_FAN 1		SYS_FAN 2		SYS_FAN 3	
Signal Description Pin#		Signal Description	Pin#	Signal Description	Pin#
FAN_TACH1_IN	1	FAN_TACH3_IN	1	FAN_TACH5_IN	1
FAN_IBMC_PWM0_R_BUF	2	FAN_IBMC_PWM1_R_BUF	2	FAN_IBMC_PWM2_R_BUF	2
P12V_FAN	3	P12V_FAN	3	P12V_FAN	3
P12V_FAN	4	P12V_FAN	4	P12V_FAN	4
FAN_TACH0_IN	5	FAN_TACH2_IN	5	FAN_TACH4_IN	5
GROUND	6	GROUND	6	GROUND	6
GROUND	7	GROUND	7	GROUND	7
FAN_SYS0_PRSNT_N	8	FAN_SYS1_PRSNT_N	8	FAN_SYS2_PRSNT_N	8
LED_FAN_FAULT0_R	9	LED_FAN_FAULT1_R	9	LED_FAN_FAULT2_R	9
LED_FAN0	10	LED_FAN1	10	LED_FAN2	10
SYS_FAN 4				SYS_Fan 6 (not used)	
SYS_FAN 4		SYS_FAN 5		SYS_Fan 6 (not used	(k
SYS_FAN 4 Signal Description	Pin#	SYS_FAN 5 Signal Description	Pin#	SYS_Fan 6 (not used Signal Description	d) Pin#
	Pin#	_	Pin#		-
Signal Description		Signal Description		Signal Description	Pin#
Signal Description FAN_TACH7_IN	1	Signal Description FAN_TACH9_IN	1	Signal Description FAN_TACH11_IN	Pin#
Signal Description FAN_TACH7_IN FAN_IBMC_PWM3_R_BUF	1 2	Signal Description FAN_TACH9_IN FAN_IBMC_PWM4_R_BUF	1 2	Signal Description FAN_TACH11_IN FAN_IBMC_PWM5_R_BUF	Pin# 1 2
Signal Description FAN_TACH7_IN FAN_IBMC_PWM3_R_BUF P12V_FAN	1 2 3	Signal Description FAN_TACH9_IN FAN_IBMC_PWM4_R_BUF P12V_FAN	1 2 3	Signal Description FAN_TACH11_IN FAN_IBMC_PWM5_R_BUF P12V_FAN	Pin# 1 2 3
Signal Description FAN_TACH7_IN FAN_IBMC_PWM3_R_BUF P12V_FAN P12V_FAN	1 2 3 4	Signal Description FAN_TACH9_IN FAN_IBMC_PWM4_R_BUF P12V_FAN P12V_FAN	1 2 3 4	Signal Description FAN_TACH11_IN FAN_IBMC_PWM5_R_BUF P12V_FAN P12V_FAN	Pin# 1 2 3 4
Signal Description FAN_TACH7_IN FAN_IBMC_PWM3_R_BUF P12V_FAN P12V_FAN FAN_TACH6_IN	1 2 3 4 5	Signal Description FAN_TACH9_IN FAN_IBMC_PWM4_R_BUF P12V_FAN P12V_FAN FAN_TACH8_IN	1 2 3 4 5	Signal Description FAN_TACH11_IN FAN_IBMC_PWM5_R_BUF P12V_FAN P12V_FAN FAN_TACH10_IN	Pin# 1 2 3 4 5
Signal Description FAN_TACH7_IN FAN_IBMC_PWM3_R_BUF P12V_FAN P12V_FAN FAN_TACH6_IN GROUND	1 2 3 4 5 6	Signal Description FAN_TACH9_IN FAN_IBMC_PWM4_R_BUF P12V_FAN P12V_FAN FAN_TACH8_IN GROUND	1 2 3 4 5 6	Signal Description FAN_TACH11_IN FAN_IBMC_PWM5_R_BUF P12V_FAN P12V_FAN FAN_TACH10_IN GROUND	Pin# 1 2 3 4 5 6
Signal Description FAN_TACH7_IN FAN_IBMC_PWM3_R_BUF P12V_FAN P12V_FAN FAN_TACH6_IN GROUND GROUND	1 2 3 4 5 6 7	Signal Description FAN_TACH9_IN FAN_IBMC_PWM4_R_BUF P12V_FAN P12V_FAN FAN_TACH8_IN GROUND GROUND	1 2 3 4 5 6 7	Signal Description FAN_TACH11_IN FAN_IBMC_PWM5_R_BUF P12V_FAN P12V_FAN FAN_TACH10_IN GROUND GROUND	Pin# 1 2 3 4 5 6 7

4.4 Power Supply Fans

Each installed power supply module includes one embedded (non-removable) 40-mm fan. It is responsible for airflow through the power supply module. This fan is managed by the fan control system. Should this fan fail, the power supply will continue to operate until its internal temperature reaches an upper critical limit. The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an over-temperature protection condition, the power supply module will shutdown.

4.5 FRUSDR Utility

The purpose of the embedded platform management and fan control systems is to monitor and control various system features, and to maintain an efficient operating environment. Platform management is also used to communicate system health to supported platform management software and support mechanisms. The FRUSDR utility is used to program the server board with platform specific environmental limits, configuration data, and the appropriate sensor data records (SDRs), for use by these management features.

The FRUSDR utility must be run as part of the initial platform integration process before it is deployed into a live operating environment. It must be run with the system fully configured and each time the system configuration changes.

The FRUSDR utility for the given server platform can be run as part of the *Intel*[®] *Server Deployment Toolkit* and *Management* DVD that ships with each Intel server, or can be downloaded from http://www.intel.com/support.

Note: The embedded platform management system may not operate as expected if the platform is not updated with accurate system configuration data. The FRUSDR utility must be run with the system fully configured and each time the system configuration changes for accurate system monitoring and event reporting.

5. System Storage and Peripheral Options

The Intel® Server System R1000BB product family has support for many storage device options, including:

- Hot Swap 2.5" Hard Disk Drives
- Hot Swap 3.5" Hard Disk Drives
- SATA Optical Drive
- Low Profile (2mm) eUSB Solid State Device (eUSB SSD)
- mSATA Solid State Device

Support for different storage and peripheral device options will vary depending on the system SKU. This section will provide an overview of each available option.

5.1 2.5" Hard Disk Drive Support

The server is available with support for eight 2.5" hard disk drives as illustrated below.

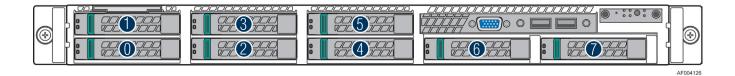
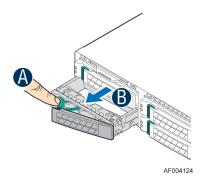


Figure 19. 2.5" Hard Drive Bay Drive Configuration

The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 2.5" hard disk drive is mounted to a drive carrier, allowing for hot swap extraction and insertion. Drive carriers have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.



Light pipes integrated into the drive tray assembly direct light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.

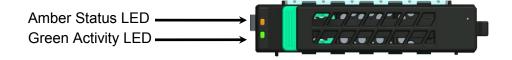


Table 20. Drive Status LED States

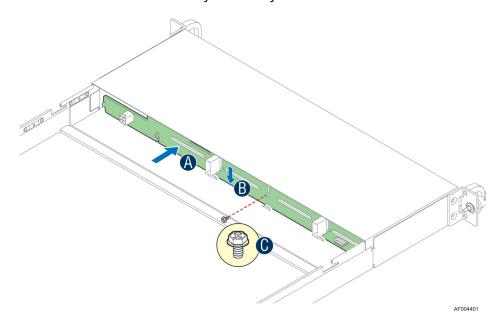
	Off	No access and no fault			
Amber	Solid On	Hard Drive Fault has occured			
	Blink	RAID rebuild in progress (1 Hz), Identify (2 Hz)			

Table 21. Drive Activity LED States

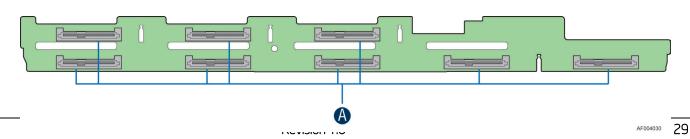
	Condition	Drive Type	Behavior
	Power on with no drive activity	SAS	LED stays on
	Power on with no drive activity	SATA	LED stays off
	Davida an with drive activity	SAS	LED blinks off when processing a command
Green	Power on with drive activity	SATA	LED blinks on when processing a command
	Power on and drive spun down Power on and drive spinning up	SAS	LED stays off
		SATA	LED stays off
		SAS	LED blinks
	i ower on and drive spiriting up	SATA	LED stays off

5.1.1 2.5" Drive Hot-Swap Backplane Overview

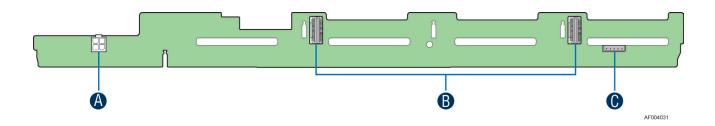
A backplane is attached to the back of the drive bay assembly.



On the front side of each backplane are mounted eight hard disk drive interface connectors (A), each providing both power and I/O signals to attached hard disk drives.



On the backside of each backplane are several connectors. The following illustration identifies each.



Label	Description
Α	Power connector
В	4-port Mini-SAS cable connectors
С	SMBus-In cable connector – From Server board

A – Power Harness Connector – The backplane includes a 2x2 connector supplying power to the backplane. Power is routed to the backplane via a power cable harness from the server board.

B – Multi-port Mini-SAS Cable Connectors – The backplane includes two multi-port mini-SAS cable connectors, each providing I/O signals for four SAS/SATA hard drives on the backplane. Cables can be routed from matching connectors on the server board, add-in SAS/SATA RAID cards, or optionally installed SAS expander cards.

C – SMBus Cable Connectors – The backplane includes a 1x5 cable connector used as a management interface to the server board.

5.1.2 Cypress* CY8C22545 Enclosure Management Controller

The backplane supports enclosure management using a Cypress* CY8C22545 Programmable System-on-Chip (PSoC*) device. The CY8C22545 drives the hard drive activity/fault LED, hard drive present signal, and controls hard drive power-up during system power-on.

5.2 3.5" Hard Disk Drive Support

The server is available with support for four 3.5" hard disk drives as illustrated below.

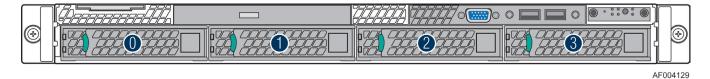
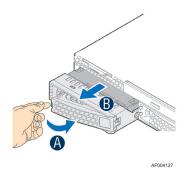
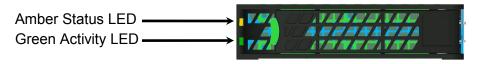


Figure 20. 3.5" Hard Drive Bay Configuration

The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 3.5" hard disk drive is mounted to a drive tray, allowing for hot swap extraction and insertion. Drive trays have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.



Light pipes integrated into the drive tray assembly direct light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.

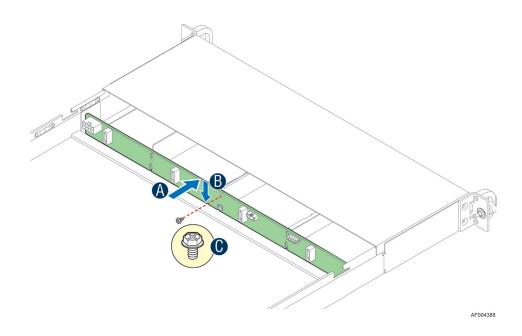


		Off	No access and no fault
Am	ber	Solid On	Hard Drive Fault has occured
		Blink	RAID rebuild in progress (1 Hz), Identify (2 Hz)

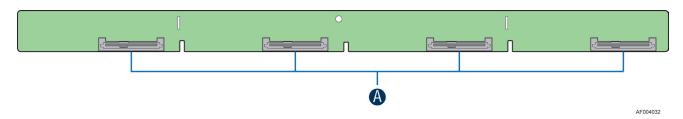
	Condition	Drive Type	Behavior
	Power on with no drive activity	SAS	LED stays on
	Fower on with no drive activity	SATA	LED stays off
	Power on with drive activity	SAS	LED blinks off when processing a command
Green	Power on with drive activity	SATA	LED blinks on when processing a command
	Dower on and drive only down	SAS	LED stays off
	Power on and drive spun down	SATA	LED stays off
	Power on and drive spinning up	SAS	LED blinks
	Power on and drive spiriting up	SATA	LED stays off

5.2.1 3.5" Drive Hot-Swap Backplane Overview

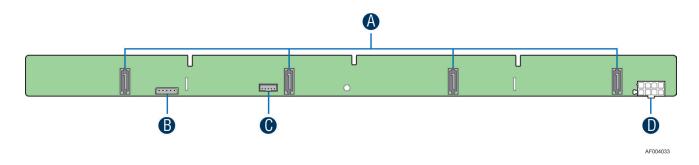
The backplane mounts to the back of the drive bay assembly.



On the front side of each back plane are mounted four hard disk drive interface connectors (A), each providing both power and I/O signals to attached hard disk drives.



On the backside of each backplane are several connectors. The following illustration identifies each.



Label	Description
Α	7-pin SATA/SAS I/O connectors
В	SMBus-In cable connector – From Server board
С	SGPIO connector
D	Power connector

- A 7-pin SATA I/O Connectors The backplane has four 7-pin SATA/SAS I/O connectors, one for each hard drive. A single multi-connector cable is routed from the backplane to a four port mini-SAS connector on the server board or other optionally installed SATA/SAS host bus adapter.
- B -. SMBus Cable Connectors The backplane includes a 1x5 cable connector used as a management interface to the server board
- C-. SGPIO Cable Connector The SGPIO connector is a management interface used to control the hard drive fault LEDs on the backplane. The SGPIO signals are routed through a multi-connectors cable that is routed to a four port mini-SAS connector on the server board or other optionally installed SATA/SAS host bus adapter.
- **D** Power Harness Connector The backplane includes a 2x2 connector supplying power to the backplane. Power is routed to the backplane via a power cable harness from the server board

5.2.2 Cypress* CY8C22545 Enclosure Management Controller

The backplanes support enclosure management using a Cypress* CY8C22545 Programmable System-on-Chip (PSoC*) device. The CY8C22545 drives the hard drive activity/fault LED, hard drive present signal, and controls hard drive power-up during system power-on.

5.3 **Optical Drive Support**

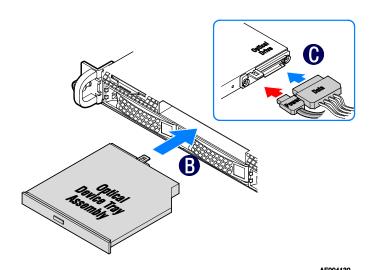
Systems configured with four 3.5" hard drive bays also include a designated drive bay 'A' to support a SATA optical drive as illustrated below.



Figure 21. Optical Drive Support

For systems that support eight 2.5" hard drives, the front I/O Panel, which provides video and USB ports, can be replaced with a SATA optical drive.

A 2x3 pin power connector on the server board labeled "ODD/SSD PWR", is designed to provide power to the optical drive. SATA signals for the optical drive are cabled from the white 7-pin single port SATA connector on the server board.



5.4 eUSB SSD Support

The system provides support for a low profile eUSB SSD storage device. A 2mm 2x5-pin connector labeled "eUSB SSD" near the rear I/O section of the server board is used to plug this small flash storage device into.

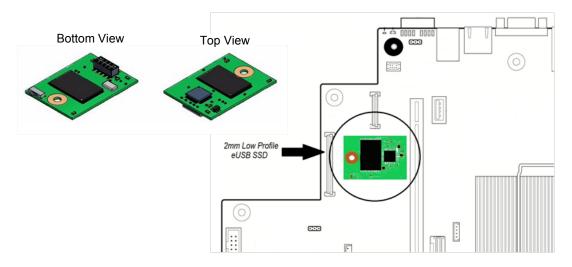


Figure 22. Low Profile eUSB SSD Support

eUSB features include:

- 2 wire small form factor Universal Serial Bus 2.0 (Hi-Speed USB) interface to host
- Read Speed up to 35 MB/s and write Speed up to 24 MB/s
- Capacity range from 32 GB to 256GB
- Support USB Mass Storage Class requirements for Boot capability

5.5 SATA DOM Support

The system has support for a vertical low profile Innodisk* SATA Disk-on-Module (DOM) device. The SATA DOM plugs directly into the 7-pin AHCI SATA port on the server board, which provides both power and I/O signals.



Figure 23. InnoDisk* Low Profile SATA DOM

SATA DOM features include:

- Ultra Low Profile
- High speed and capacity
- Built-in VCC at pin 7

Note: Visit Http://www.intel.com/support. for a list of supported InnoDisk SATA DOM parts

5.6 mSATA SSD Support

The system provides support for a mSATA SSD storage device.

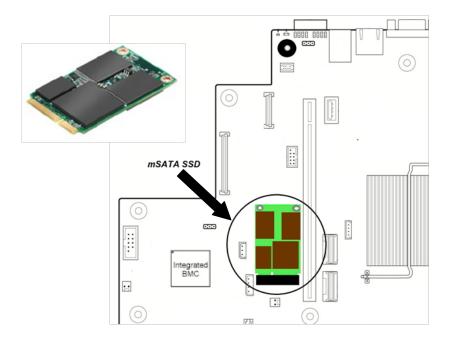


Figure 24. mSATA Placement

The mSATA storage device plugs in to a 52-pin PCle mini-connector on the server labeled "mSATA SSD". mSATA SSD features include:

- Capacities ranging from 40GB to 128GB
- Small foot print
- Low power

6. Storage Controller Options Overview

The server platform supports many different embedded and add-in SATA/SAS controller and SAS Expander options to provide a large number of possible storage configurations. This section will provide an overview of the different options available.

6.1 Embedded SATA / SAS Controller support

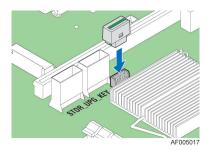
Integrated on the server board is an Intel[®] C602 chipset that provides embedded storage support via two integrated controllers: AHCI and SCU.

The standard server board (with no additional storage options installed) will support up to six SATA ports:

- One 6 Gb/sec SATA port routed from the AHCI controller to a white 7-pin SATA port labeled "SATA-1" on the server board.
- One 6 Gb/sec SATA port routed from the AHCI controller to the mSATA connector
- Four 3 Gb/sec SATA ports routed from the SCU controller to the multi-port mini-SAS connector labeled "SCU_0".

Note: The mini-SAS connector labeled "SCU_1" is NOT functional by default and is only enabled with the addition of an Intel[®] RAID C600 Upgrade Key option supporting 8 SAS/SATA ports.

With the addition of one of several available Intel[®] RAID C600 Upgrade Keys, the system is capable of supporting additional embedded SATA, SAS, and software RAID options. Upgrade keys install onto a 4-pin connector on the server board labeled "STOR UPG KEY".



The following table identifies available upgrade key options and their supported features.

Table 22. Intel® RAID C600 Upgrade Key Options

Intel® RAID C600 Upgrade Key (Intel Product Codes)	Key Color	Description
Default – No option key installed	N/A	4 Port SATA with Intel® ESRT RAID 0,1,10 and Intel® RSTe RAID 0,1,5,10
RKSATA4R5	Black	4 Port SATA with Intel® ESRT2 RAID 0,1, 5, 10 and Intel® RSTe RAID 0,1,5,10
RKSATA8	Blue	8 Port SATA with Intel® ESRT2 RAID 0,1, 10 and Intel® RSTe RAID 0,1,5,10
RKSATA8R5	White	8 Port SATA with Intel® ESRT2 RAID 0,1, 5, 10 and Intel® RSTe RAID 0,1,5,10
RKSAS4	Green	4 Port SAS with Intel® ESRT2 RAID 0,1, 10 and Intel® RSTe RAID 0,1,10
RKSAS4R5	Yellow	4 Port SAS with Intel® ESRT2 RAID 0,1, 5, 10 and Intel® RSTe RAID 0,1,10
RKSAS8	Orange	8 Port SAS with Intel® ESRT2 RAID 0,1, 10 and Intel® RSTe RAID 0,1,10
RKSAS8R5	Purple	8 Port SAS with Intel® ESRT2 RAID 0,1, 5, 10 and Intel® RSTe RAID 0,1,10

Additional information for the on-board RAID features and functionality can be found in the *Intel*[®] *RAID Software Users Guide* (Intel Document Number D29305-015).

6.2 Embedded Software RAID Support

The system includes support for two embedded software RAID options:

- Intel[®] Embedded Server RAID Technology 2 (ESRT2) based on LSI* MegaRAID SW RAID technology
- Intel[®] Rapid Storage Technology (RSTe)

Using the <F2> BIOS Setup Utility, accessed during system POST, options are available to enable/disable SW RAID, and select which embedded software RAID option to use.

6.2.1 Intel® Embedded Server RAID Technology 2 (ESRT2)¹

Features of the embedded software RAID option Intel[®] Embedded Server RAID Technology 2 (ESRT2) include the following:

- Based on LSI* MegaRAID Software Stack
- Software RAID, with system providing memory and CPU utilization
- Supported RAID Levels 0,1,5,10
 - 4 & 8 Port SATA RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key
 - o 4 & 8 Port SAS RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key
- Maximum drive support = 8
 - o NOTE: ESRT2 has no SAS Expander Support
- Open Source Compliance = Binary Driver (includes Partial Source files)
 - Meta data is also recognized by MDRAID layer in Linux (No direct Intel support, not validated by Intel)
- OS Support = Windows 7*, Windows 2008*, Windows 2003*, RHEL*, SLES*, other Linux variants using partial source builds.
- Utilities = Windows* GUI and CLI, Linux GUI and CLI, DOS CLI, and EFI CLI

6.2.2 Intel® Rapid Storage Technology (RSTe)¹

Features of the embedded software RAID option Intel® Rapid Storage Technology (RSTe) include the following:

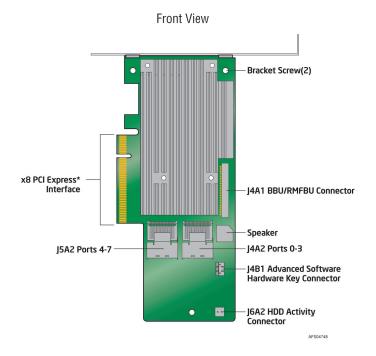
- Software RAID with system providing memory and CPU utilization
- Supported RAID Levels 0.1.5.10
 - 4 Port SATA RAID 5 available standard (no option key required)
 - o 8 Port SATA RAID 5 support provided with appropriate Intel® RAID C600 Upgrade Key
 - No SAS RAID 5 support
- Maximum drive support = 32 (in arrays with 8 port SAS), 16 (in arrays with 4 port SAS), 128 (JBOD)
- Open Source Compliance = Yes (uses MDRAID)
- OS Support = Windows 7*, Windows 2008*, Windows 2003*, RHEL* 1 and later, SLES*1, VMWare 5.x.
- Utilities = Windows* GUI and CLI, Linux CLI, DOS CLI, and EFI CLI
- NOTE: No boot drive support to targets attached through SAS expander card

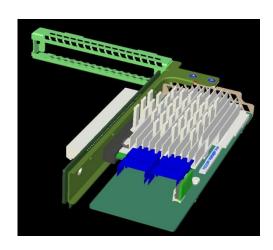
Note 1) See latest product errata list for support status. Product Errata are documented in the *Intel*[®] *Server Board S2400BB, Intel*[®] *Server System R1000BB, Intel*[®] *Server System R2000BBL Monthly Specification Update* which can be downloaded from http://www.intel.com/support.

Visit http://www.intel.com/support for a list of supported operating systems.

6.3 Intel® Integrated RAID Module Support (Available Option)

The system has support for several Intel[®] Integrated RAID adapters. The RAID card can be installed into any available x8 PCIe add-in slot. If the system is configured with the optional Butterfly riser card, the RAID adapter can be installed in the x8 PCIe add-in slot on the back side of the riser card, as shown in the following illustration. This option allows for up to three PCIe add-in cards to be installed in the system.





Features of this option include:

- SKU options to support full or entry level hardware RAID
- 4 or 8 port and SAS/SATA or SATA –only ROC options
- SKU options to support 512MB or 1GB embedded memory
- Intel designed flash + optional support for super-cap backup (Maintenance Free Back Up) or improved Lithium Polymer battery

Table 23. Supported Intel® Integrated RAID Modules

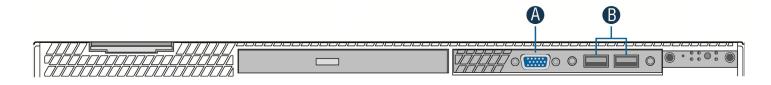
External Name	Description	Product Code
Intel [®] Integrated RAID Module RMS25PB080	8P SAS-2.1, Full HW RAID, 1GB, PCIe	RMS25PB080
Intel [®] Integrated RAID Module RMS25PB040	4P SAS-2.1, Full HW RAID, 1GB, PCIe	RMS25PB040
Intel [®] Integrated RAID Module RMT3PB080	8P SATA-3, Full HW RAID, 512MB, PCIe	RMT3PB080
Intel [®] Integrated RAID Module RMS25KB080	8P SAS-2.1, Entry-level HW RAID, PCIe	RMS25KB080
Intel [®] Integrated RAID Module RMS25KB040	4P SAS-2.1, Entry-level HW RAID, PCIe	RMS25KB040

For additional product information, please reference the following Intel document: Intel Integrated RAID Module RMS25PB080, RMS25PB040, RMS25CB080, and RMS25CB040 Hardware Users Guide – Intel Order Number G37519-001

7. Front Control Panel and I/O Panel Overview

On the front panel of all system configurations is a Control Panel providing push button system controls and LED indicators for several system features, and an I/O Panel providing USB ports and a video connector. This section describes the features and functions of both front panel options.

7.1 I/O Panel Features



Label	Description
Α	Video connector
В	USB ports

Figure 25. Front I/O Panel Features

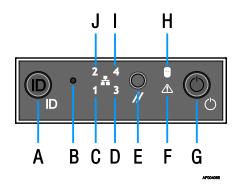
A – Video connector – The front I/O Panel video connector gives the option of attaching a monitor to the front of the system. When BIOS detects that a monitor is attached to the front video connector, it disables the video signals routed to the on-board video connector on the back of the system. Video resolutions from the front video connector may be lower than that of the rear on-board video connector. A short video cable should be used for best resolution. The front video connector is cabled to a 2x7 header on the server board labeled "FP Video".

B – USB Ports – The front I/O panel includes two USB ports. The USB ports are cabled to a 2x5 connector on the server board labeled "FP USB".

Note – On systems that support 8x2.5" hard drives, the I/O Panel can be replaced with a SATA optical drive.

7.2 Control Panel Features

The system includes a control panel that provides push button system controls and LED indicators for several system features. Depending on the hard drive configuration, the front control panel may come in either of two formats; however, both provide the same functionality. This section will provide a description for each front control panel feature.



Label	Description		Description
Α	System ID Button w/Integrated LED		System Status LED
В	NMI Button (recessed, tool required for use)		Power / Sleep Button w/Integrated LED
С	NIC-1 Activity LED	Н	Hard Drive Activity LED
D	NIC-3 Activity LED	I	NIC-4 Activity LED
Е	System Cold Reset Button		NIC-2 Activity LED

Figure 26. Front Control Panel Features

- **A System ID Button w/Integrated LED** Toggles the integrated ID LED and the Blue server board ID LED on and off. The System ID LED is used to identify the system for maintenance when installed in a rack of similar server systems. The System ID LED can also be toggled on and off remotely using the IPMI "Chassis Identify" command which will cause the LED to blink for 15 seconds.
- **B NMI Button** When the NMI button is pressed, it puts the server in a halt state and issues a non-maskable interrupt (NMI). This can be useful when performing diagnostics for a given issue where a memory download is necessary to help determine the cause of the problem. To prevent an inadvertent system halt, the actual NMI button is located behind the Front Control Panel faceplate where it is only accessible with the use of a small tipped tool like a pin or paper clip.
- **C, D, I and J Network Activity LEDs** The Front Control Panel includes an activity LED indicator for each on-board Network Interface Controller (NIC). When a network link is detected, the LED will turn on solid. The LED will blink once network activity occurs at a rate that is consistent with the amount of network activity that is occurring.
- **E System Cold Reset Button** When pressed, this button will reboot and re-initialize the system.

F – System Status LED – The System Status LED is a bi-color (Green/Amber) indicator that shows the current health of the server system. The system provides two locations for this feature; one is located on the Front Control Panel, the other is located on the back edge of the server board, viewable from the back of the system. Both LEDs are tied together and will show the same state. The System Status LED states are driven by the on-board platform management sub-system. The following table provides a description of each supported LED state.

Table 24. System Status LED State Definitions

Color	State	Criticality	Description
Off	System is not operating	Not ready	 System is powered off (AC and/or DC). System is in EuP Lot6 Off Mode. System is in S5 Soft-Off State. System is in S4 Hibernate Sleep State.
Green	Solid on	Ok	Indicates that the System is running (in S0 State) and its status is 'Healthy'. The system is not exhibiting any errors. AC power is present and BMC has booted and manageability functionality is up and running.
Green	~1 Hz blink	Degraded - system is operating in a degraded state although still functional, or system is operating in a redundant state but with an impending failure warning	 System degraded: Redundancy loss, such as power-supply or fan. Applies only if the associated platform sub-system has redundancy capabilities. Fan warning or failure when the number of fully operational fans is more than minimum number needed to cool the system. Non-critical threshold crossed – Temperature (including HSBP temp), voltage, input power to power supply, output current for main power rail from power supply and Processor Thermal Control (Therm Ctrl) sensors. Power supply predictive failure occurred while redundant power supply configuration was present. Unable to use all of the installed memory (one or more DIMMS failed/disabled but functional memory remains available) Correctable Errors over a threshold and migrating to a spare DIMM (memory sparing). This indicates that the user no longer has spared DIMMs indicating a redundancy lost condition. Corresponding DIMM LED lit. Uncorrectable memory error has occurred in memory Mirroring Mode, causing Loss of Redundancy. Correctable memory error threshold has been reached for a failing DDR3 DIMM when the system is operating in fully redundant RAS Mirroring Mode. Battery failure. BMC executing in uBoot. (Indicated by Chassis ID blinking at Blinking at 3Hz). System in degraded state (no manageability). BMC uBoot is running but has not transferred control to BMC Linux. Server will be in this state 6-8 seconds after BMC reset while it pulls the Linux image into flash BMC booting Linux. (Indicated by Chassis ID solid ON). System in degraded state (no manageability). Control has been passed from BMC uBoot to BMC Linux itself. It will be in this state for ~10-~20 seconds. BMC Watchdog has reset the BMC. Power Unit sensor offset for configuration error is asserted. <
Amber	~1 Hz blink	Non-critical - System is operating in a degraded state with an impending failure warning, although still functioning	 Non-fatal alarm – system is likely to fail: Critical threshold crossed – Voltage, temperature (including HSBP temp), input power to power supply, output current for main power rail from power supply and PROCHOT (Therm Ctrl) sensors. VRD Hot asserted. Minimum number of fans to cool the system not present or failed Hard drive fault Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies present) In non-sparing and non-mirroring mode if the threshold of correctable
			errors is crossed within the window 7. Correctable memory error threshold has been reached for a failing DDR3 DIMM when the system is operating in a non-redundant mode

Color	State	Criticality	Description
Amber	Solid on	Critical, non- recoverable –	Fatal alarm – system has failed or shutdown: 1. CPU CATERR signal asserted
		System is halted	2. MSID mismatch detected (CATERR also asserts for this case).
			3. CPU 1 is missing
			4. CPU Thermal Trip
			5. No power good – power fault
			6. DIMM failure when there is only 1 DIMM present and hence no good memory present ¹ .
			7. Runtime memory uncorrectable error in non redundant mode.
			8. DIMM Thermal Trip or equivalent
			9. SSB Thermal Trip or equivalent
			10. CPU ERR2 signal asserted
			11. BMC\Video memory test failed. (Chassis ID shows blue/solid-on for this condition)
			12. Both uBoot BMC FW images are bad. (Chassis ID shows blue/solid-on for this condition)
			13. 240VA fault
			14. Fatal Error in processor initialization:
			a. Processor family not identical
			b. Processor model not identical
			c. Processor core/thread counts not identical
			d. Processor cache size not identical
			e. Unable to synchronize processor frequency
			f. Unable to synchronize QPI link frequency

G – Power/Sleep Button – Toggles the system power on and off. This button also functions as a sleep button if enabled by an ACPI compliant operating system. Pressing this button will send a signal to the iBMC, which will either power on or power off the system. The integrated LED is a single color (Green) and is capable of supporting different indicator states as defined in the following table.

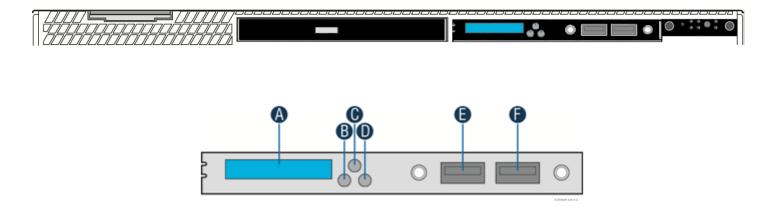
Table 25. Power/Sleep LED Functional States

State	Power Mode	LED	Description
Power-off	Non-ACPI	Off	System power is off, and the BIOS has not initialized the chipset.
Power-on	Non-ACPI	On	System power is on
S5	ACPI	Off	Mechanical is off, and the operating system has not saved any context to the hard disk.
S4	ACPI	Off	Mechanical is off. The operating system has saved context to the hard disk.
S3-S1	ACPI	Slow blink ¹	DC power is still on. The operating system has saved context and gone into a level of low-power state.
S0	ACPI	Steady on	System and the operating system are up and running.

H- Drive Activity LED - The drive activity LED on the front panel indicates drive activity from the on-board hard disk controllers. The server board also provides a header giving access to this LED for add-in controllers.

8. Intel[®] Local Control Panel

The Intel[®] Local Control Panel option (Intel Product Order Code – **AXXLCPANEL**) utilizes a combination of control buttons and LCD display to provide system accessibility and monitoring.



Label	Description	Functionality
Α	LCD Display	one line 18 character display
В	Left Control Button	moves the cursor backward one step or one character
С	"Enter" Button	selects the menu item highlighted by the cursor
D	Right Control Button	moves the cursor forward one step or one character
Е	USB 2.0 Port	
F	USB 2.0 Port	

Figure 27. Intel[®] Local Control Panel Option

The LCD (Local Control Display) is a one line character display that resides on the front panel of the chassis. It can display a maximum of 18 characters at a time. This device also contains 3 buttons (Left, Right and Enter). The user can select the content that needs to be displayed on the LCD screen by operating these buttons.

8.1 LCD Functionality

The LCD device provides the following features:

- Displays a banner when the system is healthy. The default banner is the server name.
- Displays active error messages when the system is not healthy.
- Provides basic server management configuration.
- Provides the ability to see asset information without having to open the chassis.

The LCD display is menu driven. Based on the user's selection, respective menu items are displayed. As soon as AC Power is applied to the system, the LCD panel displays faults detected while the system is on standby power prior to DC power on. If there are no faults, a banner is displayed. By default the banner is a text string which displays the "Server Name". The "Server Name" is the value specified as the product name in the product FRU information in the BMC FRU. Users can set any of the parameters under the banner configuration menu as a banner string.

When the system's status is degraded, the corresponding active event will be displayed in place of the banner. During an error, the background color will be light amber in color. The LCD panel displays the event with the highest severity that is most recent and is currently active (i.e. in an asserted state). For the case that there are multiple active events with the same severity, the most recent event will be displayed. The LCD panel returns to a light blue background when there are no longer any degraded, non-fatal, or fatal events active. The LCD panel shall operate in lock-step with the system status LED. For example, if the system is operating normally and an event occurs that results in the system status LED to blink green, then the LCD shall display the degraded event that triggered the systems status LED to blink.

Banner

Figure 28. LCP Background color during normal operation



Figure 29. LCP Background color during an error

If the user presses any button after the system is powered on, then the main menu will be displayed. The main menu contains "Error", "View" and "Config" items. Based on the user's selection, respective sub menu items will be displayed. At any point of time, if there is no user intervention for more than 10 min, a default banner (if there is no active error event in the system) or an error event will be displayed.

The following sections discuss the individual menu items. In the following sections, it is assumed that no active event exists during the LCD display. If any event (fatal or non-fatal) occurs that degrades the system's performance, the color of the LCD background turns into light amber. Even though all the contents (full text) are shown in the example screen shots in the following sections, by default, only the first 18 characters are displayed when a particular menu item is selected. The remaining text can be viewed by using right or left buttons.

8.2 Main Menu

If the user presses any button, when the Banner/Error screen is displayed, the following main menu will get displayed. Using left and right scroll buttons, the curser can be moved under any one of the following four menu items.

^ | Event | View | Config

Figure 30. LCP Main Menu

If the user selects menu item, "^", then the LCD displays the previous screen, i.e. Banner/Error string. Selecting the menu item means, moving the cursor under that item using left or right buttons and pressing enter button subsequently. In all the following sections (or for any screen shot), if the user presses "Enter" button, when the curser is under the symbol, "^", it takes to the previous screen. Selection of any of the menu items; Event, View or Config, leads the display to their corresponding screen shots and the details of these screen shots are given in the following sections.

8.3 Event Menu

If the "Event" menu, the LCD displays the following items. It displays all active error events in human readable text in chronological order. Informational events will not be displayed. There is no upper limit on the number of active events which can be displayed. The severity of the event will be indicated as either "Degraded", "Non Fatal" or "Fatal".

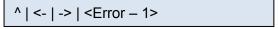


Figure 31. LCP Event Menu

The menu items, "<-" and "->" are used to traverse among the events. Selection of the menu item, "<-", displays the previous event and the item, "->", displays the next event in human readable format. By default the first event after the last power on will be displayed. If there are no events after the last power on, then fourth field is empty on the LCD screen.

By default, each error event scrolls automatically so that the entire error message can be read without pressing either the left or right scroll buttons. To stop auto scrolling, cursor has to be brought under the event message and the right button has to be pressed. Then the screen freezes. To start scrolling again right button has to be pressed when the cursor is under the event message. So, when the cursor is under event message, the right button decides whether to scroll or freeze the display of event message on the screen. When the cursor is

under the event message, pressing enter button displays the failing FRU (if any) in an easily human readable format for that error event. Pressing enter button alternatively switches the display between error message and the failing FRU (if any) information of that error message alternatively. If there is no FRU device associated with that error, then enter button has no effect when the cursor is under the error message. Left button moves the cursor under the previous token or menu item, i.e "->".

8.4 View Menu

The following screen is displayed when "View" is selected from the main menu.

```
^ | SysFwVer | SysInfo | BMC IP Conf |
RMM4 IP Config | Power | Last PC
```

Figure 32. LCP View Menu

Based on the user's selection, details of the specific item will be displayed. The following sub sections explain the above menu items in detail.

8.4.1 System FW Version (SysFwVer)

Selection of the "SysFwVer" item in the "View" menu displays the current firmware versions of the system as shown below:

```
^ | BIOS = xx.xx | BMC = xx.xx | ME = xx.xx | FRUSDR = xx.xx
```

Figure 33. System Firmware Versions Menu

This is a leaf node and there is no further traversal below this menu. User can only go to the previous screen by selecting the item, "^". This applies to all the items of "View" menu.

8.4.2 System Information (SysInfo)

Selection of "SysInfo" item in the "View" menu displays the Server's name, model, GUID, asset tag and custom string. It is also a leaf node like above menu. The blanks in the following display will be replaced by their values.

```
^ | Server Name: ...... | Server Model: ..... | Asset Tag: ..... | Server GUID: .... | Custom String: .......
```

Figure 34. System Information menu

Each of the above fields is explained below:

- a. Server Name: Value specified in the product name in the product FRU information in the main board BMC FRU.
- b. Server Model: Value specified in the product part number in the product FRU information in the main board BMC FRU.
- c. Asset tag: Value specified in the product asset tag in the product FRU information in the main board BMC FRU.
- d. Server GUID: System UUID stored by BIOS.
- e. Custom String: Custom string placed by the OEM\end user.

8.4.3 BMC IP Configuration

Selection of "BMC IP Conf" item in the "View" menu displays the RMM4 IP configuration details. These details show whether the IP is configured using DHCP or Static, IP Address, Subnet Mask and Gateway.

```
^ | DHCP (or Static) | IP Address:
xxx.xxx.xxx.xxx | Subnet Mask:
xxx.xxx.xxx.xxx | Gateway:
xxx.xxx.xxx.xxx
```

Figure 35. LCP - BMC IP Configuration

8.4.4 RMM4 IP Configuration

Selection of "RMM4 IP Conf" item in the "View" menu displays the BMC IP configuration details. These details show whether the IP is configured using DHCP or Static, IP Address, Subnet Mask and Gateway.

```
^ | DHCP (or Static) | IP Address:
xxx.xxx.xxx.xxx | Subnet Mask:
xxx.xxx.xxx.xxx | Gateway:
xxx.xxx.xxx.xxx
```

Figure 36. LCP - RMM4 IP Configuration

8.4.5 **Power**

Selection of "Power" item in the "View" menu displays the amount of AC power drawn by the system in Watts.

```
^ | xx W
```

Figure 37. LCP - Power Consumed by the System Currently

8.4.6 Last Post Code (Last PC)

Selection of "Last PC" item in the "View" menu displays the last BIOS POST code in hexadecimal.

```
^ | XX (Last BIOS POST Code in Hex)
```

Figure 38. LCP - Last BIOS Post Code

8.5 Config Menu

If the user selects "Config" item in the main menu, then the following options will be displayed to configure.

```
^ | IP Version | BMC IP | RMM4 IP |
Boot Device | Banner
```

Figure 39. LCP - Configure Menu Items

The following sub-sections will explain individual items of the configuration menu.

8.5.1 IP Version

If the user selects "IP Version" in the "Config" menu, the following options will be displayed. Based the user's selection, firmware will set the IP Version as either IPv4 or IPv6.

^ | IPv4 | IPv6

Figure 40. LCP - IP Version configuration screen

8.5.2 BMC IP

If the user selects "BMC IP" item, in the "Config" menu then the following options will be displayed.

^ | IP Source | IP Address | Subnet | Gateway

Figure 41. LCP - BMC IP Configuration Menu

Selection of the "IP Source" in the above menu, leads to the following screen. Based on the user's selection in the following menu, the firmware sets the BMC IP source as either DHCP or Static.



Figure 42. LCP – BMC IP Source Configuration Menu

If the user selects DHCP or the existing IP source is DHCP, then the other menu items, i.e. IP Address, Subnet and Gateway are not configurable. If the user selects "Static" or the existing setting is static for IP source, then the user is allowed to change the other menu items and the screen shots look as follows:

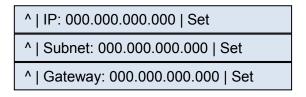


Figure 43. Screen shots for Configuring IP Address, Subnet Mask and Gateway

By default the cursor will be under the symbol, "^" and the IP address is displayed as 000.000.000.000. A right button will take the cursor to the first position (first 0) of the IP address. When the cursor is under the second menu item, the functionality of Left, Right and Enter buttons is different from the previous screens. The second token consists of twelve 0 s' separated by '.' character in IP address format. The behaviors of these buttons are as follows when the cursor is under this item.

- 1. Left and Right buttons inside the second menu item traverses among the 0 positions within the same item.
- 2. If the cursor is under last position inside the second menu item, then a right button will move the cursor to next item, that is, "Set".
- 3. If the cursor is under first position inside the second menu item, then a left button moves the cursor to the previous item, that is, "^".
- 4. First Enter button at any "0" position makes that position to be selected to increment or decrement the value at that position. The values allowed are between and including 0 and 9.
- 5. Any further Left or Right buttons will decrement or increment the value at that position.
- 6. Second Enter button at that position makes the cursor to be ready for moving left or right. Any further Left or Right moves the cursor to previous or next position respectively.
- 7. So, the Enter button is used to select a position at the first time and to leave the position at the second time.

The following state transition diagram explains the above steps pictorially, while setting an IP address using the LCD device. After entering an IP address, the user has to select "Set" item to set the entered IP address to the corresponding parameter (IP Address, Subnet Mask or Gateway).

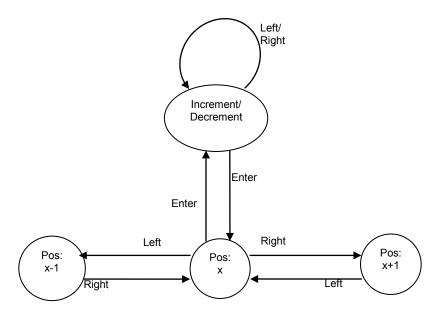


Figure 44. State transition diagram for setting IP Address

8.5.3 RMM4 IP

Same screen shots and the same description as that of the previous section ("BMC IP") are applicable for "RMM4 IP" configuration menu also.

8.5.4 Boot Device

If the user selects "Boot Device" in the "Config" menu, then the following options will be displayed. The selected item will be set as the next boot option and it will not be a permanent change.

^ | CD\DVD | Hard Drive | Network Boot | EFI Shell

Figure 45. Boot options configuration menu

8.5.5 Banner

When the user selects "Banner" in the "Config" menu, the following options will be displayed. The selected item will be set as banner and the same will be displayed from next banner screen onwards.

^ | Server Name | Server Model | Error | BMC IP | RMM4 IP | Power | Last PC | Custom String | Custom Logo

Figure 46. Banner configuration menu

Each of the menu items are explained below:

- **Server Name:** Displays the value specified in the product name in the product FRU information in the main board BMC FRU. The "Server Name" is the default banner.
- **Server Model:** Displays the value specified in the product part number in the product FRU information in the main board BMC FRU.
- Error: Displays the last active system event. The last active event may be degraded, non critical or critical only. It will not display an informational message. If the system is healthy then displays "System Health Ok".
- **BMC IP:** Displays the IPv4 or IPv6 address of BMC IP. If the BMC IP address is not configured, then nothing is displayed.

- RMM4 IP: Displays the IPv4 or IPv6 address of RMM4 dedicated LAN IP. If the RMM4 IP is not set or not present, then nothing is displayed.
- Power: Displays the current system power consumption in watts. The power consumed will be refreshed every minute.
- Last PC: Displays last BIOS post code.
- Custom string: Displays a customizable text string. The custom text string is modifiable through BIOS setup.
- **Custom Logo:** Displays a customizable bitmap logo. The OEM customized logo is programmed by the OEM and will be maintained during subsequent firmware updates.

9. PCI Riser Card Support

The system includes two riser card slots on the server board. Riser cards for this server are NOT interchangeable between riser slots. This section will provide an overview of each available riser card and describe the server board features and architecture supporting them.

9.1 Architectural Overview of the Server Board Riser Slots

The server board includes two riser card slots labeled "RISER_Slot_1" and "RISER_Slot_2". The following diagrams illustrate the general server board architecture supporting these two slots.

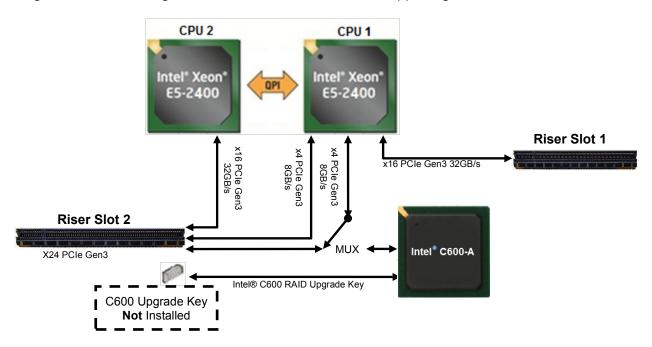


Figure 47. Riser Slot Architecture - Intel® C600 Upgrade Key NOT installed

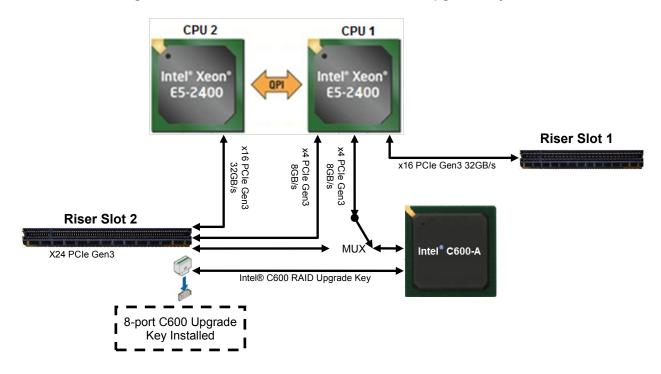


Figure 48. Riser Slot Architecture - Intel® C600 Upgrade Key Installed



CPU #1 provides Riser Slot #1 with x16 PCIe bus lanes which can be bifurcated to support multi-slot riser cards

The number of PCIe lanes routed to Riser Slot #2 is dependent on the system configuration. In a single processor configuration, CPU #1 will route x8 (default) PCIe bus lanes to Riser Slot #2. However, should the system be configured with an optionally installed 8-port Intel® C600 Upgrade Key, four of eight PCIe bus lanes from CPU #1 will be routed via a multiplexor to the Intel® C602 chipset to support the embedded 8-port SCU SATA/SAS controller. With CPU #2 installed, an additional x16 PCIe bus lanes are routed to Riser Slot #2. All available PCIe lanes routed to Riser Slot #2 can be bifurcated to support multi-slot riser cards. See the following diagram to determine PCI bus lane routing for each riser card.

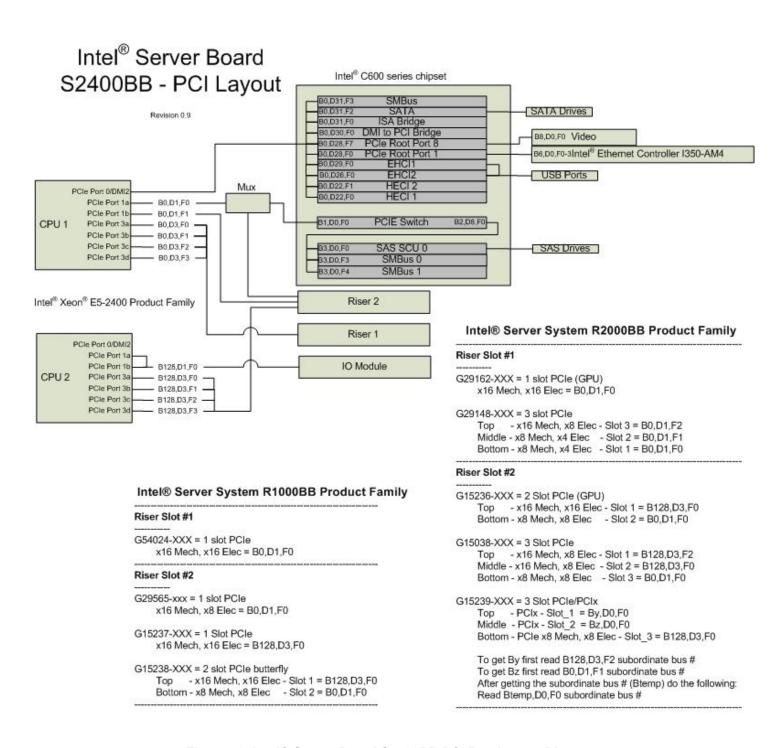


Figure 49. Intel® Server Board S2400BB PCI Bus Layout Diagram

9.2 Riser Card Support

The system has concurrent support for two riser cards. Each riser card is mounted to a bracket assembly and is installed into the system by aligning the edge connector of the riser card with the matching slot connector on the server board, and with hooks on the bracket assembly to slots on the back edge of the chassis.

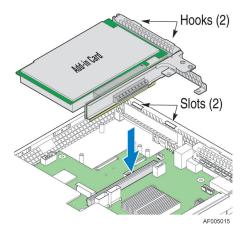


Figure 50. Add-in Card Support

The system has several riser card options. Riser cards for this server are NOT interchangeable between riser slots.

Caution: Riser cards are **NOT** interchangeable between Riser Slot #1 and Riser Slot #2. The riser card assembly for Riser #1 will include a mechanical block to prevent accidental insertion into Riser Slot #2.

Do not install a Riser Slot #1 riser card into Riser Slot #2. Doing so will electrically damage the riser card, riser slot, or both.

9.3 Riser Card Options – Riser Slot #1

All x16 PCIe bus lanes for Riser Slot #1 on the server board are routed from CPU #1. The riser card designed for Riser Slot #1 includes a single PCIe x16 (x16 lanes, x16 slot) add-in slot that can support a single full height, half length PCIe add-in card. However, add-in card size maybe limited to half height, half length PCIe add-in cards when the following options are configured:

- A cable is installed into either mini-SAS SCU connector
- An Intel[®] Integrated RAID Module is installed into the rear facing add-in PCIe slot from the butterfly riser card option installed in Riser Slot #2.

Note: Some half height PCIe add-in cards were found to interfere with the Intel® Integrated RAID Module when installed.



Figure 51. 1U Riser Card #1 Assembly Drawing

9.4 Riser Card Options – Riser Slot #2

The number of PCIe bus lanes routed to Riser Slot #2 is dependent on the number of CPUs installed, the type of riser card installed, and whether or not an 8-port Intel® C600 Upgrade Key is installed.

In a single processor configuration, by default CPU #1 will route x8 PCIe bus lanes to Riser Slot #2. However, should the system be configured with an 8-port Intel[®] C600 Upgrade Key, four of eight PCIe bus lanes from CPU #1 will be routed via a multiplexor to the Intel[®] C602 chipset to support the embedded 8-port SCU SATA/SAS controller.

With CPU #2 installed, an additional x16 PCle bus lanes are routed to the riser slot.

PCI bus lane utilization is dependent on the riser card option installed. Riser cards designed for Riser Slot #2 include the following

9.4.1 1-Slot PCle x8 Riser Card (default)

Using this riser card, x8 PCIe bus lanes are routed to Riser Slot #2 from CPU #1. However, should the system be configured with a an 8-port Intel[®] C600 Upgrade Key, four of the eight PCIe bus lanes from CPU #1 will be routed via a multiplexor to the Intel[®] C602 chipset to support the embedded 8-port SCU SATA/SAS controller.



Slot Description	PCI Lane Routing Riser Slot #2
PCIe x8 lanes, x16 slot	CPU1 with no RAID Key installed
PCIe x4 lanes, x16 slot	CPU1 with 8-port RAID Key installed

9.4.2 1-Slot PCle x16 Riser Card (option)

Using this riser card, x16 PCIe bus lanes are routed to Riser Slot #2 from CPU #2. This riser card option can only be used in a dual processor configuration. This riser card option has no functionality in a single processor configuration.



Slot Description	PCI Lane Routing Riser Slot #2
PCIe x16 lanes, x16 slot	CPU2

9.4.3 2-Slot Butterfly Riser Card (option)

This riser card option provides support for up to two add-in cards.

The riser card assembly (card + bracket) is designed specifically to support an Intel[®] Integrated RAID Module in the x8 PCIe slot on the back side of the riser. Other PCIe add-in cards cannot be supported in this add-in card slot.

By default, x8 PCIe bus lanes are routed from CPU#1 to support this add-in card slot. However, should the system be configured with a an 8-port Intel[®] C600 Upgrade Key, four of the eight PCIe bus lanes from CPU #1 will be routed via a multiplexor to the Intel[®] C602 chipset to support the embedded 8-port SCU SATA/SAS controller.

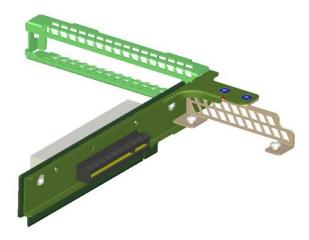


Figure 52. 1U Butterfly Riser Card #2 Assembly – Back Side View

On the front side of the riser card is a x16 PCIe slot (x16 lanes, x16 slot). This add-in card slot can support full height, half length PCIe add-in cards and can only be used in a dual processor configuration. This add-in card slot has no functionality in a single processor configuration.

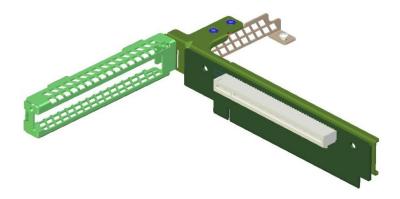


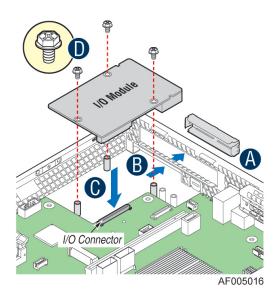
Figure 53. 1U Butterfly Riser Card #2 Assembly - Front Side View

Slot Location	Slot Description	PCI Lane Routing Riser Slot #2
Back Side add-in card slot	PCle x8 lanes, x8 slot	CPU1 with no RAID Key installed
Back Side add-in card slot	PCle x4 lanes, x8 slot	CPU1 with 8-port RAID Key installed
Front Side add-in card slot	PCIe x16 lanes, x16 slot	CPU2

10. Mezzanine Module Support

10.1 IO Module Support

In addition to the embedded I/O features of the server board, and those available with the addition of a PCIe add-in card, the server also provides concurrent support of an optionally installed mezzanine I/O module.



The following table lists the Intel® I/O modules available for this server.

Product Code & iPN	Description
AXX10GBNIAIOM	Dual SFP+ port 10GbE IO Module based on Intel® 82599 10GbE Ethernet Controller
AXX10GBTWLIOM	Dual RJ45 Port, 10GBASE-T IO Module, based on Intel® I350 ethernet chipset
AXX1FDRIBIOM	Single Port, FDR speed Infiniband module, with QSFP connector
AXX4P1GBPWLIOM	Quad Port 1GbE 1o Module based on Intel® Ethernet Controller I350
AXXQAAIOMOD	Intel® Quick Assist Accelerator IO Mezzanine Card

10.2 Intel® Remote Management Module 4 (RMM4) Lite and Management NIC Support

The integrated baseboard management controller has support for advanced management features which are enabled when an optional Intel® Remote Management Module 4 (RMM4) is installed.

RMM4 is comprised of two boards – RMM4 lite and the optional Dedicated Server Management NIC (DMN).

Intel Product Code	Description	Kit Contents	Benefits
AXXRMM4LITE	Intel® Remote Management Module 4 Lite	RMM4 Lite Activation Key	Enables KVM & media redirection via onboard NIC
AXXRMM4R	Intel® Remote Management Module 4	RMM4 Lite Activation Key Dedicated NIC Port Module	Dedicated NIC for management traffic. Higher bandwidth connectivity for KVM & media Redirection with 1Gbe NIC.

On the server board each Intel® RMM4 component is installed at the following locations.

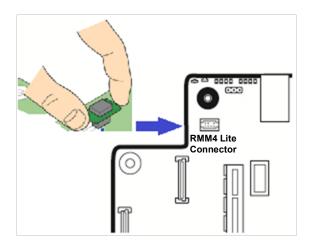


Figure 54. Intel® RMM4 Lite Activation Key Installation

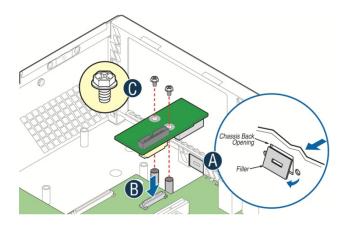


Figure 55. Intel® RMM4 Dedicated Management NIC Installation

Table 26. Enabling Advanced Management Features

Manageability Hardware	Benefits
Intel [®] Integrated BMC	Comprehensive IPMI based base manageability features
Intel® Remote Management Module 4 – Lite Package contains one module – 1- Key for advance Manageability features.	No dedicated NIC for management Enables KVM & media redirection via onboard NIC
Intel® Remote Management Module 4 Package includes 2 modules – 1 - key for advance features 2 - Dedicated NIC (1Gbe) for management	Dedicated NIC for management traffic. Higher bandwidth connectivity for KVM & media Redirection with 1Gbe NIC.

For further RMM4 information, please refer to the following documents:

- Intel[®] Server Board S2400BB Technical Product Specification
- Intel® Remote Management Module 4 Technical Product Specification
- Intel® Remote Management Module 4 and Integrated BMC Web Console Users Guide

Appendix A: Integration and Usage Tips

This section provides a list of useful information that is unique to the Intel® Server System R1000BB Product Family and should be kept in mind while configuring your server system.

- Only the Intel[®] Xeon[®] processor E5-2400 product family is supported in this Intel server system. Previous generation Intel[®] Xeon[®] processors are not supported.
- For best system performance, follow memory population guidelines as specified in the *Intel*® *Server Board S2400BB Technical Product Specification*.
- For best system performance, follow all thermal configuration guidelines as specified in this document.
- The Mini-SAS connector labeled "SCU_1" on the server board is only functional when an appropriate Intel® RAID C600 Upgrade Key is installed.
- Many integrated on-board SAS and RAID options are available by installing any of several available Intel® RAID C600 Upgrade Keys.
- The riser cards for Riser Slot #1 and Riser Slot #2 are **NOT** interchangeable.
- The embedded platform management system may not operate as expected if the platform is not updated with accurate system configuration data. The FRUSDR utility must be run with the system fully configured and each time the system configuration changes for accurate system monitoring and event reporting.
- Make sure the latest system software is loaded on the server. This includes System BIOS, BMC
 Firmware, ME Firmware and FRU & SDR data. The latest system software can be downloaded from
 http://www.intel.com/support.

Appendix B: POST Code Diagnostic LED Decoder

As an aid to assist in trouble shooting a system hang that occurs during a system's Power-On Self Test (POST) process, the server board includes a bank of eight POST Code Diagnostic LEDs on the back edge of the server board.

During the system boot process, Memory Reference Code (MRC) and System BIOS execute a number of memory initialization and platform configuration processes, each of which is assigned a specific hex POST code number. As each routine is started, the given POST code number is displayed to the POST Code Diagnostic LEDs on the back edge of the server board.

During a POST system hang, the displayed post code can be used to identify the last POST routine that was run prior to the error occurring, helping to isolate the possible cause of the hang condition.

Each POST code is represented by eight LEDs; four Green and four Amber. The POST codes are divided into two nibbles, an upper nibble and a lower nibble. The upper nibble bits are represented by Amber Diagnostic LEDs #4, #5, #6, #7. The lower nibble bits are represented by Green Diagnostics LEDs #0, #1, #2 and #3. If the bit is set in the upper and lower nibbles, the corresponding LED is lit. If the bit is clear, the corresponding LED is off.

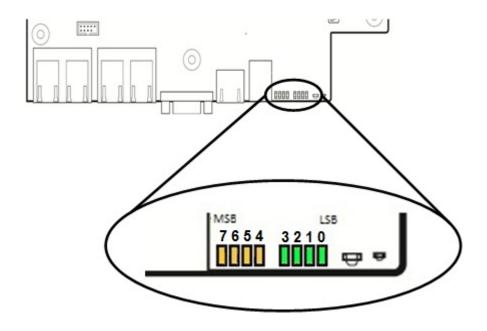


Figure 56. POST Diagnostic LEDs

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

	U	pper Nibble	AMBER LED	s	Lower Nibble GREEN LEDs				
LEDs	MSB							LSB	
LEDS	LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0	
	8h	4h	2h	1h	8h	4h	2h	1h	
Status	ON	OFF	ON	OFF	ON	ON	OFF	OFF	
Results	1	0	1	0	1	1	0	0	
Results		Α	h			С	h		

Table 27. POST Progress Code LED Example

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh.

Table 28. Diagnostic LED POST Code Decoder

1 7	Diagn	ostic	LED	Deco	der				
	1 = LF	ED O	n, 0 =	: LED	Off				
	Uppei				Low	er Nik	ble		
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
	# 7	#6	#5	#4	#3	#2	#1	#0	Description
SEC Phase				1					
	0	0	0	0	0	0	0	1	First POST code after CPU reset
02h		0	0	0	0	0	1	0	Microcode load begin
03h	0	0	0	0	0	0	1	1	CRAM initialization begin
04h		0	0	0	0	1	0	0	Pei Cache When Disabled
05h		0	0	0	0	1	0	1	SEC Core At Power On Begin.
06h		0	0	0	0	1	1	0	Early CPU initialization during Sec Phase.
-	0	0	0	0	0	1	1	1	Early SB initialization during Sec Phase.
08h	0	0	0	0	1	0	0	0	Early NB initialization during Sec Phase.
09h		0	0	0	1	0	0	1	End Of Sec Phase.
	0	0	0	0	1	1	1	0	Microcode Not Found.
	0	0	0	0	1	1	1	1	Microcode Not Loaded.
PEI Phase									
	0	0	0	1	0	0	0	0	PEI Core
11h		0	0	1	0	0	0	1	CPU PEIM
15h		0	0	1	0	1	0	1	NB PEIM
19h		0	0	1	1	0	0	1	SB PEIM
		•	•		ss Co	_	_		executed - See Table 63
PEI Phase conf			1101	rogro	00 00	, ac c	oquo	1100 10	chedita ce rabie e
31h		0	1	1	0	0	0	1	Memory Installed
32h		0	1	1	0	0	1	0	CPU PEIM (Cpu Init)
33h		0	1	1	0	0	1	1	CPU PEIM (Cache Init)
34h		0	1	1	0	1	0	0	CPU PEIM (BSP Select)
35h		0	1	1	0	1	0	1	CPU PEIM (AP Init)
36h		0	1	1	0	1	1	0	CPU PEIM (CPU SMM Init)
	<u>)</u> D	1	0	0	1	1	1	1	Dxe IPL started
DXE Phase	U		U	U	1			1	DXC II E Started
-	0	1	1	0	0	0	0	0	DXE Core started
61h		1	1	0	0	0	0	1	DXE NVRAM Init
62h		1	1	0	0	0	1	0	SB RUN Init
63h		1	1	0	0	0	1	1	Dxe CPU Init
68h		1	1	0	1	0	0	0	DXE PCI Host Bridge Init
69h		1	1	0	1	0	0	1	DXE NB Init
-	0	1	1	0	1	0	1	0	DXE NB SMM Init
	0	1	1	1	0	0	0	0	DXE SB Init
-		1	1	1	0	0	0	1	
		1	1	1	<u> </u>		4	0	DXE SB SMM Init DXE SB devices Init
-	0	1	1	1	0	0	0	0	DXE ACPI Init
		_	-		1	0	0	1	
79h (1	0	0	1	-	0	0	0	DXE CSM Init DXE BDS Started
	1		+	_	0		0	1	
91h	1	0	0	1	0	0	0	•	DXE BDS connect drivers
92h	1	0	0	1	0	0	1	0	DXE PCI Bus begin
93h	1	0	0	1	0	0	1		DXE PCI Bus HPC Init
94h	1	0	0	1	0	1	0	0	DXE PCI Bus enumeration
95h	1	0	0	1	0	1	0	1	DXE PCI Bus resource requested
96h	1	0	0	1	0	1	1	0	DXE PCI Bus assign resource
97h	1	0	0	1	0	1	1	1	DXE CON_OUT connect
98h	1	0	0	1	1	0	0	0	DXE CON_IN connect
99h 1	1	0	0	1	1	0	0	1	DXE SIO Init
9Ah 1	1	0	0	1	1	0	1	0	DXE USB start
9Bh 1	1	0	0	1	1	0	1	1	DXE USB reset
9Ch 1	1	0	0	1	1	1	0	0	DXE USB detect
9Dh	1	0	0	1	1	1	0	1	DXE USB enable
A1h	1	0	1	0	0	0	0	1	DXE IDE begin DXE IDE reset
A2h		0		0				0	

		nostic							
		ED O							
Checkpoint	Upp	er Nibl	ble		Low	er Nil	ble		
	MSE	3						LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED#	#7	#6	#5	#4	#3	#2	#1	#0	Description
A3h	1	0	1	0	0	0	1	1	DXE IDE detect
A4h	1	0	1	0	0	1	0	0	DXE IDE enable
A5h	1	0	1	0	0	1	0	1	DXE SCSI begin
A6h	1	0	1	0	0	1	1	0	DXE SCSI reset
A7h	1	0	1	0	0	1	1	1	DXE SCSI detect
A8h	1	0	1	0	1	0	0	0	DXE SCSI enable
A9h	1	0	1	0	1	0	0	1	DXE verifying SETUP password
ABh	1	0	1	0	1	0	1	1	DXE SETUP start
ACh	1	0	1	0	1	1	0	0	DXE SETUP input wait
ADh	1	0	1	0	1	1	0	1	DXE Ready to Boot
AEh	1	0	1	0	1	1	1	0	DXE Legacy Boot
AFh	1	0	1	0	1	1	1	1	DXE Exit Boot Services
B0h	1	0	1	1	0	0	0	0	RT Set Virtual Address Map Begin
B1h	1	0	1	1	0	0	0	1	RT Set Virtual Address Map End
B2h	1	0	1	1	0	0	1	0	DXE Legacy Option ROM init
B3h	1	0	1	1	0	0	1	1	DXE Reset system
B4h	1	0	1	1	0	1	0	0	DXE USB Hot plug
B5h	1	0	1	1	0	1	0	1	DXE PCI BUS Hot plug
B6h	1	0	1	1	0	1	1	0	DXE NVRAM cleanup
B7h	1	0	1	1	0	1	1	1	DXE Configuration Reset
00h	0	0	0	0	0	0	0	0	INT19
S3 Resume				-					
E0h	1	1	0	1	0	0	0	0	S3 Resume PEIM (S3 started)
E1h	1	1	0	1	0	0	0	1	S3 Resume PEIM (S3 boot script)
E2h	1	1	0	1	0	0	1	0	S3 Resume PEIM (S3 Video Repost)
E3h	1	1	0	1	0	0	1	1	S3 Resume PEIM (S3 OS wake)
BIOS Recove	ery								, , ,
F0h	1	1	1	1	0	0	0	0	PEIM which detected forced Recovery condition
F1h	1	1	1	1	0	0	0	1	PEIM which detected User Recovery condition
F2h	1	1	1	1	0	0	1	0	Recovery PEIM (Recovery started)
F3h	1	1	1	1	0	0	1	1	Recovery PEIM (Capsule found)
F4h	1	1	1	1	0	1	0	0	Recovery PEIM (Capsule loaded)
·									, (

POST Memory Initialization MRC Diagnostic Codes

There are two types of POST Diagnostic Codes displayed by the MRC during memory initialization; Progress Codes and Fatal Error Codes.

The MRC Progress Codes are displays to the Diagnostic LEDs that show the execution point in the MRC operational path at each step.

Table 29. MRC Progress Codes

	Diagn	ostic	: LEC) De	code	r			
	1 = LE	D O	n, 0	= LE	D O	ff			
Checkpoint	Upper	Nibl	ble		Low	er N	ibble	!	Description
	MSB							LSB	Description
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
MRC Progress Cod	des								
B0h	1	0	1	1	0	0	0	0	Detect DIMM population
B1h	1	0	1	1	0	0	0	1	Set DDR3 frequency
B2h	1	0	1	1	0	0	1	0	Gather remaining SPD data
B3h	1	0	1	1	0	0	1	1	Program registers on the memory controller level
B4h	1	0	1	1	0	1	0	0	Evaluate RAS modes and save rank information
B5h	1	0	1	1	0	1	0	1	Program registers on the channel level
B6h	1	0	1	1	0	1	1	0	Perform the JEDEC defined initialization sequence
B7h	1	0	1	1	0	1	1	1	Train DDR3 ranks
B8h	1	0	1	1	1	0	0	0	Initialize CLTT/OLTT
B9h	1	0	1	1	1	0	0	1	Hardware memory test and init
BAh	1	0	1	1	1	0	1	0	Execute software memory init
BBh	1	0	1	1	1	0	1	1	Program memory map and interleaving
BCh	1	0	1	1	1	1	0	0	Program RAS configuration
BFh	1	0	1	1	1	1	1	1	MRC is done

Memory Initialization at the beginning of POST includes multiple functions, including: discovery, channel training, validation that the DIMM population is acceptable and functional, initialization of the IMC and other hardware settings, and initialization of applicable RAS configurations.

When a major memory initialization error occurs and prevents the system from booting with data integrity, a beep code is generated, the MRC will display a fatal error code on the diagnostic LEDs, and a system halt command is executed. Fatal MRC error halts do NOT change the state of the System Status LED, and they do NOT get logged as SEL events. The following table lists all MRC fatal errors that are displayed to the Diagnostic LEDs.

Table 30. MRC Fatal Error Codes

	Diagi	nostic	LED	Deco	der				
	1 = L	ED O	n, 0 =	LED	Off				
Checkpoint	Uppe	er Nibl	ble		Lower Nibble				
	MSB				LSB		Description		
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
MRC Fatal E	rror C	odes	<u> </u>						
E8h	1	1	1	0	1	0	0	0	No usable memory error 01h = No memory was detected via SPD read, or invalid config that causes no operable memory. 02h = Memory DIMMs on all channels of all sockets are disabled due to hardware memtest error. 3h = No memory installed. All channels are disabled.
E9h	1	1	1	0	1	0	0	1	Memory is locked by Intel Trusted Execuiton Technology and is inaccessible
EAh	1	1	1	0	1	0	1	0	DDR3 channel training error 01h = Error on read DQ/DQS (Data/Data Strobe) init 02h = Error on Receive Enable 3h = Error on Write Leveling 04h = Error on write DQ/DQS (Data/Data Strobe
EBh	1	1	1	0	1	0	1	1	Memory test failure 01h = Software memtest failure. 02h = Hardware memtest failed. 03h = Hardware Memtest failure in Lockstep Channel mode requiring a channel to be disabled. This is a fatal error which requires a reset and calling MRC with a different RAS mode to retry.
EDh	1	1	1	0	1	1	0	1	DIMM configuration population error 01h = Different DIMM types (UDIMM, RDIMM, LRDIMM) are detected installed in the system. 02h = Violation of DIMM population rules. 03h = The 3rd DIMM slot can not be populated when QR DIMMs are installed. 04h = UDIMMs are not supported in the 3rd DIMM slot. 05h = Unsupported DIMM Voltage.
EFh	1	1	1	0	1	1	1	1	Indicates a CLTT table structure error

Appendix C: POST Code Errors

- Most error conditions encountered during POST are reported using POST Error Codes. These codes
 represent specific failures, warnings, or are informational. POST Error Codes may be displayed in the
 Error Manager display screen, and are always logged to the System Event Log (SEL). Logged events
 are available to System Management applications, including Remote and Out of Band (OOB)
 management.
- There are exception cases in early initialization where system resources are not adequately initialized for handling POST Error Code reporting. These cases are primarily Fatal Error conditions resulting from initialization of processors and memory, and they are handed by a Diagnostic LED display with a system halt.
- The following table lists the supported POST Error Codes. Each error code is assigned an error type which determines the action the BIOS will take when the error is encountered. Error types include Minor, Major, and Fatal. The BIOS action for each is defined as follows:
- Minor: The error message is displayed on the screen or on the Error Manager screen, and an error is logged to the SEL. The system continues booting in a degraded state. The user may want to replace the erroneous unit. The POST Error Pause option setting in the BIOS setup does not have any effect on this error.
- Major: The error message is displayed on the Error Manager screen, and an error is logged to the SEL.
 The POST Error Pause option setting in the BIOS setup determines whether the system pauses to the
 Error Manager for this type of error so the user can take immediate corrective action or the system
 continues booting.

Note that for 0048 "Password check failed", the system halts, and then after the next reset/reboot will displays the error code on the Error Manager screen.

Fatal: The system halts during post at a blank screen with the text "Unrecoverable fatal error found. System will not boot until the error is resolved" and "Press <F2> to enter setup" The POST Error Pause option setting in the BIOS setup does not have any effect with this class of error.

When the operator presses the **F2** key on the keyboard, the error message is displayed on the Error Manager screen, and an error is logged to the SEL with the error code. The system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system.

NOTE: The POST error codes in the following table are common to all current generation Intel server platforms. Features present on a given server board/system will determine which of the listed error codes are supported.

Table 31. POST Error Messages and Handling

Error Code	Error Message	Response
0012	System RTC date/time not set	Major
0048	Password check failed	Major
0140	PCI component encountered a PERR error	Major
0141	PCI resource conflict	Major
0146	PCI out of resources error	Major
0191	Processor core/thread count mismatch detected	Fatal
0192	Processor cache size mismatch detected	Fatal
0194	Processor family mismatch detected	Fatal
0195	Processor Intel(R) QPI link frequencies unable to synchronize	Fatal
0196	Processor model mismatch detected	Fatal
0197	Processor frequencies unable to synchronize	Fatal
5220	BIOS Settings reset to default settings	Major
5221	Passwords cleared by jumper	Major
5224	Password clear jumper is Set	Major
8130	Processor 01 disabled	Major
8131	Processor 02 disabled	Major

Error Code	Error Message	Response
8132	Processor 03 disabled	Major
8133	Processor 04 disabled	Major
8160	Processor 01 unable to apply microcode update	Major
8161	Processor 02 unable to apply microcode update	Major
8162	Processor 02 unable to apply microcode update	Major
8163	Processor 04 unable to apply microcode update	Major
8170	Processor 01 failed Self Test (BIST)	Major
8171	Processor 02 failed Self Test (BIST)	Major
8172	Processor 03 failed Self Test (BIST)	Major
8173	Processor 04 failed Self Test (BIST)	Major
8180	Processor 01 microcode update not found	Minor
8181	Processor 02 microcode update not found	Minor
8182	Processor 03 microcode update not found	Minor
8183	Processor 04 microcode update not found	Minor
8190	Watchdog timer failed on last boot	Major
8198	OS boot watchdog timer failure	Major
8300	Baseboard management controller failed self-test	Major
8305	Hot Swap Controller failure	Major
83A0	Management Engine (ME) failed Selftest	Major
83A1	Management Engine (ME) Failed to respond.	Major
84F2	Baseboard management controller failed to respond	Major
84F3	Baseboard management controller in update mode	Major
84F4	Sensor data record empty	Major
84FF	System event log full	Minor
8500	Memory component could not be configured in the selected RAS mode	Major
8501	DIMM Population Error	Major
8520	DIMM A1 failed test/initialization	Major
8521	DIMM A2 failed test/initialization	Major
8522	DIMM A3 failed test/initialization	Major
8523	DIMM B1 failed test/initialization	Major
8524	DIMM B2 failed test/initialization	Major
8525	DIMM B3 failed test/initialization	Major
8526	DIMM C1 failed test/initialization	Major
8527	DIMM C2 failed test/initialization	Major
8528	DIMM C3 failed test/initialization	Major
8529	DIMM D1 failed test/initialization	Major
852A	DIMM D2 failed test/initialization	Major
852B	DIMM D3 failed test/initialization	Major
852C	DIMM E1 failed test/initialization	Major
852D	DIMM E2 failed test/initialization	Major
852E	DIMM E3 failed test/initialization	Major
852F	DIMM F1 failed test/initialization	Major
8530	DIMM F2 failed test/initialization	Major
8531	DIMM F3 failed test/initialization	Major
8532	DIMM G1 failed test/initialization	Major
8533	DIMM G2 failed test/initialization	Major
8534	DIMM_G3 failed test/initialization	Major
8535	DIMM H1 failed test/initialization	Major
8536	DIMM H2 failed test/initialization	Major
8537	DIMM H3 failed test/initialization	Major
8538	DIMM I1 failed test/initialization	Major
8539	DIMM I2 failed test/initialization	Major
853A	DIMM I3 failed test/initialization	Major
853B	DIMM J1 failed test/initialization	Major
853C	DIMM J2 failed test/initialization	Major
853D	DIMM J3 failed test/initialization	Major
853E	DIMM K1 failed test/initialization	Major
853F	DIMM_K2 failed test/initialization	Major
(Go to		-94.
85C0)		
8540	DIMM_A1 disabled	Major
8541	DIMM_A2 disabled	Major
	·	

Error Code Error Message Response S42 DIMM A3 disabled Major B543 DIMM B1 disabled Major B544 DIMM B2 disabled Major B544 DIMM B2 disabled Major B545 DIMM B2 disabled Major B546 DIMM C1 disabled Major B547 DIMM C2 disabled Major B548 DIMM C3 disabled Major B548 DIMM C3 disabled Major B549 DIMM C3 disabled Major B549 DIMM D2 disabled Major B549 DIMM D2 disabled Major B549 DIMM D2 disabled Major B548 DIMM D2 disabled Major B548 DIMM D2 disabled Major B549 DIMM E2 disabled Major B550 DIMM E2 disabled Major B550 DIMM E3 disabled Major B550 DIMM E3 disabled Major B550 DIMM E3 disabled Major B551 DIMM G3 disabled Major B552 DIMM G3 disabled Major B552 DIMM G3 disabled Major B553 DIMM G3 disabled Major B553 DIMM G3 disabled Major B554 DIMM H2 disabled Major B555 DIMM H1 disabled Major B555 DIMM H1 disabled Major B556 DIMM H2 disabled Major B557 DIMM H3 disabled Major B559 DIMM H2 disabled Major B559 DIMM H2 disabled Major B559 DIMM H3 disabled M3 B300 DIMM H3 disabled M3	
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B546 DIMM C1 disabled Major	
B547 DIMM C2 disabled Major	
B548 DIMM_D1 disabled Major	
B549 DIMM D1 disabled Major	
B54A DIMM D3 disabled Major	
B54B DIMM D3 disabled Major	
BS4D DIMM_E3 disabled Major	
B54E DIMM E3 disabled Major	
B54F DIMM F1 disabled Major	
B550 DIMM F2 disabled Major	
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B553 DIMM G2 disabled Major	
B554 DIMM G3 disabled Major	
B555 DIMM_H2 disabled Major	
B556 DIMM_H3 disabled Major	
B557 DIMM_H3 disabled Major	
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B559 DIMM_I3 disabled Major	
B55A DIMM_I3 disabled Major	
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B55E DIMM_K1 disabled Major	
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8573 DIMM_G2 encountered a Serial Presence Detection (SPD) failure Major	
8574 DIMM_G3 encountered a Serial Presence Detection (SPD) failure Major	
8575 DIMM_H1 encountered a Serial Presence Detection (SPD) failure Major	
8576 DIMM_H2 encountered a Serial Presence Detection (SPD) failure Major	
8577 DIMM_H3 encountered a Serial Presence Detection (SPD) failure Major	
8578 DIMM_I1 encountered a Serial Presence Detection (SPD) failure Major	
8579 DIMM_I2 encountered a Serial Presence Detection (SPD) failure Major	
857A DIMM_I3 encountered a Serial Presence Detection (SPD) failure Major	
857B DIMM_J1 encountered a Serial Presence Detection (SPD) failure Major	
857C DIMM_J2 encountered a Serial Presence Detection (SPD) failure Major	
857D DIMM_J3 encountered a Serial Presence Detection (SPD) failure Major	

Error Code	Error Message	Response
857E	DIMM_K1 encountered a Serial Presence Detection (SPD) failure	Major
857F	DIMM_K2 encountered a Serial Presence Detection (SPD) failure	Major
(Go to		
85E0)	DIMM 1/0 failed to attack in the line of a	NA. C.
85C0	DIMM_K3 failed test/initialization	Major
85C1 85C2	DIMM_L1 failed test/initialization DIMM L2 failed test/initialization	Major Major
85C3	DIMM_L3 failed test/initialization	Major
85C4	DIMM M1 failed test/initialization	Major
85C5	DIMM M2 failed test/initialization	Major
85C6	DIMM M3 failed test/initialization	Major
85C7	DIMM N1 failed test/initialization	Major
85C8	DIMM_N2 failed test/initialization	Major
85C9	DIMM_N3 failed test/initialization	Major
85CA	DIMM_O1 failed test/initialization	Major
85CB	DIMM_O2 failed test/initialization	Major
85CC	DIMM_O3 failed test/initialization	Major
85CD	DIMM_P1 failed test/initialization	Major
85CE	DIMM_P2 failed test/initialization	Major
85CF	DIMM_P3 failed test/initialization	Major
85D0 85D1	DIMM_K3 disabled	Major
85D1	DIMM_L1 disabled DIMM L2 disabled	Major Major
85D3	DIMM L3 disabled	Major
85D4	DIMM M1 disabled	Major
85D5	DIMM M2 disabled	Major
85D6	DIMM M3 disabled	Major
85D7	DIMM_N1 disabled	Major
85D8	DIMM_N2 disabled	Major
85D9	DIMM_N3 disabled	Major
85DA	DIMM_O1 disabled	Major
85DB	DIMM_O2 disabled	Major
85DC	DIMM_O3 disabled	Major
85DD	DIMM_P1 disabled	Major
85DE 85DF	DIMM_P2 disabled DIMM_P3 disabled	Major Major
85E0	DIMM K3 encountered a Serial Presence Detection (SPD) failure	Major
85E1	DIMM_L1 encountered a Serial Presence Detection (SPD) failure	Major
85E2	DIMM L2 encountered a Serial Presence Detection (SPD) failure	Major
85E3	DIMM L3 encountered a Serial Presence Detection (SPD) failure	Major
85E4	DIMM_M1 encountered a Serial Presence Detection (SPD) failure	Major
85E5	DIMM_M2 encountered a Serial Presence Detection (SPD) failure	Major
85E6	DIMM_M3 encountered a Serial Presence Detection (SPD) failure	Major
85E7	DIMM_N1 encountered a Serial Presence Detection (SPD) failure	Major
85E8	DIMM_N2 encountered a Serial Presence Detection (SPD) failure	Major
85E9	DIMM_N3 encountered a Serial Presence Detection (SPD) failure	Major
85EA	DIMM_O1 encountered a Serial Presence Detection (SPD) failure	Major
85EB	DIMM_O2 encountered a Serial Presence Detection (SPD) failure	Major
85EC	DIMM_O3 encountered a Serial Presence Detection (SPD) failure	Major
85ED 85EE	DIMM_P1 encountered a Serial Presence Detection (SPD) failure	Major
85EF	DIMM_P2 encountered a Serial Presence Detection (SPD) failure DIMM_P3 encountered a Serial Presence Detection (SPD) failure	Major Major
8604	POST Reclaim of non-critical NVRAM variables	Minor
8605	BIOS Settings are corrupted	Major
8606	NVRAM variable space was corrupted and has been reinitialized	Major
92A3	Serial port component was not detected	Major
92A9	Serial port component encountered a resource conflict error	Major
A000	TPM device not detected.	Minor
A001	TPM device missing or not responding.	Minor
A002	TPM device failure.	Minor
A003	TPM device failed self test.	Minor
A100	BIOS ACM Error	Major

Error Code	Error Message	Response
A421	PCI component encountered a SERR error	Fatal
A5A0	PCI Express component encountered a PERR error	Minor
A5A1	PCI Express component encountered an SERR error	Fatal
A6A0	DXE Boot Service driver: Not enough memory available to shadow a Legacy Option ROM	Minor

POST Error Beep Codes

The following table lists the POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user-visible code on the POST Progress LEDs

Table 32. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
1	USB device action	NA	Short beep sounded whenever a USB device is discovered in POST, or inserted or removed during runtime
1 long	Intel® TXT security violation	0xAE, 0xAF	System halted because Intel® Trusted Execution Technology detected a potential violation of system security.
3	Memory error	See Tables 28 and 29	System halted because a fatal error related to the memory was detected.
2	BIOS Recovery started	NA	Recovery boot has been initiated
4	BIOS Recovery failure	NA	BIOS recovery has failed. This typically happens so quickly after recovery us initiated that it sounds like a 2-4 beep code.

The Integrated BMC may generate beep codes upon detection of failure conditions. Beep codes are sounded each time the problem is discovered, such as on each power-up attempt, but are not sounded continuously. Codes that are common across all Intel server boards and systems that use same generation chipset are listed in the following table. Each digit in the code is represented by a sequence of beeps whose count is equal to the digit.

Table 33. Integrated BMC Beep Codes

Code	Reason for Beep	Associated Sensors
1-5-2-1	No CPUs installed or first CPU socket is empty.	CPU1 socket is empty, or sockets are populated incorrectly
		CPU1 must be populated before CPU2.
1-5-2-4	MSID Mismatch	MSID mismatch occurs if a processor is installed into a system board that has incompatible power capabilities.
1-5-4-2	Power fault	DC power unexpectedly lost (power good dropout) – Power unit sensors report power unit failure offset
1-5-4-4	Power control fault (power good assertion timeout).	Power good assertion timeout – Power unit sensors report soft power control failure offset
1-5-1-2	VR Watchdog Timer sensor assertion	VR controller DC power on sequence was not completed in time.
1-5-1-4	Power Supply Status	The system does not power on or unexpectedly powers off and a Power Supply Unit (PSU) is present that is an incompatible model with one or more other PSUs in the system.

Glossary

ACA Australian Communication Authority ANSI American National Standards Institute BMC Baseboard Management Controller BIOS Basic Input/Output System CMOS Complementary Metal-oxide-semiconductor D2D DC-to-DC EMP Emergency Management Port FP Front Panel FRB Faut Resilient Boot FRU Field Replaceable Unit I'C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-uoitage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Express* PSU Power-on Self Test PSU Power-on Self Content Power Sensor Data Record SE Single Connector Attachment SDR Sensor Data Record SE Single Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus Voltage Standby Voltage Standby	Word/Acronym	Definition
BMC Baseboard Management Controller BIOS Basic Input/Output System CMOS Complementary Metal-oxide-semiconductor D2D DC-to-DC EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I*C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Express* PSU Power Factor Correction POST Power- Oself Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single-Ended THD Total Harmonic Distortion UART Universal Serial Bus VCCI Voluntary Control Council for Interference	ACA	Australian Communication Authority
BIOS Basic Input/Output System CMOS Complementary Metal-oxide-semiconductor D2D DC-to-DC EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I'C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single-Ended THD Total Harmonic Distortion USR Universal Serial Bus VCCI Voluntary Control Council for Interference	ANSI	American National Standards Institute
CMOS Complementary Metal-oxide-semiconductor D2D DC-to-DC EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I**C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-voltage Protection OVP Over-voltage Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory <	BMC	Baseboard Management Controller
D2D DC-to-DC EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I'C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UNAT Universal Seynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	BIOS	Basic Input/Output System
EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I'C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Sugnificant SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UNIC Universal Serial Bus VCCI Voluntary Control Council for Interference	CMOS	Complementary Metal-oxide-semiconductor
FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I*C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Extended PFC Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Universal Serial Bus VCCI Voluntary Control Council for Interference	D2D	DC-to-DC
FRB Fault Resilient Boot FRU Field Replaceable Unit FRU Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	EMP	Emergency Management Port
FRU Field Replaceable Unit I*C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ided Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	FP	Front Panel
Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	FRB	Fault Resilient Boot
LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Intercence	FRU	Field Replaceable Unit
LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Serial Bus VCCI Voluntary Control Council for Interference	I ² C	Inter-integrated Circuit bus
LESB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAMM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	LCD	Liquid Crystal Display
MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAMM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	LPC	Low-pin Count
MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	LSB	Least Significant Bit
MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Serial Bus VCCI Voluntary Control Council for Interference	MSB	Most Significant Bit
NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	MTBF	Mean Time Between Failure
NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	MTTR	Mean Time to Repair
OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	NIC	Network Interface Card
OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	NMI	Non-maskable Interrupt
PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	OTP	Over-temperature Protection
PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	OVP	Over-voltage Protection
PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	PCI	Peripheral Component Interconnect
PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	PCB	Printed Circuit Board
PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	PCle*	Peripheral Component Interconnect Express*
POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	PCI-X	Peripheral Component Interconnect Extended
PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	PFC	Power Factor Correction
RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	POST	Power-on Self Test
RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	PSU	
SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	RAM	·
SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference		
SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	SCA	
THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	SDR	Sensor Data Record
UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference	SE	Single-Ended
USB Universal Serial Bus VCCI Voluntary Control Council for Interference	THD	Total Harmonic Distortion
VCCI Voluntary Control Council for Interference		Universal Asynchronous Receiver Transmitter
•	USB	
VSB Voltage Standby	VCCI	Voluntary Control Council for Interference
	VSB	Voltage Standby

Reference Documents

See the following documents for additional information:

- Intel[®] Server Board S2400BB Technical Product Specification
- Intel® Server Board S2400BB Product Family Spares/Parts List and Configuration Guide
- Intel[®] Server System R1000BB Service Guide
- Intel[®] Server System R1000BB Quick Installation Guide
- BIOS for EPSD Platforms Based on Intel® Xeon Processor E5-4600/2600/2400/1600 Product Families
 External Product Specification
- EPSD Platforms Based On Intel Xeon® Processor E5 4600/2600/2400/1600 Product Families BMC Core Firmware External Product Specification
- SmaRT & CLST Architecture on "Romley" Systems and Power Supplies Specification (Doc Reference # 461024)
- Intel Integrated RAID Module RMS25PB080, RMS25PB040, RMS25CB080, and RMS25CB040 Hardware Users Guide
- Intel® Remote Management Module 4 Technical Product Specification
- Intel® Remote Management Module 4 and Integrated BMC Web Console Users Guide