



Monthly Specification Update

Intel® Server Boards S5500HV

Intel® Server System SR1670HV



Intel Order Number E77965-001

July, 2009

Enterprise Platforms and Services Marketing

Revision History

Date	Modifications
July 2009	Initial release.

Disclaimers

The Intel Products Specified may contain design defects or errors known as errata that may cause the products to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

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Preface

This document is an update to the specifications contained in the *Intel® Server Boards S5500HV and Intel® Server System SR1670HV Technical Product Specification* (Order Number E69391). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain specification changes, specification clarifications, errata, and document changes.

Refer to the *Intel® Xeon® Processor 5500 Series Specification Update* (Order Number 321324) for specification updates concerning the Intel® Xeon® Processor 5500 Series. Items contained in the *Intel® Xeon® Processor 5500 Series Specification Update* that either do not apply to the *Intel® Server Boards S5500HV and Intel® Server System SR1670HV* or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Refer to the *Intel® 5520 and Intel® 5500 Chipsets I/O Hub (IOH) Specification Update* (Order Number 313069) for specification updates concerning the *Intel® 5520 and Intel® 5500 Chipsets I/O Hub (IOH)*. Items contained in the *Intel® 5520 and Intel® 5500 Chipsets I/O Hub (IOH) Specification Update* that either do not apply to the *Intel® Server Boards S5500WB and S5500WB12V* or have been worked around are noted in this document. Otherwise, it should be assumed that any chipset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Refer to the *Intel® I/O Controller Hub 10 (ICH10) Family Specification Update* (Order Number 319974) for specification updates concerning the *Intel® I/O Controller Hub 10 (ICH10) Family*. Items contained in the *Intel® I/O Controller Hub 10 (ICH10) Family Specification Update* that either do not apply to the *Intel® Server Boards S5500HV and Intel® Server System SR1670HV* or have been worked around are noted in this document. Otherwise, it should be assumed that any chipset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

- **Specification Changes** are modifications to the current published specifications for Intel® server boards. These changes will be incorporated in the next release of the specifications.
- **Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
- **Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
- **Errata** are design defects or errors. Errata may cause the server board behavior to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

Product Scope

Below are the specific boards, BIOS and components covered by this update:

Product Code	Baseboard PBA Revision	BIOS Revision	BMC Revision	Change Description (PCN#)
S5500HV	E68256-101	0110	1.13	Product Launch
SR1670HV	E68256-101	0110	1.13	Product Launch

Summary Tables of Changes

The following tables provide an overview of known errata and known document changes that apply to the specified Intel Server Products. The tables use the following notations:

Doc: Intel intends to update the appropriate documentation in a future revision.

Fix: Intel intends to correct this erratum.

Fixed: This erratum has been corrected.

NoFix: There are no plans to correct this erratum.

Shaded: This item is new or has been modified from the previous specification update.

Table 1. Errata Summary

No.	Plans	Description of Errata
1.	Fix	User can not use IPMI command to modify the BMC username of "admin"
2.	Fix	LAN 1 & LAN 3 cannot be pinged successfully when a specific configuration is enabled
3.	No Fix	The ICTS (IPMI v2.0 Conformance Test Suite) fails the "Set Lan configuration parameters" item when run
4.	Fix	The chassis Hard Disk Drive (HDD) fault LED function is disabled when the Intel Matrix RAID is enabled

Table 2. Documentation Changes

No.	Plans	Document Name	Description of Documentation Change
1.	Fix	TPS	One power connector pin-outs definition in TPS is not correct

Following are in-depth descriptions of each erratum / documentation change indicated in the tables above. The errata and documentation change numbers referenced in the following sections correspond to the numbers in the tables above.

Errata

1. User can not use IPMI command to modify the BMC username of "admin"

Problem	When using Set User Name Command to set the name of the default username "admin", the BMC will return 0xCC which means "Invalid data field in Request" as completion code.
Implication	Access to the BMC through the IPMI command will require the use of the default username, "admin."
Status	This issue may be fixed in future revision of the firmware (F/W).
Workaround	None.

2. LAN 1 & LAN 3 cannot be pinged successfully when a specific configuration is enabled

Problem	<p>On-board network connections LAN 1 and LAN 3 cannot be successfully pinged under specific configurations. Those conditions are as followed:</p> <ul style="list-style-type: none">▪ Network configuration in web interface (GUI) is set to "Both"▪ LAN 3 is configured for Static IP mode▪ LAN 1 is linked while LAN 3 is not linked <p>LAN 3 may encounter the same issue even when LAN 1 is not linked.</p>
Implication	Limitation as a result of this errata will prevent LAN 1 and LAN 3 from successfully being pinged when configured with the settings and conditions provided above
Status	This issue may be fixed in future revision of the firmware (F/W).
Workaround	Please don't meet above three configuration at same time and then Lan will be pinged successfully

3. The ICTS (IPMI v2.0 Conformance Test Suite) fails the “Set Lan configuration parameters” item when run

Problem The ICTS fails the “Set LAN Configuration Parameters” when used by the test suite.

Implication The latest ICTS version will report failure on the “Set LAN Configuration Parameters” item, It is a false failure and caused by ICTS tool limitation.

Status No Fix.

Workaround Modify the two ICTS tcl scripts, then the ICTS will pass completely:

```
/ICTS602/tests/ICTS_tests/Get_LAN_Configuration_Parameters.tcl  
/ICST602/tests/ICTS_tests/LAN/lan_lib_mod.tcl  
Set the Parameter#4(IP Address Source) to 0x01 before modifying  
Parameter#3 & Parameter#6.
```

IPMI spec:
Parameter#3 IP Address

Parameter#4 IP Address Source
0x00 = unspecified
0x01 = static address
0x02 = address obtained by BMC running DHCP (default)

Parameter#6 Subnet Mask

4. The chassis Hard Disk Drive (HDD) fault LED function is disabled when the Intel Matrix RAID is enabled

Problem When using Intel Matrix RAID the hard drive fault LED functionality is disabled.

Implication There is no HDD failure indicator when enable Intel Matrix RAID

Status This issue may be fixed in future revision of the system BIOS.

Workaround None.

Documentation Changes

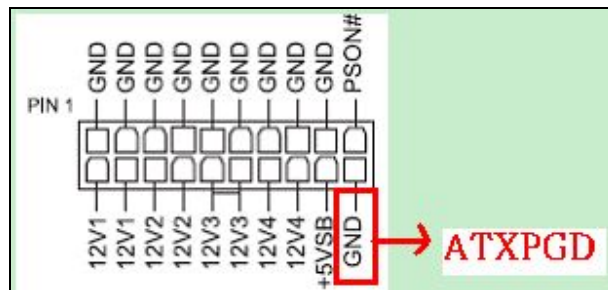
1. One power connector pin-outs definition in TPS is not correct

Problem

One power connector pin-outs definition is not correct,

Implication

Please refer below revision



Status

This correction will be implemented in next TPS revision 1.1.