Intel® Telco and Industrial Grade Server TIGPR2U

Technical Product Specification

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Revision History

Date	Revision Number	Modifications
May, 2003	0.6	Initial release for external review
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December, 2004	1.1	Miscellaneous updates

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1. Introduction

This document provides an overview of the Intel® Telco/Industrial Grade Server TIGPR2U.

1.1 Document Structure and Outline

This document is organized into the following chapters:

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Provides an overview of this document.

Chapter 2: System Overview
Provides an overview of the Intel® Telco/Industrial Grade Server TIGPR2U hardware.

Chapter 3: Cables and Connectors
Describes the cables and connectors used to interconnect the system board set and the server system components.

Chapter 4: Intel® Server Board SE7501WV2 Functional Architecture

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Chapter 7: BIOS

Chapter 8: Intel® Server Board SE7501WV2 ACPI Implementation

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Describes the specifications of the front panel/SCSI backplane board.

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Describes the specifications of the CDROM/Floppy interface board.

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Describes the specifications of the AC power subsystem.

Chapter 15: Regulatory Specifications
Describes system compliance to regulatory specifications.

2. System Overview

This chapter describes the features of the Intel® Telco/Industrial Grade Server TIGPR2U chassis.

2.1 System Features

The following table provides a list and brief description of the features of the Intel® Telco/Industrial Grade Server TIGPR2U.

Table 1. Intel® Telco/Industrial Grade Server TIGPR2U Feature List

Feature	Description	
Compact, high-density system	Rack-mount server with a height of 2U (3.5 inches) and a depth of 20.0 inches	
Configuration flexibility	1 or -2 way CPU capability in low profile and cost/value effective packaging Stand-alone system Support for the Intel® Xeon™ processor 2.4 GHz	
Serviceability	Back access to hot-swap power supplies Front access to hot swap disk drives Front access to blind-mate CDROM or Floppy Carrier Module	
Availability	Two hot-swap power supplies in a redundant (1+1) configuration Zero Channel RAID ready (requires Intel® SRCMRU PCI adapter) to provide RAID 1 capability using two hot-swap SCSI disk drives.	
Manageability	Remote management Emergency management port (Serial and LAN) IPMI 1.5 compliant Remote diagnostics support	
Upgradeability and investment protection	Designed to support Intel® Xeon™ processor family Multi-generational chassis	
System-level scalability	12 GB DDR266 Registered SDRAM DIMM memory support Dual Intel® Xeon™ processor support 3 Full Height Full Length 3.3V 64-bit x 66/100 MHz PCI Slots* OR 3 Full Height Full Length 5V 64-bit x 33 MHz PCI Slots 3 Low Profile / Half Length 64-bit x 66/100 MHz PCI Slots* 2 internal hot-swap SCSI disk drives (SCA support) 1 Low Profile CD-ROM or 1 Low Profile floppy drive * PCI speed is configuration-dependent – see Intel® Server Board SE7501WV2 section	
Front panel	Power switch Reset switch NMI switch ID switch Main power LED HDD activity LED NIC activity LED ID LED	Hard Drive 1 Fault LED Hard Drive 2 Fault LED Telco power alarm fault LED/Relay Telco critical alarm fault LED/Relay Telco major alarm fault LED/Relay Telco minor alarm fault LED/Relay

2.2 Chapter Structure and Outline

This chapter is organized into the following sections. The content of each section is summarized as follows.

Section 2.3: Introduction
Provides an overview and block diagram of the Intel® Telco/Industrial Grade Server TIGPR2U.

Section 2.4: External Chassis Features
Describes features of the Intel® Telco/Industrial Grade Server TIGPR2U chassis in detail (e.g., buttons, switches, bezel, etc.).

Section 2.5: Internal Chassis Features
Provides an overview of the components of the Intel® Telco/Industrial Grade Server TIGPR2U.

Section 2.6: Server Management
Describes the server management features of the Intel® Telco/Industrial Grade Server TIGPR2U.

Section 2.7: Specifications
Summarizes the environmental and physical specifications of the Intel® Telco/Industrial Grade Server TIGPR2U.

2.3 Introduction

The Intel® Telco/Industrial Grade Server TIGPR2U is a compact, high-density, rack mount server system with support for 1 or 2 Intel® Xeon™ processors and 12 GB DDR266 SDRAM DIMM memory. The Intel® Telco/Industrial Grade Server TIGPR2U supports high-availability features such as hot swap disk drives and hot-swap and redundant power supply modules. The scalable architecture of the Intel® Telco/Industrial Grade Server TIGPR2U supports symmetric multiprocessing (SMP) and a variety of operating systems (OS).

The following figure shows an isometric view of the system.

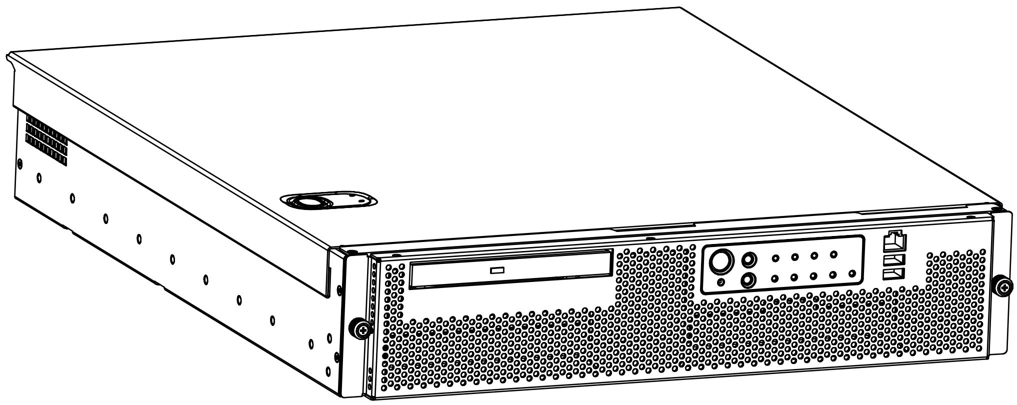
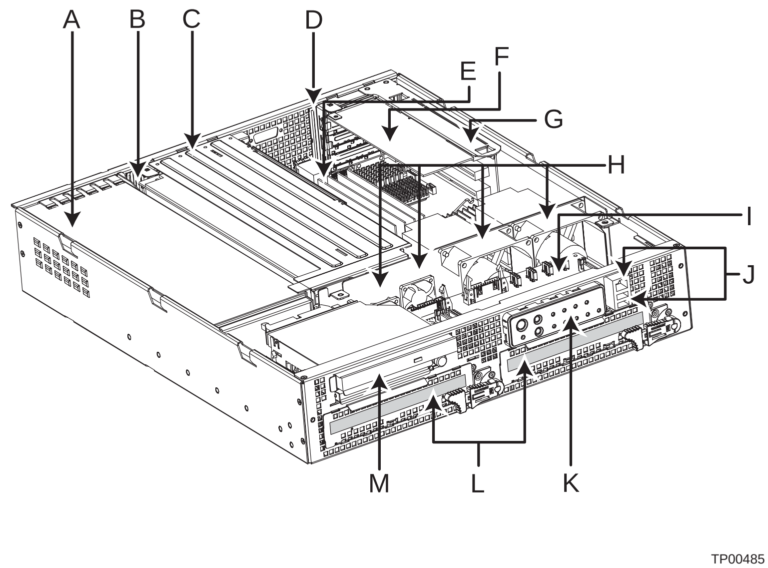


Figure 1. Isometric View of the Intel® Telco/Industrial Grade Server TIGPR2U

The Intel® Telco/Industrial Grade Server TIGPR2U uses the Intel® Server Board SE7501WV2, which contains FCPGA sockets for installing up to two Intel® Xeon™ processors. The baseboard has 6 DIMM slots and supports up to 12 GB of error checking and correcting (ECC) SDRAM memory. The Intel® Server Board SE7501WV2 also contains 6 PCI slots (implemented via riser cards), input/output (I/O) ports and various controllers.

The following figure shows the system with the top covers and front bezel removed.

Figure 2. Intel® Telco/Industrial Grade Server TIGPR2U with Top Covers and Front Bezel Removed



A. Power Supply	H. System Fans
B. PCI card bracket (full-length)	I. FPIO system board
C. Riser card assembly (full-length)	J. RJ45 COM2 and Dual USB ports
D. PCI card bracket (low-profile)	K. Control Panel
E. SE7501WV2 Server Baseboard	L. SCSI Hard Disk Drive Bays
F. PCI add-in card (accessory to system)	M. Peripheral bay (optional CD-ROM module or FDD module available)
G. Riser card assembly (low-profile)	

The Intel® Server Board SE7501WV2 is mounted horizontally toward the rear of the chassis behind the system fan array.

Up to two 1-inch Ultra-320 SCSI technology hard drives can be mounted in the hot swap drive bays located in the bottom front of the chassis. The front bezel needs to be removed to access the hot swap drive bays. Figure 2 shows the location of the two hot swap drive trays.

One peripheral drive (either a slim-line floppy drive or a slim-line CD-ROM drive) can be mounted in the system using a blind-mate peripheral drive carrier inserted into the peripheral drive bay. The peripheral drive bay is located above the hard drive tray and to the left. The blind-mate peripheral drive sheet-metal carrier for the floppy drive is different from the blind-mate peripheral drive sheet-metal carrier for the CD-ROM drive.

The Front Panel I/O (FPIO) board is located above the hard drive tray and provides user interface for the system front panel and for system management as well as SCSI backplane connectivity for the hot swap drives.

The power supply cage (both AC-input and DC-input options are available) is mounted at the left-rear of the chassis and supports up to two hot-swap 470W DC or 480W AC power supply modules in a 1 + 1 redundant configuration. A filler module for the empty power supply location is supplied for systems without redundancy. The power supply modules and filler modules are specific to either the AC or DC power supply cages.

The system contains a fan array consisting of two 80 x 38mm fans and two 40 x 28mm fans to cool the Intel® Server Board SE7501WV2 and other components. The fans are installed directly behind the drive bays and are located in front of the baseboard. Individual fan connectors are located on the FPIO board. A fan failure is indicated by one of the fault light-emitting diodes (LEDs) located on the FPIO board.

The front bezel can be customized to meet OEM industrial design requirements. The bezel design allows adequate airflow to cool the system components. The front bezel is removed to access the drive tray. The front bezel also supports an air filter.

The following figure shows a block diagram of the Intel® Telco/Industrial Grade Server TIGPR2U with interconnections.

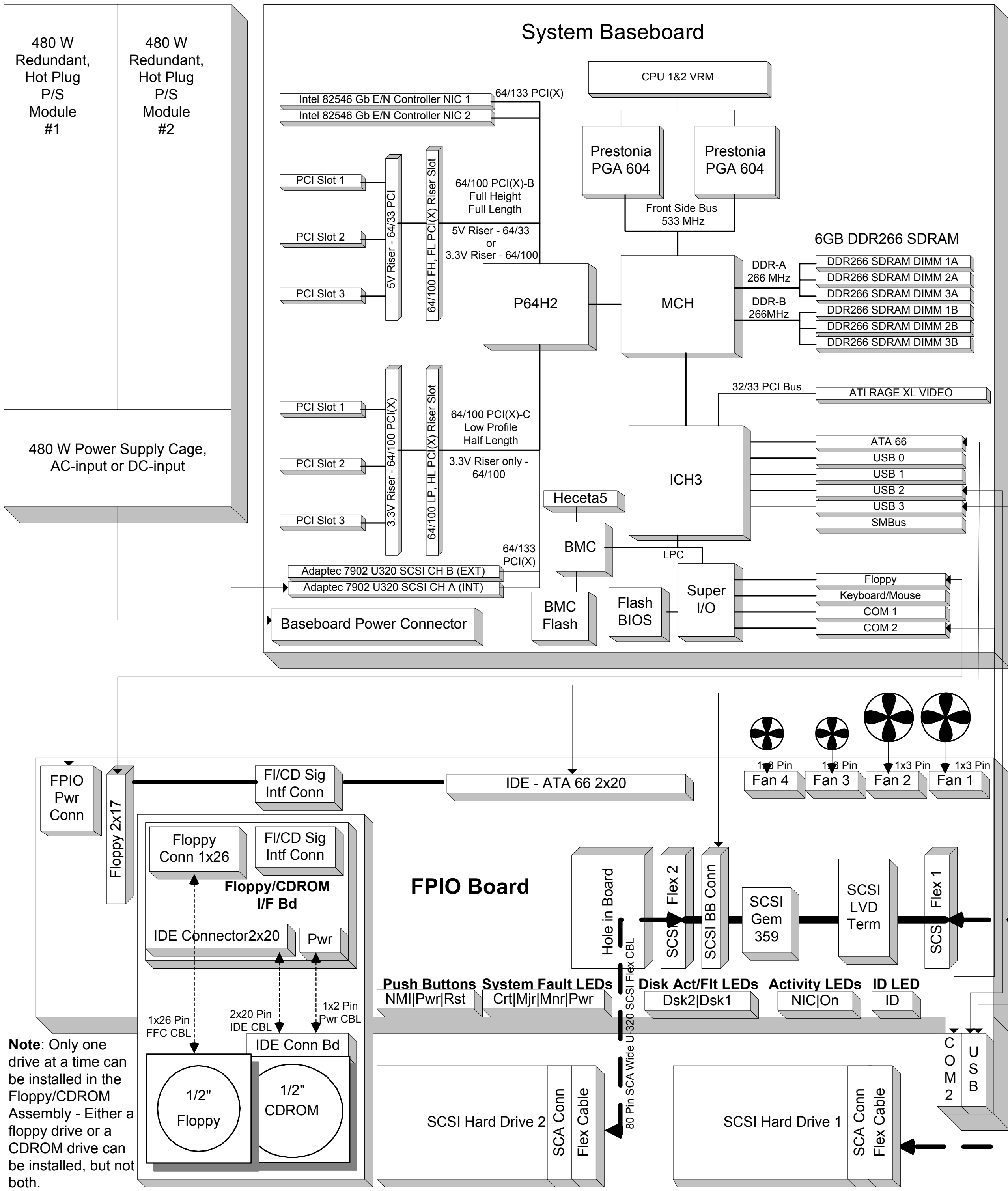


Figure 3. Intel® Telco/Industrial Grade Server TIGPR2U Block Diagram

2.4 External Chassis Features

2.4.1 Front View of Chassis

Figure 4 shows the front view of the system. Figure 5 shows the front view of the system with the front bezel removed. Removing the front bezel provides access to the two hot-plug hard drive bays. Removing the front bezel also provides access to the peripheral bay.

Both areas are described in detail in the following sections.

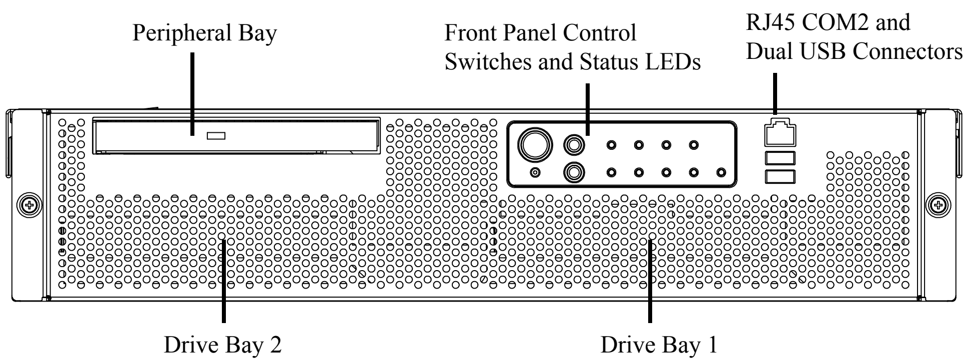


Figure 4. Front View of System

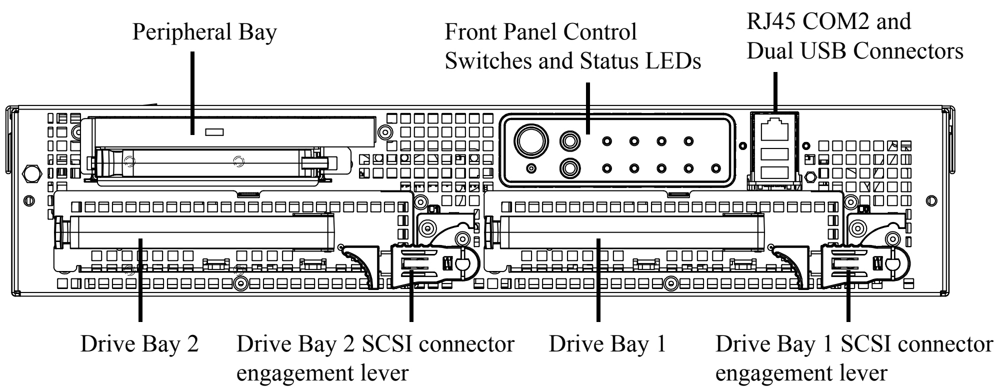


Figure 5. Front View of System (shown with bezel removed)

2.4.2 Front Panel

The front panel features are shown in Figure 6 and described in Table 2. All front panel control switches and status LEDs are contained on the FPIO system board. Please refer to Section 5, "FPIO System Board," for a detailed description of the control switches and status LEDs contained on the front panel.

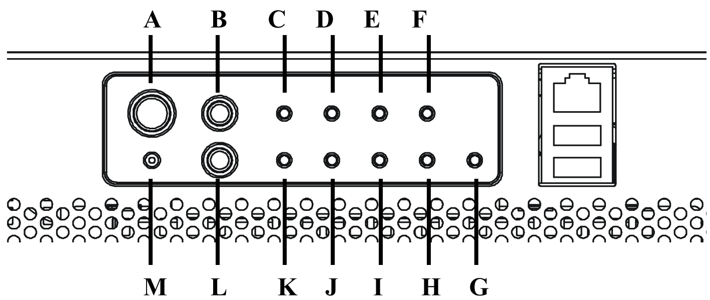


Figure 6. Front Panel Details

Table 2. Front Panel Features

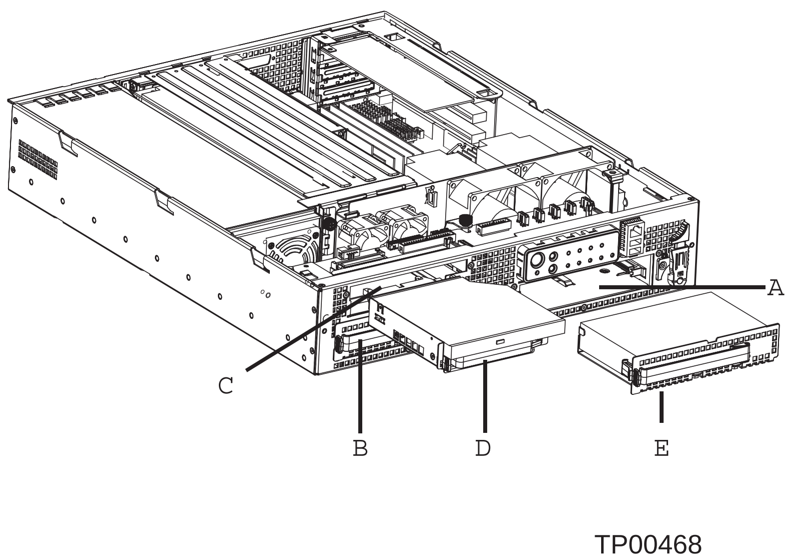
Item	Feature	Description
Front Panel Switches		
A	Power switch	Toggles the system power
B	Reset switch	Resets the system
L	ID switch	Toggles system ID LED
M	NMI switch	Assert NMI to baseboard
Front Panel Alarm LEDs and Relays		
C	Critical (amber)	When continuously lit, indicates the presence of a Critical System Fault. A critical system fault is an error or event that is detected by the system with a fatal impact to the system. In this case, the system cannot continue to operate. An example could be the loss of a large section of memory, or other corruption, that renders the system not operational. The front panel critical alarm relay will be engaged.
D	Major (amber)	When continuously lit, indicates the presence of a Major System Fault. A major system fault is an error or event that is detected by the system that has discernable impact to system operation. In this case, the system can continue to operate but in a "degraded" fashion (reduced performance or loss of non-fatal feature reduction). An example could be the loss of one of two mirrored disks. The front panel major alarm relay will be engaged.
E	Minor (amber)	When continuously lit, indicates the presence of a Minor System Fault. A minor system fault is an error or event that is detected by the system but has little impact to actual system operation. An example would be a correctable ECC error. The front panel minor alarm relay will be engaged.
F	Power (amber)	When continuously lit, indicates the presence of a Power System Fault. The front panel power alarm relay will be engaged.
Front Panel Status LEDs		
G	Disk 1 Activity/Fault LED (green/amber)	Indicates disk 1 SCSI hard drive activity when green, or a disk 1 SCSI hard drive fault when amber

H	Disk 2 Activity/Fault LED (green/amber)	Indicates disk 2 SCSI hard drive activity when green, or a disk 2 SCSI hard drive fault when amber.
I	Main power LED (green)	When continuously lit, indicates the presence of DC power in the server. The LED goes out when the power is turned off or the power source is disrupted.
J	NIC0/NIC1 activity LED (green)	Indicates activity on either NIC0 or NIC1.
K	System ID LED (white)	Used to help locate a given server platform requiring service when installed in a multi-system rack.

2.4.3 Chassis Peripheral Bay and Hard Drive Bays

The Intel® Telco/Industrial Grade Server TIGPR2U chassis provides two hot-swap hard drive bays at the front of the chassis, along with a non hot-swap blind-mate peripheral bay that supports either a floppy drive carrier or a CDROM drive carrier. Both hard drive bays may be populated with a tray-mounted 3.5” SCSI SCA hard disk drive.

Figure 7. Chassis Peripheral Bay and Hard Drive Bays



A. Hard drive bay 1
B. Hard drive bay 2
C. Peripheral drive bay
D. CD-ROM drive or floppy disk drive module
E. Hard disk drive module

2.4.3.1 Peripheral Drive Bay

The peripheral bay supports either a floppy drive carrier assembly or a CDROM drive carrier assembly. Both the blind-mate floppy drive carrier assembly and the blind-mate CDROM drive carrier assembly can be inserted or removed when the system power is off. Note that both a floppy drive and a CDROM drive cannot be installed in the system at the same time.

The floppy drive carrier assembly utilizes a 0.5” (12.7mm) slim-line 3.5” floppy drive. The CDROM drive carrier assembly utilizes a 0.5” (12.7mm) slim-line CD-ROM or DVD drive.

As shown in the following figure, the CDROM or Floppy drive carrier assembly is installed in the system, and the handle is rotated closed in the direction indicated and snapped into place to lock the drive carrier into the chassis.

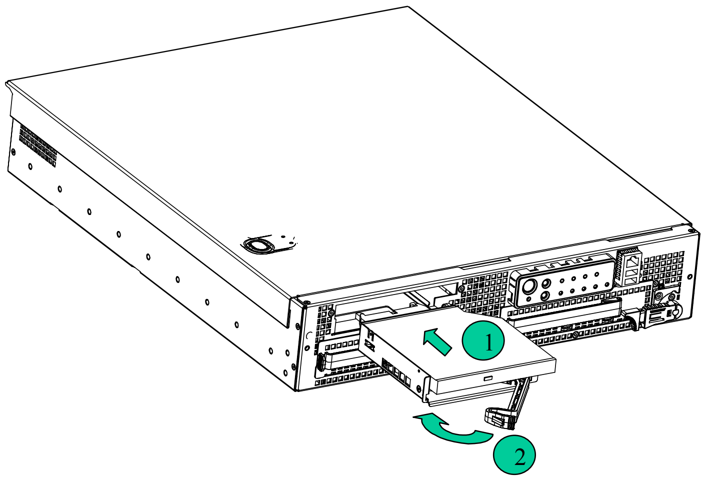
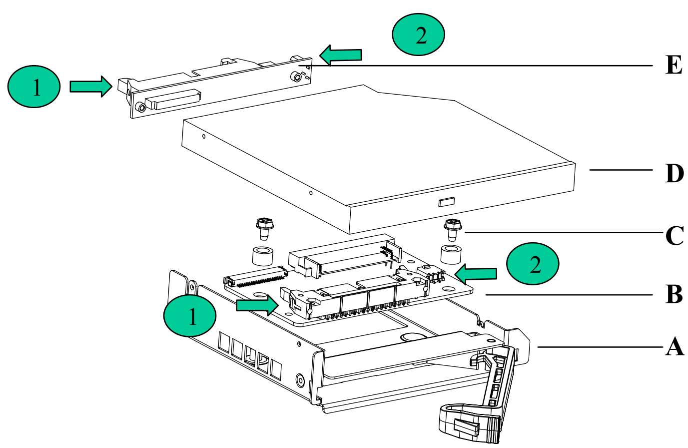


Figure 8. Peripheral Drive Bay

2.4.3.1.1 CDROM Drive Carrier Assembly

The CDROM drive is installed in a CDROM drive carrier assembly before installing it into the system. An exploded view of the CDROM drive carrier assembly is shown in the following figure.



A. CDROM drive carrier metal housing
B. CDROM drive carrier interface board
C. Two screws to connect interface board to metal housing
D. CD-ROM Drive
E. CD-ROM interface board

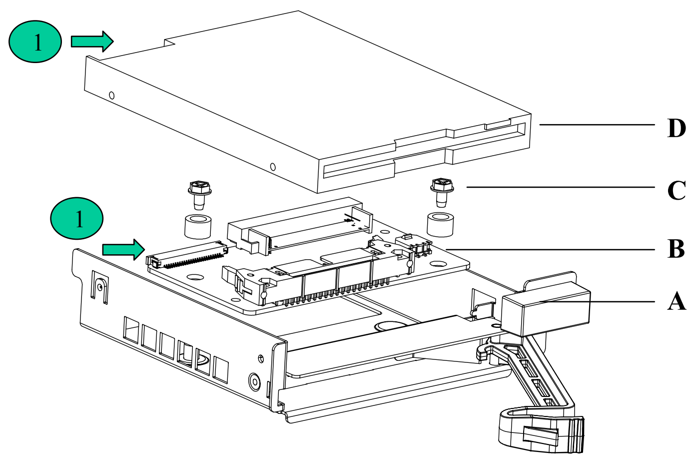
Figure 9. CDROM Drive Carrier Assembly

Two cables are required to connect between the CDROM drive carrier interface board (B) and the CD-ROM interface board (E). An IDE cable is used to connect between the 2x20 IDE connector on both these interface boards as indicated in (1). A 1x2 power cable is used to connect between the power connector on both of these interface boards as indicated in (2).

The CD-ROM drive carrier assembly inserts into the peripheral bay on the front of the system. The mating connectors on the CD-ROM drive carrier assembly and the FPIO board are blind-mate style connectors, and will seat fully when the rotating handle on the CD-ROM drive carrier assembly is snapped into place in the chassis.

2.4.3.1.2 Floppy Drive Carrier Assembly

The floppy drive is installed in a Floppy drive carrier assembly before installing it into the system. An exploded view of the Floppy drive carrier assembly is shown in the following figure.



A. Floppy drive carrier metal housing
B. Floppy drive carrier interface board
C. Two screws to connect interface board to metal housing
D. Floppy Drive

Figure 10. Floppy Drive Carrier Assembly

One FFC cable is required to connect between the Floppy drive carrier interface board (B) and the Floppy drive (D) as indicated by (1). This FFC cable has a keying feature that allows it to be inserted correctly in only one orientation.

The Floppy drive carrier assembly inserts into the peripheral bay on the front of the system. The mating connectors on the Floppy drive carrier assembly and the FPIO board are blind-mate, and will seat fully when the rotating handle on the Floppy drive carrier assembly is snapped into place in the chassis.

2.4.3.2 Hard Drive Bays

There are two hard drive bays in the system (see (1) and (2) in Figure 11). Each hard drive bay supports a tray-mounted U320 SCSI disk drive with SCA (single connector attach) interconnect. The drive tray is installed into the front of the chassis in the hard drive bay, and then secured in place by pushing in the handle on the drive tray. A small lever on the front of the system is then rotated into the horizontal position to connect the SCA connector on the system flex circuit SCSI cable to the SCA connector on the drive. Ultra 320 SCSI technology (SCA interconnect) or slower hard disk drives can be installed in this hard drive tray. The hard drive bays are designed to accept 15,000 RPM (and below) hard drives that consume up to 18 W of power.

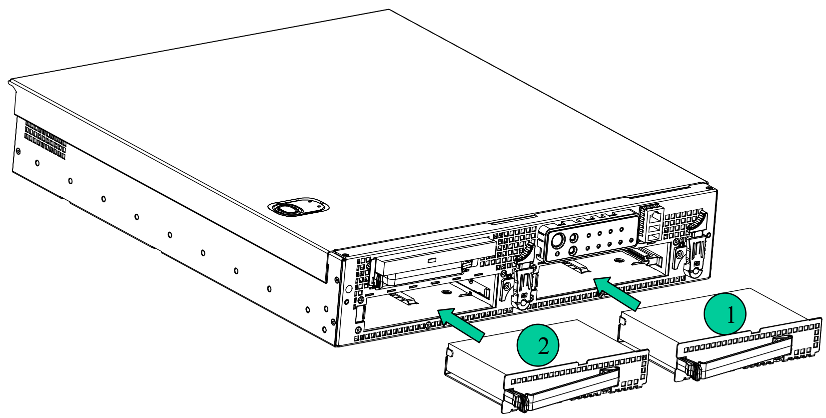


Figure 11. SCSI Hard Drive Bays

2.4.3.2.1 Hard Drive Tray

Each hard drive used in the system must be mounted to a drive tray using four screws inserted into the bottom of the drive as shown in the following figure.

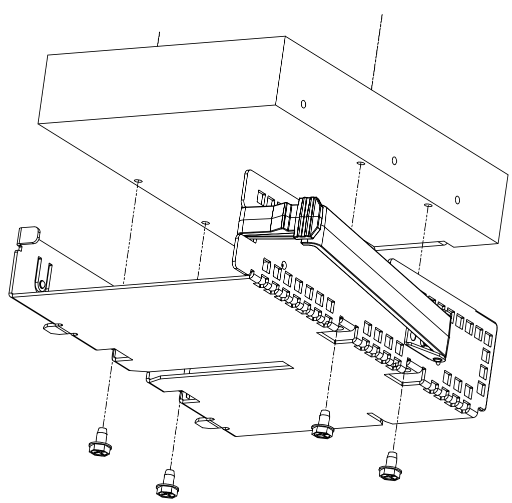


Figure 12. SCSI Hard Drive Tray

2.4.4 Rear View of Chassis

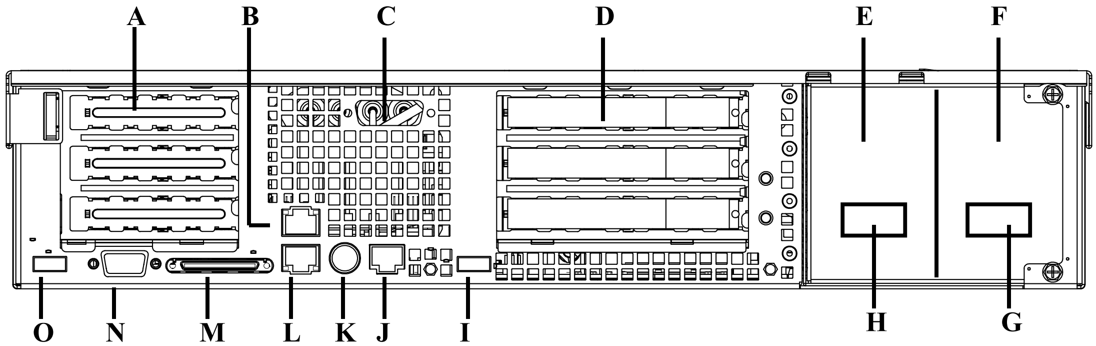


Figure 13. Rear View of DC System

Table 3. System Features - Rear

Item	Description
A	PCI card bracket (low profile)
B	RJ45 NIC 2 connector - Green Status LED / Yellow Status LED
C	DB15 Alarm Connector
D	PCI card bracket (full-height)
E	Power supply module, primary
F	Power supply module, redundant (system accessory)
G	DC power input (redundant)
H	DC power input (primary)
I	USB connector 1
J	RJ45 serial 2 port
K	PS/2 mouse/keyboard connector – requires dongle (“Y” cable) to connect both keyboard and mouse
L	RJ45 NIC 1 connector
M	U320 SCSI connector
N	Video connector
O	USB connector 0

2.5 Internal Chassis Features

2.5.1 Intel® Server Board SE7501WV2

The Intel® Server Board SE7501WV2 is a monolithic printed circuit board that can accept one or two Intel® Xeon™ processors using the Socket 604 INT3/ FCPGA package. The following figure shows the functional blocks of the Intel® Server Board SE7501WV2 and the plug-in modules that it supports.

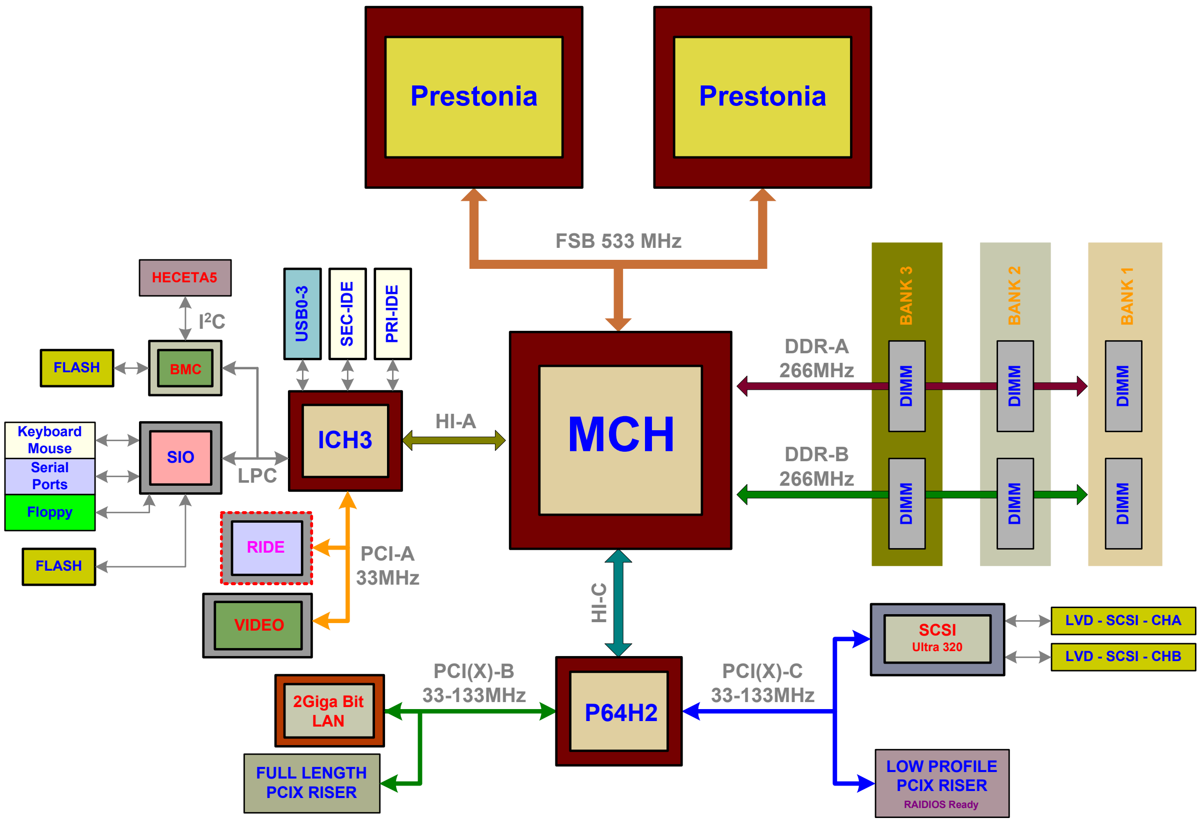


Figure 14. Intel® Server Board SE7501WV2 Block Diagram

- Dual Intel® Xeon™ processors in the Socket 604 INT3/FCPGA package
- 533 MHz Front Side Bus
- Intel® E7501 chipset
  - E7501 North Bridge
  - P64H2 I/O Bridge
  - ICH3-S South Bridge
- Support for up to six DDR266 compliant registered ECC DIMMs providing up to 12 GB of memory using 2G DIMMs.
- Three separate and independent PCI buses:
  - Segment A: 32-bit, 33 MHz, 5 V (P32-A) with one embedded device:
    - ➢ 2D/3D graphics controller: ATI* Rage XL Video Controller with 8 MB of memory.

- Segment B: 64-bit, 100 MHz, 3.3 V, PCI-X (P64-B) supporting the following configuration:
  - ➢ One PCI I/O riser slot capable of supporting full length PCI add-in cards
  - ➢ Dual-channel Intel® 10/100/1000 82546EB Gigabit Ethernet Controller
- Segment C: 64-bit, 100 MHz, 3.3 V PCI-X (P64-C) supporting the following device:
  - ➢ One PCI I/O riser slot capable of supporting low-profile PCI add-in cards
  - ➢ Dual-channel Adaptec* 7902 U320 SCSI Controller
  - ➢ RAID (Zero Channel RAID) support.

- LPC (Low Pin Count) bus segment with two embedded devices:
  - Baseboard Management Controller (BMC) providing monitoring, alerting, and logging of critical system information obtained from embedded sensors on the server board
  - Super I/O controller chip providing all PC-compatible I/O (floppy, serial, keyboard, mouse)
- X-Bus segment with one embedded device:
  - Flash ROM device for system BIOS: Intel® 32-megabit 28F320C3 Flash ROM
- Two external Universal Serial Bus (USB) ports with an additional internal header providing two optional USB ports for front panel support
- One external low-profile RJ45 serial 2 port. An internal header is also available providing an optional serial 1 port.
- One IDE connector, supporting one or two ATA-100 compatible devices
- Support for up to four system fans
- Fault/Status LEDs throughout the server board
- Multiple server management headers providing on-board interconnects to server management features
- SSI-compliant connectors for SSI interface support: front panel, floppy, and ATA-33

2.5.2 Segment B Full-Height, Full-Length PCI Adapter Subsystem

A three-slot PCI adapter assembly that supports both full-height/full-length and full-height/half-length PCI adapters is installed in the segment B PCI riser slot located in the middle of the Intel® Server Board SE7501WV2. This PCI adapter assembly is configured and installed as shown in the following figure. After the PCI adapter assembly is removed from the system, it is configured with PCI adapters by plugging the PCI adapters into the PCI connectors on the riser card (either a 3.3V riser card or a 5V riser card) integrated into the PCI adapter assembly. The PCI adapter assembly is then installed into the system by plugging the riser card into the riser card connector on the Intel® Server Board SE7501WV2. In addition, it is necessary to make sure that the interlocking metal tabs on the back of the PCI adapter assembly are correctly inserted into the slots in the back of the chassis. Refer to the Intel® Server Board SE7501WV2 specification for electrical characteristics for this PCI adapter subsystem.

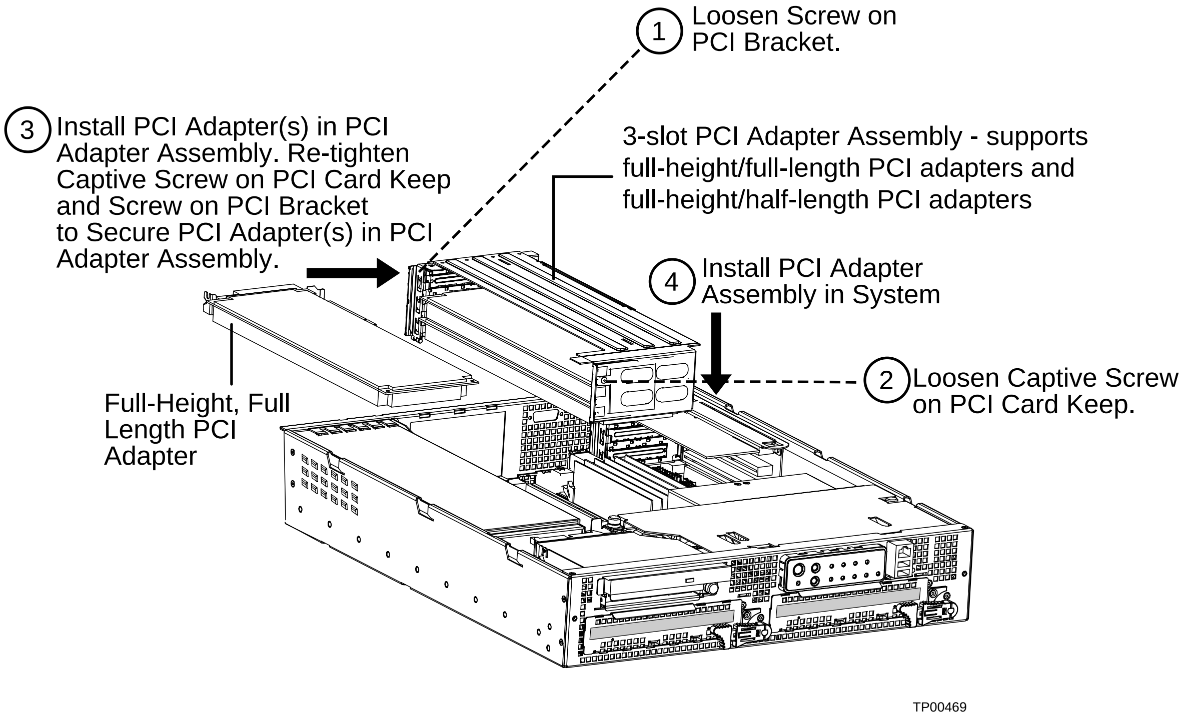


Figure 15. Segment B Full-Height, Full-Length PCI Adapter Subsystem

The following table shows the maximum PCI bus speed achievable on PCI Bus Segment B. The slowest PCI adapter installed in the PCI Adapter Subsystem will determine the bus speed.

Table 4. Segment B PCI Bus Maximum Speed Table

Configuration	Bus B with Anvik Dual NIC and 3.3V Riser	Bus B with Anvik Dual NIC and 5V Riser
0 Adapter Cards installed and on board device enabled	PCI-X 64/100	PCI-X 64/33
1 Adapter Card installed and on board device enabled	PCI-X 64/100	PCI-X 64/33
2 Adapter Cards installed and on board device enabled	PCI-X 64/66	PCI-X 64/33
3 Adapter Cards installed and on board device enabled	PCI-X 64/66	PCI-X 64/33
1 Adapter Card installed and on board device disabled	PCI-X 64/100	PCI-X 64/33
2 Adapter Cards installed and on board device disabled	PCI-X 64/66	PCI-X 64/33
3 Adapter Cards installed and on board device disabled	PCI-X 64/66	PCI-X 64/33

2.5.3 Segment C Low Profile, Half-Length PCI Adapter Subsystem

A three-slot PCI adapter assembly that supports only low profile, half-length PCI adapters is installed in the segment C PCI riser slot located on the right side of the Intel® Server Board SE7501WV2. This PCI adapter assembly is configured and installed as shown in the following figure. After the PCI adapter assembly is removed from the system, it is configured with PCI adapters by plugging the PCI adapters into the PCI connectors on the 3.3V riser card that is part of the PCI adapter assembly. The PCI adapter assembly is then installed into the system by plugging the riser card into the riser card connector on the Intel® Server Board SE7501WV2. Refer to the Intel® Server Board SE7501WV2 specification for electrical characteristics for this PCI adapter subsystem.

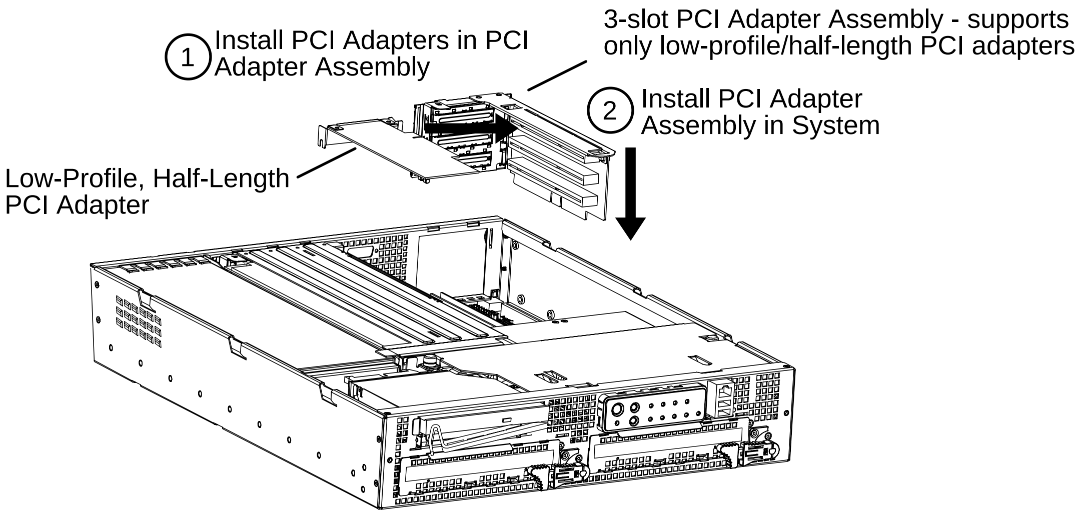


Figure 16. Segment C Low Profile, Half-Length PCI Adapter Subsystem

The following table shows the maximum PCI bus speed achievable on PCI Bus Segment C. The slowest PCI adapter installed in the PCI Adapter Subsystem will determine the bus speed.

Table 5. Segment C PCI Bus Maximum Speed Table

Configuration	Bus C with AIC7902* SCSI and 3.3V Riser
0 Adapter Cards installed and on board device enabled	PCI-X 64/100
1 Adapter Card installed and on board device enabled	PCI-X 64/100
2 Adapter Cards installed and on board device enabled	PCI-X 64/100
3 Adapter Cards installed and on board device enabled	PCI-X 64/66
1 Adapter Card installed and on board device disabled	PCI-X 64/100
2 Adapter Cards installed and on board device disabled	PCI-X 64/100
3 Adapter Cards installed and on board device disabled	PCI-X 64/66

2.5.4 Power Subsystem

The Intel® Telco/Industrial Grade Server TIGPR2U can be configured with either an AC-input power subsystem or a DC-input power subsystem. The power supply modules are located in the power supply cage, which is mounted at the left rear of the chassis. The power supply modules used in the AC-input power subsystem cannot be used in the DC-input subsystem, and the power supply modules used in the DC-input power subsystem cannot be used in the AC-input power subsystem. Both the AC and DC-input power subsystems may contain up to two power supply modules and can be configured as follows:

- Two power supply modules installed, (1+1) power redundancy for maximum system load.

- One power supply module installed[1], non-redundant for maximum system load.

When the system is configured with two power supply modules, the hot-swap feature allows the user to replace a failed power supply module without interrupting system functionality. To ensure that all components remain within specification under all system environmental conditions, it is recommended that power supply module hot-swap operations not exceed two minutes in duration.

Power from the power subsystem is carried to internal system boards and peripheral devices via discrete cables. One power supply module is capable of handling the worst-case power requirements for a fully configured server system. This includes two Intel® Xeon™ processors, 12 GB of memory, two hard drives at 18 W per drive (typical worst case 3.5-inch by 1.0-inch, 15k RPM drive), and a full complement of PCI adapters.

The total power requirement for the server system exceeds the 240 VA energy hazard limit, which defines an operator-accessible area. As a result, only qualified technical individuals should access the processor, memory, and I/O areas on the SE7501WV2 System Baseboard while the system is energized.

Refer to *Section 13, "DC Power Subsystem"* or *Section 14, "AC Power Subsystem"* of this document for detailed power specifications.

2.5.5 Cooling Subsystem

2.5.5.1 Description

All system components except the power supply cage are cooled by a set of fans mounted near the middle of the chassis and behind the hard drive bays. This is shown in the following figure.

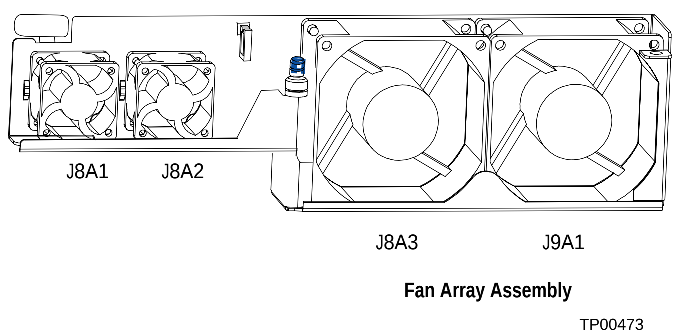


Figure 17. Fan Array with Four System Fans Installed

The Intel® Telco/Industrial Grade Server TIGPR2U comes in a non-redundant, four-fan configuration that consists of two 80mm x 38mm fans and two 40mm x 28mm fans.

Air flows in through the front bezel over the peripheral bay and the hard drive bays, passes through the fans and over the baseboard, and exhausts through the rear of the chassis. Each

[1] Proper power subsystem cooling by the power subsystem fan requires the population of both (power supply bay) receptacles either by a power supply module or a filler panel.

fan provides tachometer signal output to the Intel® Server Board SE7501WV2 to indicate a fan failure.

2.5.5.2 Ambient Temperature Control

The Intel® Server Board SE7501WV2 contains a pulse-width-modulation (PWM) circuit, which cycles the 12 VDC fan voltage to provide quiet operation when system ambient temperature is low and there are no fan failures. Under normal room ambient conditions (less than 24°C) the fan power circuit supplies an effective fan voltage of 6.0 VDC. When the room ambient temperature exceeds 24°C, the fan control circuit provides increased voltage levels to increase the speed of the fan. There are sixteen fan speed increments between 24°C and 40°C. At 40°C the fans operate at their maximum speed to provide maximum airflow.

2.5.5.3 Cooling Summary

The four-fan cooling subsystem is sized to provide cooling for:

- Up to two processors
- 12 GB of SDRAM memory
- Two 15,000 RPM hard drives at a maximum of 18W per drive
- 6 PCI cards

The cooling subsystem is designed to meet acoustic and thermal requirements at the lower fan speed settings. At the higher fan speed settings, thermal requirements are met for the maximum ambient temperatures, but acoustic requirements are not met. The environmental specifications are summarized in Section 2.7.1.

2.6 Server Management

The Intel® Server Board SE7501WV2 server management architecture features a Baseboard Management Controller (BMC), which autonomously monitors server status and provides the interface to server management control functions. This controller is responsible for controlling system power, resets, monitoring voltages, temperatures, fans, and communicating with secondary controllers on its Intelligent Platform Management Bus (IPMB).

The functions of each controller are summarized in the following sections. The firmware for all of the controllers is field upgradeable using the *Server Management Firmware Update Utility*. Refer to the *System Server Management External Architecture Specification* for more details.

2.6.1 Baseboard Management Controller

The BMC on the Intel® Server Board SE7501WV2 provides server management monitoring capabilities. A flash memory is associated with the BMC that holds the operational code, sensor data records (SDR), and system event log (SEL). There is also a serial EEPROM that holds the BMC configuration defaults and field replaceable unit (FRU) information. The various server management functions provided by the BMC are listed as follows:

- Baseboard voltage monitoring
- Fan failure detection
- Fan speed control
- Processor voltage monitoring

- Processor presence detection
- Processor internal error (IERR) monitoring
- Fault resilient booting (FRB)
- Processor disable control
- Watchdog timer
- Periodic system management interrupt (SMI) timer
- I^2C master controller for the Intelligent Platform Management Bus (IPMB)
- Two private I^2C management bus interfaces
- Server management software (SMS) and server management mode (SMM) IPMB message receiver
- Event message receiver
- System event log (SEL) management and access
- Sensor data record (SDR) repository management and access
- Processor non-maskable interrupt (NMI) monitoring
- Processor SMI monitoring
- Time-stamp clock
- Secure mode, video blank, and floppy write protect
- Software front panel NMI generation

2.7 Specifications

2.7.1 Environmental Specifications

The Intel® Telco/Industrial Grade Server TIGPR2U has been tested to the environmental specifications as indicated in the following table. All testing was performed per procedures defined in Bellcore* GR-63-CORE NEBS Physical Protection, Bellcore GR-3580 NEBS Criteria Levels, Bellcore GR-1089-CORE EMC and Electrical Safety – Generic Criteria for Network Telecommunications Equipment, and the *Intel Environmental Standards Handbook*.

Table 6. Environmental Specifications Summary

Environment	Specification
Temperature operating	5° C to 40° C (41° F to 104° F)
Temperature non-operating	-40° C to 70° C (-104° F to 158° F)
Altitude	0 to 1,800 m (0 to 5,905 ft)
Humidity non-operating	95%, non-condensing at temperatures of 23° C (73° F) to 40° C (104° F)
Vibration operating	Swept sine survey at an acceleration amplitude of 0.1 g from 5 to 100 Hz and back to 5 Hz at a rate of 0.1 octave/minute, 90 minutes per axis on all three axes as per Bellcore* GR-63-CORE standards
Vibration non-operating	Swept sine survey at an acceleration amplitude of 0.5 g from 5 to 50 Hz at a rate of 0.1 octaves/minute, and an acceleration amplitude of 3.0 g from 50 to 500 Hz at a rate of 0.25 octaves/minute, on all three axes as per Bellcore* GR-63-CORE standard. 2.2 Grms, 10 minutes per axis on all three axes as per the *Intel Environmental Standards Handbook*
Shock operating	Half-sine 2 G, 11 ms pulse, 100 pulses in each direction, on each of the three axes as per the *Intel Environmental Standards Handbook*
Shock non-operating	Trapezoidal, 25 G, 170 inches/sec delta V, three drops in each direction, on each of the three axes as per *Intel Environmental Standards Handbook*

Environment	Specification
Safety	UL 1950, CSA 950, IEC 950, TUV/GS EN60950
Emissions	Certified to FCC Class A; tested to CISPR 22 Class A, EN 55022 Class A, VCCI Class A ITE, AS/NZS 3548 Class A
Immunity	Verified to comply with EN 50082-1
Electrostatic discharge (ESD)	Tested to ESD levels up to 15 kilovolts (kV) air discharge and up to 8 kV contact discharge without physical damage as per *Intel Environmental Standards Handbook*
Acoustic	Sound pressure: < 55 dBA at ambient temperatures < 24°C measured at bystander positions in operating mode

2.7.2 Physical Specifications

The following table describes the physical specifications of the Intel® Telco/Industrial Grade Server TIGPR2U.

Table 7. Dimensions and Weights

Height	3.45 inches (87.6 mm)
Width	17.14 inches (435.3 mm)
Depth	20 inches (510 mm)
Front clearance	2 inches (76 mm)
Side clearance	1 inches (25 mm)
Rear clearance	3.6 inches (92 mm)
2 AC PS modules, 2 HDD, CD, 2 proc., 2 DIMMS, no PCI adapters	39 pounds
1 AC power supply module, 1 AC power supply filler, 2 HDD, CD, 2 processors, 2 DIMMS, no PCI adapters	37.1 pounds
1 AC power supply module, 1 AC power supply filler, 1 HDD, CD, 2 processors, 2 DIMMS, no PCI adapters	35.7 pounds
1 AC power supply module, 1 AC power supply filler, 1 HDD, CD filler, 2 processors, 2 DIMMS, no PCI adapters	34.8 pounds
2 AC power supply modules, 2 HDD, CD filler, 2 processors, 2 DIMMS, no PCI adapters	38.2 pounds
Packaging	8.1 pounds

3. Cables and Connectors

This chapter describes interconnections between the various components of the Intel® Telco/Industrial Grade Server TIGPR2U. Also, this chapter includes an overview diagram of the Intel® Telco/Industrial Grade Server TIGPR2U interconnections, as well as tables describing the signals and pin-outs for the ½" peripheral adapter boards. Refer to the appropriate Intel® Server Board SE7501WV2 section in this document for other connector signal descriptions and pin-outs.

3.1 Chapter Structure and Outline

The information contained in this chapter is organized into four sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 3.2: **Interconnect Block Diagram**
Provides an overview of system interconnects.

Section 3.3: **Cable and Interconnect Descriptions**
Provides a list of all the connectors and cables in the system.

Section 3.4: **User-accessible Interconnects**
Describes the form-factor and pin-out of user-accessible interconnects.

3.2 Interconnect Block Diagram

The following figure shows the interconnections for all the boards used in the Intel® Telco/Industrial Grade Server TIGPR2U.

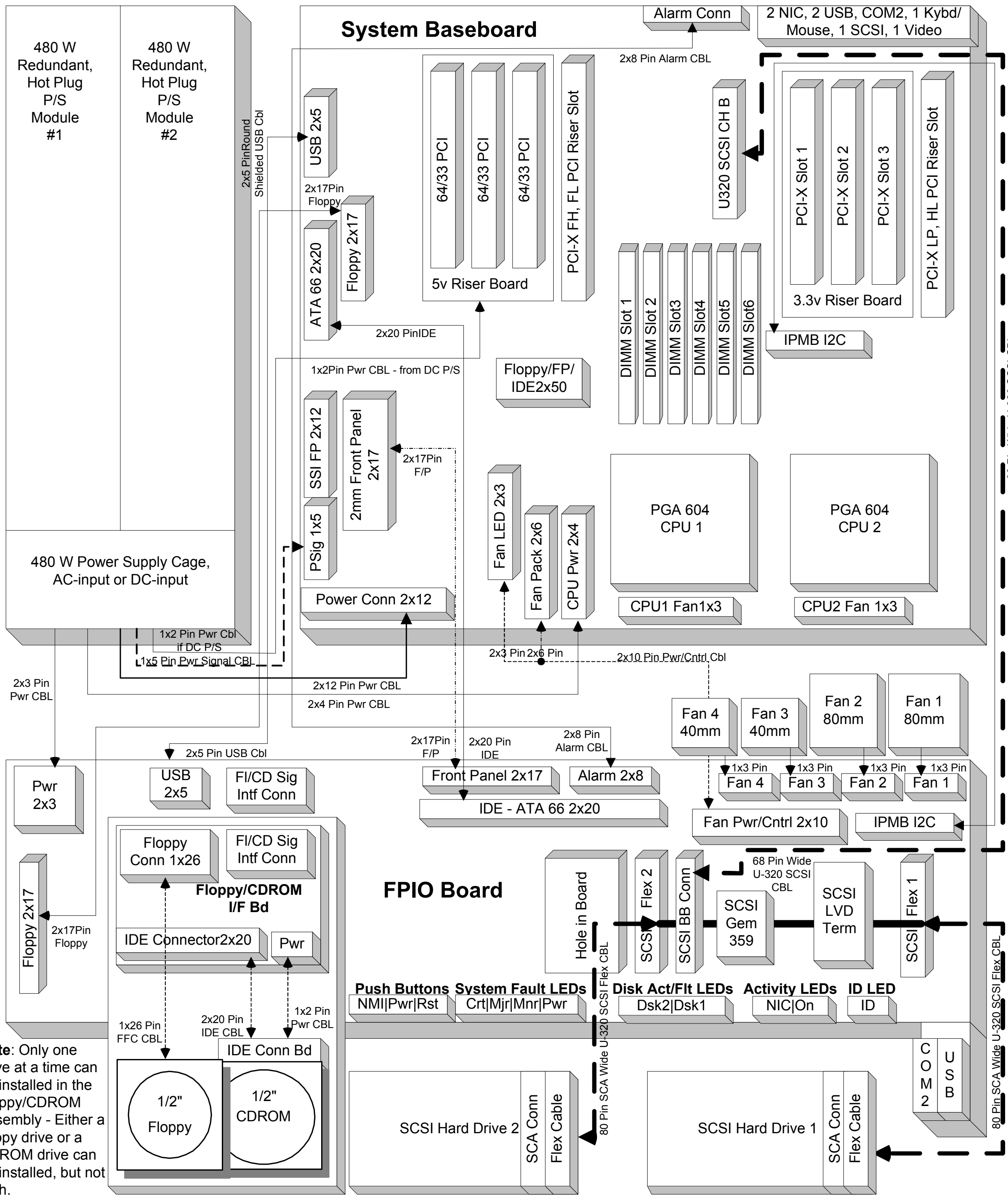


Figure 18. Intel® Telco/Industrial Grade Server TIGPR2U Interconnect Block Diagram

3.3 Cable and Interconnect Descriptions

The following table describes all cables and connectors of the Intel® Telco/Industrial Grade Server TIGPR2U.

Table 8. System Interconnect Descriptions

Intel® Server Board SE7501WV2 Connections					
Baseboard	J1J1	1x5 P/S Signal Connector	P/S Assembly	J1J1	1x5 P/S Signal Connector
Baseboard	J3J1	2x12 P/S Power Connector	P/S Assembly	J3J1	2x12 P/S Power Connector
Baseboard	J4J1	2x4 P/S Power Connector	P/S Assembly	J4J1	2x4 P/S Power Connector
Baseboard	J1G2	2x20 IDE Connector	IDE Cable	J1G2	2x20 IDE Connector
Baseboard	J1G1	2x17 Floppy Connector	Floppy Cable	J1G1	2x17 Floppy Connector
Baseboard	J7B1	68 pin SCSI Ch B Connector	SCSI BB Cbl	J7B1	68 pin SCSI Connector
Baseboard	J3J2	2x6 Fan Speed Control/Tach	Fan Cable	J3J2	2x6 Fan Spd Control/Tach
Baseboard	J2J1	2x3 Fan LED Connector	Fan Cable	J2J1	2x3 Fan LED Connector
Baseboard	J1G4	2x17 Front Panel Connector	FP Cable	J1G4	2x17 Front Panel Connector
Baseboard	J1D3	2x5 USB Connector	USB Cable	J1D3	2x5 USB Connector
Baseboard	J9C1	1x3 IPMB Connector	I2C Cable	J9C1	1x3 IPMB Connector
FPIO Board Connections					
FPIO Board	J5A1	2x20 IDE Connector	IDE Cable	J5A1	2x20 IDE Connector
FPIO Board	J2A1	68 Pin Blind Mate receptacle	CDFDD I/F	J2A1	68 Pin Blind Mate plug
FPIO Board	J7A1	2x10 System Fan Cntrl conn	Fan Cntrl Cbl	J7A1	2x10 System Fan Cntrl con
FPIO Board	J5B1	68 pin SCSI Connector	SCSI BB Cbl	J5B1	68 pin SCSI Connector
FPIO Board	J6A1	2x8 Alarms Connector	Alarms Cable	J6A1	2x8 alarm connector 2mm
FPIO Board	J1A1	2x3 P/S Power Connector	P/S Assembly	J1A1	2x3 P/W Power Connector
FPIO Board	J9A1	1x3 System Fan 1 Conn	Fan 1	J9A1/ J8A3	Right 1x3 80mm Fan Cable
FPIO Board	J8A3	1x3 System Fan 2 Conn	Fan 2		Left 1x3 80mm Fan Cable
FPIO Board	J8A2	1x3 System Fan 3 Conn	Fan 3	J8A1/ J8A2	Right 1x3 40mm Fan Cable
FPIO Board	J8A1	1x3 System Fan 4 Conn	Fan 4		Left 1x3 40mm Fan Cable
FPIO Board	J9D1	80 pin SCA Connector	SCSI Flex 1	J9D1	80 pin SCA Connector
FPIO Board	J5D1	80 pin SCA Connector	SCSI Flex 2	J5D1	80 pin SCA Connector
FPIO Board	J3A1	2x5 USB Connector	USB Cable	J3A1	2x5 USB Connector
FPIO Board	J1C1	2x17 Floppy Conn	Floppy Cable	J1C1	2x17 Floppy Connector
FPIO Board	J4A1	2x17 Front Panel conn 2mm	FP Cable	J4A1	2x17 front panel conn 2mm
FPIO Board	J9D2	RJ45 COM2/Dual USB conn	N/C		
FPIO Board	J9A2	I2C Connector	I2C Cable	J9A2	1x4 I2C Connector
CDROM/Floppy Interface Board Connections					
CDFDD I/F	J1	68 pin Blind Mate Plug	FPIO Board	J2A1	68 pin Blind Mate receptacle
CDFDD I/F	J2	1x26 FFC Sig/Pwr Conn	FFC Cable	J2	1x26 FFC Sig/Pwr Conn
CDFDD I/F	J3	2x20 IDE Signal Connector	IDE Cable	J3	2x20 IDE Signal Connector
CDFDD I/F	J4	1x2 CDROM Power Conn	CD Power Cbl	J4	1x2 CDROM Power Conn
CDROM Board Connections					

CDROM Bd	P3	2x20 IDE Signal Connector	IDE Cable	P3	2x20 IDE Signal Connector
CDROM Bd	P1	1x2 CDROM Power Conn	CD Power Cbl	P1	1x2 CDROM Pwr Conn
CDROM Bd	P4	2x25 Signal/Pwr Connector	CDROM Drive	J1	2x25 Signal/Pwr Connector
5V Riser Board Connections (only if DC P/S)					
5V Riser	J4	2x5 Power Connector	DC P/S Assy	P4	1x5 Power Connector

3.4 User-accessible Interconnects

3.4.1 Keyboard and Mouse Ports

The keyboard and mouse port share a common housing. A dongle is required to split the keyboard and mouse signals to separate PS/2 style connectors for use with a separate PS/2 style keyboard device and a separate PS/2 style mouse device.

Table 9. Keyboard and Mouse Port

Pin	Signal
1	KEYDAT (keyboard data)
2	MSEDAT (mouse data)
3	GND (ground)
4	Fused VCC (+5 V)
5	KEYCLK (keyboard clock)
6	MSECLK (mouse clock)

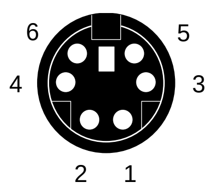


Figure 19. Keyboard/Mouse Connector

3.4.2 Serial Ports

One serial port is provided on both the front panel and the rear I/O to supply COM2 using an 8-pin RJ-45 connector. The COM2 serial port can be used either as an emergency management port (EMP) or as a normal serial port. As an emergency management port, COM2 is used as a communication path by the server management software that provides a level of emergency management through an external modem. Additional information can be found in the *IPMI 1.5 Specification for Serial Port Sharing.*

Table 10. Serial Port Connector on Rear I/O Port

Pin	Signal
1	RTS (request to send)
2	DTR (data terminal ready)
3	TXD (transmit data)
4	GND
5	RIA (ring indicator)

6	RXD (receive data)
7	DSR/DCD (date set ready / data carrier detect[1])
8	CTS (clear to send)

[1] Use jumper on SE7501WV2 System Baseboard to select

The front panel board has provision for the COM2 port using a RJ45 connector. This RJ45 connector is accessible without removing the front bezel. Note that Pin 5 needs to be grounded to disable the COM2 port on the rear I/O panel.

Table 11. Serial Port Connector on Front Panel

Pin	Signal
1	RTS (request to send)
2	DTR (data terminal ready)
3	TXD (transmit data)
4	GND
5	EMP_INUSE_L (GND disables rear COM2 I/O Port)
6	RXD (receive data)
7	DSR (date set ready)
8	CTS (clear to send)

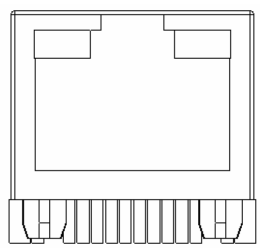


Figure 20. Serial Port Connector

3.4.3 Video Port

The video port interface is a standard VGA compatible, 15-pin connector. Onboard video is supplied by an ATI* Rage XL video controller with 8 MB of onboard video SGRAM.

Table 12. Video Connector

Pin	Signal
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND
6	GND
7	GND
8	GND

Pin	Signal
9	Fused VCC (+5 V)
10	GND
11	No connection
12	DDCDAT
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	DDCCLK

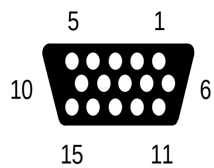


Figure 21. Video Connector

3.4.4 Universal Serial Bus (USB) Interface

The baseboard provides four USB ports. USB ports 0 and 1 are brought out the rear of the unit on the baseboard, and USB ports 2 and 3 are brought out the front of the unit on the front panel. The front USB ports are accessible without removing the front bezel. The built-in USB ports permit the direct connection of four USB peripherals without an external hub. If more devices are required, an external hub can be connected to any of the built-in ports.

Table 13. Single USB Connector

Pin	Signal
1	Fused VCC (+5 V w/over-current monitor of ports 0, 1, 2, and 3)
2	DATAL0 (differential data line paired with DATAH0)
3	DATAH0 (differential data line paired with DATAL0)
4	GND
5	GND
6	GND

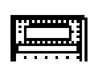


Figure 22. USB Connector

3.4.5 Ethernet Connector

The Intel® Server Board SE7501WV2 supports one stacked dual NIC RJ45 connector. The following table details the pin-out of the connector.

Table 14. Ethernet Connector

Pin	Signal Name	Pin	Signal Name
1	GND	18	NICA_MDI2P
2	NICB_MDI3M	19	NICA_MDI3M
3	NICB_MDI2P	20	GND
4	2.5V	21	NICA_MDI0M
5	NICB_MDI1M	22	2.5V
6	NICB_MDI0P	23	NICA_MDI1P
7	2.5V	24	NICA_MDI2M
8	NICB_MDI3P	25	2.5V
9	2.5V	26	NICA_MDI3P
10	NICB_MDI2M	27	NICA_LINK_ACT_L
11	NICB_MDI1P	28	NICA_LINK_ACT
12	2.5V	29	NICA_SPEED_1
13	NICB_MDI0M	30	NICA_SPEED_2
14	2.5V	31	NICB_LINK_ACT_L
15	NICA_MDI0P	32	NICB_LINK_ACT
16	NICA_MDI1M	33	NICB_SPEED_1
17	2.5V	34	NICB_SPEED_2

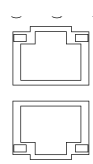


Figure 23. Dual Ethernet Connector

3.4.6 Telco Alarms Connector

The system provides one telco DB15 alarms connector on the rear bulkhead. Table 15 shows the pinout for the telco alarms connector, and Figure 24 shows the telco alarms connector as viewed from the back of the server.

Table 15. Telco Alarms Connector

Pin	Description	Pin	Description
1	Minor Reset +	9	Minor Alarm – NC
2	Minor Reset -	10	Minor Alarm - COM
3	Major Reset +	11	Major Alarm - NO
4	Major Reset -	12	Major Alarm - NC
5	Critical Alarm – NO	13	Major Alarm - COM
6	Critical Alarm – NC	14	Pwr Alarm - NO
7	Critical Alarm – COM	15	Pwr Alarm - COM
8	Minor Alarm – NO		

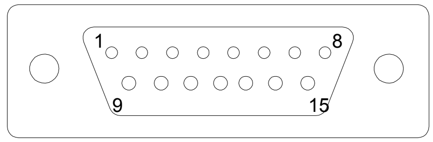


Figure 24. Telco Alarms Connector

3.4.7 Internal and External Ultra 320 SCSI Hard Disk Drive Connector

The Intel® Server Board SE7501WV2 provides an internal connection to Channel B of the Adaptec* AIC7902 Ultra-320 SCSI controller to the SCSI hard disk drives mounted in the hard drive bays. The SCSI bus on the Intel® Server Board SE7501WV2 is routed first to a SCSI bus on the FPIO board using a 68-pin LVD SCSI round cable, and then from the SCSI bus on the FPIO board to the SCSI disk drives using an 80-pin LVD SCSI flex circuit cable. The hot-plug circuitry resides on the FPIO board and not on the Intel® Server Board SE7501WV2.

In addition, the server system provides a shielded external VHDCI SCSI connection. This connection is on Channel A of the Adaptec* AIC7902 Ultra-320 SCSI controller.

Table 16. 68-pin SCSI Connectors on Intel® Server Board SE7501WV2

Connector Contact Number	Signal Name	Signal Name	Connector Contact Number
1	+DB(12)	-DB(12)	35
2	+DB(13)	-DB(13)	36
3	+DB(14)	-DB(14)	37
4	+DB(15)	-DB(15)	38
5	+DB(P1)	-DB(P1)	39
6	+DB(0)	-DB(0)	40
7	+DB(1)	-DB(1)	41
8	+DB(2)	-DB(2)	42
9	+DB(3)	-DB(3)	43
10	+DB(4)	-DB(4)	44
11	+DB(5)	-DB(5)	45
12	+DB(6)	-DB(6)	46
13	+DB(7)	-DB(7)	47
14	+DB(P)	-DB(P)	48
15	GROUND	GROUND	49
16	GROUND	GROUND	50
17	RESERVED	RESERVED	51
18	RESERVED	RESERVED	52
19	RESERVED	RESERVED	53
20	GROUND	GROUND	54
21	+ATN	-ATN	55
22	GROUND	GROUND	56
23	+BSY	-BSY	57

24	+ACK	-ACK	58
25	+RST	-RST	59
26	+MSG	-MSG	60
27	+SEL	-SEL	61
28	+C/D	-C/D	62
29	+REQ	-REQ	63
30	+I/O	-I/O	64
31	+DB(8)	-DB(8)	65
32	+DB(9)	-DB(9)	66
33	+DB(10)	-DB(10)	67
34	+DB(11)	-DB(11)	68

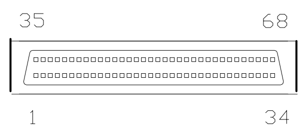


Figure 25. Internal Standard 68-pin SCSI Connector

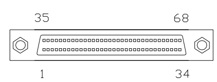


Figure 26. External VHDCI SCSI Connector

3.4.8 AC Power Input for AC-Input Power Supply Cage

Two single IEC320-C13 receptacles are provided at the rear of the AC-input power supply cage. It is recommended to use an appropriately sized power cord and AC main. Please refer to *Section 14, "AC Power Subsyst,"* of this document for system voltage, frequency, and current draw specifications.

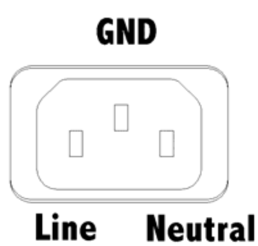


Figure 27. AC Power Input Connector

3.4.9 DC Power Input for DC-Input Power Supply Cage

A pluggable DC power terminal block is used to provide the DC-input power connection to each of the DC-input power supply modules that are configured in the DC power supply cage. It is recommended to use appropriately sized power wire and DC main. Please refer to *Section 13, "DC Power Subsystem,"* of this document for system DC voltage and current draw specifications.

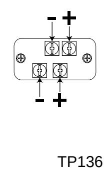


Figure 28. DC Power Input Connector

The pluggable terminal block will accept standard terminal lugs, size Newark stock # 81N1501 type CRS-T0-1406-HT. These lugs accept 14AWG wire gauge. The width (w, see Figure 29) of the lug can be no larger than 0.25 inches.

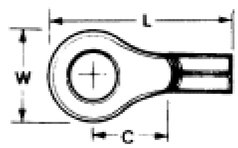


Figure 29. Terminal Lug

4. Intel® Server Board SE7501WV2 Functional Architecture

This chapter provides a high-level description of the functionality distributed between the architectural blocks of the Intel® Server Board SE7501WV2.

4.1 Processor and Memory Subsystem

The Intel® E7501 chipset provides a 36-bit address, 64-bit data processor host bus interface, operating at 533Mz in the AGTL+ signaling environment. The MCH component of the chipset provides an integrated memory controller, an 8-bit Hub Interface, and three 16-bit Hub Interfaces.

The Hub Interface provides the interface to two 64-bit, 100 MHz, Rev 1.0 compliant PCI-X buses via the P64H2. The Intel® Server Board SE7501WV2 directly supports up to 12 GB of ECC memory, using six DDR266 compliant registered ECC DIMMs. The ECC implementation in the MCH can detect and correct single-bit errors, detect multiple-bit errors, and support the Intel® Single Device Data Correction features.

4.1.1 Processor Support

The Intel® Server Board SE7501WV2 supports one or two Intel® Xeon™ processors in the Socket 604 INT3/FCPGA package. When two processors are installed, all processors must be of identical revision, core voltage, and bus/core speed. When only one processor is installed, it should be in the socket labeled CPU-1 and the other socket must be empty. The support circuitry on the server board consists of the following:

- Dual Socket 604 INT3/FCPGA CPU sockets supporting 533 MHz.
- Processor host bus AGTL+ support circuitry

Table 17. Intel® Telco/Industrial Grade Server TIGPR2U Processor Support Matrix for 533MHz

Speed (MHz) 533MHz	Product Code	MM#	Test Specification (S-spec)	Stepping	CPUID	L2 Cache Size	Notes
2.4 GHz	BX80532KE2400D	851280	SL6GD	C1	0F24	512k	1
2.4 GHz	BX80532KE2400D	851269	SL6NQ	C1	0F24	512k	1
2.4 GHz	RK80532KE056512	852305	SL6VL	D1		512k	1

Note: Processors must be populated in sequential order. That is, CPU socket #1 must be populated before CPU socket #2.

The Intel® Server Board SE7501WV2 is designed to provide up to 75 A per processor. Processors with higher current requirements are not supported. Processor terminators are not required in unpopulated processor sockets.

In addition to the circuitry described above, the processor subsystem contains the following:

- Processor module presence detection logic
- Server management registers and sensors

4.1.1.1 Processor VRM

The Intel® Server Board SE7501WV2 has a single VRM (Voltage Regulator Module) to support two processors. It is compliant with the VRM 9.1 specification and provides a maximum of 150 AMPs, which is capable of supporting currently supported processors as well as those supported in the future.

The board hardware and BMC must read the processor VID (voltage identification) bits for each processor before turning on the VRM. If the VIDs of the two processors are not identical, then the BMC will not turn on the VRM and a beep code is generated.

4.1.1.2 Reset Configuration Logic

The BIOS determines the processor stepping, cache size, etc., through the CPUID instruction. The requirements are that all processors in the system must operate at the same frequency, have the same cache sizes, and have the same VID. No mixing of product families is supported.

On the Intel® Server Board SE7501WV2, the BIOS is responsible for configuring the processor speeds. The processor information is read at every system power-on. The speed is set to correspond to the speed of the slowest processor installed.

Note: No manual processor speed setting options exist either in the form of a BIOS setup option or jumpers when using production-level processors.

4.1.1.3 Processor Module Presence Detection

Logic is provided on the baseboard to detect the presence and identity of installed processors. The BMC checks the logic and will not turn on the system DC power unless the VIDs of both processors match in a dual processor configuration.

4.1.1.4 Interrupts and APIC

Interrupt generation and notification to the processors is done by the APICs in the ICH3 and the P64H2 using messages on the front side bus.

4.1.1.5 Server Management Registers and Sensors

The BMC manages registers and sensors associated with the processor/memory subsystem. For more information, refer to Section 6.

4.1.2 Memory Subsystem

The Intel® Server Board SE7501WV2 supports up to six DIMM slots for a maximum memory capacity of 12 GB. The DIMM organization is x72, which includes eight ECC check bits. The memory interface runs at 266MHz.

The memory controller supports memory scrubbing, single-bit error correction, multiple-bit error detection, and the Intel® Single Device Data Correction feature. Memory can be implemented with either single sided (one row) or double-sided (two row) DIMMs.

The following figure provides a block diagram of the memory sub-system implemented on the Intel® Server Board SE7501WV2.

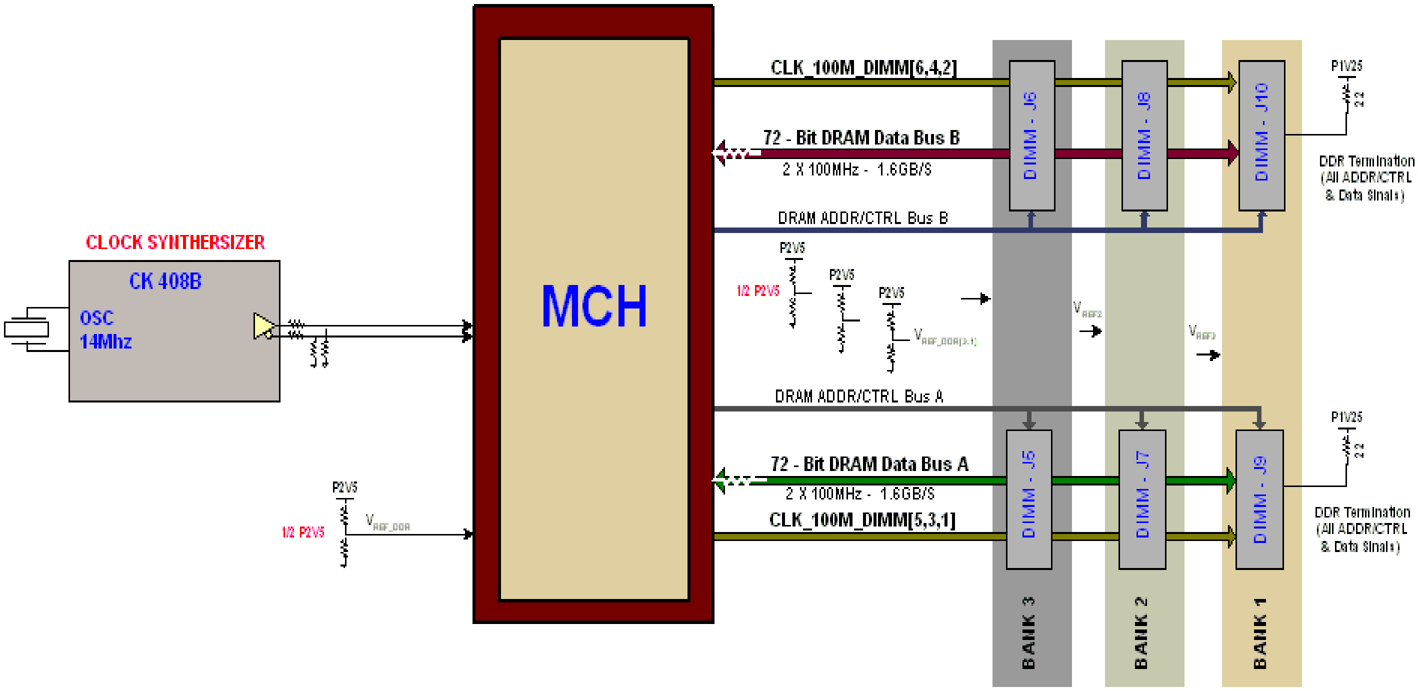


Figure 30. Memory Sub-system Block Diagram

4.1.2.1 Memory DIMM Support

The Intel® Server Board SE7501WV2 supports DDR266 compliant registered ECC DIMMs operating at 266MHz.

Only DIMMs tested and qualified by Intel or a designated memory test vendor are supported on the Intel® Server Board SE7501WV2. Tested DIMMs are listed in the *Intel® Server Board SE7501WV2 Memory List Test Report,* which is available on FDBL/IBL. Note that all DIMMs are supported by design, but only fully tested DIMMs will be supported.

The minimum supported DIMM size is 128 MB. Therefore, the minimum main memory configuration is 2 x 128 MB or 256 MB. The largest size DIMM supported is a 2 GB stacked registered DDR266 ECC DIMM based on 512 megabit technology.

Only registered DDR266 compliant, ECC, DDR memory DIMMs will be supported.

ECC single-bit errors will be corrected and multiple-bit errors will be detected. The Intel® Server Board SE7501WV2 also supports the Intel® Single Device Data Correction feature.

- The maximum memory capacity is 12 GB.
- The minimum memory capacity is 256 MB.

4.1.2.2 Memory Configuration

The memory interface between the MCH and DIMMs is 144 bits wide. This requires that two DIMMs be populated per bank in order for the system to operate. At least one bank has to be populated in order for the system to boot. If additional banks have less than two DIMMs, the memory for that bank(s) will not be available to the system.

There are three banks of DIMMs, labeled 1, 2, and 3. Bank 1 contains DIMM locations 1A and 1B, Bank 2 contains 2A and 2B, and Bank 3 contains 3A and 3B. DIMM socket identifiers are marked with silkscreen next to each DIMM socket on the baseboard. Note that the sockets associated with any given bank are located next to each other.

Certain combinations of DIMM types in the same system can violate the write Ringback measurement specification during analog validation.

When mixing double-ranked DIMMs (x4 or x8) with single-ranked DIMMs (x4 or x8), if a single-ranked DIMM is placed in the populated slot closest to the MCH, the Write Ringback at that DIMM violates the JEDEC DRAM specification.

Note: For the current list of DIMM stuffing rules and tested memory, see the *Intel® Server Board SE7501WV2 Memory List Test Report* available on FDBL/IBL.

The baseboard's signal integrity and cooling are optimized when memory banks are populated in order. Therefore, when installing memory, DIMMs should be installed starting with Bank 1 and ending with Bank 3.

DIMM and memory configurations must adhere to the following:

- DDR266 registered ECC DIMM modules
- DIMM organization: x72 ECC
- Pin count: 184
- DIMM capacity: 128 MB, 256 MB, 512 MB, 1 GB, 2 GB
- Serial PD: JEDEC Rev 2.0
- Voltage options: 2.5 V (VDD/VDDQ)
- Interface: SSTL2
- Two DIMMs must be populated in a bank for a x144 wide memory data path.
- Any or all memory banks may be populated.

Table 18. Memory Bank Labels

Memory DIMM	Bank
J5F1 (DIMM 1B), J5F2 (DIMM 1A)	1
J5F3 (DIMM 2B), J6F1 (DIMM 2A)	2
J6F2 (DIMM 3B), J6F3 (DIMM 3A)	3

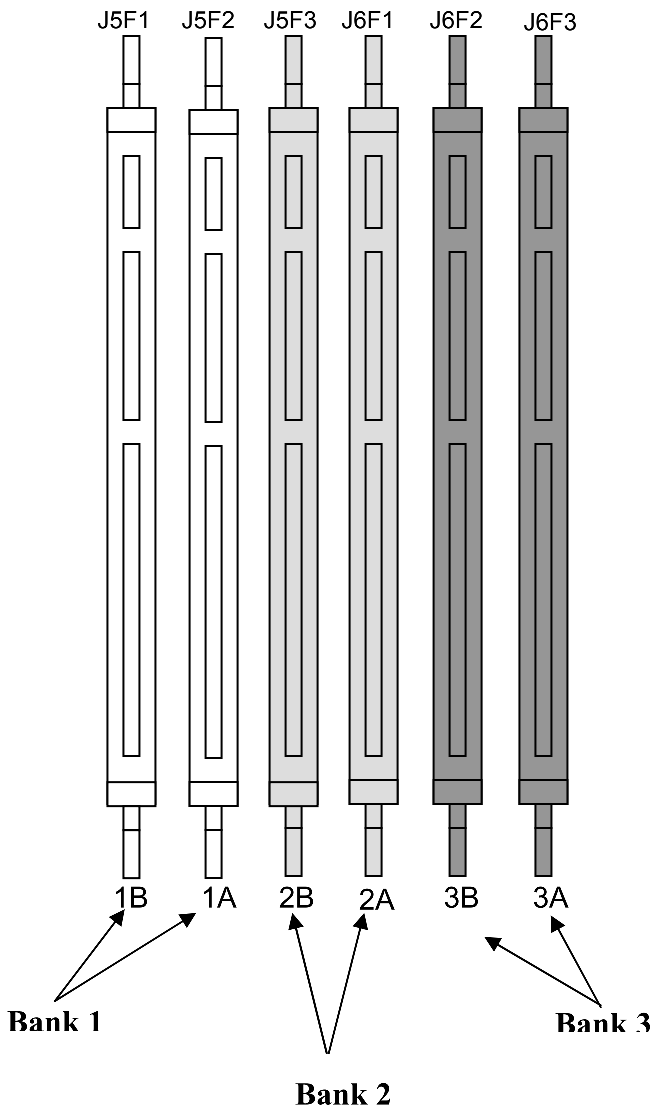


Figure 31. Memory Bank Label Definition

4.1.2.3 I²C Bus

An I²C bus connects the six DIMM slots to the ICH3-S and the BMC. This bus is used by the system BIOS to retrieve DIMM information needed to program the MCH memory registers which are required to boot the system.

4.1.2.4 DIMM Failure LED

The Intel® Server Board SE7501WV2 provides DIMM Failure LEDs located next to each DIMM slot on the baseboard. The DIMM Failure LEDs are used to indicate double-bit DIMM errors. If a double-bit error is detected during POST, the BIOS sends a Set DIMM State command to the BMC indicating that the DIMM LED is lit.

4.1.2.5 Intel® Single Device Data Correction feature

The Intel® Server Board SE7501WV2 supports the Intel® Single Device Data Correction correct memory architecture, which gives the memory sub-system the ability to withstand a multi-bit failure within a DRAM device, including a failure that causes incorrect data on all data bits of the device.

4.2 Intel® E7501 Chipset

The Intel® Server Board SE7501WV2 is designed around the Intel® E7501 chipset. The chipset provides an integrated I/O bridge and memory controller, and a flexible I/O subsystem core (PCI-X). This is targeted for multiprocessor systems and standard high-volume servers. The Intel® E7501 chipset consists of three components:

- **MCH: Memory Controller Hub North Bridge.** The MCH North Bridge accepts access requests from the host (processor) bus and directs those accesses to memory or to one of the PCI buses. The MCH monitors the host bus, examining addresses for each request. Accesses may be directed to a memory request queue for subsequent forwarding to the memory subsystem, or to an outbound request queue for subsequent forwarding to one of the PCI buses. The MCH also accepts inbound requests from the P64H2 and the ICH3-S. The MCH is responsible for generating the appropriate controls to control data transfer to and from memory.
- **P64H2: PCI-X 64bit Hub 2.0 I/O Bridge.** The P64H2 provides the interface for two 64-bit, 133MHz Rev. 1.0 compliant PCI-X buses. The P64H2 is both master and target on both PCI-X buses.
- **ICH3-S: South Bridge.** The ICH3-S controller has several components. It provides the interface for a 32-bit, 33-MHz Rev. 2.2-compliant PCI bus. The ICH3-S can be both a master and a target on that PCI bus. The ICH3-S includes a USB controller and an IDE controller. The ICH3-S is responsible for much of the power management functions, with ACPI control registers built in. The ICH3-S also provides a number of GPIO pins and has the LPC bus to support low speed legacy I/O.

The MCH, P64H2, and ICH3-S chips provide the pathway between processor and I/O systems. The MCH is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to one of the PCI buses or legacy I/O locations. If the cycle is directed to one of the 64-bit PCI segments, the MCH communicates with the P64H2 through a private interface called the HI (Hub Interface). If the cycle is directed to the ICH3-S, the cycle is output on the MCH's 8bit HI 1.5 bus. The P64H2 translates the HI 2.0 bus operation to a 64-bit PCI-X Rev. 1.0-compliant signaling environment operating from 100MHz to 133 MHz. The ICH3-S translates the HI 1.5 bus operation to a 32-bit PCI Rev. 2.2-compliant signaling environment operating at 33MHz.

The HI 2.0 bus is 16 bits wide and operates at 66 MHz with 512MT/s, providing over 1 GB per second of bandwidth.

All I/O for the Intel® Server Board SE7501WV2, including PCI and PC-compatible I/O, is directed through the MCH and then through either the P64H2 or the ICH3-S provided PCI buses.

- The ICH3-S provides a 32-bit/33-MHz PCI bus, hereafter called P32-A.

- The P64H2 provides two independent 64-bit, 133-MHz PCI-X buses, hereafter called P64-B and P64-C.

This independent bus structure allows all three PCI buses to operate concurrently.

4.2.1 MCH Memory Architecture

The MCH supports a 144-bit wide Memory sub-system that can support a maximum of 12 GB (using 2 GB DIMMs). This configuration needs external registers for buffering the memory address and control signals. In this configuration the MCH supports six DDR266 compliant registered stacked DIMMs for a maximum of 12 GB. The six chip selects are registered inside the MCH and need no external registers for chip selects.

The memory interface runs at 266 MHz. The memory interface supports a 144-bit wide memory array. It uses fifteen address lines (BA[1:0] and MA[12:0]) and supports 128 Mb, 256 Mb, 512 Mb, 1 Gb, and 2 Gb DRAM densities. The DDR DIMM interface supports memory scrubbing, single-bit error correction, and multiple bit error detection as well as the Intel® Single Device Data Correction features.

4.2.1.1 DDR Configurations

The DDR interface supports up to 12 GB of main memory and supports single- and double-density DIMMs.

4.2.2 MCH North Bridge

The E7501 MCH North Bridge (MCH) is a 1005 ball FC-BGA device and uses the proven components of previous generations like the Intel® Pentium® 4 bus interface unit, the Hub Interface unit, and the DDR memory interface unit. In addition, the MCH incorporates a Hub Interface (HI). The HI enables the MCH to directly interface with the P64H2. The MCH also increases the main memory interface bandwidth and maximum memory configuration with a 144-bit wide memory interface.

The MCH integrates three main functions:

- An integrated high performance main memory subsystem.
- An HI 2.0 bus interface that provides a high-performance data flow path between the host bus and the I/O subsystem.
- An HI 1.5 bus which provides an interface to the ICH3-S (South Bridge).

Other features provided by the MCH include the following:

- Full support of ECC on the memory bus
- Full support of the Intel® Single Device Data Correction features.
- Twelve deep in-order queue
- Full support of registered DDR266 ECC
- Support for 12 GB of DDR memory
- Memory scrubbing

4.2.3 P64H2

The P64H2 is a 567-ball FCBGA device and provides an integrated I/O bridge that provides a high-performance data flow path between the HI 2.0 and the 64-bit I/O subsystem. This subsystem supports peer 64-bit PCI-X segments. Because it has two PCI interfaces, the P64H2 can provide large and efficient I/O configurations. The P64H2 functions as the bridge between the HI and the two 64-bit PCI-X I/O segments. The HI can support 1 GB/s of data bandwidth.

4.2.3.1 PCI Bus P64-B I/O Subsystem

The P64-B supports the following embedded devices and connectors:

- One 184-pin, 5-volt keyed, 64-bit PCI expansion slot connector. The expansion slot can be used for a 3-slot PCI riser card. The PCI slots on the P64-B PCI bus support both full-length PCI cards and low profile PCI cards with the appropriate faceplate.
- One Intel® 82546EB dual channel 10/100/1000 Ethernet controller.

The BIOS is responsible for setting the bus speed of the P64-B. The following table shows the bus frequency according to slot population. The bus speed will always be set up to run at the speed of the slowest card installed.

Table 19. P64-B Speeds

Configuration	Bus B with Anvik Dual NIC down and 5-V Riser)	Bus B with Anvik Dual NIC down and 3.3-V Riser
0 Adapter Cards installed and on board device enabled	PCI-X 64/33	PCI-X 64/100
1 Adapter Card installed and on board device enabled	PCI-X 64/33	PCI-X 64/100
2 Adapter Cards installed and on board device enabled	PCI-X 64/33	PCI-X 64/66
3 Adapter Cards installed and on board device enabled	PCI-X 64/33	PCI-X 64/66
1 Adapter Card installed and on board device disabled	PCI-X 64/33	PCI-X 64/100
2 Adapter Cards installed and on board device disabled	PCI-X 64/33	PCI-X 64/66
3 Adapter Cards installed and on board device disabled	PCI-X 64/33	PCI-X 64/66

4.2.3.2 PCI Bus P64-C I/O Subsystem

P64-C supports the following embedded devices and connectors:

- One 184-pin, 5-volt keyed, 64-bit PCI expansion slot connector. The expansion slot can be used for a 3-slot PCI riser card. The PCI slots on the P64-C PCI bus support only low profile PCI cards.
- One Adaptec* 7902 dual channel U-320 SCSI controller.
- Support for Zero Channel RAID (ZCR) or M-ROMB that allows the on board SCSI controller to be “hidden” from system and used by the RAID processor on the add-in card.

The BIOS is responsible for setting the bus speed of the P64-C. The bus speed will always be set up to run at the speed of the slowest card installed.

Table 20. P64-C Speeds

Configuration	Bus C with AIC7902* SCSI down and 3.3-V Riser
0 Adapter Cards installed and on board device enabled	PCI-X 100
1 Adapter Card installed and on board device enabled	PCI-X 100
2 Adapter Cards installed and on board device enabled	PCI-X 100
3 Adapter Cards installed and on board device enabled	PCI-X 64/66
1 Adapter Card installed and on board device disabled	PCI-X 64/100
2 Adapter Cards installed and on board device disabled	PCI-X 64/100
3 Adapter Cards installed and on board device disabled	PCI-X 64/66

4.2.4 ICH3-S

The ICH3-S is a multi-function device, housed in a 421-pin BGA device, providing an HI 1.5 to PCI bridge, a PCI IDE interface, a PCI USB controller, and a power management controller. Each function within the ICH3-S has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

On the Intel® Server Board SE7501WV2, the primary role of the ICH3-S is to provide the gateway to all PC-compatible I/O devices and features. The Intel® Server Board SE7501WV2 uses the following ICH3-S features:

- PCI bus interface
- LPC bus interface
- IDE interface, with Ultra DMA 100 capability
- Universal Serial Bus (USB) interface
- PC-compatible timer/counter and DMA controllers
- APIC and 8259 interrupt controller
- Power management
- System RTC
- General purpose I/O

The following sections provide descriptions on how each supported feature is used on the Intel® Server Board SE7501WV2.

4.2.4.1 PCI Bus P32-A I/O Subsystem

The ICH3-S provides a legacy 32-bit PCI subsystem and acts as the central resource on this PCI interface. The P32-A supports the following embedded devices and connectors:

- An ATI* Rage XL video controller with 3D/2D graphics accelerator

4.2.4.2 PCI Bus Master IDE Interface

The ICH3-S acts as a PCI-based Ultra DMA/100 IDE controller that supports programmed I/O transfers and bus master IDE transfers. The ICH3-S supports two IDE channels, supporting two drives each (drives 0 and 1). The Intel® Server Board SE7501WV2 provides two separate interfaces to the IDE controller. The first is a single SSI compliant 40-pin (2x20) IDE connector. The second is through the high-density 100-pin floppy / IDE / front panel connector.

The IDE interface supports Ultra DMA/100 Synchronous DMA Mode transfers on the 40-pin connector and supports Ultra DMA/33 transfers on the 100-pin connector.

4.2.4.3 USB Interface

The ICH3-S contains three USB controllers and six USB ports. The USB controller moves data between main memory and the six USB ports. All six ports function identically and with the same bandwidth. The Intel® Server Board SE7501WV2 only supports four of the six ports on the board.

The Intel® Server Board SE7501WV2 provides two external USB ports on the back of the server board. The first external connector is located within the standard ATX I/O panel area while the second is located directly behind the P64-B full-length PCI card slot. The USB specification defines the external connectors.

The third and fourth USB ports can be accessed from the front of the system.

4.2.4.4 Compatibility Interrupt Control

The ICH3-S provides the functionality of two 82C59 PIC devices for ISA-compatible interrupt handling.

4.2.4.5 APIC

The ICH3-S integrates an APIC that is used to distribute 24 interrupts.

4.2.4.6 Power Management

One of the embedded functions of the ICH3-S is a power management controller. The Intel® Server Board SE7501WV2 uses this to implement ACPI-compliant power management features. The Intel® Server Board SE7501WV2 supports sleep states S0, S1, S4, and S5.

4.3 Super I/O

The National Semiconductor* PC87417 Super I/O device contains all of the necessary circuitry to control two serial ports, one parallel port, one floppy disk, and one PS/2-compatible keyboard and mouse. The Intel® Server Board SE7501WV2 supports the following features:

- GPIOs
- Two serial ports
- Floppy
- Keyboard and mouse through one PS/2 connector
- Wake up control

4.3.1 GPIOs

The National Semiconductor* PC87417 Super I/O provides general-purpose input/output pins that the Intel® Server Board SE7501WV2 utilizes. The following table identifies the pin and the signal name used in the schematic.

Table 21. Super I/O GPIO Usage Table

Pin	Name	IO/GPIO	Intel® Server Board SE7501WV2 Use
124	GPIO00/CLKRUN_L	I/O	TP
125	GPIO01/KBCLK	I/O	KB_CLK
126	GPIO02/KBDAT	I/O	KB_DAT
127	GPIO03/MCLK	I/O	MS_CLK
128	GPIO04/MDAT	I/O	MS_DAT
9	GPIO05/XRDY	I/O	TP
10	GPIO06/XIRQ	I/O	BMC_SYSIRQ
13	GPIO07/HFCKOUT	I/O	SIO_CLK_40M_BMC
1	GPIOE10/XA11	I/O,I(E)1	XBUS_A<11>
2	GPIOE11/XA10	I/O,I(E)1	XBUS_A<10>
3	GPIOE12/XA9	I/O,I(E)1	XBUS_A<9>
4	GPIOE13/XA8	I/O,I(E)1	XBUS_A<8>
5	GPIOE14/XA7	I/O,I(E)1	XBUS_A<7>
6	GPIOE15/XA6	I/O,I(E)1	XBUS_A<6>
7	GPIOE16/XA5	I/O,I(E)1	XBUS_A<5>
8	GPIOE17/XA4	I/O,I(E)1	XBUS_A<4>
14	GPIO20/XRD_XEN_L	I/O	XBUS_XRD_L
15	GPIO21/XWR_XRW_L	I/O	XBUS_XWR_L
16	GPIO22/XA3	I/O	XBUS_A<3>
17	GPIO23/XA2	I/O	XBUS_A<2>
18	GPIO24/XA1	I/O	XBUS_A<1>
19	GPIO25/XA0	I/O	XBUS_A<0>
22	GPIO26/XCS1_L	I/O	TP
23	GPIO27/XCS0_L	I/O	XBUS_XCS0_L
24	GPIO30/XD7	I/O	XBUS_D<7>
25	GPIO31/XD6	I/O	XBUS_D<6>
26	GPIO32/XD5	I/O	XBUS_D<5>
27	GPIO33/XD4	I/O	XBUS_D<4>
28	GPIO34/XD3	I/O	XBUS_D<3>
29	GPIO35/XD2	I/O	XBUS_D<2>
30	GPIO36/XD1	I/O	XBUS_D<1>
31	GPIO37/XD0	I/O	XBUS_D<0>
20	GPIOE40/XCS3_L	I/O,I(E)1	TP
21	GPIOE41/XCS2_L	I/O,I(E)1	TP
35	GPIOE42/SLBTIN_L	I/O,I(E)1	TP
49	GPIOE43/PWBTOUT_L	I/O,I(E)1	ZZ_POST_CLK_LED_L
50	GPIOE44/LED1	I/O,I(E)1	ZZ_BIOS_ROLLING

Pin	Name	IO/GPIO	Intel® Server Board SE7501WV2 Use
51	GPIOE45/LED2	I/O,I(E)1	FP_PWR_LED_L
52	GPIOE46/SLPS3_L	I/O,I(E)1	TP
53	GPIOE47/SLPS5_L	I/O,I(E)1	TP
36	GPIO50/PWBTN_L	I/O	TP
37	GPIO51/SIOSMI_L	I/O	TP
38	GPIO52/SIOSCI_L	I/O	SIO_PME_L
45	GPIO53/LFCKOUT/MSEN0	I/O	TP
54	GPIO54/VDDFELL	I/O	ZZ_POST_DATA_LED_L
56	GPIO55/CLKIN	I/O	CLK_48M_SIO
32	GPO60/XSTB2/XCNF2_L	O	PU_XBUS_XCNF2
33	GPO61/XSTB1/XCNF1_L	O	XBUS_XSTB1_L
34	GPO62/XSTB0/XCNF0_L	O	PU_XBUS_XCNF0
48	GPO63/ACBSA	O	PU_SIO_ACBSA
55	GPO64/WDO_L/CKIN48	O	PU_SIO_CKIN48

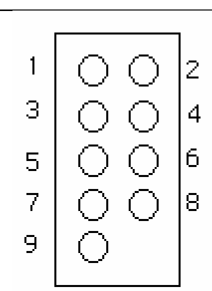
4.3.2 Serial Ports

The Intel® Server Board SE7501WV2 provides two serial ports: an external low-profile RJ45 Serial port, and an internal Serial header. The following sections provide details on the use of the serial ports.

4.3.2.1 Serial Port A

Serial A is an optional port, accessed through a 9-pin internal header (J9A2). A standard DH-10 to DB9 cable can be used to direct Serial A out the back of a given chassis. The Serial A interface follows the standard RS232 pin-out. The baseboard has a Serial Port A silkscreen label next to the connector as well as a location designator of J9A2. The Serial A connector is located next to the P64-C low-profile PCI card slot. A standard DH-10 to DB9 cable is available from Intel Corporation in the Intel® Server Board SE7501WV2 Serial Port Accessory Kit.

Table 22. Serial A Header Pin-out

Pin	Signal Name	Serial Port A Header Pin-out
1	DCD	
2	DSR	
3	RX	
4	RTS	
5	TX	
6	CTS	
7	DTR	
8	RI	
9	GND	

4.3.2.2 Serial Port B

Serial B is an external low profile 8-pin RJ45 connector that is located on the back of the board. For those server applications that require an external modem, an RJ45-to-DB9 adapter is necessary. A standard DH-10 to DB9 cable is available from Intel in the Intel® Server Board SE7501WV2 Serial Port Accessory Kit.

4.3.2.3 Serial Port Multiplexer Logic

The Intel® Server Board SE7501WV2 has a multiplexer to connect the rear RJ45 connector to either Serial Port A or Serial Port B. This facilitates the routing of Serial Port A to the rear RJ45 connector if Serial Port B is used for SOL (Serial Over LAN). This serial port selection can be done through the BIOS setup option.

The following figure shows the serial port mux functionality.

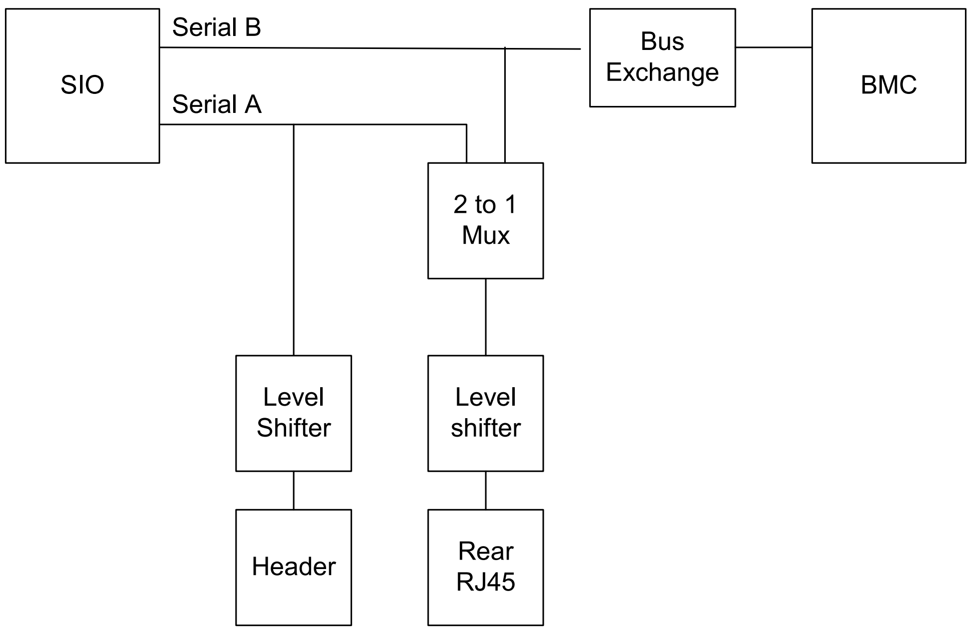


Figure 32. Serial Port Mux Logic

4.3.2.3.1 Rear RJ45 Serial B Port

The rear RJ45 Serial B port is a fully functional serial port that can support any standard serial device. Using an RJ45 connector for a serial port allows direct support for serial port concentrators, which typically use RJ45 connectors and are widely used in the high-density server market. For server applications that use a serial concentrator to access the server management features of the baseboard, a standard 8-pin CAT-5 cable from the serial concentrator is plugged directly into the rear RJ45 serial port.

To allow support of either of two serial port configuration standards used by serial port concentrators, the J5A2 jumper block located directly behind the rear RJ45 serial port must be jumpered appropriately according to the desired standard.

Note: By default as configured in the factory, the Intel® Server Board SE7501WV2 will have the rear RJ45 serial port configured to support a DSR signal which is compatible with the Cisco* standard.

For serial concentrators that require a DCD signal, the J5A2 jumper block must be configured as follows: The Serial Port jumper placed in position 1 and 2. Pin 1 on the jumper is denoted by an arrow directly next to the jumper block. The following diagram provides the jumper block pin-out for this configuration.

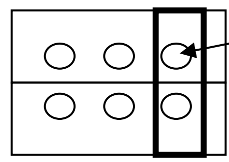


Figure 33. J5A2 Jumper Block for DCD Signal

For serial concentrators that require a DSR signal (Default), the J5A2 jumper block must be configured as follows: The Serial Port jumper in position 3 and 4. Pin 1 on the jumper is denoted by an arrow directly next to the jumper block.

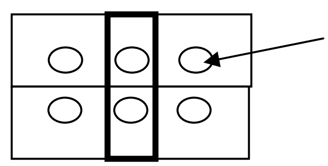


Figure 34. J5A2 Jumper Block for DSR Signal

For those server applications that require a DB9 serial connector, an 8-pin RJ45-to-DB9 adapter must be used. The following table provides the pin-out required for the adapter to provide RS232 support. A standard DH-10 to DB 9 cable and 8-pin RJ45 to DB9 DCD and DSR adapters are available from Intel in the Intel® Server Board SE7501WV2 Serial Accessory Kit.

Table 23. Rear Serial Port B Adapter Pinout

RJ45	Signal	Abbr.	DB9
1	Request to Send	RTS	7
2	Data Terminal Ready	DTR	4
3	Transmitted Data	TD	3
4	Signal Ground	SGND	5
5	Ring Indicator	RI	9
6	Received Data	RD	2
7	DCD or DSR	DCD/DSR	1 or 6*
8	Clear To Send	CTS	8

Note: The RJ45-to-DB9 adapter should match the configuration of the serial device used. One of two pin-out configurations is used depending on whether the serial device requires a DSR or DCD signal. The final adapter configuration should also match the desired pin-out of the RJ45 connector, as it can also be configured to support either DSR or DCD.

For example, Modem applications typically use a DCD signal. In this case the user would use a DCD-configured adapter and set the jumper block as shown in Figure 33.

4.3.2.4 Floppy Disk Controller

The floppy disk controller (FDC) in the SIO is functionally compatible with floppy disk controllers in the DP8473 and N844077. All FDC functions are integrated into the SIO including analog data separator and 16-byte FIFO. The Intel® Server Board SE7501WV2 provides two separate interfaces for the floppy disk controller. The first is an SSI compliant 36-pin connector, and the second is through the high-density 100-pin floppy / front panel / IDE connector.

Note: Using both interfaces in a common configuration is not supported.

4.3.2.5 Keyboard and Mouse

One external PS/2 port located on the back of the baseboard is provided for either a keyboard or a mouse. A PS/2 Y-cable can be used to provide simultaneous support for both a keyboard and mouse.

4.3.2.6 Wake-up Control

The Super I/O contains functionality that allows various events to control the power-on and power-off the system.

4.3.3 BIOS Flash

The Intel® Server Board SE7501WV2 incorporates an Intel® 3 Volt Advanced+ Boot Block 28F320C3 Flash memory component. The 28F320C3 is a high-performance 32-megabit memory component that provides 2048K x 16 of BIOS and non-volatile storage space. The flash device is connected through the X-bus from the SIO.

5. Configuration and Initialization

This section describes the configuration and initialization of various baseboard sub-systems as implemented on the Intel® Server Board SE7501WV2.

5.1.1 Main Memory

All installed memory greater than 1 MB is mapped to local main memory, up to the top of physical memory, which is located at 12 GB. Memory between 1 MB to 15 MB is considered standard ISA extended memory. 1 MB of memory starting at 15 MB can be optionally mapped to the PCI bus memory space.

The remainder of this space, up to 12 GB, is always mapped to main memory, unless Extended SMRAM is used, which limits the top of memory to 256 MB.

5.1.1.1 PCI Memory Space

Memory addresses below the 4 GB range are mapped to the PCI bus. This region is divided into three sections: High BIOS, APIC Configuration Space, and General-purpose PCI Memory. The General-purpose PCI Memory area is typically used for memory-mapped I/O to PCI devices. The memory address space for each device is set using PCI configuration registers.

5.1.1.2 High BIOS

The top 2 MB of Extended Memory is reserved for the system BIOS, extended BIOS for PCI devices, and A20 aliasing by the system BIOS. The Intel® Xeon™ processor begins executing from the high BIOS region after reset.

5.1.1.3 I/O APIC Configuration Space

A 64 KB block located 20 MB below 4 GB is reserved for the I/O APIC configuration space.

5.1.1.4 Extended Xeon Processor Region (above 4GB)

An Intel® Xeon™ processor-based system can have up to 64 GB of addressable memory. The BIOS uses the Extended Addressing mechanism to use the address ranges.

5.1.2 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into main memory. This is typically done to allow ROM code to execute more rapidly out of RAM. ROM is designated read-only during the copy process while RAM at the same address is designated write-only. After copying, the RAM is designated read-only and the ROM is designated write-only (shadowed). Processor bus transactions are routed accordingly. Transactions originated from the PCI bus or ISA masters and targeted at the shadowed memory block will not appear on the processor’s bus.

5.1.3 System Management Mode Handling

The Intel® E7501 MCH supports System Management Mode (SMM) operation in standard (compatible) mode. System Management RAM (SMRAM) provides code and data storage space for the SMI_L handler code, and is made visible to the processor only on entry to SMM, or other conditions, which can be configured using Intel® E7501 PCI registers.

5.2 I/O Map

The Intel® Server Board SE7501WV2 allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including the ICH3-S, have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On the Intel® Server Board SE7501WV2, the ICH3-S provides the bridge to ISA functions through the LPC bus.

5.3 Accessing Configuration Space

All PCI devices contain PCI configuration space, accessed using mechanism #1 defined in the PCI Local Bus Specification.

If dual processors are used, only the processor designated as the Boot-strap Processor (BSP) should perform PCI configuration space accesses. Precautions should be taken to guarantee that only one processor performs system configuration.

When CONFIG_ADDRESS is written to with a 32-bit value (selecting the bus number, device on the bus, and specific configuration register in the device), a subsequent read or write of CONFIG_DATA initiates the data transfer to/from the selected configuration register. Byte enables are valid during accesses to CONFIG_DATA; they determine whether the configuration register is being accessed or not. Only full Dword reads and writes to CONFIG_ADDRESS are recognized as a configuration access by the Intel® chipset. All other I/O accesses to CONFIG_ADDRESS are treated as normal I/O transactions.

5.3.1 CONFIG_ADDRESS Register

CONFIG_ADDRESS is 32 bits wide and contains the field format shown in the following figure. Bits [23::16] choose a specific bus in the system. Bits [15::11] choose a specific device on the selected bus. Bits [10::8] choose a specific function in a multi-function device. Bit [6::2] select a specific register in the configuration space of the selected device or function on the bus.

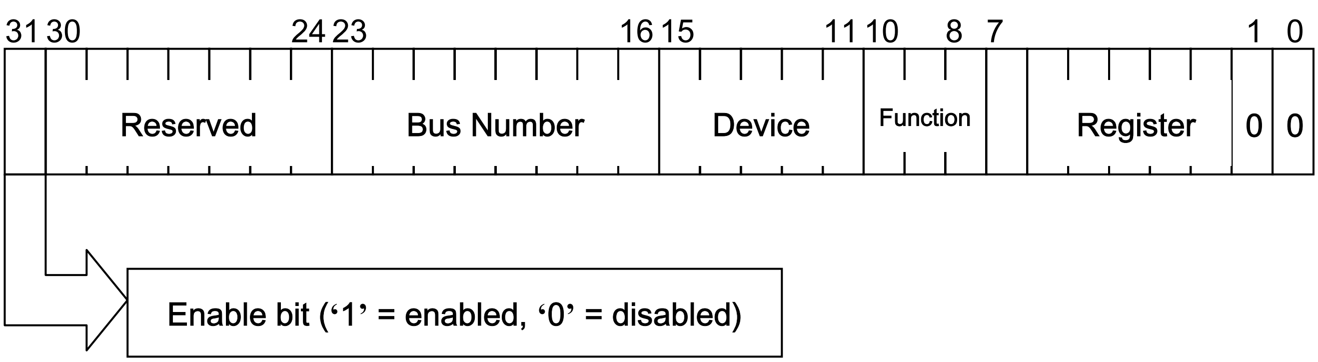


Figure 35. CONFIG_ADDRESS Register

5.3.1.1 Bus Number

PCI configuration space protocol requires that all PCI buses in a system be assigned a bus number. Furthermore, bus numbers must be assigned in ascending order within hierarchical buses. Each PCI bridge has registers containing its PCI bus number and subordinate PCI bus number, which must be loaded by POST code. The Subordinate PCI bus number is the bus number of the last hierarchical PCI bus under the current bridge. The PCI bus number and the subordinate PCI bus number are the same in the last hierarchical bridge.

5.3.1.2 Device Number and IDSEL Mapping

Each device under a PCI bridge has its IDSEL input connected to one bit out of the PCI bus address/data signals AD[31::11] for the PCI bus. Each IDSEL-mapped AD bit acts as a chip select for each device on PCI. The host bridge responds to a unique PCI device ID value, that along with the bus number, cause the assertion of IDSEL for a particular device during configuration cycles. The following table shows the correspondence between IDSEL values and PCI device numbers for the PCI bus. The lower 5-bits of the device number are used in CONFIG_ADDRESS bits [15::11].

Table 24. PCI Device IDs

Device Description	Bus	Device ID (Hex)
North Bridge (MCH)	0	00
ICH3 P2P Bridge	1	1E
ICH3 USB	1	1D
ICH3 IDE	1	1F
Video	1	0C
RIDE	1	02
RMC Connector	1	0A
P64H2 P2P Bridge A	2	1F
P64H2 P2P Bridge B	2	1D
Dual Gigabit NIC	3	07
PCI Slot 1B	3	08
PCI Slot 2B	3	09
PCI Slot 3B	3	0A
SCSI	4	07
PCI Slot 1C	4	08
PCI Slot 2C	4	09
PCI Slot 3C	4	0A

5.4 Hardware Initialization

An Intel® Xeon™ processor system based on the Intel® E7501 MCH is initialized in the following manner.

1. When power is applied, after receiving RST_PWRGD_PS from the power supply, the BMC provides resets using the RST_P6_PWRGOOD signal. The ICH3-S asserts PCIRST_L to MCH, P64H2, and other PCI devices. The MCH then asserts RST_CPURST_L to reset the processor(s).

2. The MCH is initialized, with its internal registers set to default values. Before RST_CPURST_L is deasserted, the MCH asserts BREQ0_L. Processor(s) in the system

determine which host bus agents they are, Agent 0 or Agent 3, based on whether their BREQ0_L or BREQ1_L is asserted. This determines bus arbitration priority and order.

3. After the processor(s) in the system determines which processor will be the BSP, the non-BSP processor becomes an application processor and idles, waiting for a Startup Inter Processor Interrupt (SIPI).

4. The BSP begins by fetching the first instruction from the reset vector.

5. The Intel® E7501 chipset registers are updated to reflect memory configuration. DIMM is sized and initialized.

6. All PCI and ISA I/O subsystems are initialized and prepared for booting.

Refer to the Intel® Server Board SE7501WV2 BIOS EPS for more details regarding system initialization and configuration.

5.5 Clock Generation and Distribution

All buses on the Intel® Server Board SE7501WV2 operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 100 MHz differentials: For INT3/FCPGA sockets, the MCH, and the ITP port.
- 66 MHz at 3.3 V logic levels: For MCH, P64H2, ICH3, and IDE RAID Controller clock
- 33.3 MHz at 3.3 V logic levels: Reference clock for ICH3, BMC, Video, SIO, and the IDE RAID controllers
- 48MHz: ICH3-S, and SIO
- 14.318 MHz at 3.3V logic levels: ICH3-S, and video clocks

For information on processor clock generation, see the *CK408B Synthesizer/Driver Specification*.

The Intel® Server Board SE7501WV2 also provides asynchronous clock generators:

- 80-MHz clock for the embedded SCSI controller
- 25-MHz clock for the embedded Network Interface controllers
- 32-KHz clock for the ICH3-S RTC

The following figure illustrates clock generation and distribution on the Intel® Server Board SE7501WV2.

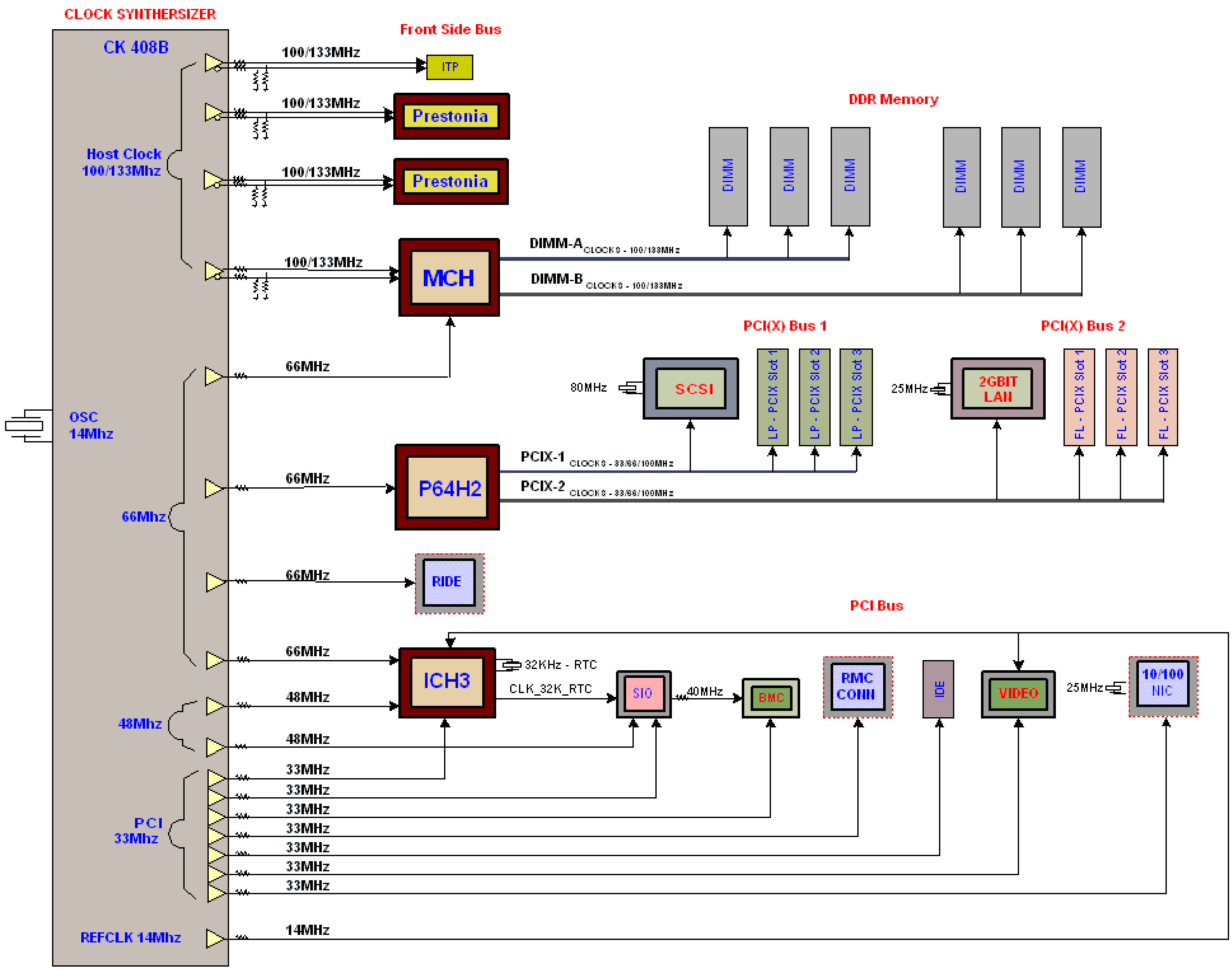


Figure 36. Intel® Server Board SE7501WV2 Clock Distribution

5.6 PCI I/O Subsystem

5.6.1 PCI Subsystem

The primary I/O bus for the Intel® Server Board SE7501WV2 is the PCI subsystem, with three independent PCI bus segments. The PCI bus complies with the *PCI Local Bus Specification*, Rev *2.2*. The P32-A bus segment is directed through the ICH South Bridge while the two 64-bit segments, P64-B and P64-C, are directed through the P64H2 I/O Bridge. The following table lists the characteristics of the three PCI bus segments.

Table 25. PCI Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Speed	Type	PCI I/O Riser Slots
P32-A	5 V	32-bits	PCI 33 MHz	Peer Bus	–
P64-B	3 V	64-bits	PCI-X 100 MHz	Peer Bus	Supports full-length cards, 3.3V bus
P64-C	3 V	64-bits	PCI-X 100 MHz	Peer Bus	Supports low-profile cards, 3.3V bus

5.6.2 P32-A: 32-bit, 33-MHz PCI Subsystem

All 32-bit, 33-MHz PCI I/O for the Intel® Server Board SE7501WV2 is directed through the ICH South Bridge. The 32-bit, 33-MHz PCI segment created by the ICH is known as the P32-A segment. The P32-A segment supports the following embedded devices and connectors:

- 2D/3D Graphics Accelerator: ATI* Rage XL Video Controller

Each of the embedded devices listed above can be disabled via a BIOS Setup option.

5.6.2.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD[31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P32-A devices and the corresponding device description.

Table 26. P32-A Configuration IDs

IDSEL Value	Device
28	ATI* Rage XL Video Controller

5.6.2.2 P32-A Arbitration

P32-A supports two PCI masters (ATI* Rage XL, and the ICH3-S). All PCI masters must arbitrate for PCI access, using resources supplied by the ICH. The host bridge PCI interface (ICH) arbitration lines REQx* and GNTx* are special cases in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 27. P32-Arbitration Connections

Baseboard Signals	Device
P32_REQ0*/P32_GNT0*	ATA Rage XL video controller

5.6.3 P64-B and P64-C: 64-bit, 100-MHz PCI-X Subsystem

There are two peer 64-bit, 100-MHz PCI-X bus segments directed through the P64H2 I/O Bridge.

The first PCI-X segment, P64-B, provides a single I/O Riser slot capable of supporting full length, full height PCI cards. The PCI cards must meet the PCI specification for height, inclusive of cable connections and memory. In addition to the riser connector, the P64-B segment also has an Intel® 82546EB dual channel Gigabit Ethernet controller.

The second PCI-X segment, P64-C, provides a second I/O riser slot. Because of physical limitations of the baseboard, this riser slot is only capable of supporting low-profile PCI cards. In addition to the riser connector, the P64-C segment also has an Adaptec* 7902 dual channel U-320 SCSI controller.

5.6.3.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD[31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following tables show the bit each IDSEL signal is attached to for P64-B and P64-C devices, and the corresponding device description.

Table 28. P64-B Configuration IDs

IDSEL Value	Device
23	On-board Gigabit Ethernet controller
24	First slot of the riser card
25	Second slot of the riser card
26	Third slot of the riser card

Table 29. P64-C Configuration IDs

IDSEL Value	Device
23	On-board U320 SCSI controller
24	First slot of the riser card
25	Second slot of the riser card
26	Third slot of the riser card

5.6.3.2 P64-B Arbitration

The P64-B supports five PCI masters (the on-board gigabit ethernet controller, three slots on the 3-slot PCI Riser, and the P64H2). All PCI masters must arbitrate for PCI access using resources supplied by the P64H2. The host bridge PCI interface (P64H2) arbitration lines REQx* and GNTx* are special cases in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 30. P64-B Arbitration Connections

P64H2 Signals	Device
P_REQ1*/P_GNT1*	Embedded Ethernet controller
P_REQ2*/P_GNT2*	P64-B: Top slot of the 3-slot riser
P_REQ3*/P_GNT3*	P64-B: Middle slot of the 3-slot riser
P_REQ4*/P_GNT4*	P64-B: Bottom slot of the 3-slot riser

5.6.3.3 P64-C Arbitration

P64-C supports five PCI masters (three slots on the 3-slot PCI riser, the embedded U-320 SCSI controller, and the P64H2). All PCI masters must arbitrate for PCI access, using resources supplied by the P64H2. The host bridge PCI interface (P64H2) arbitration lines REQx* and GNTx* are special cases in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 31. P64-C Arbitration Connections

P64H2 Signals	Device
S_REQ1*/S_GNT1*	Embedded U320 SCSI controller
S_REQ2*/S_GNT2*	P64-B: Top slot of the 3-slot riser
S_REQ3*/S_GNT3*	P64-B: Middle slot of the 3-slot riser
S_REQ4*/S_GNT4*	P64-B: Bottom slot of the 3-slot riser

5.6.3.4 Zero Channel RAID (ZCR) Capable Riser Slot

The SCSI version of the Intel® Server Board SE7501WV2 is capable of supporting the following zero channel RAID controllers, the Intel® SRCZCR, SRCMRU and SRCMRX RAID Adapter and the Adaptec* 2000S RAID adapter. ZCR cards are only supported in the first slot of the 3-slot PCI riser cards or the 1-slot riser cards used on the P64-C PCI segment.

The ZCR add-in cards leverage the on-board SCSI controller along with their own built-in intelligence to provide a complete RAID controller subsystem on-board. The riser card and baseboard use an implementation commonly referred to as RAID I/O Steering (RAIDIOS) specification version 0.92 to support this feature. If either of these supported RAID cards are installed, then the SCSI interrupts are routed to the RAID adapter instead of to the PCI interrupt controller. Also the IDSEL of the SCSI controller is not driven to the controller and thus will not respond as an on-board device. The host-based I/O device is effectively hidden from the system.

5.7 Ultra320 SCSI

The SCSI version of the Intel® Server Board SE7501WV2 provides an embedded dual-channel SCSI bus through the use of the Adaptec* AIC-7902W SCSI controller, which is capable of supporting up to 132 MB/sec SCSI transfers. The Adaptec* AIC-7902W controller contains two independent SCSI controllers that share a single 64-bit, 100-MHz PCI-X bus master interface as a multifunction device, packaged in a 456-pin BGA.

Internally, each controller is identical and is capable of operations using either 16-bit SE or Low-Voltage Differential (LVD) SCSI providing 40 MBps (Ultra-wide SE), 80 MBps (Ultra 2), 160 MBps (Ultra 160/m) or 320 MBps (Ultra 320/M). Each controller has its own set of PCI configuration registers and SCI I/O registers. The Intel® Server Board SE7501WV2 supports disabling of the on-board SCSI controller through the BIOS Setup menu.

The Intel® Server Board SE7501WV2 provides active terminators, termination voltage, a re-settable fuse, and a protection diode for both SCSI channels. By design, the on-board termination will always be enabled. No ability will be provided to disable termination. Each of the two SCSI channels has a connector interface. Channel A is an external high-density connector located on the back of the board, and Channel B is a standard 68-pin internal connector.

The Adaptec* AIC-7902W SCSI controller adds a feature called Integrated SCSI mirroring/striping also know as HostRAID[2]. Integrated SCSI mirroring/striping offers an entry-level Raid functionality for reliable performance and fill data protection for storage systems. HostRAID supports the following features:

- Boot array support
- Support for TAID 0 and DATA1 with Microsoft* Windows* operating systems
- RAID configuration and management utility in the system BIOS.

5.8 Video Controller

The Intel® Server Board SE7501WV2 provides an ATI* Rage XL PCI graphics accelerator, along with 8 MB of video DDR and support circuitry for an embedded SVGA video subsystem. The ATI Rage XL chip contains a SVGA video controller, clock generator, 2D and 3D engine, and RAMDAC in a 272-pin PBGA. One 2Mx32 SDRAM chip provides 8 MB of video memory.

The SVGA subsystem supports a variety of modes, up to 1600 x 1200 resolution in 8/16/24/32 bpp modes under 2D, and up to 1024 x 768 resolution in 8/16/24/32 bpp modes under 3D. It also supports both CRT and LCD monitors up to a 100 Hz vertical refresh rate.

The Intel® Server Board SE7501WV2 provides a standard 15-pin VGA connector and supports disabling of the on-board video through the BIOS setup menu or when a plug-in video card is installed in any of the PCI slots.

5.8.1 Video Modes

The ATI* Rage XL chip supports all standard IBM VGA modes. The following table shows the 2D/3D modes supported for both CRT and LCD.

[2] For more details on Integrated SCSI mirroring/striping or HostRAID, see the Adaptec* HostRAID User's Guide.

Table 32. Video Modes

2D Mode	Refresh Rate (Hz)	Intel® Server Board SE7501WV2 2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
800x600	60, 70, 75, 90, 100	Supported	Supported	Supported	Supported
1024x768	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
1280x1024	43, 60	Supported	Supported	Supported	Supported
1280x1024	70, 72	Supported	–	Supported	Supported
1600x1200	60, 66	Supported	Supported	Supported	Supported
1600x1200	76, 85	Supported	Supported	Supported	–
3D Mode	**Refresh Rate (Hz)**	**Intel® Server Board SE7501WV2 3D Video Mode Support with Z Buffer Enabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	–	–
1600x1200	60,66,76,85	Supported	–	–	–
3D Mode	**Refresh Rate (Hz)**	**Intel® Server Board SE7501WV2 3D Video Mode Support with Z Buffer Disabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	Supported	–
1600x1200	60,66,76,85	Supported	Supported	–	–

5.8.2 Video Memory Interface

The memory controller subsystem of the ATI* Rage XL arbitrates requests from direct memory interface, the VGA graphics controller, the drawing coprocessor, the display controller, the video scalar, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

The Intel® Server Board SE7501WV2 supports a 8-MB (512K x 32bit x 4 banks) SDRAM device for video memory. The following table shows the video memory interface signals.

Table 33. Video Memory Interface

Signal Name	I/O Type	Description
CAS#	O	Column Address Select
CKE	O	Clock Enable for Memory
CS#[1. .0]	O	Chip Select for Memory
DQM[7..0]	O	Memory Data Byte Mask
DSF	O	Memory Special Function Enable
HCLK	O	Memory Clock
[11..0]	O	Memory Address Bus
MD[31..0]	I/O	Memory Data Bus

RAS#	O	Row Address Select
WE#	O	Write Enable

5.9 Network Interface Controller (NIC)

The Intel® Server Board SE7501WV2 supports a dual-channel gigabit network interface controller based on the Intel® 82546EB. The 82546EB is a highly integrated PCI LAN controller in a 21 mm^2 PBGA package. The controller supports 10/100/1000 operation on both channels as well as supports alert-on-LAN functionality. The Intel® Server Board SE7501WV2 supports independent disabling of the two NIC controllers using the BIOS Setup menu.

The 82546EB chipset supports the following features:

- 32-bit PCI/CarBus master interface
- Integrated IEEE 802.3 10Base-T, 100Base-TX and 1000Base-TX compatible PHY
- IEEE 820.3u auto-negotiation support
- Full duplex support at 10 Mbps, 100Mbps and 1000 Mbps operation
- Integrated UNDI ROM support
- MDI/MDI-X and HWI support
- Low power +3.3 V device

5.9.1 NIC Connector and Status LEDs

The 82546EB drives two LEDs located on each network interface connector. The link/activity LED (to the left of the connector) indicates network connection when on, and Transmit/Receive activity when blinking. The speed LED (to the right of the connector) indicates 1000-Mbps operations when amber, 100-Mbps operations when green, and 10-Mbps when off.

5.10 Interrupt Routing

The Intel® Server Board SE7501WV2 interrupt architecture accommodates both PC-compatible PIC mode and APIC mode interrupts through use of the integrated APICs in the ICH3-S and the P64H2.

5.10.1 Legacy Interrupt Routing

For PC-compatible mode, the ICH3-S provides two 82C59-compatible interrupt controllers. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing.

5.10.1.1 Legacy Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on the Intel® Server Board SE7501WV2. The actual interrupt map is defined using configuration registers in the ICH3-S.

Table 34. Interrupt Definitions

ISA Interrupt	Description
INTR	Processor interrupt.

ISA Interrupt	Description
NMI	NMI to processor.
IRQ1	Keyboard interrupt.
IRQ3	Serial port A or B interrupt from SIO device, user-configurable.
IRQ4	Serial port A or B interrupt from SIO device, user-configurable.
IRQ5	
IRQ6	Floppy disk.
IRQ7	
IRQ8_L	Active low RTC interrupt.
IRQ9	
IRQ10	
IRQ11	
IRQ12	Mouse interrupt.
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1.
IRQ15	
SMI*	System Management Interrupt. General purpose indicator sourced by the ICH3-S and BMC to the processors.
SCI*	System Control Interrupt. Used by system to change sleep states and other system level type functions.

5.10.2 Serialized IRQ Support

The Intel® Server Board SE7501WV2 supports a serialized interrupt delivery mechanism. Serialized IRQs (SERIRQ) consist of a start frame, a minimum of 17 IRQ / data channels, and a stop frame. Any slave device in the quiet mode may initiate the start frame. While in the continuous mode, the start frame is initiated by the host controller.

5.10.3 APIC Interrupt Routing

For APIC mode, the Intel® Server Board SE7501WV2 interrupt architecture incorporates three Intel® APIC devices to manage and broadcast interrupts to local APICs in each processor. One of the APICs is located in the ICH3-S and the other two APICs are in the P64H2 (one for each PCI bus). The I/O APICs monitor each interrupt on each PCI device, including the PCI. When an interrupt occurs, a message corresponding to the interrupt is sent across the FSB processors.

The following table shows how the interrupts from the embedded devices and the PCI-X slots are connected.

Table 35. Intel® Server Board SE7501WV2 Interrupt Mapping

	IRQ	Device				
		PCI Riser Connector	PCI Riser Slot 1	PCI Riser Slot 2	PCI Riser Slot 3	Other
ICH3	IRQA					P64H2
	IRQB					Video
	IRQC					
	IRQD					
	IRQE					
	IRQF					
	IRQG					
	IRQH					

	IRQ14					Pri IDE
	IRQ15					Sec IDE
	SER IRQ					SIO
P64H2 Ch A	IRQ0	LP INTA	LP INTA	LP INTD	LP INTC	
	IRQ1*	LP INTC	LP INTC			SCSI INTB
	IRQ2*	LP INTD	LP INTD			SCSI INTA
	IRQ3	LP INTB	LP INTB	LP INTA	LP INTD	
	IRQ4	LP TDO		LP INTB	LP INTA	
	IRQ5	LP TCK		LP INTC	LP INTB	
	IRQ6					
	IRQ7					
	IRQ8					
	IRQ9					
	IRQ10					
	IRQ11					
	IRQ12					
	IRQ13					
	IRQ14					
	IRQ15					
P64H2 Ch B	IRQ1	FL INTC	FL INTC			
	IRQ2	FL INTD	FL INTD			
	IRQ3	FL INTB	FL INTB	FL INTA	FL INTD	
	IRQ4	FL TDO		FL INTB	FL INTA	
	IRQ5	FL TCK		FL INTC	FL INTB	
	IRQ6					Gigabit Ch A
	IRQ7					Gigabit Ch B
	IRQ8					
	IRQ9					
	IRQ10					
	IRQ11					
	IRQ12					
	IRQ13					
	IRQ14					
	IRQ15					

Notes:

LP = Low Profile

FL = Full Length

6. Server Management

The Intel® Server Board SE7501WV2 server management features are implemented using the Sahalee server board management controller chip. The Sahalee BMC is an ASIC packaged in a 156-pin BGA that contains a 32-bit RISC processor core and associated peripherals. The following diagram illustrates the Intel® Server Board SE7501WV2 server management architecture.

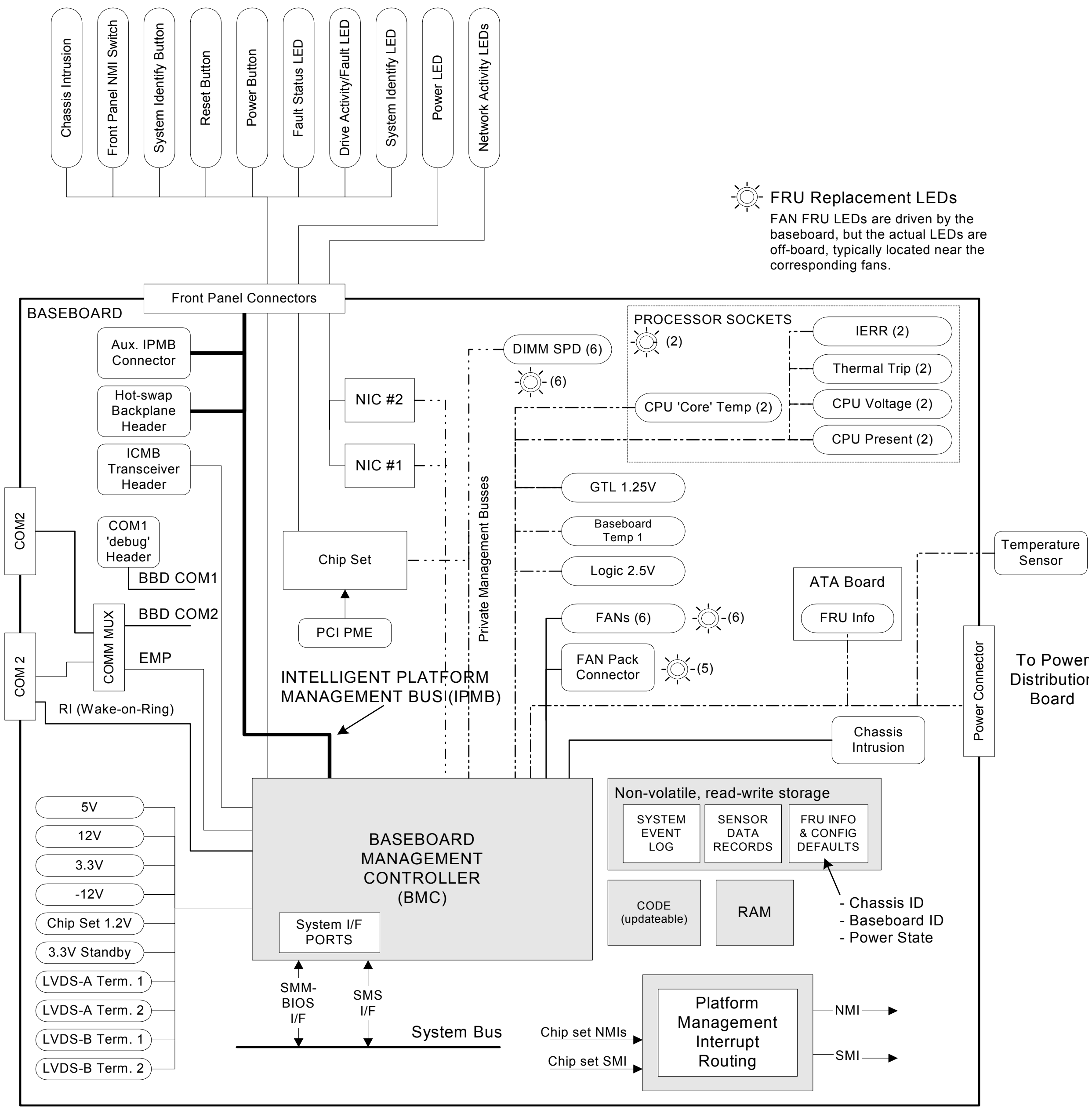


Figure 37. Intel® Server Board SE7501WV2 Sahalee BMC Block Diagram

6.1 Sahalee Baseboard Management Controller (BMC)

The Sahalee BMC contains a 32-bit RISC processor core and associated peripherals used to monitor the system for critical events. The Sahalee BMC, packaged in a 156-pin BGA, monitors all power supplies, including those generated by the external power supplies and those regulated locally on the server board. The Sahalee BMC also monitors SCSI termination voltage, fan tachometers for detecting a fan failure, and system temperature. Temperature is measured on each of the processors and at locations on the server board away from the fans. When any monitored parameter is outside of defined thresholds, the Sahalee BMC logs an event in the system event log.

Management controllers and sensors communicate on the I^2C*-based Intelligent Platform Management Bus (IPMB). Attached to one of its private I^2C bus is the Heceta5, an ADM1026 device, which is a versatile systems monitor ASIC. Some of its features include:

- Analog measurement channels
- Fan speed measurement channels
- General-Purpose Logic I/O pins
- Remote temperature measurement
- On-chip temperature sensor
- Chassis intrusion detect

The following table details the inputs/outputs of the Sahalee BMC as used in the SE7501WV2 server system.

Table 36. BMC Pinout

Pin #	Pin Name	Signal	Type/ Config	Description
D1	RST*	BMC_RST_DLY_L	input	Delayed version of A/C power-on reset signal from Heceta5
M7	XTAL2	TP_SAH_XTAL2	output	Unused
P8	XTAL1	CLK_40M_BMC	input	40MHz clock from SIO
C3	VREF	VREF_A_BMC_2P5V	input	+2.5v reference voltage from Heceta5
A3	A2D0	TP_BMC_16	input	
B4	A2D1	TP_TIC2_A2D<1>	input	
C4	A2D2	TP_BMC_15	input	
A4	A2D3	TP_BMC_A2D<3>	input	
D5	A2D4	TP_BMC_A2D<4>	input	
B5	A2D5	TP_BMC_A2D<5>	input	
C5	A2D6	PV_TERMPWR_SCWB_SCALED	input	SCSI Wide B Terminator voltage monitor.
A5	A2D7	PV_TERMPWR_SCWA_SCALED	input	SCSI Wide A Terminator voltage monitor.
J13	XINT0	RST_PWRGD_PS	input	Power Good signal from power supply
K11	XINT1	ICH3_SLP_S5_L	input	Sleep S5 signal from chipset ICH3
K12	XINT2	ICH3_SLP_S1_L	input	Sleep S1 signal from ICH3.
K14	XINT3	ZZ_FRB3_TIMER_HALT_L	input	

Pin #	Pin Name	Signal	Type/ Config	Description
K13	XINT4	NIC1_SMBALERT_L	input	SMBus Alert Signal from NIC1 (82546EB) TCO port
L14	XINT5	ICH3_SMI_BUFF_L	input	
L12	XINT6	BMC_PCU12_PROCHOT_L	input	Prochot signal. Can be Polled or Interrupt
L13	XINT7	BMC_NMI_L	OD out/in	NMI signal, monitored or asserted by BMC
D4	LPCRST*	RST_PCIRST_L	input	Buffered ICH3 PCIRST
E2	LPCPD*	ICH3_SUS_STAT_L	input	Signal used to 3-state LPC outputs to prevent leakage
B11	LSMI*	BMC_SCI_L	OD output	SCI output signal
F4	LDRQ*	LPC_DRQ_L<0>	output	
G2	SYSIRQ	IRQ_SIO_SERIRQ	output	Connected to SIO GPIO06/XIRQ input
F3	LFRAME*	LPC_FRAME_L	input	
G1	LCLK	CLK_33M_BMC	input	
F1	LAD0	LPC_AD<0>	bidir	
F2	LAD1	LPC_AD<1>	bidir	
E3	LAD2	LPC_AD<2>	bidir	
E1	LAD3	LPC_AD<3>	bidir	
G3	CS1*	BMC_SRAM_CE_L	output	Chip enable for external SRAM
H1	CS0*	BMC_CS0_L	output	Chip enable for BMC flash/ memory mapped latch
M10	WE*	BMC_WE_L	output	Flash/SRAM write enable
N10	OE*	BMC_OE_L	output	Flash/SRAM output enable
M14	BW8*	BMC_SLP_BTN_L	OD output	Sleep input to ICH3
M13	IOCHRDY	FP_RST_BTN_L	input	Reset button signal from front panel
N14	BALE	FP_NMI_BTN_L	input	NMI button signal from front panel
P13	MEMR*	FP_ID_BTN_L	input	System ID signal from front panel
N13	MEMW*	FP_SLP_BTN_L	input	Sleep button signal from front panel. For ref chassis support. (Not supported)
M12	IOR*	BMC_SECURE_MODE_KB	input	Secure mode signal from SIO keyboard controller (pin 12)
N12	IOW*	FP_PWR_BTN_L	input	Power button signal from front panel
P12	SBHE*	BMC_SBHE_L	OD output	High byte enable to external SRAM and flash
M11	CE2*	RST_VRM_DIS_L	TP output	Disables CPU VRM.
N11	CE1*	BMC_VID_BLANK_L	TP output	Disables Hsync and Vsync video buffers
P11	REG*	BMC_CLR_CMOS_L	TP output	Clear CMOS signal asserted by BMC.
L4	ADDR0	BMC_A<0>	output	
P4	ADDR1	BMC_A<1>	output	
M4	ADDR2	BMC_A<2>	output	
N4	ADDR3	BMC_A<3>	output	
P3	ADDR4	BMC_A<4>	output	
P2	ADDR5	BMC_A<5>	output	
N2	ADDR6	BMC_A<6>	output	
N1	ADDR7	BMC_A<7>	output	

Pin #	Pin Name	Signal	Type/ Config	Description
M2	ADDR8	BMC_A<8>	output	
M3	ADDR9	BMC_A<9>	output	
L2	ADDR10	BMC_A<10>	output	
L3	ADDR11	BMC_A<11>	output	
L1	ADDR12	BMC_A<12>	output	
K4	ADDR13	BMC_A<13>	output	
K2	ADDR14	BMC_A<14>	output	
K3	ADDR15	BMC_A<15>	output	
K1	ADDR16	BMC_A<16>	output	
J2	ADDR17	BMC_A<17>	output	
J3	ADDR18	BMC_A<18>	output	
J1	ADDR19	BMC_A<19>	output	
H4	ADDR20	BMC_A<20>	output	Only used if a 16M flash part is populated, then unstuff pdn
H2	ADDR21	BMC_A<21>	output	
P10	DATA0	BMC_D<0>	bidir	
L9	DATA1	BMC_D<1>	bidir	
N9	DATA2	BMC_D<2>	bidir	
M9	DATA3	BMC_D<3>	bidir	
P9	DATA4	BMC_D<4>	bidir	
L8	DATA5	BMC_D<5>	bidir	
N8	DATA6	BMC_D<6>	bidir	
P7	DATA7	BMC_D<7>	bidir	
N7	DATA8	BMC_D<8>	bidir	
M6	DATA9	BMC_D<9>	bidir	
P6	DATA10	BMC_D<10>	bidir	
N6	DATA11	BMC_D<11>	bidir	
L5	DATA12	BMC_D<12>	bidir	
M5	DATA13	BMC_D<13>	bidir	
P5	DATA14	BMC_D<14>	bidir	
N5	DATA15	BMC_D<15>	bidir	
J14	BAUD	BMC_IRQ_SMI_L	OD output	Need to connect to SMI capable pin at ICH3
J12	RI*	SPB_RI_L	input	Serial 2 ring indicate signal.
F14	DTR0*	SPB_DTR_L	output	Serial 2 DTR signal.
F12	DCD0*	SPB_DCD_L	input	Serial 2 DCD signal.
F13	CTS0*	SPB_CTS_L	input	Serial 2 CTS signal.
F11	RTS0*	SPB_RTS_L	output	Serial 2 RTS signal.
E12	RX0	SPB_SIN	input	Serial 2 serial input signal
E13	TX0	SPB_SOUT	output	Serial 2 serial output signal
J11	DTR1*	BMC_LATCH_OE_L	TP output	Enables output of expansion latch
H13	DCD1*	BMC_ICMB_RX	input	ICMB receive data interrupt signal (same as ICMB serial input)
H14	CTS1*	NSI_BMC_FRC_UPDATE_L	input	Forces BMC to run from boot block code.

Pin #	Pin Name	Signal	Type/ Config	Description
H12	RTS1*	BMC_ICMB_TX_ENB _L	TP output	ICMB transceiver enable signal, asserted by BMC
G14	RX1	BMC_ICMB_RX	input	ICMB serial receive data
G13	TX1	BMC_ICMB_TX	output	ICMB serial send data
A12	TIC1_OUT	BMC_SPKR_L	TP output	BMC speaker tone enable signal (for beeps)
B12	TIC2_IN0	FAN_TACH1	input	
A13	TIC2_IN1	FAN_TACH2	input	
B13	TIC2_IN2	FAN_TACH3	input	
B14	TIC2_IN3	FAN_TACH4	input	
C13	TIC2_IN4	FAN_TACH5	input	
C14	TIC2_IN5	FAN_TACH6	input	PWT fan, CPU1
D13	TIC2_IN6	FAN_TACH7	input	PWT fan, CPU2
D12	TIC2_IN7	BMC_CPU1_SKTOCC_L	input	Socket occupied signal from CPU1
D14	TIC3_0UT	BMC_CPU2_SKTOCC_L	input	Socket occupied signal from CPU2
E11	TIC4_IN	SIO_CLK_32K_RTC_BMC	input	32kHz clock signal from IHC3
C10	LED0	BSEL_EQUAL_L	input	XOR gate compares CPU's BSEL: if equal, XOR will output a LO. Otherwise HI
A10	LED1	ZZ_BMC_ROLLING_BIOS_L	TP output	ROLLING BIOS flash control pin
B10	LED2	ZZ_SPA_SWITCH_EN	TP output	Connects to serial port Mux logic allowing SPA to route to back in 1U chassis with SOL enabled
D11	LED3	BMC_PWR_BTN_L	TP output	Power button signal from BMC to ICH3
A11	LED4	BMC_PS_PWR_ON_L	TP output	Power On signal to power supply
C11	LED5	RST_P6_PWR_GOOD	TP output	Chipset power good/rst signal
A6	SDA0	IPMB_I2C_5VSB_SDA	bidir	IPMB I2C data
B6	SCL0	IPMB_I2C_5VSB_SCL	bidir	IPMB I2C clock
B7	SDA1	SMB_I2C_3VSB_SDA	bidir	SMB I2C Bus data
D7	SCL1	SMB_I2C_3VSB_SCL	bidir	SMB I2C Bus clock
C8	SDA2	PB1_I2C_5VSB_SDA	bidir	BMC Private I2C Bus 1 - data.
A7	SCL2	PB1_I2C_5VSB_SCL	bidir	BMC Private I2C Bus 1 - clock.
B8	SDA3	SERIAL_TO_LAN_L	TP output	Serial bus cross-bar enable for null modem operation through BMC to LAN.
A8	SCL3	EMP_INUSE_L	input	This status signal from the front panel indicates that something is plugged into Serial 2 RJ45.
C9	SDA4	PB3_I2C_3V_SDA	bidir	BMC Private I2C Bus 3 - data
D9	SCL4	PB3_I2C_3V_SCL	bidir	BMC Private I2C Bus 3 - clock
B9	SDA5	PB4_I2C_3VSB_SDA	bidir	BMC Private I2C Bus 4 - data
A9	SCL5	PB4_I2C_3VSB_SCL	bidir	BMC Private I2C Bus 4 - clock
C1	TMS	BMC_TMS	input	Sahalee JTAG signal
D2	TCK	BMC_TCK	input	Sahalee JTAG signal
B2	TDI	BMC_TDI	input	Sahalee JTAG signal
B1	TDO	BMC_TDO	output	Sahalee JTAG signal
C2	TRST*	BMC_TRST_L	input	Sahalee JTAG signal
D3	TEST_MODE*	PULLUP	input	Sahalee test mode signal, should be pulled high.

Pin #	Pin Name	Signal	Type/ Config	Description
D6	AVDD	SB5V	pwr/gnd	
M1	VDD5V	SB5V	pwr/gnd	
E14	VDD5V	SB5V	pwr/gnd	
E4	IOVCC	SB3V	pwr/gnd	
N3	IOVCC	SB3V	pwr/gnd	
L10	IOVCC	SB3V	pwr/gnd	
G11	IOVCC	SB3V	pwr/gnd	
D10	IOVCC	SB3V	pwr/gnd	
H3	COREVCC	SB3V	pwr/gnd	
M8	COREVCC	SB3V	pwr/gnd	
G12	COREVCC	SB3V	pwr/gnd	
C7	COREVCC	SB3V	pwr/gnd	
B3	AVS	GND	pwr/gnd	
A2	AVSUB	GND	pwr/gnd	
J4	IOGND	GND	pwr/gnd	
L6	IOGND	GND	pwr/gnd	
L11	IOGND	GND	pwr/gnd	
C12	IOGND	GND	pwr/gnd	
C6	IOGND	GND	pwr/gnd	
G4	COREGND	GND	pwr/gnd	
L7	COREGND	GND	pwr/gnd	
H11	COREGND	GND	pwr/gnd	
D8	COREGND	GND	pwr/gnd	

An ADM1026 has been attached to the Private 1 I^2C bus for monitoring the system temperature, additional analog voltages, and the voltage identifications bits for both processors. The following table describes these added signals. The ADM1026 device also provides a PWM (Pulse Width Modulation) for fan speed control.

Table 37. ADM1026 Input Definition

Pin #	Pin Name	Signal	Type/ Config	Description
1	GPIO9	BMC_CPU2_IERR_L	input	This is the IERR signal from CPU2
2	GPIO8	BMC_CPU1_IERR_L	input	This is the IERR signal from CPU1
3	FAN0/GPIO0	BMC_DIS_CPU1_L	output	
4	FAN1/GPIO1	BMC_DIS_CPU1_L	output	
5	FAN2/GPIO2	VID_CPU2<0>	input	
6	FAN3/GPIO3	VID_CPU2<1>	input	
7	VDD	VCC3	pwr/gnd/in	
8	DGND	GND	pwr/gnd	
9	FAN4/GPIO4	VID_CPU2<2>	input	
10	FAN5/GPIO5	VID_CPU2<3>	input	
11	FAN6/GPIO6	VID_CPU2<4>	input	

Pin #	Pin Name	Signal	Type/ Config	Description
12	FAN7/GPIO7	VID_CPU1<0>	input	
13	SCL	PB1_I2C_5VSB_SCL	bidir	BMC Private I2C Bus 1 - clock
14	SDA	PB1_I2C_5VSB_SDA	bidir	BMC Private I2C Bus 1 - data
15	ADDR/NTESTOUT	PD_HEC5_ADDR	input	I2C address selection signal - I2C addr = 0X58
16	CHS_INT	NSI_CHASSIS_INTRUSION	input	Chassis intrusion signal
17	INT*	TP_HEC5_INT_L	output	This pin does not yet have a specified connection.
18	PWM	FAN_PWM_CNTRL	output	Fan speed control signal
19	RESET_STBY*	RST_BMC_RST_L	output	AC PowerOn reset
20	RESET*	TP_HEC5_RESET_L	in/out	This pin does not yet have a specified connection.
21	AGND	GND	pwr/gnd	
22	STBY_VDD	P3V3_STBY	pwr/gnd/in	
23	DAC	TP_HEC5_DAC	output	This pin does not yet have a specified connection.
24	VREF	VREF_A_BMC_2P5V	output	Analog input reference to Sahalee
25	D1-/NTESTIN	ZZ_CPU1_THERMDC	output	
26	D1+	ZZ_CPU1_THERMDA	input	
27	D2-/AIN9	ZZ_CPU2_THERMDC	output	
28	D2+/AIN8	ZZ_CPU2_THERMDA	input	
29	VBAT	P2V5_NIC	input	Baseboard P2V5_NIC monitor
30	+5V	P5V	input	Baseboard P5V monitor
31	-12V	N12V	input	Baseboard N12V monitor
32	+12V	P12V	input	Baseboard P12V monitor
33	VCCP	P_VCCP	input	Baseboard P_VCCP monitor
34	AIN7	P1V2	input	Baseboard P1V2 monitor
35	AIN6	P1V25_VTT	input	Baseboard P1V25_VTT monitor
36	AIN5	P12V_VRM_SCALED	input	External attenuator=232/(232+1k)~0.19
37	AIN4	P1V8	input	Baseboard P1V8 monitor
38	AIN3	P2V5	input	Baseboard P2V5 monitor
39	AIN2	P5V_STBY_SCALED	input	External attenuator=1k/(1k+1k)=0.5
40	AIN1	P1V8_STBY	input	Baseboard P1V8_STBY monitor
41	AIN0	P3V3_VAUX	input	External attenuator=499k/(499+365~=0.58
42	THERM*/GPIO16	TP_HEC5_GPIO16	gpio	This pin does not yet have a specified connection.
43	GPIO15	BMC_CPU2_THRMTRIP_L	input	Processor Thermal Trip signal from CPU2
44	GPIO14	BMC_CPU1_THRMTRIP_L	input	Processor Thermal Trip signal from CPU1
46	GPIO13	VID_CPU1<3>	input	
45	GPIO12	VID_CPU1<4>	input	
47	GPIO11	VID_CPU1<2>	input	
48	GPIO10	VID_CPU1<1>	input	

6.1.1 Fault Resilient Booting

The Sahalee BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If the default bootstrap processor (BSP) fails to complete the boot process, FRB attempts to boot using an alternate processor.

- FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.
- FRB level 2 is for recovery from a watchdog timeout during POST. The watchdog timer for FRB level 2 detection is implemented in the Sahalee BMC.
- FRB level 3 is for recovery from a watchdog timeout on hard reset or power-up. The Sahalee BMC provides hardware functionality for this level of FRB.

6.1.1.1 FRB-1

In a multiprocessor system, the BIOS registers the application processors in the MP table and the ACPI tables. When started by the BSP, if an AP fails to complete initialization within a certain time, it is assumed nonfunctional. If the BIOS detects that an application processor has failed BIST or is nonfunctional, it requests the BMC to disable that processor. The BMC then generates a system reset while disabling the processor; the BIOS will not see the bad processor in the next boot cycle. The failing AP is not listed in the MP table (refer to the *Multi-Processor Specification, Rev. 1.4*), nor in the ACPI APIC tables, and is invisible to the operating system. If the BIOS detects that the BSP has failed BIST, it sends a request to the BMC to disable the present processor. If there is no alternate processor available, the BMC beeps the speaker and halts the system. If BMC can find another processor, BSP ownership is transferred to that processor via a system reset.

6.1.1.2 FRB-2

The second watchdog timer (FRB-2) in the BMC is set for approximately 6 minutes by BIOS and is designed to guarantee that the system completes BIOS POST. The FRB-2 timer is enabled before the FRB-3 timer is disabled to prevent any “unprotected” window of time.

Near the end of POST, before the option ROMs are initialized, the BIOS disables the FRB-2 timer in the BMC. If the system contains more than 1 GB of memory and the user chooses to test every DWORD of memory, the watchdog timer is disabled before the extended memory test starts, because the memory test can take more than 6 minutes under this configuration. If the system hangs during POST, the BIOS does not disable the timer in the BMC, which generates an asynchronous system reset (ASR).

6.1.1.3 FRB-3

The first timer (FRB-3) starts counting down whenever the system comes out of hard reset, which is usually about 5 seconds. If the BSP successfully resets and starts executing, the BIOS disables the FRB-3 timer in the BMC by de-asserting the FRB3_TIMER_HLT* signal (GPIO) and the system continues with the POST. If the timer expires because of the BSP’s failure to fetch or execute BIOS code, the BMC resets the system and disables the failed processor. The system continues to change the bootstrap processor until the BIOS POST gets past disabling the FRB-3 timer in the BMC. The BMC sounds beep codes on the speaker, if it fails to find a good processor. The process of cycling through all the processors is repeated upon system reset or power cycle.

6.2 System Reset Control

Reset circuitry on the Intel® Server Board SE7501WV2 looks at resets from the front panel, ICH3-S, ITP, and the processor subsystem to determine proper reset sequencing for all types of resets. The reset logic is designed to accommodate several methods to reset the system, which can be divided into the following categories:

- Power-up reset
- Hard reset
- Soft (programmed) reset

The following subsections describe each type of reset.

6.2.1 Power-up Reset

When the system is disconnected from AC power, all logic on the server board is powered off. When a valid input (AC) voltage level is provided to the power supply, 5-volt standby power will be applied to the server board. The baseboard has a 5-volt to 3.3-volt regulator to produce 3.3-volt standby voltage. A power monitor circuit on 3.3-volt standby will assert BMCRST_L, causing the BMC to reset. The BMC is powered by 3.3-volt standby and monitors and controls key events in the system related to reset and power control.

After the system is turned on, the power supply will assert the RST_PWRGD_PS signal after all voltage levels in the system have reached valid levels. The BMC receives RST_PWRGD_PS and after 500 ms asserts RST_P6_PWR_GOOD, which indicates to the processors and ICH3-S that the power is stable. Upon RST_P6_PWR_GOOD assertion, the ICH3-S will toggle PCI reset.

6.2.2 Hard Reset

A hard reset can be initiated by resetting the system through the front panel switch. During the reset, the Sahalee BMC de-asserts RST_P6_PWR_GOOD. After 500 ms, it is reasserted, and the power-up reset sequence is completed.

The Sahalee BMC is not reset by a hard reset; it is only reset when AC power is applied to the system.

6.2.3 Soft Reset

A soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers. Soft resets can be generated by the keyboard controller located in the SIO, by the ICH3-S, or by the operating system.

6.3 Intelligent Platform Management Buses (IPMB)

Management controllers (and sensors) communicate on the I^2C-based Intelligent Platform Management Bus. A bit protocol, defined by the *I^2C Bus Specification*, and a byte-level protocol, defined by the *Intelligent Platform Management Bus Communications Protocol Specification*, provide an independent interconnect for all devices operating on this I^2C bus.

The IPMB extends throughout the server board and system chassis. An added layer in the protocol supports transactions between multiple servers on Inter-Chassis Management Bus (ICMB) I^2C segments.

The server board provides a 3-pin IPMB connector to support add-in cards with IPMB interface.

In addition to the "public" IPMB, the BMC also has three private I^2C busses. The BMC is the only master on the private busses. The following table lists all server board connections to the Sahalee BMC private I^2C busses.

Table 38. Intel® Server Board SE7501WV2 I²C Address Map

I²C Bus	I2C Addr	Device
PB1	0x58	Heceta5
	0x60	SIO
PB3	0x30	CPU1 therm sensor
	0x32	CPU2 therm sensor
	0x44	ICH3
	0x60	MCH
	0xA0	DIMM1
	0xA2	DIMM3
	0xA4	DIMM5
	0xA6	CPU1 SEEPROM
	0xA8	DIMM2
	0xAA	DIMM4
	0xAC	DIMM6
	0xAE	CPU2 SEEPROM
	0xC4	P64H2
	0xD2	CK408B
PB4		NIC

6.4 Inter Chassis Management Bus (ICMB)

The BMC on the Intel® Server Board SE7501WV2 has built in support for ICMB interface. An optional ICMB card is required to use this feature because the ICMB transceivers are not provided on the server board. A 5-pin ICMB connector on the Intel® Server Board SE7501WV2 provides the interface to the ICMB module.

6.5 Error Reporting

This section documents the types of system bus error conditions monitored by the Intel® Server Board SE7501WV2.

6.5.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors on the Intel® Server Board SE7501WV2, which can be disabled and enabled individually, can be categorized as follows:

- PCI bus errors
- Processor bus errors
- Memory single- and multi-bit errors
- General Server Management sensors

On the Intel® Server Board SE7501WV2, the general server management sensors are managed by the Sahalee BMC.

6.5.2 PCI Bus Errors

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled by BIOS.

6.5.3 Intel® Xeon™ Processor Bus Errors

The MCH supports the data integrity features supported by the Intel® Xeon™ bus, including address, request, and response parity. In addition, the MCH can generate BERR# on unrecoverable errors detected on the processor bus. Unrecoverable errors are routed to an NMI by the BIOS.

6.5.4 Memory Bus Errors

The MCH is programmed to generate an SMI on single-bit or double-bit data errors in the memory array if ECC memory is installed. The MCH performs the scrubbing. The SMI handler records the error and the DIMM location to the system event log.

6.5.5 Fault and Status LEDs

The Intel® Server Board SE7501WV2 uses system fault/status LEDs in many areas of the board. There are fault LEDs for the memory DIMMs, the fan headers, and the processors. There are also status LEDs for 5-volt stand-by and system status indication. A blue LED is provided as a system ID LED. When the error reporting system determines there is a problem with any device, it will light the LED of the failing component. In the event of a power switch power down or loss of AC, the status of all baseboard fault LEDs will be remembered and restored by BMC when AC is restored. Fault LEDs will only be reset when a Front Panel Reset is performed with main power available to the system or under control of an IPMI command.

6.5.5.1 DIMM LEDs

One LED for each DIMM will be illuminated if that DIMM has an uncorrectable or multi-bit memory ECC. These LEDs will maintain the same state across power switch power down or loss of AC. These LED's will only be reset when a Front Panel Reset is performed with main power available to the system or under control of an IPMI command.

6.5.5.2 CPU LEDs

There is one LED for each CPU. This LED will be illuminated if the associated processor has been disabled. These LEDs will maintain the same state across power switch power down or loss of AC. These LED's will only be reset when a Front Panel Reset is performed with main power available to the system or under control of an IPMI command.

6.5.5.3 Fan LEDs

One LED is provided for each fan header. This LED will be illuminated if the associated fan fails. These LEDs will maintain the same state across power switch power down or loss of AC. There is a consolidated fan fail LED for the fans powered by the fan assembly header (J3J2). These LED's will only be reset when a Front Panel Reset is performed with main power available to the system or under control of an IPMI command.

6.5.5.4 5VSB Status LED

One single-color LED is located next to the main power connector. This LED indicates the presence of 5-volt stand-by when AC power is applied to the system. AC is applied to the system as soon as the AC cord is plugged into the power supply.

6.5.5.5 System Status LED

The SE7501WV2 server board has a System Status LED, which can be found on the other side of the baseboard notch from the PORT80 diagnostic LEDs located near the back edge of the baseboard. This LED is tied to the front panel System Status LED and should reflect the same system status. The LED is a multi colored LED. The following table describes what each state signifies:

Table 39. System Status LEDs

LED	Color	State	Description
System Status [on standby power]	Green	ON	Running / Normal operation
		Blink	Degraded
	Amber	ON	Critical or Non-Recoverable Condition.
		Blink	Non-Critical condition.
	Off	OFF	POST / System Stop.

6.5.5.5.1 System Status Indications

Critical Condition

A critical condition is any critical or non-recoverable threshold crossing associated with the following events:

- Temperature, Voltage, or Fan critical threshold crossing
- Power Subsystem Failure. The BMC asserts this failure whenever it detects a power control fault (e.g., the BMC detects that the system power is remaining ON even though the BMC has de-asserted the signal to turn off power to the system).
  A hot-swap backplane would use the *Set Fault Indication* command to indicate when one or more of the drive fault status LEDs are asserted on the hot-swap backplane.
- The system is unable to power up due to incorrectly installed processor(s), or processor incompatibility.
- Satellite controller sends a critical or non-recoverable state, via the *Set Fault Indication* command to the BMC.
- “Critical Event Logging” errors.

Non-Critical Condition

- Temperature, Voltage, or Fan non-critical threshold crossing
- Chassis Intrusion
- Satellite controller sends a non-critical state, via the *Set Fault Indication* command, to the BMC.
- Set Fault Indication Command

Degraded Condition

- Non-redundant power supply operation. This only applies when the BMC is configured for a redundant power subsystem. The power unit configuration is configured via OEM SDR records.
- A processor is disabled by FRB or BIOS.
- BIOS has disabled or mapped out some of the system memory.

6.5.5.6 ID LED

The Blue ID LED, located at the back edge of the baseboard near the speaker, is used to help locate a given server platform requiring service when installed in a multi-system rack. The LED is lit when the front panel ID button is pressed and it is turned off when the button is pressed again. A user-defined interface can be developed to activate the ID LED remotely.

6.5.5.7 POST Code Diagnostic LEDs

To help diagnose POST failures, a set of four bi-color diagnostic LEDs is located on the back edge of the baseboard. Each of the four LEDs can have one of four states: Off, Green, Red, or Amber. During the POST process, each light sequence represents a specific Port-80 POST code. If a system should hang during POST, the diagnostic LEDs will present the last test executed before the hang. When reading the lights, the LEDs should be observed from the back of the system. The most significant bit (MSB) is the first LED on the left, and the least significant bit (LSB) is the last LED on the right.

Table 40. Boot Block POST Progress Codes

	Diagnostic LED Decoder G=Green, R=Red, A=Amber				**Description**
	Hi			**Low**	
10h	Off	Off	Off	R	The NMI is disabled. Start Power-on delay. Initialization code checksum verified.
11h	Off	Off	Off	A	Initialize the DMA controller, perform the keyboard controller BAT test, start memory refresh, and enter 4 GB flat mode.
12h	Off	Off	G	R	Get start of initialization code and check BIOS header.
13h	Off	Off	G	A	Memory sizing.
14h	Off	G	Off	R	Test base 512K of memory. Return to real mode. Execute any OEM patches and set up the stack.
15h	Off	G	Off	A	Pass control to the uncompressed code in shadow RAM. The initialization code is copied to segment 0 and control will be transferred to segment 0.
16h	Off	G	G	R	Control is in segment 0. Verify the system BIOS checksum. If the system BIOS checksum is bad, go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
17h	Off	G	G	A	Pass control to the interface module.
18h	G	Off	Off	R	Decompress of the main system BIOS failed.
19h	G	Off	Off	A	Build the BIOS stack. Disable USB controller. Disable cache.
1Ah	G	Off	G	R	Uncompress the POST code module. Pass control to the POST code module.
1Bh	A	R	Off	R	Decompress the main system BIOS runtime code.
1Ch	A	R	Off	A	Pass control to the main system BIOS in shadow RAM.

	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	Hi			Low	
E0h	R	R	R	Off	Start of recovery BIOS. Initialize interrupt vectors, system timer, DMA controller, and interrupt controller.
E8h	A	R	R	Off	Initialize extra module if present.
E9h	A	R	R	G	Initialize floppy controller.
EAh	A	R	A	Off	Try to boot floppy diskette.
EBh	A	R	A	G	If floppy boot fails, initialize ATAPI hardware.
ECh	A	A	R	Off	Try booting from ATAPI CD-ROM drive.
EEh	A	A	A	Off	Jump to boot sector.
EFh	A	A	A	G	Disable ATAPI hardware.
20h	Off	Off	R	Off	Uncompress various BIOS Modules
22h	Off	Off	A	Off	Verify password Checksum
24h	Off	G	R	Off	Verify CMOS Checksum.
26h	Off	G	A	Off	Read Microcode updates from BIOS ROM.
28h	G	Off	R	Off	Initializing the processors. Set up processor registers. Select least featured processor as the BSP.
2Ah	G	Off	A	Off	Go to Big Real Mode
2Ch	G	G	R	Off	Decompress INT13 module
2Eh	G	G	A	Off	Keyboard Controller Test: The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller
30h	Off	Off	R	R	Keyboard/Mouse port swap, if needed
32h	Off	Off	A	R	Write Command Byte 8042: The initialization after the keyboard controller BAT command test is done. The keyboard command byte will be written next.
34h	Off	G	R	R	Keyboard Init: The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands
36h	Off	G	A	R	Disable and initialize 8259
38h	G	Off	R	R	Detect Configuration Mode, such as CMOS clear.
3Ah	G	Off	A	R	Chipset Initialization before CMOS initialization
3Ch	G	G	R	R	Init System Timer: The 8254 timer test is over. Starting the legacy memory refresh test next.
3Eh	G	G	A	R	Check Refresh Toggle: The memory refresh line is toggling. Checking the 15 second on/off time next
40h	Off	R	Off	Off	Calculate CPU speed
42h	Off	R	G	Off	Init interrupt Vectors: Interrupt vector initialization is done.
44h	Off	A	Off	Off	Enable USB controller in chipset
46h	Off	A	G	Off	Initialize SMM handler. Initialize USB emulation.
48h	G	R	Off	Off	Validate NVRAM areas. Restore from backup if corrupted.
4Ah	G	R	G	Off	Load defaults in CMOS RAM if bad checksum or CMOS clear jumper is detected.
4Ch	G	A	Off	Off	Validate date and time in RTC.
4Eh	G	A	G	Off	Determine number of micro code patches present
50h	Off	R	Off	R	Load Micro Code To All CPUs
52h	Off	R	G	R	Scan SMBIOS GPNV areas
54h	Off	A	Off	R	Early extended memory tests

	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	Hi			Low	
56h	Off	A	G	R	Disable DMA
58h	G	R	Off	R	Disable video controller
5Ah	G	R	G	R	8254 Timer Test on Channel 2
5Ch	G	A	Off	R	Enable 8042. Enable timer and keyboard IRQs. Set Video Mode: Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
5Eh	G	A	G	R	Init PCI devices and motherboard devices. Pass control to video BIOS. Start serial console redirection.
60h	Off	R	R	Off	Initialize memory test parameters
62h	Off	R	A	Off	Initialize AMI display manager Module. Initialize support code for headless system if no video controller is detected.
64h	Off	A	R	Off	Start USB controllers in chipset
66h	Off	A	A	Off	Set up video parameters in BIOS data area.
68h	G	R	R	Off	Activate ADM: The display mode is set. Displaying the power-on message next.
6Ah	G	R	A	Off	Initialize language module. Display splash logo.
6Ch	G	A	R	Off	Display Sign on message, BIOS ID and processor information.
6Eh	G	A	A	Off	Detect USB devices
70h	Off	R	R	R	Reset IDE Controllers
72h	Off	R	A	R	Displaying bus initialization error messages.
74h	Off	A	R	R	Display Setup Message: The new cursor position has been read and saved. Displaying the Hit Setup message next.
76h	Off	A	A	R	Ensure Timer Keyboard Interrupts are on.
78h	G	R	R	R	Extended background memory test start
7Ah	G	R	A	R	Disable parity and NMI reporting.
7Ch	G	A	R	R	Test 8237 DMA Controller: The DMA page register test passed. Performing the DMA Controller 1 base register test next
7Eh	G	A	A	R	Init 8237 DMA Controller: The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
80h	R	Off	Off	Off	Enable Mouse and Keyboard: The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next
82h	R	Off	G	Off	Keyboard Interface Test: A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
84h	R	G	Off	Off	Check Stuck Key Enable Keyboard: The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
86h	R	G	G	Off	Disable parity NMI: The command byte was written and global data initialization has completed. Checking for a locked key next
88h	A	Off	Off	Off	Display USB devices
8Ah	A	Off	G	Off	Verify RAM Size: Checking for a memory size mismatch with CMOS RAM data next
8Ch	A	G	Off	Off	Lock out PS/2 keyboard/mouse if unattended start is enabled.
8Eh	A	G	G	Off	Init Boot Devices: The adapter ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
90h	R	Off	Off	R	Display IDE mass storage devices.

	Diagnostic LED Decoder G=Green, R=Red, A=Amber				**Description**
	Hi			**Low**	
92h	R	Off	G	R	Display USB mass storage devices.
94h	R	G	Off	R	Report the first set of POST Errors To Error Manager.
96h	R	G	G	R	Boot Password Check: The password was checked. Performing any required programming before Setup next.
98h	A	Off	Off	R	Float Processor Initialize: Performing any required initialization before the coprocessor test next.
9Ah	A	Off	G	R	Enable Interrupts 0,1,2: Checking the extended keyboard, keyboard ID, and NUM Lock key next. Issuing the keyboard ID command next
9Ch	A	G	Off	R	Init FDD Devices. Report second set of POST errors To Error messager
9Eh	A	G	G	R	Extended background memory test end
A0h	R	Off	R	Off	Prepare And Run Setup: Error manager displays and logs POST errors. Waits for user input for certain errors. Execute setup.
A2h	R	Off	A	Off	Set Base Expansion Memory Size
A4h	R	G	R	Off	Program chipset setup options, build ACPI Tables, build INT15h E820h table
A6h	R	G	A	Off	Set Display Mode
A8h	A	Off	R	Off	Build SMBIOS table and MP tables.
AAh	A	Off	A	Off	Clear video screen.
ACh	A	G	R	Off	Prepare USB controllers for operating system
AEh	A	G	A	Off	One Beep to indicate end of POST. No beep if silent boot is enabled.
000h	Off	Off	Off	Off	POST completed. Passing control to INT 19h boot loader next.

6.5.6 Temperature Sensors

The Intel® Server Board SE7501WV2 has the ability to measure system and board temperature from a variety of sources. The first is located inside the Heceta chip (U6G1) and is used to measure the baseboard temperature. In addition, diodes located inside each processor are used by the Intel® Server Board SE7501WV2 to monitor temperature at the processors.

7. BIOS

This section describes the BIOS-embedded software for the Intel® Server Board SE7501WV2. This section also describes BIOS support utilities that are required for system configuration (ROM resident) and flash ROM update (not ROM resident). The BIOS contains standard PC-compatible basic input/output (I/O) services and standard Intel® server features.

The BIOS is implemented as firmware that resides in the flash ROM. Support for applicable baseboard peripheral devices (SCSI, NIC, video adapters, etc.) that are also loaded into the baseboard flash ROM are not specified in this document. Hooks are provided to support adding BIOS code for these adapters. The binaries for these must be obtained from the peripheral device manufacturers and loaded into the appropriate locations.

7.1 System Flash ROM Layout

The flash ROM contains system initialization routines, the BIOS Setup Utility, and runtime support routines. The exact layout is subject to change, as determined by Intel. A 16 KB user block is available for user ROM code or custom logos. A 96 KB area is used to store the string database. The flash ROM also contains initialization code in compressed form for on-board peripherals, like SCSI and video controllers.

The complete ROM is visible, starting at physical address 4 GB minus the size of the flash ROM device. Only the BIOS needs to know the exact map. The BIOS image contains all of the BIOS components at appropriate locations. The Flash Memory Update utility loads the BIOS image minus the recovery block to the flash.

Because of shadowing, none of the flash blocks is visible at the aliased addresses below 1 MB.

A 16 KB parameter block in the flash ROM is dedicated to storing configuration data that controls the system configuration (ESCD) and the on-board SCSI configuration. Application software must use standard APIs to access these areas; application software cannot access the data directly.

7.2 BIOS Boot Specification Compliance

The BIOS conforms to the *BIOS Boot Specification (BBS)*, Revision 1.01, which describes the method used to identify all initial program load (IPL) devices in the system, prioritizes them in the order selected in Setup, and then sequentially attempts to boot from each device.

If more than one non-BBS compliant device exists in the system, the boot device is determined by the option ROM scan order. Option ROMs residing lower in memory are scanned first. In some instances, control of which non-BBS compliant device from which the system is booted may be achieved by moving the adapter cards to different slots in the system. The BIOS may include special code and may be able to selectively boot from one of several non-BBS compliant devices in the system. Such techniques do not always work and are outside the scope of this document.

BIOS Setup provides boot order options including: CD-ROM, hard drive, removable device, and other bootable devices such as a network card or a SCSI CD-ROM. The system BIOS tries to boot from devices in the order specified by Setup. BIOS Setup also allows the C: drive to be any hard drive that is controlled by a *Boot BIOS Specification* compliant option ROM BIOS, including drives attached to the on-board SCSI controller or on-board IDE.

Hard drives that are controlled by non-BBS compliant devices may appear under a different name, based on the BIOS vendor. The user may or may not be able to control the order on a drive-by-drive basis for such controllers. Some BBS compliant option ROM BIOSes may present all the drives as a single device, and may not allow the user to manipulate the order on a drive-by-drive basis. If booting from a hard drive, the user is responsible for making sure that the C: drive has a bootable image.

The BIOS is limited to a maximum of 15 drives under BBS control. Therefore, up to 15 hard drives, including those connected to the on-board SCSI controller, appear in the hard drive menu. For compatibility reasons, drive letters are assigned only to the first eight devices. [3]

By pressing the ESC key during POST execution, the user can request a boot selection menu before booting. This menu allows the user to change the primary boot device, such as to a CD-ROM drive, for the current boot cycle without making a permanent change and without entering Setup. Selections made in this menu are temporary; these choices are not saved in non-volatile memory.

The BIOS handles booting from an ATAPI CD-ROM or an ATAPI DVD-ROM. It can boot from a floppy image, hard drive type image, an emulation image on an ISO 9660 file format, and from media that is compliant with the “El Torito” Bootable CD-ROM Format Specification. The system can boot from a SCSI CD-ROM or from a SCSI DVD-ROM drive if the corresponding SCSI option ROM provides appropriate support.

BBS runtime functions 60-66 are supported. See the *BIOS Boot Specification (BBS)*, Revision 1.01 for details.

7.3 Memory

The following is a list of memory specifications that the system BIOS supports:

- Only registered DDR266 registered ECC memory is supported. When populated with more than 4 GB of memory, the memory between 4 GB and 4 GB minus 256 MB is remapped and may not be accessible for use by the operating system and may be lost to the user. This area is reserved for the BIOS, for APIC configuration space, for PCI adapter interface, and for virtual video memory space. This memory space is also remapped if the system is populated with memory configurations between 3.75 GB and 4 GB.
- The system BIOS supports registered DIMMs with CL=2 components when available.
- The system BIOS supports only ECC memory.
- Each memory bank can have different size DIMMs. Memory timing defaults to the slowest DIMM. Intel only tests identical DIMM sizes in the Intel® Server Board SE7501WV2.

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[3] The BIOS is limited to a maximum of 15 drives under BBS control. Up to 15 hard drives, including those connected to the onboard SCSI controller, will appear in the hard drive menu. Drive letters will be assigned to the first 8 devices only.

- Intel® Xeon™ running at 533MHz Front Side Bus only supports DDR266 DIMMs.

All DIMMs must use SPD EEPROM to be recognized by the BIOS. Mixing vendors of DIMMs is supported but it is not recommended because the system defaults to the slowest speed that will work with all of the vendors' DIMMs.

7.3.1 Memory Configuration

The Intel® Server Board SE7501WV2 uses the Intel® E7501 chipset to configure the system baseboard memory.

The Intel® Server Board SE7501WV2 BIOS is responsible for configuring and testing the system memory. The configuration of the system memory involves probing the memory modules for their characteristics and programming the chipset for optimum performance.

When the system comes out of reset, the main memory is not usable. The BIOS verifies that the memory subsystem is functional. It has knowledge of the memory subsystem and it knows the type of memory, the number of DIMM sites, and their locations.

7.3.2 Memory Sizing and Initialization

During POST, the BIOS tests and sizes memory, and configures the memory controller. The BIOS determines the operational mode of the MCH based on the number of DIMMS installed and the type, size, speed, and memory attributes found on the on-board EEPROM or serial presence detect (SPD) of each DIMM.

The memory system is based on rows. Since the Intel® Server Board SE7501WV2 supports a 2-way interleave, DIMMs must be populated in pairs. This means two DIMMs are required to constitute a row. Although DIMMs within a row must be identical, the BIOS supports various DIMM sizes and configurations allowing the rows of memory to be different. Memory sizing and configuration is guaranteed only for DIMMs listed on the Intel tested memory list. Intel only tests identical DIMMs in the Intel® Server Board SE7501WV2.

The memory-sizing algorithm determines the size of each row of DIMMs. The BIOS tests extended memory according to the option selected in the BIOS Setup Utility. The total amount of configured memory can be found using INT 15h, AH = 88h; INT 15h, function E801h, or INT 15h, function E820h.

Because the system supports up to 12 GB of memory, the BIOS creates a hole just below 4 GB to accommodate the system BIOS flash, APIC memory, and memory-mapped I/O located on 32-bit PCI devices. The size of this hole depends upon the number of PCI cards and the memory mapped resources requested by them. It is typically less than 128 MB.

7.3.3 ECC Initialization

Because only ECC memory is supported, the BIOS must initialize all memory locations before using them. The BIOS uses the auto-initialize feature of the MCH to initialize ECC.

7.3.4 Memory Remapping

During POST memory testing, the detection of single-bit and multi-bit errors in DIMM banks is enabled. If a single-bit error is detected, a single DIMM number will be identified. If a multiple-bit error is detected, a bank of DIMMs will be identified. The BIOS logs all memory errors into the System Event Log (SEL).

If an error is detected, the BIOS will reduce the usable memory so that the byte containing the error is no longer accessible. This prevents a single-bit error (SBE) from becoming a multi-bit error (MBE) after the system has booted, and it prevents SBEs from being detected and logged each time the failed location(s) are accessed. This is done automatically by the BIOS during POST. User intervention is not required.

Memory remapping can occur during base memory testing or during extended memory testing. If remapping occurs during the base memory testing, the SEL event is not logged until after the BIOS remaps the memory and successfully configures and tests 8 MB of memory. In systems where all memory is found to be unusable, only the BIOS beep codes indicate the memory failure. Once the BIOS locates a functioning bank of memory, remapping operations and other memory errors are logged into the SEL and reported to the user at the completion of POST.

7.3.5 DIMM Failure LED

The Intel® Server Board SE7501WV2 provides DIMM failure LEDs located next to each DIMM slot on the baseboard. The DIMM failure LEDs are used to indicate double-bit DIMM errors. If a double-bit error is detected during POST, the BIOS sends a *Set DIMM State* command to the BMC indicating that the DIMM LED is lit. These LED's will only be reset when a Front Panel Reset is performed with main power available to the system.

7.4 Processors

The BIOS determines the processor stepping, cache size, etc., through the CPUID instruction. The requirements are that all processors in the system must operate at the same frequency and have the same cache sizes. No mixing of product families is supported:

- If two 533MHz processors are installed, the system will run with a Front Side Bus (FSB) speed of 533MHz.

Processors run at a fixed speed and cannot be programmed to operate at a lower or higher speed.

7.5 Extended System Configuration Data (ESCD), Plug and Play (PnP)

The system BIOS supports industry standards for making the system Plug-and-Play ready. Refer to the following reference documents:

- *Advanced Configuration and Power Interface Specification*
- *PCI Local Bus Specification*
- *PCI BIOS Specification*
- *System Management BIOS Reference Specification*

In addition, refer to the relevant sections of the following specifications:

- *Extended System Configuration Data Specification*

- *Plug and Play ISA Specification*
- *Plug and Play BIOS Specification*

7.5.1 Resource Allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Intel® servers. The BIOS scans for the following, in order:

1. ISA devices: Although add-in ISA devices are not supported on these systems, some standard PC peripherals may require ISA-style resources. Resources for these devices are reserved as needed.
2. Add-in video graphics adapter (VGA) devices: If found, the BIOS initializes and allocates resources to these devices.
3. PCI devices: The BIOS allocates resources according to the parameters set up by the System Setup Utility and as required by the *PCI Local Bus Specification*, Revision 2.2 and *PCI –X Addendum to the PCI Local Bus Specification, Revision 1.0a*.

The system BIOS Power-on Self Test (POST) guarantees there are no resource conflicts prior to booting the system. Note that PCI device drivers must support sharing IRQs, which should not be considered a resource conflict. Only four legacy IRQs are available for use by PCI devices. Therefore, most of the PCI devices share legacy IRQs. In SMP mode, the I/O APICs are used instead of the legacy “8259-style” interrupt controller. There is very little interrupt sharing in SMP mode.

7.5.2 PnP ISA Auto-Configuration

The system BIOS does the following:

- Supports relevant portions of the *Plug and Play ISA Specification*, Revision 1.0a and the *Plug and Play BIOS Specification*, Revision 1.0A.
- Assigns I/O, memory, direct memory access (DMA) channels, and IRQs from the system resource pool to the embedded PnP Super I/O device.

Add-in PnP ISA devices are not supported.

7.5.3 PCI Auto-Configuration

The system BIOS supports the INT 1Ah, AH = B1h functions, in conformance with the *PCI Local Bus Specification*, Revision 2.1. The system BIOS also supports the 16- and 32-bit protected mode interfaces as required by the *PCI BIOS Specification*, Revision 2.1.

Beginning at the lowest device, the BIOS uses a “depth-first” scan algorithm to enumerate the PCI buses. Each time a bridge device is located, the bus number is incremented and scanning continues on the secondary side of the bridge until all devices on the current bus are scanned.

The BIOS then scans for PCI devices using a “breadth-first” search. All devices on a given bus are scanned from lowest to highest before the next bus number is scanned.

The system BIOS POST maps each device into memory and/or I/O space, and assigns IRQ channels as required. The BIOS programs the PCI-ISA interrupt routing logic in the chipset hardware to steer PCI interrupts to compatible ISA IRQs.

The BIOS dispatches any option ROM code for PCI devices to the DOS compatibility hole (C0000h to E7FFFh) and transfers control to the entry point. Because the DOS compatibility hole is a limited resource, system configurations with a large number of PCI devices may encounter a shortage of this resource. If the BIOS runs out of option ROM space, some PCI option ROMs are not executed and a POST error is generated. The scanning of PCI option ROMs can be controlled on a slot-by-slot basis in BIOS setup.

Drivers and/or the operating system can detect installed devices and determine resource consumption using the defined PCI, legacy PnP BIOS, and/or ACPI BIOS interface functions.

7.6 NVRAM API

The non-volatile RAM (NVRAM) API and the PCI data records are not supported by the system BIOS. The configuration information of the PCI devices is stored in ESCD. The System Setup Utility can update the ESCD to change the IRQ assigned to a PCI device.

7.7 Legacy ISA Configuration

Legacy ISA add-in devices are not supported.

7.8 Automatic Detection of Video Adapters

The BIOS detects video adapters in the following order:

1. Off-board PCI
2. On-board PCI

The on-board (or off-board) video BIOS is shadowed, starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to off-board devices.

7.9 Keyboard / Mouse Configuration

The BIOS will support either a mouse or a keyboard in the single PS/2 connector. The BIOS will support both a keyboard and mouse if a Y-cable is used with the single PS/2 connector. The devices are detected during POST and the keyboard controller is programmed accordingly. Hot plugging of a keyboard from the PS/2 connector using DOS is supported by the system.

7.9.1 Boot without Keyboard and/or Mouse

The system can boot with or without a keyboard and/or mouse. Setup does not include an option to disable them. The presence of the keyboard and mouse is detected automatically during POST, and, if present, the keyboard is tested. The BIOS displays the message "Keyboard Detected" if it detects a keyboard during POST and it displays the message "Mouse Initialized" if it detects a mouse during POST. The system does not halt for user intervention on errors if either the keyboard or the mouse is not detected.

7.10 Floppy Drives

The Intel® Server Board SE7501WV2 BIOS supports floppy controllers and floppy drives that are compatible with IBM* XT/AT standards. Most floppy controllers have support for two floppy drives although such configurations are rare. At a minimum, the SE7501WV2 BIOS supports 1.44 MB and 2.88 MB floppy drives. LS-120 floppy drives are attached to the IDE controller and are covered elsewhere.

The BIOS does not attempt to auto-detect the floppy drive because there is no reliable algorithm for detecting the floppy drive type if no media is installed. The BIOS auto-detects the floppy media if the user specifies the floppy drive type through setup.

See the following table for details on various floppy types supported by each floppy drive. The 1.25/1.2 MB format is primarily used in Japan. 1.25/1.2 MB floppies use the same raw media as the 1.44 MB floppies, but must be read using 3-mode drives. In order to access the 1.25/1.2 MB floppies, the BIOS must change the spindle speed to 360 rpm. Please note that the 1.44 MB media uses spindle speed 300 RPM. The DENSSEL (density select) pin on a 3-mode floppy drives selects the spindle speed. The spindle rotates at 300 RPM when DENSSEL signal is high. The BIOS sets the spindle speed to match the media.

Table 41. Allowed Combinations of Floppy Drive and Floppy Media

Floppy Drive	Floppy Format	Note
1.44 MB (3 mode)	1.25 MB (Toshiba) 1.25 MB (NEC PC98) 1.44 MB	Floppies formatted under 1.25 MB NEC* PC98 format require a special driver. The BIOS has native support for 1.25 MB Toshiba format.
1.44 MB (ordinary)	1.44 MB	DENSEL pin is ignored by these floppy drives
2.88 MB (3 mode)	1.25 MB (Toshiba) 1.25 MB (NEC PC98) 1.44 MB 2.88 MB	Floppies formatted under 1.25 MB NEC PC98 format require special driver. The BIOS has native support for 1.25 MB Toshiba format
2.88 MB (ordinary)	1.44 MB 2.88 MB	The DENSEL pin is ignored by these floppy drives

The BIOS provides a setup option to disable the floppy controller. In addition, some platforms support the 3-mode floppy BIOS extension specification, revision 1.0. This specification defines a 32-bit protected mode interface that can be invoked from a 32-bit operating system.

Note: The recovery BIOS requires a 1.44 MB media in a 1.44 MB floppy drive or LS-120 drive.

7.11 Universal Serial Bus (USB)

The Intel® Server Board SE7501WV2 BIOS supports USB keyboard, mouse and boot devices. The Intel® Server Board SE7501WV2 contains two USB host controllers. Each host controller includes the root hub and two USB ports. During POST, the BIOS initializes and configures the root hub ports and looks for a keyboard, mouse, boot device, and the USB hub and enables them.

The BIOS implements legacy USB keyboard support. USB legacy support in BIOS translates commands that are sent to the PS/2 devices into the commands that USB devices can understand. It also makes the USB keystrokes and the USB mouse movements appear as if they originated from the standard PS/2 devices.

7.12 BIOS Supported Server Management Features

The Intel® Server Board SE7501WV2 BIOS supports many standards-based server management features and several proprietary features. The Intelligent Platform Management Interface (IPMI) is an industry standard that defines standardized abstracted interfaces to platform management hardware. The Intel® Server Board SE7501WV2 BIOS supports version 1.5 of the IPMI specification. The BIOS also implements many proprietary features that are allowed by the IPMI specification, but which are outside of the scope of the IPMI specification.

This section describes the implementation of the standard and proprietary features, including console redirection, the Emergency Management Port (EMP), Service Partition boot, Direct Platform Control over the serial port, and Platform Event Paging and Filtering. The BIOS owns console redirection over a serial port, but plays only a minimal role in Platform Event Paging and Filtering.

7.12.1 IPMI

The term intelligent platform management refers to the autonomous monitoring and recovery features that are implemented in platform hardware and firmware. Platform management functions such as inventory, the event log, monitoring and reporting system health, etc., are available in a powered down state and without help from the host processors. The Baseboard Management Controller (BMC) and other controllers perform these tasks independent of the server processor. The BIOS interacts with the platform management controllers through standard interfaces.

The BIOS is responsible for opening the system interface to the BMC early in the POST. This may involve enabling chip selects, decode, etc.

The BIOS also logs system events and POST error codes during system operation. The BIOS logs a boot event to the BMC early in POST. These events follow the IPMI specification. The IPMI specification version 1.5 requires the use of all but two bytes in each event log entry, called Event Data 2 and Event Data 3. An event generator can specify that these bytes contain OEM-specified values.

7.12.2 Advanced Configuration and Power Interface (ACPI)

The primary role of the ACPI BIOS is to supply the ACPI Tables. POST creates the ACPI Tables and locates them above 1 MB in extended memory. The location of these tables is conveyed to the ACPI-aware operating system through a series of tables located throughout memory. The format and location of these tables is documented in the publicly available ACPI specification. To prevent conflicts with a non-ACPI-aware operating system, the memory used for the ACPI Tables is marked as “reserved” in the INT 15h, function E820h.

As described in the ACPI specification, an ACPI-aware operating system generates an SMI to request that the system be switched into ACPI mode. The BIOS responds by setting up all system (chipset) specific configuration required to support ACPI, issues the appropriate command to the BMC to enable ACPI mode and sets the SCI_EN bit as defined by the ACPI specification. The system automatically returns to legacy mode on hard reset or power-on reset.

There are three runtime components to ACPI:

- **ACPI Tables:** These tables describe the interfaces to the hardware. ACPI Tables can make use of a p-code type of language, the interpretation of which is performed by the operating system. The operating system contains and uses an AML (ACPI Machine Language) interpreter that executes procedures encoded in AML and stored in the ACPI Tables; ACPI Machine Language is a compact, tokenized, abstract machine language. The tables contain information about power management capabilities of the system, APICs, and the bus structure. The tables also describe control methods that the operating system uses to change PCI interrupt routing, control legacy devices in Super I/O, and find the cause of wake events.

- **ACPI Registers:** ACPI registers are the constrained part of the hardware interface, described (at least in location) by the ACPI Tables.
- **ACPI BIOS:** This code boots the machine and implements interfaces for sleep, wake, and some restart operations. The ACPI BIOS also provides the ACPI Description Tables.

All IA-32 server platforms support S0, S4, and S5 states. The Intel® Server Board SE7501WV2 also supports the S1 state. S1 and S4 are considered sleep states. The ACPI specification defines the sleep states and requires the system to support at least one of them.

While entering the S4 state, the operating system saves the context to the disk and most of the system is powered off. The system can wake from such a state on various inputs depending on the hardware. The Intel® Server Board SE7501WV2 will wake on a power button press, or a signal received from a wake-on-LAN compliant LAN card (or on-board LAN), modem ring, PCI power management interrupt, or RTC alarm. The BIOS performs a complete POST upon a wake from S4 and initializes the platform. S4BIOS is not supported.

The Intel® Server Board SE7501WV2 can wake from the S1 state using a PS/2 keyboard, mouse, and USB device in addition to the sources described above.

The wake sources are enabled by the ACPI operating systems with co-operation from the drivers; the BIOS has no direct control over the wake sources when an ACPI operating system is loaded. The role of the BIOS is limited to describing the wake sources to the operating system and controlling secondary control/status bits via a Differentiated System Description Table (DSDT).

The S5 state is equivalent to an operating system shutdown. No system context is saved.

7.12.3 Wake Events

The system BIOS is capable of configuring the system to wake up from several sources under a non-ACPI configuration, such as when the operating system does not support ACPI. The wake up sources are described in the following table. Under ACPI, the operating system programs the hardware to wake up on the desired event. The BIOS describes various wake sources to the operating system.

In legacy mode, the BIOS enables or disables wake sources based on a switch in Setup. The operating system or driver must clear any pending wake up status bits in the associated hardware, such as the Wake on LAN status bit in the LAN application specific integrated circuit (ASIC), or PCI power management event (PME) status bit in a PCI device. The legacy wake up feature is disabled by default.

Table 42. Supported Wake Events

Wake Event	Supported via ACPI (by sleep state)	Supported Via Legacy Wake
Power Button	Always wakes system	Always wakes system
Ring indicate from COM-A	Wakes from S1 and S4.	Yes
Ring indicate from COM-B	Wakes from S1 and S4. If Serial-B is used for Emergency Management Port, Serial-B wakeup is disabled.	Yes
PME from PCI cards	Wakes from S1 and S4.	Yes
RTC Alarm	Wakes from S1. Always wakes the system up from S4.	Yes
Mouse	Wakes from S1	No
Keyboard	Wakes from S1	No
USB	Wakes from S1	No

7.12.4 Front Panel Switches

The BMC forwards the power button request to the ACPI power state machines in the chipset. The button signal is monitored by the BMC and does not directly control power on the power supply.

The power switch behaves differently depending on whether the operating system supports ACPI. If the operating system supports ACPI the power button can be configured as a sleep button. The operating system causes the system to transition to the appropriate system state depending on the user settings.

7.12.4.1 Power Switch Off to On

The chipset may be configured to generate wake up events for several system events: Wake-on-LAN, PCI Power Management Interrupt, and the Real-Time Clock Alarm are examples of these events. If the operating system is ACPI-aware, it programs the wake sources before shutdown. In non-ACPI mode, the BIOS performs the configuration. The BMC monitors the power button and wake up event signals from the chipset. A transition from either source results in the BMC starting the power-up sequence. Since the processors are not executing, the BIOS does not participate in this sequence. The hardware receives power good and reset from the BMC and then transitions to an ON state.

7.12.4.2 On to Off (Legacy)

The ICH3 is configured to generate an SMI due to a power button event. The BIOS services this SMI and sets the state of the machine in the chipset to the OFF state. The BMC monitors power state signals from the chipset and de-asserts PS_PWR_ON to the power supply. As a safety mechanism, the BMC automatically powers off the system in 4-5 seconds if the BIOS fails to service the SMI.

7.12.4.3 On to Off (ACPI)

If an ACPI operating system is loaded, the power button switch generates a request via SCI to the operating system to shutdown the system. The operating system retains control of the system and operating system policy determines the sleep state, if any, into which the system transitions.

7.12.4.4 On to Sleep (ACPI)

If an ACPI operating system is loaded and the power button is configured as a sleep button, the sleep button switch generates a request via SCI to the operating system to place the system into sleep mode. The operating system retains control of the system and operating system policy determines the sleep state, if any, into which the system transitions.

7.12.4.5 Sleep to On (ACPI)

If an ACPI operating system is loaded and the power button is configured as a sleep button, the sleep button switch generates a wake event to the ACPI chipset and a request via SCI to the operating system to place the system in the On state. The operating system retains control of the system and operating system policy determines the sleep state, if any, and the sleep sources from which the system can wake.

7.12.5 Wired For Management (WFM)

Wired for Management (WFM) is an industry-wide initiative to increase overall manageability and reduce the total cost of ownership. WFM allows a server to be managed over a network. The system BIOS supports revision 2.0 of the *Wired For Management Baseline Specification*. It also supports the preboot execution environment, as outlined in the WFM baseline specification, because the system includes an embedded WFM compliant network device.

The system BIOS supports version 2.3 of the *System Management BIOS Reference Specification* to help higher-level instrumentation software meet the WFM requirements. The higher-level software can use the information provided by the system management (SM) BIOS to instrument desktop management interface (DMI) standard groups that are specified in the WFM specification.

The BIOS also configures the SYSID table as described in the *Network PC System Design Guidelines, Revision 1.0*. This table contains the globally unique ID (GUID) of the baseboard. The mechanism that sets the GUID in the factory is defined in the *SYSID BIOS Support Interface Requirement Specification, Version 1.2*. The caller must provide the correct security key for this call to succeed.

The system BIOS implements the following:

- WFM 2.0 items per the server checklist supplied in the WfM specification.
- INT15h functions 2500h, 2501h and 2502h as required.
- Support for and display of F12 Network boot POST hot key.

7.12.6 PXE BIOS Support

This section discusses host system BIOS support required for PXE compliance and how PXE boot devices (ROMs) and PXE Network Boot Programs (NBPs) use it.

7.12.6.1 BIOS Requirements

PXE-compliant BIOS implementations must:

- Locate and configure all PXE-capable boot devices (UNDI Option ROMs) in the system, both built-in and add-ins.
- Supply a PXE according to this specification if the system includes a built-in network device.

Implement the following specifications:

- Plug-and-Play BIOS Specification v1.0a or later
- System Management BIOS (SMBIOS) Reference Specification v2.2 or later
- The requirements defined in Sections 3 and 4 of the BIOS Boot Specification (BBS) v1.01or later, to support network adapters as boot devices
- Supply a valid UUID and Wake-up Source value for the system via the SMBIOS structure table.

7.12.7 BIOS Recommendations

To be PXE 2.1-compliant, the BIOS implements the following:

- *POST Memory Manager Specification* v1.01. PMM provides a straightforward way for LAN on Motherboard PXE implementations to move their ROM image from UMB to extended memory. While methods to do this exist outside of PMM, their use is undefined and unreliable. Placing PXE ROM images into UMB space reduces the available UMB space by approximately 32 KB. This is sufficient to compromise or even prevent successful operation of some downloaded programs.

The Intel® Server Board SE7501WV2 is compliant with PXE 2.1. It implements the *Post Memory Manager Specification v1.01.*

7.13 Console Redirection

The BIOS supports redirection of both video and keyboard via a serial link (serial port 1 or 2). When console redirection is enabled, the local (host server) keyboard input and video output are passed both to the local keyboard and video connections, and to the remote console via the serial link. Keyboard inputs from both sources are valid and video is displayed to both outputs. As an option, the system can be operated without a keyboard or monitor attached to the host system and run entirely from the remote console. Setup and any other text-based utilities can be accessed through console redirection.

7.13.1 Operation

When redirecting the console through a modem as opposed to a null modem cable, the modem needs to be configured with the following:

- Auto-answer (for example, ATS0=2, to answer after two rings)
- Modem reaction to DTR set to return to command state (e.g., AT&D1). Failure to provide this option will result in the modem either dropping the link when the server reboots (as in AT&D0) or becoming unresponsive to server baud rate changes (as in AT&D2).
- The Setup/System Setup Utility option for handshaking must be set to CTS/RTS + CD for optimum performance. The CD refers to carrier detect.
- If the Emergency Management Port shares the serial port with serial redirection, the handshaking must be set to CTS/RTS + CD. In selecting this form of handshaking, the server is prevented from sending video updates to a modem that is not connected to a remote modem. If this is not selected, video update data being sent to the modem inhibits many modems from answering an incoming call. An Emergency Management

Port option utilizing the CD should not be used if a modem is not used and the CD is not connected.

If the BIOS determines that console redirection is enabled, it reads the current baud rate from CMOS and passes this value to the appropriate management controller via the IPMB.

Once console redirection is selected via Setup or the System Setup Utility, redirection is loaded into memory and is activated during POST. While redirection cannot be removed without rebooting, it can be inhibited and restarted. When inhibited, the serial port is released from redirection and might be used by another application. Restarting reclaims the serial port and continues redirection.

Inhibiting/restarting is accomplished through an INT 16h mechanism. The standard INT 16h (keyboard handler) function ah=05h places a keystroke in the key buffer, as if an actual key has been pressed. Keystrokes buffered in this way are examined by redirection. If a valid command string has been sent, it is executed. The following commands are supported in this fashion:

- Esc-CDZ0: Inhibit console redirection
- Esc-CDZ1: Restart console redirection
- Esc-CDZ2 - “Soft” Inhibit Console Redirection, without serial port or modem reset

To inhibit redirection, the software must call INT 16h, function ah=05h five times to place the five keys in the key buffer. Keystrokes sent to the INT 16h buffers for purposes of invoking a command are buffered and should be removed via the normal INT 16h calls. This prevents these keystrokes from being passed to another application.

7.13.2 Keystroke Mappings

For keys that have a 7-bit character ASCII mapping, such as A and Ctrl-A, the remote simply sends the ASCII character. For keys that do not have an ASCII mapping, such as F1 and Alt-A, the remote must send a string of characters. This character string is a function of the terminal emulation supported by the BIOS. There are two non-overlapping terminal emulation systems supported simultaneously by Intel BIOS. These are known as VT100+ and a PC-ANSI.

Microsoft prescribes a terminal emulation that they call VT100+ for use with Microsoft* systems. Microsoft* Windows* systems will interpret input <ESC> sequences and other character sequences using this terminal emulation interpretation. The VT100+ terminal emulation is based upon the behavior of the DEC* VT100 terminal and its keyboard character sequences.

Another common terminal emulation, different from VT100+, is called PC-ANSI. The PC-ANSI terminal emulation is also based on the DEC* VT100 terminal behavior. However, it maps its function keys, and other auxiliary (non-alpha-numeric-symbol) keys such as Page Up, Page Down, etc., using different character sequences than the Microsoft defined VT100+.

Intel® BIOS will accept non-character key input from either a VT100+ or a PC-ANSI terminal emulation. Because the differences in these two terminal emulations occur only in specific input key sequences, and not in output sequences and positioning data, this is possible. In addition, the different input key sequences do not reuse any of the same sequences for different functions. Therefore, it is possible to accept and recognize the F1 key press by either the

VT100+ sequence for this event, or the PC-ANSI sequence for this event. The BIOS will accept either encoding, in something of a “superset” VT100+/PC-ANSI terminal emulation. This input character mapping is presented in the following table.

Alt key combinations are created by sending the combination **<ESC>}** (**^[}**) or **<ESC>^A** (**^[^A**) followed by the character to be Alt modified. Once this Alt key combination is sent (**<ESC>}** or **<ESC>^A**), the next keystroke sent will be translated into its Alt-key mapping (that is, if **^[}** is mapped to Shift-F1, then pressing Shift-F1 followed by ‘a’ would send an Alt-a to the server). These mappings are provided for emulators that don’t properly send ALT shift key sequences.

The remote terminal can force a refresh of its video by sending **<ESC>{**. The sequence to switch the emulation dynamically is as follows: <esc>CDZt0/1/2/3 switches to PC-ANSI, VT100, VT100+, VTUTF8 respectively (VT100 is actually honored as VT100+).

Unusual combinations outside of the ANSI mapping and not in the following table, such as Ctrl-F1, are not supported.

Table 43. Non-ASCII Key Mappings

Key	PC-ANSI	VT100+	Shift	Ctrl	Alt
ESC	^[	^[	NS	NS	NS
F1	<ESC>OP	<ESC>1	NS	NS	NS
F2	<ESC>OQ	<ESC>2	NS	NS	NS
F3	<ESC>OR	<ESC>3	NS	NS	NS
F4	<ESC>OS	<ESC>4	NS	NS	NS
F5	<ESC>OT	<ESC>5	NS	NS	NS
F6	<ESC>OU	<ESC>6	NS	NS	NS
F7	<ESC>OV	<ESC>7	NS	NS	NS
F8	<ESC>OW	<ESC>8	NS	NS	NS
F9	<ESC>OX	<ESC>9	NS	NS	NS
F10	<ESC>OY	<ESC>0	NS	NS	NS
F11	<ESC>OZ	<ESC>!	NS	NS	NS
F12	<ESC>O1	<ESC>@	NS	NS	NS
Print Screen	NS	NS		NS	NS
Scroll Lock	NS	NS	NS	NS	NS
Pause	NS	NS	NS	NS	NS
Insert	<ESC> [L	<ESC>+	NS	NS	NS
Delete	(7Fh)	<ESC>-	NS	NS	NS
Home	<ESC> [H	<ESC>h	NS	NS	NS
End	<ESC> [K	<ESC>k	NS	NS	NS
Pg Up	<ESC> [M	<ESC>?	NS	NS	NS
Pg Down	<ESC> [2J	<ESC>/	NS	NS	NS
Up Arrow	<ESC> [A	<ESC>[A	NS	NS	NS
Down Arrow	<ESC> [B	<ESC>[B	NS	NS	NS
Right Arrow	<ESC> [C	<ESC>[C	NS	NS	NS
Left Arrow	<ESC> [D	<ESC>[D	NS	NS	NS
Tab	(09h)	^I	NS	NS	NS
Shift Modifier		<ESC>^S			

Key	PC-ANSI	VT100+	Shift	Ctrl	Alt
Alt Modifier	<ESC>}	<ESC>^A			
Ctrl Modifier		<ESC>^C			

NS = Not supported

(xxh) = ASCII character xx

Table 44. ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
Backspace (^H)	(08h)	(08h)	(7Fh)	<ESC>}(08h)
(accent) `	`	(tilde) ~	NS	<ESC>}`
1	1	!	NS	<ESC>}1
2	2	@	NS	<ESC>}2
3	3	#	NS	<ESC>}3
4	4	$	NS	<ESC>}4
5	5	%	NS	<ESC>}5
6	6	^	NS	<ESC>}6
7	7	&	NS	<ESC>}7
8	8	*	NS	<ESC>}8
9	9	(	NS	<ESC>}9
0	0	)	NS	<ESC>}0
(dash) -	-	(under) _	(1Fh)	<ESC>}-
=	=	+	NS	<ESC>}=
a to z	a to z	A to Z	(01h) to (1Ah)	<ESC>}a to <ESC>}z
[	[	{	(1Bh)	<ESC>}[
]	]	}	(1Dh)	<ESC>}]
\	\	|	(1Ch)	<ESC>}\
(semi-colon) ;	;	(colon) :	NS	<ESC>};
(apostrophe) '	‘	(quote) "	NS	<ESC>}'
(comma) ,	,	<	NS	<ESC>},
(period) .	.	>	NS	<ESC>}.
/	/	?	NS	<ESC>}/
(space)	(20h)	(20h)	(20h)	<ESC>}(20h)
(carriage return or ^M)	(0Dh)			

NS = not supported

(xxh) = ASCII character xx

7.13.3 Limitations

Console redirection is a real-mode BIOS extension. It does not operate outside of real mode. In addition, console redirection will not function if the operating system or a driver, such as EMM386*, takes the processor into protected mode. If an application moves the processor in and out of protected mode, it should inhibit redirection before entering protected mode and restart redirection when it returns to real mode.

Video is redirected by scanning and sending changes in text video memory. Therefore, console redirection is unable to redirect video in graphics mode. Since the BIOS scans the text video memory, an additional limitation exists if the system does not contain a video graphics adapter or a proprietary means of buffering the video memory. The BIOS may not have a method to send changes in text video memory if an application such as an option ROM writes directly to video memory.

Keyboard redirection operates through the use of the BIOS INT 16h handler. Software bypassing this handler does not receive redirected keystrokes.

7.14 Emergency Management Port (EMP)

The Intel® Server Board SE7501WV2 provides a communication serial port with the BMC. The BMC controls a multiplexor that determines if the external RJ45 Serial 2 connector is electrically connected to the BMC or to the standard serial port of the Super I/O. Refer to the *Emergency Management Port EPS* for information about Emergency Management Port features.

7.14.1 Serial Ports

The SE7501WV2 server board has two serial ports, both external RJ45 connectors. Serial port 2 can be used for both the Emergency Management Port and for modem use. Refer to the SE7501WV2 Hardware External Product Specification for additional serial port information.

7.14.2 Interaction with BIOS Console Redirection

Additional features are available if BIOS console redirection is enabled on the same serial port as the Emergency Management Port, and the EMP mode is set to "Always active" or "Preboot."

BIOS console redirection supports an extra control escape sequence to force the serial port to the BMC. After this command is sent, Serial port 2 attaches to the BMC Emergency Management Port serial port and the Super I/O Serial 2 data is ignored. This feature allows a remote user to monitor the status of POST using the standard BIOS console redirection features and then takes control of the system reset or power using the Emergency Management Port features. If a failure occurs during POST, a watchdog time-out feature in the BMC automatically takes control of Serial Port 2.

The character sequence that switches the multiplexor to the BMC serial port is "ESC O 9". This is also denoted as ^[O9. This key sequence is above the normal ANSI function keys and will not be used by an ANSI terminal. This key sequence is also not defined by the Microsoft* document Standardizing Out-of-Band Management Console Output and Terminal Emulation (VT-UTF8 and VT100+). That document does define an alternate representation, "**ESC (**" (or **^[(**), which is also recognized by Intel BIOS and BMC.

One restriction of using the same serial port for both the Emergency Management Port and BIOS console redirection is that console redirection must be set up to CTS/RTS for direct connection and to CTS/RTS+CD for a modem connection. Both the Emergency Management Port and console redirection assume N, 8, 1 mode. The BIOS redirection and the Emergency Management Port can work at different baud rates by using the auto baud feature of the modem.

7.15 Service Partition Boot

The Intel® Server Board SE7501WV2 BIOS supports a Service Partition boot. The Service Partition is installed as a separate file system partition on one of the local hard drives. It hosts the DOS operating system, the System Setup Utility, and diagnostic agents and tests. The Service Partition communicates with remote console applications, and can transfer files between the Service Partition over the LAN, serial port, or a modem.

The BIOS provides setup options to configure the Service Partition type (the default is 98h), and the option for enabling and disabling the Service Partition boot. A remote agent can direct the BMC firmware to set the Service Partition boot request and reboot the system.

Upon rebooting, the system BIOS checks for a service partition boot request. On finding a boot request, the system searches for the service partition type starting from the highest disk number in the scan order. If a service partition is found, the system boots from it. The drive containing the service partition becomes the C: drive.

The drive numbers of all other drives are incremented by one, except for the drive that has a scan order that is higher than the Service partition drive. The BIOS can be directed by the user to perform a one-time boot from the service partition. The service partition is serviced once per request. The service partition boot option is disabled upon each boot attempt.

The BIOS considers a Service Partition boot as a continuation of the BIOS POST. The BIOS does not hide the serial port that is used by console redirection or the Emergency Management Port if it is booting to the Service Partition. The state of all Emergency Management Port functionality remains in the same state as in POST. The state of Pre-Boot and Always-Active EMP mode also do not change. The Service Partition is always scanned for presence, even if Service Partition booting is inactive.

The BIOS sets the watchdog timer inside BMC while it is attempting to boot from a Service Partition. This timer is reset upon booting of the Service Partition by an application. If the system hangs on booting, a reset brings the system out of the Service Partition boot and an error is logged.

The BIOS starts serial console redirection on a service partition boot. Console redirection is controlled by IPMI commands and synched to BMC serial port parameters. Any reboot after a service partition boot reverts to the previous settings of Serial Console Redirection. For example, if console redirection was turned off before the service boot, it reverts to disabled.

7.16 System Management BIOS (SMBIOS)

This section references the *System Management BIOS Reference Specification, Version 2.3*.

The *Desktop Management Interface Specification* and its companion, the *DMTF Systems Standard Groups Definition,* define "…manageable attributes that are expected to be supported by DMI-enabled computer systems." Many of these attributes do not have a standard interface to the management software, but are known by the system BIOS. The system BIOS provides this interface via data structures through which system attributes are reported.

The system administrator can use SMBIOS to obtain the types, capabilities, operational status, installation date, and other information about the system components. The Intel® Server Board SE7501WV2 BIOS provides the SMBIOS structures via a table-based method. The table convention, provided as an alternative to the calling interface, allows the SMBIOS structures to be accessed under 32-bit protected-mode operating systems such as Windows NT*. This convention provides a searchable entry-point structure that contains a pointer to the packed SMBIOS structures residing somewhere in 32-bit physical address space.

The SMBIOS entry-point structure described below can be located by application software by searching for the anchor-string on paragraph (16-byte) boundaries within the physical memory address range 000F0000h to 000FFFFFh. This entry point encapsulates an intermediate anchor string, which is used by some existing DMI browsers.

The total number of structures can be obtained from the SMBIOS entry-point structure. The system information is presented to an application as a set of structures that are obtained by traversing the SMBIOS structure table referenced by the SMBIOS entry-point structure. The following table describes the types of SMBIOS structures supported by the system BIOS.

Table 45. SMBIOS Header Structure

Structure Type	Supported	Comments
BIOS Information (Type 0)	Yes	One record for the system BIOS. SMBIOS 2.3 does not allow the use of type 0 records to describe the option ROMs. The system BIOS version string is described in Section 7.45
System Information (Type 1)	Yes	
Baseboard Information (Type 2)	Yes	
Chassis Information (Type 3)	Yes	
Processor Information (Type 4)	Yes	One for every processor slot.
Memory Controller Information (Type 5)	No	Browsers should use Type 16 records.
Memory Module Information (Type 6)	No	Browsers should use Type 17 records.
Cache Information (Type 7)	Yes	Two records for every processor. One record describes L1 cache and the second one describes L2 cache. The disabled bit in the cache configuration field is set if the corresponding processor is absent or disabled.
Port Connector Information (Type 8)	Yes	Describes the baseboard connectors including IDE, floppy, SCSI, keyboard, mouse, COM ports, and parallel port.
System Slots (Type 9)	Yes	One record for each PCI slot. The number of PCI slots is determined by a supported 1U or 2U riser.
On-board Device Configuration (Type 10)	Yes	One for each on-board device, like SCSI controller, video controller etc.
OEM Strings (Type 11)	Yes	From OEM GPNV area.
System Configuration Options (Type 12)	Yes	Describes the baseboard jumper settings.
BIOS Language Information (Type 13)	Yes	
Group Association (Type 14)	No	None required.
Event Log (Type 15)	No	Absent if the system is IPMI compliant. In that case, the System Event Log can be accessed using the IPMI standard, not SMBIOS specification. Present if event log can be accessed using SMBIOS methods.
Physical Memory Array (Type 16)	Yes	

Structure Type	Supported	Comments
Memory Device (Type 17)	Yes	One record for each memory device slot, six total. DIMM3A/BANK3 will be the 1st entry DIMM3B/BANK3 will be the 2nd entry DIMM2A/BANK2 will be the 3rd entry DIMM2B/BANK2 will be the 4th entry DIMM1A/BANK1 will be the 5th entry DIMM1B/BANK1 will be the 6th entry BIOS will log memory SEL events during runtime that will contain a DIMM number that can be used to reference these tables. Thus DIMM 0 will reference DIMM3A, DIMM 1 will reference 3B etc.
Memory Error Information (Type 18)	No	Much more extensive information available in the System Event Log.
Memory Array Mapped Addresses (Type 19)	Yes	
Memory Device Mapped Addresses (Type 20)	Yes	
Built-in Pointing Devices (Type 21)	No	Applies only to mobile platforms.
Portable Battery (Type 22)	No	Applies only to mobile platforms.
System Reset (Type 23)	No	
Hardware Security (Type 24)	Yes	
Probe Information (Type 26-29, 34-36)	No	Information about sensors and probes can be obtained using IPMI mechanisms. Not populated for non-IPMI compliant systems as well.
Out-of-band Remote Access (Type 30)	No	
BIS Entry Point (Type 31)	No	Support for Boot Integrity Services (BIS).
System Boot Information (Type 32)	Yes	
64-bit Memory Error Information (Type 33)	No	Much more extensive information available in the System Event Log and can be accessed using IPMI mechanisms.
IPMI Device Information	Yes	The information in this structure defines the attributes of an Intelligent Platform Management Interface (IPMI) Baseboard Management Controller (BMC).
Structure Not In Effect (Type 126)	Yes	Indicates software should ignore this structure. These structures may be present.
End of Table (Type 127)	Yes	Structure indicating end of table.

7.17 Microsoft* Windows* Compatibility

The Intel® Server Board SE7501WV2 is compliant with the *Hardware Design Guide v3.0*.

The Hardware Design Guide (HDG) for a Windows* 2000 Server platform is intended for systems that are designed to work with Windows 2000 Server family class operating systems. Each specification classifies the systems further and has different requirements based on the intended usage for that system. For example, a server system used in small home/office environments has different requirements than one that is used for enterprise applications.

The Intel® Server Board SE7501WV2 BIOS meets the applicable requirements as specified in version 3.0 of the HDG specification.

7.17.1 Quiet Boot

Version 3.0 of the Hardware Design Guide for Microsoft Windows 2000 requires that the BIOS provide minimal startup display during BIOS POST. The system start-up must only draw the user's attention in case of errors or when there is a need for user interaction. By default, the system must be configured so the screen display does not display memory counts, device status, etc., but presents a "clean" BIOS start-up. The only screen display allowed is the OEM splash screen, which can include information such as copyright notices.

The Intel® Server Board SE7501WV2 BIOS supports the <ESC> and <F2> hot-keys during POST, giving the user the ability to temporarily disable the splash screen to view all diagnostic and initialization messages for the current boot. The BIOS displays a message about the hot-keys below the splash screen, at the bottom of the display. The splash screen can be disabled for all subsequent boot up sequences by going into the BIOS setup utility and disabling the "Quiet Boot" option found under the "Boot" menu. The Quiet Boot option should be disabled when using BIOS console redirection, since it cannot redirect the video if configured for graphics mode.

If the Service Partition boot is enabled, the BIOS turns off the splash screen for that boot and restores it during subsequent, normal boots. The BIOS may temporarily remove the splash screen when the user is prompted for a password during POST. The BIOS also allows an OEM to override the standard Intel® splash screen with a custom one.

The Intel® Server Board SE7501WV2 BIOS maintains the splash screen during option ROM initialization. Since option ROMs expect the video to be in text mode, the BIOS emulates text mode. The BIOS remembers the Int 10 calls made by the option ROMs and displays the option ROM screen if the user presses the <Esc> key. The ROM screen is restored if the BIOS detects any key combination that includes the <Ctrl> or <Alt> key during option the ROM scan. This is because many option ROMs use one of these key combinations to enter setup.

The Intel® Server Board SE7501WV2 BIOS displays a progress meter at the top of the screen. This meter provides a visual indication of percentage of POST completed. The BIOS measures the amount of time required for completing POST during every boot and uses that information to update the progress meter during the next boot.

Note: If the "Extended Memory Test" option in BIOS setup is set for "Extensive", the progress meter may stop until the memory test has completed, causing the system to appear to be hung. Once the memory test has completed, the progress meter will continue as POST progresses. Depending on the amount of memory installed, the progress meter may stop for anywhere from 15 seconds to several minutes.

7.18 BIOS Serviceabilty Features

7.18.1 CMOS Reset

The CMOS configuration RAM may be reset by one of two methods: the CMOS clear jumper located on the baseboard, or the CMOS clear button sequence from the front panel. The CMOS can also be set to a default setting through the BIOS Setup. It will automatically be reset if it becomes corrupted.

Five steps are required to reset the CMOS through the buttons on the front panel:

1. Power off the system, but leave the AC power connected so the 5 V standby is available.

2. Assure that the CMOS clear jumper is in the 'not clear' position.
3. Hold down the reset button for at least 4 seconds.
4. While reset button is still depressed, press the on / off button.
5. Simultaneously release both the on / off button and reset buttons.

Upon completion of these steps, the BMC asserts the clear CMOS signal to emulate the movement of the clear CMOS jumper. The BIOS clears CMOS as if the user had moved the CMOS clear jumper on the baseboard. CMOS is cleared only once per front panel button sequence. The BMC releases the CMOS clear line during the next system reset. Removing the CMOS Clear jumper from the baseboard can disable the Front Panel CMOS reset function. The jumper should be retained in case the CMOS needs to be cleared using the baseboard header.

When the BIOS detects a reset CMOS request, CMOS defaults are loaded during the next POST sequence. Note that non-volatile storage for embedded devices may or may not be affected by the clear CMOS operation depending on the available hardware support. Refer to the sections specific to this platform to determine which embedded device nonvolatile storage areas are cleared during a clear CMOS operation.

7.19 BIOS Updates

There are two major changes to the current method of updating the BIOS code stored in Flash memory on the Intel® Server Board SE7501WV2. Currently, the BIOS updates are achieved via iFLASH updates and by applying recovery procedures as mentioned in the Flash Update Utility section below. In addition, the Intel® Server Board SE7501WV2 also supports On-line Update / Rolling BIOS capability for the purpose of BIOS updates from the OS as described in the Rolling BIOS and On-line updates section below.

7.19.1 Flash Update Utility

The Flash Memory Update utility (iFLASH) loads a fresh copy of the BIOS into flash ROM. The loaded code and data include the following:

- On-board video BIOS, SCSI BIOS, and other option ROMs for the devices embedded on the system board
- The Setup utility
- A user-definable flash area (user binary area)

When running iFLASH in interactive mode, the user may choose to update a particular Flash area. Updating a Flash area reads a file, or a series of files, from a hard or floppy disk, and loads it in the specified area of flash ROM. In interactive mode, iFLASH can display the header information of the selected files.

Note: The iFLASH utility must be run without the presence of a 386 protected mode control program, such as Windows* or EMM386*. iFLASH uses the processor's flat addressing mode to update the Flash component.

7.19.2 Loading the System BIOS

The new BIOS is contained in .BIx files. The number of .BIx files is determined by the size of the BIOS area in the flash part. The number of files is constrained by the fact that the image and the utilities fit onto a single, 1.44 MB DOS-bootable floppy. These files are named as follows:

- xxxxxxxx.BIO
- xxxxxxxx.BI1
- xxxxxxxx.BI2

The first eight letters of each filename can be any value, but the files cannot be renamed. Each file contains a link to the next file in the sequence. iFLASH does a link check before updating to ensure that the process is successful. See Section 7.19.4.

The user binary area is updated during a system BIOS update. The user binary can be updated independently from the system BIOS. CMOS is not cleared when the system BIOS is updated in normal or recovery mode. Configuration information like ESCD is not overwritten during the BIOS flash update. The user is prompted to reboot after a BIOS update completes.

7.19.3 User Binary Area

The baseboard includes an area in flash for implementation-specific OEM add-ons. The user binary area can be saved and updated as previously described in the *Loading the System BIOS* section. For this update, only one file is needed. The valid extension for user files is .USR.

7.19.4 BIOS Recovery Mode

If an update to the system BIOS is not successful or if the system fails to complete POST and BIOS is unable to boot an operating system, it may be necessary to run the BIOS recovery procedure.

To place the baseboard into recovery mode, move the boot option jumper located on the baseboard to the recovery position. The BIOS is then able to execute the recovery BIOS (also known as the boot block) instead of the normal BIOS. The recovery BIOS is a self-contained image that exists solely as a fail-safe mechanism for installing a new BIOS image. The recovery BIOS boots from a 1.44 MB floppy diskette as used in one of the following devices: a standard 1.44 MB floppy drive, a USB 1.44 MB floppy drive, or an LS-120 removable drive. Recovery mode requires at least 4 MB of RAM, and drive A: must be set up to support a 3.5” 1.44 MB floppy drive. This is the mode of last resort, used only when the main system BIOS will not boot. In recovery mode operation, iFLASH (in non-interactive mode only) automatically updates only the main system BIOS. iFLASH senses that the platform is in recovery mode and automatically attempts to update the system BIOS.

Note: During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beeps. Failure is indicated by a long series of short beeps.

7.19.4.1 Performing BIOS Recovery

The following procedure boots the recovery BIOS and flashes the normal BIOS:

1. Turn off the system power.
2. Move the BIOS recovery jumper to the recovery state.
3. Insert a bootable BIOS recovery diskette containing the new BIOS image files.
4. Turn on the system power.

The recovery BIOS boots from the DOS-bootable recovery diskette and emits one beep when it passes control to DOS. DOS then executes a special AUTOEXEC.BAT that contains “iFLASH” on the first line. If it is determined that the system is in recovery mode, iFLASH will start the flash update without user intervention. iFLASH reads the flash image and programs the necessary blocks. It emits one beep to indicate the beginning of the flash operation. After a period of time, the BIOS emits two beeps to indicate that the flash procedure was completed successfully. If the flash procedure fails, the BIOS emits a continuous series of beeps.

When the flash update completes:

1. Turn off the system power.
2. Remove the recovery diskette.
3. Restore the jumper to its original position.
4. Turn on the system power.
5. Re-flash any custom blocks, such as user binary or language blocks.

The system should now boot normally using the updated system BIOS.

7.19.5 Rolling BIOS and On-line updates

The online update nomenclature refers to the ability to update the BIOS while the server is online, in operation, as opposed to having to put the server out of operation while doing a BIOS update. The rolling BIOS nomenclature refers to the capability for having two copies of BIOS: the one in use, and the second to which an updated BIOS version can be written. When ready, the system can roll forward to the new BIOS. In case of a failure with the new version, the system can roll back to the previous version.

In addition to the set of binaries that are used by iFLASH application, the on-line update application relies on a capsule file with a .cit extension, which is generated by the BIOS build process. The usage model is explained in the document titled “Update Application – EPS, On-line FW and BIOS Updates, Rev 1.0”.

While the exact nature of hardware changes for the support of on-line update/rolling BIOS changes are out of scope of this document, BIOS relies on changes to BMC and additional flash space for this. Flash is divided into two partitions, primary and secondary. The active partition from which the system boots shall be referred to as the primary partition. There is a change in iFLASH/On-line updates, in that they continue to preserve the existing BIOS image on the primary partition. Instead, BIOS updates are diverted to the secondary partition. After the update, a notification flag will be set. During the subsequent boot following the BIOS update, the system will continue to boot from the primary BIOS partition. On determining that a BIOS update occurred during the previous boot, the system will request the Baseboard Management Controller (BMC) to switch to the new BIOS image that is on the secondary partition and reset the system. If the boot from the new BIOS is successful, the BIOS will register with the BMC that the change to a new partition is permanent, thus affecting a “Roll Forward” as mentioned above. The secondary partition is now the primary partition and will be used to boot from until another BIOS update is performed. If a flash failure occurs, the BMC will switch back to the BIOS on the other partition, thus affecting a “Roll Back” as mentioned above.

Unlike IFLASH / On-line updates, a recovery method will continue to change the BIOS on the primary partition.

7.20 BIOS and System Setup

Two utilities are used to configure the BIOS and system resources, the BIOS Setup utility and the System Setup Utility. On-board devices are configured with the BIOS Setup utility that is embedded in flash ROM. BIOS Setup provides enough configuration functionality to boot an operating system image or a CD-ROM containing the System Setup Utility. The System Setup Utility is used to configure the IRQ assignments on PCI add-in cards. The System Setup Utility is released on diskette or CD-ROM. The BIOS Setup Utility is always provided in flash for basic system configuration.

The configuration utilities allow the user to modify the CMOS RAM and NVRAM. The actual hardware configuration is accomplished by the BIOS POST routines and the BIOS Plug-N-Play Auto-configuration Manager. The configuration utilities update a checksum for both areas, so potential data corruption is detected by the BIOS before the hardware configuration is saved. If the data is corrupted, the BIOS requests that the user reconfigure the system and reboot.

7.20.1 BIOS Setup Utility

This section describes the ROM-resident Setup utility that provides the means to configure the platform. The BIOS Setup utility is part of the system BIOS and allows limited control over on-board resources. The System Setup Utility must be used for configuring the on-board devices and add-in cards.

The user can disable embedded PCI devices through the setup menus. When these devices are disabled through setup, their resources are freed.

The following embedded devices can be disabled through setup menus, making them invisible to a plug-and-play operating system that scans the PCI bus:

- Embedded SCSI
- Embedded video
- Each embedded NIC (2)
- Embedded ATA RAID
- ICH3 USB Controller

Note: The BIOS options described in this section may or may not be present in pre-production versions of the system BIOS. This section describes the BIOS utility as it is planned to be at production and is subject to change. Option locations in a given menu of the BIOS setup utility as described in this section may be different from those observed on any one pre-production version of the system BIOS.

7.20.2 Setup Utility Operation

The ROM-resident BIOS Setup utility is only used to configure on-board devices. The System Setup Utility is required to configure added PCI cards.

The BIOS Setup utility screen is divided into four functional areas. The following table describes each area.

Table 46. Setup Utility Screen

Functional Area	Description
Keyboard Command Bar	Located at the bottom of the screen or as part of the help screen. This bar displays the keyboard commands supported by the Setup utility.
Menu Selection Bar	Located at the top of the screen. Displays the various major menu selections available to the user. The server Setup utility major menus are: Main Menu, Advanced Menu, Security Menu, Server Menu, Boot Menu, and the Exit Menu.
Options Menu	Each Option Menu occupies the left and center sections of the screen. Each menu contains a set of features. Selecting certain features within a major Option Menu drops you into sub-menus.
Item Specific Help Screen	Located at the right side of the screen is an item-specific Help screen.

7.20.2.1 Entering the BIOS Setup Utility

During the BIOS POST operation, the user is prompted to use the F2 function key to enter Setup as follows:

```
Press <F2> to enter Setup
```

A few seconds might pass before Setup is entered. This is the result of POST completing test and initialization functions that must be completed before Setup can be entered. When Setup is entered, the Main Menu options page is displayed.

7.20.2.2 Keyboard Command Bar

The bottom portion of the Setup screen provides a list of commands that are used to navigate through the Setup utility. These commands are displayed at all times.

Each menu page contains a number of configurable options and/or informational fields. Depending on the level of security in affect, configurable options may or may not be changed. If an option cannot be changed due to the security level, its selection field is made inaccessible. The Keyboard Command Bar supports the following table.

Table 47. Keyboard Command Bar

Key	Option	Description
Enter	Execute Command	The Enter key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected option has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu.
ESC	Exit	The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered. When the ESC key is pressed in any sub-menu, the parent menu is re-entered. When the ESC key is pressed in any major menu, the exit confirmation window is displayed and the user is asked whether changes can be discarded. If “No” is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before ESC was pressed without affecting any existing any settings. If “Yes” is selected and the Enter key is pressed, setup is exited and the BIOS continues with POST.
↑	Select Item	The up arrow is used to select the previous value in a pick list, or the previous options in a menu item's option list. The selected item must then be activated by pressing the Enter key.

Key	Option	Description
↓	Select Item	The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the Enter key.
↔	Select Menu	The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed.
Tab	Select Field	The Tab key is used to move between fields. For example, Tab can be used to move from hours to minutes in the time item in the main menu.
-	Change Value	The minus key on the keypad is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list.
+	Change Value	The plus key on the keypad is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list. On 106-key Japanese keyboards, the plus key has a different scan code than the plus key on the other keyboard, but will have the same effect
F9	Setup Defaults	Pressing F9 causes the following to appear: **Setup Confirmation** **Load default configuration now?** **[Yes] [No]** If "Yes" is selected and the Enter key is pressed, all Setup fields are set to their default values. If "No" is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before F9 was pressed without affecting any existing field values
F10	Save and Exit	Pressing F10 causes the following message to appear: **Setup Confirmation** **Save Configuration changes and exit now?** **[Yes] [No]** If "Yes" is selected and the Enter key is pressed, all changes are saved and Setup is exited. If "No" is selected and the Enter key is pressed, or the ESC key is pressed, the user is returned to where they were before F10 was pressed without affecting any existing values.

7.20.2.3 Menu Selection Bar

The Menu Selection Bar is located at the top of the screen. It displays the various major menu selections available to the user:

- Main Menu
- Advanced Menu
- Security Menu
- Server Menu
- Boot Menu
- Exit Menu

These and associated sub-menus are described in the following sections.

7.20.2.4 Main Menu Selections

The following tables describe the available functions on the top-level menus and on various sub-menus. Default values are highlighted.

Table 48. Main Menu Selections

Feature	Option	Description
System Time	HH:MM:SS	Set the System Time.
System Date	MM/DD/YYYY	Set the System Date.
Floppy A	Not Installed **1.44 / 1.2 MB 3½"** 2.88 MB 3½"	Selects Diskette Type.
Hard Disk Pre-delay	**Disabled** 3 seconds 6 seconds 9 seconds 12 seconds 15 seconds 21 seconds 30 seconds	Allows slower spin-up drives to come ready.
Primary IDE Master	Informational. Drive size CD-ROM or ATAPI Removable	Also selects sub-menu
Primary IDE Slave	Informational. Drive size CD-ROM or ATAPI Removable	Also selects sub-menu
Secondary IDE Master	Informational. Drive size CD-ROM or ATAPI Removable	Also selects sub-menu
Processor Settings	N/A	Selects sub-menu
Language	**7-bit English (US**) English (US) Spanish Italian French German	Selects which language BIOS displays. (console re-direction with default VT100+ only works with English)

Table 49. Primary Master and Slave Adapters Sub-menu Selections

Feature	Option	Description
Type	None **Auto**	Auto allows the system to attempt auto-detection of the drive type. None informs the system to ignore this drive.
LBA Mode Control	**Disabled** Enabled	Disabled by default if no devices are detected, otherwise the setting is auto detected This field is informational only.
Multi-Sector Transfer	**Disabled** 2 Sectors 4 Sectors 8 Sectors 16 Sectors	Displays the number of sectors per block for multiple sector transfers. This field is informational only. This option is viewable only if an IDE HDD is detected.
PIO Mode	**Standard** 1 2 3 3 / DMA 1 4 4 / DMA 2	Displays the method for moving data to/from the drive. This field is informational only.
Ultra DMA	2 4	Displays the method for moving data to/from the drive. This field is informational only.

Table 50. Processor Settings Sub-menu

Feature	Option	Description
Processor Type	Information Only	Displays the type of processor(s) installed
Processor POST Speed	Information Only	Displays the measured processor speed
Processor Retest	**Disabled** Enabled	If enabled, BIOS will clear historical processor status and retest all processors on the next boot.
Hyper-Threading Technology	Disabled **Enabled**	Controls the state of Hyper-Threading Technology in the processors.
Processor 1 CPUID	**CPU ID** Non Installed Disabled	Reports CPUID for Processor 1, if present. If empty, reports Not Installed. If disabled by the BMC, reports Disabled.
Processor 1 L2 Cache Size	N/A	Reports L2 Cache Size for Processor 1.
Processor 2 CPUID	CPU ID **Non Installed** Disabled	Reports CPUID of Processor 2 , if present. If empty, reports Not Installed. If disabled by the BMC, reports Disabled.
Processor 2 L2 Cache Size	N/A	Reports L2 Cache Size for Processor 2.

7.20.2.5 Advanced Menu Selections

The following tables describe the menu options and associated sub-menus available on the Advanced Menu.

Table 51. Advanced Menu Selections

Feature	Option	Description
PCI Configuration	N/A	Selects sub-menu.
Peripheral Configuration	N/A	Selects sub-menu.
Memory Configuration	N/A	Selects sub-menu.
Advanced Chipset Control	N/A	Selects sub-menu. May not be present, if there are no advanced chipset settings under user control.
Boot-time Diagnostic screen	**Disabled** Enabled	If enabled, the boot diagnostic screen is displayed during POST. If disabled, the boot logo is displayed during POST.
Reset Configuration Data	**No** Yes	Select 'Yes' if you want to clear the System Configuration Data during next boot. Automatically reset to 'No' in next boot.
Numlock	On **Off**	Sets power on Numlock state.

Table 52. Advanced Chipset Control Sub-menu Selections

Feature	Option	Description
Wake On Ring	Enable **Disable**	Only controls legacy wake up.
Wake On LAN/PME PCI-X B	Enable **Disable**	Only controls legacy wake up on PCI-X segment B.
Wake On PME PCI-X C	Enable **Disable**	Only controls legacy wake up on PCI-X segment C.
Wake On RTC Alarm	Enable **Disable**	Only controls legacy wake up

Table 53. PCI Configuration Sub-menu Selections

Feature	Option	Description
USB Function	N/A	Selects sub-menu
On-board NIC	N/A	Selects sub-menu
On-board SCSI	N/A	Selects sub-menu, if SCSI SKU
On-board R-IDE	N/A	Selects sub-menu, if ATA SKU
On-board Video	N/A	Selects sub-menu
PCI Slot 1B	**Enabled** Disabled	Enable option ROM scan of the device in the selected PCI slot.
PCI Slot 2B	**Enabled** Disabled	Enable option ROM scan of the device in the selected PCI slot. (This option is only present if a 2U riser card is installed.)
PCI Slot 3B	**Enabled** Disabled	Enable option ROM scan of the device in the selected PCI slot. (This option is only present if a 2U riser card is installed.)
PCI Slot 1C	**Enabled** Disabled	Enable option ROM scan of the device in the selected PCI slot.
PCI Slot 2C	**Enabled** Disabled	Enable option ROM scan of the device in the selected PCI slot. (This option is only present if a 2U riser card is installed.)

PCI Slot 3C	**Enabled** Disabled	Enable option ROM scan of the device in the selected PCI slot. (This option is only present if a 2U riser card is installed.)

Table 54. PCI Device, Embedded Devices

Feature	Option	Description
USB Function	Disabled **Enabled**	If disabled, the USB controllers are turned off and the device resources are hidden from the system.
On-board NIC	Disabled **Enabled**	If disabled, embedded NICs are turned off and the device resources are hidden from the system.
On-board NIC 1 ROM	**Enabled** Disabled	If enabled, initialize NIC 1 expansion ROM.
On-board NIC 2 ROM	**Enabled** Disabled	If enabled, initialize NIC 2 expansion ROM.
On-board SCSI	Disabled **Enabled**	If disabled, the embedded SCSI device is turned off and the device resources are hidden from the system. (This option is only present in the SCSI SKU)
On-board SCSI ROM	**Enabled** Disabled	If enabled, initialize embedded SCSI device expansion ROM. (This option is only present in the SCSI SKU)
On-board R-IDE	Disabled **Enabled**	If disabled, the embedded R-IDE device is turned off and the device resources are hidden from the system. (This option is only present in the ATA SKU)
On-board R-IDE ROM	**Enabled** Disabled	If enabled, initialize embedded RIDE device expansion ROM. (This option is only present in the ATA SKU)
On-board Video	**Enabled** Disabled	If disabled, embedded video is turned off and the device resources are hidden from the system.

Table 55. I/O Device/Peripheral Configuration Sub-menu Selections

Feature	Option	Description
Serial 1 (9-pin header) Address	Disabled **3F8h** 2F8h 3E8h 2E8h	Selects the base I/O address for serial port 1.
Serial 1 (9-pin header) IRQ	**4** 3	Selects the IRQ for serial port 1.
Serial 2 (RJ45) Address	Disabled 3F8h **2F8h** 3E8h 2E8h	Selects the base I/O address for serial port 2.
Serial 2 (RJ45) IRQ	4 **3**	Selects the IRQ for serial port 2.
Diskette Controller	Disabled **Enabled**	If disabled, the diskette controller in the Super I/O is disabled.

Legacy USB support	Disabled Keyboard only **Auto** Keyboard and Mouse	If disabled, legacy USB support is turned off at the end of the BIOS POST.
Front Panel USB	Disabled **Enabled**	If disabled, the front panel USB ports are inactive.

Table 56. Memory Configuration Menu Selections

Feature	Option	Description
Extended Memory Test	**Disabled** 1 MB 1 KB Every Location	Selects the size of step to use during Extended RAM tests.
Memory Bank #1	Installed **Not Installed** Disabled	Displays the current status of the memory bank. Disabled indicated that a DIMM in the bank has failed and the entire bank has been disabled.
Memory Bank #2	Installed **Not Installed** Disabled	Displays the current status of the memory bank. Disabled indicated that a DIMM in the bank has failed and the entire bank has been disabled.
Memory Bank #3	Installed **Not Installed** Disabled	Displays the current status of the memory bank. Disabled indicated that a DIMM in the bank has failed and the entire bank has been disabled.
Memory Retest	**No** Yes	Causes BIOS to retest all memory on next boot.

7.20.2.6 Security Menu Selections

Table 57. Security Menu Selections

Feature	Option	Description
User Password is	**Not Installed** Installed	Status only; user cannot modify. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Administrator Password is	**Not Installed** Installed	Status only; user cannot modify. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Set Administrative Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Set User Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clear password jumper on board. Only Displayed when the Administrative Password is set.
Password On Boot	**Disabled** Enabled	If enabled, requires password entry before boot.
Fixed Disk Boot Sector	**None** **Write Protect**	Write protects the boot sector of the hard drive to prevent viruses from corrupting the drive under DOS.

Feature	Option	Description
Secure Mode Timer	**1 minute** 2 minutes 5 minutes 10 minutes 20 minutes 60 minutes 120 minutes	Period of key/PS/2 mouse inactivity specified for Secure Mode to activate. A password is required for Secure Mode to function. Has no effect unless at least one password is enabled.
Secure Mode Hot Key (Ctrl-Alt-)	[Z] [**L**]	Key assigned to invoke the secure mode feature. Cannot be enabled unless at least one password is enabled. Can be disabled by entering a new key followed by a backspace or by entering delete.
Secure Mode Boot	**Disabled** Enabled	System boots in Secure Mode. The user must enter a password to unlock the system. Cannot be enabled unless at least one password is enabled.
Video Blanking	**Disabled** Enabled	Blank video when Secure mode is activated. A password is required to unlock the system. This cannot be enabled unless at least one password is enabled. This option is only present if the system includes an embedded video controller.
Power Switch Inhibit	Disabled Enabled	When enabled, the power switch is inoperable.
NMI Control	**Enabled** Disabled	Enables/disables NMI control through the BMC for the front panel NMI button.

7.20.2.7 Server Menu Selections

Table 58. Server Menu Selections

Feature	Option	Description
System Management	N/A	Selects sub-menu.
Console Redirection	N/A	Selects sub-menu.
Event Log Configuration	N/A	Selects sub-menu.
Fault Resilient Booting	N/A	Selects sub-menu.
Assert NMI on PERR	**Disabled** Enabled	If enabled, PCI bus parity error (PERR) is enabled and is routed to NMI.
Assert NMI on SERR	**Enabled** Disabled	If enabled, PCI bus system error (SERR) is enabled and is routed to NMI.
FRB-2 Policy	**Disable BSP** Do Not Disable BSP Retry 3 Times Disable FRB2 Timer	Controls the policy of the FRB-2 timeout. This option determines when the Boot Strap Processor (BSP) should be disabled if FRB-2 error occur.
POST Error Pause	**Enabled** Disabled	If enabled, the system will wait for user intervention on critical POST errors. If disabled, the system will boot with no intervention, if possible.
Platform Event Filtering	**Disabled** Enabled	Enable/Disable triggers for system sensor events inside the BMC. Only displayed when PEF is enabled. This option is only used for disabling PEF. This feature cannot be used to enable PEF.

Boot Monitoring	**Disabled** 5 minutes, 10 minutes, 15 minutes, 20 minutes, 25 minutes, 30 minutes, 35 minutes , 40 minutes , 45 minutes , 50 minutes , 55 minutes , 60 minutes	Sets the amount of time the OS Watchdog timer is programmed with. If disabled, the OS Watchdog timer is not programmed. BIOS programs this value in the BMC when setting the OS Watchdog timer at the end of POST. This feature is not available if HD OS Boot timeout or PXE OS Boot timeout is enabled.
Boot Monitoring Policy	**Retry 3 times** Retry Service Boot Always Reset	Configures the system response to the expiration of the OS Watchdog timer. If “Retry 3 times” is selected, the system will attempt to boot the OS partition 3 times followed by the Service Partition once. If “Retry Service Boot” is selected, the system will attempt to boot the OS partition 3 times followed by the Service Partition 3 times followed by halting the system. If “Always Reset” is selected, the system will always retry booting the OS partition. This feature is not available if HD OS Boot timeout or PXE OS Boot timeout is enabled.

Table 59. System Management Sub-menu Selections

Feature	Option	Description
Board Part Number	N/A	Information field only
Board Serial Number	N/A	Information field only
System Part Number	N/A	Information field only
System Serial Number	N/A	Information field only
Chassis Part Number	N/A	Information field only
Chassis Serial Number	N/A	Information field only
BIOS Revision	N/A	Information field only. Full BIOS Revision information
BMC Device ID	N/A	Information field only.
BMC Firmware Revision	N/A	Information field only.
BMC Device Revision	N/A	Information field only.
PIA Revision	N/A	Information field only.
SDR Revision	N/A	Information field only.
HSBP Revision	N/A	Information field only, hidden if not detected

Table 60. Serial Console Redirection Sub-menu Selections

Feature	Option	Description
BIOS Redirection Port	Disabled Serial 1 (DB-9) **Serial 2 (RJ45)**	Selects the Serial port to use for BIOS Console Redirection. "Disabled" completely disables BIOS Console Redirection.
ACPI Redirection Port	Disabled Serial 1 (DB-9) **Serial 2 (RJ45)**	Selects the Serial port to use for ACPI Headless Console Redirection. "Disabled" completely disables ACPI Headless Console Redirection.
BIOS Redirection Baud Rate	9600 **19.2k** 57.6K 115.2k	When console redirection is enabled, use the baud rate specified. When the Emergency Management Port shares the COM port as console redirection, the baud rate must be set to 19.2 k to match the Emergency Management Port baud rate, unless auto-baud feature is used. BMC/IPMI may override this value.
BIOS Redirection Flow Control	No Flow Control **CTS/RTS** XON/XOFF CTS/RTS + CD	NoFlow Control = No flow control. CTS/RTS = Hardware based flow control. XON/XOFF = Software flow control. CTS/RTS +CD = Hardware based + Carrier Detect flow control. When EMP is sharing the same serial port as console redirection, the flow control must be set to CTS/RTS or CTS/RTS+CD depending on whether a modem is used.
Bios Redirection Terminal Type	**VT100+** VT-UTF8 PC-ANSI	This selects the character set to send out the serial port when console redirection is enabled. VT-UTF8 makes use of Unicode characters and is intended specifically for use by new Microsoft software or other companies that use Unicode. PC-ANSI is a "legacy" selection that uses the same character map as previous Intel server console redirection and is intended to support existing software. Note that for VT100+ you must select English as your language.
Serial Port Connector	Serial A **Serial B/EMP**	Only present on 1U systems. Selects which serial port will be routed to the serial port connector on the back of the chassis. Serial A selects UARTA and Serial B selects UARTB.

Table 61. Event Log Configuration Sub-menu Selections

Feature	Option	Description
Clear All Event Logs	**No** Yes	When yes is chosen, the BIOS will clear the System Event Log on the next boot.
Event Logging	Disabled **Enabled**	Enables / disables System Event Logging.
Critical Event Logging	Disabled **Enabled**	Enables/ disables critical system event logging including PERR, SERR, ECC memory errors, and NMI.

Table 62. Fault Resilient Boot Sub-menu Selections

Feature	Option	Description
Late POST Timeout	**Disable** 5 minutes 10 minutes 15 minutes 20 minutes	Controls the timeout value for addin PCI cards to be detected and execute their option ROMs.
Fault Resilient Booting	**Stay ON** Reset Poweroff	Controls the FRB policy upon timeout for Late POST timeout, Hard Disk OS Boot Timeout, and PXE OS Boot Timeout.
Hard Disk OS Boot Timeout	**Disable** 5 minutes 10 minutes 15 minutes 20 minutes	Controls the time limit allowed for booting an OS from a Hard Disk. This option is not available when Boot Monitoring is enabled.
PXE OS Boot Timeout	**Disable** 5 minutes 10 minutes 15 minutes 20 minutes	Controls the time limit allowed for booting an OS using PXE boot. This option is not available when Boot Monitoring is enabled.

7.20.2.8 Boot Menu Selections

Boot Menu options allow the user to select the boot device. The following table is an example of a list of devices ordered in priority of the boot invocation. Items can be re-prioritized by using the up and down arrow keys to select the device. Once the device is selected, use the Enter key to move the device to the current boot priority.

Table 63. Boot Menu Selections

Feature	Option	Description
Quiet Boot	Disabled **Enabled**	If enabled, the BIOS will display the OEM logo during POST. This option is hidden if the BIOS does not detect a valid logo in the flash area reserved for this purpose.
Boot Device Priority	N/A	Selects sub-menu.
Hard Disk Drives	N/A	Selects sub-menu.
Removable Devices	N/A	Selects sub-menu.
ATAPI CD-ROM Drives	N/A	Selects sub-menu.

Table 64. Boot Device Priority Selections

Boot Priority	Device	Description
1	Removable Devices	Attempt to boot from a legacy floppy A: or removable media device like LS-120.
2	Hard Drive	Attempt to boot from a hard drive device.
4	ATAPI CD-ROM Drive	Attempt to boot from an ATAPI CD-ROM drive.

Boot Priority	Device	Description
5	(any) SCSI CD-ROM Drive	Attempt to boot from a SCSI CD-ROM containing bootable media. This entry will appear if there is a bootable CD-ROM that is controlled by a BIOS Boot Specification compliant SCSI option ROM.
6	PXE UNDI	Attempt to boot from a network. This entry will appear if there is a network device in the system that is controlled by a PXE compliant option ROM.

Table 65. Hard Drive Selections

Option	Description
Drive #1 (or actual drive string) Other bootable cards Additional entries for each drive that has a PnP header	To select the boot drive, use the up and down arrows to highlight a device, then press the plus key (+) to move it to the top of the list or the minus key (–) to move it down. Other bootable cards cover all the boot devices that are not reported to the system BIOS through BIOS boot specification mechanism. It may or may not be bootable, and may not correspond to any device. If BIOS boot spec. support is set to limited, this item covers all drives that are controlled by option ROMs (like SCSI drives). Press ESC to exit this menu.

Table 66. Removable Devices Selections

Feature	Option	Description
Lists Bootable Removable Devices in the System	+ –	Use +/– keys to place the removable devices in the boot order you want. Includes Legacy 1.44 MB floppy, 120 MB floppy etc.

7.20.2.9 Exit Menu Selections

The following menu options are available on the Exit menu. The up and down arrow keys are used to select an option, then the Enter key is pressed to execute the option.

Table 67. Exit Menu Selections

Option	Description
Exit Saving Changes	Exit after writing all modified Setup item values to NVRAM.
Exit Discarding Changes	Exit leaving NVRAM unmodified. User is prompted if any of the setup fields were modified.
Load Setup Defaults	Load default values for all SETUP items.
Load Custom Defaults	Load values of all Setup items from previously saved Custom Defaults. Hidden if custom defaults are not valid to prevent.
Save Custom Defaults	Stores Custom Defaults in NVRAM.
Discard Changes	Read previous values of all Setup items from NVRAM.

7.21 BIOS Security Features

The Intel® Server Board SE7501WV2 BIOS provides a number of security features. This section describes the security features and operating model.

Note: The Intel® Server Board SE7501WV2 has the ability to boot from a device attached to the USB port, such as a floppy disk, disk drive, CD-ROM, or ZIP* drive, even if it is attached through a hub. The security model is not supported when booting to a USB device.

7.21.1 Operating Model

The following table summarizes the operation of security features supported by the Intel® Server Board SE7501WV2 BIOS.

Table 68. Security Features Operating Model

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Secure mode	Keyboard Inactivity Timer, Runtime activation of PS/2 keyboard controller Hotkey	User Password enabled in setup	• On-board video goes blank (if enabled in Setup). • All switches on the front panel except NMI are disabled • No PS/2 mouse or PS/2 keyboard input is accepted. • Keyboard LEDs flash	User Password	• Video is restored. • Front Panel switches are enabled. • Keyboard and mouse inputs are accepted.
Secure boot	Power On/Reset	User Password and Secure Boot Enabled	• Prompts for password, if booting from drive A • Enter secure mode just before scanning option ROMs i.e. Keyboard LEDs flash, but video blanking and front panel lock is not invoked until operating system boot • All the switches on the front panel are disabled except NMI. • No input from PS/2 mouse or PS/2 keyboard is accepted; however, the Mouse driver is allowed to load before a password is required. • If booting from drive A, and the user enters correct password, the system boots normally.	User Password	• Floppy writes are re-enabled. • Front panel switches are re-enabled. • PS/2 Keyboard and PS/2 mouse inputs are accepted. • System attempts to boot from drive A. If the user enters correct password, and drive A is bootable, the system boots normally
Password on boot	Power On/Reset	User Password set and password on boot enabled and Secure Boot Disabled in setup	• System halts for user Password before scanning option ROMs. The system is not in secure mode. • No mouse or keyboard input is accepted except the password.	User Password	• Front Panel switches are re-enabled. • PS/2 Keyboard and PS/2 mouse inputs are accepted. • The system boots normally. Boot sequence is determined by setup options.
Fixed disk boot sector	Power On/Reset	Set feature to Write Protect in Setup	Will write protect the master boot record of the IDE hard drives only if the system boots from a floppy. The BIOS will also write protect the boot sector of the drive C: if it is an IDE drive.	Set feature to Normal in Setup	Hard drive will behave normally.

7.22 Password Protection

The BIOS uses passwords to prevent unauthorized tampering with the system. Once secure mode is entered, access to the system is allowed only after the correct password(s) has been entered. Both the user and administrator passwords are supported by the BIOS. The Administrator password must be set prior to setting the User password. The maximum length of the password is seven characters. The password can have only alphanumeric characters (a-z, A-Z, 0-9). The user and administrator passwords are not case sensitive.

Once set, a password can be cleared by changing it to a null string. Entering the user password allows the user to modify the time, date, language, user password, secure mode timer, and secure mode hot-key setup fields. Other setup fields can be modified only if the administrator password is entered. The user password also allows the system to boot if secure boot is enabled. If only one password is set, this password is required to enter Setup. The Administrator has control over all fields in the setup including the ability to clear the user password.

If the user enters three wrong passwords in a row during the boot sequence, the system will be placed into a halt state. This feature makes it difficult to break the password by “trial and error” method. When entering a password, the backspace key is accepted as a character of the password. Entering the backspace key will result in a wrong password. In addition, when entering a password, the numeric keys are not equal to the numeric keypad keys. For example, if the password contains a ‘0’ entered from the numeric keys, and the user enters ‘0’ from the numeric keypad, the result will be an incorrect password.

The Emergency Management Port password is only utilized by the BMC, this password does not effect the BIOS security in any way, nor does the BIOS security engine provide any validation services for this password. Emergency Management Port security is handled primarily through the BMC and Emergency Management Port utilities.

7.23 Inactivity Timer

If the inactivity timer function is enabled, and no keyboard or mouse actions have occurred for the specified time-out period, the following occurs until the user password is entered:

- PS/2 keyboard and PS/2 mouse input is disabled. PS/2 keyboard lights start blinking.
- On-board video is blanked (if selected in setup)
- Floppy drive is write protected (if selected in setup)
- Front panel reset, sleep (if present) and power switches are locked

If a user password is entered, a time-out period must be specified in setup.

7.24 Hot Key Activation

Rather than having to wait for the inactivity time-out to expire, a hot-key combination allows the user to activate secure mode immediately. The hot-key combination is configured through Setup. The following keys are valid hot keys: Ctrl-Alt <L, Z>. Setup will not permit the user to choose any other key as the hot key. Note that the hot key will only work on PS/2 keyboards. The hot key will also only work locally; it will not work from a remote session over redirection.

7.25 Password Clear Jumper

If the user or administrator password(s) is lost or forgotten, both passwords may be cleared by moving the password clear jumper on the base board, into the “clear” position. The BIOS determines if the password clear jumper is in the “clear” position during BIOS POST and clears any passwords if required. The password clear jumper must be restored to its original position before a new password(s) can be set.

7.26 Secure Mode (Unattended start)

Secure mode refers to a system state where many of the external inputs and outputs are disabled to prevent tampering. These include PS/2 ports, floppy and on-board video.

7.27 Front Panel Lock

The front panel buttons, including power and reset, are always disabled when the system is in secure mode. If the system has a sleep switch, it will also be disabled while the system is in secure mode.

7.28 Video Blanking

If enabled in Setup, and a monitor is attached to the embedded VGA controller, the video will be blanked upon entering secure mode. This feature prevents unauthorized users from viewing the screen while the system is in secure mode. Video monitors attached to add-in video adapters will not be blanked regardless of the setting of the video blanking feature.

7.29 PS/2 Keyboard and Mouse Lock

Keyboard and/or mouse devices attached to the PS/2 connector are unavailable while the system is in secure mode. The keyboard controller will not pass any keystrokes or mouse movements to the system until the correct user password is entered.

Note: Because secure mode has direct control of the keyboard controller and is able to secure access to the system via the PS/2 connector, the USB ports are not under secure mode control. USB ports are still functional when the system is in secure mode. It is recommended that all USB ports be “Disabled” in BIOS setup if a Secure Mode environment is in use.

7.30 Secure Boot (Unattended Start)

Secure boot allows the system to boot and run the operating system without requiring the user password even if a user password is set. Secure boot is nothing but booting the system while keeping it in secure mode. However, until the user password is entered, mouse input, keyboard input, and activation of the enabled secure mode features described above are not accepted.

In secure boot mode, if the BIOS detects a floppy diskette in the A: drive at boot time, it displays a message and waits for the user password before booting. After the password is entered, the system can boot from the floppy and secure mode is disabled. Any of the secure mode triggers will cause the system to return to secure mode.

If there is no diskette in drive A, the system will boot from the next boot device and will automatically be placed into secure mode. The PS/2 keyboard and mouse are locked before option ROMs are scanned. Video is blanked and the front panel is locked immediately before the operating system boots. If secure boot is enabled, the user cannot enter option ROM setup unless the user password is entered. This prevents entering the configuration utilities in the option ROMs where it is possible to format drives, etc. The on-board video is not blanked until the end of the POST.

7.31 Error Handling

This section defines how errors are handled by the system BIOS. It also discusses the role of the BIOS in handling errors, and the interaction between the BIOS, platform hardware, and server management firmware with regard to error handling. In addition, error-logging techniques are described and beep codes for errors are defined.

7.31.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors which can be disabled and enabled individually or as a group, can be categorized as follows:

- PCI bus
- Memory single- and multi-bit errors
- Sensors
- Processor internal errors, bus/address errors, thermal trip errors, temperatures and voltages, and GTL voltage levels
- Errors detected during POST, logged as POST errors

Sensors are managed by the BMC. The BMC is capable of receiving event messages from individual sensors and logging system events. Refer to the Intel® Server Board SE7501WV2 BMC EPS for additional information concerning BMC functions.

7.32 SMI Handler

The SMI handler is used to handle and log system level events that are not visible to the server management firmware. If the SMI handler control bit is disabled in Setup, SMI signals are not generated on system errors. If enabled, the SMI handler preprocesses all system errors, even those that are normally considered to generate an NMI. The SMI handler sends a command to the BMC to log the event and provides the data to be logged. System events that are handled by the BIOS generate a SMI.

7.33 PCI Bus Error

The PCI bus defines two error pins: PERR# for reporting parity errors and SERR# for reporting system errors. The BIOS can be instructed to enable or disable reporting PERR# and SERR# through NMI. For a PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if bit 2 of I/O register 61 is set to 0. If SERR# is enabled in BIOS setup, all PCI-to-PCI bridges will generate an SERR# on the primary interface whenever an SERR# occurs on the secondary side of the bus. The same is true for PERR#s.

7.34 Processor Bus Error

If irrecoverable errors are encountered on the host processor bus, proper execution of the BIOS SMI handler cannot be guaranteed. The BIOS SMI handler will record errors to the system event log only if the system has not experienced a catastrophic failure that compromises the integrity of the SMI handler.

7.35 Single-Bit ECC Error Throttling Prevention

The system detects, corrects, and logs correctable errors as long as these errors occur infrequently (the system should continue to operate without a problem).

Occasionally, correctable errors are caused by a persistent failure of a single component. Although these errors are correctable, continual calls to the error logger can throttle the system, preventing further useful work.

For this reason, the system counts certain types of correctable errors and disables reporting if errors occur too frequently. Error correction remains enabled but calls to the error handler are disabled. This allows the system to continue running, despite a persistent correctable failure. The BIOS adds an entry to the event log to indicate that logging for that type of error has been disabled. This entry indicates a serious hardware problem that must be repaired at the earliest possible time.

The system BIOS implements this feature for correctable bus errors. If ten errors occur within an hour, the corresponding error handler disables further reporting of that type of error. The BIOS re-enables logging and SMIs the next time the system is rebooted.

7.36 System Limit Error

The BMC monitors system operational limits. It manages the A/D converter, defining voltage and temperature limits as well as fan sensors and chassis intrusion. Any sensor values outside of specified limits are fully handled by BMC. The BIOS does not generate an SMI to the host processor for these types of system events.

Refer to the Intel® Server Board SE7501WV2 *Server Management External Architecture Specification* for details on various sensors and how they are managed.

7.37 Boot Event

The BIOS downloads the system date and time to the BMC during POST and logs a boot event in the system event log. Software applications that parse the event log should not treat this boot event as an error.

7.38 Fault Resilient Booting (FRB)

The BIOS and firmware provide a feature to guarantee that the system boots, even if one or more processors fail during POST. The BMC contains two watchdog timers that can be configured to reset the system upon time-out.

7.38.1 FRB3

FRB3 refers to the FRB algorithm that detects whether the BSP is healthy enough to run BIOS at all. The BMC starts the FRB3 timer when the system is powered up or hard reset. The BIOS stops this timer in the power-on self test (POST) by asserting the *FRB3 timer halt* signal to the BMC. This requires that the BSP actually runs BIOS code. If the timer is not stopped within 5 seconds, and it expires, the BMC disables the BSP, logs an FRB3 error event, chooses another BSP (from the set of non-failed processors), and resets the system. FRB3 provides a check to verify that the selected BSP is not dead on start up and can actually run code. This process repeats until either the system boots without an FRB3 timeout, or all of the remaining processors have been disabled. At this point, if all the processors have been disabled, the BMC will attempt to boot the system on one processor at a time, irrespective of processor error history. This is called desperation mode.

7.38.2 FRB2

FRB2 refers to the level of FRB in which the BIOS uses the BMC watchdog timer to back up its operation during POST. The BIOS configures the watchdog timer for approximately 6-10 minutes indicating that the BIOS is using the timer for the FRB2 phase of operation.

After BIOS has identified the BSP and saved that information, it will then check to see if the watchdog timer expired on the previous boot. If so, it will store the Time Out Reason bits in a fixed CMOS location (token name = cmosWDTimerFailReason) for applications or a User Binary to examine and act upon. Next, it sets the watchdog timer FRB2 timer use bit, loads the watchdog timer with the new timeout interval, and disables FRB3 using the *FRB3 timer halt* signal. This sequence ensures that no gap exists in watchdog timer coverage between FRB3 and FRB2.

Note: FRB2 is not supported when the BIOS is in Recovery Mode.

If the watchdog timer expires while the watchdog use bit is set to FRB2, the BMC logs a watchdog expiration event showing an FRB2 timeout (if so configured). It then hard resets the system, assuming Reset was selected as the watchdog timeout action.

The BIOS is responsible for disabling the FRB2 timeout before initiating the option ROM scan, prior to displaying a request for a Boot Password or prior to an Extensive Memory Test. The BIOS will re-enable the FRB2 timer after the Extensive Memory Test. The BIOS will provide a user-configurable option to change the FRB2 response behavior. These four options shall be:

- Disable on FRB2
- Never Disable
- Disable after 3 consecutive FRB2s
- Disable FRB2 timer

The option of “Disable on FRB2” will do the following. If the FRB2 timer expires (i.e., a processor has failed FRB2), the BMC resets the system. As part of its normal operation, the BIOS obtains the watchdog expiration status from the BMC. If this status shows an expiration of the FRB2 timer, the BIOS logs an FRB2 event with the event data being the last Port 80h code issued in the previous boot. The BIOS also issues a Set Processor State command to the

BMC, indicating an FRB2 failure and telling it to disable the BSP and reset the system. The BMC then disables the processor that failed FRB2 and resets the system, causing a different processor to become the BSP.

The option of “Never Disable” will perform all the same functions as “Disable on FRB2” with the exception that the BIOS will not send a Set Processor State command to the BMC. The BIOS will still log the FRB2 event in the SEL.

The option of “Disable after 3 consecutive FRB2s” will perform all the same functions as “Disable on FRB2” with the following exception. The BIOS will maintain a failure history of the successive boots. If the same BSP fails 3 consecutive boots with an FRB2, the processor would then be disabled. If the system successfully boots to a BSP, the failure history maintained by the BIOS should be cleared.

The option of “Disable FRB2 Timer” will cause the BIOS to not start the FRB2 timer in the BMC during POST. If this option is selected, the system will have no FRB protection after the FRB3 timer is disabled. The BIOS and BMC implement additional safeguards to detect and disable the application processors (AP) in a multiprocessor system. If an AP fails to complete initialization within a certain time, it is assumed to be nonfunctional. If the BIOS detects that an AP is nonfunctional, it requests the BMC to disable that processor. When the BMC disables the processor and generates a system reset, the BIOS will not see the bad processor in the next boot cycle. The failing AP is not listed in the MP table (refer to the *Multi-Processor Specification,* Rev. 1.4), nor in the ACPI APIC tables, and is invisible to the operating system.

All the failures (late POST, OS Boot, FRB-3, FRB-2, and AP failures) including the failing processor are recorded into the System Event Log. However, the user should be aware that if the setup option for error logging is disabled, these failures are not recorded. The FRB-3 failure is recorded automatically by the BMC while the late POST, OS Boot, FRB-2, and AP failures are logged to the SEL by the BIOS. In the case of an FRB-2 failure, some systems will log additional information into the OEM data byte fields of the SEL entry. This additional data indicates the last POST task that was executed before the FRB-2 timer expired. This information may be useful for failure analysis.

The BMC maintains failure history for each processor in nonvolatile storage. Once a processor is marked “failed,” it remains “failed” until the user forces the system to retest the processor. The BIOS reminds the user about a previous processor failure during each boot cycle until all processors have been retested and successfully pass the FRB tests or AP initialization. Processors that have failed in the past are not allowed to become the BSP and are not listed in the MP table and ACPI APIC tables.

It might happen that all the processors in the system are marked bad. An example is a uni-processor system where the processor has failed in the past. If all the processors are bad, the system does not alter the BSP; it attempts to boot from the original BSP. Error messages are displayed on the console, and errors are logged in the System Event Log of a processor failure.

If the user replaces a processor that has been marked bad by the system, the user must inform the system of this change by running BIOS Setup and selecting that processor to be retested. If a bad processor is removed from the system and is replaced with a new processor, the BMC automatically detects this condition and clears the status flag for that processor during the next boot.

There are three possible states for each processor slot:

1. Processor installed (status only, indicates processor has passed BIOS POST).
2. Processor failed. The processor may have failed FRB-2 or FRB-3, and has been disabled.
3. Processor not installed (status only, indicates the processor slot has no processor in it).

7.39 Boot Monitoring

7.39.1 Purpose

The Boot Monitoring feature is designed to allow watchdog timer protection of the OS load process. This is done in conjunction with an OS-present device driver or application that will disable the watchdog timer once the OS has successfully loaded. If the OS load process fails, the BMC will reset the system. This feature can be configured through BIOS Setup to operate in one of three modes or be disabled (the default state). In the “Always Reset” mode, the BMC will reset the system if the OS-present device driver or application does not disable the watchdog timer. In the “Retry 3 times” mode, after 3 consecutive failures to load the OS successfully, the BIOS will automatically boot to the Service Partition, if present. If a valid Service Partition is not detected, the system should continue to boot. If the Service Partition boot fails, the cycle starts again. In the “Retry Service Boot” mode, the system operates in a similar manner to the “Retry 3 times” mode. The system will instead try to boot the Service partition up to 3 consecutive times. If this is unsuccessful, the system halts. Additionally, in this mode, if a valid Service Partition is not detected, the system will halt rather than attempt to boot to it.

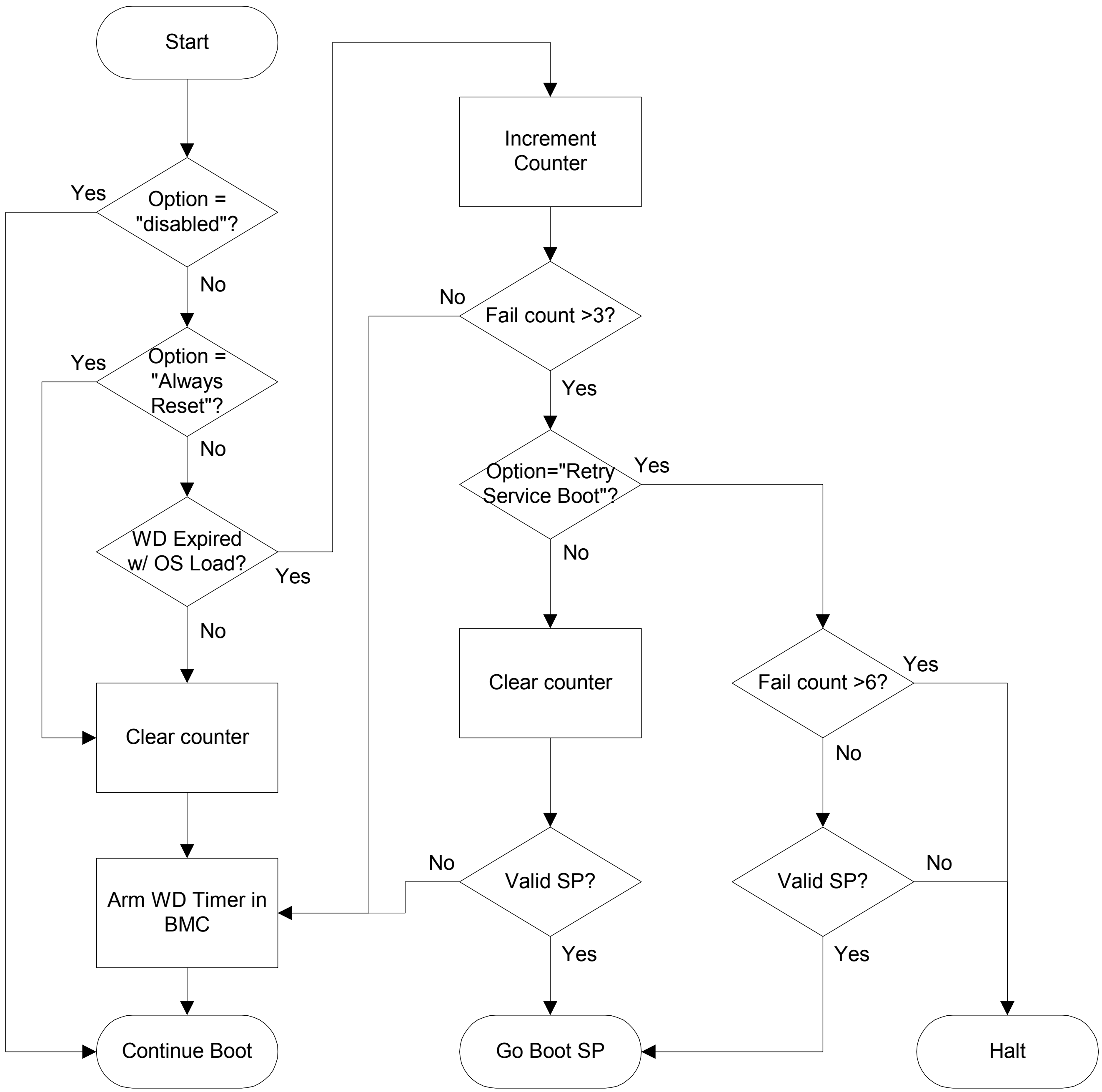


Figure 38. BIOS Boot Monitoring Flowchart

7.40 Logging Format Conventions

The BIOS complies with Version 1.5 of the *Intelligent Platform Management Interface Specification*. IPMI specifications 0.9, 1.0, and 1.5 define the required use of all but two bytes in each event log entry, Event Data 2 and Event Data 3. An event generator can specify that these bytes contain OEM-specified values. The system BIOS uses these two bytes to record additional information about the error.

The format of the OEM data bytes (Event Data 2 and Event Data 3) for memory errors, PCI bus errors and FRB-2 errors has been standardized and is described here. Although only one format is defined in this version, this specification allows for multiple formats. This format is supported by all platforms that are compliant with IPMI Version 1.0 (or later).

Bits 3:1 of the generator ID field define the format revision. The system software ID is a 7-bit quantity. For events discussed in this document, the system software IDs are within the range 0x18 – 0x1F. System software ID of 0x18 indicates that OEM data byte 2 and 3 are encoded using data format scheme revision 0. The current document defines revision 0 of the format.

System software IDs in the range of 0x10 through 0x1f are reserved for the SMI handler. The IPMI specification reserves two distinct ranges for the BIOS and SMI handler. Since the distinction between the two is not significant, the same generator ID values are used for the BIOS and the SMI handler. Technically, the FRB-2 event is not logged by the SMI handler, but it will use the same generator ID range as memory errors. This makes it easier for the BIOS and the event log parser code.

The BIOS logs events using the discrete event trigger class. For this class, the format of the event data bytes is defined in Table 17.5 of the *Intelligent Management Platform Interface Specification*.

The system BIOS sensors are logical entities that generate events. The BIOS ensures that each combination of sensor type (e.g., memory) and event type (e.g., sensor-specific) has a unique sensor number.

7.40.1 Memory Error Events

The following table defines the data byte formats for memory-related errors logged by the BIOS. Memory errors, both correctable and uncorrectable cause an SMI. The BIOS then reads the current memory error state from the North Bridge to generate IPMI sensor events. The BIOS will count the number of correctable memory errors that occur on each DIMM over time. If more than 10 errors occur on a DIMM within an hour, an Event Logging Disabled event will be generated and logging of correctable errors will be stopped until the next reset or power-on. If the BIOS detects an uncorrectable error, it will generate an *Uncorrectable ECC* event against the memory sensor and set the *failed* offset in the associated DIMM sensor (if a failing DIMM can be determined).

Table 69. Memory Error Event Data Field Contents

Field	IPMI Definition	BIOS-Specific Implementation
Generator ID	7:1 System software ID or IPMB slave address. 1=ID is system software ID 0=ID is IPMB slave address.	If BIOS is the source: 7:4 0x3 for system BIOS 3:1 1 = Format revision, Revision of the data format for OEM data bytes 2 and 3, For this revision of the specification, set this field to 1. All other revisions are reserved for now. 0 1 = ID is system software ID. As a result, the generator ID byte will start from 0x31 and go up to 0x3f, in increments of 2 for events logged by the BIOS. If BMC is the source: 7:1 7 bit I^2C Slave Address 0 0 = ID is IPMB Slave Address
Sensor Type	Sensor Type Codes, in the *Intelligent Management Platform Interface Specification v1.5*.	0xC for memory errors
Sensor Number	Number of sensor that generated this event	Unique value for each type of event because IPMI specification requires it that way. This field has no other significance. Should not be displayed to the end user if the event is logged by BIOS. For Single Bit memory errors the value is 0x08, for Multi-bit memory errors, the value is 0x08. For Single Bit memory error login disabled, the value is 0x09.
Type code	0x6F if event offsets are specific to the sensor	0x6F
Event Data 1	7:6 00 = unspecified byte 2 10 = OEM code in byte 2. 5:4 00 = unspecified byte 3 10 = OEM code in byte 3. (BIOS will not use encodings 01 and 11 for errors covered by this document.). 3:0 Offset from Event Trigger for discrete event state.	Follow IPMI definition. If either of the two data bytes following this do not have any data, that byte should be set to 0xff, and the appropriate filed in event data 1 should indicate that that it is unspecified. According to Table 30.3 in the *Intelligent Management Platform Interface Specification*, 3:0 is 0 for single bit error and 1 for multi-bit error.
Event Data 2	7:0 OEM code 2 or unspecified.	If format rev is 1 and if this byte is specified, Syndrome Byte.
Event Data 3	7:0 OEM code 3 or unspecified.	For format rev 1, if this byte is specified, 7:6 Zero based Memory card number. Matches the number of type 16 entry in SMBIOS table. For example, card 0 corresponds to the first type 16 entry in SMBIOS tables. If all DIMMs are onboard, this field will always be 0. 5:0 Zero based DIMM number on the card. DIMM 0 corresponds to the first type 17 record in SMBIOS tables for that memory card.

7.40.2 PCI Error Events

The following table defines the data byte formats for PCI bus-related errors logged by the BIOS.

Table 70. PCI Error Event Data Field Contents

Field	IPMI Definition	BIOS Specific Implementation
Generator ID	7:1 System software ID or IPMB slave address. 1=ID is system software ID; 0=ID is IPMB slave address.	7:4 0x3 for system BIOS 3:1 0 Format revision, Revision of the data format for OEM data bytes 2 and 3, For this revision of the specification, set this field to 0. All other revisions are reserved for now. 0 1=ID is system software ID As a result, the generator ID byte will start from 0x31 and go up to 0x3f, in increments of 2 for events logged by the BIOS.
Sensor Type	See Table 34.3, Sensor Type Codes, in the *Intelligent Management Platform Interface Specification v1.5*.	0x13 for critical interrupt
Sensor number	Number of sensor that generated this event	Unique value for each type of event because IPMI specification requires it that way. This field has no other significance. Should not be displayed to the end user if the event is logged by BIOS. For PERRs, the sensor number is 0xEA, for SERRs, the sensor number is 0xEB.
Type code	0x6F if event offsets are specific to the sensor	0x6F
Event Data 1	7:6 00 = unspecified byte 2 10 = OEM code in byte 2 5:4 00 = unspecified byte 3 10 = OEM code in byte 3. (BIOS will not use encodings 01 and 11 for errors covered by this document.) 3:0 Offset from Event Trigger for discrete event state.	Follows the IPMI definition. If either of the two data bytes following this do not have any data, that byte should be set to 0xff, and the appropriate filed in event data 1 should indicate that that it is unspecified. According to Table 30.3 in the *Intelligent Management Platform Interface Specification*, 3:0 is 04 for PCI PERR and 05 for PCI SERR.
Event Data 2	7:0 OEM code 2 or unspecified	For format rev 0, if this byte is specified, it contains the PCI bus number on which the failing device resides. If the source of the PCI error cannot be determined, this byte contains 0xff and the event data 1 byte indicates that byte 2 is unspecified.
Event Data 3	7:0 OEM code 3 or unspecified.	For format rev 0, if this byte is specified, it contains the PCI device/function address in the standard format: 7:3 Device number of the failing PCI device 2:0 PCI function number. Will always contain a zero if the device is not a multifunction device. If the source of the PCI error cannot be determined, this byte contains 0xff and the event data 1 byte indicates that byte 3 is unspecified.

The following table provides examples of the event data fields for PCI device-related errors.

Table 71. Examples of Event Data Field Contents for PCI Errors

Error Type	Event Data 1	Event Data 2	Event Data 3
PCI PERR, failing device is not known	04	0xFF	0xFF
PCI SERR, failing device is not known	05	0xFF	0xFF
PCI PERR, device 3, function 1 on PCI bus 5 reported the error	0xA4	0x05	0x19 (Bits 7:3 = 03 Bits 2:0 = 01)
An unknown device on PCI bus 0 reported the SERR	0x85	0x00	0xFF

7.40.3 FRB-2 Error Events

The following table defines the data byte formats for FRB-2 errors logged by the BIOS.

Table 72. FRB-2 Event Data Field Contents

Field	IPMI Definition	BIOS Specific Implementation
Generator ID	7:1 System software ID or IPMB slave address. 1=ID is system software ID; 0=ID is IPMB slave address	7:4 0x3 for system BIOS 3:1 0 Format revision, Revision of the data format for OEM data bytes 2 and 3, For this revision of the specification, set this field to 0. All other revisions are reserved for now. 0 1=ID is system software ID As a result, the generator ID byte will start from 0x31 and go up to 0x3f, in increments of 2 for events logged by the BIOS.
Sensor Type	See Table 34.3, Sensor Type Codes, in the *Intelligent Management Platform Interface Specification v1.5*.	0x7 for processor related errors
Sensor number	Number of sensor that generated this event	Unique value for each type of event because IPMI specification requires that. This field has no other significance, and it should not be displayed to the end user if the event is logged by BIOS.
Type code	0x6F if event offsets are specific to the sensor	0x6F
Event Data 1	7:6 00 = unspecified byte 2 10 = OEM code in byte 2 5:4 00 = unspecified byte 3 10 = OEM code in byte 3. (BIOS will not use encodings 01and 11 for errors covered by this document.) 3:0 Offset from Event Trigger for discrete event state.	If Event data 2 and event data 3 contain OEM codes, bits 7:6 and bits 5:4 contain 10. For platforms that do not include the POST code information with FRB-2 log, both these fields will be 0. BIOS either should specify both bytes or should mark both bytes as unspecified. According to IPMI 1.0 specification, Table 30.3, Byte 3:0 is 03 for FRB-2 failure during POST.
Event Data 2	7:0 OEM code 2 or unspecified	For format rev 0, if this byte is specified, it contains bits 7:0 of the POST code at the time FRB-2 reset occurred (port 80 code)
Event Data 3	7:0 OEM code 3 or unspecified	For format rev 0, if this byte is specified, it contains bits 15:8 of the POST code at the time FRB-2 reset occurred (port 81 code). If the BIOS only uses one byte POST codes, this byte will always be zero.

The following table provides examples of the event data fields for FRB-2 errors.

Table 73. Examples of Event Data Field Contents for FRB-2 Errors

Error type	Event Data 1	Event Data 2	Event Data 3
FRB-2 error, failing POST code information not available	0x03	0xFF	0xFF
FRB-2 error, BIOS uses 1-byte POST codes. The last POST code before FRB-2 reset was 0x60.	0xA3	0x60	0x0
FRB-2 error, BIOS uses 1-byte POST codes. The last POST code before FRB-2 reset was 0x1942.	0xA3	0x42	0x19

7.41 POST Codes, Error Messages, and Error Codes

The BIOS indicates the current testing phase during POST by writing a hex code to the Enhanced Diagnostic LEDs. See Table 40 for a list of supported POST progress codes. If errors are encountered, error messages or codes will either be displayed to the video screen, or if an error has occurred prior to video initialization, errors will be reported through a series of audio beep codes. POST errors are logged in to the System Event Log.

The error codes are defined by Intel and whenever possible are backward compatible with error codes used on earlier platforms.

7.41.1 POST Progress Code LEDs

The SE7501WV2 provides LEDs to display POST progress codes. The purpose of the POST Progress Code LEDs is to provide a troubleshooting tool in the event of a system hang during POST. The LEDs will display the hex POST code for the last test the BIOS performed before the system hung.

The POST Progress Code LED feature consists of a hardware decoder and four dual color LEDs located on the back of the baseboard. During POST, the LEDs will display all normal POST progress codes representing the progress of the BIOS POST. Each code will be represented by a combination of colors from the four LEDs. The LEDs are in pairs of green and red. The POST progress codes are broken into two nibbles, an upper and a lower nibble. Each bit in the upper nibble is represented by a red LED and each bit in the lower nibble is represented by a green LED. If both bits are set in the upper and lower nibble then both red and green LEDs are lit, resulting in an amber color. Likewise, if both bits are clear then the red and green LEDs are off.

Table 74. POST Progress Code LED Example

Scenario: BIOS sent value of 95h to POST Progress Code LED

LEDs	Red	Green	Red	Green	Red	Green	Red	Green
95h	1	0	0	1	0	0	1	1
Result	Red		Green		Off		Amber	
	(8) - Hi Bit – as viewed by looking into the system from the back		(4)		(2)		(1) Low Bit – as viewed by looking into the system from the back	

Note: When comparing a diagnostic LED color string from the baseboard to those listed in the diagnostic LED decoder in the following tables, the LEDs on the baseboard should be referenced when viewed by looking into the system from the back. Reading the LEDs from left to right, the Hi bit is located on the left.

7.41.2 POST Error Codes and Messages

The following table defines POST error codes and their associated messages. The BIOS prompts the user to press a key in case of serious errors. Some of the error messages are preceded by the string "Error" to highlight the fact that the system might be malfunctioning. All POST errors and warnings are logged in the System Event Log, unless the System Event Log is full.

Table 75. Standard POST Error Messages and Codes

Error Code	Error Message	Pause on Boot
100	Timer Channel 2 Error	Yes
101	Master Interrupt Controller	Yes
102	Slave Interrupt Controller	Yes
103	CMOS Battery Failure	Yes
104	CMOS Options not Set	Yes
105	CMOS Checksum Failure	Yes
106	CMOS Display Error	Yes
107	Insert Key Pressed	Yes
108	Keyboard Locked Message	Yes
109	Keyboard Stuck Key	Yes
10A	Keyboard Interface Error	Yes
10B	System Memory Size Error	Yes
10E	External Cache Failure	Yes
110	Floppy Controller Error	Yes
111	Floppy A: Error	Yes
113	Hard disk 0 Error	Yes
114	Hard disk 1 Error	Yes
115	Hard disk 2 Error	Yes
116	Hard disk 3 Error	Yes
117	CD-ROM disk 0 Error	Yes
118	CD-ROM disk 1 Error	Yes
119	CD-ROM disk 2 Error	Yes
11A	CD-ROM disk 3 error	Yes
11B	Date/Time not set	Yes
11E	Cache memory bad	Yes
120	CMOS clear	Yes
121	Password clear	Yes
140	PCI Error	Yes
141	PCI Memory Allocation Error	Yes
142	PCI IO Allocation Error	Yes

Error Code	Error Message	Pause on Boot
143	PCI IRQ Allocation Error	Yes
144	Shadow of PCI ROM Failed	Yes
145	PCI ROM not found	Yes
146	Insufficient Memory to Shadow PCI ROM	Yes

Table 76. Extended POST Error Messages and Codes

Error Code	Error Message	Pause on Boot
8110	Processor 1 Internal error (IERR)	No
8111	Processor 2 Internal error (IERR)	No
8120	Processor 1 Thermal Trip error	No
8121	Processor 2 Thermal Trip error	No
8130	Processor 1 disabled	No
8131	Processor 2 disabled	No
8140	Processor 1 failed FRB-3 timer	No
8141	Processor 2 failed FRB-3 timer	No
8150	Processor 1 failed initialization on last boot.	No
8151	Processor 2 failed initialization on last boot.	No
8160	Processor 01: unable to apply BIOS update	Yes
8161	Processor 02: unable to apply BIOS update	Yes
8170	Processor P1 :L2 cache Failed	Yes
8171	Processor P2 :L2 cache Failed	Yes
8180	BIOS does not support current stepping for Processor P1	Yes
8181	BIOS does not support current stepping for Processor P2	Yes
8190	Watchdog Timer failed on last boot	No
8191	4:1 Core to bus ratio: Processor Cache disabled	Yes
8192	L2 Cache size mismatch	Yes
8193	CPUID, Processor Stepping are different	Yes
8194	CPUID, Processor Family are different	Yes
8195	Front Side Bus Speed mismatch. System Halted	Yes, Halt
8196	Processor Model are different	Yes
8197	CPU Speed mismatch	Yes
8198	Failed to load processor microcode	Yes
8300	Baseboard Management Controller failed to function	Yes
8301	Front Panel Controller failed to Function	Yes
8305	Hotswap Controller failed to Function	Yes
8420	Intelligent System Monitoring Chassis Opened	Yes
84F1	Intelligent System Monitoring Forced Shutdown	Yes
84F2	Server Management Interface Failed	Yes
84F3	BMC in Update Mode	Yes
84F4	Sensor Data Record Empty	Yes
84FF	System Event Log Full	No
8500	Bad or missing memory in slot 3A	Yes
8501	Bad or missing memory in slot 2A	Yes

Error Code	Error Message	Pause on Boot
8502	Bad or missing memory in slot 1A	Yes
8504	Bad or missing memory in slot 3B	Yes
8505	Bad or missing memory in slot 2B	Yes
8506	Bad or missing memory in slot 1B	Yes
8601	All Memory marked as fail. Forcing minimum back online	Yes

7.41.3 POST Error Beep Codes

Prior to system video initialization, the BIOS uses beep codes to inform users of error conditions. Short beeps will be generated and an error code will be POSTed on the POST Progress Code LEDs.

7.41.4 BIOS Recovery Beep Codes

In the case of a Bootblock update, where video is not available for text messages to be displayed, speaker beeps are necessary to inform the user of any errors. The following table describes the type of error beep codes that may occur during the Bootblock update.

Table 77. BIOS Recovery Beep Codes

Beeps	Error message	POST Progress Code	Description
1	Recovery started		Start recovery process
2	Recovery boot error	Flashing series of POST codes: E9h EEh EBh ECh EFh	Unable to boot to floppy, ATAPI, or ATAPI CD-ROM. Recovery process will retry.
Series of long low-pitched single beeps	Recovery failed	EEh	Unable to process valid BIOS recovery images. BIOS already passed control to operating system and flash utility.
2 long high-pitched beeps	Recovery complete	EFh	BIOS recovery succeeded, ready for power-down, reboot.

Recovery BIOS will generate two beeps and flash a POST code sequence of 0E9h, 0EAh, 0EBh, 0ECh, and 0EFh on the POST Progress Code LEDs.

During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beeps. Failure is indicated by a long series of short beeps.

7.42 BMC Error Beep Codes

Table 78. BMC Error Beep Codes

Beeps	Description
1	Front panel CMOS clear initiated
1-5-1-1	FRB failure (processor failure)
1-5-2-1	No processors installed
1-5-2-3	Processor configuration error (e.g., mismatched VIDs, Processor slot 1 is empty)
1-5-2-4	Front-side bus select configuration error (e.g., mismatched BSELs)
1-5-4-2	Power fault: DC power unexpectedly lost (e.g. power good from the power supply was deasserted)
1-5-4-3	Chipset control failure
1-5-4-4	Power control failure (e.g., power good from the power supply did not respond to power request)

7.42.1 Bootblock Error Beep Codes

Table 79. Bootblock Error Beep Codes

Beeps	Error message	Description
1	Refresh timer failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity error	Parity can not be reset
3	Base memory failure	Base memory test failure. **See Table 43. "3-Beep-Boot Block Memory Failure Error Code" table for additional error details.
4	System timer	System timer is not operational
5	Processor failure	Processor failure detected
6	Keyboard controller Gate A20 failure	The keyboard controller may be bad. The BIOS cannot switch to protected mode.
7	Processor exception interrupt error	The CPU generated an exception interrupt.
8	Display memory read/write error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM checksum error	System BIOS ROM checksum error
10	Shutdown register error	Shutdown CMOS register read/write error detected
11	Invalid BIOS	General BIOS ROM error

Table 80. Three-beep Boot Block Memory Failure Error Codes

Beep Code		Diagnostic LED Decoder G=Green, R=Red, A=Amber				Meanings
		Hi			Low	
3	00h	Off	Off	Off	Off	No memory was found in the system
3	01h	Off	Off	Off	G	Memory mixed type detected
3	02h	Off	Off	G	Off	EDO is not supported
3	03h	Off	Off	G	G	First row memory test failure
3	04h	Off	G	Off	Off	Mismatched DIMMs in a row
3	05h	Off	G	Off	G	Base memory test failure
3	06h	Off	G	G	Off	Failure on decompressing POST module
3	07h-0Dh	Off G G G G G G	G Off Off Off Off G G	G Off Off G G Off Off	G Off G Off G Off G	Generic memory error
3	0Eh	G	G	G	Off	SMBUS protocol error
3	0Fh	G	G	G	G	Generic memory error

7.43 "POST Error Pause" Option

In case of POST error(s), which occur during system boot-up, BIOS will stop and wait for the user to press an appropriate key before booting the O/S or entering BIOS setup. The user can override this option by setting "POST Error Pause" to "disabled" on the BIOS Setup Server menu page. If the "POST Error Pause" option is set to "disabled", the system will boot the operating system without user-intervention. Option default value is set to "enabled".

7.44 Intel® Server Board SE7501WV2 BIOS Runtime APIs

The Intel® Server Board SE7501WV2 BIOS supports runtime APIs that can be used for diagnostics in a real-mode environment, such as DOS. This interface is in addition to the standard PC-AT INT interface.

7.45 INT 15 Extensions

Table 81. Interrupt 15h Extensions

Function (AX)	Description
DA12h	Cache services
DA15h, DA8Ch	Intel ID string
DA20h	IPMB services and Extended NVRAM extensions
DA92h	Processor information

7.45.1 Cache Services

Cache Services sets the state of the processor caches. Cache services are intended for diagnostic purposes only. The Intel® Server Board SE7501WV2 BIOS does not support switching from writeback to write-through modes.

Call With	AH	= DAh	
	AL	= 12h	
	CL	= 0	Disable cache
		= 1	Enable cache
		= 2	Read cache status
		= 3	Set Writeback Mode
Returns	AH, bit 0		
		= 0	Cache Disabled
		= 1	Cache Enabled
	AH, bit 1		
		= 0	Write-through Mode
		= 1	Writeback Mode
	CX, bit 15		
		= 0	Size information is invalid
		= 1	Size information is valid
	CX, bits 14:0		Size of L2 cache in 32KB blocks
	CF	= 0	Success
		= 1	Function not support (if AH = 86h)

7.45.2 Intel ID String

The Intel ID String sets the Intel ID string for the BIOS. The string may look similar to:

```
SWV20.86B.0001.P01.0006061355
```

Call With	AH	= DAh	
	AL	= 15h and 8Ch	
	ES:DI	= Points to 32-byte buffer to store results	
Returns	CF	= 0	Success
		= 1	Function not support (if AH = 86h)

The 32-byte ID is formatted as follows:

3-7-byte board ID, “SWV2”

1-byte board revision, starting from ‘0’

3-byte OEM ID, ‘86B’ for standard BIOS

4-byte build number

1 – 3 bytes describing build type (D for development, A for Alpha, B for Beta, Pxx for production version xx)

10-byte build date in yymmddtime format

The remaining bytes are reserved for future use

7.45.3 Processor Information

Processor Information returns information about the system processors.

Call With	AH	= DAh
	AL	= 92h
	CL	= Processor number (0…7)
Returns	AL	= Stepping ID
	AH	= Model
	BL	= Family
	BH	= Number of processors supported by platform
	CX	= Processor bus speed in BCD (MHz)
	DX	= Processor core speed in BCD (MHz)
	CF	= 0 Success, or
		= 1 Processor not present, or
		= 1 Function not supported (If AH=86h)

If processor not present, (AH)=87h, (CF)=1

If function not supported, (AH)=86h, (CF)=1

Note: The processor number that is passed in (CL) as input refers to the physical position of the processor.

7.45.4 Extended NVRAM Services

The Intel® Server Board SE7501WV2 BIOS supports NVRAM read and write to specific areas in the NVRAM to support option ROMs that need NVRAM storage. These services are enabled based on the platform requirements.

Call With	AH	= Dah
	AL	= 20h
	BL	= 85 Read Extended NVRAM/Flash
		= 86 Write Extended NVRAM/Flash
	BH	= 0 ESCD area
		= 1 SCSIA area
		= 2 SCSIB area
		= 3 LCD User String area
		= 4 System limits area
		= 5 User NVRAM area
		= 6 Multiboot area
		= 7 GUID/UUID area (data buffer must contain special signatures for the write call to succeed, read always works)
	ES:DI	= Pointer to data buffer

Returns ES:DI = Pointer to data buffer

CF = 0 Success

= 1 Failure

Error codes:

AH = 1 Flash area not supported

= 2 Flash write failed

= 5 Invalid OEM index

= 86h Function not supported

= 88h Security failure

7.45.5 IPMB Services

The system BIOS provides real-mode calls to Read, Write, and Master Read/Write the IPMB. The Read and Write functions are used for all master/slave I^2C devices on all buses.

IPMB Services have the following characteristics:

- They are 16-bit real-mode (EMM386 cannot be running).
- They can be used for all IPMB commands.
- They can be used to communicate with any I2C controller.
- If the carry flag is set, the interface has broken or timed-out.
- The caller is responsible for providing proper inputs. No sanity check is provided.
- The caller is responsible for checking completion code.

7.45.6 INT15h, Function DA20h, Subfunction 99h/9Ah/9Bh – Read/Write/Bus Master Write IMB

Call With AH = Dah

AL = 20h

BH = IMB Command

BL = 99h (Read) or 9Ah (Write)

CH = Bus Indicator

CL = Number of bytes to write

DH = I2C Controller Slave Address

DL[7:2] = Network Function number

DL[1:0] = LUN

ES:DI = Input/Output Buffer

Returns ES:DI = Pointer to output data (if READ)

CF = 0 Success

= 1 Function not supported (if AH = 86h)

7.46 Multiple Processor Support (MPS)

The Intel® Server Board SE7501WV2 BIOS supports one or two Intel® Xeon™ processors with 512 cache.

7.46.1 Multiprocessor Specification Support

The Intel® Server Board SE7501WV2 BIOS complies with all requirements of the Intel *Multi-Processor Specification (MPS), Revision 1.4*, for symmetric multiprocessor support. The version number can be configured using BIOS Setup. The base MP configuration table contains the following entries:

- MP table header
- Processor entries
- PCI bus entries
- I/O APIC entries
- Local interrupt entries
- System address space-mapping entries
- Bus hierarchy descriptor
- Compatibility bus address space modifier entries

7.46.2 Multiple Processor Support

IA-32 processors have a microcode-based MP initialization protocol. On reset, all of the processors compete to become the bootstrap processor (BSP). If a serious error is detected during a Built-in Self-Test (BIST), the processor does not participate in the initialization protocol. A single processor that successfully passes BIST is automatically selected by the hardware as the BSP and starts executing from the reset vector (F000:FFF0h). A processor that does not perform the role of BSP is referred to as an application processor (AP).

The BSP is responsible for executing POST and preparing the machine to boot the operating system. The system BIOS performs several other tasks in addition to those required for MPS support, as described in Revision 1.4 of the MP specification. These tasks are part of the fault resilient booting algorithm. At the time of booting, the system is in virtual wire mode and only the BSP is programmed to accept local interrupts (INTR driven by programmable interrupt controller (PIC) and non-maskable interrupt (NMI)). For platforms with a single processor configuration, the system is put in the virtual wire mode, which uses the local APIC of the processor.

As a part of the boot process, the BSP wakes each AP. When awakened, the AP programs its memory type range registers (MTRRs) to be identical to those of the BSP. All APs execute a halt instruction with their local interrupts disabled. The server management module (SMM) handler expects all processors to respond to an SMI. To ensure that an AP can respond to an SMI, any agent that wakes an AP must ensure that the AP is left in the Halt State, not the “wait for startup IPI” state. The waking agent must also ensure that the code segment containing the halt code executed by an AP is protected and does not get overwritten. Failure to comply with these guidelines results in a system hang during the next SMI.

7.46.3 Mixed Processor Support

The Intel® Server Board SE7501WV2 BIOS supports different versions of processors of various clock frequencies without changes to the BIOS, but only across different system configurations. All installed processors will be configured to run at the same frequency. (For example, the bus frequency of all processors must be identical. If the core frequency of the processors differs, the

BIOS will configure both processors to run at the core speed of the slower processor.) For best performance, all processors must be of the same revision.

Mixing processor families is considered an error condition. Mixing processors with different cache sizes results in a warning message. Mixing steppings (within the same family) is supported as long as the processors are + one or – one stepping within each other, only identical processors are tested by Intel.

The BIOS setup reports the type, cache size and speed of all detected and enabled processors.

7.47 Hyper-Threading Technology

Refer to the *Intel® Netburst™ Micro-architecture BIOS Writer's Guide* for details regarding the implementation of Hyper-Threading Technology-enabled processors. In addition to these requirements, the following are also implemented:

- Display of processors during POST. BIOS displays the number of physical processors detected.
- Display of processors during BIOS Setup. BIOS displays the corresponding physical processors.
- Number of processors in the MPS table. BIOS only presents the primary thread processor in the MPS table.
- SMBIOS Type 4 structures. Unaffected. Type 4 structures refer to sockets not processors.

7.48 OEM Customization

System OEMs can differentiate their products by customizing the BIOS. The extent of customization is limited to that which is stated in this section.

The user binary capability of the system BIOS allows system vendors to change the look and feel of the BIOS and to manage OEM-specific hardware by executing custom code during POST. Custom code should not hook critical interrupts, reprogram the chip set, or take any other action that affects the correct functioning of system BIOS.

7.49 User Binary

System customers can supply 16 KB of code and data for use during POST and at run-time. Individual platforms may support a larger user binary. User binary code is executed at several defined hook points within the POST.

The user binary code is stored in the system flash. If no run-time code is added, the BIOS temporarily allocates a code buffer according to the *POST Memory Manager Specification*. If run-time code is present, the BIOS shadows the entire block as though it were an option ROM. The BIOS leaves this region writeable to allow the user binary to update any data structures it defines. System software can locate a run-time user binary by searching for it like an option ROM, checking each 2KB boundary from C0000h to EFFFFh. The system vendor can place a signature within the user binary to distinguish it from other option ROMs.

Intel will provide the tools and reference code to help OEM's build a user binary. The user binary must adhere to the following requirements:

- In order to be recognized by the BIOS and protected from runtime memory managers, the user binary must have an option ROM header (55AA, size).
- The system BIOS performs a scan of the user binary area at predefined points during POST. Mask bits must be set within the user binary to inform the BIOS if an entry point exists for a given time during POST.
- The system state must be preserved by the user binary.
- User binary code must be relocatable. It will be located within the first Megabyte. The user binary code should not make any assumptions about the value of the code segment.
- User binary code will always be executed from RAM and never from flash.
- The code in user binary should not hook critical interrupts, should not reprogram the chipset and should not take any action that affects the correct functioning of the system BIOS.

The BIOS copies the user binary into system memory before the first scan point. If the user binary reports that it does not contain runtime code, it is located in conventional memory (0 - 640 KB).

Reporting that the user binary is POST has only the advantage that it does not use up limited option ROM space, and more option ROMs can be fitted. If user binary code is required at run-time, it is copied to option ROM space. At each scan-point during POST, the system BIOS determines if this scan-point has a corresponding user binary entry point to which it transfers control.

To determine this, the bitmap at byte 4 of the header is tested against the current mask bit that has been determined / defined by the scan point. If the bitmap has the appropriate bit set, the mask is placed in AL and execution is passed to the address computed by (ADR(Byte 5)+5*scan sequence #).

During execution, the user binary may access 11 bytes of Extended BIOS Data Area RAM (EBDA). The segment of the EBDA can be found at address 40:0e. Offset 18 to offset 21h is available for the user binary. The BIOS also reserves eight CMOS bits for the user binary. These bits are in a non-checksummed region of CMOS with default values of zero, and will always be located in the first bank of CMOS. These bits are contiguous, but are not in a fixed location. Upon entry into the user binary, DX contains a 'token' that points to the reserved bits.

This token has the following format:

MSB LSB

15			12	11											0
# of bits available -1				Bit offset from start of CMOS of first bit											

The most significant 4 bits are equal to the number of CMOS bits available, minus 1. This field is equal to 7 since 8 CMOS bits are available. The 12 least significant bits define the position of the CMOS bit in RTC. This is a bit address, not a byte address. The CMOS byte location is 1/8th of the 12-bit number, and the remainder is the starting bit position within that byte. For example, if the 12-bit number is 0109h, user binary can use bit 1 of CMOS byte 0108h/8 or 021h.

The following code fragment shows the header and format for a user binary:

```
db  55h, 0AAh, 20h   ; 8KB USER Area

MyCode   PROC  FAR   ; MUST be a FAR procedure
db  CBh              ; Far return instruction
db  04h              ; Bit map to define call points, a
                     ; 1 in any bit specifies
                     ; that the BIOS is called at that
                     ; scan point in POST
db  CBh              ; First transfer address used to
                     ; point to user binary extension structure
dw  ?                ; Word Pointer to extension structure
dw  0                ; Reserved

JMP ErrRet           ; This is a list of 7 transfer
                     ; addresses, one for each
JMP ErrRet           ; bit in the bitmap.
                     ; 5 Bytes must be used for each
JMP Start            ; JMP to maintain proper offset for
                     ; each entry. Unused entry JMP's
                     ; should be filled with 5 byte
                     ; filler or JMP to a RETF
 JMP     ErrRet      ;
 JMP     ErrRet
 JMP     ErrRet
 JMP     ErrRet
```

7.49.1 Scan Point Definitions

The following table defines the bitmap for each scan point, indicating when the scan point occurs and which resources are available (RAM, stack, binary data area, video, keyboard).

Table 82. User Binary Area Scan Point Definitions

Scan Point	Mask	RAM/Stack/BDA	Video/Keyboard
Near the pointer to the user binary extension structure. The mask bit is 0 if this structure is not present. Instead of a jump instruction, the scan address (offset 5) contains a 0CB followed by a near pointer.	01h	Not applicable	Not applicable
Obsolete, no action taken.	02h	Not applicable	Not applicable
This scan occurs immediately after video initialization.	04h	Yes	Yes
This scan occurs immediately before video initialization	08h	Yes	No
This scan occurs on POST error. On entry, BX contains the number of the POST error	10h	Yes	Yes

Scan Point	Mask	RAM/Stack/BDA	Video/Keyboard
This final scan occurs immediately prior to the INT 19 for normal boot and allows one to completely circumvent the normal INT 19 boot if desired.	20h	Yes	Yes
This scan occurs immediately before the normal option ROM scan.	40h	Yes	Yes
This scan occurs immediately following the option ROM area scan.	80h	Yes	Yes

7.49.2 Format of the User Binary Information Structure

Table 83. User Binary Information Structure

Offset	Bit definition
0	Bit 0 1 if mandatory user binary, 0 if not mandatory. If a user binary is mandatory, it will always be executed. If a platform supports a disabling of the user binary scan through CU, this bit will override CU setting. Bit 1 1 If runtime presence required (other than SMM user binary portion, SMM user binary will always be present in runtime irrespective of setting of this bit) 0, if not required in runtime, and can be discarded at boot time. Bit 7:2 reserved for future expansion
1 – 0fh	Reserved for future expansion

If this structure is not present, that is, if the mask bit 01 is not set, the system BIOS assumes that the user binary is not mandatory and is required in runtime.

7.49.3 OEM Splash Screen

The Intel® Server Board SE7501WV2 BIOS supports a splash screen during POST; a 16-KB region of flash ROM is available to store the OEM logo in compressed format. The BIOS contains the standard Intel logo. This logo could be stored in the same area as the OEM logo or it could be stored in a separate area. Using the iFLASH utility, this region can be updated with an OEM supplied logo image. The OEM logo must fit within a 640 X 384 size to accommodate the progress meter at the top and hot key messages at the bottom of the screen. If an OEM logo is flashed into the system, it will override the built-in Intel® logo.

Intel supplies utilities that compress and convert a 16-color bitmap file into a logo file suitable for iFLASH. Intel also supplies a blank logo. If the logo area is updated with a blank logo, the system behaves as if there is no logo and will always display the POST diagnostic screen.

7.49.4 Localization

The Intel® Server Board SE7501WV2 BIOS supports English, Spanish, French, German, and Italian. Intel provides translations for all of the strings in the supported languages. The language can be selected using BIOS setup. BIOS setup can detect which languages are included in the language database and present the correct selections to the user.

8. Intel® Server Board SE7501WV2 ACPI Implementation

8.1 ACPI

An ACPI aware operating system (OS) generates an SMI to request that the system be switched into ACPI mode. The BIOS responds by sending the appropriate command to the BMC to enable ACPI mode. The system automatically returns to legacy mode upon hard reset or power-on reset.

The Intel® Server Board SE7501WV2 supports S0, S1, S4, and S5 states. When the system is operating in ACPI mode, the operating system retains control of the system and operating system policy determines the entry methods and wakeup sources for each sleep state. Sleep entry and wakeup event capabilities are provided by the hardware but are enabled by the operating system.

S0 Sleep State The S0 sleep state is when everything is on. This is the state that no sleep is enabled.

S1 Sleep State The S1 sleep state is a low wake-up latency sleep state. In this state, no system context is lost (Processor or chip set). The system context is maintained by the hardware.

S4 Sleep State The S4 Non-Volatile Sleep state (NVS) is a special global system state that allows system context to be saved and restored (relatively slowly) when power is lost to the baseboard. If the system has been commanded to enter the S4 sleep state, the operating system will write the system context to a non-volatile storage file and leave appropriate context markers.

S5 Sleep State The S5 sleep state is similar to the S4 sleep state except the operating system does not save any context nor enable any devices to wake the system. The system is in the “soft” off state and requires a complete boot when awakened.

8.1.1 Front Panel Switches

The Intel® Server Board SE7501WV2 supports up to four front panel buttons (via any of three different front panel interface connectors):

- Power button/ sleep button
- Reset button
- System identification button
- NMI button

The power button input (FP_PWR_BTN*) on the Intel® Server Board SE7501WV2 design is a request that is forwarded by the BMC to the power state functions in the National* PC87417

Super I/O chip. The power button state is monitored by the BMC. It does not directly control power on the power supply.

The power button input (FP_SLP_BTN*) will behave differently depending on whether or not the operating system supports ACPI. The sleep switch has no effect unless an operating system with ACPI support is running. If the operating system supports ACPI and the system is running, pressing the sleep switch causes an event. The operating system will cause the system to transition to the appropriate system state depending on the user settings.

Power/Sleep Button Off to On: The ICH3-S and SIO may be configured to generate wakeup events for several different system events: Wake on LAN*, PCI Power Management Interrupt, and Real Time Clock Alarm are examples of these events. The BMC monitors the power button and wakeup event signals from the ICH3-S. A transition from either source results in the BMC starting the power-up sequence. Since the processors are not executing, the BIOS does not participate in this sequence. The ICH3-S receives power good and reset from the BMC and then transitions to an ON state.

Power/Sleep Button On to Off (Legacy): The BMC monitors power state signals from the ICH-3 and de-asserts the PS_PWR_ON signal to the power supply. As a safety mechanism, the BMC automatically powers off the system in 4-5 seconds.

Power/Sleep Button On to Off (ACPI): If an ACPI operating system is loaded, the power button switch generates a request (via SCI) to the operating system to shutdown the system. The operating system retains control of the system and determines what sleep state (if any) the system transitions to.

Power/Sleep Button On to Sleep (ACPI): If an ACPI operating system is loaded, the sleep button switch generates a request (via SCI) to the operating system to place the system in “sleep” mode. The operating system retains control of the system and determines into which sleep state, if any, the system transitions.

Power/Sleep Button Sleep to On (ACPI): If an ACPI operating system is loaded, the sleep button switch generates a wake event to the ICH3-S and a request (via SCI) to the operating system to place the system in the “On” state. The operating system retains control of the system and determines from which sleep state, if any, the system can wake.

Reset Button: The reset button will generate a hard reset to the system.

NMI Button: The NMI button will force an NMI to the BMC, which will generate an NMI to the processor.

System ID Button: The System ID button is used to aid a technician in locating a system for servicing when installed in a rack environment. Pushing the ID button will light the blue ID light located on the back edge of the baseboard near the speaker and battery. It will also light an LED on a front panel if configured to do so.

8.1.2 Wake up Sources (ACPI and Legacy)

The Intel® Server Board SE7501WV2 is capable of wake up from several sources under a non-ACPI configuration, e.g., when the operating system does not support ACPI. The wake up sources are defined in the following table. Under ACPI, the operating system programs the ICH3-S and SIO to wake up on the desired event, but in legacy mode, the BIOS enables/disables wake up sources based on an option in BIOS Setup. It is required that the operating system or a driver clear any pending wake up status bits in the associated hardware (such as the Wake on LAN status bit in the LAN application specific integrated circuit (ASIC), or PCI power management event (PME) status bit in a PCI device). The legacy wake up feature is disabled by default.

Table 84. Supported Wake Events

Wake Event	Supported via ACPI (by sleep state)	Supported Via Legacy Wake
Power Button	Always wakes system	Always wakes system
Ring indicate from Serial A	S1, S4, S5	Yes
Ring indicate from Serial B	S1, S4, S5	Yes
PME from PCI 32/33	S1, S4, S5	Yes
PME from PCI secondary 64/33	S1, S4, S5	No
PME from primary PCI 64/66	S1, S4, S5	Yes
BMC source (i.e. EMP)	Simulated as power button	Simulated as power button
RTC Alarm	S1, S4, S5	Yes
Mouse	S1	No
Keyboard	S1	No
USB	No	No

9. Front Panel IO (FPIO) System Board

This chapter describes the basic functions and interface requirements of the Front Panel IO (FPIO) system board that is designed for the Intel® Telco/Industrial Grade ServerTIGPR2U.

9.1 Features

- Four switches to control power-on, reset, NMI, and the system ID LED
- One system ID LED that can be controlled remotely or by the system ID switch
- Two system activity LEDs that indicate power-on and NIC activity
- Two hard drive activity/fault LEDS that indicate activity/fault status for drives 0 and 1
- Four system fault LEDs that indicate critical, major, minor, and power system fault status
- Four system fault relays for external critical, major, minor, and power fault indicators
- One SCSI bus with hot-swap circuitry for controlling hot-swap SCSI disk drives 0 and 1
- IDE Bus from IDE Connector to blind mate connector
- Floppy Bus from Floppy Connector to blind mate connector
- One blind mate connector for interfacing to CDROM or Floppy drive carrier assembly
- Connectors for interfacing to the power supply, Intel® Server Board SE7501WV2, drive carrier assemblies, and hot plug disk drives 1 and 2.

9.2 Chapter Structure and Outline

The information contained in this chapter is organized into eight sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 9.3: Introduction
Provides an overview of the Intel® Telco/Industrial Grade Server TIGPR2U FPIO board, showing primary components and their relationships, and physical board layout diagrams.

Section 9.4: Functional Description of Front Panel Switches, LEDs, and Relays
Provides a functional description of the front panel switches, LEDs, and relays contained on the FPIO board.

Section 9.5: RJ-45 COM2 Port and USB Ports
Provides functional descriptions of the RJ-45 COM2 port and USB ports.

Section 9.6: Connector Information
Provides information on all connectors contained on the FPIO board. Gives signal descriptions and the corresponding electrical parameters for each input and output of a given connector.

Section 9.7: IDE and Floppy Bus
Provides information on the interconnection of the SE7501WV2 System Baseboard IDE bus and floppy bus to the CDROM or Floppy drive carrier assemblies through the blind mate connector on the FPIO board.

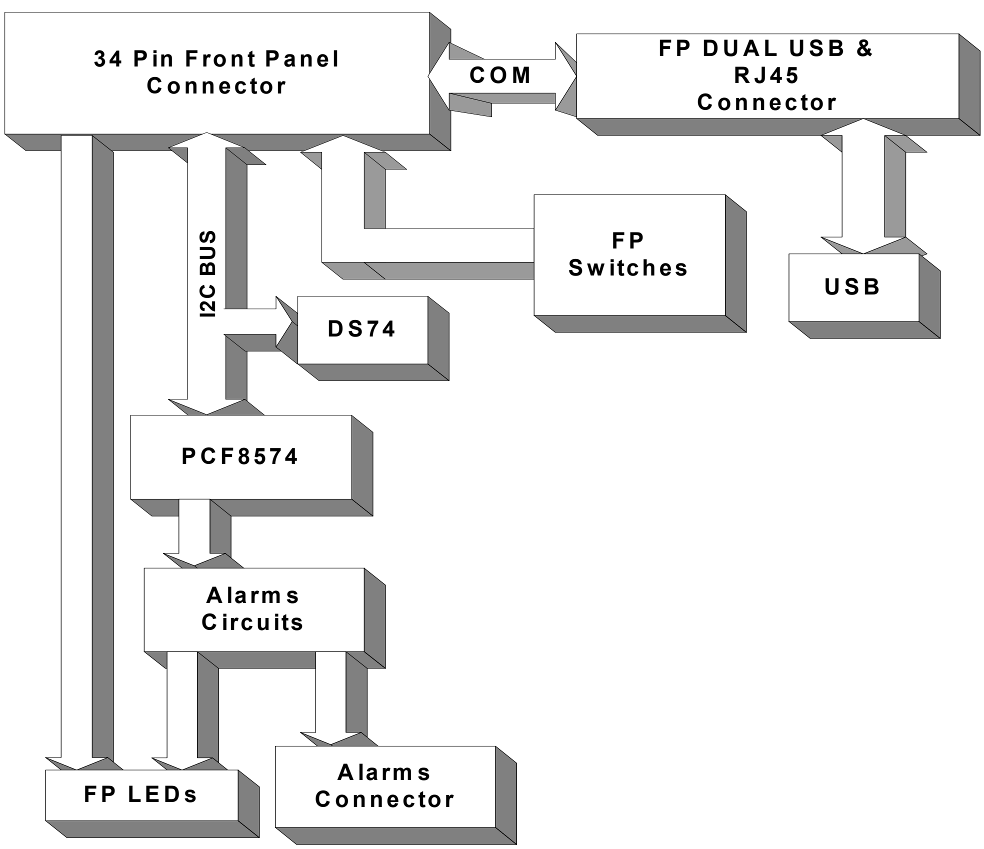
Section 9.8: SCSI Subsystem
Provides information on the SCSI subsystem on the FPIO board. The SCSI subsystem is designed to give the end user support for two SCSI hot-plug hard drives. The design enables easy use and replacement of the SCSI hard drives without powering down the system.

Section 9.9: Specifications
Describes the electrical, environmental and mechanical specifications.

9.3 Introduction

The FPIO system board provides the means of mounting and electrically connecting switches and indicators for system operation and status. These features are accessible and visible from the front of the chassis. In addition, it contains the blind-mate connector for interfacing to either the CDROM drive carrier assembly or the Floppy drive carrier assembly. It also contains the SCSI bus and hot-plug control circuitry necessary for the hot-plug SCSI disk drives. An alarms function is also provided. The FPIO system board is designed for use with SSI compliant telecom SE7501WV2 Server Baseboards.

9.4 Functional Description of Front Panel Switches, LEDs, and Relays



9.4.1 Front Panel Switches

The front panel has a power switch, a reset switch, an NMI switch, and a system ID switch. The function of these switches is described in the following table.

Table 85. Front Panel Switch Description

Switch	Function
Power Switch	A momentary switch, APCI compliant, used to toggle system power on/off.
Reset Switch	A momentary switch used to reset the system when it is in the power-on state.
NMI Switch	A momentary switch used to instruct the processor to copy system memory to hard disk
System ID Switch	A momentary switch used to instruct the processor to toggle the state of the system ID LED

9.4.2 Front Panel LEDs

Table 86. LED Specifications

LED Function	LED Color	Peak Wavelength (nm)	Luminous Intensity Typ(mcd)	Luminous Intensity Min(mcd)
ID	White	N/A	8.9	4.5
	Blue	470	1.1	0.5
	Red	640	8.6	4.3
	Green	525	2.0	1.0
NIC	Green	560	4.3	1.7
ON	Green	560	4.3	1.7
DRV 1/0 Activity	Green	568	6.8	4.5
DRV 1/0 Fault	Red	625	7.9	4.0
DRV 1/0 Fault	Yellow	597	10.4	6.0
CRT	Red	627	8.9	3.0
	Yellow	590	11.4	4.5
MJR	Red	627	8.9	3.0
	Yellow	590	11.4	4.5
MNR	Yellow	580	3.3	1.6
PWR	Yellow	580	3.3	1.6

9.4.3 System Status LEDs

There are five FPIO system board system status LEDs. The function of these system status LEDs is described in the following table.

Table 87. Front Panel System Status LED Description

Status LED	Function
Power	The green *Power LED* indicates that system power is on when it is illuminated continuously. When it is blinking green, it indicates that the system is in ACPI sleep mode.
NIC1/NIC2	The green *NIC activity LED* indicates network link presence and activity on either NIC1 or NIC2

System ID	The white or blue *NIC activity LED* is used to identify a particular system. The LED can be toggled remotely or with the System ID Switch
Disk 0	The *green/amber/red hard drive 1 activity/fault LED* displays activity or fault status for hard disk drive 1
Disk 1	The *green/amber/red hard drive 2 activity/fault LED* displays activity or fault status for hard disk drive 2

9.4.4 System Fault LEDs

There are four front panel system fault LEDs. The function of these system fault LEDs is described in the following table.

Table 88. Front Panel System Fault LED Description

Fault LED	Function
Critical	This amber or red LED alarm is illuminated via SMBUS bus and may only be turned off via SMBUS control. When continuously lit, it indicates the presence of a Critical System Fault. A critical system fault is an error or event that is detected by the system with a fatal impact to the system. In this case, the system cannot continue to operate. An example could be the loss of a large section of memory, or other corruption, that renders the system not operational. The front panel critical alarm relay will be engaged.
Major	This amber or red major alarm is illuminated via SMBUS bus and may be turned off via SMBUS control or alarm connector reset. When continuously lit, it indicates the presence of a Major System Fault. A major system fault is an error or event that is detected by the system that has discernable impact to system operation. In this case, the system can continue to operate, but in a “degraded” fashion (reduced performance or loss of non-fatal feature reduction). An example could be the loss of one of two mirrored disks. The front panel major alarm relay will be engaged.
Minor	This amber LED minor alarm is illuminated via SMBUS bus and may be turned off via SMBUS control or alarm connector reset. When continuously lit, it indicates the presence of a Minor System Fault. A minor system fault is an error or event that is detected by the system but has little impact to actual system operation. An example would be a correctable ECC error. The front panel minor alarm relay will be engaged.
Power	The amber power alarm is illuminated via SMBUS bus or SYS_FLT_LED_L signal and may only be turned off via SMBUS control. When continuously lit, it indicates the presence of a Power System Fault. The front panel power alarm relay will be engaged.

9.4.5 LED Color Selection

Colors of the ID, disk fault, major alarm and critical alarm are configurable using 2 position 0.1-inch shunts/jumpers on header J7D1(see the following table). The ID LED may be configured as blue or white. A white ID LED needs shunts across pins 3-4 and 5-6.

Table 89. LED Color Selection

Shunt	Pins	ON	OFF
ID Blue	1-2	N/C	Blue
ID Green	3-4	Green	off
ID Red	5-6	Red	off
Critical Alarm	7-8	Red	Yellow

Shunt	Pins	ON	OFF
Disk 0 Fault	9-10	Yellow	Red
Disk 1 Fault	11-12	Yellow	Red
spare	13-14		
spare	15-16		

9.4.6 System Fault Relays

The front panel board contains four relays. These relays are for power, critical, major and minor alarms. The relays are controlled by the SMBUS. See Section 9.4.7 for programming information. Section 9.6.4 describes the relay outputs.

9.4.7 I^2C Interfaces

This section describes the programming of front panel board.

A PFC8574 remote 8-bit I/O expander on the private I^2C bus controls the front panel alarms. All signals are active low. All outputs power up high (inactive). The PFC8574 I^2C address is 40 hex (write) and 41 hex (read). On system reset, all ones should be written to PFC8574 since the part doesn't have a reset input pin.

Table 90. Front Panel Board I^2C Interface Input/Output Bit Description

Bit	I/O	Name	Description
0	O	Power alarm	Writing 0 turns on the power alarm relay and illuminates the POWER LED, writing 1 turns both off. The relay and LED may also be turned on by a FAN_FAIL_L signal.
1	O	Critical alarm	Writing 0 turns on the critical alarm relay and illuminates the CRITICAL LED, writing 1 turns both off.
2	O	Major alarm	Writing a 1 to 0 edge will turn on the flip-flip that enables major alarm relay. Writing a 1 will turn off the major alarm relay or a MAJOR_RESET signal input. MAJOR LED in on when output is 0, off when output is 1. [1]
3	O	Minor alarm	Writing a 1 to 0 edge will turn on the flip-flip that enables major alarm relay. Writing a 1 will turn off the major alarm relay or a MINOR_RESET signal input. MINOR LED in on when output is 0, off when output is 1. [1]
4	I	Major alarm sense	Senses the state of the major alarm relay. 0 relay is on, 1 relay is off. This allows software to detect if the MAJOR_RESET signal was activated. Always write 1 during write operations.
5	I	Minor alarm sense	Senses the state of the minor alarm relay. 0 relay is on, 1 relay is off. This allows software to detect if the MINOR_RESET signal was activated. Always write 1 during write operations.
6	I	Critical/Major color	Writing a 1 turns CRITICAL and MAJOR LEDs to yellow, writing 0 color is RED. Strapping J7D1 pins 7-8 forces LEDs to RED. Resets to yellow.
7	I	Not used	Reserved for future use, always write 1 during write operations.

[1] Normally closed (NC) and normally open (NO) relay contacts are provided on the rear panel Telco alarms connector. To activate the relay, a 1 to 0 transition must be written.

1.1.1.1 Temperature sensor

The front panel I^2C bus has a DS75 temperature sensor at address 92 hex (write) and 93 hex (read). The sensor is located just to the left of the switch looking at the front of the unit.

9.5 RJ-45 COM2 Port and USB Ports

9.5.1 RJ-45 COM2 RS-232 Port

The FPIO Board has provision for an RS-232C port using an RJ-45 connector. This is available for use at the front of the chassis. Grounding EMP_INUSE_L disables the rear COM2 port and enables the front port.

Table 91. RJ-45 (RS232-C) Pin-out

Pin #	I/O	Signal Name	Description
1	O	SPB_EMP_RTS_L	Request To Send
2	O	SPB_EMP_DTR_L	Data Terminal Ready
3	O	SPB_EMP_SOUT	Serial Out
4	PWR	GND	GND
5	I	EMP_INUSE_L	In Use
6	I	SPB_EMP_SIN	Serial In
7	I	SPB_EMP_DSR_L	Data Set Ready
8	I	SPB_EMP_CTS_L	Clear To Send

9.5.2 Dual USB ports

The FPIO Board has provision for USB 1.1 for use at the front of the chassis. A dual vertical stacked connector is used for connections.

Table 92. USB Connector Pin-out

Pin #	I/O	Signal Name	Description
A1	PWR	VREG_FP_USBPWR	USB_PWR_3
A2	I/O	USB_DM3_FP	USB_BCK2_L
A3	I/O	USB_DP3_FP	USB_BCK2
A4	GND	VSS (GND)	VSS (GND)
B1	PWR	VREG_FP_USBPWR	USB_PWR_2
B2	I/O	USB_DM4_FP	USB_BCK3_L
B3	I/O	USB_DP4_FP	USB_BCK3
B4	GND	VSS (GND)	VSS (GND)

9.6 Connector Information

The following table shows all the connectors on the FPIO system board, the interconnect used for each connector, and the destination for the interconnect. In addition, the first column references the location of the connector location on the following figure.

Table 93. FPIO System Board Connector Information

FPIO Board Connections				
Loc	**Ref Des**	**Function**	**Interconnect**	**Connects to**
A	J5A1	2x20 IDE Connector	IDE Cable	Baseboard IDE Connector
B	J2A1	68 Pin Blind Mate receptacle	CDFDD I/F	CDROM or Floppy Carrier
C	J7A1	2x10 System Fan Cntrl conn	Fan Cntrl Cbl	Baseboard Fan Connectors
D	J5B1	68 pin SCSI Connector	SCSI BB Cbl	Baseboard SCSI Connector
E	J6A1	2x8 Alarms Connector	Alarms Cable	System Chassis Back
F	J1A1	2x3 P/S Power Connector	P/S harness	Power Supply Assembly
G	J9A1	1x3 System Fan 1 Conn	Fan 1 harness	Fan 1
H	J8A3	1x3 System Fan 2 Conn	Fan 2 harness	Fan 2
I	J8A2	1x3 System Fan 3 Conn	Fan 3 harness	Fan 3
J	J8A1	1x3 System Fan 4 Conn	Fan 4 harness	Fan 4
K	J9D1	80 pin SCA Connector	SCSI Flex 1	SCSI Disk Drive 1
L	J5D1	80 pin SCA Connector	SCSI Flex 2	SCSI Disk Drive 2
M	J3A1	2x5 USB Connector	USB Cable	Baseboard USB Connector
N	J1C1	2x17 Floppy Conn	Floppy Cable	Baseboard Floppy Connector
O	J4A1	2x17 Front Panel conn 2mm	FP Cable	Baseboard Front Panel Connector
P	J9D2	RJ45 COM2/Dual USB conn	N/C	
Q	J9A2	1x4 IPMB I2C Connector	IPMB Cable	Baseboard IPMB I2C Connector

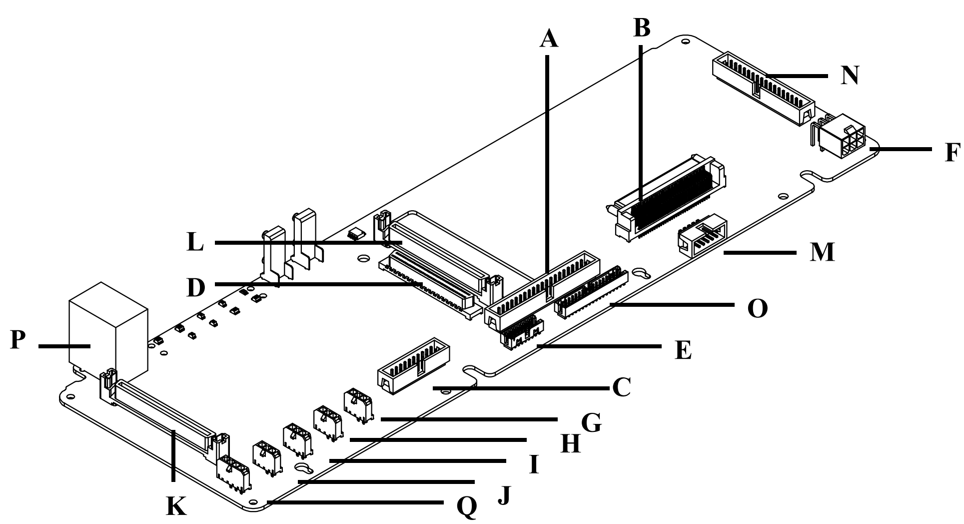


Figure 39. FPIO Connector Location

Table 94. Connector Housing information

Conn	Function	Intel PN	AML	s/k/l/p[1]	cnt	hsn
FPIO Board C13071-200						
J5A1	IDE 2x20	201418-954	Foxconn* HL16207-D2	y/y/y/y	15u"	94V0
J2A1	B/M 68p	C14315-001	Molex* 87537-6811	na-bb	30u"	94V0
J7A1	Fan 2x10	201418-956	Foxconn* HL16107-D2	y/y/y/y	15u"	94V0
J5B1	SCSI 68	628525-169	FXN* QA01343-P4S	y/y/**n**/y	15u"	94V0
J6A1	Alrm 2x8	744983-006	Foxconn* HL54087-L7	y/y/y/y	15u"	94V0
J1A1	Pwr 2x3	626997-006	Molex* 39-30-0060	y/y/y/y	T/L	94V0
J9A1 J8A3 J8A2 J8A1	Fan 1x3	C13083-002	Molex* 43650-0317 Tyco* 1445093-3	y/y/y/y y/y/y/y	30u" 30u"	94V0 94V0
J5D1 J9D1	SCSI 80	626530-381	AMP* 787311-1	y/y/**n**/y	30u"	94V0
J3A1	USB 2x5	201418-957	Foxconn* HL15057-P9	y/y/y/y	15u"	94V0
J1C1	Flp 2x17	201418-955	Foxconn* HL16177-P4	y/y/y/y	15u"	94V0
J4A1	FP 2x17	744983-005	Foxconn* HL54177-D3	y/y/y/y	15u"	94V0
J9D2	USB/com	680356-003	FXN* UB11123-L40	**na**	30u"	94V0
J9A2	I2C 1x4	C13083-004	Molex* 43650-0417	y/y/y/y	30u"	94V0

1. **s/k/l/p -** shrouded/keyed/latching/polarized

The IDE, SCSI, USB, and Floppy connector pin-outs are industry standard and will not be given in this document. The 2x3 power connector pin-out is shown in the power supply section of this document and will not be shown here. The 2x34 pin blindmate, the 2x10 fan, the 2x8 alarm, the 1x3 fan, and the 2x17 front panel connector pin-outs are shown in the following tables.

9.6.1 FPIO Board Front Panel Connector Pinout

The following table details the pin-out of the front panel connector to the Intel® Server Board SE7501WV2.

Table 95. 34-pin Front Panel J4A1 Connector

Pin	Front Panel Signal	Pin	Front Panel Signal
1	GND	2	FP_SYS_FLT_LED_L
3	PWR_LED_ON_L	4	NC
5	NC	6	+5V_STDBY
7	HDD_LED_ACT_L	8	UID_L
9	FP_PWR_BTN_L	10	NC
11	NC	12	PRI_NIC_LED_L
13	FP_RST_BTN_L	14	I2C_SDA
15	GND	16	I2C_SCL
17	FP_ID_BTN_L	18	NC
19	GND	20	NC
21	Keying Pin	22	NC
23	FP_NMI_BTN_L	24	SEC_NIC_LED_L
25	EMP_DSR_L	26	EMP_INUSE_L
27	EMP_SIN	28	EMP_SOUT
29	EMP_RTS_L	30	EMP_CTS_L

Pin	Front Panel Signal	Pin	Front Panel Signal
31	EMP_DTR_L	32	EMP_DCD_L
33	NC	34	NC

9.6.2 Fan 1x3 Connector Pin-out

The four fans all have the same wire harness, and the connector pin-out is shown in the following table.

Table 96. Fan 1x3 Connector

Pin	Signal
1	GND
2	Fan Speed Control
3	Fan Tachometer Signal

9.6.3 Fan 2x10 Connector Pin-out

One cable brings the fan speed control voltage to the FPIO board from the baseboard, and returns the fan tachometer signal from the FPIO board to the baseboard. This fan 2x10 connector pin-out is shown in the following table.

Table 97. Fan 2x10 Connector

Pin	Fan Signal	Pin	Fan Signal
1	+5V_STB_FAN	2	FAN_LED_1
3	FAN_LED_2	4	FAN_LED_3
5	FAN_LED_4	6	TP
7	GND	8	GND
9	GND	10	FAN_SPD1
11	FAN_SPD2	12	FAN_SPD3
13	FAN_SPD4	14	FAN_TACH1
15	FAN_TACH2	16	FAN_TACH3
17	FAN_TACH4	18	NC
19	NC	20	NC

9.6.4 Alarms Port Pin-out

The alarms port interface is a standard DB15-pin connector. Each alarm (major, minor, critical and power) is the output of a STDT relay contacts. A common contact with normally open and normally closed connections is included. Power alarm has only common and normally open contact outputs. The major and minor alarms contain external reset circuits.

Table 98. Alarms Connector

Pin	Signal
1	Minor reset positive
2	Minor reset negative
3	Major reset positive
4	Major reset negative
5	Critical alarm normally open

Pin	Signal
6	Critical alarm normally closed
7	Critical alarm common
8	Minor alarm normally open
9	Minor alarm normally closed
10	Minor alarm common
11	Major alarm normally open
12	Major alarm normally closed
13	Major alarm common
14	Power alarm normally open
15	Power alarm common

9.6.5 FPIO Board Blind Mate 2x34 Connector Pin-out

The following table details the pin-out of the 2x34 blind mate connector that is used to interface to the CDROM or Floppy drive carrier assembly.

Table 99. 2x34 Blind Mate Connector

Pin	Blind Mate Signal	Pin	Blind Mate Signal
1	FD_INDEX_L	35	+5V
2	FD_DS_L	36	+5V
3	FD_DSKCHG_L	37	+5V
4	GND	38	FD_RDY_L
5	FD_MTR_L	39	GND
6	FD_WDATA_L	40	FD_DIR_L
7	FD_WGATE_L	41	FD_STEP_L
8	GND	42	FD_WPD_L
9	FD_TRK0_L	43	GND
10	FD_RDATA_L	44	FD_DENSEL0_L
11	FD_HDSEL_L	45	FD_DENSEL1_L
12	GND	46	BM_SPARE
13	IDE_RST_L	47	GND
14	IDE_PDD7	48	IDE_PDD8
15	IDE_PDD6	49	IDE_PDD9
16	GND	50	IDE_PDD10
17	IDE_PDD5	51	GND
18	IDE_PDD4	52	IDE_PDD11
19	IDE_PDD3	53	IDE_PDD12
20	GND	54	IDE_PDD13
21	IDE_PDD2	55	GND
22	IDE_PDD1	56	IDE_PDD14
23	IDE_PDD0	57	IDE_PDD15
24	GND	58	GND
25	IDE_PDDREQ	59	IDE_CSEL_P
26	GND	60	IDE_PDIOR_L
27	IDE_PDIOW_L	61	GND
28	GND	62	IDE_PIORDY

Pin	Blind Mate Signal	Pin	Blind Mate Signal
29	IDE_PIRQ_P	63	GND
30	IDE_PDA1	64	IDE_PDDACK_L
31	IDE_PDA0	65	IDE_CBL_DET
32	GND	66	IDE_PDA2
33	IDE_PDCS0_L	67	GND
34	IDE_PRI_HD_ACL_L	68	IDE_PDCS1_L

9.7 IDE and Floppy Bus

There is an IDE connector and a Floppy connector on the FPIO system board for interfacing to the IDE bus and the Floppy bus on the Intel® Server Board SE7501WV2. The IDE bus and the Floppy bus on the FPIO system board are routed from these connectors to the 2x34 blindmate connector for interfacing to either the CDROM drive carrier assembly or the Floppy drive carrier assembly. Pin definitions for the 2x34 blindmate connector are shown in the preceding table. The IDE bus is ULTRA DMA mode two (DMA33) capable.

9.8 SCSI Subsystem

The SCSI subsystem on the FPIO board is designed to give the end user support for two SCSI hot-plug hard drives. The design enables easy use and replacement of the SCSI hard drives without powering down the system. The following block diagram and functional description will give a general idea of how the FPIO SCSI subsystem works.

9.8.1 FPIO Board SCSI Subsystem Block Diagram

The block diagram in the following figure illustrates the general architecture of the FPIO SCSI subsystem. The physical and functional blocks of the FPIO SCSI subsystem are shown, with arrows representing buses and signals, and the blocks representing the functional parts of the SCSI subsystem.

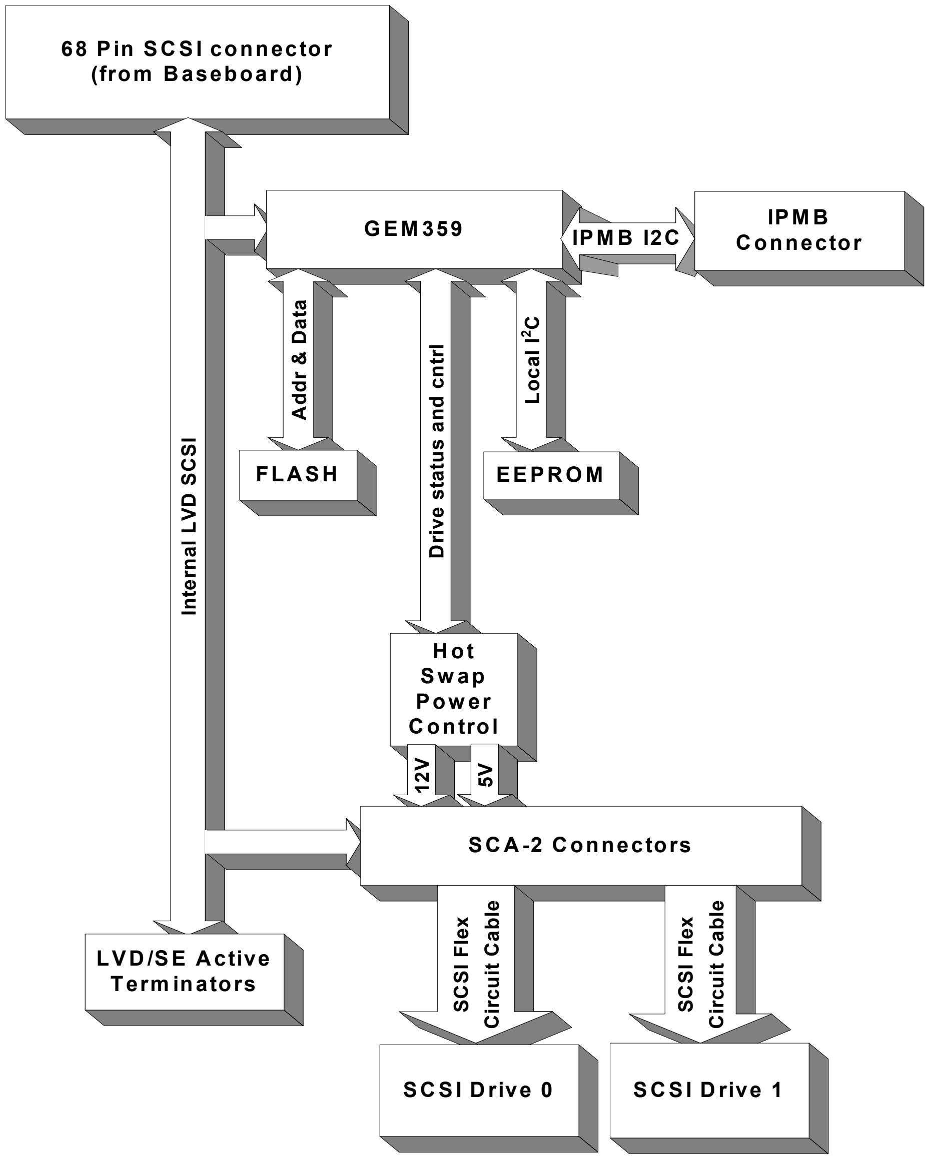


Figure 40. FPIO Board SCSI Subsystem Block Diagram

9.8.2 SCSI Bus

The FPIO SCSI subsystem passes the SCSI bus from the Intel® Server Board SE7501WV2 to the internal SCSI drives. The SCSI bus is Ultra 320 (SPI-4) capable. SE drives are not supported. SE drives should not be installed as the behavior of the drives is unpredictable and data corruption could result. The bus is comprised of 68 signals. The bus clock is 80 MHz. The 320 Mbytes data rate results from double transition (DT) data transfers on a two byte wide bus. The SCSI bus attaches to the Intel® Server Board SE7501WV2 via a 68-pin SCSI connector.

320 Mbytes/s = 2 byte bus * 80 MHz clock * double transitions.

NOTE: The SCSI drives and SCSI controller on the Intel® Server Board SE7501WV2 determine actual SCSI bus data rate.

9.8.3 FPIO SCSI Drive Power Control

SCSI Power Control is provided by the FPIO SCSI subsystem. SCSI Power Control includes SCSI drive power switching, over-current protection, system status notification, and SCSI drive status LEDS.

If a SCSI drive is detected, the system will be notified. Then the system will instruct the FPIO SCSI subsystem to apply power to the internal SCSI drive. Status LEDs will provide the user with visual indicators for the internal SCSI drive.

Once the system is powered up, the user can request the system to remove power to a SCSI drive. The system will instruct the FPIO SCSI subsystem to remove power from the internal SCSI drive. The user can then safely remove the internal SCSI drive. Upon reinserting an internal SCSI drive, the user must notify the system. The system will then instruct the FPIO SCSI subsystem to apply power to the specified drive.

9.8.4 Internal SCSI Drive Power Switching

Each SCSI drive is supplied with +12 V and +5 V. Separate MOSFET switches apply and remove the +12 V and +5 V to each internal SCSI drive.

9.8.5 Initial Soft Power-on

When power is first applied to a SCSI drive there is a large initial current surge (up to 20 Amps). At turn-on, the gate of each external N-Channel MOSFET is charged with a 10υA current source. Capacitors on each gate create a programmable ramp (soft turn-on) to control inrush currents.

9.8.6 Over-current Protection

If either of the drive's power rails exceeds 5 amps, the MOSFET switch for the problematic rail will be turned off. Removing power will protect the MOSFET and system from damage in the event of a short on one of the power rails. After one third of a second, the MOSFET will be turned on to see if the short has been removed. Turning on and checking for a short every one third of a second will continue until the system instructs the FPIO SCSI subsystem to remove power or the fault disappears.

When the MOSFET is first enabled, the over-current condition is not detected for the first 640 nS period. This no OCP period allows the initial current surge produced by many SCSI drives. The 640 nS period is short enough to not allow damage to occur to the MOSFETS or the system.

9.8.7 Power Control Inter-lock

The Power Control Inter-lock prevents drives from powering on at the same time. Since only one drive can power on at once the board power requirements can be kept lower. After one drive starts the next drive will start one third of a second later.

9.8.8 System Status Notification

Internal SCSI drive status information is collected by the micro-controller. The micro-controller passes the information to the Server Management via the global I^2C bus and Enclosure Management via the SCSI bus.

9.8.9 FPIO SCSI Subsystem Status LEDs

The status LEDs give the user a visual indication of the drives' condition. There is a single LED for each drive. The LEDs are bi-colored and use a combination of color and blinking frequency to indicate multiple conditions. The LEDs are mounted on the FPIO board, and the light is directed to the front panel through the use of a light pipe assembly. See the following table for LED activity definitions. See Firmware EPS for definitions of the different blink rates.

Table 100. LED Activity Definitions

LED State	Drive Active	Fault Condition
Solid or Blinking Green	X	
Solid or Blinking Yellow		X
Solid or Blinking Red		X

9.8.10 FPIO SCSI Subsystem Enclosure Management

SCSI Enclosure Management allows the FPIO SCSI subsystem to report on SCSI drive status via the SCSI bus. Normally a RAID controller will interface with Enclosure Management. The SCSI Enclosure Management subsystem consists of a Qlogic* GEM359 controller, Flash, and PLD (Programmable Logic Device). Refer to Figure 40 when reading the following subsystem descriptions.

9.8.10.1 Qlogic* GEM359 Enclosure Management Controller

The GEM359 sends acquired board information to the SCSI bus and IPMB bus. The GEM359 also acts on requests from both the SCSI bus and IPMB bus. GEM359 GPIOs send LED and drive power control. Please see the Qlogic* GEM359 firmware EPS for further information.

9.8.10.2 4 Meg Flash

The GEM359 code is stored in a 4 Meg FLASH (512K x 8). The FLASH boot block is stored in the top block. The boot block is normally protected. Non-protected FLASH can be updated via the IPMB bus.

9.8.11 Server Management Interface

The FPIO SCSI subsystem will support the following Server Management features:

Local I^{2}C Interface

- SCSI subsystem Field Replaceable Unit (FRU)
- Micro-controller interface

System I^{2}C Interface

- Micro-controller IPMB interface

9.8.11.1 Local I^2C Bus

The local I^2C bus has an Atmel* AT24C02N (or equivalent) serial EEPROM to the micro-controller.

9.8.11.2 Global I^2C Bus (IPMB)

The global I^2C bus connects the micro-controller to the system. The micro-controller is isolated from the system until the system PWRGRD signal is asserted.

9.8.11.3 I^2C Addresses

Two I^2C devices and their addresses are listed in the following two tables. Two I^2C devices can be addressed on or through the FPIO SCSI subsystem:

- Hot Swap Micro Controller
- FPIO SCSI subsystem FRU EEPROM

Table 101. I^2C Local Bus Addresses

Device	Address	Bus/Location	Description
AT24C02	0xA0	Legacy I^2C/ SCSI backplane	Private SCSI backplane FRU EEPROM

Table 102. I^2C Global Bus Addresses (IPMB Bus)

Device	Address	Bus/Location	Description
GEM359	0x10-0x1F	Legacy I^2C/ SCSI backplane	Micro controller public IPMB bus

9.8.12 Power Good Circuit

Power Good circuits are positive logic signals reflecting the status of various power rails.

9.8.12.1 Power Good Outputs

On board Power Good circuits monitor both the 12-V and 5-V rails. When the +5-V rail is within +/-5% of +5 V, the 5-volt Power Good signal is asserted. When the 12-V signal is greater than 12 V –5%, the 12-volt Power Good signal is asserted. Both detection circuits have built in hysteresis to prevent chatter. The 5-V and 12-V Power Good signals are ANDed together (via the PLD) to generate the SCSI_V_GOOD output signal.

9.8.12.2 Power Good Inputs

The Power Good input tells the FPIO SCSI subsystem that the system power supply is powered up and working within specifications.

9.8.13 Reset Control

The Reset signal resets the GEM micro-controller only on power up.

9.8.14 SCA2 Connector Interlocks

The SCA2 connectors on the FPIO SCSI subsystem have interlocks. Interlock is used by the FPIO SCSI subsystem to determine if a SCSI device is present. Drive presence is used by enclosure management.

9.8.15 Clock Generation

A single 10MHz clock on the FPIO supplies clock input to the GEM359.

9.8.16 Programmable Devices

There are two programmable devices on the FPIO SCSI subsystem. These will be described in the next three sections.

9.8.16.1 FLASH

Flash contains program code to be run by the onboard micro-controller.

Memory configuration: 512 K x 8

9.8.16.2 Field Replaceable Unit (FRU)

The FRU is programmed at ATE.

Memory Configuration: 2 k serial

9.8.17 Signal Descriptions

The following notations are used to describe the signal type, from the perspective of the FPIO SCSI subsystem:

I	Input pin to the SCSI subsystem
O	Output pin from the SCSI subsystem
I/O	Bi-directional (input/output) pin
PWR	Power Supply pin

The signal description also includes the type of buffer used for the particular signal:

LVD	Low Voltage Differential SCSI
SE	Standard Single Ended SCSI
TTL	5V TTL signals
CMOS	5V CMOS signals
3.3V CMOS	3.3V CMOS signals
Analog	Typically a voltage reference or specialty power supply

9.8.17.1 LVD SCSI Connectors

The LVD connector carries signals between the FPIO SCSI bus and internal SCSI drives through the SCSI flex circuit cables. The LVD SCSI bus signals are driven by either the baseboard SCSI controller, the LVD/SE Transceiver, or the internal SCSI drives. The following table provides a description of each signal on the SCSI connectors.

Table 103. LVD SCSI Bus Signals – J9D1, J5D1, J5B1

Signal	Type	Driver	Name and Description
DB_[15..0][P, N]	I/O	LVD/ SE	**SCSI Data Bus.** These pins, with the DBP[1/0][P/N] pins form the bi-directional SCSI data bus.
DB_P0[P, N] DB_P1[P, N]	I/O	LVD/ SE	**SCSI Data Parity.** These pins support parity on the SCSI bus. DBP0[P/N] supports parity for data [7..0] DBP1[P/N] supports parity for data [15..8]
DIFFSENSE	I	Analog	**Differential Sense.** This pin monitors the DIFFSENSE signal from the terminator. The voltage level determines the operating mode of the target devices on the SCSI bus. If the voltage on the DIFFSENSE signal is from –0.35 V to +0.5 V the mode will be SE. If it is from +0.7 V to 1.9 V the mode will be LVD.
ATN_[P, N]	I/O	LVD/ SE	**SCSI Bus Attention.** These pins are asserted by a SCSI device in initiator mode to alert the target that the initiator has a message to transfer.
BSY_[P, N]	I/O	LVD/ SE	**SCSI Bus Busy.** In SE mode, these pins are bi-directional and are asserted to gain use of the SCSI bus and to indicate that that SCSI bus is in use.
ACK_[P, N]	I/O	LVD/ SE	**SCSI Bus Acknowledge.** These pins are asserted by a SCSI device in initiator mode to acknowledge the target's request for a data transfer.
RST_[P, N]	I/O	LVD/ SE	**SCSI Bus Reset.** In SE mode, these pins are bi-directional and are asserted when all the SCSI devices attached to the SCSI bus need to be reset.
MSG_[P, N]	I/O	LVD/ SE	**SCSI Bus Message Phase.** These pins are asserted by a SCSI device in target mode to indicate the Message In or Message Out phase.
SEL_[P, N]	I/O	LVD/ SE	**SCSI Bus Select.** In SE mode, these pins are bi-directional and are asserted by the controller when attempting to select or reselect a SCSI device.
CD_[P, N]	I/O	LVD/ SE	**SCSI Bus Control/Data Phase.** These pins are asserted or de-asserted by a SCSI device in target mode to indicate that control or data information is being transferred over the SCSI bus
REQ_[P, N]	I/O	LVD/ SE	**SCSI Bus Request.** These pins are asserted by a SCSI device in target mode to indicate that the target is requesting a data transfer over the SCSI bus.
IO_[P, N]	I/O	LVD/ SE	**SCSI Bus I/O Phase.** These pins are asserted by a SCSI device in target mode to indicate the direction of data movement on the SCSI bus between the target and the initiator.
SCSI_ID	O	GND/OPEN	**SCSI ID.** Sets internal SCSI ID depending on slot. Drive 0 has SCSI address 0. Drive 1 has SCSI address 1.
MATED [1,2]	I/O	TTL	**SCSI MATED.** Pins are used to determine if SCSI is present and has proper contact. See T10/1302D Annex C for additional information.
GND	I/O	PWR	**Ground. These pins provide Secondary Ground reference.**
P12V	O	PWR	**+12-V supply.** Max 1 amp of continuous current. Max 6 amps peak current.
P5V	O	PWR	**+5-V supply.** Max 1.4 amps of continuous current. Max 6 amps peak current.

9.8.18 Internal Logic Signals

The following table presents a summary of the signals that route between logic that is contained in the FPIO SCSI subsystem.

Table 104. Internal Logic Signals

	Signal	Type	Driver	Name and Description
Clks	CLK_20MHZ	O	CMOS	**20-MHz Clock.** This signal is the 20-MHz clock used by the GEM359 and PLD.
Qlogic* GEM359 Logic Control	ADDR<16..0>	O	CMOS	**Address/Bus.** These pins are used as address bus for the FLASH.
	PROM_VPP_L	O	CMOS	**FLASH PROGRAM VOLTAGE ENABLE.** This pin is driven by the SCSI backplane GEM359 to enable the Flash to be programmed.
	PROM_OE_L	O	CMOS	**FLASH Output Enable.** This pin is driven by the SCSI backplane GEM359 to enable the Flash for writing data on the bus.
	PROM_WE_L	I	CMOS	**FLASH Chip Enable.** This pin is driven by the SCSI backplane GEM359 to enable the Flash to be written to.
Misc. Logic	5V_RST_N	O	TTL	**5-V reset.** This signal is driven by micro controller reset chip. Output is asserted low for 150 ms after +5 V returns to an in-tolerance condition (+/- 5%).
	POWER_GD	O	TTL	**Power Good.** Asserted high when 5-V supply is with in tolerance and system power good is asserted.

9.9 Specifications

9.9.1 Electrical Specifications

DC specifications for the Telco/Industrial Grade Server INTEL® TELCO/INDUSTRIAL GRADE SERVER TIGPR2U front panel board power connectors are summarized in this section excluding disk drive power. All power rails must operate within +/- 5% voltage range.

Table 105. Maximum Power Requirements (mA)

12V	5V	3.3V	+5V_STBY
20(mA)	186(mA)	384(mA)	184(mA)

Maximum current on +5V_STBY with all LEDs illuminated and relays energized is 320 mA. The typical current with no LEDs illuminated or relay energized is 150 mA.

Note: Software limits 2 alarms active at once: power fault and one of the major, minor or critical alarms.

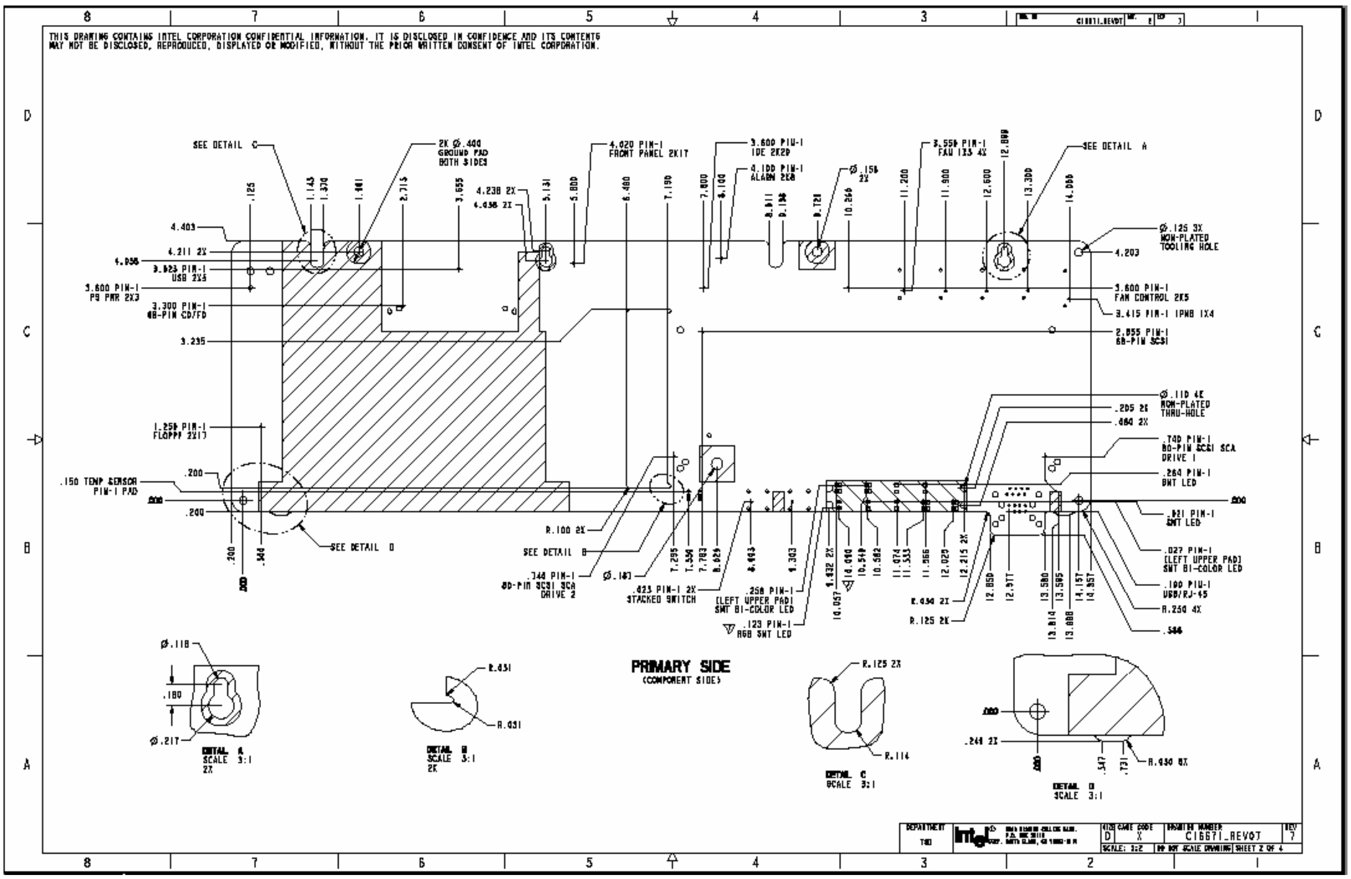
Alarms connector relay contacts are rated at 1 A with a maximum rating of 30 W(DC) / 60 VA (AC).

Alarms connector external alarm (major and/or minor) reset is an optoisolated input that is reverse voltage protected. A voltage of 3.3 V to 48 V input with a pulse width of at least 200 ms is required to activate the alarm-reset function. Maximum current is 12 mA.

9.9.2 Mechanical Specifications

The following figure shows the mechanical specifications of the Intel® Telco/Industrial Grade Server TIGPR2U front panel board. All dimensions are given in inches.

Figure 41. FPIO Board Mechanical Specifications



10. Interconnect System Board

This chapter describes the basic functions and interface requirements of the interface system board that is designed for the Intel® Telco/Industrial Grade Server TIGPR2U.

10.1 Features

- Used in CDROM drive carrier assembly and Floppy drive carrier assembly
- Blind-mate connector for connection to FPIO system board
- IDE connector and power connector for interfacing with the CDROM Drive
- Floppy FFC connector for interfacing to the Floppy Drive
- No active components on board

10.2 Chapter Structure and Outline

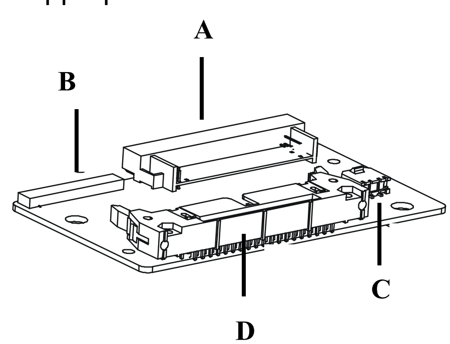
The information contained in this chapter is organized into four sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 10.3: Functional Description of Interface Board
Provides an overview of the TIGPR2U FPIO board and a physical board layout diagram.

Section 10.4: Connector Descriptions
Provides connector descriptions for all connectors on the interface board.

10.3 Functional Description of Interface Board

The interface board is used in both the CDROM drive carrier assembly and the Floppy drive carrier assembly as the signal and power interface between the CDROM/Floppy drive and the FPIO system board. The interface board has standard IDE, Floppy, and power connectors for interfacing to the CDROM or Floppy drive, and has a high-density blind-mate connector for interfacing to the FPIO system board. These connectors are identified in the following figure. All IDE bus signals, floppy bus signals, and +5V and GND are routed from the FPIO board through the blind mate connector to the appropriate connector on the interface board.



A. Blind Mate Connector
B. Floppy FFC connector
C. CDROM Power Connector
D. CDROM IDE Connector

Figure 42. Description of Interface Board

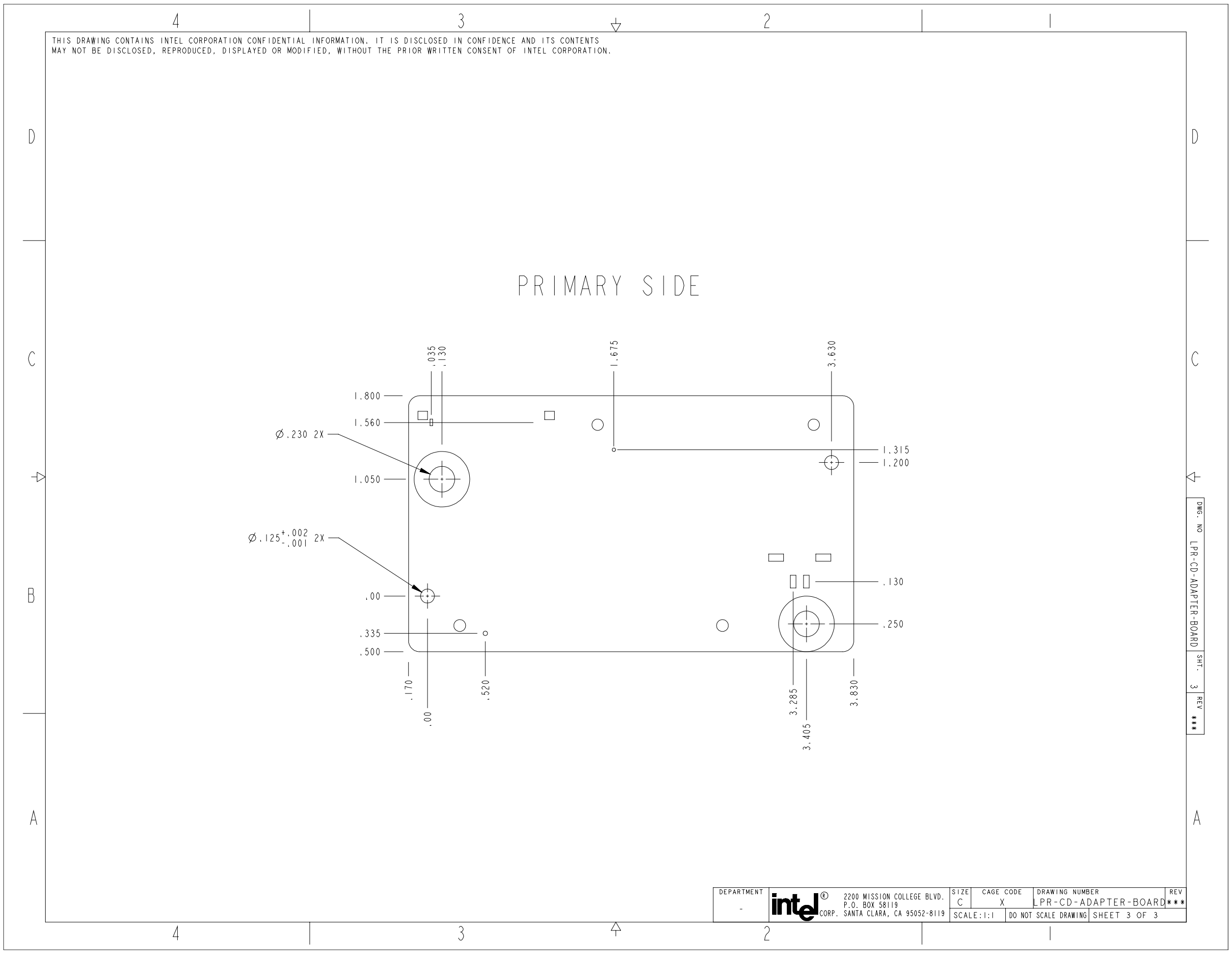


Figure 43. Dimensions of Interface Board

10.4 Connector Descriptions

10.4.1 Interface Board Blind Mate 2x34 Connector Pinout

The following table details the pin-out of the 2x34 blind mate connector that is used to interface to the FPIO Board.

Table 106. 2x34 Blind Mate Connector

Pin	Blind Mate Signal	Pin	Blind Mate Signal
1	FD_INDEX_L	35	+5V
2	FD_DS_L	36	+5V
3	FD_DSKCHG_L	37	+5V
4	GND	38	FD_RDY_L
5	FD_MTR_L	39	GND
6	FD_WDATA_L	40	FD_DIR_L
7	FD_WGATE_L	41	FD_STEP_L
8	GND	42	FD_WPD_L
9	FD_TRK0_L	43	GND

Pin	Blind Mate Signal	Pin	Blind Mate Signal
10	FD_RDATA_L	44	FD_DENSEL0_L
11	FD_HDSEL_L	45	FD_DENSEL1_L
12	GND	46	BM_SPARE
13	IDE_RST_L	47	GND
14	IDE_PDD7	48	IDE_PDD8
15	IDE_PDD6	49	IDE_PDD9
16	GND	50	IDE_PDD10
17	IDE_PDD5	51	GND
18	IDE_PDD4	52	IDE_PDD11
19	IDE_PDD3	53	IDE_PDD12
20	GND	54	IDE_PDD13
21	IDE_PDD2	55	GND
22	IDE_PDD1	56	IDE_PDD14
23	IDE_PDD0	57	IDE_PDD15
24	GND	58	GND
25	IDE_PDDREQ	59	IDE_CSEL_P
26	GND	60	IDE_PDIOR_L
27	IDE_PDIOW_L	61	GND
28	GND	62	IDE_PIORDY
29	IDE_PIRQ_P	63	GND
30	IDE_PDA1	64	IDE_PDDACK_L
31	IDE_PDA0	65	IDE_CBL_DET
32	GND	66	IDE_PDA2
33	IDE_PDCS0_L	67	GND
34	IDE_PRI_HD_ACL_L	68	IDE_PDCS1_L

10.4.2 Interface Board CDROM 1x2 Power Connector Pinout

The following table details the pin-out of the 1x2 power connector that is used to interface to the CDROM interface board.

Table 107. 1x2 CDROM Power Connector

Pin	Power Signal	Pin	Power Signal
1	GND	2	+5V

10.4.3 Interface Board CDROM 2x20 IDE Connector Pinout

The following table details the pin-out of the CDROM 2x20 IDE connector that is used to interface IDE signals to the CDROM drive interface board.

Table 108. 2x20 IDE Connector Pinout

Pin	IDE Signal	Pin	IDE Signal
1	IDE_RST_L	2	GND
3	IDE_DD7	4	IDE_DD8
5	IDE_DD6	6	IDE_DD9
7	IDE_DD5	8	IDE_DD10

Pin	IDE Signal	Pin	IDE Signal
9	IDE_DD4	10	IDE_DD11
11	IDE_DD3	12	IDE_DD12
13	IDE_DD2	14	IDE_DD13
15	IDE_DD1	16	IDE_DD14
17	IDE_DD0	18	IDE_DD15
19	GND	20	KEY – Pin Pulled
21	IDE_PDDREQ	22	GND
23	IDE_PDIOW_L	24	GND
25	IDE_PDIOR_L	26	GND
27	IDE_PIORDY	28	GND
29	IDE_PDDACK_L	30	GND
31	IDE_PIRQ_L	32	TP
33	IDE_PDA1	34	IDE_CBL_DET_P
35	IDE_PDA0	36	IDE_PDA2
37	IDE_PDCS0_L	38	IDE_PDCS1_L
39	IDE_DASP_L	40	GND

10.4.4 Interface Board Floppy 1x26 FFC Connector Pinout

The following table details the pin-out of the Floppy 1x26 FFC connector that is used to interface to the FFC connector on the Floppy drive.

Table 109. 2x20 IDE Connector Pin-out

Pin	Floppy Signal
1	+5V
2	FD_INDEX_L
3	+5V
4	FD_DS_L
5	+5V
6	FD_DSKCHG_L
7	TP
8	FD_RDY_L
9	FD_DENOUT_L
10	FD_MTR_L
11	TP
12	FD_DIR_L
13	FD_DENSEL0_L
14	FD_STEP_L
15	TP
16	FD_WDATA_L
17	GND
18	FD_WGATE_L
19	GND
20	FD_TRK_L

Pin	Floppy Signal
21	GND
22	FD_WPD_L
23	GND
24	FD_RDATA_L
25	GND
26	FD_HDSEL_L

10.5 CD-ROM Connectors

The ½" slim-line CD-ROM uses a 50-pin JAE signal/power interface connector. The pin-out is listed in the following table.

Table 110. CD-ROM JAE Signal/Power Connector Pin-out

Pin	Signal	Signal	Pin
1	Audio L-Ch	Audio R-Ch	2
3	Audio GND	GND	4
5	RESET-	DD8	6
7	DD7	DD9	8
9	DD6	DD10	10
11	DD5	DD11	12
13	DD4	DD12	14
15	DD3	DD13	16
17	DD2	DD14	18
19	DD1	DD15	20
21	DD0	DMARQ	22
23	GND	/DIOR	24
25	DIOW-	GND	26
27	IORDY	/DMACK	28
29	INTRQ	/IOCS16	30
31	DA1	/PDIAG	32
33	DA0	DA2	34
35	/CS1FX	/CS3FX	36
37	/DASP	+5V	38
39	+5V	+5V	40
41	+5V	+5V	42
43	GND	GND	44
45	GND	GND	46
47	CSEL	GND	48
49	RESERV	RESERV	50

A small interface board is connected to the 50-pin JAE signal/power interface connector on the CD-ROM. This small interface board has three connectors: (1) the mating 50-pin JAE signal/power interface connector to the one on the CD-ROM drive, (2) a 2x20 IDE connector for interfacing via a standard IDE cable to the 2x20 IDE connector contained on the interconnect board, and (3) a 1x2 power connector for interfacing via a two-wire power cable to the 1x2 power connector on the interconnect board.

10.6 Floppy Drive Connectors

The ½” slim-line floppy drive uses a 26-pin FFC signal/power interface connector. The pin-out for this connector is shown in the following table.

Table 111. 26-Position Floppy FFC Signal/Power Connection

Pin #	Signal	Signal	Pin #
1	+5V	INDEX	2
3	+5V	DRIVE SELECT	4
5	+5V	DISK CHANGE	6
7	NC	READY	8
9	HD OUT (HD AT HIGHT LEVEL)	MOTOR ON	10
11	NC	DIRECT SELECT	12
13	NC	STEP	14
15	GND	WRITE DATA	16
17	GND	WRITE GATE	18
19	GND	TRACK 00	20
21	NC	WRITE PROTECT	22
23	GND	READ DATA	24
25	GND	SIDE ONE SELECT	26

11. 5-V Riser Board

This chapter describes the design and external interface of the Intel® Telco/Industrial Grade Server TIGPR2U 5-V riser board. Features of the 5-V riser board include:

- Three 33-MHz 5-V 64-bit PCI slots
- 5 V to 3.3 V signal level translation

11.1 Chapter Structure and Outline

The information contained in this chapter is organized into four sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 11.2: Introduction:
Provides an overview of the Intel® Telco/Industrial Grade Server TIGPR2U 5-V riser board, showing primary components and their relationships, and physical board layout diagrams.

Section 11.3: Functional Description:
Provides a functional description of the 5 V riser board.

Section 11.4: Connector Interface:
Gives signal descriptions and the corresponding electrical parameters for each input and output of a given connector.

Section 11.5: Electrical Specification:
Describes the electrical, environmental, and mechanical specifications.

11.2 Introduction

The riser card supports three 5-V 64-bit slots at 33 MHz. The board contains voltage level translation, converting the 5 V PCI cards signals to conform to the baseboard, which has 3.3-V signaling levels.

The following figure presents an illustration of the board.

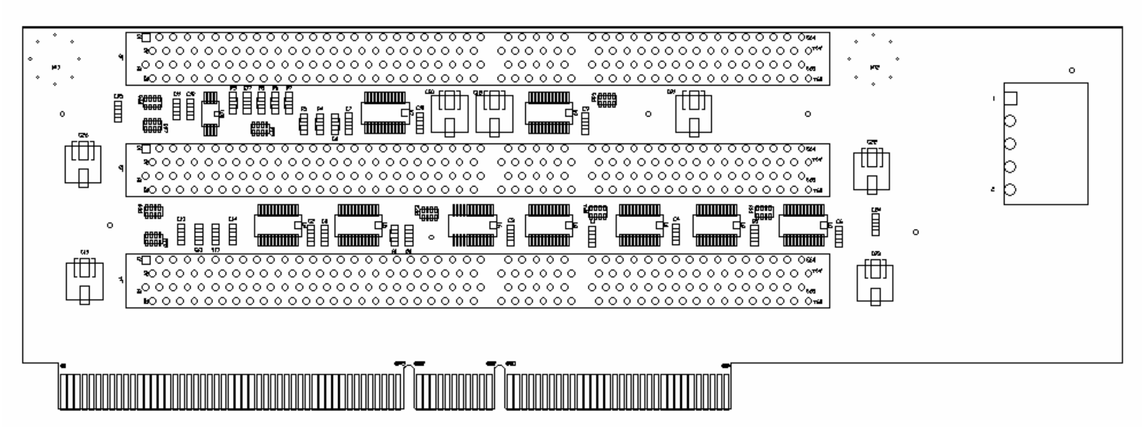


Figure 44. 5-V Riser Board Layout

11.3 Functional Description

The 5-V riser card has three 5-V 64-bit slots at 33 MHz. Voltage translation circuits convert the 5-V PCI signals to 3.3-V signal levels for use on the baseboard.

IDSELs are AD24 for slot 1, AD25 for slot 2 and AD26 for slot 3.

11.4 Connector Interface

The following table describes the common signals between the edge fingers and each of the slots.

Table 112. Riser Card Slot Pin-out Common Signals

Pin	Side B	Side A	Pin	Side B	Side A
1	-12V	**Error! Reference source not found.**	49	M66EN	AD[09]
2	**Error! Reference source not found.**	+12V	50	Connector Key	Connector Key
3	Ground	**Error! Reference source not found.**	51	Connector Key	Connector Key
4	**Error! Reference source not found.**	**Error! Reference source not found.**	52	AD[08]	C/BE[0]#
5	+5V	+5V	53	AD[07]	+3.3V
6	+5V	**Error! Reference source not found.**	54	+3.3V	AD[06]
7	**Error! Reference**	**Error! Reference**	55	AD[05]	AD[04]

Pin	Side B	Side A	Pin	Side B	Side A
	source not found.	**source not found.**			
8	**Error! Reference source not found.**	+5V	56	AD[03]	Ground
9	**Error! Reference source not found.**	NC	57	Ground	AD[02]
10	**Error! Reference source not found.**	+5V (I/O)	58	AD[01]	AD[00]
11	**Error! Reference source not found.**	NC	59	+5V (I/O)	+5V (I/O)
12	Ground	Ground	60	ACK64#	REQ64#
13	Ground	Ground	61	+5V	+5V
14	NC	3.3VAUX	62	+5V	+5V
15	Ground	RST#		Connector Key	Connector Key
16	**Error! Reference source not found.**	+5V (I/O)		Connector Key	Connector Key
17	Ground	**Error! Reference source not found.**	63	Clock Slot2	Ground
18	**Error! Reference source not found.**	Ground	64	Ground	C/BE[7]#
19	+5V (I/O)	PME#	65	C/BE[6]#	C/BE[5]#
20	AD[31]	AD[30]	66	C/BE[4]#	+5V (I/O)
21	AD[29]	+3.3V	67	Ground	PAR64
22	Ground	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Ground
24	AD[25]	Ground	70	+5V (I/O)	AD[60]
25	+3.3V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]#	**Error! Reference source not found.**	72	AD[57]	Ground
27	AD[23]	+3.3V	73	Ground	AD[56]
28	Ground	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	+5V (I/O)
30	AD[19]	Ground	76	Ground	AD[52]
31	+3.3V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Ground
33	C/BE[2]#	+3.3V	79	+5V (I/O)	AD[48]

Pin	Side B	Side A	Pin	Side B	Side A
34	Ground	FRAME#	80	AD[47]	AD[46]
35	IRDY#	Ground	81	AD[45]	Ground
36	+3.3V	TRDY#	82	Ground	AD[44]
37	DEVSEL#	Ground	83	AD[43]	AD[42]
38	Ground	STOP#	84	AD[41]	+5V (I/O)
39	LOCK#	+3.3V	85	Ground	AD[40]
40	PERR#	SMBUS SCL	86	AD[39]	AD[38]
41	+3.3V	SMBUS SDA	87	AD[37]	Ground
42	SERR#	Ground	88	+5V (I/O)	AD[36]
43	+3.3V	PAR	89	AD[35]	AD[34]
44	C/BE[1]#	AD[15]	90	AD[33]	Ground
45	AD[14]	+3.3V	91	Ground	AD[32]
46	Ground	AD[13]	92	NC	NC
47	AD[12]	AD[11]	93	NC	Ground
48	AD[10]	Ground	94	Ground	NC

The following table describes each of the pins with unique signals.

Table 113. Riser Card Slot Pin-out Unique Signals

PIN	Edge Finger	SLOT 1	SLOT 2	SLOT 3
B2	INTDX_L	S1_TCK	S2_TCK	S3_TCK
B4	IINTCX_L	NC	NC	NC
B7	INTB_L	INTB_L	INTCX_L	INTDX_L
B8	INTD_L	INTD_L	INTA_L	INTB_L
B9	NC	S1_PRSNT1_L	S2_PRSNT1_L	S3_PRSNT1_L
B10	GNT_L<2>	NC	NC	NC
B11	NC	S1_PRSNT2_L	S2_PRSNT2_L	S3_PRSNT2_L
B14	REQ_L<2>	NC	NC	NC
B16	CLK_SLOT1	CLK__SLOT1	CLK_SLOT2	CLK_SLOT3
B18	REQ_L<1>	REQ_L<1>	REQ_L<2>	REQ_L<3>
B63	CLK_SLOT2	NC	NC	NC
B92	CLK_SLOT3	NC	NC	NC
A1	NC	S1_TRST_L	S2_TRST_L	S3_TRST_L
A3	NC	S1_TMS	S2_TMS	S3_TMS
A4	S1_TDI	S1_TDI	S2_TDI	S3_TDI
A6	INTA_L	INTA_L	INTB_L	INTDX_L
A7	INTC_L	INTC_L	INTCX_L	INTA_L
A9	REQ_L<3>	NC	NC	NC
A17	GNT_L<1>	GNT_L<1>	GNT_L<2>	GNT_L<3>
A26	NC	SLOT1_IDSEL	SLOT2_IDSEL	SLOT3_IDSEL

11.5 Electrical Specification

All PCI slots on the riser are limited to a maximum of 50 W total power for the installed cards. The maximum power per slot is 25 W. This maximum power per slot conforms to *PCI Specification 2.2*.

In systems equipped with DC power, an auxiliary connector is provided from the DC power supply cage to provide up to an additional 25 W of power to the 5V riser. Refer to Section 13.3.3.1.4, *P4 5V Riser Board Power Connector,* for more detail on the connector.

12. 3.3 V Riser Board

This chapter describes the design and external interface of the Intel® Telco/Industrial Grade Server TIGPR2U 3.3-V riser board. Features of the 3.3 V riser board include:

- Three 3.3-V 64-bit PCI slots

12.1 Chapter Structure and Outline

The information contained in this chapter is organized into four sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 12.2: Introduction:
Provides an overview of the Intel® Telco/Industrial Grade Server TIGPR2U 3.3-V riser board, showing primary components and their relationships, and physical board layout diagrams.

Section 12.3: Functional Description:
Provides a functional description of the 3.3-V riser board.

Section 12.4: Connector Interface:
Gives signal descriptions and the corresponding electrical parameters for each input and output of a given connector.

Section 12.5: Electrical Specification:
Describes the electrical, environmental and mechanical specifications.

12.2 Introduction

The 3.3-V riser card supports three 3.3-V 64-bit slots. The bus speed varies from 33MHz to 133MHz depending on the type of PCI adapters configured in the 3.3V riser card. This is described in the Intel® Server Board SE7501WV2 specification.

The following figure presents an illustration of the board.

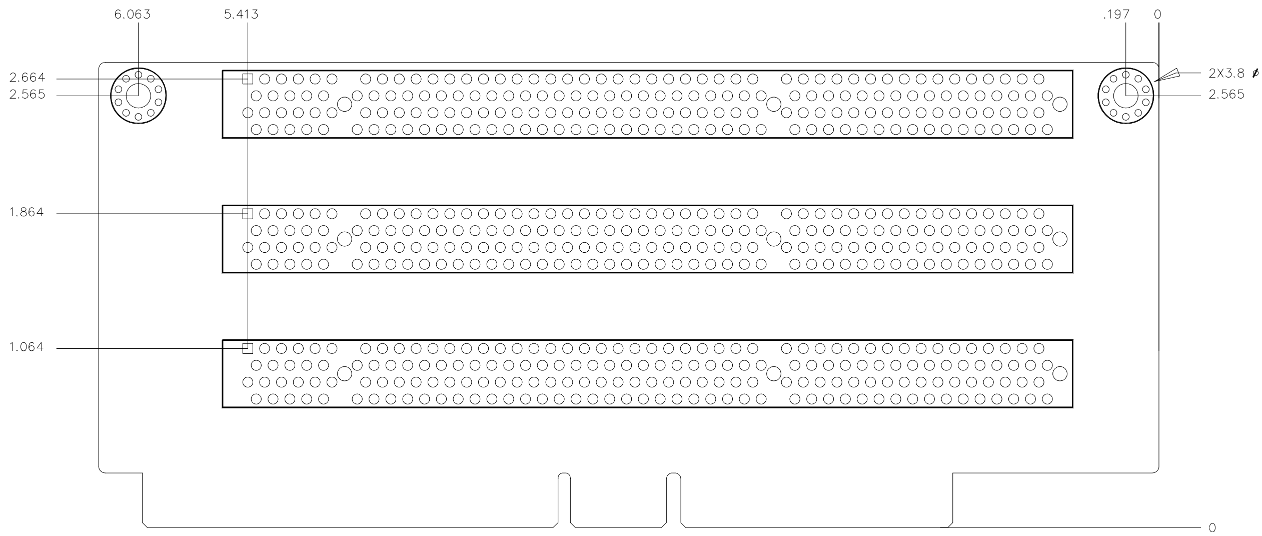


Figure 45. 3.3-V Riser Board Layout

12.3 Functional Description

The 3.3-V riser card has three 3.3-V 64-bit slots with a maximum bus speed of 133MHz.

IDSELs are AD24 for slot 1, AD25 for slot 2 and AD26 for slot 3.

12.4 Connector Interface

The following table describes the common signals between the edge fingers and each of the slots.

Table 114. Riser Card Slot Pin-out Common Signals

Pin	Side B	Side A	Pin	Side B	Side A
1	-12V	**Error! Reference source not found.**	49	M66EN	AD[09]
2	**Error! Reference source not found.**	+12V	50	**Error! Reference source not found.**	**Error! Reference source not found.**
3	Ground	**Error! Reference source not found.**	51	**Error! Reference source not found.**	**Error! Reference source not found.**
4	**Error! Reference source not found.**	**Error! Reference source not found.**	52	AD[08]	C/BE[0]#
5	+5V	+5V	53	AD[07]	+3.3V
6	+5V	**Error! Reference source not found.**	54	+3.3V	AD[06]

Pin	Side B	Side A	Pin	Side B	Side A
7	**Error! Reference source not found.**	**Error! Reference source not found.**	55	AD[05]	AD[04]
8	**Error! Reference source not found.**	+5V	56	AD[03]	Ground
9	**Error! Reference source not found.**	NC	57	Ground	AD[02]
10	**Error! Reference source not found.**	VIO	58	AD[01]	AD[00]
11	**Error! Reference source not found.**	NC	59	VIO	VIO
12	**Error! Reference source not found.**	**Error! Reference source not found.**	60	ACK64#	REQ64#
13	**Error! Reference source not found.**	**Error! Reference source not found.**	61	+5V	+5V
14	**Error! Reference source not found.**	3.3VAUX	62	+5V	+5V
15	Ground	RST#		Connector Key	Connector Key
16	**Error! Reference source not found.**	VIO		Connector Key	Connector Key
17	Ground	**Error! Reference source not found.**	63	Clock Slot2	Ground
18	**Error! Reference source not found.**	Ground	64	Ground	C/BE[7]#
19	VIO	PME#	65	C/BE[6]#	C/BE[5]#
20	AD[31]	AD[30]	66	C/BE[4]#	VIO
21	AD[29]	+3.3V	67	Ground	PAR64
22	Ground	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Ground
24	AD[25]	Ground	70	VIO	AD[60]
25	+3.3V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]#	**Error! Reference source not**	72	AD[57]	Ground

Pin	Side B	Side A	Pin	Side B	Side A
		found.			
27	AD[23]	+3.3V	73	Ground	AD[56]
28	Ground	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	VIO
30	AD[19]	Ground	76	Ground	AD[52]
31	+3.3V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Ground
33	C/BE[2]#	+3.3V	79	VIO	AD[48]
34	Ground	FRAME#	80	AD[47]	AD[46]
35	IRDY#	Ground	81	AD[45]	Ground
36	+3.3V	TRDY#	82	Ground	AD[44]
37	DEVSEL#	Ground	83	AD[43]	AD[42]
38	Ground	STOP#	84	AD[41]	VIO
39	LOCK#	+3.3V	85	Ground	AD[40]
40	PERR#	SMBUS SCL	86	AD[39]	AD[38]
41	+3.3V	SMBUS SDA	87	AD[37]	Ground
42	SERR#	Ground	88	VIO	AD[36]
43	+3.3V	PAR	89	AD[35]	AD[34]
44	C/BE[1]#	AD[15]	90	AD[33]	Ground
45	AD[14]	+3.3V	91	Ground	AD[32]
46	Ground	AD[13]	92	**Error! Reference source not found.**	NC
47	AD[12]	AD[11]	93	NC	Ground
48	AD[10]	Ground	94	Ground	**Error! Reference source not found.**

Note: VIOs are 5V on edge finger and 3.3V on all slots.

The following table describes each of the pins with unique signals.

Table 115. Riser Card Slot Pin-out Unique Signals

PIN	Edge Finger	SLOT 1	SLOT 2	SLOT 3
B2	SLOT_INTD_L	NC	NC	NC
B4	SLOT_INTC_L	NC	NC	NC
B7	INTB_L	INTB_L	SLOT_INTC_L	SLOT_INTD_L
B8	INTD_L	INTD_L	INTA_L	INTB_L
B9	S1_PRSNT1_L	S1_PRSNT1_L	S2_PRSNT1_L	S3_PRSNT1_L
B10	GNT_S3_L	NC	NC	NC
B11	S1_PRSNT2_L	S1_PRSNT2_L	S2_PRSNT2_L	S3_PRSNT2_L
B12	Ground	Connector Key	Connector Key	Connector Key
B13	Ground	Connector Key	Connector Key	Connector Key
B14	REQ_S3_L	NC	NC	NC

PIN	Edge Finger	SLOT 1	SLOT 2	SLOT 3
B16	CLK_66M_S1	CLK_66M_S1	CLK_66M_S2	CLK_66M_S3
B18	REQ_S1_L	REQ_S1_L	REQ_S2_L	REQ_S3_L
B50	Connector Key	Ground	Ground	Ground
B51	Connector Key	Ground	Ground	Ground
B63	CLK_SLOT2	NC	NC	NC
B92	CLK_SLOT3	NC	NC	NC
A1	EDGE_TRST_L	NC	NC	NC
A3	TMS	NC	NC	NC
A4	TDI	TDI	NC	NC
A6	INTA_L	INTA_L	INTB_L	SLOT_INTD_L
A7	INTC_L	INTC_L	SLOT_INTC_L	INTA_L
A9	REQ_S2_L	NC	NC	NC
A12	Ground	Connector Key	Connector Key	Connector Key
A13	Ground	Connector Key	Connector Key	Connector Key
A17	GNT_S1_L	GNT_S1_L	GNT_S2_L	GNT_S3_L
A26	IDSEL_S1	IDSEL_S1	IDSEL_S2	IDSEL_S3
A50	Connector Key	Ground	Ground	Ground
A51	Connector Key	Ground	Ground	Ground
A94	SLOT_ID	NC	NC	NC

12.5 Electrical Specification

All PCI slots on the riser are limited to a maximum of 50 W total power from the installed cards. The maximum power per slot is 25 W. This maximum power per slot conforms to *PCI Specification 2.2*.

13. DC Power Subsystem

This chapter defines the features and functionality of the DC-input switching power subsystem. The DC power subsystem will be NEBS hardened, so NEBS certification of the Intel® Telco/Industrial Grade Server TIGPR2U will be performed with a DC power subsystem configuration of the system.

13.1 Features

- 470 W output capability in full DC input voltage range
- Power good indication LEDs
- Predictive failure warning
- Internal cooling fans with multispeed capability
- Remote sense of 3.3-V and 5-Vdc outputs
- DC_OK circuitry for brown out protection and recovery
- Built-in load sharing capability
- Built-in overloading protection capability
- Onboard field replaceable unit (FRU) information
- I^2C interface for server management functions
- Integral handle for insertion/extraction

13.2 Chapter Structure and Outline

The information contained in this chapter is organized into two sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 13.3: DC-input Power Supply Cage
Provides an overview of the Intel® Telco/Industrial Grade Server TIGPR2U DC-input power supply cage.

Section 13.4: DC-input Power Supply Module
Provides an overview of the Intel® Telco/Industrial Grade Server TIGPR2U DC-input power supply module.

13.3 DC-input Power Supply Cage

13.3.1 DC-input Power Supply Cage Mechanical Specification

The DC-input chassis power supply cage can support up to two 470W TPS power supply modules in a 1+1 configuration or a non-redundant single module configuration. Each power supply module incorporates dual DC inputs with EMI filters.

A mechanical drawing for the power supply cage is shown in the following figure.

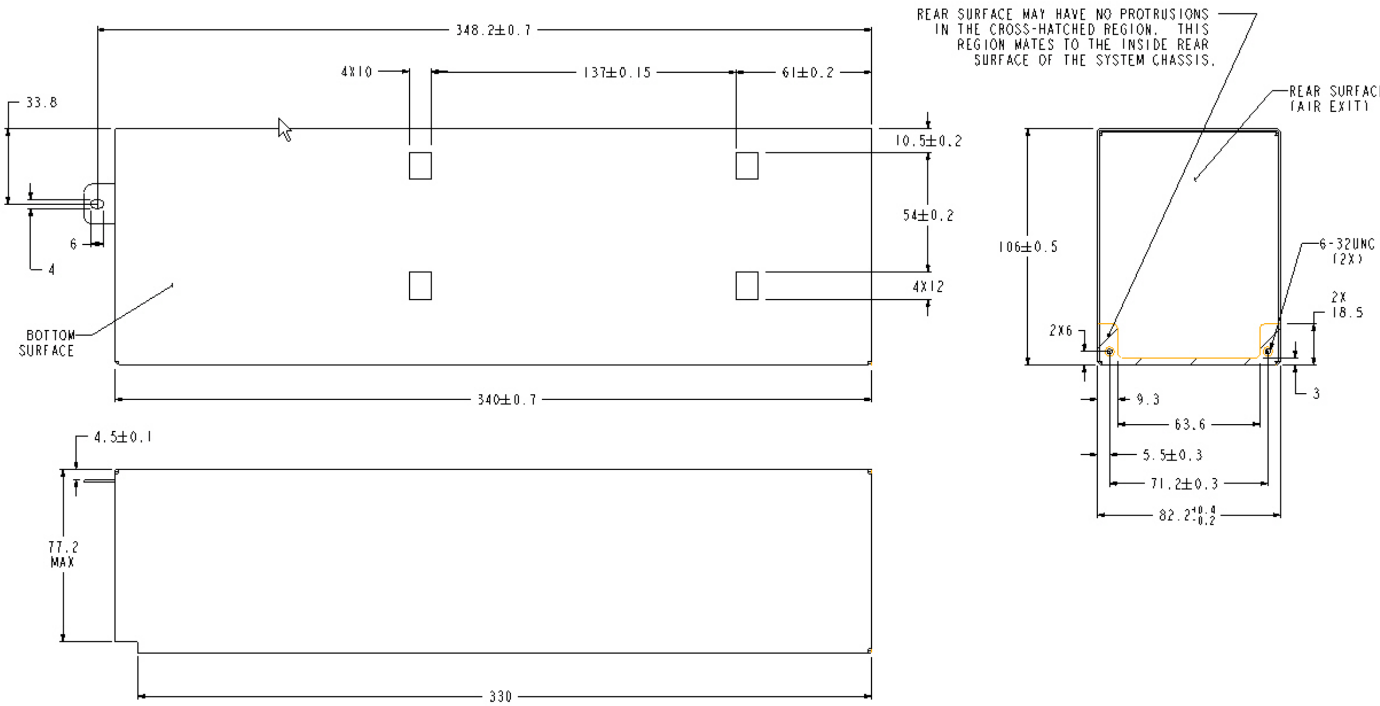


Figure 46. Power Supply Cage Mechanical Drawing

13.3.2 Power Supply Edge Connector Slot

See Section 13.4 for details.

13.3.3 Power Supply Cage Harness

The following figure shows the harness lengths and designators. The DC output harness connectors are UL1007 rated: 90°C, 300V or an Intel-approved equivalent. Each connector is described in detail in the following sections.

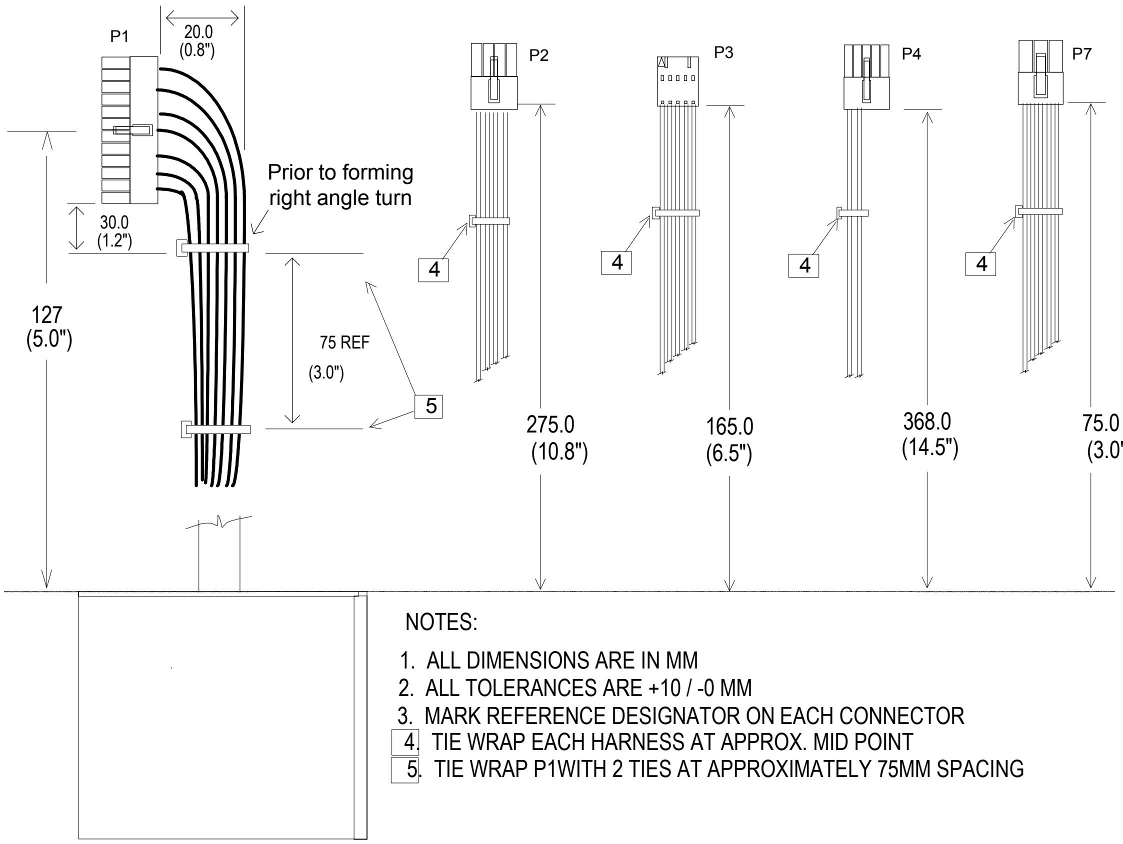


Figure 47. Power Supply Harness Detail

13.3.3.1.1 P1 Baseboard Connector

A 24-pin Molex* 39-01-2245 connector and harness from the power supply cage provides the Intel® Server Board SE7501WV2 with the required voltages and interface signals. The following table provides the connector pin-out.

Table 116. 24-pin Baseboard Power Connector Pin-out

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+3.3 V	Orange	13	+3.3V	Orange
2	+3.3 V	Orange	14	-12V	Blue
3	COM	Black	15	COM	Black
4	+5 V	Red	16	PS_ON#	Green
5	COM	Orange	17	COM	Black
6	+5 V	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray	20	Reserved	NC
9	5 VSB	Purple	21	+5V	Red
10	+12 V1	Yellow	22	+5V	Red
11	+12 V1	Yellow	23	+5V	Red

12	+3.3 V	Orange	24	COM	Black

13.3.3.1.2 P2 Processor Power Connector

An 8-pin Molex* 39-01-2080 connector and harness from the power supply cage provides the Intel® Server Board SE7501WV2 with the required +12V power required for the processors. The following table provides the connector pin-out.

Table 117. P2 Processor Power Connector Pin Assignments

PIN	SIGNAL	18 AWG COLOR	PIN	SIGNAL	18 AWG COLOR
1	COM	Black	5	+12 V3	Yellow/Black Stripe
2	COM	Black	6	+12 V3	Yellow/Black Stripe
3	COM	Black	7	+12 V3	Yellow/Black Stripe
4	COM	Black	8	+12 V3	Yellow/Black Stripe

13.3.3.1.3 P3 Power Management Signal Cable

A 5-wire cable with a Molex* 50-57-9705 female housing connector is used to direct power management signals to the Intel® Server Board SE7501WV2. The following table shows the pin-out.

Table 118. Power Management Signal Cable Pin-out

Pin	Signal	Description
1	I2C-SCL	Serial Clock.
2	I2C-SDA	Serial Data. Information from the power supply.
3	Alert#	Indicates power supply is operating beyond its limits and has failed or may fail soon.
4	COM	Return remote sense
5	3.3VS	3.3V sense

13.3.3.1.4 P4 5V PCI Riser Board Power Connector

A 2-wire cable with a Molex* 39-01-4051 connector attached is used to provide power to the 5-V PCI riser board.

Table 119. P4 5-V PCI Riser Power Supply Connector Pin Assignments

Pin	Signal	18 AWG COLOR
1	3.3V	No Connection
2	3.3V	No Connection
3	3.3V	No Connection
4	Ground	Black
5	5V	Red

13.3.3.1.5 P7 FPIO System Board Connector

A 6-wire cable with a Molex* Mini-Fit Jr. PN# 39-01-2065 connector is used to provide power to the FPIO system board for system logic power, peripheral drive power, and disk drive power.

Table 120. FPIO System Board Connector Pin-out

Pin	Signal	22 AWG COLOR
1	Ground	Black
2	Ground	Black
3	5V	Red
4	12V2	Yellow/Blue Stripe
5	12V2	Yellow/Blue Stripe
6	3.3V	Orange

13.3.3.2 Hot Swapping Power Modules

The DC-input power supply cage is capable of supporting hot swapping of power supply modules in a 1+1 configuration. Hot swapping a power supply module is the process of extracting and inserting a power supply module from an operating system.

13.3.4 Power Supply Cage Output Power/Currents

The combined output power of all outputs does not exceed 470W. Each output has a maximum and minimum current rating shown in the following table. Two DC-to-DC converters located in the cage provide the 3.3V and 5V rails. Total combined power for the 3.3V and 5V outputs does not exceed 150W. The power supply meets both static and dynamic voltage regulation requirements for the minimum dynamic loading conditions. The power supply meets only the static load voltage regulation requirements for the minimum static load conditions.

Table 121. Power Supply Cage Output Load Ratings

	+3.3V	+5V	+12V1	+12V2	+12V3	-12V	5VSB
MAX1	3	26	16(22-peak)*	7	0.5	0.5	2(2.5- peak)
MAX2	3	26	0.5	12(18-peak)	11	0.5	2(2.5- peak)
MAX3	3	26	0.5	11	12(18-peak)	0.5	2(2.5- peak)
MAX4	20	17	16(22-peak)*	7	0.5	0.5	2(2.5- peak)
MAX5	20	17	0.5	12(18-peak)	11	0.5	2(2.5- peak)
MAX6	20	17	0.5	11	12(18-peak)	0.5	2(2.5- peak)
MAX7	0.5	0.5	16(22-peak)*	12(18-peak)	9.5	0	0
MAX8	0.5	0.5	13.5	12(18-peak)	12(18-peak)	0	0
MIN DYNAMIC	1.0	2.0	1.5	1.5	1.5	0A	0A
MIN STATIC	0.5	0.5	0.5	1.5A	0.5	0A	0A

* For peak time duration refer to sec. 240VA protection.

13.4 DC-input Power Supply Module

The DC-input power system supports one 470W TPS module for a non-redundant configuration, or two in a 1+1 redundant configuration. The power supply module provides two outputs; 12V and 5V standby. Two DC-to-DC converters located in the cage provide the 3.3V and 5V rails from the 12V provided by the power supply module.

The power supply module contains two fans to provide cooling for the components in the module. The module provides a handle to assist in insertion and extraction and can be inserted and extracted without the assistance of tools.

Table 122. Power Supply Module Load Ratings

	+12V	+5VSB
MAX	39A	2.0A
MIN DYNAMIC	3.5A	0.1A
MIN STATIC	1.5A	0A

Table 123. Power Supply Module DC Input Rating

PARAMETER	MIN	RATED	MAX	Max Input Current
DC Voltage	-38 VDC	-48VDC/-60VDC	-75VDC	-17ADC

13.4.1 Power Supply Module Mechanical

The power supply module mechanical outline is shown in the following figure.

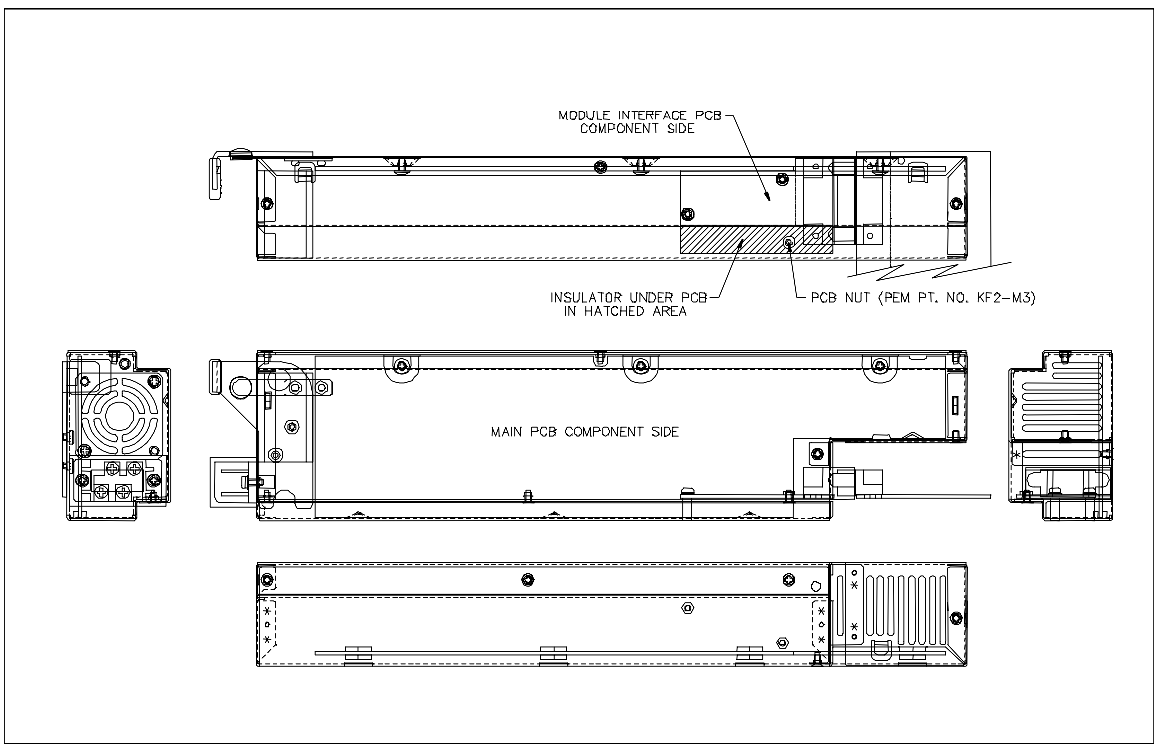


Figure 48. Outline Drawing of Power System Enclosure

13.4.2 Power Supply LED Indicator

A bi-color LED indicates power supply status. When DC is applied to the power supply and standby voltages are available, the LED blinks GREEN. The LED turns on solid GREEN to indicate that all the power outputs are available. The LED turns on solid AMBER to indicate a power supply failure, shutdown due to over-current, or shutdown due to over-temperature. Refer to the following table for conditions of the LED.

Table 124. LED Indicators

POWER SUPPLY CONDITION	Bi-Color LED
No DC power to all PSU	OFF
No DC power to this PSU only	AMBER
DC present / Only Standby Outputs On	BLINK GREEN
Power supply DC outputs ON and OK	GREEN
Power supply failure (includes over voltage, over current, 240VA protection, over temperature, fan failure)	AMBER

The LED is visible on the power supply's exterior face. The LED location meets ESD requirements. The LED is securely mounted in such a way that incidental pressure on the LED will not cause it to become displaced.

13.4.3 Thermal Protection

The power supply is protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an over-temperature protection (OTP) condition, the power supply will shutdown. When the power supply temperature drops to within specified limits, the power supply restores power automatically. The OTP circuit has built in hysteresis such that the power supply will not oscillate on and off due to a temperature recovery condition. The OTP trip level has a minimum of 4°C of ambient temperature hysteresis. The power supply alerts the system of the OTP condition via the power supply FAIL signal and the PWR LED.

13.4.4 Air Flow

The DC-input power supply module contains two 40mmx38mm fans to provide air flow for cooling. The cooling air enters the subsystem from the DC connector side, passing through the power supply module. The air flowing through the power supply module is pre-heated by the system. Inlet air to the power supply shall be in the range of 0° to 50°C.

13.4.5 DC Power Redundancy

The DC-input power system supports one 470W TPS module for a non-redundant configuration, or two modules for a 1 + 1 redundant configuration. Input power redundancy can only be obtained and supported with the use of two separate input modules. The input power modules may be wired to a single source or to two different sources for maximum redundancy.

The input power connector is a plug type terminal block that will accept standard terminal lugs, size Newark stock # 81N1501 type CRS-TO-1406-HT. These lugs accept 14 AWG wire gauge.

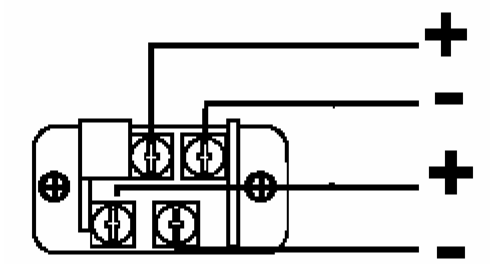


Figure 49. DC Power Input Connector

13.4.5.1 DC-Input Power Wiring

The DC-input connector has two sets of screw terminals. Both sets of terminals should be wired using 14AWG wire. Each terminal input should be fused with a maximum of 10A fuse.

14. AC Power Subsystem

This chapter defines the features and functionality of the AC-input switching power subsystem. The AC power supply will not be NEBS hardened, so NEBS certification of an Intel® Telco/Industrial Grade Server TIGPR2U configured with an AC power subsystem will not be possible.

14.1 Features

- 480-W output capability in full AC input voltage range
- Power good indication LEDs
- Predictive failure warning
- External cooling fans with multispeed capability
- Remote sense of 3.3-V and 5-Vdc outputs
- AC_OK circuitry for brown-out protection and recovery
- Built-in load sharing capability
- Built-in overloading protection capability
- Onboard field replaceable unit (FRU) information
- I^2C interface for server management functions
- Integral handle for insertion/extraction

14.2 Chapter Structure and Outline

The information contained in this chapter is organized into three sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 14.3: AC-input Power Supply Cage
Provides an overview of the Intel® Telco/Industrial Grade Server TIGPR2U AC-input power cage.

Section 14.4: AC-input Power Supply Module
Provides an overview of the Intel® Telco/Industrial Grade Server TIGPR2U AC-input power supply module.

14.3 AC-input Power Supply Cage

14.3.1 AC-input Power Supply Cage Mechanical Specification

The AC-input power supply cage can support up to two 500W SSI TPS power supply modules in a 1+1 configuration or a non-redundant single module configuration. The cage incorporates dual AC inputs with two EMI filters.

A mechanical drawing for the power supply cage is presented in the following figure.

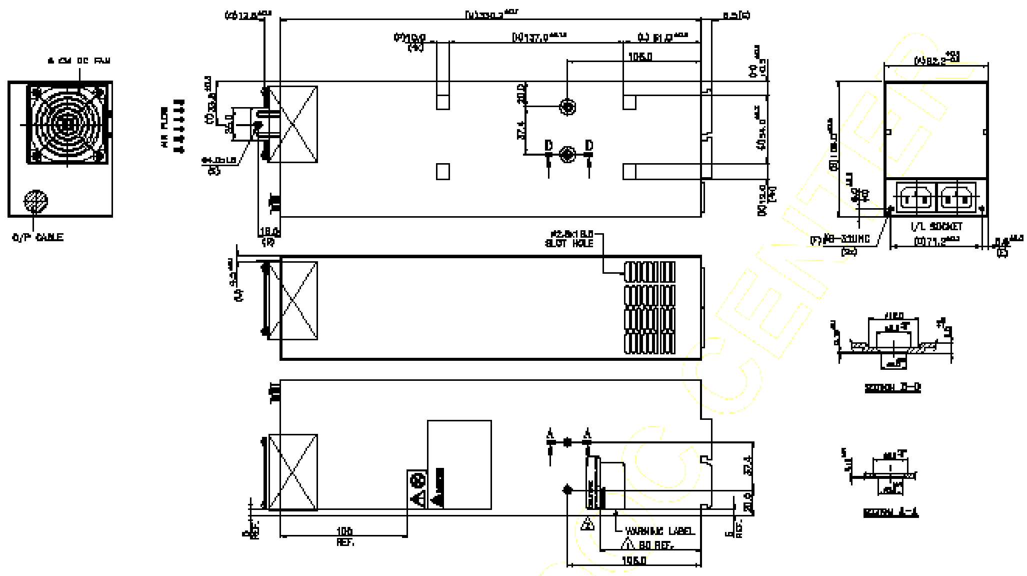


Figure 50. Power Supply Cage Mechanical Drawing

14.3.1.1 Power Supply Edge Connector Slot

See Section 14.4 for details.

14.3.1.2 Power Supply Harness

The following figure shows the harness lengths and designators. The DC output harness connectors are UL1007 rated: 90°C, 300V or an Intel-approved equivalent. Each connector is described in detail in the following sections.

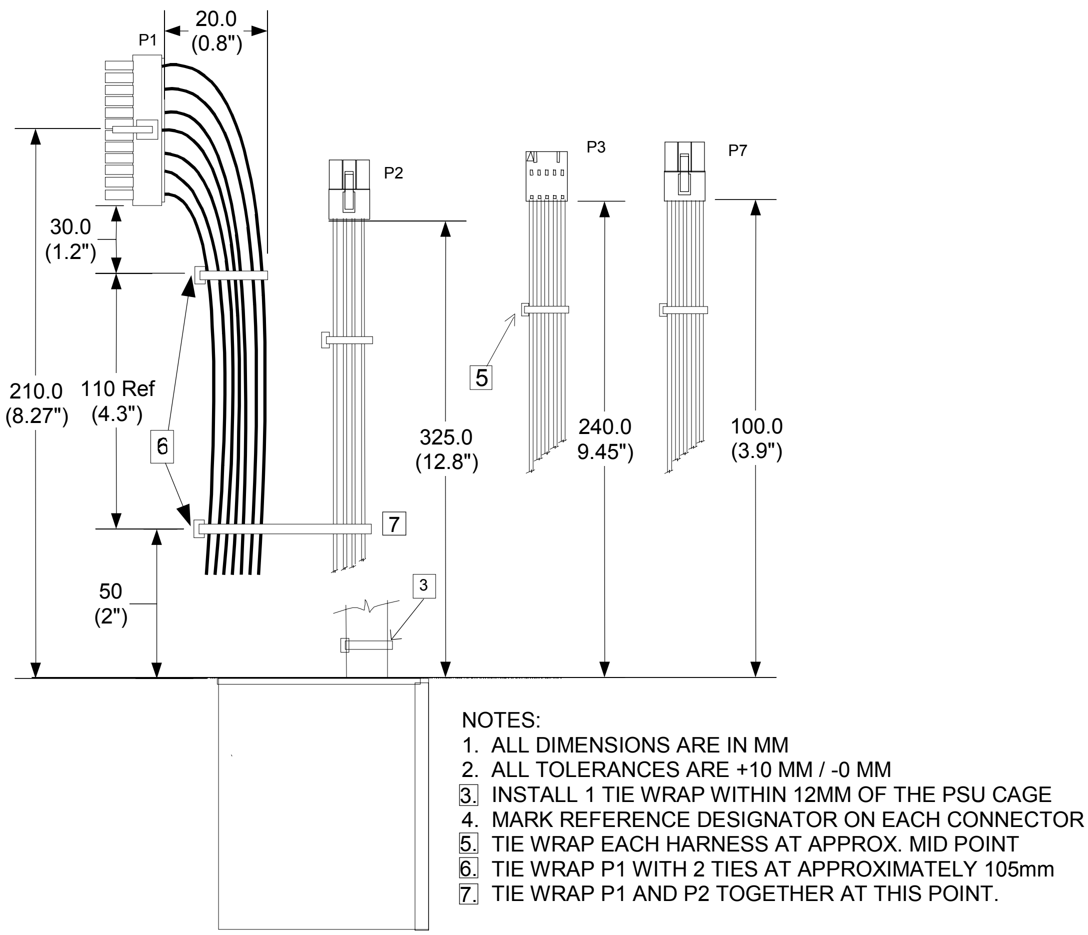


Figure 51. Power Supply Harness Detail

14.3.1.2.1 P1 Baseboard Connector

A 24-pin Molex* 39-01-2245 connector and harness from the power supply cage provides the Intel® Server Board SE7501WV2 with the required voltages and interface signals. The following table provides the connector pin-out.

Table 125. 24-pin Baseboard Power Connector Pin-out

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+3.3 VDC	Orange	13	+3.3VDC	Orange
2	+3.3 VDC	Orange	14	-12VDC	Blue
3	COM	Black	15	COM	Black
4	+5 VDC*	Red	16	PS_ON	Green
5	COM *	Orange	17	COM	Black
6	+5 VDC	Red	18	COM	Black

7	COM	Black	19	COM	Black
8	PWR OK	Gray	20	Reserved	NC
9	5 VSB	Purple	21	+5VDC	Red
10	+12 V1	Yellow	22	+5VDC	Red
11	+12 V1	Yellow	23	+5VDC	Red
12	+3.3 VDC	Orange	24	COM	Black

14.3.1.2.2 P2 Processor Power Connector

An 8-pin Molex* 39-01-2080 connector and harness from the power supply cage provides the Intel® Server Board SE7501WV2 with the required +12V power required for the processors. The following table provides the connector pin-out.

Table 126. P2 Processor Power Connector Pin Assignments

PIN	SIGNAL	18 AWG COLOR	PIN	SIGNAL	18 AWG COLOR
1	COM	Black	5	+12 V3	Yellow/Black Stripe
2	COM	Black	6	+12 V3	Yellow/Black Stripe
3	COM	Black	7	+12 V3	Yellow/Black Stripe
4	COM	Black	8	+12 V3	Yellow/Black Stripe

14.3.1.2.3 P3 Power Management Signal Cable

A 5-wire cable with a Molex* 50-57-9405 female housing connector is used to direct power management signals to the Intel® Server Board SE7501WV2. The following table shows the pin-out.

Table 127. Power Management Signal Cable Pin-out

Pin	Signal	Description
1	I2C Clock	Serial Clock.
2	I2C Data	Serial Data. Information from the power supply.
3	Alert#	Indicates power supply is operating beyond its limits and has failed or may fail soon.
4	COM	Return remote sense
5	3.3RS	3.3V sense

14.3.1.2.4 P7 FPIO System Board Connector

A 6-wire cable with a Molex* Mini-Fit Jr. PN# 39-01-2065 connector is used to provide power to the FPIO system board for system logic power, for peripheral drive power, and for disk drive power.

Table 128. FPIO System Board Connector Pin-out

Pin	Signal	22 AWG COLOR
1	Ground	Black
2	Ground	Black

3	5V	Red
4	12V3	Yellow/Blue Stripe
5	12V3	Yellow/Blue Stripe
6	3.3V	Orange

14.3.1.3 Output Current Requirements

The combined output power of all outputs is 480W. Each output has a maximum and minimum current rating shown in the following table. Two DC-to-DC converters, located in the cage, provide the 3.3V and 5V rails. Total combined power for the 3.3V and 5V outputs is a maximum of 120W.

Table 129. Power Supply Cage 480W Load Ratings

	+3.3V	+5V	+12V1	+12V2	+12V3	-12V	5VSB
MAX1	6A	20A	18A	5.3A	5.3A	0.5A	2A (2.5A- peak)
MAX2	20A	11A	6A	16.5A	6A	0.5A	2A (2.5A- peak)
MAX3	9A	0.5A	18A	15A	1.5A	0.5A	2A (2.5A- peak)
MAX4	0.5A	6A	1.5A	15A	18A	0.5A	2A (2.5A- peak)
MAX5	0.5A	6A	15A	18A	1.5A	0.5A	2A (2.5A- peak)
MAX6	0.5A	6A	1.5A	15A	18A	0.5A	2A (2.5A- peak)
MIN DYNAMIC	2.0A	2.0A	1.5A	1.5A	1.5A	0A	0A
MIN STATIC	0.5A	0.5A	1.5A	1.5A	0.5A	0A	0A

14.3.1.4 Hot Swapping Power Modules

The AC-input power supply cage is capable of supporting hot swapping of power supply modules in a 1+1 configuration. Hot swapping a power supply module is the process of extracting and inserting a power supply module from an operating system.

14.3.1.5 Intelligent Cage Functions

The power supply cage contains a Microchip* PIC16C74B OTP or PIC16C74C:MASK ROM microcontroller to monitor the status of the modules and provide control functions for the cage. The microcontroller is configured as a slave device on the SMBus. The status of the module and cage signals are available via the SMBus interface. The SMBus is also connected to each power module. The microcontroller is powered by 5Vstby and is connected to the ground on the power share board. The microcontroller makes use of the watchdog timer to reset the device in case the controller locks up.

14.3.1.6 FRU Data

The power supply cage contains a 2 KB EEPROM device that contains FRU data for the cage according to the IPMI spec. Each separate output is given a different number for identification purposes.

14.3.1.7 Air Flow

The cage incorporates a 60mm fan for self-cooling. The cooling air enters the cage from the DC connector side, passing through the cage. The air flowing through the power supply may be pre-heated by the system. Inlet air to the cage should be in the range of 5 to 50°C.

14.4 AC-input Power Supply Module

The AC-input power system supports one 500W SSI TPS (Thin Power Supply) module for a non-redundant configuration, or two in a 1+1 redundant configuration. The power supply module provides three main outputs; +12V, -12V, and 5V standby, along with the 15VBIAS voltage. Two DC-to-DC converters located in the cage provide the 3.3V and 5V rails from the 12V provided by the power supply module.

The power supply module contains no fans. However, a fan in the AC-input power supply cage provides cooling to the module(s). The module provides a handle to assist in insertion and extraction and can be inserted and extracted without the assistance of tools.

The combined maximum output power of all outputs is 500W. Each output has a maximum and minimum current rating as shown in the following table.

Table 130. Power Supply Module 500W Load Ratings

	+12V	-12V	5VSB	15Vbias
MAX	40A	0.5A	2.5A	50mA
MIN STATIC	0A	0A	0A	0mA
MIN DYNAMIC	1.5A	0A	0A	0mA

14.4.1.1.1 Power Supply Module Mechanical

The power supply module mechanical outline and dimensions are shown in the following figure.

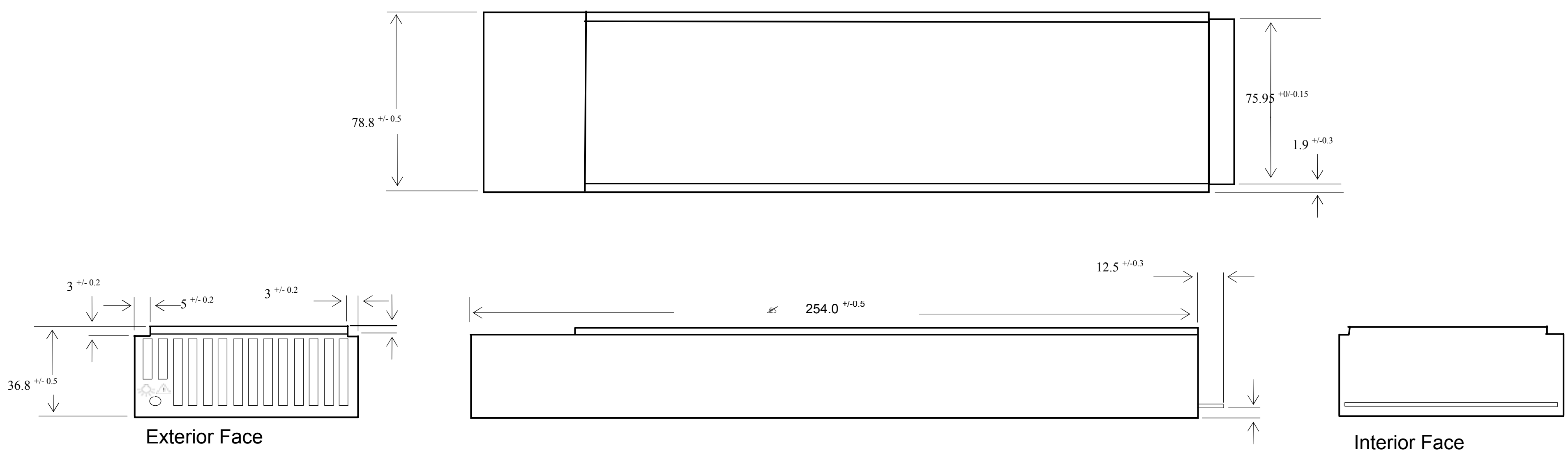


Figure 52. Outline Drawing Power System Enclosure

14.4.1.1.2 Power Supply LED Indicator

The power supply module provides a single external bi-color LED to indicate the status of the power supply. When AC is applied to the PSU and standby voltages are available, the LED will blink green. The LED will be solid green to indicate that all the power outputs are available. The LED will be solid amber to indicate a power supply failure, shutdown due to over-current, or shutdown due to over-temperature. Refer to the following table for conditions of the LED.

Table 131. LED Indicators

POWER SUPPLY CONDITION	Power Supply LED
No AC power to all PSU	OFF
No AC power to this PSU only	AMBER
AC present / Only Standby Outputs On	BLINK GREEN
Power supply DC outputs ON and OK	GREEN
Power supply failure (includes over voltage, over current, over temperature)	AMBER
VRM failure (cage related)	AMBER
240VA limit protection (cage related)	AMBER

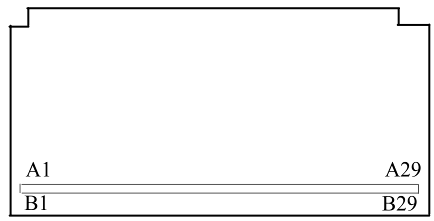
14.4.1.1.3 Power Supply Module to Cage Interconnect

The power supply module provides edge fingers that mate to a connector located in the power supply cage. This is a blind mating type connector that connects the power supply's input voltage, output voltages and signals.

The following table provides the pin-out for the power supply edge connector.

- Signals that can be defined as low true or high true use the convention: *signal*# = low true
- Reserved pins are for future use.
- No Connect (NC) locations must be empty locations on the power supply edge card and in the mating connector to meet spacing requirements.

Table 132. Edge Connector Pin-out



Interior Face

Description	Pin#	Pin#	Description
NC	B1	A1	NC
AC Neutral Pre-charge	B2	A2	AC Neutral
NC	B3	A3	NC
AC Line Pre-charge	B4	A4	AC Line
NC	B5	A5	NC
NC	B6	A6	NC
-12V	B7	A7	5VSB
PSON#	B8	A8	PSKill
A0	B9	A9	ReturnS
A1	B10	A10	SCL
ACWarning	B11	A11	SDA
Fail	B12	A12	Alert#
PWOK	B13	A13	Vbias
12LS	B14	A14	12VS
Ground	B15	A15	Present#
Ground	B16	A16	12V
Ground	B17	A17	12V
Ground	B18	A18	12V
Ground	B19	A19	12V
Ground	B20	A20	12V
Ground	B21	A21	12V
Ground	B22	A22	12V
Ground	B23	A23	12V
Ground	B24	A24	12V
Ground	B25	A25	12V
Ground	B26	A26	12V
Ground	B27	A27	12V
Ground	B28	A28	12V
Ground	B29	A29	12V

14.4.1.2 Thermal Protection

The power supply incorporates thermal protection that causes a shut down if airflow through the power supply is insufficient. Thermal protection activates shutdown before the temperature of any power supply component exceeds the maximum rated temperature. This shutdown takes place prior to over-temperature induced damage to the power supply.

15. Regulatory Specifications

The Intel® Telco/Industrial Grade Server meets the specifications and regulations for safety and EMC defined in this chapter.

15.1 Safety Compliance

USA	UL 60950, 3rd Edition/CSA 22.2, No. 650-M93
Canada	cUL Certified – CAN/CSA 22.2. No. 60950-00 for Canada (product bears the single UL mark for U.S. and Canada)
Europe	Low Voltage Directive, 73/23/EECTUV/GS to EN60950 2nd Edition with Amendments, A1 = A2 + A3 + A4
International	TUV/CB to IEC 60950 3rd Edition, EN60 950 2nd Edition + Amd 1-4, EMKO-TSE (74-SEC) 207/94 plus all international deviations
Australia/New Zealand	CB Report to IEC 60950, 3rd Edition plus International deviations

15.2 Electromagnetic Compatibility

USA	FCC 47 CFR Parts 2 and 15, Verified Class A Limit
Canada	IC ICES-003 Class A Limit
Europe	EMC Directive, 89/336/EEC EN55022, Class A Limit, Radiated & Conducted Emissions EN55024, ITE Specific Immunity Characteristics for ITE EN61000-4-2, ESD Immunity (Level 2 Contact Discharge, Level 3 Air Discharge) EN61000-4-3, Radiated Immunity (Level 2) EN61000-4-4, Electrical Fast Transient (Level 2) EN61000-4-5, AC Surge EN61000-4-6, Conducted RF EN61000-4-8, Power Frequency Magnetic Fields EN61000-4-11, Voltage Dips and Interrupts EN61000-3-2, Limit for Harmonic Current Emissions EN61000-3-3, Voltage Flicker
Australia/New Zealand	AS/NZS 3548, Class A Limit
Japan	VCCI Class A ITE (CISPR 22, Class A Limit) IEC 1000-3-2, Limit for Harmonic Current Emissions
Taiwan	BSMI Approval, CNS 13438, Class A
Korea	RRL Approval, Class A
China	CCC Approval
Russia	GOST Approval
International	CISPR 22, Class A Limit

15.3 CE Mark

The CE marking on this product indicates that it is in compliance with the European Union's EMC Directive 89/336/EEC, and Low Voltage Directive, 73/23/EEC.

15.4 NEBS Compliance (DC Input Only)

The Intel® Telco/Industrial Grade Server TIGPR2U with DC input is compliant with the following NEBS specifications:

- NEBS GR-63-CORE – Physical Protection
- NEBS GR-1089-CORE – Electromagnetic Compatibility and Electrical Safety

15.5 ETSI Standards Compliance (DC Input Only)

The Intel® Telco/Industrial Grade Server TIGPR2U with DC input is compliant with the following ETSI specifications:

• ETSI EN 300 386	EMC requirements for Telecom Equip.
• ETS 300-019-2-1	Storage Tests, Class T1.2
• ETS 300-019-2-2	Transportation Tests, Class T2.3
• ETS 300-019-2-3	Operational Tests, Class T3.2
• ETS 753	Acoustic Noise

Appendix A: Glossary

This appendix contains important acronyms and terms used in the preceding chapters.

Term	Definition
A, Amp	Ampere
A/µs	Amps per microsecond
AC	Alternating current
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
APIC	Advanced Programmable Interrupt Controller
ASIC	Application specific integrated circuit
AWG	American wire gauge
BIOS	Basic input/output system
BMC	Bus management controller
Bridge	Circuitry that connects one computer bus to another
Byte	8-bit quantity
C	Centigrade
CE	Community European
CFM	Cubic feet per minute
CISPR	International Special Committee on Radio Interference
CSA	Canadian Standards Organization
CTS	Clear to send
DAT	Digital audio tape
dB	Decibel
dBA	Acoustic decibel
DC	Direct current
DIMM	Dual inline memory module
DMI	Desktop management interface
DOS	Disk operating system
DRAM	Dynamic random access memory
DSR	Data set ready
DTR	Data terminal ready
DWORD	Double word - 32-bit quantity
ECC	Error checking and correcting
EEPROM	Electrically erasable programmable read-only memory
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EMP	Emergency management port
EN	European Standard (Norme Européenne or Europäische Norm)
EPS	External product specification
ESCD	Extended system configuration data
ESD	Electrostatic discharge
ESR	Equivalent series resistance
F	Fahrenheit

Term	Definition
FCC	Federal Communications Commission
FFC	Flexible flat connector
Flash ROM	EEPROM
FPC	Front panel controller
FRB	Fault resilient booting
FRU	Field replaceable unit
G	Acceleration in gravity units, 1G = 980665 m/s^2
GB	Gigabyte - 1024 MB
GND	Ground
GPIO	General purpose input/output
Grms	Root mean square of acceleration in gravity units
GUI	Graphical user interface
HDD	Hard disk drive
HPIB	Hot-plug indicator board
HSC	Hot-swap controller
Hz	Hertz – 1 cycle/second
I/O	Input/output
I^2C*	Inter-integrated circuit bus
ICMB	Intelligent Chassis Management Bus
IDE	Integrated drive electronics
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IFLASH	Utility to update Flash EEPROM
IMB	Intelligent management bus
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Initiative
IRQ	Interrupt request line
ITE	Information technology equipment
ITP	In-target probe
JAE	Japan Aviation Electronics
KB	Kilobyte - 1024 bytes
kV	Killivolt – 1,000 volts
L2	Second-level cache
LAN	Local area network
LED	Light-emitting diode
LVDS	Low voltage differential SCSI
mA	Milliamp
MB	Megabyte - 1024 KB
MEC	Memory expansion card
mm	Millimeter
MPS	Multiprocessor specification
MTTR	Mean time to repair
mΩ	Milliohm
NEMKO	Norges Elektriske Materiellkontroll (Norwegian Board of Testing and Approval of Electrical Equipment)

Term	Definition
NIC	Network interface card
NMI	Non-maskable interrupt
NWPA	NetWare* Peripheral Architecture
ODI	Open data-link interface
OEM	Original equipment manufacturer
OPROM	Option ROM (expansion BIOS for a peripheral)
OS	Operating system
OTP	Over-temperature protection
OVP	Over-voltage protection
PC-100	Collection of specifications for 100 MHz memory modules
PCB	Printed circuit board
PCI	Peripheral component interconnect
PHP	PCI hot-plug
PID	Programmable interrupt device
PIRQ	PCI interrupt request line
PMM	POST memory manager
PnP	Plug and play
POST	Power-on Self Test
PSU	Power supply unit
PVC	Polyvinyl chloride
PWM	Pulse width modulation
RAS	Reliability, availability, and serviceability
RIA	Ring indicator
RPM	Revolutions per minute
RTS	Request to send
SAF-TE	SCSI Accessed Fault-Tolerant Enclosures
SCA	Single connector attachment
SCL	Serial clock
SCSI	Small Computer Systems Interface
SDR	Sensor data records
SDRAM	Synchronous dynamic RAM
SEC	Single edge connector
SEL	System event log
SELV	Safety extra low voltage
SEMKO	Sverge Elektriske Materiellkontroll (Swedish Board of Testing and Approval of Electrical Equipment)
SGRAM	Synchronous graphics RAM
SM	Server management
SMBIOS	System management BIOS
SMBus	Subset of I^2C bus/protocol (developed by Intel)
SMI	System management interrupt
SMM	Server management mode
SMP	Symmetric multiprocessing
SMRAM	System management RAM
SMS	Server management software

Term	Definition
SPD	Serial presence detect
SSI	Server system infrastructure
TUV	Technischer Uberwachungs-Verein (A safety testing laboratory with headquarters in Germany)
UL	Underwriters Laboratories, Inc.
USB	Universal Serial Bus
UV	Under-voltage
V	Volt
VA	Volt-amps (volts multiplied by amps)
Vac	Volts alternating current
VCCI	Voluntary Control Council for Interference
Vdc	Volts direct current
VDE	Verband Deutscher Electrotechniker (German Institute of Electrical Engineers)
VGA	Video graphics array
VRM	Voltage regulator module
VSB	Voltage standby
W	Watt
WfM	Wired for Management
Word	A 16-bit quantity
Ω	Ohm
μF	Microfarad
μs	Microsecond

Appendix B: Reference Documents

Refer to the following documents for additional information:

ACPI

- *Advanced Configuration And Power Interface Specification*, Revision 1.0b, http://www.teleport.com/~acpi/.

Boot

- *BIOS Boot Specification*, Version 1.01, http://www.ptltd.com/techs/specs.html.
- *El Torito CD-ROM Boot Specification*, Version1.0, http://www.ptltd.com/techs/specs.html.

DMI

- *Desktop Management Interface (DMI) Specification*, Version 2.0s, Desktop Management Task Force, Inc., http://www.dmtf.org/spec/dmis.html.

ESCD

- *Extended System Configuration Data Specification*, Version 1.02a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

Ethernet

- *Intel 82559 Fast Ethernet Multifunction PCI/Cardbus Controller Datasheet*, Intel Corporation, http://developer.intel.com/design/network/datashts/738259.htm.

Flash

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