Intel® Server Board SE7210TP1-E

Technical Product Specification

Intel order number C49240-002

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Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
February 2004	1.0	Initial Release.
October 2004	2.0	Updated BIOS information to be consistent with latest BIOS release.

This product specification applies to the Intel® Server Board SE7210TP1-E with BIOS identifier SE7210TP P04.10.

Changes to this specification will be published in the Intel Server Board SE7210TP1-E Specification Update before being incorporated into a revision of this document.

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1. Introduction

This Technical Product Specification (TPS) provides detail to the architecture and feature set of the Intel® Server Board SE7210TP1-E.

The target audience for this document is anyone wishing to obtain more in depth detail of the server board than what is generally made available in the board's Users Guide. It is a technical document meant to assist people with understanding and learning more about the specific features of the board.

This is one of several technical documents available for this server board. All of the functional sub-systems that make up the board are described in this document. However, certain low level detail of specific sub-systems is not included. Design level information for specific sub-systems can be obtained by ordering the External Product Specification (EPS) for a given sub-system. The EPS documents available for this server board include the following:

- Intel® Server Board SE7210TP1-E BIOS External Product Specification
- Intel Server Management Essential Firmware EPS

These documents are not made publicly available and must be ordered by your local Intel representative.

1.1 Chapter Outline

This document is divided into the following chapters

Chapter 1 – Introduction

Chapter 2 – Product Overview

Chapter 3 – Board Architecture

Chapter 4 – System BIOS

Chapter 5 – Platform Management Architecture

Chapter 6 – Error Reporting and Handling

Chapter 7 – Connector Pin-out and Jumper Blocks

Chapter 8 – Environmental Specifications

Chapter 9 – Miscellaneous Board Information

Appendix A – Glossary of Terms

1.2 Server Board Use Disclaimer

Intel Corporation server boards contain a number of high-density VLSI and power delivery components which need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation can not be held responsible, if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. Server Board Overview

The Intel® Server Board SE7210TP1-E is a monolithic printed circuit board with features that were designed to support the entry server markets.

2.1 SE7210TP1-E SKU Availability

In this document, ”SE7210TP1-E” will be used to describe the family of boards that will be made available under a common marketing name. The core features for each board will be common; however each board will have the following distinctions:

SE7210TP1:	Onboard SATA (RAID)
SE7210TP1SCSI:	Onboard SCSI + Onboard SATA (RAID)
SR1325TP1:	Onboard SATA (RAID) + Low Profile PCI Slot and Riser

Throughout this document, all references to SE7210TP1-E will refer to all three board SKUs unless specifically noted otherwise. The board you select to use may or may not have all the features described based on the listed board differences.

2.2 SE7210TP1-E Feature Set

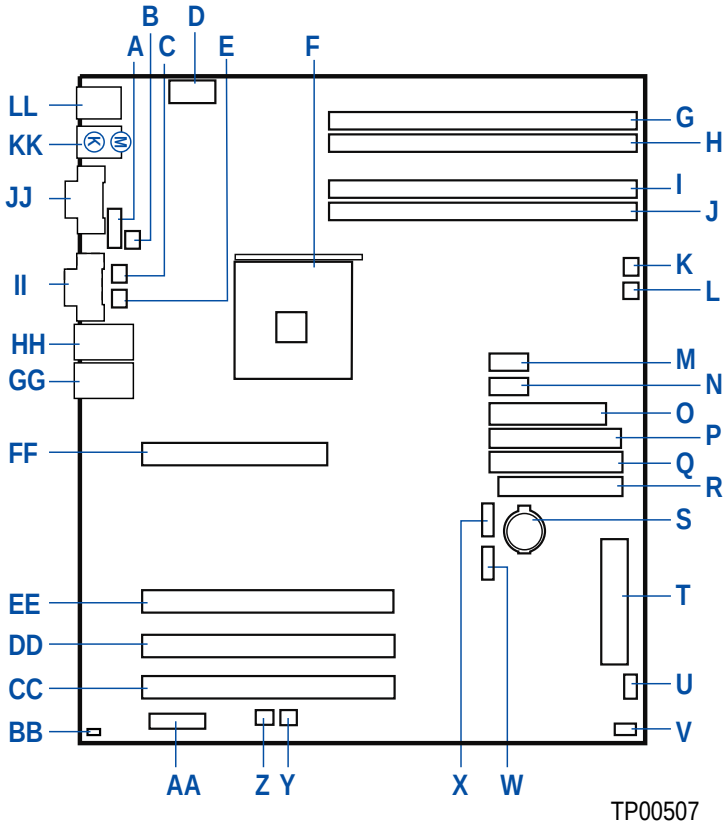
The Intel Server Board SE7210TP1-E provides the following feature set:

- Support for an Intel® Celeron processor or an Intel® Pentium® 4 processor with hyper-threading technology in a μPGA478 socket.
- 400/533/800 MHz Front Side Bus (FSB)
- Intel® E7210 chipset
  - Intel® 827210 Memory Controller Hub (MCH)
  - Intel® 6300ESB I/O Controller Hub
  - Intel® 82802AC 8 Megabit Firmware Hub (FWH)
- Support for single-sided or double-sided dual inline memory module (DIMM) double-data rate (DDR) memory providing up to 4 GB of system memory with four 184-pin DIMM sockets.
  - PC3200 (400 MHz): to run 400 MHz memory at full speed requires an Intel Pentium 4 processor with 800 MHz system bus frequency.
  - PC2700 (333 MHz): to run 333 MHz memory at full speed requires an Intel Pentium 4 processor with 533 MHz system bus frequency.

    Note: PC2700 (333 MHZ) memory will run at 320 MHz frequency when using an Intel Pentium 4 processor with 800 MHz system bus frequency.
  - PC2100 (266 MHZ): PC2100 (266 MHZ) memory may only be used with an Intel Pentium 4 processor with 400 MHz or 533 MHz system bus frequency only.
- Intel 82547GI Platform LAN Connect (PLC) device for 10/100/1000 Mbits/sec Ethernet LAN connectivity
- Intel 82551QM device for 10/100 Mbits/sec Ethernet LAN connectivity

- Two independent PCI buses (one 32-bit, 33 MHz, 5 V; one 64-bit, 66 MHz, 3.3V) with four PCI connectors and two embedded devices:
  - Three PCI-X 64-bit PCI slots
  - One 32-bit PCI slot
  - Integrated 2D/3D graphics controller: ATI Rage* XL Video Controller with 8 MB of SDRAM
  - Optional single channel, Ultra 320 SCSI controller (on SE7210TP1SCSI): Adaptec* 7901
- LPC (Low Pin Count) bus segment with one embedded device: Winbond* W83627HF-AW LPC Bus I/O controller chip providing all PC-compatible I/O (floppy, serial, keyboard and mouse)
- Three external USB 2.0 ports on the back panel with an additional internal header, which provides support for one additional USB port for front panel support (four total possible USB 2.0 ports)
- One serial port and one serial port header
- Two Serial ATA (SATA) ports provide interface for SATA hard drives and ATAPI devices
- Two IDE interfaces with Ultra 33, 66 and 100 DMA mode
- Support for up to six system fans and one processor fan
- Server System Infrastructure (SSI)-compliant connectors for SSI interface support: front panel, power connector
- Intel Server Management 5.8 support via the National* Semiconductor PC87431 integrated management controller

Figure 1. Intel Server Board SE7210TP1-E Diagram shows the board layout of the server board SE7210TP1-E. Each connector and major component is identified by number and identified below the figure.



A: Serial B Header
B: CPU Fan Header
C: Sys Fan Header 3
D: +12 V CPU Power Connector
E: Sys Fan Header 4
F: Processor Socket
G: DIMM 2B Socket
H: DIMM 2A Socket
I: DIMM 1B Socket
J: DIMM 1A Socket
K: Sys Fan Header 1
L: Sys Fan Header 2
M: Front Panel USB Header
N: Aux Power Connector
O: Main Power Connector
P: Secondary IDE Connector
Q: Primary IDE Connector
R: Floppy Connector
S: Battery
T: Front Panel Connector
U: Hot Swap Backplane Header
V: SCSI LED Header
W: SATA-A1 Connector
X: SATA-A2 Connector
Y: Sys Fan Header 6
Z: Sys Fan Header 5
AA: Jumper Block
BB: Chassis Intrusion Header
CC: PCI-X Slot 1, 64/66 RAIDIOS
DD: PCI-X Slot 2, 64/66
EE: PCI-X Slot 3, 64/66
FF: PCI Slot 6, 32/33
GG: NIC 2 (10/100 Mbit)
HH: NIC 1 (1 Gbit)
II: Video Connector
JJ: Serial A Connector
KK: Keyboard and Mouse
LL: USB Connectors

Figure 1. Intel Server Board SE7210TP1-E Diagram

The following mechanical drawing shows the physical dimensions of the baseboard.

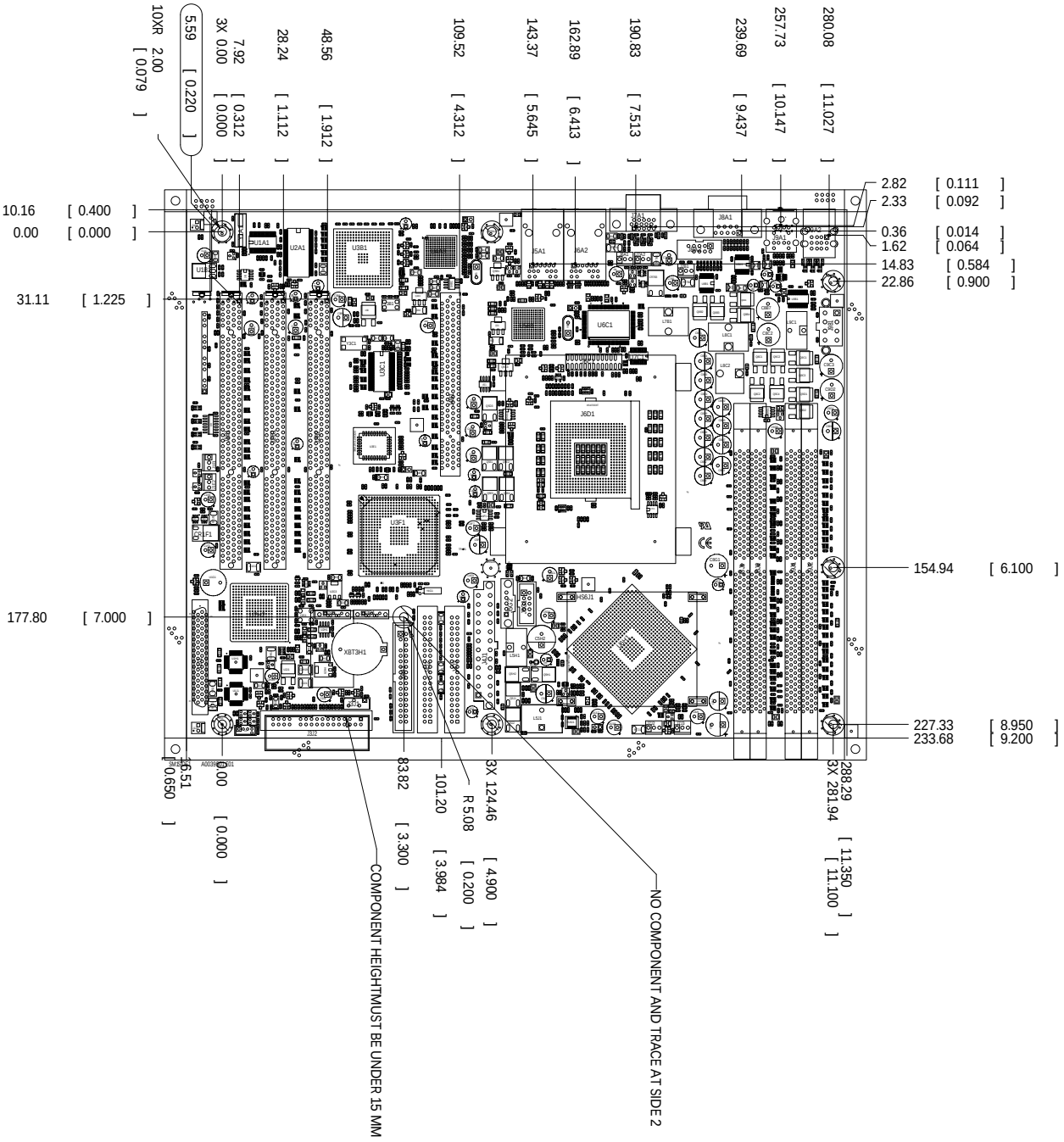
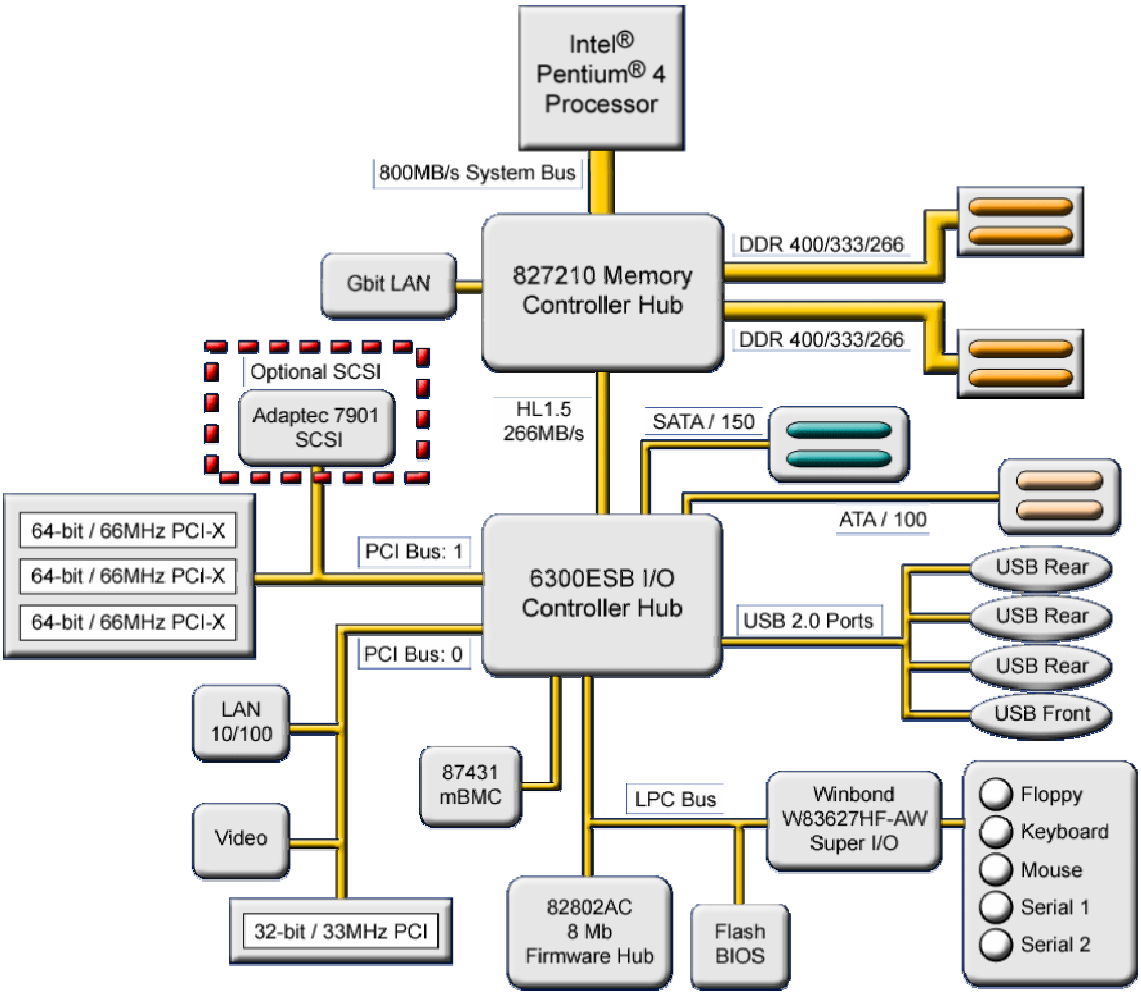


Figure 2. Intel Server Board SE7210TP1-E Mechanical Drawing

3. Functional Architecture

This chapter provides a high-level description of the functionality distributed between the architectural blocks of the Intel Server Board SE7210TP1-E.



3.1 Processor Subsystem

The support circuitry for the processor sub-system consists of the following:

Single µPGA478 processor socket
Processor host bus AGTL+ support circuitry.
Reset configuration logic.

3.1.1 Reset Configuration Logic

The BIOS determines the processor stepping, cache size, and other processor information through the CPUID instruction. The requirement is for the processor to run at a fixed speed. The processor cannot be programmed to operate at a lower or higher speed.

On the SE7210TP1-E platform, the BIOS is responsible for configuring the processor speed. The BIOS uses CMOS settings to determine which speed to program into the speed setting device. The processor information is read at every system power-on.

3.1.2 Processor Support

The Intel Server Board SE7210TP1-E supports a single Intel® Pentium® 4 processor, or a single Intel® Celeron® processor with a system bus of 400 /533 /800 MHz. The server board supports the processors listed in Table 1.

Table 1. Processor Support Matrix

Type	Designation	System Bus	L2 Cache Size
Pentium® 4 processor supporting Hyper-Threading Technology	3.4, 3.2 GHz	800 MHz	2 MB
Pentium® 4 processor supporting Hyper-Threading Technology	3.4, 3.2, 3.0, 2.8 GHz	800 MHz	1 MB
Pentium® 4 processor supporting Hyper-Threading Technology	2.8 GHz	533 MHz	1 MB
Pentium® 4 processor supporting Hyper-Threading Technology	3.2, 3.0, 2.80, 2.40, 2.60 GHz	800 MHz	512 KB
Pentium® 4 processor supporting Hyper-Threading Technology	3.06 GHz	533 MHz	512 KB
Pentium® 4 processor	2.8, 2.66, 2.6, 2.53, 2.4, 2.26, 2.0 GHz	400 / 533 MHz	512 KB
Celeron® processor	2.8, 2.7, 2.6, 2.5, 2.4, 2.3, 2.2, 2.1, 2.0 GHz	400 MHz	128 KB

⚠ CAUTION

Use only the processors listed above. Use of unsupported processors can damage the board, the processor, and the power supply. See the Intel® Server Board SE7210TP1-E Specification Update or go to http://support.intel.com/support/motherboards/server/SE7210TP1-E/ for the current list of supported processors for this board.

NOTE

Use only ATX12V or EPS12V compliant power supplies with the server board SE7210TP1-E. ATX12V and EPS12V power supplies have an additional power lead that provides required supplemental power for the Intel Pentium 4 processor. The board will not boot if you do not connect the 20-pin (or 24-pin) and 4-pin (or 8-pin) leads of ATX12V or EPS12V power supplies to the corresponding connectors.

Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.

3.1.3 Microcode

IA32 processors have the capability of correcting specific errata through the loading of an Intel-supplied data block (microcode update). The BIOS is responsible for storing the update in nonvolatile memory and loading it into each processor during POST. The BIOS performs all the recommended update signature verification prior to storing the update in the Flash.

3.1.4 Processor Cache

The BIOS enables all levels of processor cache as early as possible during POST. There are no user options to modify the cache configuration, size or policies. All detected cache sizes are reported in the SMBIOS Type 7 structures. The largest and highest level cache detected is reported in BIOS Setup

3.1.5 Hyper-Threading Technology

Intel® Pentium® 4 processors support Hyper-Threading Technology. The BIOS will detect processors that support this feature and will enable the feature during POST. BIOS Setup provides an option to selectively enable or disable this feature. The default behavior is enabled.

The BIOS will create additional entries in the ACPI MP tables to describe the virtual processors. The SMBIOS Type 4 structure will show only the physical processors installed.

3.2 Intel E7210 Chipset

The Intel E7210 chipset consists of the following devices:

- Intel 827210 Memory Controller Hub (MCH) with Accelerated Hub Architecture (AHA) bus
- Intel 6300ESB I/O Controller Hub with AHA bus
- Intel 82802AC (8 Mbit) Firmware Hub (FWH)

3.2.1 Intel 827210 Memory Controller Hub (MCH)

The MCH is a centralized controller for the system bus, the memory bus and the Accelerated Hub Architecture interface. The 6300ESB I/O is a centralized controller for the Server Board SE7210TP1-E's I/O paths. The FWH provides the nonvolatile storage of the BIOS. The component combination provides the chipset interfaces as shown in Figure 3.

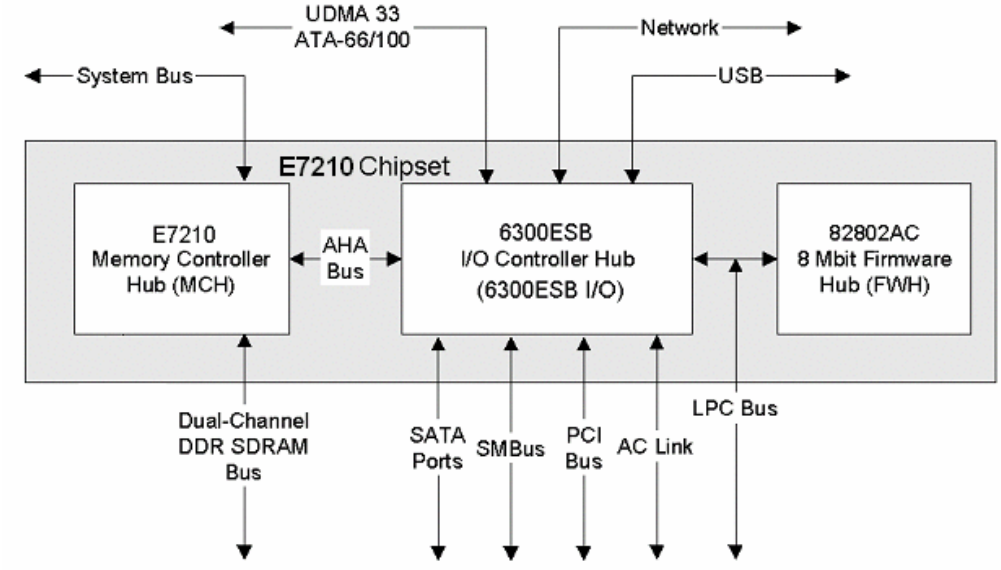


Figure 3. Intel E7210 Chipset Block Diagram

3.2.2 Intel 82802AC 8 Megabit Firmware Hub (FWH)

The FWH provides the following:

- System BIOS program
- Logic that enables protection for storing and updating platform information

3.2.3 PCI-X

The PCI-X segment comes from 6300ESB I/O, and only runs at 66MHz maximum.

The PCI-X interfaces of the 6300ESB I/O are compliant with the PCI-X Addendum to the PCI Local Bus Specification Revision 1.0b as well as the Mode 1 and Mode 2 (266 MHz) sections of the PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification Revision 2.0a and the PCI-X Protocol Addendum to the PCI Local Bus Specification Revision 2.0a. PCI-X Mode 2 provides enhancements over PCI that enable faster and more efficient data transfers. For conventional PCI Mode, the 6300ESB I/O supports PCI bus frequencies of 66 MHz, 100 MHz, and 133 MHz. For the PCI-X Mode 2, the 6300ESB I/O supports PCI bus frequencies of 66 MHz, 100 MHz, 133 MHz and 266 MHz.

On the SE7210TP1-E server board, the PCI-X interface (P64-A) is independently controlled to operate in either a conventional PCI or PCI-X mode. P64-A is routed to control I/O from the 82547GI Ethernet controller and is capable of supporting MCH CSA interfaces depending on the riser card used. P32-A is routed to control I/O from the 32-bit PCI slot and the Adaptec* 7901Single Channel SCSI controller.

3.2.4 Low Profile Riser Slot

The Low Profile riser slot is a standard 202-pin slot supporting PCI-X signals. Its location on the board will allow only the use of low profile add-in cards.

3.2.5 SMBus Interface

The SMBus interface can be used for system and power management related tasks. The interface is compliant with System Management Bus Specification Revision 2.0. The SMBus interface allows full read/write access to all configuration and memory spaces in the FWH.

3.2.6 6300ESB I/O Controller Hub

The 6300ESB I/O is a multi-function device providing an upstream hub interface for access to several embedded I/O functions and features including:

- PCI Local Bus Specification, Revision 2.2 with support for 33 MHz PCI operations and 66 MHz PCI-X operations.
- ACPI power management logic support
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated IDE controller with support for Ultra ATA100/66/33
- Integrated SATA controller
- USB host interface with support for four USB ports; two UHCI host controllers; one EHCI high-speed USB 2.0 host controller
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I2C devices
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support

Each function within the 6300ESB has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

Performance Note: The Hub Link 1.5 interface between the 6300ESB ICH and the 827210 MCH has a theoretical maximum throughput of 266MB/s. Each bus supported by the 6300ESB ICH will share the Hub Link 1.5 bandwidth, this includes the P64-A bus, the P32-A bus, the BMC interface, the LPC bus, the USB 2.0 interface, the Parallel ATA bus and the Serial ATA bus.

3.2.7 PCI Interface

The 6300ESB I/O PCI interface provides a 33 MHz, Revision 2.3 compliant implementation. All PCI signals are 5-V tolerant, except PME#. The 6300ESB I/O integrates a PCI arbiter that supports up to four external PCI bus masters in addition to the internal 6300ESB I/O requests. On the SE7210TP1-E server board this PCI interface is used to support on-board PCI devices including the ATI* video controller.

3.2.8 IDE Interface

The 6300ESB I/O IDE controller has two independent bus-mastering IDE interfaces that can be independently enabled. The IDE interfaces support the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supports Ultra 100 DMA Mode Transfers up to 100Mbytes/s for reads from disk;88.88 Mbytes/s for writes to disk. As well as Ultra66 and Ultra33 DMA mode..
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. The ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The 6300ESB I/O ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized 40-pin, 80-wire cable to reduce reflections, noise, and inductive coupling.

The IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes. The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The server board SE7210TP1-E supports Laser Servo (LS-120) diskette technology through the IDE interfaces. The BIOS supports booting from an LS-120 drive.

NOTE

The BIOS will always recognize an LS-120 drive as an ATAPI floppy drive. To ensure correct operation, do not configure the drive as a hard disk drive.

3.2.9 Serial ATA (SATA) Controller

The SATA controller supports two SATA devices providing an interface for SATA hard disks and ATAPI devices. The SATA interface supports PIO IDE transfers up to 16 Mb/s and Serial ATA transfers up to 1.5 Gb/s (150 MB/s). The 6300ESB I/O's SATA system contains two independent SATA signal ports. They can be electrically isolated independently. Each SATA device can have independent timings. They can be configured to the standard primary and secondary channels.

3.2.10 Low Pin Count (LPC) Interface

The 6300ESB I/O implements an LPC Interface as described in the Low Pin Count Interface Specification, Revision 1.1. The Low Pin Count (LPC) Bridge function of the 6300ESB I/O resides in PCI Device 31: Function 0. In addition to the LPC bridge interface function, D31:F0 contains other functional units including DMA, interrupt controllers, timers, power management, system management, GPIO, and RTC.

3.2.11 Compatibility Modules (DMA Controller, Timer/Counters, Interrupt Controller)

The DMA controller incorporates the logic of two 82C37 DMA controllers, with seven independently programmable channels. Channels 0–3 are hardwired to 8-bit, count-by-byte transfers, and channels 5–7 are hardwired to 16-bit, count-by-word transfers. Any two of the seven DMA channels can be programmed to support fast Type-F transfers.

The 6300ESB I/O supports two types of DMA (LPC and PC/PCI). LPC DMA and PC/PCI DMA use the 6300ESB I/O's DMA controller. The PC/PCI protocol allows PCI-based peripherals to initiate DMA cycles by encoding requests and grants via two PC/PC REQ#/GNT# pairs. LPC DMA is handled through the use of the LDRQ# lines from peripherals and special encoding on LAD[3:0] from the host. Single, Demand, Verify, and Increment modes are supported on the LPC interface. Channels 0–3 are 8 bit channels. Channels 5–7 are 16 bit channels. Channel 4 is reserved as a generic bus master request.

The timer/counter block contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. These three counters are combined to provide the system timer function, and speaker tone. The 14.31818 MHz oscillator input provides the clock source for these three counters.

The 6300ESB I/O provides an ISA-compatible Programmable Interrupt Controller (PIC) that incorporates the functionality of two 82C59 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and two internal interrupts are possible. In addition, the 6300ESB I/O supports a serial interrupt scheme. All of the registers in these modules can be read and restored. This is required to save and restore system state after power has been removed and restored to the platform.

3.2.12 Advanced Programmable Interrupt Controller (APIC)

In addition to the standard ISA-compatible PIC described in the previous section, the 6300ESB I/O incorporates the Advanced Programmable Interrupt Controller (APIC).

3.2.13 Universal Serial Bus (USB) Controller

The 6300ESB I/O contains an Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 -compliant host controller that supports USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480 Mb/s which is 40 times faster than full-speed USB. The 6300ESB I/O also contains four Universal Host Controller Interface (UHCI) controllers that support USB full-speed and low-speed signaling.

The Intel Server Board SE7210TP1-E supports up to four USB 2.0 ports, supports Universal Host Controller Interface (UHCI) and Enhanced Host Controller Interface (EHCI), and uses UHCI- and EHCI-compatible drivers.

The 6300ESB I/O provides the USB controller for all ports, as shown in Figure 4. The port arrangement is as follows:

- Three ports are implemented with stacked back panel connectors
- One port is routed to a USB header which can be connected with a USB cable to the front panel connector

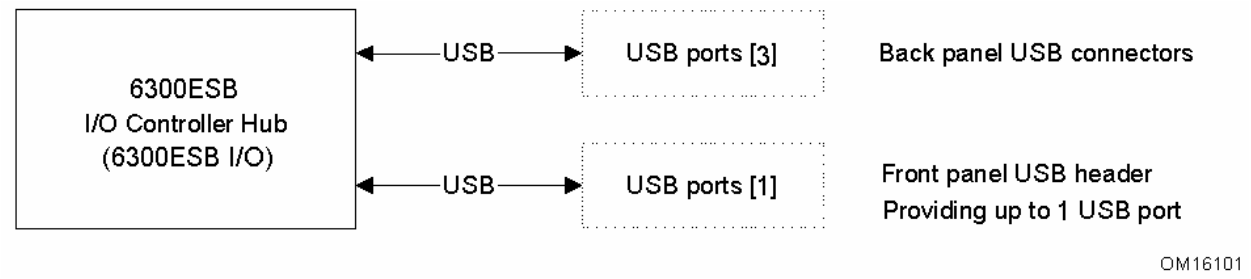


Figure 4. USB Port Configuration

NOTES

Server systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

3.2.14 Real Time Clock, CMOS SRAM, and Battery

The real-time clock provides a time-of-day clock and a multi-century calendar with alarm features. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the server is not plugged into a wall socket, the battery has an estimated life of three years. When the server is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTE

If the battery and AC power fail, the custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

3.2.15 GPIO

Various general purpose inputs and outputs are provided for custom system design. The number of inputs and outputs varies depending on the 6300ESB I/O configuration. All unused GPI pins must be pulled high or low, so that they are at a predefined level and do not cause undue side effects.

3.2.16 Enhanced Power Management

The 6300ESB I/O's power management functions include enhanced clock control, local and global monitoring support for 14 individual devices, and various low-power (suspend) states (e.g., Suspend-to-DRAM and Suspend-to-Disk). A hardware-based thermal management circuit permits software-independent entrance to low-power states. The 6300ESB I/O contains full support for the Advanced Configuration and Power Interface (ACPI) Specification, Revision 2.0b.

3.2.17 System Management Bus (SMBus 2.0)

The 6300ESB I/O contains an SMBus Host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I2C devices. Special I2C commands are implemented. The 6300ESB I/O's SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). Also, the 6300ESB I/O supports slave functionality, including the Host Notify protocol. Hence, the host controller supports eight command protocols of the SMBus interface (see System Management Bus (SMBus) Specification, Version 2.0): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify.

3.3 Memory Subsystem

The Intel 827210 Memory Controller Hub (MCH) is one component of the Intel E7210 chipset. The MCH is a centralized controller for the system bus, the memory bus and the accelerated hub architecture interface.

The server board SE7210TP1-E provides four DIMM slots and supports a maximum memory capacity of 4 GB. The DIMM organization is x72, which includes eight ECC check bits. ECC from the DIMMs are passed through to the processor's system bus. Memory scrubbing, single-bit error correction and multiple-bit error detection is supported. Memory can be implemented with either single-sided (one row) or double-sided (two row) DIMMs.

Table 2. Supported Memory Configurations

DIMM Capacity	Configuration	DDR SDRAM Density	DDR SDRAM Organization Front-side/Back-side	Number of DDR SDRAM Devices
128 MB	DS	64 Mbit	8 M x 8/8 M x 8	16
128 MB	SS	128 Mbit	16 M x 8/empty	8
128 MB	SS	256 Mbit	16 M x 16/empty	4
256 MB	DS	128 Mbit	16 M x 8/16 M x 8	16
256 MB	SS	256 Mbit	32 M x 8/empty	8
256 MB	SS	512 Mbit	32 M x 16/empty	4
512 MB	DS	256 Mbit	32 M x 8/32 M x 8	16
512 MB	SS	512 Mbit	64 M x 8/empty	8
1024 MB	DS	512 Mbit	64 M x 8/64 M x 8	16

Note: In the second column, “DS” refers to double-sided memory modules (containing two rows of DDR SDRAM) and “SS” refers to single-sided memory modules (containing one row of DDR SDRAM).

DIMM and memory configurations must adhere to the following:

- 2.5 V (only) 184-pin DDR SDRAM DIMMs with gold-plated contacts
- Unbuffered, single-sided or double-sided DIMMs with the following restriction:
- Double-sided DIMMS with x16 organization are not supported.
- Maximum total system memory: 4 GB
- Minimum total system memory: 128 MB
- ECC and non-ECC DIMMs supported
- Serial Presence Detect
- PC3200 (400 MHZ), PC2700 (333 MHZ), and PC2100 (266 MHZ) SDRAM DIMMs

Table 3 lists the supported system bus frequency and memory speed combinations.

Table 3. Supported System Bus Frequency and Memory Speed Combinations

To use this type of DIMM…	The processor's system bus frequency must be…
PC3200 (400 MHZ)	800 MHz
PC2700 (333 MHZ)	800 or 533 MHz (Note)
PC2100 (266 MHZ)	800, 533, or 400 MHz

Note: When using PC2700 (333 MHZ) memory with an 800 MHz system bus frequency processor, the memory channel will be set to 320 MHz.

Only DIMMs tested and qualified by Intel or a designated memory test vendor will be supported on the Intel Server Board SE7210TP1-E. A list of qualified DIMMs will be made available through http://support.intel.com/support/motherboards/server/SE7210TP1-E/. Note that all DIMMs are supported by design, but only fully qualified DIMMs will be supported.

NOTES

To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.

For ECC functionality, all installed DIMMs must be ECC. If both ECC and non-ECC DIMMs are used, ECC will be disabled and will not function.

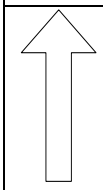
3.3.1 Memory Configurations

The Intel 827210 MCH component provides two features for enhancing memory throughput:

- Dual Channel memory interface. The board has two memory channels, each with two DIMM sockets.
- Dynamic Addressing Mode. Dynamic mode minimizes overhead by reducing memory accesses.

Table 4 summarizes the characteristics of dual and single channel configurations with and without the use of Dynamic Mode.

Table 4. Characteristics of Dual/Single Channel Configuration with/without Dynamic Mode

Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched (Example configurations are shown in Figure 5)
	Dual Channel without Dynamic Mode	DIMMs matched from Channel A to Channel B DIMMs not matched within channels (Example configuration is shown in Figure 6)
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched with a channel (Example configurations are shown in Figure 7)
Lowest	Single Channel without Dynamic Mode	DIMMs not matched (Example configurations are shown in Figure 8)

Dual Channel Configuration with Dynamic Mode
(All DIMMs Matched)

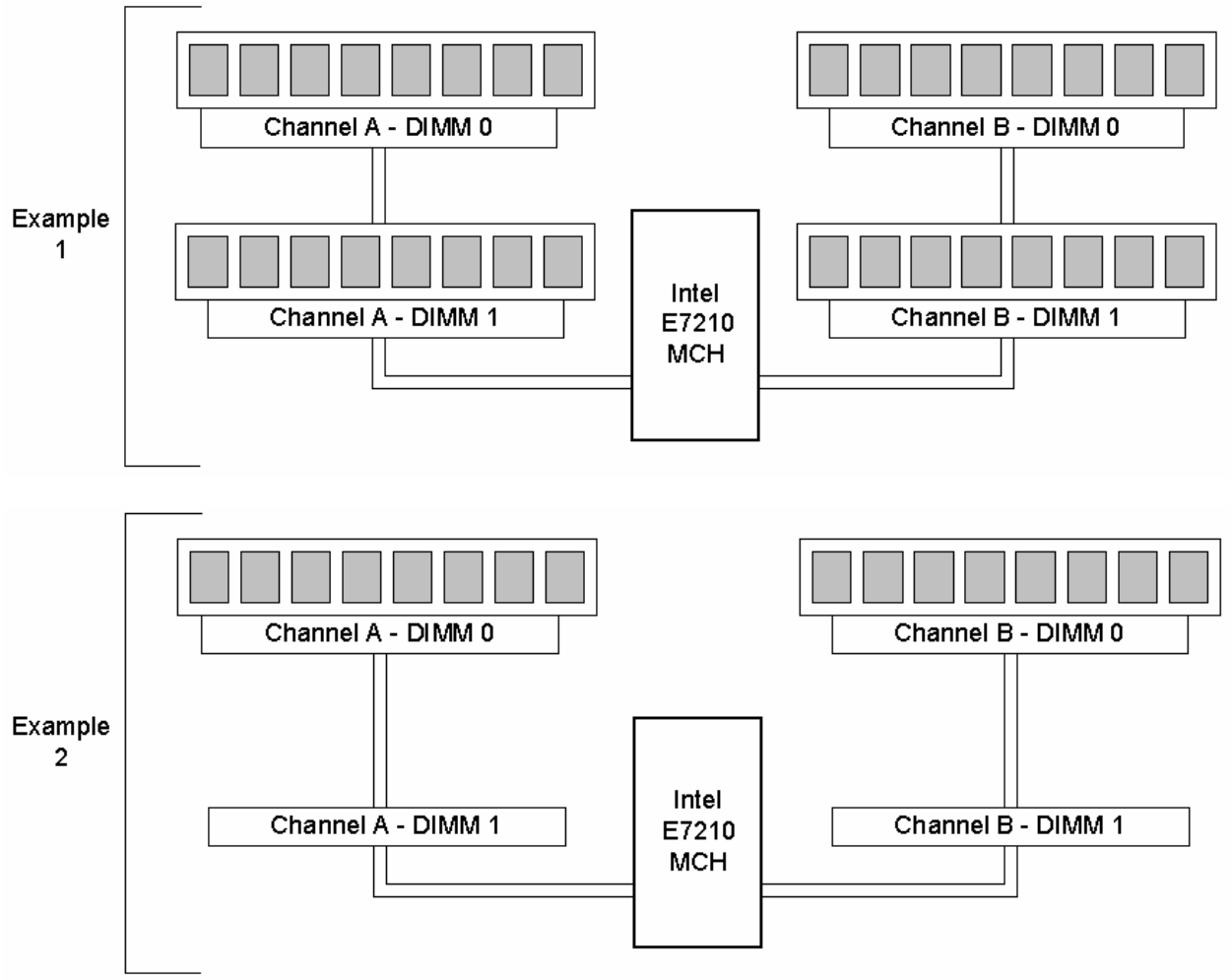


Figure 5. Examples of Dual Channel Configuration with Dynamic Mode

Dual Channel Configuration without Dynamic Mode
- DIMMs not matched within channel
- DIMMs match Channel A to Channel B

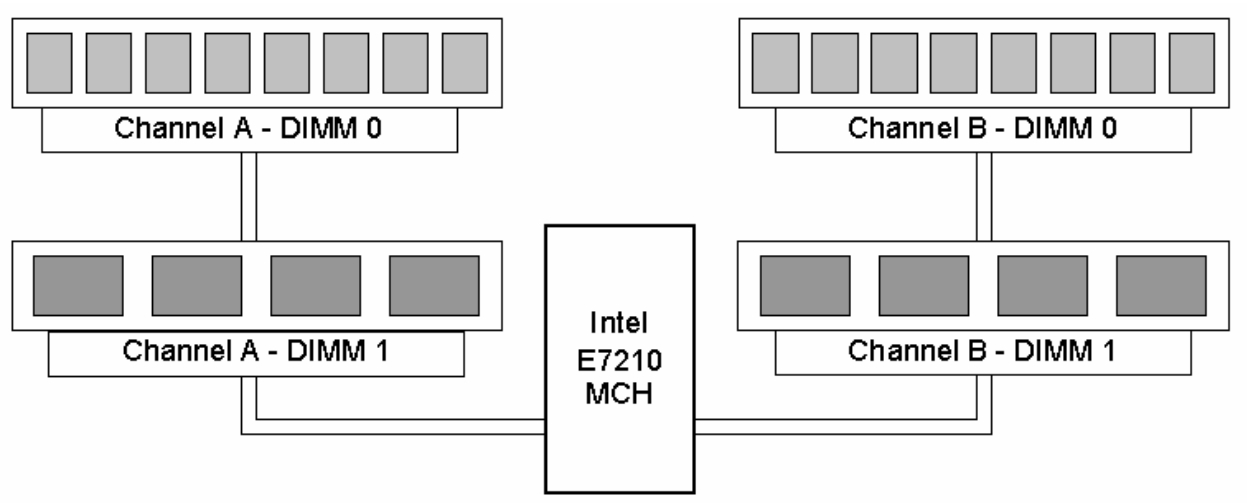


Figure 6. Example of Dual Channel Configuration without Dynamic Mode

Single Channel Configuration with Dynamic Mode
(Single DIMM or DIMMs matched within Channel)

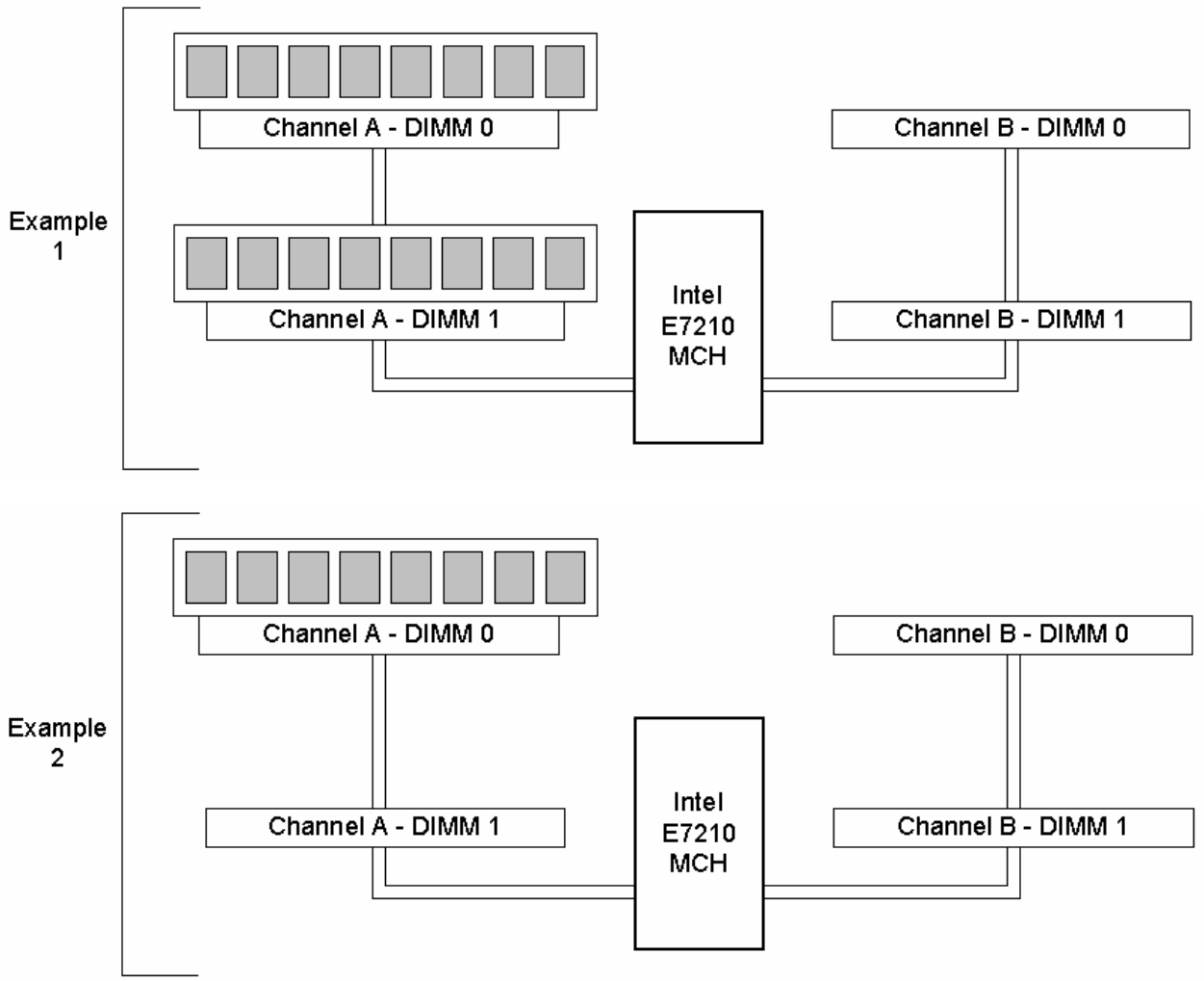


Figure 7. Examples of Single Channel Configuration with Dynamic Mode

Single Channel Configuration without Dynamic Mode
(DIMMs not matched)

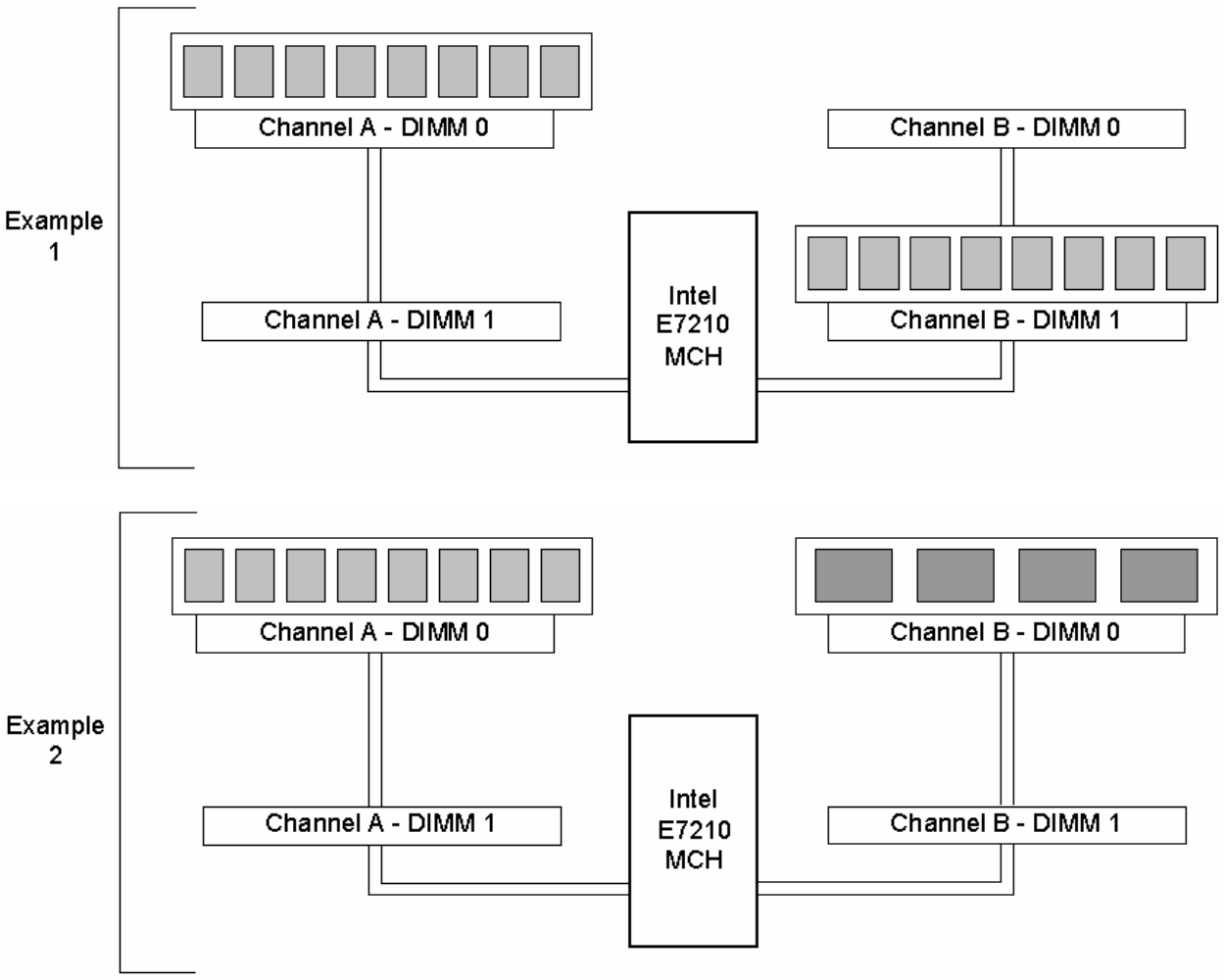


Figure 8. Examples of Single Channel Configuration without Dynamic Mode

3.4 I/O Sub-System

The I/O sub-system is made up of several components: the 6300ESB I/O providing the PCI-X interfaces for the three PCI slots and riser slot on board 3, the on-board SCSI controller, the on-board Ethernet controllers, the onboard video controller, Super IO chip, and Management Sub-system. This section describes the function of each I/O interface and how they operate on the SE7210TP1-E server board.

3.4.1 PCI Sub-System

The primary I/O bus for the Intel Server Board SE7210TP1-E is PCI, with two independent PCI buses. The PCI buses comply with the *PCI Local Bus Specification, Rev 2.2*. The PCI bus is directed through the Intel 6300ESB I/O Controller Hub. The table below lists the characteristics of the two PCI bus segments.

Table 5: PCI Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Speed	Type	PCI I/O Card Slots
P32-A	5 V	32-bits	33 MHz	PCI	1 - capable of supporting full-length PCI add-in cards. Internal component use.
P64-A	3.3 V	64-bits	66 MHz	PCI-X	3 - capable of supporting full-length PCI-X add-in cards
P64-A	3.3 V	64-bits	66 MHz	PCI-X	1 - riser slot supporting low-profile add-in cards (Only on board 3)

3.4.1.1 P32-A: 32-bit, 33MHz PCI Sub-system

All 32-bit, 33-MHz PCI I/O for the SE7210TP1-E server board is directed through the 6300ESB I/O. The 32-bit, 33-MHz PCI segment created by the 6300ESB I/O is known as the P32-A segment. The P32-A segment supports the following devices:

- One 32-bit PCI slot
- 2D/3D Graphics Accelerator: ATI Rage XL Video Controller
- SIO Chip: Winbond* W83627 HF-AW Super I/O
- Hardware monitoring sub-system: SMBUS.

3.4.1.2 P64-A: 64-bit, 66MHz PCI Subsystem

There is one 64-bit PCI-X bus segment directed through the 6300ESB I/O. P64-A supports the interface for the on-board Adaptec* 7901 Ultra 320 SCSI controller in addition to supporting up a maximum of three PCI slots.

3.4.1.3 Scan Order

The BIOS assigns PCI bus numbers in a depth-first hierarchy, in accordance with the *PCI Local Bus Specification*. When a bridge device is located, the bus number is incremented in exception

of a bridge device in the chipsets. Scanning continues on the secondary side of the bridge until all subordinate buses are defined. PCI bus numbers may change when PCI-PCI bridges are added or removed. If a bridge is inserted in a PCI bus, all subsequent PCI bus numbers below the current bus will be increased by one.

3.4.1.4 Resource Assignment

The resource manager assigns the PIC-mode interrupt for the devices that will be accessed by the legacy code. The BIOS will ensure the PCI BAR registers and the command register for all devices are correctly set up to match the behavior of the legacy BIOS. Code cannot make assumptions about the scan order of devices or the order in which resources will be allocated to them. The BIOS will support the INT 1Ah PCI BIOS interface calls.

3.4.1.5 Automatic IRQ Assignment

The BIOS automatically assigns IRQs to devices in the system for legacy compatibility. No method is provided to manually configure the IRQs for devices.

3.4.1.6 Option ROM Support

The option ROM support code in the BIOS will dispatch the option ROMs in available memory space in the address range 0C0000h-0DFFFFh and will follow all rules with respect to the option ROM space. The SE7210TP1-E BIOS will integrate option ROMs for the Intel 82547GI, Intel 82551QM, ATI Rage XL, SATA RAID and Adaptec 7901 SCSI controller.

3.4.1.7 Zero Channel RAID (ZCR) Capable Slot

The SCSI version of the Server Board SE7210TP1-E is capable of supporting the following zero channel RAID controllers, the Intel® RAID Controller SRCZCR and the Adaptec* ASR-2010S RAID adapter. ZCR cards are only supported in slot one the P64-A PCI segment.

The ZCR add-in cards leverage the on-board SCSI controller along with their own built-in intelligence to provide a complete RAID controller subsystem on-board. The riser card and baseboard use an implementation commonly referred to as RAID I/O Steering (RAIDIOS) specification version 0.92 to support this feature. If either of these supported RAID cards are installed, then the SCSI interrupts are routed to the RAID adapter instead of to the PCI interrupt controller. Also the IDSEL of the SCSI controller is not driven to the controller and thus will not respond as an on-board device. The host-based I/O device is effectively hidden from the system.

3.4.2 DMA Channels

Table 6. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	
4	8 or 16 bits	DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

3.4.3 Interrupts

The interrupts can be routed through the Advanced Programmable Interrupt Controller (APIC) portion of the 6300ESB I/O component. The APIC is supported in Windows* 2000 Server and Windows XP and supports a total of 24 interrupts.

Table 7. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
6	Diskette drive
8	Real-time clock
9	Reserved for 6300ESB I/O system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)
16	USB UHCI controller 1 (through PIRQA)
17	User available (through PIRQB)
18	6300ESB I/O USB controller 3 (through PIRQC)
19	6300ESB I/O USB controller 2 (through PIRQD)
20	6300ESB I/O LAN (through PIRQE)
21	User available (through PIRQF)
22	User available (through PIRQG)
23	6300ESB I/O USB 2.0 EHCI controller/User available (through PIRQH)

Notes:

1. Default, but can be changed to another IRQ.

3.4.4 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- **INTA**: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- **INTB**: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- **INTC** and **INTD**: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The 6300ESB I/O has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the Server Board SE7210TP1-E and therefore share the same interrupt. Table 8 shows an example of how the PIRQ signals are routed.

For example, using Table 8 as a reference, assume an add-in card using INTB is plugged into PCI bus connector 3. In PCI bus connector 3, INTB is connected to PIRQA, which is already connected to the Promise PDC20319 Controller. The add-in card in PCI bus connector 3 now shares an interrupt with the onboard interrupt source.

Table 8. PCI Interrupt Routing Map

IDSEL	P_AD18	PX_AD19	PX_AD20	PX_AD17	P_AD16	P_AD17	P_AD18
P_INTA*							INTA
P_INTB*						INTB	INTB
P_INTC*							INTC
P_INTD*							INTD
P_INTE*							PIN B2, INTE
P_INTF*					INTF		PIN B4, INTE
PX_INTA*	INTA	INTB	INTC				
PX_INTB*	INTB	INTC	INTD				
PX_INTC*	INTC	INTD	INTA				
PX_INTD*	SCSI_A*	INTA	INTB				
PX_IRQ*				IRQ3			
REQ/GNT	1	2	3	0	0	1	2
	PCI 64 bit SLOT1	PCI 64 bit SLOT2	PCI 64 bit SLOT3	SCSI	ATI RAGE	LAN 10/100	PCI 32 bit SLOT6

NOTE

In PIC mode, the 6300ESB I/O can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. See Table 7 for the allocation of PIRQ lines to IRQ signals in APIC mode.

3.4.5 SCSI Support

The SCSI sub-system consists of the Adaptec 7901 Single Channel, PC-2001-compliant PCI-X Ultra 320 SCSI controller which has one internal 80-pin connector (SCSI Channel A).

3.4.5.1 Adaptec 7901 Single Channel Ultra 320 SCSI Controller

The Adaptec 7901 is PCI bus master single-channel SCSI ASICs package. The Adaptec 7901 is an Ultra320 SCSI ASIC supporting a data transfer rate up to 320 MB/sec. The Adaptec 7901 complies with PCI Local Bus Specification, Revision 2.2 PCI-X Addendum, Rev. 1.0, and SCSI Parallel Interface-4 (SPI-4) for both Single-Ended (SE) and Low Voltage Differential (LVD) devices.

These ASICs comply with:

PCI Local Bus Specification, Revision 2.2
PCI-X Addendum, Revision. 1.0a
SCSI Parallel Interface-4 (SPI-4), Revision 6

For both Single-Ended (SE) and LVD devices. In addition, they comply with the SCSI-3 standard and provide multimode SCSI support.

In PCI and PCI-X modes, these ASICs can operate as a multifunction 32-bit or 64-bit bus master capable of supporting zero-wait-state 32- or 64-bit memory transfers. They can also function as a PCI or PCI-X target.

The Adaptec 7901 supports up to 64-bit, 122 MHz PCI-X bus. The Ultra320 SCSI features for the Adaptec 7901 include:

- Double-transition (DT) clocking
- Paced transfers using packetized protocol
- Packetized protocol
- Dual data FIFO
- Quick arbitration and selection/reselection (QAS) protocol
- Manual PIO mode data transfer
- Automatic mode data transfer
- Normal (DMA) mode data transfer
- Cyclic redundancy check (CRC) codes

The single-channel Adaptec 7901 delivers Ultra320 SCSI data rates up to 320 MBytes/sec to address emerging bandwidth hungry applications, such as real-time video, data mining, Internet/Intranet, and scientific modeling and simulation. The chip features a 66 MHz, 64-bit PCI interface and a 133 MHz, 64-bit PCI-X interface.

Migration to new Ultra320 SCSI technology is easy with the Adaptec 7901. It is backward compatible with Ultra320, Ultra160, Ultra2, and earlier SCSI generations. The chip is available in a 356-pin Thermally Enhanced Ball Grid Array (TEBGA) package, which is signal compatible with the Ultra160 SCSI Adaptec 7892 for a smooth upgrade to Ultra320 SCSI.

Now offered with the Adaptec 7901 is HostRAID*, an advanced RAID solution that includes hardware mirroring on the Adaptec 7901. HostRAID offers bootable RAID levels 0 and 1 with other advanced RAID features such as dedicated hot spares with automatic recovery, on-line capacity expansion, event scheduling, SAF-TE support, SNMP, DMI, and on-line RAID level migration.

The Adaptec 7901 uses Ultra320 technology to double Ultra160 data transfer rates up to 320 MBytes/sec. In addition, Adaptec Seamless Streaming* technology allows the Adaptec 7901 to take full advantage of the SCSI packet protocol enhancements (transfers multiple commands, data contexts and statuses in single connection) that replaces the legacy SCSI protocol (transfers single commands, data contexts or statuses per connection).

The Adaptec 7901 also supports Quick Arbitration and Selection (QAS) and SCSI arbitration fairness. QAS reduces the overhead of control release on the SCSI bus from one device to another. This improvement reduces command overhead and maximizes bus utilization. SCSI arbitration fairness prevents a device from dominating the bus by guaranteeing that all devices have an opportunity to arbitrate.

The Adaptec 7901 fully supports CRC for 16-bit SCSI synchronous data transfers. CRC detects data integrity errors that would not be detected by simple parity checking used by previous SCSI generations. The higher data rates achieved on existing Low Voltage Differential (LVD) cable configurations mandated this improved data integrity feature.

The Adaptec 7901 fully supports Domain Validation, which provides two levels (Basic and Enhanced) of SCSI bus configuration testing to help ensure Ultra320 and Ultra160 SCSI topologies operate at optimum speed.

Using Low Voltage Differential (LVD), each Adaptec 7901 channel supports a maximum of 15 devices on a 12-meter cable. In a point-to-point arrangement, cabling can extend to 25 meters.

The Adaptec 7901 incorporates an advanced multi-mode SCSI I/O cell that supports Ultra2, Ultra160, and Ultra320 SCSI LVD devices, as well as single-ended devices. With only Ultra2, Ultra160, and Ultra320 devices attached, the SCSI bus performs at full speed and full LVD cable lengths. When SE devices are attached, the bus defaults to SE speed and cable length.

3.4.5.1.1 Adaptec 7901 Summary of Features

The Adaptec 7901 contains the following SCSI performance features:

- SCSI data transfers up to 320 MB/sec
- 8- or 16-bit SCSI data path
- SCSI offsets to 254 transfers
- Advanced multimode I/O cell is compatible with LVD or SE devices
- Extensive hardware support for disconnect/reconnect and scatter/gather
- Full support for both initiator and target operations
- Full support for domain validation, which provides two levels (basic and enhanced) of SCSI bus configuration testing to help ensure Ultra320 and Ultra160 SCSI topologies operate at optimum speed
- Multiple target ID enables responses to multiple IDs as a SCSI target
- Full support for CRC for 16-bit SCSI synchronous data transfers. CRC detects data integrity errors that would not be detected by simple parity checking used by previous SCSI generations. The higher data rates achieved on existing LVD cable configurations mandated this improved data integrity feature.
- Supports Quick Arbitration and Selection (QAS) and SCSI arbitration fairness. QAS reduces overhead when bus control is transferred between devices. Arbitration fairness prevents devices from hogging the bus by guaranteeing each device a chance to arbitrate.
- Supports Seamless Streaming technology, which allows full implementation of SCSI packet protocol for sending many commands, receiving many statuses, and transferring data for many commands during one SCSI connection. There is virtually no delay between packets for different commands.

The Adaptec 7901 has a 133 MHz, 64-bit PCI/PCI-X Host Interface that supports the following PCI features:

- PC2001 compliant
- Direct pin connection to the PCI/PCI-X interface, from 133-MHz, 64-bit interface down to PCI 33-MHz, 32-bit interface
- Leading and trailing offset bytes on a 32- or 64-bit bus
- Performance-enhanced 32-bit operating mode allows 32-bit data transactions with 32- and 64-bit addressing (SAC/DAC)
- 3.3-V/5-V PCI and 3.3-V PCI-X interfaces provide flexibility for designing high performance, low-power systems
- PCI bus master and slave timing referenced to PCLK
- PCI bus-programmable Latency Timer, Cache Size, and Interrupt Line Select registers
- Supports external read access to the BIOS FLASH on the host bus adapter (HBA)
- Supports SEEPROM read and write word access with an Adaptec utility
- Medium PCI target device select response time
- Streaming PCI-enhanced master Direct Memory Access (DMA) read and write burst commands
- PCI bus address and data parity generation and checking
- Supports PCI PERR# and SERR# requirements
- Supports up to five outstanding split completions
- PCI bus address and data phase error generation for checking host and device error support

- PCI/PCI-X target latency of 16 clocks maximum for first target access cycle that transfers data and 8 clocks for other responses
- Supports wire interrupts and Message-Signaled Interrupts (MSI)
- Hardware-implemented endian support for command and scatter/gather data transfer to reduce driver translation overhead

3.4.5.2 Performance and Throughput

The Adaptec 7901 contain improved Adaptec RISC-based processors (ARPs) that execute SCSI Control Blocks (SCBs) to initiate data transfers between the PCI-X and SCSI interfaces. The ARPs support execution speeds of 40 MIPS and provide 8 KB of SRAM microcode storage.

These ASICs operate at up to 66 MHz in PCI mode with a maximum 533 MB/sec data burst rate.

3.4.5.3 PCI/PCI-X Mode Operation

Depending on the state of the initialization pattern on the PCI bus during power up, the Adaptec 7901 can be initialized to operate in either conventional PCI or PCI-X mode; both wire and message-signaled interrupts are supported.

3.4.5.4 PCI Bus

The Adaptec 7901 performance levels at 3.3 VIO are as follows:

- When operation in PCI-X mode as a 64-bit bus master, the Adaptec 7901 can support memory data transfer up to 533 MB/sec at 66 MHz.
- When operation in PCI-X mode as a 32-bit bus master, the Adaptec 7901 can support memory data transfer up to 266 MB/sec at 66MHz
- When operation in PCI-X mode as a 64-bit bus master, the Adaptec 7901 can support memory data transfer up to 266 MB/sec at 33MHZ
- When operation in PCI-X mode as a 32-bit bus master, the Adaptec 7901 can support memory data transfer up to 133 MB/sec at 33MHZ

3.4.5.5 SCSI Bus

The Adaptec 7901 can operate in SE or LVD mode, depending on the voltage level of the SCSI DIFFSENSE (F2), which is determined by the combination of the SCSI devices attached to the bus, the SCSI bus operates in SE mode and the SCSI data transfer rate is speed of the SCSI device currently transferring data.

Note: The Adaptec 7901 does not support High Voltage Differential (HVD) devices. When an HVD device is detected, the bus goes tri-state and transmission stops.

3.4.6 IDE Support

Integrated IDE controllers of the 6300ESB I/O provide two independent IDE channels, each capable of supporting up to two drives. A standard 40-pin IDE connector on the baseboard interfaces with both channels. Both IDE channels can be configured or enabled/disabled by accessing the BIOS Setup Utility during POST.

3.4.6.1 Ultra ATA/100

The IDE interfaces of the ICH5R DMA protocol redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 100 MB/s.

3.4.6.2 IDE Initialization

The BIOS supports the ATA/ATAPI Specification, version 6 or later. The BIOS initializes the embedded IDE controller in the chipset (ICH5R) and the IDE devices that are connected to these devices. The BIOS scans the IDE devices and programs the controller and the devices with their optimum timings. The IDE disk read/write services that are provided by the BIOS will use PIO mode, but the BIOS will program the necessary Ultra DMA registers in the IDE controller so that the operating system can use the Ultra DMA Modes.

3.4.7 SATA Support

The integrated Serial ATA (SATA) controller of the 6300ESB I/O provides two SATA ports on the baseboard. The SATA ports can be enabled/disabled and/or configured by accessing the BIOS Setup Utility during POST.

The SATA function in the 6300ESB I/O has dual modes of operation to support different operating system conditions. In the case of Native IDE enabled operating systems, the 6300ESB I/O has separate PCI functions for serial and parallel ATA. To support legacy operating systems, there is only one PCI function for both the serial and parallel ATA ports. The MAP register provides the ability to share PCI functions. When sharing is enabled, all decode of I/O is done through the SATA registers. Device 31, Function 1 (IDE controller) is hidden by software writing to the Function Disable Register (D31, F0, offset F2h, bit 1), and its configuration registers are not used. The SATA Capability Pointer Register (offset 34h) will change to indicate that MSI is not supported in combined mode.

The 6300ESB I/O SATA controller features two sets of interface signals that can be independently enabled or disabled. Each interface is supported by an independent DMA controller. The 6300ESB I/O SATA controller interacts with an attached mass storage device through a register interface that is equivalent to that presented by a traditional IDE host adapter. The host software follows existing standards and conventions when accessing the register interface and follows standard command protocol conventions.

SATA interface transfer rates are independent of UDMA mode settings. SATA interface transfer rates will operate at the bus's maximum speed, regardless of the UDMA mode reported by the SATA device or the system BIOS.

3.4.7.1 SATA RAID

The Adaptec HostRAID™ Technology solution, available with the 6300ESB I/O, offers data stripping for higher performance (RAID Level 0 and 1), alleviating disk bottlenecks by taking advantage of the dual independent SATA controllers integrated in the 6300ESB I/O. There is no loss of PCI resources (request/grant pair) or add-in card slot.

Adaptec HostRAID Technology functionality requires the following items:

- 6300ESB I/O
- Two SATA hard disk drives.

Adaptec Host RAID Technology is not available in the following configurations:

- The SATA controller in compatible mode.
- Adaptec Host RAID Technology has been disabled - D31:F0:AE bits [7:6] have been cleared

3.4.7.2 Adaptec Host RAID Technology Option ROM

HostRAID offers bootable RAID levels 0 and 1 with other advanced RAID features such as dedicated hot spares with automatic recovery, on-line capacity expansion, event scheduling, SAF-TE support, SNMP, DMI, and on-line RAID level migration.

3.4.8 Video Controller

The SE7210TP1-E server board provides an ATI* Rage XL PCI graphics accelerator, along with 8 MB of video SDRAM and support circuitry for an embedded SVGA video subsystem. The ATI Rage XL chip contains a SVGA video controller, clock generator, 2D and 3D engine, and RAMDAC in a 272-pin PBGA. One 2Mx32 SDRAM chip provides 8 MB of video memory.

The SVGA subsystem supports a variety of modes, up to 1600 x 1200 resolution in 8/16/24/32 bpp modes under 2D, and up to 1024 x 768 resolution in 8/16/24/32 bpp modes under 3D. It also supports both CRT and LCD monitors up to 100 Hz vertical refresh rate.

Video is accessed using a standard 15-pin VGA connector found on the back edge of the server board. On-board video can be disabled using the BIOS Setup Utility which is accessed during POST or when an add-in video card is installed in any of the PCI slots.

3.4.8.1 Video Modes

The Rage XL chip supports all standard IBM VGA modes. The following table shows the 2D/3D modes supported for both CRT and LCD.

Table 9: Video Modes

2D Mode	Refresh Rate (Hz)	SE7210TP1-E 2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
800x600	60, 70, 75, 90, 100	Supported	Supported	Supported	Supported
1024x768	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
1280x1024	43, 60	Supported	Supported	Supported	Supported
1280x1024	70, 72	Supported	–	Supported	Supported
1600x1200	60, 66	Supported	Supported	Supported	Supported
1600x1200	76, 85	Supported	Supported	Supported	–
3D Mode	**Refresh Rate (Hz)**	**SE7210TP1-E 3D Video Mode Support with Z Buffer Enabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	–	–
1600x1200	60,66,76,85	Supported	–	–	–
3D Mode	**Refresh Rate (Hz)**	**SE7210TP1-E 3D Video Mode Support with Z Buffer Disabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	Supported	–
1600x1200	60,66,76,85	Supported	Supported	–	–

3.4.8.2 Video Memory Interface

The memory controller subsystem of the Rage XL arbitrates requests from direct memory interface, the VGA graphics controller, the drawing coprocessor, the display controller, the video scalar, and hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

The SE7210TP1-E supports an 8 MB SDRAM device for video memory.

3.4.9 Network Interface Controller (NIC) Subsystem

The Intel Server Board SE7210TP1-E supports two Network Interface Controllers (NICs), one that runs at 10/100Mb and is based on the Intel 82551QM NIC and the other that runs at one gigabit and is based on the Intel 82547GI NIC. When looking at the rear of the chassis, the gigabit NIC is at the right (closest to the video port) and the 10/100Mb NIC is at the left. The

Intel Server Board SE7210TP1-E supports independent disabling of the two NIC controllers using the BIOS Setup menu.

The NIC subsystem consists of the following:

- Intel 82547GI Platform LAN Connect (PLC) device for 10/100/1000 Mbits/sec Ethernet LAN connectivity
- Intel 82551QM device for 10/100 Mbits/sec Ethernet LAN connectivity
- RJ-45 LAN connector with integrated status LEDs

The 82547GI is controlled by the CSA interface off of the MCH and supports the following features:

- Basic 10/100/1000 Ethernet LAN connectivity
- Integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY)
- IEEE 802.3 10BASE-T/100BASE-TX/1000BASE-T compliant physical layer interface
- IEEE 802.3ab Auto-Negotiation support
- Low power (less than 350mW in active transmit mode)
- Reduced power in “unplugged mode” (less than 50mW)
- Automatic detection of “unplugged mode”
- Communication Streaming Architecture (CSA) port provides higher throughput and lower latencies resulting in up to 30% higher bus throughput (up to wire speed)
- Full device driver compatibility
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address
- Teaming and Fail over support

The 82551QM is controlled by the 6300ESB I/O and supports the following features:

- Integrated IEEE 802.3 10BASE-T and 100BASE-TX compatible PHY
- 32-bit PCI/CardBus master interface
- Modem interface for combination solutions
- Integrated power management functions
- Full Duplex support at both 10 and 100 Mbps
- IEEE 802.3u Auto-Negotiation support
- 3 Kbyte transmit and 3 Kbyte receive FIFOs
- Fast back-to-back transmission support with minimum interframe spacing
- IEEE 802.3x 100BASE-TX Flow Control support
- Advanced Power management capabilities
- Low power 3.3 V device
- Efficient dynamic standby mode
- Deep power down support
- Clockrun protocol support

- Wired for Management support
- Integrated Alert on LAN* 2 Support
- ACPI and PCI Power Management standards compliance
- Wake on "interesting" packets and link status change support
- Remote power up support

Additional features of the NIC subsystem include:

- PCI bus master interface
- CSMA/CD protocol engine
- PCI power management
- Supports ACPI technology
- Supports LAN wake capabilities

3.4.9.1 RJ-45 LAN Connectors with Integrated LEDs

Two LEDs are built into each RJ-45 LAN connector (as shown in Figure 9). For the 82551QM NIC, the green LED indicates a link to the LAN and the green LED indicates the connection speed. Table 10 describes the LED states when the board is powered up and the 10/100 Ethernet LAN subsystem is operating.

Table 10. 10/100 Ethernet LAN Connector LEDs

LED	LED Color	LED State	Indicates
Left	Green	Off	10 Mbit/sec data rate is selected.
		On	100 Mbit/sec data rate is selected.
Right	Green	Off	LAN link is not established.
		On (steady state)	LAN link is established.
		On (brighter and pulsing)	The server is communicating with another computer on the LAN.

Table 11 describes the LED states when the board is powered up and the 10/100/1000 Mbits/sec LAN subsystem is operating.

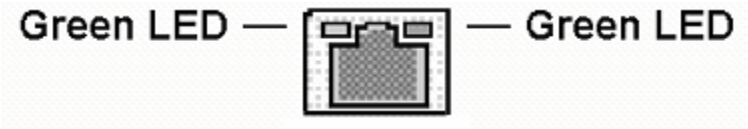


Figure 9. LAN Connector LED Locations

Table 11. 10/100/1000 LAN Connector LED States

LED	Color	LED State	Condition
Left	Green	Off	LAN link is not established.

		On (steady state)	LAN link is established.
		On (brighter and pulsing)	The server is communicating with another computer on the LAN.
Right	Green	Off	10 Mbit/sec data rate is selected.
		On	100 Mbit/sec data rate is selected.
	Orange	On	1000 Mbit/sec data rate is selected.

3.4.10 USB 2.0 Support

The USB controller functionality integrated into 6300ESB I/O provides the baseboard with the interface for up to four USB 2.0 ports. Three external connectors are located on the back edge of the baseboard. One internal 2x5 header is provided, capable of supporting an additional optional connector.

3.4.11 I/O Controller

The Winbond* W83627HF-AW I/O Controller provides the following features:

- Two serial ports
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.44 MB diskette drive
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
WINBOND W83627HF-AW I/O controller	http://www.Winbond.com

3.4.11.1 Serial Ports

The Intel Server Board SE7210TP1-E has one 9-pin D-sub serial port connector and one 2 x 5 serial port header. The serial port A connector is located in the rear I/O area. The serial port B header is located near serial port A. Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs.

For information about	Refer to
The signal names of the serial port A connector	Table 80
The location of the serial port B header	Figure 1
The signal names of the serial port B header	Table 81

3.4.11.2 Floppy Disk Controller

The floppy disk controller of the W83627HF-AW integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution.

For information about	Refer to
The location of the diskette drive connector	Figure 1
The signal names of the diskette drive connector	Section 7.9

3.4.11.3 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch* fuse circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the server should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the American MegaTrends* (AMI) keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

For information about	Refer to
The location of the keyboard and mouse connectors	Section 3.4.11.3
The signal names of the keyboard and mouse connectors	Table 82

3.4.11.4 Wake Up Control

The I/O controller contains functionality that allows various events to control the power-on and power-off the system.

3.5 Configuration and Initialization

This section describes the initial programming environment including address maps for memory and I/O, techniques and considerations for programming ASIC registers, and hardware options configuration.

3.5.1 Memory Space

Table 12. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 4194304 K	100000 - FFFFFFFF	4095 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to the PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)

512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

3.5.1.1 PCI Configuration Space Map

Table 13. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel E7210 component
00	01	00	
00	1E	00	Hub link to PCI bridge
00	1F	00	Intel 82801ER 6300ESB I/O PCI-to-LPC bridge
00	1F	01	IDE controller
00	1F	03	SMBus controller
00	1F	05	
00	1F	06	modem controller (optional)
00	1D	00	USB UHCI controller 1
00	1D	01	USB UHCI controller 2
00	1D	02	USB UHCI controller 3
00	1D	07	EHCI controller
01	00	00	
02	08	00	LAN controller
02	00	00	PCI bus connector 1
02	01	00	PCI bus connector 2
02	02	00	PCI bus connector 3
02	03	00	PCI bus connector 4
02	04	00	PCI bus connector 5
02	06	00	SATA/SATA RAID

3.5.2 I/O Map

Table 14. I/O Map

Address (hex)	Size	Description
0000 - 00FF	256 bytes	Used by the Server Board SE7210TP1-E. Refer to the 6300ESB I/O data sheet for dynamic addressing information.
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
0228 - 022F (Note 1)	8 bytes	
0278 - 027F (Note 1)	8 bytes	
02E8 - 02EF (Note 1)	8 bytes	COM4/video (8514A)
02F8 - 02FF (Note 1)	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port

Address (hex)	Size	Description
0378 - 037F	8 bytes	
03B0 - 03BB	12 bytes	Intel E7210 MCH
03C0 - 03DF	32 bytes	Intel E7210 MCH
03E8 - 03EF	8 bytes	
03F0 - 03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400	8 bytes	
0CF8 - 0CFB (Note 2)	4 bytes	PCI configuration address register
0CF9 (Note 3)	1 byte	Reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

3.5.2.1 Device Number and IDSEL Mapping

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD[31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows each IDSEL value for the PCI bus devices and the corresponding device description.

Table 15. PCI Bus Configuration IDs

IDSEL Value	Device
18	PCI slot 6 (closest to middle of the board)
20	PCI slot 3 (middle slot)
19	PCI slot 2 (middle slot)
18	PCI slot 1 (closest to left edge of board)
16	ATI Rage XL Video Controller
17	Single channel U320 controller Adaptec 7901

3.6 Clock Generation and Distribution

All buses on the SE7210TP1-E baseboard operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 66 MHz at 3.3 V logic levels: For the E7210, 6300ESB I/O and 82547GI clocks.
- 14.318 MHz at 3.3V logic levels: 6300ESB I/O and VGA
- 100/133-MHz host clock generator for processor, MCH, Memory DIMMs, and the ITP.
- 48-MHz clock for Super I/O and USB.
- 33.3-MHz PCI reference clock.

Note: The clock for memory DIMMs come from Intel® 827210 Memory Controller Hub (MCH).

4. System BIOS

This section details the functionality and features supported by the Intel® Server Board SE7210TP1-E Basic Input/Output System (BIOS), which is based on an AMI 8.0 core architecture. The BIOS is implemented as firmware that resides in a Flash ROM. It provides hardware-specific initialization algorithms and standard PC-compatible basic input/output (I/O) services, and standard Intel server board features. The Flash ROM also contains firmware for certain embedded devices.

The SE7210TP1-E BIOS is comprised of the following components:

- IA-32 core BIOS. This component contains most of the standard services and components found in an IA-32 system, such as the PCI Resource manager, ACPI support, POST, and RUNTIME functionality.
- Server BIOS extensions: Support for the National Semiconductor PC87431 integrated management controller and Intelligent Platform Management Interface (IPMI).
- Processor Microcode Updates: The BIOS also includes latest processor microcode updates.

The following table provides a list of all the features supported by the system BIOS.

Table 16: Supported BIOS Features

ID	Feature Name	Comments
	Support at least 128KB of available option space (C0000h ~ E0000h).	Support Option ROM available space in address (C0000h~DFFFFh - total 128K).
	Support Wired for Management specification as required to obtain WHQL compliance.	Now added to the Microsoft* Windows* Logo Program System and Device Requirements 2.0 document.
	PXE 2.1 (or higher) for on-board network controllers.	Both NIC controllers have: • PXE2.1 support • PXE optional ROM with no setup screen
	Support Boot Integrity Services (BIS). Security handshake on PXE.	
	UUID - UUID support (open standard in PXE environment).	UUID is written during manufacturing.
	Wake up	• RTC (real time clock): S1/S4 • PME: S1/S4/S5 • PS2 KB/MS: S1 • USB: S1 • Power button: S1/S4/S5
	USB Boot	USB boot support for USB 1.1/2.0 legacy compliant hard disk, CD-ROM, floppy drives, and disk-on-key.

ID	Feature Name	Comments
	Support for BIOS recovery.	• LS120/LS240 • USB bootable devices such as disk-on-key (USB 1.1/2.0) • USB CD-ROM(1.1/2.0) • ATAPI CD-ROM • ATAPI DVD • Support for legacy/USB floppy only due to BIOS image size (1MB).
	Legacy USB device support.	• Legacy USB KB/MS • Implemented by SMI
	Post Code/Port 80 Capture: Support POST Progress FIFO feature. Will be able to capture all POST Codes and Port 80 codes for debugging with onboard LEDs.	Supported via onboard LEDs. POST check points are logged in the National Semiconductor PC87431 integrated management controller.
	NMI dump switch support. Logging of NMI dump event.	• Front panel NMI button. • Operating system will log the dump data if NMI button is pressed.
	Power Switch Disable: Power switch can be disabled.	This is supported by the National Semiconductor PC87431 integrated management controller through IPMI commands.
	BIOS Boot Block: BIOS will have a segregated boot block enabling recovery of a corrupted BIOS. Will have BIOS Recovery Jumper.	Force BIOS recovery by jumper or when BIOS corruption is detected. Protect boot block by using the block lock feature built into the flash device.
	BIOS Update: Enable Flash BIOS update and allow updates from network drives in DOS and via PXE.	Support for CD-ROM, USB storage and network, except for floppy.
	Chassis intrusion detection.	LDCM will detect chassis intrusion state, and notify administrator via network.
	Hardware support for monitoring voltages, temperature, and fans.	Supported by National Semiconductor PC87431 integrated management controller.
	BIOS Setup will provide options to disable onboard I/O peripheral components (LAN components, Serial ATA, SCSI, etc.). When disabled, these components are to be completely removed from the PCI address space, making them invisible to any loaded operating system.	Must be able to disable embedded video (ATI* RAGE XL), SCSI (LSI* 53C1030), ICH5R serial ATA, and NIC controllers.
	BIOS Setup will provide options to disable/enable Option ROMs of onboard devices and PCI slots.	Enable/disable Option ROMs by BIOS setup.
	Ability to store error events in non-volatile space.	System stores events via National Semiconductor PC87431 integrated management controller.
	Support for Split Option ROM, based on PCI-SIG PCI Firmware Specification Revision 3.0.	
	Active thermal management to minimize noise at the system level. Will adhere to acoustic specifications.	Supported via the National Semiconductor PC87431 integrated management controller.
	Factory Automation support. This includes the ability to upgrade/update FW, BIOS, CMOS settings, OEM splash screen image, FRU/SDR and HSC code remotely (over a LAN) using automated tools in a volume production environment.	
	NMI detection. Ability to detect parity/system errors on all PCI buses. Ability to detect single/double bit errors.	

ID	Feature Name	Comments
	Support for the sleep button.	
	Support for clear password by jumper.	
	Support for clear CMOS by jumper.	
	Support for IPMP1.5.	National Semiconductor PC87431 integrated management controller only.
	Support for Intel diagnostic LEDs.	
	Support for serial console redirection.	COM A / COM B
	Support for LAN console redirection.	Intel 82546GI
	Support for FRU LEDs.	
	Support for FRB1 / FRB2.	
	Support for memory.	DDR266/DDR333/DDR400 supported. Max memory size: 4GB
	CPU Support.	• Hyper-threading: enable/disable by BIOS setup. • CPU microcode update during POST. • CPU micro code update during runtime: POST and runtime (Int 15h, AX= 0D042h). • Allow variable size microcode update (maximum microcode size is 16KB).
	Support for BBS.	BBS Rev. 1.02
	Support for PCI.	• PCI • PCI-X • PCI-X DDR
	Support for MPS (APIC mode).	MPS 1.4 (MPS table)
	Support for PIC mode.	PCI IRQ routing table
	Support for ACPI.	• ACPI 2.0 / 1.0b • S0/S1/S4/S5 • ACPI SPCR (Serial Port Console Redirection) table
	Support for SMBIOS.	SMBIOS 2.3.1, below 1 MB in memory.
	Support for keyboard and mouse swap.	AMI firmware
	BIOS warning messages in English, assuming video is available instead of beep codes.	
	Multi-language ready.	English, French, Spanish, Italian, German
	Support for security.	• PS/2 KB and MS lock • Floppy write protection • Password protection
	Support for boot.	• Quiet boot during POST • Quick boot during POST • Console-free boot • Boot menu
	Support for Alliance BIOS Specification V2.0.	
	Windows BIOS update utility.	
	Server Management	
	Power control in any state (operating system up, down, hung).	Supported by the National Semiconductor PC87431 integrated management controller.

ID	Feature Name	Comments
	Sensor monitoring and fault alerting while operating system is present.	Supported by the National Semiconductor PC87431 integrated management controller.
	Fault alerting via local or via LAN while operating system present.	Supported by the National Semiconductor PC87431 integrated management controller.
	IPMI / DMI / CIM compliant.	• IPMI 1.5, DMI, and CIM • Full IPMI 1.5 for server module • Subset of IPMI 1.5 for onboard National Semiconductor PC87431 integrated management controller.
	Integration with ISM software.	
	Security features to protect unwanted tampering of the server.	LDCM provides chassis intrusion and hardware and software change reporting.

4.1 BIOS Identification String

The BIOS Identification string is used to uniquely identify the revision of the BIOS being used on the system. The string is formatted as follows:

BoardId.OEMID.BuildType.Major.Minor.BuildID.BuildDateTime

where:

BoardID = up to 10 character ID. SE7210TP10
OEMID = 3 character OEM ID. 86B is used for Intel EPSD.
BuildType = where xx=2 digit number and:
Dxx = Development
Xxx = Power On
Axx = Alpha BIOS
Bxx = Beta BIOS
RCxx = Release Candidate
Pxx = Production
Major = The major revision identifies the feature set corresponding to this BIOS release.
Minor = The minor revision identifies the feature set corresponding to this BIOS release.
BuildID = 4 decimal digit build number, starting with "0000".
BuildDateTime = Build date and time in MMDDYYYYHHMM format.

4.2 Flash ROM

The Intel 82802AC Firmware Hub (FWH) includes an 8 megabit symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable.

4.2.1 Removable Media Support

The BIOS supports removable media devices, including 1.44MB floppy removable media devices and optical devices such as a CD-ROM drive or DVD drive. The BIOS supports booting from USB mass storage devices connected to the chassis USB port, such as a USB key device.

The BIOS supports USB 2.0 media storage devices that are backward compatible to the USB 1.1 specification.

4.2.2 Legacy USB

Legacy USB support enables USB devices such as keyboard, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When the user applies power to the server, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing the user to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboard and mice are recognized and may be used to configure the operating system. (Keyboard and mice are not recognized during this period if Legacy USB support was set to disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

⟹ NOTE

Legacy USB support is for keyboard, mice, and hubs only. Other USB devices are not supported in legacy mode.

4.3 Resource Configuration

4.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be on-board or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card. Autoconfiguration information is stored in ESCD format.

4.3.2 PCI IDE Support

If Auto is selected from the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance.

To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. The user can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTES

ATA-66/100 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an ATA-66/100 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate between the drives is reduced to that of the slowest device.

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

4.4 System Management BIOS (SMBIOS)

SMBIOS is a Server Management Interface (SMI) compliant method for managing servers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows* NT, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

4.5 BIOS Updates

The BIOS can be updated with the AMI Flash Utility (AFUDOS.exe), which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM. Please refer to the SE7210TP1-E BIOS EPS for details.

It supports the following BIOS maintenance functions:

- Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.
- Updating both the BIOS boot block and the main BIOS. This process is fault tolerant to prevent boot block corruption.
- Changing logo utility.

⟹ NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

4.6 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is video support. The user can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the AMI Flash Utility are available from Intel Customer Support through the Intel World Wide Web site.

⟹ NOTE

Even if the server is configured to boot from an LS-120 diskette (in the Setup program's Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

4.7 BIOS POST

The BIOS supports one system splash screen. When the system is booting, the BIOS will display the splash screen instead of BIOS messages. BIOS messages can be viewed by pressing the 'ESC' key during POST. Once the BIOS POST message screen is selected, the splash screen is no longer accessible during the current boot sequence. The splash screen can be customized by with the 'Change Logo' utility. Refer to the *Change Logo for AMIBIOS User's Guide* (Version 2.22) for details.

4.7.1 User Interface

There are two types of consoles used for displaying the user interface: graphical or text based. Graphics consoles are in 640x480x8bpp mode; text consoles are 80x25.

Console output is partitioned into three areas: the System Activity/State, Logo/Diagnostic, and Current Activity windows. The System Activity Window displays information about the current state of the system, such as if it is active, hung, or requires user intervention. The Logo/Diagnostic Window displays the OEM splash screen logo or a diagnostic boot screen. The Current Activity Window displays information about the currently executing portion of POST as well as user prompts or status messages.

If the CMOS is corrupt, the BIOS displays the following message:

```
"Press F1 to load default values and continue

 Press F2 to run SETUP".
```

The BIOS always wait until <F1> or <F2> is pressed; Or always not wait if [POST Error Pause] is set disabled in BIOS setup.

The BIOS displays the following information during POST:

- Copyright message
- BIOS ID
- Current processor configuration
- Installed physical memory size
- Current activity and user intervention

4.8 BIOS Setup Utility

The BIOS Setup utility is provided to perform system configuration changes and to display current settings and environment information.

The BIOS Setup utility stores configuration settings in system non-volatile storage. Changes affected by BIOS Setup will not take effect until the system is rebooted. The BIOS Setup Utility can be accessed when prompted during POST by using the F2 key.

4.8.1 Localization

The BIOS Setup utility uses the Unicode standard and is capable of displaying setup forms in the languages currently included in the Unicode standard: English, French, Italian, German, and Spanish. Intel provides translations for console strings in the supported languages. The language can be selected using the BIOS user interface.

4.8.2 Keyboard Commands

The Keyboard Command Bar supports the following:

Table 17: BIOS Setup Keyboard Command Bar Options

Key	Option	Description
Enter	Execute Command	The Enter key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected option has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu.
ESC	Exit	The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered. When the ESC key is pressed in any sub-menu, the parent menu is re-entered. When the ESC key is pressed in any major menu, the exit confirmation window is displayed and the user is asked whether changes can be discarded. If “No” is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before ESC was pressed without affecting any existing any settings. If “Yes” is selected and the Enter key is pressed, setup is exited and the BIOS continues with POST.
↑	Select Item	The up arrow is used to select the previous value in a pick list, or the previous options in a menu item's option list. The selected item must then be activated by pressing the Enter key.
↓	Select Item	The down arrow is used to select the next value in a menu item’s option list, or a value field’s pick list. The selected item must then be activated by pressing the Enter key.
↔	Select Menu	The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed.
Tab	Select Field	The Tab key is used to move between fields. For example, Tab can be used to move from hours to minutes in the time item in the main menu.

Key	Option	Description
-	Change Value	The minus key on the keypad is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list.
+	Change Value	The plus key on the keypad is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list. On 106-key Japanese keyboards, the plus key has a different scan code than the plus key on the other keyboard, but will have the same effect
F9	Setup Defaults	Pressing F9 causes the following to appear: Setup Confirmation Load default configuration now? [Yes] [No] If “Yes” is selected and the Enter key is pressed, all Setup fields are set to their default values. If “No” is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before F9 was pressed without affecting any existing field values
F10	Save and Exit	Pressing F10 causes the following message to appear: Setup Confirmation Save Configuration changes and exit now? [Yes] [No] If “Yes” is selected and the Enter key is pressed, all changes are saved and Setup is exited. If “No” is selected and the Enter key is pressed, or the ESC key is pressed, the user is returned to where they were before F10 was pressed without affecting any existing values.

4.8.3 Entering BIOS Setup

The BIOS Setup utility is accessed by pressing the <F2> hotkey during POST.

4.8.4 Menu Selection

The first screen displayed when entering the BIOS Setup Utility is the Main Menu selection screen. This screen displays the major menu selections available. The following tables describe the available options on the top-level and lower level menus. Default values are highlighted.

4.8.4.1 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

Main	Advanced	Boot	Security	Server	Exit

Table 18 describes the BIOS setup main menu options. This menu reports processor and memory information and is for configuring the system date and system time.

Table 18: BIOS Setup Main Menu Options

Feature	Options	Description
Server BIOS: Version Build Date ID	• No option	BIOS version, date and ID
Processor: Type Speed Count	• No option	CPU type, speed, count
System Memory: Size	• No option	Memory Size
System time	• Current time	Displays the current time.
System date	• Current date	Displays the current date.

4.8.4.2 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

Table 19 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

Table 19. Advanced Menu

Feature	Options	Description
>CPU Configuration	• Submenu	CPU Configuration.
>IDE Configuration	• Submenu	Configure the IDE device(s).
>Floppy Configuration	• Submenu	Configure the Floppy drive(s).
>Super I/O Configuration	• Submenu	Configure Super I/O Chipset Win627.
>USB Configuration	• Submenu	Configure the USB support.
>PCI Configuration	• Submenu	Configure the PCI support.

4.8.4.3 CPU Configuration Submenu

To access this submenu, select Advanced on the menu bar, then CPU Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

The submenu represented by Table 20 is for configuring the CPU.

Table 20. CPU Configuration Submenu

Feature	Options	Description
Manufacturer	• No options	CPU Manufacturer
Brand String	• No options	CPU Brand String
Frequency	• No options	CPU Frequency
FSB Speed	• No options	FSB Speed
CPU ID	• No options	CPU stepping identification
Cache L1	• No options	Display Cache L1 size
Cache L2	• No options	Display Cache L2 size
Max CPUID Value Limit	• Disable (default) • Enable	This should be enabled order to boot legacy OSes that cannot support CPUs with extended CPUID functions.
Hyper Threading Technology	• Disable • Enable (default)	This option is only available if the installed CPU is capable of Hyper Threading Technology support.

4.8.4.4 IDE Configuration Submenu

To access this submenu, select Advanced on the menu bar, then IDE Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

The submenu represented by Table 21 is for IDE Configuration.

Table 21. IDE Configuration Submenu

Feature	Options	Description
ATA Configuration	• [DISABLE PATA/SATA] • [CONFIG PATA & SATA] (default) • [CONFIG SATA ATA] • [LEGACY ATA CONFIG • [ENABLE SATA RAID]	Select ATA mode to change bellow ATA configuration.
Map PATA to Legacy ATA, Config SATA.	• Submenu	The item will be present when selecting CONFIG PATA & SATA in ATA Configuration.
Map SATA to Legacy ATA, Disable PATA	• Submenu	The item will be present when selecting CONFIG SATA ATA in ATA Configuration.
Map PATA & SATA to Legacy ATA	• Submenu	The item will be present when selecting LEGACY ATA CONFIG in ATA Configuration.
Enable SATA RAID, & Map PATA to Legacy ATA	• Submenu	The item will be present when selecting ENABLE SATA RAID in ATA configuration.
>Primary IDE Master	• Submenu	When BIOS auto detects the presence of IDE devices, Setup will display the status of auto-detection of IDE devices.
>Primary IDE Slave	• Submenu	
>Secondary IDE Master	• Submenu	
>Secondary IDE Slave	• Submenu	
>Third IDE Master	• Submenu	
	•	
>Fourth IDE Master	• Submenu	
	•	
Hard Disk Write Protect	• Disable (default) • Enable	Enable write protection.

Feature	Options	Description
IDE Detect Time Out (Sec)	• 0 • 5 • 10 • 15 • 20 • 25 • 30 • 35(default)	Select time out value for ATA/ATAPI.
ATA (PI) 80Pin Cable Detection	• Host & Device (default) • Host • Device	Select the mechanism for detecting 80pin ATA.

4.8.4.4.1 Map PATA to Legacy ATA, Config SATA Sub-menu Selections

To access this menu, select Advanced on the menu bar, then IDE Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

The submenu represented by Table 22 is used to configure the IDE Configuration.

Table 22. Primary/Secondary/Third/Fourth Master/Slave Submenu

Feature	Options	Description
SATA Control Enhanced	• Enabled (default) • Disabled	If enabled, PATA ports may use the primary and/or secondary ATA channel addresses and the SATA ports are limited to using the third and fourth ATA channel addresses. If disabled, the SATA ports are not available.
P-ATA Channel Selection	• Primary • Secondary • Both (default)	Selection determines assignment of only primary, only secondary or both ATA channel addresses for the PATA ports.
S-ATA Ports Definition	• A1-3rd, A2-4th. (default) • A1-4th, A2-3rd.	This option allows swapping of port mappings between the third and fourth ATA channels for the SATA ports.

4.8.4.4.2 Map SATA to Legacy ATA, Disable PATA Sub-menu Selections

To access this menu, select Advanced on the menu bar, then IDE Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

The submenu represented by Table 23 is used to configure the IDE Configuration.

Table 23. Primary/Secondary/Third/Fourth Master/Slave Submenu

Feature	Options	Description
S-ATA Ports Definition	• A1-PRI, A2-SEC. (default) • A1-SEC, A2-PRI.	This option allows swapping of port mappings between the third and fourth ATA channels for the SATA ports.

4.8.4.4.3 Map PATA & SATA to Legacy ATA Sub-menu Selections

To access this menu, select Advanced on the menu bar, then IDE Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

The submenu represented by Table 24 is used to configure the IDE Configuration.

Table 24. Primary/Secondary/Third/Fourth Master/Slave Submenu

Feature	Options	Description
Combined Mode Option	• PATA-PRI, SATA-SEC. (default) • PATA-SEC, SATA-PRI	The PATA port is assigned the primary or secondary ATA channel addresses; the SATA port is assigned the remaining channel address.

4.8.4.4.4

4.8.4.4.5 Enable SATA RAID, & Map PATA to Legacy ATA Sub-menu Selections

To access this menu, select Advanced on the menu bar, then IDE Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

The submenu represented by Table 25 is used to configure the IDE Configuration.

Table 25. Primary/Secondary/Third/Fourth Master/Slave Submenu

Feature	Options	Description
P-ATA Channel Selection	• Primary • Secondary • Both (default)	Selection determines assignment of only primary, only secondary or both ATA channel addresses for the PATA ports.

4.8.4.4.6 Primary/Secondary/Third/Fourth Master/Slave Submenu*s*

To access these submenus, select Advanced on the menu bar, then Drive Configuration, and then the master or slave to be configured.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration>DMI Event Logging				
	>PCI Configuration>USB Configuration				

There are four IDE submenus: primary master, primary slave, secondary master, and secondary slave. Table 26 shows the format of the IDE submenus. For brevity, only one example is shown.

Table 26. Primary/Secondary/Third/Fourth Master/Slave Submenu

Feature	Options	Description
Type	• Not Installed • Auto (default) • CDROM • ARMD	Select the type of device connected to the system.

Feature	Options	Description
LBA/Large Mode	• Auto (default) • Disable	Enable LBA Mode if the device supports it.
Block Mode	• Disabled • Auto (default)	This option can be changed only if User is selected as the type.
PIO Mode	• Auto (default) • 0 • 1 • 2 • 3 • 4	This option can be changed only if User is selected as the type.
S.M.A.R.T	• Auto (default) • Disabled • Enabled	This option can be changed only if User is selected as the type. If Auto is selected, this option is not displayed. Enables or disables Self-monitoring, Analysis, and Reporting Technology.
32Bit Data Transfer	• Disabled (default) • Enabled	Enable 32-bit Data Transfer.

4.8.4.5 Floppy Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Floppy Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

The submenu represented in Table 27 is the Floppy Configuration Submenu.

Table 27. Floppy Configuration Submenu

Feature	Options	Description
Floppy A	• Disabled • 720 KB 3½ inch • 1.44 MB 3½ inch (default) • 2.88 MB 3½ inch	Specifies the capacity and physical size of diskette drive A. Note: 720Kb & 2.88Mb drives will be as “Untestable”.
Onboard floppy controller	• Disable • Enable	

4.8.4.6 Super I/O Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Super I/O Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

The menu represented in Table 28 is used to configure Super I/O options.

Table 28. Super I/O Configuration Submenu

Feature	Options	Description
Serial PortA Address	• Disable • 3F8/IRQ4 (default) • 3E8/IRQ4 • 2E8/IRQ3	Allow BIOS to select serial Port 1 base Addresses.
Serial PortB Address	• Disable • 2F8/IRQ3 (default) • 3E8/IRQ4 • 2E8/IRQ3	Allow BIOS to select serial Port 1 base Addresses.

4.8.4.7 USB Configuration Submenu

To access this menu, select Advanced on the menu bar, then USB Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

The submenu represented by Table 29 is used to configure the USB features.

Table 29. USB Configuration Submenu

Feature	Options	Description
USB Devices Enabled	• NO option	USB device numbers.
USB Function	• Disable • 2 USB Ports • All USB Ports (default)	Enable USB HOST control.
Legacy USB Support	• Enable (default) • Disable • Auto	Support legacy USB.
Port 64/60 Emulation	• Enable • Disable (default)	This option is typically not used since most OSes are now USB-aware.
USB 2.0 Controller	• Enable (default) • Disable	Support USB2.0.
USB 2.0 Controller mode	• FullSpeed • HiSpeed (default)	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps). When USB 2.0 Controller is disabled, it will disappear
USB Beep Message	• Enable (default) • Disable	Enables the beep during USB device enumeration.
USB Mass Storage Device Configuration	• Submenu	Configure the USB Mass Storage Device Class. Only available when USB Mass Storage Device detected in system.

4.8.4.7.1 BIOS Setup USB Mass Storage Device Configuration Sub-menu Selections

Table 30. USB Mass Storage Device Configuration Sub-menu Selections

Feature	Options	Help Text	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.	
Device #1	N/A	N/A	Only displayed if a device is detected, includes a DeviceID string returned by the USB device.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto is selected, USB devices less than 530MB will be emulated as Floppy drives and the remaining as hard drives. The Forced FDD option will force a formatted HDD to boot as a FDD (Ex. ZIP drive).	

Device #n	N/A	N/A	Only displayed if a device is detected, includes a DeviceID string returned by the USB device.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto is selected, USB devices less than 530MB will be emulated as Floppy drives and the remaining as hard drives. The Forced FDD option will force a formatted HDD to boot as a FDD (Ex. ZIP drive).	

4.8.4.8 PCI Configuration Submenus

To access this submenu, select Advanced on the menu bar, then PCI Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
	>CPU Configuration				
	>IDE Configuration				
	>Floppy Configuration				
	>Super I/O Configuration				
	>USB Configuration				
	>PCI Configuration				

The submenu represented in Table 31 is used for PCI Configuration Submenu.

Table 31. PCI Configuration Submenu

Feature	Options	Description
Onboard Video	• Enable (default) • Disable	
Onboard NIC1	• Enable (default) • Disable	
NIC1 PXE	• Enable • Disable (default)	
Onboard NIC2	• Enable (default) • Disable	
NIC2 PXE	• Enable • Disable (default)	
Slot 1 Option ROM	• Enable (default) • Disable	No such item in SKU3,4
Slot 2 Option ROM	• Enable (default) • Disable	No such item in SKU3,4
Slot 3 Option ROM	• Enable (default) • Disable	No such item in SKU3,4
Slot 4 Option ROM	• Enable (default) • Disable	No such item in SKU3,4

4.8.5 BOOT menu

To access this menu, select Exit from the menu bar at the top of the screen.

Main	**Advanced**	Boot	Security	Server	Exit
		>Boot Settings Configuration			
		>Boot Device Priority			
		>Hard Disk Drives			
		>Removable Drives			
		> CD/DVD Drives			

The menu represented by Table 32 is for Boot features.

Table 32. Boot Features

Feature	Options	Description
>Boot Settings Configuration	• Submenu	Configuration Settings during boot.
>Boot Device Priority	• Submenu	Boot device priority sequence.
>Hard Disk Drives	• Submenu	Boot device priority sequence from available driver.
>Removable Drives	• Submenu	Boot device priority sequence from available removable driver.
>CD/DVD Drives	• Submenu	Boot device priority sequence from available ATAPI CDROM driver.

4.8.5.1 Boot Settings Configuration Submenu

To access this menu, select Boot on the menu bar, then Boot Settings Configuration

Main	**Advanced**	Boot	Security	Server	Exit
		>Boot Settings Configuration			
		>Boot Device Priority			
		>Hard Disk Drives			
		>Removable Drives			
		>CD/DVD Drives			

The submenu represented by Table 33 is for Boot Settings Configuration.

Table 33. Boot Settings Configuration Submenu

Feature	Options	Description
Quick Boot	• Enable (default) • Disable	Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.

Feature	Options	Description
Quiet Boot	• Enable (default) • Disable	Displays OEM Logo instead of POST messages.
AddOn ROM Display Mode	• Force BIOS (default) • Keep Current	Set display mode for Option ROM.
Bootup Num-Lock	• Off • On (default)	Select Power-on state for Numlock.
PS/2 Mouse Support	• Enable • Disable • Auto (default)	Select support for PS/2 Mouse.
POST Error Pause	• Enable (default) • Disable	If enabled, the system will wait for user intervention on critical POST errors. If disabled, the system will boot with no intervention, if possible.
Hit <F2> Message Display	• Enable (default) • Disable	Displays "Press <F2> to run Setup" in POST.
Extended Memory Test	• 1 MB • 1 KB • Every Location • Disabled (default)	Extended Memory Test Tests extended memory - Once per KB, or - Once per MB, or - Every location or - Disable Enabling this option disables Quiet Boot.
Scan User Flash Area	• Enable • Disable (default)	Allows BIOS to scan the Flash ROM for user binaries.

4.8.5.2 Boot Device Priority Submenu

To access this menu, select Boot on the menu bar, then Boot Device Priority Configuration.

Main	**Advanced**	Boot	Security	Server	Exit
		>Boot Settings Configuration			
		>Boot Device Priority			
		>Hard Disk Drives			
		>Removable Drives			
		> CD/DVD Drives			

The submenu represented by Table 34 is for Boot Device Priority.

Table 34. Boot Device Priority Submenu

Feature	Options	Description
1st Boot Device	• Varies	Number of entries will vary based on system configuration.
nth Boot Device	• Varies	Number of entries will vary based on system configuration.

4.8.5.3 Hard Disk Drives submenu

To access this menu, select Boot on the menu bar, then Hard Disk Drives.

Main	**Advanced**	Boot	Security	Server	Exit
		>Boot Settings Configuration			
		>Boot Device Priority			
		>Hard Disk Drives			
		>Removable Drives			
		>CD/DVD Drives			

The submenu represented by Table 35 is for Boot Device Priority.

Table 35. Boot Disk Drives Submenu

Feature	Options	Description
1st~15th Boot Device	• Option	Specifies the boot sequence from the available devices

4.8.5.4 Removable Drives Submenu

To access this menu, select Boot on the menu bar, then Removable Drives.

Main	**Advanced**	Boot	Security	Server	Exit
		>Boot Settings Configuration			
		>Boot Device Priority			
		>Hard Disk Drives			
		>Removable Drives			
		>CD/DVD Drives			

The menu represented in Table 36 is for Removable Drives.

Table 36. Removable Drives Submenu

Feature	Options	Description
1st Device	• Varies	Varies based on system configuration.
nth Device	• Varies	Varies based on system configuration.

4.8.5.5 CD/DVD Drives Submenu

To access this menu, select Boot on the menu bar, then CD/DVD Drives.

Main	**Advanced**	Boot	Security	Server	Exit
		>Boot Settings Configuration			
		>Boot Device Priority			
		>Hard Disk Drives			
		>Removable Drives			
		>CD/DVD Drives			

The submenu represented in Table 37 is for setting the CD/DVD Drives.

Table 37. CD/DVD Drives Submenu

Feature	Options	Description
1st Device	• Varies	Varies based on system configuration.
nth Device	• Varies	Varies based on system configuration.

4.8.6 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Main	Advanced	Boot	**Security**	Server	Exit

The menu represented in Table 38 is for Security features.

Table 38. Security Menu

Feature	Options	Description
Change Supervisor Password	• No options	Set password to null to clear.
Change User Password	• No options	Set password to null to clear.
Clear User Password	• no options	Immediately clears the User Password.
Boot Sector Virus Protection	• Enable • Disable (default)	Enable/Disable Boot Sector Virus Protection.
Diskette Write Protect	• Enable • Disable (default)Enable	Disables/Enables diskette driver write protection.
NMI Control	• Enable • Disable (default)	Enable/Disable NMI control through the National Semiconductor PC87431 Integrated Management Controller for the front panel NMI button.

4.8.7 Server Menu

To access this menu, select Server from the menu bar at the top of the screen.

Main	Advanced	Boot	**Security**	Server	Exit
	>> System Management				
	>> Serial Console Features				
	>> Event Log configuration				
	Assert NMI on PERR				
	Assert NMI on SERR				
	Power Link				
	Platform Event Filtering				
	FRB-2 Policy				
	Late POST Timeout				
	Hard Disk OS Boot Timeout				
	PXE OS Boot Timeout				
	FRB-4 Policy				

The menu represented in Table 39 is for Server features.

Table 39. Server Menu

Feature	Options	Description
System Management	• No options	Selects submenu.
Serial Console Features	• No options	Selects submenu.
Event Log configuration	• No options	Selects submenu.
Assert NMI on PERR	• Disabled • Enabled (default)	If enabled, NMI is generated. SERR option needs to be enabled to activate this option.
Assert NMI on SERR	• Disabled • Enabled (default)	If enabled, NMI is generated on SERR and logged.
Power Link	• Stays Off • Power On	Determines the mode of operation if a power loss occurs. If Stays Off is selected, the system remains off once power is restored. If Power On is selected, the system will boot after power is restored. When available, Last State restores the system to state it was in before power failed.
Platform Event Filtering	• Disabled • Enabled	
FRB-2 Policy	• Retry on Next Boot (default) • Disable FRB2 Timer	Controls whether or not the FRB2 Timer will be disabled.

Late POST Timeout	• Disable (default) • 5 minutes • 10 minutes • 15 minutes • 20 minutes	Controls the time limit allowed for add-in card detection. The system is reset on timeout.
Hard Disk OS Boot Timeout	• Disable (default) • 5 minutes • 10 minutes • 15 minutes • 20 minutes	Controls the time limit allowed for booting an OS from a hard disk drive. The action taken on timeout is determined by the Fault Resilient Boot Timer policy setting.
PXE OS Boot Timeout	• Disable (default) • 5 minutes • 10 minutes • 15 minutes • 20 minutes	This controls the time limit allowed for booting an OS using PXE boot. The action taken on timeout is determined by the Fault Resilient Boot Timer policy setting.
FRB-4 Policy	• Stay On (default) • Reset • Power Off	Controls the policy upon timeout. If Stay On is selected, no overt action will be taken. If Reset is selected, the system will be forced to reset. If Power Off is selected, the system will be forced to power off.

4.8.7.1 System Management Submenu

To access this menu, select Server on the menu bar, then System Management.

Main	Advanced	Boot	**Security**	Server	Exit

>> System management
>> Serial Console Features
>> Event Log configuration
Assert NMI on PERR
Assert NMI on SERR
AC Link
FRB-2 Policy
Late POST Timeout
Hard Disk OS Boot Timeout
PXE OS Boot Timeout
FRB-4 Policy

The submenu represented in Table 40 is for setting the System Management.

Table 40. System Managment Submenu

Feature	Options	Description
Board Part Number:	• No options	Varies
Board Serial Number:	• No options	Varies
System Part Number:	• No options	Varies
System Serial Number:	• No options	Varies
Chassis Part Number:	• No options	Varies
Chassis Serial Number:	• No options	Varies
Version:	• No options	BIOS ID string.
BMC Device ID	• No options	Varies
BMC Firmware Revision:	• No options	Varies
BMC Revision:	• No options	Varies
SDR Revision:	• No options	Varies

4.8.7.2 Serial Console Features Submenu

To access this menu, select Server on the menu bar, then Serial Console Features

Main	Advanced	Boot	**Security**	Server	Exit
	>> System management				
	>> Serial Console Features				
	>> Event Log configuration				
	Assert NMI on PERR				
	Assert NMI on SERR				
	Power Link				
	Platform Event Filtering				
	FRB-2 Policy				
	Late POST Timeout				
	Hard Disk OS Boot Timeout				
	PXE OS Boot Timeout				
	FRB-4 Policy				

The submenu represented in Table 41 is for setting the Serial Console Features.

Table 41. Serial Console Features Submenu

Feature	Options	Description
BIOS Redirection Port	• Disabled (default) • Serial 1 (DB-9) • Serial 2 (RJ-45)	If enabled, BIOS uses the specified serial port to redirect the console to a remote ANSI terminal. Enabling this option disables Quiet Boot. Keys used in console: ESC +'0' :F10 ESC +'1'..'9' :F1..F9 +'0' ESC +'{' :Refresh Screen
Baud Rate	• 9600 • 19.2K (default) • 38.4K • 57.6K • 115.2K	
Flow Control	• No Flow Control • CTS/RTS (default) • XON/XOFF • CTS/RTS + CD	If enabled, it will use the Flow control selected. CTS/RTS = Hardware XON/XOFF = Software CTS/RTS + CD = Hardware + Carrier Detect for Modem use.
Terminal Type	• PC-ANSI • VT100+ (default) • VT-UTF8	VT100+ selection only works for English as the select language. VT-UTF8 uses Unicode. PC-ANSI is the standard PC-type terminal.

4.8.7.3 Event Log Configuration Submenu

To access this menu, select Server on the menu bar, then Event Log Configuration.

Main	Advanced	Boot	**Security**	Server	Exit

>> System management
>> Serial Console Features
>> Event Log Configuration
Assert NMI on PERR
Assert NMI on SERR
Power Link
Platform Event Filtering
FRB-2 Policy
Late POST Timeout
Hard Disk OS Boot Timeout
PXE OS Boot Timeout
FRB-4 Policy

The submenu represented in Table 42 is for setting the Event Log Configuration.

Table 42. Event Log Configuration Submenu

Feature	Options	Description
Clear All Event Logs	• Disabled (default) • Enabled	Setting this to Enabled will clear the DMI event log after system booting.
Event Logging	• Disabled • Enabled (default)	Select Enabled to allow logging of events.
Critical Event Logging	• Disabled • Enabled (default)	If enabled, BIOS will detect and log events for system critical errors. Critical errors are fatal to system operation. These errors include PERR, SERR, and ECC.
ECC Event Logging	• Disabled • Enabled (default)	
PCI Error logging	• Disabled • Enabled (default)	

4.8.8 Exit Menu

To access this menu, select Exit from the menu bar at the top of the screen.

Main	Advanced	Boot	Security	Server	**Exit**

The menu represented in Table 43 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 43. Exit Menu

Feature	Description
Save Changes and Exit	Exits and saves the changes in CMOS SRAM. F10 key can be used for this operation.
Discard Changes and Exit	Exits without saving any changes made in the BIOS Setup program. ESC key can be used for this operation.
Discard Changes	Discards changes without exiting Setup. The option values present when the server was turned on are used. F7 key can be used for this operation
Load Optimal Defaults	Load Optimal Default values for all the setup questions. F9 key can be used for this operation.
Load Failsafe Defaults	Load Failsafe Default values for all the setup questions. F8 key can be used for this operation.
Load Custom Defaults	Load Custom Defaults
Save Custom Defaults	Save Custom Defaults

4.9 Operating System Boot, Sleep and Wake

4.9.1 Microsoft* Windows* Compatibility

Intel Corporation and Microsoft Corporation co-author design guides for system designers using Intel processors and Microsoft* operating systems. These documents are updated yearly to address new requirements and current trends.

PC200x specifications are intended for systems that are designed to work with Windows 2000 and Windows XP class operating systems. The Hardware Design Guide (HDG) for the Windows XP platform is intended for systems that are designed to work with Windows XP class operating systems. Each specification classifies the systems further and has requirements based on the intended usage for that system. For example, a server system that will be used in small home/office environments has different requirements than the one used for enterprise applications.

The server board SE7210TP1-E supports HDG3.0.

4.9.2 Advanced Configuration and Power Interface (ACPI)

ACPI gives the operating system direct control over the power management and Plug and Play functions of a server. The use of ACPI with the Intel Server Board SE7210TP1-E requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the standby or sleeping state
- A Soft-off feature that enables the operating system to power-off the server
- Support for multiple wake-up events.
- Support for a front panel power and sleep mode switch

4.9.3 Sleep and Wake Functionality

The BIOS supports up to four front panel buttons: the power button, the reset button, the sleep button, and the NMI button. The NMI button is a recessed button and may not be accessible on all front panel designs.

The power button is a request that is forwarded by the National Semiconductor PC87431 integrated management controller to the ACPI power state machines in the chipset. It is monitored by the National Semiconductor PC87431 integrated management controller and does not directly control power on the power supply.

The BIOS supports a front panel NMI button. The NMI button is a request that causes the National Semiconductor PC87431 integrated management controller to generate an NMI (non-maskable interrupt). The operating system is responsible for handling the NMI core dump.

The power button behaves differently depending on whether the operating system supports ACPI. If the operating system supports ACPI the power button can be configured as a sleep

button. The operating system causes the system to transition to the appropriate system state depending on the user settings.

4.9.3.1 On to Off (OS-Present) or OS to Sleep

If an operating system is loaded, the power button switch generates a request via the system control interrupt (SCI) to the operating system to shutdown the system. The operating system retains control of the system and operating system policy determines if the system transitions into S4/S1 or shuts down.

4.9.3.2 Sleep to On (ACPI)

If an operating system is loaded, the power button or Wake on LAN (WOL) can generate a wake event to the ACPI chipset and a request (via SCI). If system wakes up from S4/S5, the BIOS POST is completed and then control is given to operating system to wake up the system. If wakeup is from S1, the operating system will wake up the system.

4.9.3.3 System Sleep States

The platform supports the following ACPI System Sleep States:

- ACPI S0 (working) state
- ACPI S1 (sleep) state
- ACPI S4 (suspend to disk) state
- ACPI S5 (soft-off) state

Table 44: Supported Wake Events

Wake Event	Supported via ACPI (by sleep state)	Supported Via Legacy Wake
Power Button	Always wakes system.	Always wakes system
PME from PCI cards	Wakes from S1 and S4.	Yes
RTC Alarm	Wakes from S1. Always wakes the system up from S4.	No
Mouse	Wakes from S1.	No
Keyboard	Wakes from S1.	No
USB	Wakes from S1.	No

Table 45 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 45. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI S5 – Soft off)	Less than four seconds	Power-on (ACPI S0 – working state)
On (ACPI S0 – working state)	Less than four seconds	Soft-off/Standby (ACPI S1 or S3 – sleeping state)
On (ACPI S0 – working state)	More than four seconds	Fail safe power-off (ACPI S5 – Soft off)

4.9.3.4 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 46 lists the power states supported by the server board SE7210TP1-E along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 46. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G2/G5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the server.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

4.10 Security

The BIOS provides a number of security features. This section describes the security features and operating model.

The BIOS uses passwords to prevent unauthorized tampering with the system. Once secure mode is entered, access to the system is allowed only after the correct password(s) has been entered. Both User and Administrator passwords are supported by the BIOS. Each password can be independently set or cleared during system configuration using a setup. The maximum length of the password is seven characters. The password cannot have characters other than alphanumeric (a-z, A-Z, 0-9).

Once set, a password can be cleared by changing it to a null string. Entering the User password will allow the user to modify the time, date, language, user password. Other setup fields can be modified only if the Administrator password is entered. If only one password is set, this password is required to enter Setup.

Administrator has control over all fields in the setup including the ability to clear user password.

If the user enters three wrong passwords in a row during the boot sequence, the system will be placed into a halt state. This feature makes it difficult to break the password by “trial and error” method.

4.10.1 Administrator/User Passwords and F2 Setup Usage Model

Notes:

- Visible=option string is active and changeable
- Hidden=option string is inactive and not visible
- Shaded=option string is gray-out and view-only

There are four possible password scenarios:

Scenario #1

Admin/Supervisor Password	Not Installed
User Password	Not Installed
Login Type: N/A	
Set Admin/Supervisor Password (visible) Set User Password (visible) User Access Level [Full]** (shaded) Clear User Password (hidden)	

**: User Access Level option will be Full and Shaded as long as the admin/supervisor password is not installed.

Scenario #2

Admin/Supervisor Password Installed User Password Installed
Login Type: Admin/Supervisor
Set Admin/Supervisor Password (visible) Set User Password (visible) User Access Level [Full] (visible) Clear User Password (visible)
Login Type: User
Set Admin/Supervisor Password (hidden) Set User Password (visible) User Access Level [Full] (Shaded) Clear User Password (hidden)

Scenario #3

Admin/Supervisor Password - Not Installed User Password - Installed
Login Type: User
Set Admin/Supervisor Password (visible) Set User Password (visible) User Access Level [Full]** (shaded) Clear User Password (hidden)
Login Type: <Enter>
No Access

**: User Access Level option will be Full and Shaded as long as the admin/supervisor password is not installed.

Scenario #4

Admin/Supervisor Password Installed User Password Not Installed
Login Type: Supervisor
Set Admin/Supervisor Password (visible) Set User Password (visible) User Access Level [Full] (visible) Clear User Password (hidden)
Login Type: <Enter>
No Access

4.10.2 Password Clear Jumper

If the user or administrator password(s) is lost or forgotten, both passwords may be cleared by moving the password clear jumper to the clear position. The BIOS determines if the password clear jumper is in the clear position during BIOS POST and clears any passwords if required. The password clear jumper must be restored to its original position before a new password(s) can be set.

5. Platform Management Architecture

This chapter will provide an overview of the integrated platform management architecture and details of the features and functionality of the Essentials management model.

5.1 Essential Management Features and Functionality

5.1.1 Overview of National* Semiconductor PC87431 Integrated Management Controller

The National Semiconductor PC87431 integrated management controller is an Application Specific Integrated Circuit (ASIC) with a Reduced Instruction Set Computer (RISC)-based processor and many peripheral devices embedded into it. The National Semiconductor PC87431 integrated management controller contains the logic needed for executing the firmware, controlling the system, monitoring the sensors, and communicating with other systems and devices via various external interfaces.

The following figure is a block diagram of the National Semiconductor PC87431 integrated management controller as it is used in a server management system. The external interface blocks to the National Semiconductor PC87431 integrated management controller are the discrete hardware peripheral device interface modules.

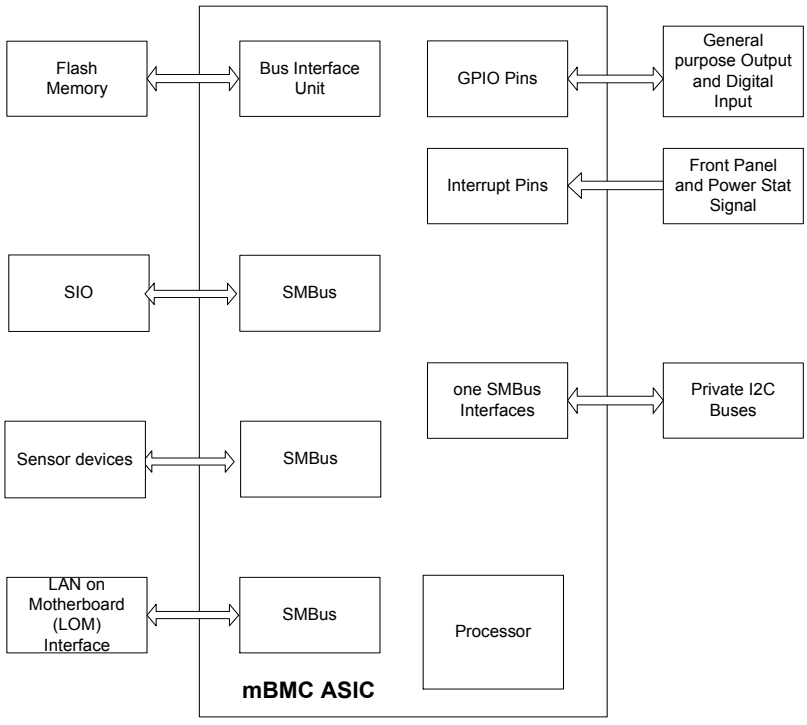


Figure 10: National Semiconductor PC87431 integrated management controller in a Server Management System

5.1.2 National Semiconductor PC87431 integrated management controller Self-test

The National Semiconductor PC87431 integrated management controller performs various tests as part of its initialization. If a failure is determined, the National Semiconductor PC87431 integrated management controller stores the error internally. A failure may be caused by a corrupt National Semiconductor PC87431 integrated management controller FRU, SDR, or SEL. Two commands may be used to retrieve the detected errors. The *IPMI 1.5 Get Self Test Results* command can be used to return the first error detected.

Executing the *Get Self Test Results* command causes the National Semiconductor PC87431 integrated management controller self-test to be run. It is strongly recommended to reset the National Semiconductor PC87431 integrated management controller via the *Cold Reset* command afterwards.

5.1.3 SMBus Interfaces

The National Semiconductor PC87431 integrated management controller incorporates one master/slave and two master-only SMBus interfaces. The National Semiconductor PC87431 integrated management controller interfaces with the host through a slave SMBus interface. It interfaces with the LAN On Motherboard (LOM) and peripherals through two independent master bus interfaces.

5.1.4 External Interface to National Semiconductor PC87431 integrated management controller

Figure 11 shows the data/control flow to and within the functional modules of the National Semiconductor PC87431 integrated management controller. External interfaces from the host system, LOM, and peripherals, interact with the National Semiconductor PC87431 integrated management controller through the corresponding interface modules as shown.

The National Semiconductor PC87431 integrated management controller communicates with the internal modules using its private SMBus. External devices and sensors interact with the National Semiconductor PC87431 integrated management controller using the peripheral SMBus through SIO. LOM communicates through the LOM SMBus. GPIO pins are available and can be configured for general purpose output or digital input events. Dedicated LED lines are available for LED/color control.

Also built into the National Semiconductor PC87431 integrated management controller are the control functions for both the power supply and front panel.

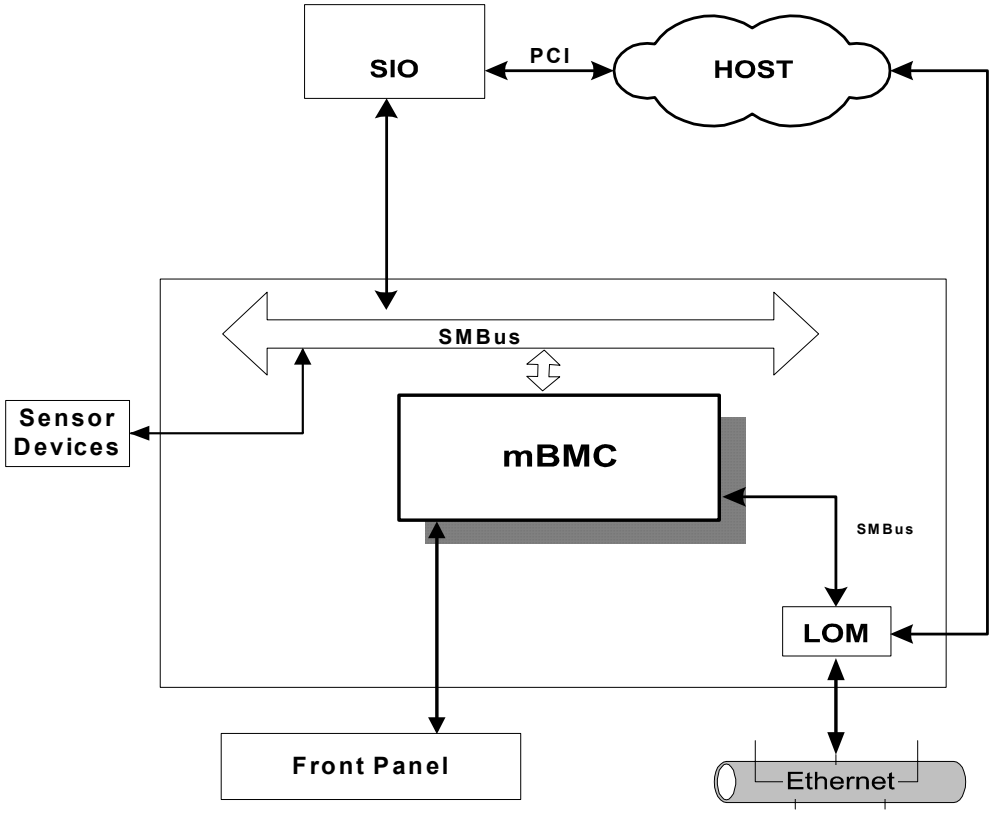


Figure 11: External Interfaces to National Semiconductor PC87431 integrated management controller

5.1.4.1 Private Management I²C Buses

The National Semiconductor PC87431 integrated management controller implements a single private management bus. The National Semiconductor PC87431 integrated management controller is the sole master on this bus. External agents must use the National Semiconductor PC87431 integrated management controller *Master Write/Read I²C* command if they require direct communication with a device on this bus. In addition, the National Semiconductor PC87431 integrated management controller provides a *Reserve Device* command that gives an external agent exclusive access to a specific device for a selectable time.

5.1.5 Messaging Interfaces

This section describes the supported National Semiconductor PC87431 integrated management controller communication interfaces:

- Host SMS interface via SMBus interface
- LAN interface using the LAN On Motherboard SMBus

5.1.5.1 Channel Management

The National Semiconductor PC87431 integrated management controller supports two channels:

- System interface
- 802.3 LAN

Table 47: Supported Channel Assigments

Channel Id	Media type	Interface	Supports Sessions
1	802.3 LAN	IPMB 1.0	Multi sessions
2	System Interface	IPMI-SMBus	Session-less

5.1.5.2 User Model

The National Semiconductor PC87431 integrated management controller supports one anonymous user (null user name) with a settable password. The IPMI command to set the password is not supported.

5.1.5.3 Request/Response Protocol

All of the protocols used in the host interface and the LOM interface are Request/Response protocols. A Request Message is issued to an intelligent device, to which the device responds with a separate Response Message.

5.1.5.4 Host to National Semiconductor PC87431 integrated management controller Communication Interface

The host communicates with the National Semiconductor PC87431 integrated management controller via the System Management Bus (SMBus). The interface consists of three signals:

- SMBus clock signal (SCLH)
- SMBus data signal (SDAH)
- Optional SMBus alert signal (SMBAH). The signal notifies the host that the PC87431x has data to provide.

When the system main power is off (PWRGD signal is low), the host interface signals are in TRI-STATE to perform passive bus isolation between the National Semiconductor PC87431 integrated management controller SCLH, SDAH and SMBAH signals and the SMBus controller signals. The passive bus isolation can be disabled by host SMBus isolation control to support various system designs.

The National Semiconductor PC87431 integrated management controller is a slave device on the bus. The host interface is designed to support polled operations. Host applications can optionally handle an SMBus alert interrupt if the National Semiconductor PC87431 integrated management controller is unable to respond immediately to a host request. In this case, “Not Ready” is indicated in one of two ways:

- The host interface bandwidth is limited by the bus clock and National Semiconductor PC87431 integrated management controller latency. To meet the device latency, the National Semiconductor PC87431 integrated management controller slows down the bus periodically by extending the SMBus clock low interval (SCLH).
- If the National Semiconductor PC87431 integrated management controller is in the middle of a LAN or peripheral device communication, or if a response to the host request is not yet ready, the National Semiconductor PC87431 integrated management controller does not acknowledge the device address (“NACK”). This forces the host software to stop and restart the session.

For more information on read-write through SMBus refer the *System Management Bus* (SMBus) Specification 2.0.

5.1.5.5 LAN Interface

The baseboard supports one DPC LAN interface via a UDP port 26Fh. The National Semiconductor PC87431 integrated management controller supports a maximum of one simultaneous session across all authenticated channels. The baseboard implements gratuitous ARP support according to the IPMI 1.5 Specification.

The IPMI Specification v1.5 defines how IPMI messages, encapsulated in RMCP packet format, can be sent to and from the National Semiconductor PC87431 integrated management controller. This capability allows a remote console application to access the National Semiconductor PC87431 integrated management controller and perform the following operations:

- Chassis Control, e.g., get chassis status, reset chassis, power-up chassis, power-down chassis
- Get system sensor status
- Get and Set system boot options
- Get Field Replaceable Unit (FRU) information
- Get System Event Log (SEL) entries
- Get Sensor Data Records (SDR)
- Set Platform Event Filtering (PEF)
- Set LAN configurations

In addition, the National Semiconductor PC87431 integrated management controller supports LAN alerting in the form of SNMP traps that conform to the IPMI Platform Event Trap (PET) format.

Table 48: LAN Channel Capacity

LAN CHANNEL Capability	Options
Number of Sessions	1
Number of Users	1
User	Name NULL (anonymous)
User Password	Configurable
Privilege Levels	User, Operator, Administrator
Authentication Types	MD5
Number of LAN Alert Destinations	1
Address Resolution Protocol (ARP)	Gratuitous ARP

5.1.6 Direct Platform Control (IPMI over LAN)

Direct Platform Control provides a mechanism for delivering IPMI Messages directly to the management controllers via a LAN connection. The NICs and the management controllers remain active on standby power, enabling the IPMI Messaging when the system is powered up, powered down, and in a system sleep state. This allows a remote console application to be able to access the management controller capabilities, including:

- Power on/off and reset control with the ability to set BIOS boot flags
- FRU, SDR, and SEL access
- National Semiconductor PC87431 integrated management controller configuration access
- Ability to transfer IPMI messages between the LAN interface and other interfaces, such as the System Interface, IPMB, and PCI SMBus. This capability enables messages to be delivered to system management software, and provides the ability to access sensors and FRU information on other management controllers.

IPMI Messages are encapsulated in a packet format called RMCP (Remote Management Control Protocol). The Distributed Management Task Force (DMTF) has defined RMCP for supporting pre-OS and OS-absent management. RMCP is a simple request-response protocol that can be delivered using UDP datagrams. IPMI-over-LAN uses version 1 of the RMCP protocol and packet format.

UDP port 26Fh is a ‘well known’ port address that is specified to carry RMCP (Remote Management Control Protocol) formatted UDP datagrams. The on-board Intel network interface controllers contain circuitry that enables detecting and capturing RMCP packets that are received on Port 26Fh and making them available to the management controller via a ‘side-band’ interface that is separate from the PCI interface to the NIC. Similarly, the management controller can use the side-band interface to send packets from Port 26Fh, as shown in the following figure.

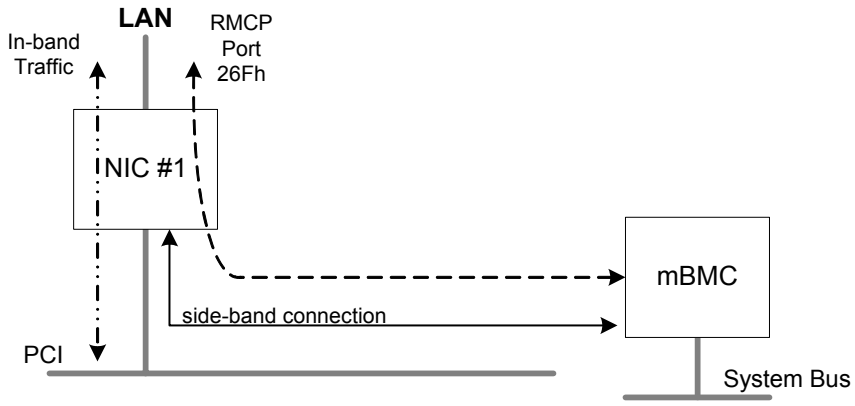


Figure 12 - IPMI-over-LAN

RMCP includes a field that indicates the class of messages that can be embedded in an RMCP message packet. For RMCP version 1.0, the defined classes are IPMI, ASF, and OEM. IPMI-over-LAN uses the IPMI class to transfer IPMI Messages encapsulated in RMCP packets. Intelligent Platform Management Interface v1.5 Specification specifies the packet formats and commands used to perform IPMI Messaging on LAN via RMCP.

The management controller transmits to other port addresses as needed. For example, LAN Alerts, which are sent as SNMP Traps, can be transmitted to the SNMP Trap 'well known' port address, 162 (0A2h).

5.1.6.1 LAN Channel Specifications

The following table presents the minimum support that will be provided. Note that system management software and utilities may not use all the available management controller options and capabilities. For detailed technical information on the operation of the LAN channel operation and LAN Alerting, refer to Intelligent Platform Management Interface v1.5 Specification.

Table 49: LAN Channel Specifications

Configuration Capability	Options	Description/Notes
Channel Access Modes	always-active, disabled	This option determines when the National Semiconductor PC87431 integrated management controller can be accessed via IPMI Messaging over LAN.
Number of Sessions	1 (Essentials)	The number of simultaneous sessions that can be supported is shared across the LAN and serial/modem channels.
Number of Users	1 (Essentials)	User information is a resource that is shared across the LAN and serial/modem channels.
Configurable User Names	No (Essentials)	User information is a resource that is shared across the LAN and serial/modem channels.
Configurable User Passwords	Yes	

Configuration Capability	Options	Description/Notes
Privilege Levels	User, Operator, Administrator	
IPMI Message Authentication Type Support	MD5	
Number of LAN Alert destinations	1 (Essentials)	
PET Acknowledge support	Yes	
Gratuitous ARP Support	Yes	

5.1.6.2 LAN Drivers and Setup

The IPMI-over-LAN feature must be used with the appropriate Intel NIC Driver, and the NIC correctly configured in order for DPC LAN operation to occur transparently to the operating system and network applications. If an incorrect driver or NIC configuration is used, it is possible to get driver timeouts when the IPMI-over-LAN feature is enabled.

5.1.6.3 BIOS Boot Flags

A remote console application can use the IPMI *Set System Boot Options* command to configure a set of BIOS boot flags and boot initiator info parameters that are held by the management controller. These parameters include information that identifies the party that initiated the boot, plus flags and other information that can be used to direct the way booting proceeds after a system reset or power-up. For example, whether the system should boot normally, boot using PXE, boot to a diagnostic partition, etc.

5.1.6.4 Boot Flags and LAN Console Redirection

The system BIOS includes a LAN Console Redirection capability. This capability can only be directed to one IP Address at a time. Thus, the boot flags and boot initiator information are also used to tell the BIOS where to send LAN Console Redirection.

5.1.7 Wake On LAN / Power On LAN and Magic Packet Support

The baseboard supports Wake On LAN / Power On LAN capability using the on-board network interface chips or an add-in network interface card. An add-in network card can deliver the wake signal to the baseboard via the PME signal on the PCI bus. The actual support for Magic Packet and/or packet filtering for Wake On LAN / Power On LAN is provided by the NIC. The baseboard handles the corresponding wake signal.

5.1.7.1 Wake On LAN in S4/S5

A configuration option is provided that allows the on-board NICs to be enabled to wake the system in an S4/S5 state, even if the operating system disabled Wake-On-LAN when it powered down the system. This provides an option for users who want to use standard, but non-secure, WOL capability for operations such as after-hours maintenance. Note that the DPC LAN capability provides a secure system power-up, plus the ability to provide BIOS boot options, by sending authenticated IPMI messages directly to the National Semiconductor PC87431 integrated management controller via the on-board NICs.

5.1.8 Watchdog Timer

The National Semiconductor PC87431 integrated management controller implements an IPMI 1.5-compatible watchdog timer. See the IPMI specification for details. SMI and NMI pre-timeout actions are supported, as are hard reset, power down, and power cycle timeout actions.

5.1.9 System Event Log (SEL)

The National Semiconductor PC87431 integrated management controller implements the logical System Event Log device as specified in the *Intelligent Platform Management Interface Specification, Version 1.5.* The SEL is accessible via all communication transports. In this way, the SEL information can be accessed while the system is down by means of out-of-band interfaces. The maximum SEL size that is supported by National Semiconductor PC87431 integrated management controller is 92 entries.

Supported commands are:

- Get SEL Info
- Reserve SEL
- Get SEL Entry
- Add SEL Entry
- Clear SEL
- Get SEL Time
- Set SEL Time

5.1.9.1 Timestamp Clock

The National Semiconductor PC87431 integrated management controller maintains a four-byte internal timestamp clock used by the SEL and SDR subsystems. This clock is incremented once per second. It is read using the *Get SEL Time* command and set using the *Set SEL Time* command. The *Get SDR Time* command can also be used to read the timestamp clock. These commands are specified in the *Intelligent Platform Management Interface Specification, Version 1.5.*

After a National Semiconductor PC87431 integrated management controller reset, the National Semiconductor PC87431 integrated management controller sets the initial value of the timestamp clock to 0x00000000. It is incremented once per second after that. A SEL event containing a timestamp from 0x00000000 to 0x140000000 has a timestamp value that is relative to National Semiconductor PC87431 integrated management controller initialization.

The BIOS provides the time to the National Semiconductor PC87431 integrated management controller during POST. During POST, the BIOS tells the National Semiconductor PC87431 integrated management controller the current RTC time via the *Set SEL Time* command. The National Semiconductor PC87431 integrated management controller maintains this time, incrementing it once per second, until the National Semiconductor PC87431 integrated management controller is reset or the time is changed via another *Set SEL Time* command.

If the RTC changes during system operation, system management software synchronizes the National Semiconductor PC87431 integrated management controller time with the system time.

5.1.10 Sensor Data Record (SDR) Repository

The National Semiconductor PC87431 integrated management controller includes built-in Sensor Data Records that provide platform management capabilities (sensor types, locations, event generation and access information). SDR Repositories are kept in the non-volatile storage area (flash) of the National Semiconductor PC87431 integrated management controller. The SDR Repository is accessible via all communication transports. This way, out-of-band interfaces can access the SDR Repository information if the system is down.

The National Semiconductor PC87431 integrated management controller supports 2176 bytes of storage for SDR records. The SDR defines the type of sensor, thresholds, hysteresis values and event configuration. The National Semiconductor PC87431 integrated management controller supports up to six threshold values for threshold-based full sensor records, and up to 15 events for non threshold-based full and compact sensor records. It also supports both low-going and high-going sensor devices.

5.1.10.1 Initialization Agent

The National Semiconductor PC87431 integrated management controller implements the internal sensor initialization agent functionality specified in the *Intelligent Platform Management Interface Specification, Version 1.5.* When the National Semiconductor PC87431 integrated management controller initializes, or when the system boots, the initialization agent scans the SDR repository and configures the sensors referenced by the SDRs. This includes setting sensor thresholds, enabling/disabling sensor event message scanning, and enabling/disabling sensor event messages.

5.1.11 Event Message Reception

The National Semiconductor PC87431 integrated management controller supports externally (e.g., BIOS) generated events via the Platform Event Message command. Events received via this command will be logged to the SEL and processed by PEF.

5.1.12 Event Filtering and Alerting

The National Semiconductor PC87431 integrated management controller implements the following IPMI 1.5 alerting features:

- PEF
- Alert over LAN

5.1.12.1 Platform Event Filtering (PEF)

The National Semiconductor PC87431 integrated management controller monitors platform health and logs failure events into the SEL. The Platform Event Filtering feature provides a configurable mechanism to allow events to trigger alert actions. PEF provides a flexible, general mechanism that enables the National Semiconductor PC87431 integrated management controller to perform selectable actions triggered by a configurable set of platform events. The National Semiconductor PC87431 integrated management controller supports the following IPMI PEF actions:

- Power-down
- Soft shut-down
- Power cycle
- Reset
- Diagnostic Interrupt
- Alert

In addition, the National Semiconductor PC87431 integrated management controller supports the following OEM actions:

- Fault LED action
- Identification LED action
- Device feedback

The power-down, soft shut-down, power cycle and reset actions can be delayed by a specified number of 100ms.

The National Semiconductor PC87431 integrated management controller maintains an Event Filter table with 30 entries that is used to select the actions to perform. Also maintained is a fixed/read-only Alert Policy Table entry. No alert strings are supported.

Note: All Fault/Status LED and ID LED behaviors are driven off of PEF. PEF should not be disabled and the default entry configuration should not be modified or those behaviors will be changed.

Each time the PEF module receives either an externally or internally generated event message, it compares the event data against the entries in the event filter table. The National Semiconductor PC87431 integrated management controller scans all entries in the table and determines a set of actions to be performed. If a combination of actions is identified, such as power down, power cycle, and/or reset actions, the action are performed according to PEF Action Priorities. Action priorities are outlined in

Table 50.

Note: An action that has changed from delayed to non-delayed, or an action whose delay time has been reduced has a higher priority. Each generated event is logged by SEL.

Table 50: PEF Action Priorities

Action	Priority	Delayed	Type	Note
Power-down	1	Yes	PEF Action	
Soft shut-down	2	Yes	OEM PEF Action	Not executed if a power-down action was also selected.
Power cycle	3	Yes	PEF Action	Not executed if a power-down action was also selected.
Reset	4	Yes	PEF Action	Not executed if a power-down action was also selected.
Diagnostic Interrupt	5	No	PEF Action	Not executed if a power-down action was also selected.
PET Alert	6	No	PEF Action	When selected, always occurs immediately after detection of a critical event.
Sensor feedback	7	No	OEM PEF Action	When selected, always occurs immediately after detection of a critical event.
IPMB message event	8	No	OEM PEF Action	When selected, always occurs immediately after detection of a critical event.
Fault LED action	9	No	OEM PEF Action	When selected, always occurs immediately after detection of a critical event, and is stopped after the de-assertion of all critical events that requested LED blinking.
Identification LED action	10	No	OEM PEF Action	When selected, always occurs immediately after detection of a critical event.

Table 51. National Semiconductor PC87431 integrated management controller Factory Default Event Filters

Event Filter #	Offset Mask	Events
1	Non-critical	Voltage Assert
2	Non-critical	Voltage Deassert
3	Critical	Voltage Assert
4	Critical	Voltage Deassert
5	Critical	PS Soft Fail Assert
6	Critical	PS Soft Fail Deassert
7	Critical	Proc 1-2 Thermal Trip Assert
8	Critical	Proc 1-2 Thermal Trip, Config Error & IERR Deassert
9	Degraded	Proc 1-2 FRB3 Assert
10	Degraded	Proc 1-2 FRB3 Deassert
11	Degraded	Proc 1-2 Hot Assert
12	Degraded	Proc 1-2 Hot Deassert
13	Critical	FP NMI Assert
14	Critical	FP NMI Deassert
15	Non Critical	SCSI Terminator Fail Assert
16	Non Critical	SCSI Terminator Fail Deassert
17	N/A	ID Button Assert

Event Filter #	Offset Mask	Events
18	N/A	ID Button Deassert
19	Critical	Fan Speed Assert
20	Critical	Fan Speed Deassert
21	Non Critical	Fan Speed Assert
22	Non Critical	Fan Speed Deassert
23	Critical	Temperature Assert
24	Critical	Temperature Deassert
25	Non Critical	Temperature Assert
26	Non Critical	Temperature Deassert
27	Critical	Proc 1-2 IERR Assert
28	Critical	CPU Configuration Error
29	N/A	Reserved for ISM
30	N/A	Reserved for ISM

5.1.12.2 Alert over LAN

LAN alerts are sent as SNMP traps in ASF formatted Platform Event Traps to a specified alert destination. The Alert over LAN feature is used to send either Platform Event Trap alerts or directed events to a remote system management application, regardless of the state of the host's operating system. LAN alerts may be sent over any of the LAN channels supported by a platform. LAN alerts can be used by PEF to send out alerts to selected destination when ever an event matches an event filter table entry For more information on LAN alerts, see the *IPMI Specification v1.5*.

5.1.12.3 System Identification in Alerts

The PET alert format used in PPP and LAN Alerting contains a system GUID field that can be used to uniquely identify the system that raised the alert. In addition, since the PET is carried in a UDP packet, the alerting system's IP Address is also present.

5.1.12.4 Platform Alerting Setup

The management controller provides commands via the System Interface that support setting/retrieving the alerting configuration LAN alerting in National Semiconductor PC87431 integrated management controller NV storage.

The user does not typically deal with filter contents directly. Instead, the Server Setup Utility provides a user interface that allows the user to select among a fixed set of pre-configured event filters.

The following list presents the type of Alerting configuration options that are provided:

- Enabling/Disabling PEF.
- Configuring Alert actions.
- Selecting which pre-configured events trigger an alert.
- Generating a 'test' event to allow the paging configuration to be checked.
- Configuring the serial/modem and PPP communication and link parameters.
- Configuring the alert destination information, including LAN addresses, phone numbers, Alert strings, etc.
- Configuring the PPP Accounts for PPP Alerting (PPP Accounts represent the phone number and user login information necessary to connect to a remote system via PPP).

5.1.12.5 Alerting On Power Down Events

The National Semiconductor PC87431 integrated management controller is capable of generating alerts while the system is powered down. A watchdog power-down event alert is sent after the power down so that the alert does not delay the power-down action.

5.1.12.6 Alerting On System Reset Events

Reset event alerts occur after the reset. The alerting process must complete before the system reset is completed. This is done to simplify timing interactions between the National Semiconductor PC87431 integrated management controller and BIOS initialization after a system reset.

5.1.12.7 Alert-in-Progress Termination

An alert in progress will be terminated by a system reset or power on, or by disabling alerting via commands to the management controller.

5.1.13 NMI Generation

The following may cause the National Semiconductor PC87431 integrated management controller to generate an NMI pulse:

- Receiving a C*hassis Control* command issued from one of the command interfaces. Use of this command will not cause an event to be logged in the SEL.
- Detecting that the front panel Diagnostic Interrupt button has been pressed.
- A PEF table entry matching an event where the filter entry has the NMI action indicated.
- A processor IERR or Thermal Trip (if the National Semiconductor PC87431 integrated management controller is so configured).
- Watchdog timer pre-timeout expiration with NMI pre-timeout action enabled.

The National Semiconductor PC87431 integrated management controller-generated NMI pulse duration is 200ms. This time is chosen to try to avoid the BIOS missing the NMI if the BIOS is in the SMI Handler and the SMI Handler is masking the NMI.

Once an NMI has been generated by the National Semiconductor PC87431 integrated management controller, the National Semiconductor PC87431 integrated management

controller will not generate another NMI until the system has been reset or powered down, however, enabling NMI via an *NMI Enable/Disable* command will re-arm the NMI.

The National Semiconductor PC87431 integrated management controller captures the NMI source(s) and makes that information available via a *Get NMI Source* command. Reading the NMI source information causes it to be cleared. A second *Set NMI Source* command can be used by other agents, such as the BIOS SMI Handler, to register NMI sources when they detect NMI generating errors. Operating system NMI handlers that save the system crash state can use the *Get NMI Source* command to determine and save the cause of the NMI.

5.1.14 SMI Generation

The National Semiconductor PC87431 integrated management controller can generate an SMI due to watchdog timer pre-timeout expiration with SMI pre-timeout interrupt specified. The SMI generation is software configurable. The above conditions may or may not be enabled to cause an SMI.

5.2 Platform Management Interconnects

5.2.1 Power Supply Interface Signals

The National Semiconductor PC87431 integrated management controller supports two power supply control signals: *Power On* and *Power Good*. The *Power On* signal connects to the chassis power subsystem and is used to request power state changes (asserted = request *Power On*). The *Power Good* signal from the chassis power subsystem indicates current the power state (asserted = power is on).

Figure 13 shows the power supply control signals and their sources. To turn the system on, the National Semiconductor PC87431 integrated management controller asserts the *Power On* signal and waits for the *Power Good* signal to assert in response, indicating that DC power is on.

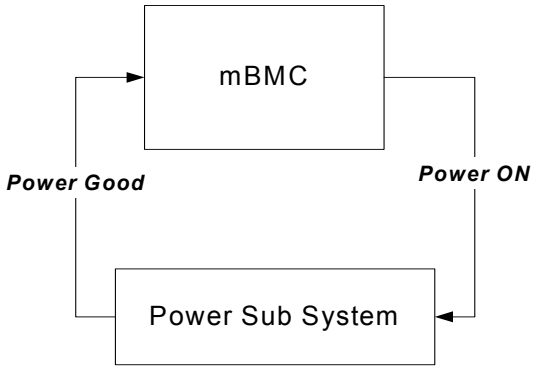


Figure 13: Power Supply Control Signals

The National Semiconductor PC87431 integrated management controller uses the *Power Good* signal to monitor whether the power supply is on and operational, and to confirm whether the actual system power state matches the intended system on/off power state that was commanded with the *Power On* signal.

De-assertion of the *Power Good* signal generates an interrupt that the National Semiconductor PC87431 integrated management controller uses to detect either power subsystem failure or loss of AC power. If AC power is suddenly lost, the National Semiconductor PC87431 integrated management controller:

1. Immediately asserts system reset
2. Powers down the system
3. Waits for configured system off time (depending on configuration)
4. Attempts to power the system on (depending on configuration)

5.2.1.1 Power-up Sequence

When turning on the system power in response to one of the event occurrences listed in Table 52 below, the National Semiconductor PC87431 integrated management controller executes the following procedure:

1. The National Semiconductor PC87431 integrated management controller asserts *Power On* and waits for the power subsystem to assert *Power Good*. The system is held in reset.
2. The National Semiconductor PC87431 integrated management controller sends a *Set ACPI Power State* command, indicating an S0 state to all management controllers whose SDR management device records indicate that they should receive the notification.
3. The National Semiconductor PC87431 integrated management controller initializes all sensors to their *Power On* initialization state. The Init Agent is run.
4. The National Semiconductor PC87431 integrated management controller attempts to boot the system by running the FRB algorithm.

5.2.1.2 Power-down Sequence

To power down the system, the National Semiconductor PC87431 integrated management controller effectively performs the sequence of power-up steps in reverse order. This operation can be initiated by one of the event occurrences listed in Table 52 and proceeds as follows:

1. The National Semiconductor PC87431 integrated management controller asserts system reset (de-asserts *Power Good*).
2. If enabled, the National Semiconductor PC87431 integrated management controller sends a *Set ACPI Power State* command, indicating an S0 state to all management controllers whose SDR management device records indicate that they should receive the notification.
3. The National Semiconductor PC87431 integrated management controller de-asserts the *Power On* signal.
4. The power subsystem turns off system power upon de-assertion of the *Power On* signal.

5.2.1.3 Power Control Sources

The sources listed in the following table can initiate power-up and/or power-down activity.

Table 52: Power Control Initiators

#	Source	External Signal Name or Internal Subsystem	Capabilities
1	Power Button	FP Power button	Turns power ON or OFF
2	National Semiconductor PC87431 integrated management controller Watchdog Timer	Internal National Semiconductor PC87431 integrated management controller timer	Turns power OFF, or power cycle
3	Platform Event Filtering	PEF	Turns power OFF, or power cycle
4	Command	Routed through command processor	Turns power ON or OFF, or power cycle
5	Power state retention	Implemented via National Semiconductor PC87431 integrated management controller internal logic	Turns power ON when AC power returns
6	Chipset	sleep S5	Turns power ON or OFF

5.2.2 System Reset Control

5.2.2.1 Reset Signal Output

The National Semiconductor PC87431 integrated management controller asserts the *System Reset* signal on the baseboard to perform a system reset. The National Semiconductor PC87431 integrated management controller asserts the *System Reset* signal before powering the system up. After power is stable (as indicated by the power subsystem *Power Good* signal), the National Semiconductor PC87431 integrated management controller sets the processor enable state as appropriate and de-asserts the *System Reset* signal, taking the system out of reset.

To reset the system without a power state change, the National Semiconductor PC87431 integrated management controller:

1. Asserts the *System Reset* signal.
2. Holds this state for as long as the reset button is pushed. When a command is used to generate a system reset, the state is held for the stipulated time.
3. De-asserts the *System Reset* signal.

5.2.2.2 Reset Control Sources

The following table shows the reset sources and the actions taken by the system.

Table 53: System Reset Sources and Actions

#	Reset Source	System Reset?	PC87431 Reset
1	Standby power comes up	No (no DC power)	Yes
2	Main system power comes up	Yes	No
3	Reset button or in-target probe (ITP) reset	Yes	No
4	Warm boot (example: DOS Ctrl-Alt-Del)	Yes	No
5	Command to reset the system	Yes	No
6	Set Processor State command	Yes	No
7	Watchdog timer configured for reset	Yes	No
8	FRB3 failure	Yes	No
9	PEF action	Optional	No

5.2.3 Temperature-based Fan Speed Control

Baseboard hardware implements an ambient-temperature-based Fan Speed control that is part of *normal system operation.* With one exception, the management controller does not participate in fan speed control. The feature allows the baseboard to drive different fan speeds based on various temperature measurements in order to lower the acoustic noise of the system.

The ambient-temperature thresholds at which the Fan Speed increases does not correspond to a non-critical (warning) condition for the fan - since the fan's state is still 'OK' from the system point-of-view.

The baseboard has two analog Fan Speed signals that are driven by pulse-width modulator (PWM) circuits by the baseboard hardware. These signals can be driven to several levels according to temperature measurements. Multiple bytes of a Sensor Initialization Table is used to hold parameters that set the temperature thresholds and corresponding PWM duty cycles. This SDR or table is loaded as part of the baseboard configuration.

The management controller firmware expects to find an LM30 temperature sensor on the front panel board. Thus, the ambient temperature-based fan speed control capability is not enabled by default, but can be enabled via a management controller configuration change.

5.2.3.1 Fan Kick Start

Some fans may not begin rotating unless started at high speed. To ensure that the fans start, the baseboard hardware will start and run the fans at high speed for a brief interval following system power up.

5.2.4 Front Panel Control

The National Semiconductor PC87431 integrated management controller provides the main front panel control functions. These include control of the system Power Button, Reset Button, Diagnostic Interrupt (Front Panel NMI) Button, System Identify Button, System ID LED, Status/Fault LED, and Chassis Intrusion Switch. Front panel control also includes the front panel lockout features.

5.2.4.1 Power Button

After de-bouncing the front panel *Power Button* signal, the National Semiconductor PC87431 integrated management controller routes the signal state directly to the chipset *Power Button* signal input. If the chipset has been initialized by the BIOS, the chipset responds to the assertion of the signal by requesting a power state change. It reacts to the press of the switch, not the release of it.

The *Power Button* signal toggles the system power. The *Power Button* signal to the National Semiconductor PC87431 integrated management controller is activated by a momentary contact switch on the front panel assembly. The National Semiconductor PC87431 integrated management controller de-bounces the signal. After de-bouncing the signal, the National Semiconductor PC87431 integrated management controller routes it directly to the chipset via the *Power Button* signal. The chipset responds to the assertion of the signal. It responds to the press of the switch, not the release of it.

If the system is in Secure Mode or the *Power Button* is forced protected, then when the power switch is pressed, a Platform Security Violation Attempt event message is generated and no power control action is taken.

In the case of simultaneous button presses, the *Power Button* action takes priority over all other buttons. For example, if the sleep button is depressed for one second and then the *Power Button* is pressed and released, the system powers down. Due to the routing of the de-bounced *Power Button* signal to the chipset, the power signal action overrides the action of the other switch signals.

5.2.4.2 Reset Button

The reset button is a momentary contact button on the front panel. Its signal is routed through the front panel connector to the National Semiconductor PC87431 integrated management controller, which monitors and de-bounces it. The signal must be stable for at least 25ms before a state change is recognized.

An assertion of the front *Panel Reset* signal to the National Semiconductor PC87431 integrated management controller causes the National Semiconductor PC87431 integrated management controller to start the reset and reboot process. This action is immediate and without the cooperation of any software or operating system running on the system.

If *Secure Mode* is enabled or the button is forced protected, the reset button does not reset the system, but instead a Platform Security Violation Attempt event message is generated. The reset button is disabled in sleep mode.

5.2.4.3 Diagnostic Interrupt Button (Front Panel NMI)

As stated in the *IPMI 1.5 Specification,* a Diagnostic Interrupt is a non-maskable interrupt or signal for generating diagnostic traces and core dumps from the operating system. The National Semiconductor PC87431 integrated management controller generates the NMI, which can be used as an OEM-specific diagnostic front panel interface.

The Diagnostic Interrupt button is connected to the National Semiconductor PC87431 integrated management controller through the front panel connector. A Diagnostic Interrupt button press causes the National Semiconductor PC87431 integrated management controller to generate a system NMI pulse whose duration is platform-specific and unrelated to the button press duration.

This generates an event (NMI button sensor) and PEF OEM action causes NMI generation.

5.2.4.4 Chassis ID Button and LED

The front panel interface supports a *Chassis Identify* Button and a corresponding Blue *Chassis Identify* LED. A second Blue Chassis Identify LED is mounted on the back edge of the baseboard where it may be visible when viewed from the back of an integrated system.

The LED can provide a mechanism for identifying one system out of a group of identical systems in a high density rack environment

The Chassis Identify LED can be turned on either locally via the push-button signal, or by local or remote software using the IPMI *Chassis Identify* command. The following list summarizes the Chassis Identify Push-button and LED operation:

- The Identify signal state is preserved on Standby power across system power-on/off and system hard resets. It is not preserved if A/C power is removed. The initial LED state is Off when A/C power is applied.
- The IPMI *Chassis Identify* command can also be used to control the LED. If a the *Chassis Identify* command is used to turn the LED On, the command will automatically time out and turn off the LED unless another *Chassis Identify* command to turn on the LED is received. The default timeout for the command is 15 seconds. The baseboard supports the optional command parameter to allow the timeout to be set anywhere from 1 to 255 seconds.
- The optional timeout parameter in the *Chassis Identify* command also allows software to tell the LED to go Off immediately.
- The Chassis Identify Pushbutton works using a “push-on/push-off” operation. Each press of the push-button toggles the LED signal state between On and Off. If the pushbutton is used to turn the LED On, it will stay on indefinitely, until either the button is pressed again or a *Chassis Identify* or *Chassis Identify LED* command causes the LED to go Off.

Table 54: Chassis ID LEDs

Color	Condition	When

Blue	Off	Ok
	Blink	Identify button pressed or Chassis Identify command executed

5.2.4.5 Status/Fault LED

The following table shows mapping of sensors/faults to the LED state.

Table 55: Fault/Status LED

Color	Condition	When
Green	Solid	System Ready
	Blink	System Ready, but degraded. CPU fault, DIMM killed
Amber	Solid	Critical Failure: critical fan, voltage, temperature state
	Blink	Non-Critical Failure: non-critical fan, voltage, temperature state
Off	Solid	Not Ready. POST error/NMI event/CPU or terminator missing

Critical Condition
Any critical or non-recoverable threshold crossing associated with the following events:

- Temperature, voltage, or fan critical threshold crossing
- Power subsystem failure. The National Semiconductor PC87431 integrated management controller asserts this failure whenever it detects a power control fault (e.g., the National Semiconductor PC87431 integrated management controller detects that the system power is remaining on even though the National Semiconductor PC87431 integrated management controller has de-asserted the signal to turn off power to the system). A hot-swap backplane would use the *Set Fault Indication* command to indicate when one or more of the drive fault status LEDs are asserted on the hot-swap backplane
- The system is unable to power up due to incorrectly installed processor(s), or processor incompatibility
- Satellite controller sends a critical or non-recoverable state, via the *Set Fault Indication* command to the National Semiconductor PC87431 integrated management controller
- “Critical Event Logging” errors, including: System Memory Uncorrectable ECC error and Fatal/Uncorrectable Bus errors, such as PCI SERR and PERR

Non-Critical Condition

- Temperature, voltage, or fan non-critical threshold crossing
- Chassis intrusion
- Satellite controller sends a non-critical state, via the *Set Fault Indication* command, to the National Semiconductor PC87431 integrated management controller
- *Set Fault Indication* command from system BIOS. The BIOS may use the *Set Fault Indication* command to indicate additional, non-critical status such as system memory or CPU configuration changes

Degraded Condition

- One or more processors are disabled by Fault Resilient Boot (FRB) or BIOS
- BIOS has disabled or mapped out some of the system memory

5.2.4.6 Chassis Intrusion Switch

The server board SE7210TP1-E supports chassis intrusion detection. The National Semiconductor PC87431 integrated management controller monitors the state of the *Chassis Intrusion* signal and makes the status of the signal available via the *Get Chassis Status* command and *Physical Security* sensor state. If enabled, a chassis intrusion state change causes the National Semiconductor PC87431 integrated management controller to generate a *Physical Security* sensor event message with a *General Chassis Intrusion* offset.

5.2.4.7 Front Panel Lockout

The management controller monitors a 'Secure Mode' signal from the keyboard controller on the baseboard. When the Secure Mode signal is asserted, the management controller may lock out the ability to power down or reset the system using the power or reset push buttons, respectively. Secure Mode may also block the ability to initiate a sleep request using the Sleep push-button.

The management controller generates a 'Secure Mode Violation Attempt' event message if an attempt it made to power-down, sleep, or reset the system using the push buttons while Secure Mode is active.

Note: The National Semiconductor PC87431 integrated management controller will prevent the system from powering up via button press when either secure mode or the front panel lockout I/O signal is asserted.

5.2.5 Secure Mode Operation

Secure mode is a signal from the SIO/keyboard controller. Power and reset buttons are locked out, except for the NMI and Chassis ID buttons. A security violation event is generated if buttons are pressed while secure mode is active.

The Secure Mode feature allows the front panel switches and other system resources to be protected against unauthorized use or access. Secure Mode is enabled and controlled via the *Set Secure Mode Options* command.

If it is enabled, Secure Mode can be controlled via the *Secure Mode KB* signal from the keyboard controller. When Secure Mode is active, pressing a protected front panel switch generates a Secure Mode Violation event. Specifically, this generates an assertion of the *Secure Mode Violation Attempt* offset of the National Semiconductor PC87431 integrated management controller's *Platform Security Violation Attempt* sensor.

The Secure Mode state is cleared whenever AC power or system power is applied, when a system reset occurs, or when a National Semiconductor PC87431 integrated management controller reset occurs. The Secure Mode state includes the bits that specify the actions that are to be taken when Secure Mode is active, as well as the *Force Secure Mode On* bit.

The *Set Secure Mode Options* command allows specific front panel switches to be protected irrespective of Secure Mode state. Please see the command definition in the IPMI v1.5 specification for details.

The NMI switch can be locked using the *Set Secure Mode Options* command but is never protected by Secure Mode. This allows a system to be recovered from a hung state when Secure Mode is active.

5.2.6 FRU Information

The platform management architecture supports providing FRU (Field Replaceable Unit) information for the baseboard and major replaceable modules in the chassis. 'Major Module' is defined as any circuit board in the system containing active electronic circuitry.

FRU information includes board serial number, part number, name, asset tag, and other information. FRUs that contain a management controller use the controller to provide access to the FRU information. FRUs that lack a management controller can make their FRU information available via a SEEPROM directly connected to the IPMB or a private I^2C bus. This allows the system integrator to provide a chassis FRU device without having to implement a management controller. This information can be accessed via IPMI FRU commands or using Master Write-Read commands.

The National Semiconductor PC87431 integrated management controller implements the interface for logical FRU inventory devices as specified in the *Intelligent Platform Management Interface Specification, Version 1.5.* This functionality provides commands used for accessing and managing the FRU inventory information associated with the National Semiconductor PC87431 integrated management controller (FRU ID 0). These commands can be delivered via all interfaces.

5.2.6.1 National Semiconductor PC87431 integrated management controller FRU Inventory Area Format

The National Semiconductor PC87431 integrated management controller FRU inventory area format follows the Platform Management FRU Information Storage Definition. Refer to *Platform Management FRU Information Storage Definition, Version 1.0* for details.

The National Semiconductor PC87431 integrated management controller provides only low-level access to the FRU inventory area storage. It does not validate or interpret the data that are written. This includes the common header area. Applications cannot relocate or resize any FRU inventory areas.

The baseboard's FRU information is kept in the National Semiconductor PC87431 integrated management controller internal flash memory.

5.2.7 LCD Support

The baseboard supports the addition of an LCD display via an IPMI-compatible management controller connected to the IPMB. The system BIOS sends IPMB commands to the display as described in the *LCD Interface for IPMB* specification.

5.3 Sensors

5.3.1 Sensor Type Codes

The following tables list the sensor identification numbers and information regarding the sensor type, name, supported thresholds, assertion and de-assertion information, and a brief description of the sensor purpose. Refer to the *Intelligent Platform Management Interface Specification, Version 1.5*, for sensor and event/reading-type table information.

- **Sensor Type**
  The Sensor Type references the values enumerated in the *Sensor Type Codes* table in the IPMI specification. It provides the context in which to interpret the sensor, e.g., the physical entity or characteristic that is represented by this sensor.

1 Event/Reading Type
The Event/Reading Type references values from the *Event/Reading Type Code Ranges* and *Generic Event/Reading Type Codes* tables in the *IPMI specification*. Note that digital sensors are a specific type of discrete sensors, which have only two states.

2 Event Offset/Triggers
Event Thresholds are supported event generating thresholds for threshold types of sensors.

- [u,l][nr,c,nc] upper nonrecoverable, upper critical, upper noncritical, lower nonrecoverable, lower critical, lower noncritical
- uc, lc upper critical, lower critical

Event Triggers are supported event generating offsets for discrete type sensors. The offsets can be found in the *Generic Event/Reading Type Codes* or *Sensor Type Codes* tables in the IPMI specification, depending on whether the sensor event/reading type is generic or a sensor specific response.

3 **Assertion/De-assertion Enables**
Assertions and De-assertion indicators reveals the type of events the sensor can generate:

- As: Assertions
- De: Deassertion

4 Readable Value / Offsets

- Readable Value indicates the type of value returned for threshold and other non-discrete type sensors.
- Readable Offsets indicates the offsets for discrete sensors that are readable via the *Get Sensor Reading* command. Unless otherwise indicated, all Event Triggers are readable, i.e., *Readable Offsets* consists of the reading type offsets that do not generate events.

5 **Event Data**
This is the data that is included in an event message generated by the associated sensor. For threshold-based sensors, the following abbreviations are used:

- R: Reading value

- T: Threshold value

The following table lists the core sensors located within the National Semiconductor PC87431 integrated management controller. These sensors are fixed and hard-coded. They cannot be modified by a user.

Table 56: National Semiconductor PC87431 integrated management controller Built-in Sensors

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets	EventData
Physical Security Violation	01	Physical Security 05h	Sensor Specific 6Fh	LAN Leash Lost	As	LAN Leash Lost	Trig Offset
Platform Security Violation	02	Platform Security Violation Attempt 06h	Sensor Specific 6Fh	Out-of-band access password violation	As	–	Trig Offset
Power Unit Status	03	Power Unit 09h	Sensor Specific 6Fh	• Power On/Off • Power cycle • AC Lost	As	–	Trig Offset
Button	04h	Button 14h	Sensor Specific 6Fh	Power Button Reset Button	As	–	Trig Offset
Watchdog	05h	Watchdog2 23h	Sensor Specific 6Fh	• Timer Expired • Hard Reset • Power Down • Power cycle • Timer Interrupt	As	–	Trig Offset

The following table shows the baseboard/platform sensors that are supported by the National Semiconductor PC87431 integrated management controller.

Table 57: SE7520JR2 Platform Sensors for Essentials Management

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value/Offsets	Event Data	PEF Action	SDR Record Type
Physical Security Violation	07h	Physical Security 05h	Sensor Specific 6Fh	General Chassis Intrusion	As	General Chassis Intrusion	Trig Offset	X	02
CPU1 12v	08h	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
CPU2 12v	09h	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
BB +1.5V	0Ah	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
BB +1.8V	0Bh	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
BB +3.3V	0Ch	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
BB +5V	0Dh	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
BB +12V	0Eh	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
BB -12V	0Fh	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
FSB Vtt	10h	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
MCH Vtt	11h	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
SCSI Core(1.8v)	12h	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Proc1 VCCP	13h	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Proc2 VCCP	14h	Voltage 02h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Tach Fan 1	15h	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Tach Fan 2	16h	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Tach Fan 3	17h	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Tach Fan 4	18h	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Tach Fan 5	19h	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value/Offsets	Event Data	PEF Action	SDR Record Type
Tach Fan 6	1Ah	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Tach Fan 7	1Bh	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Tach Fan 8	1Ch	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Tach Fan 9	1Dh	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
System Event	1Eh	System Event 12h	Sensor Specific 6Fh	PEF Action	As	–	Trig Offset	–	02
Proc1 IERR	1Fh	Processor 07h	Sensor Specific 6Fh	IERR	As	–	Trig Offset	–	02
Proc2 IERR	20h	Processor 07h	Sensor Specific 6Fh	IERR	As	–	Trig Offset	–	02
Proc1 Thermal trip	21h	Processor 07h	Sensor Specific 6Fh	Thermal Trip	As	–	Trig Offset	Fault LED Action	02
Proc2 Thermal trip	22h	Processor 07h	Sensor Specific 6Fh	Thermal Trip	As	–	Trig Offset	Fault LED Action	02
Proc1 Throttle	23h	Temp 01h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	Trig Offset	Fault LED Action	01
Proc2 Throttle	24h	Temp 01h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	Trig Offset	Fault LED Action	01
Diagnostic Interrupt Button	25h	Critical Interrupt 13h	Sensor Specific 6Fh	FP NMI Button	As	–	Trig Offset	NMI Pulse	02
Chassis Identify Button	26h	Button 14h	Generic 03h	Sate Deasserted State Assert	As & De	–	Trig Offset	ID LED Action	02
Proc1 Fan	27h	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Proc2 Fan	28h	Fan 04h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Proc1 Core temp	29h	Temp 01h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
Proc2 Core temp	2Ah	Temp 01h	Threshold 01h	[u,l][nr, c,nc]	As & De	Analog	R, T	Fault LED Action	01
CPU Configuration Error	2Bh	Processor 07h	Generic 03h	State Asserted	As & De	Discrete	R, T	Fault LED Action	02

6. Error Reporting and Handling

This section documents the types of system bus error conditions monitored by the Intel Server Board SE7210TP1-E.

6.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors, which can be disabled and enabled individually or as a group, can be categorized as follows:

- PCI bus
- Memory single- and multi-bit errors
- Sensors
- Processor internal errors, bus/address errors, thermal trip errors, temperatures and voltages, and GTL voltage levels
- Errors detected during POST, logged as 'POST errors'

On the SE7210TP1-E platform, the Winbond* chip manages general hardware monitoring sensors on a hardware level; however action is only taken by software (i.e., an application such as LANDesk™ Client Manager).

6.1.1 PCI Bus Errors

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled by BIOS.

6.1.2 Processor Bus Errors

The MCH supports the data integrity features supported by the Pentium® Pro bus, including address, request, and response parity. The E7210 chipset always generates ECC data while it is driving the processor data bus, although the data bus ECC can be disabled or enabled by BIOS. It is enabled by default.

6.1.3 Memory Bus Errors

The MCH is programmed to flag and log multi-bit errors (MBEs). The MCH then triggers an SMI to the 6300ESB I/O and the 6300ESB I/O asserts the SMI# signal. BIOS then logs the errors in the event log.

6.2 BIOS Error Messages, POST Codes, and BIOS Beep Codes

The BIOS indicates the current testing phase during POST by writing a hex code to I/O location 80h. If errors are encountered, error messages or codes will either be displayed to the video screen, or if an error has occurred prior to video initialization, errors will be reported through a series of audio beep codes. POST errors are logged in to the SEL.

The error codes are defined by Intel and, whenever possible, are backward compatible with error codes used on earlier platforms.

6.2.1 BIOS Error Messages

During POST, if an error is detected, the BIOS will display an error code and message to the screen. The following table defines POST error codes and their associated messages. The BIOS prompts the user to press a key in case of serious errors. Some of the error messages are preceded by the string "Error" to highlight the fact that the system may be malfunctioning. All POST errors and warnings are logged in the SEL

Table 58: POST Error Messages and Handling

Error Code	Error Message	Response
0000	Timer Error	Pause
0003	CMOS Battery Low	Pause
0004	CMOS Settings Wrong	Pause
0005	CMOS Checksum Bad	Pause
0008	Unlock Keyboard	Halt
0009	PS2 Keyboard not found	Not an error
000A	KBC BAT Test failed	Halt
000B	CMOS memory size different	Pause
000C	RAM R/W test failed	Pause
000E	A: Drive Error	Pause
000F	B: Drive Error	Pause
0010	Floppy Controller Failure	Pause
0012	CMOS Date/Time not set	Pause
0014	PS2 Mouse not found	Not an error
0040	Refresh timer test failed	Halt
0041	Display memory test failed	Pause
0042	CMOS Display Type Wrong	Pause
0043	~<INS> Pressed	Pause
0044	DMA Controller Error	Halt
0045	DMA-1 Error	Halt
0046	DMA-2 Error	Halt
0047	Unknown BIOS error. Error code = 147 (this is really a PMM_MEM_ALLOC_ERR)	Halt
0048	Password check failed	Halt
0049	Unknown BIOS error. Error code = 149 (this is really SEGMENT_REG_ERR)	Halt
004A	Unknown BIOS error. Error code = 14A (this is really ADM_MODULE_ERR)	Pause
004B	Unknown BIOS error. Error code = 14B (this is really LANGUAGE_MODULE_ERR)	Pause
004C	Keyboard/Interface Error	Pause
004D	Primary Master Hard Disk Error	Pause

004E	Primary Slave Hard Disk Error	Pause
004F	Secondary Master Hard Disk Error	Pause
0050	Secondary Slave Hard Disk Error	Pause
0055	Primary Master Drive - ATAPI Incompatible	Pause
0056	Primary Slave Drive - ATAPI Incompatible	Pause
0057	Secondary Master Drive - ATAPI Incompatible	Pause
0058	Secondary Slave Drive - ATAPI Incompatible	Pause
0059	Third Master Device Error	Pause
005B	Fourth Master Device Error	Pause
005D	S.M.A.R.T. Status BAD, Backup and Replace	Pause
005E	Password check failed	Pause
0120	Thermal failure due to PROCHOT#	Pause
0146	Insufficient Memory to Shadow PCI ROM	Pause
0147	Custom CMOS Defaults loaded	Pause
0150	BSP Processor failed BIST	Pause
0160	Processor missing microcode	Pause
0180	BIOS does not support current stepping	Pause
0195	Front side bus mismatch.	Pause
0197	Processor speeds mismatch.	Pause
5120	CMOS Cleared By Jumper	Pause
5121	Password cleared by jumper	Pause
5122	CMOS Cleared By mBMC Request	Pause
8104	Warning! Port 60h/64h emulation is not supported by this USB Host Controller!!!	Warning
8105	Warning! EHCI controller disabled. It requires 64bit data support in the BIOS.	Warning
8110	Processor 01 Internal error (IERR)	Warning
8120	Processor 01 Thermal Trip error	Warning
8140	Processor 01 failed FRB level 3 timer	Warning
8190	Watchdog Timer failed on last boot	Warning
8198	OS boot Watchdog Timer Failure	Pause
8300	Baseboard Management Controller failed Self Test	Pause
8301	Not enough space in Runtime area!!. SMBIOS data will not be available.	Pause
8305	Primary Hot swap Controller failed to function	Pause
84F2	BaseBoard Management Controller failed to respond	Pause
84F3	BaseBoard Management Controller in Update Mode	Pause
84F4	Sensor Data Record Empty	Pause
84FF	System Event Log Full	Warning
8500	Bad or missing memory in slot 2A	Pause
8501	Bad or missing memory in slot 1A	Pause
8504	Bad or missing memory in slot 2B	Pause
8505	Bad or missing memory in slot 1B	Pause

6.2.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Table 59: POST Code Checkpoints

Check point	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Diagnostic LED Decoder G=Green, R=Red, A=Amber
	Hi			Low	
03	OFF	OFF	G	G	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	OFF	G	OFF	OFF	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	OFF	G	OFF	G	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	OFF	G	G	OFF	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	G	OFF	OFF	OFF	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	R	R	OFF	OFF	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	R	R	OFF	G	Set up boot strap processor Information
C2	R	R	G	OFF	Set up boot strap processor for POST
C5	R	A	OFF	G	Enumerate and set up application processors
C6	R	A	G	OFF	Re-enable cache for boot strap processor
C7	R	A	G	G	Early CPU Init Exit
0A	G	OFF	G	OFF	Initializes the 8042 compatible Key Board Controller.
0B	G	OFF	G	G	Detects the presence of PS/2 mouse.
0C	G	G	OFF	OFF	Detects the presence of Keyboard in KBC port.

0E	G	G	G	OFF	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	OFF	OFF	G	A	Early POST initialization of chipset registers.
24	OFF	G	R	OFF	Uncompress and initialize any platform specific BIOS modules.
30	OFF	OFF	R	R	Initialize System Management Interrupt.
2A	G	OFF	A	OFF	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	G	G	R	OFF	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	G	G	A	OFF	Initializes all the output devices.
31	OFF	OFF	R	A	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	OFF	OFF	A	A	Initializes the silent boot module. Set the window for displaying text information.
37	OFF	G	A	A	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	G	OFF	R	R	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
39	G	OFF	R	A	Initializes DMAC-1 & DMAC-2.
3A	G	OFF	A	R	Initialize RTC date/time.
3B	G	OFF	A	A	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	G	G	R	R	Mid POST initialization of chipset registers.
40	OFF	R	OFF	OFF	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
50	OFF	R	OFF	R	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	OFF	R	G	R	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	OFF	R	R	OFF	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	OFF	A	R	A	Initialize Int-13 and prepare for IPL detection.
78	G	R	R	R	Initializes IPL devices controlled by BIOS and option ROMs.

7A	G	R	A	R	Initializes remaining option ROMs.
7C	G	A	R	R	Generate and write contents of ESCD in NVRam.
84	R	G	OFF	OFF	Log errors encountered during POST.
85	R	G	OFF	G	Display errors to the user and gets the user response for error.
87	R	G	G	G	Execute BIOS setup if needed / requested.
8C	A	G	OFF	OFF	Late POST initialization of chipset registers.
8D	A	G	OFF	G	Build ACPI tables (if ACPI is supported)
8E	A	G	G	OFF	Program the peripheral parameters. Enable/Disable NMI as selected
90	R	OFF	OFF	R	Late POST initialization of system management interrupt.
A0	R	OFF	R	OFF	Check boot password if installed.
A1	R	OFF	R	G	Clean-up work needed before booting to OS.
A2	R	OFF	A	OFF	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	R	G	R	OFF	Initialize runtime language module.
A7	R	G	A	G	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	A	OFF	R	OFF	Prepare CPU for OS boot including final MTRR values.
A9	A	OFF	R	G	Wait for user input at config display if needed.
AA	A	OFF	A	OFF	Uninstall POST INT1Ch vector and INT09h vector. De-initializes the ADM module.
AB	A	OFF	A	G	Prepare BBS for Int 19 boot.
AC	A	G	R	OFF	End of POST initialization of chipset registers.
B1	R	OFF	R	A	Save system context for ACPI.
00	OFF	OFF	OFF	OFF	Passes control to OS Loader (typically INT19h).

Table60: Bootblock Initialization Code Checkpoints

Check	Diagnostic LED Decoder G=Green, R=Red, A=Amber	Diagnostic LED Decoder G=Green, R=Red, A=Amber

point	Hi			Low	
Before D1	A	A	A	A	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	R	R	OFF	A	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	R	R	OFF	R	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	R	R	G	R	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	R	R	G	A	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	R	A	OFF	R	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	R	A	OFF	A	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	R	A	G	R	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	R	A	G	A	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	A	R	OFF	R	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	A	R	OFF	A	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	A	R	G	R	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.

6.2.2.1 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Table61: Bootblock Recovery Code Checkpoints

Check point	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Diagnostic LED Decoder G=Green, R=Red, A=Amber
	Hi			Low	
E0	R	R	R	OFF	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	A	R	R	G	Set up floppy controller and data. Attempt to read from floppy.
EA	A	R	A	OFF	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	A	R	A	G	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	A	A	A	G	Read error occurred on media. Jump back to checkpoint EB.
E9 or EA	A (A)	R (R)	R (A)	R (OFF)	Determine information about root directory of recovery media.
F0	R	R	R	R	Search for pre-defined recovery file name in root directory.
F1	R	R	R	A	Recovery file not found.
F2	R	R	A	R	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	R	R	A	A	Start reading the recovery file cluster by cluster.
F5	R	A	R	A	Disable L1 cache.
FA	A	R	A	R	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	A	R	A	A	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	R	A	R	R	The recovery file size does not equal the found flash part size.
FC	A	A	R	R	Erase the flash part.
FD	A	A	R	A	Program the flash part.
FF	A	A	A	A	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

6.2.2.2 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem. The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table62 : POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
1	Refresh timer test failed		Display message and beeps.
3	RAM R/W test failed		Display message and beeps.
6	KBC BAT Test failed		Display message and beeps.

6.2.2.3 BIOS Recovery Beep Codes

Table63 : BIOS Recovery Beep Codes

Beeps	Error Message	POST Progress Code	Description
1	Recovery Started	E9h	Start of recovery process
2 then 5	Recovery Boot Error	Flashing series of POST codes: EFh, F1h,cycle.	Unable to boot to floppy, ATAPI, or ATAPI CD-ROM. Recovery process will retry.

6.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 64 describes the bus initialization checkpoints.

Table 64. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 65 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 65. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned.

1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.
8	func#8, BBS ROM init for all buses.

Table 66 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 66. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	On-board System devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

7. Connector Pin-Outs and Jumper Blocks

7.1 Power Connectors

The main power supply connection is obtained using the 24-pin connector (only the first 20 pins are populated when using an ATX12V power supply).

12V CPU power is obtained using the 8-pin connector (only the first 4 pins are populated when using an ATX12V power supply).

The following table defines the pin-outs of the connectors.

Table 67. Power Connector Pin-out (J4J1)

Pin	Signal	Color	Pin	Signal	Color
1	+3.3Vdc	Orange	13	+3.3Vdc	Orange
2	+3.3Vdc	Orange	14	-12Vdc	Blue
3	COM	Black	15	COM	Black
4	+5Vdc	Red	16	PS_ON#	Green
5	COM	Black	17	COM	Black
6	+5Vdc	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR_OK	Gray	20	RSVD_(-5V)	White
9	5VSB	Purple	21	+5Vdc	Red
10	+12Vdc	Yellow	22	+5Vdc	Red
11	+12Vdc	Yellow	23	+5Vdc	Red
12	+3.3Vdc	Orange	24	COM	Black

Table 68. 12V CPU Power Connector (J9B1)

Pin	Signal
1	Ground
2	Ground
3	Ground
4	Ground
5	+12V
6	+12V
7	Unused
8	Unused

NOTE

The board will not boot if the 12V CPU power connector is not attached to the board.

Table 69. Auxiliary Signal Connector (J5G2)

Pin	Signal
1	SMB_SCLP
2	SMB_SDAP
3	PS_ALERT#
4	GND
5	3.3V

7.2 PCI Bus Connectors

Table 70. PCI Bus Connectors

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#) (See Note)	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK) (See Note)	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS) (See Note)	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI) (See Note)	B4	Not connected (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9[2]	Reserved	B9	Not connected (PRSNT1#) (See Note)	A40	SMBus Clock Line	B40	PERR#
A10	+5 V (I/O)	B10	Reserved[3]	A41	SMBus Data Line	B41	+3.3 V
A11	Reserved	B11	Not connected (PRSNT2#) (See Note)	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V aux	B14	Reserved[4]	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

Note:

1. The signals (in parentheses) are optional in the PCI specification and are not currently implemented.
2. On PCI Slot 6, A9 becomes P_REQ3#
3. On PCI Slot 6, B10 becomes P_GNT3#
4. On PCI Slot 6, B14 becomes CK_P_33M_S6 RISER

7.3 Front Panel Connector

A high density, 34-pin SSI header is provided to support a system front panel. The header contains reset, NMI, power control buttons, and LED indicators. The following table details the pin out of the header.

Table 71. High-Density Front Panel 34-Pin Header Pin Out (J3J4)

Pin	Function	Pin	Function
1	Power LED Anode	2	5VSB
3	Key	4	5VSB
5	Power LED Cathode	6	COOL LED Cathode
7	VCC3	8	5VSB
9	HDD Activity LED Cathode	10	SYSTEM LED Cathode
11	Power Switch	12	NIC#1 Activity LED Anode
13	GND	14	NIC#1 Activity LED Cathode
15	Reset Switch	16	RESUME I2C DATA
17	GND	18	RESUME I2C CLK
19	ACPI Sleep Switch	20	Unused
21	GND	22	NIC#2 Activity LED Anode
23	NMI Switch	24	NIC#2 Activity LED Cathode
25	Key	26	Key
27	5VSB	28	5VSB
29	ID LED Cathode	30	SYS RDY LED Cathode
31	ID Button Cathode	32	VCC
33	GND	34	Unused

7.4 VGA Connector

The following table details the pin out of the VGA connector.

Table 72. VGA Connector Pin-out (J7A1)

Pin	Signal Name
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND
6	GND
7	GND
8	GND
9	Fused VCC(+5V)
10	GND
11	No connection
12	V_MONID1
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	V_MONID2

7.5 NIC /USB Connector

The Intel Server Board SE7210TP1-E supports two Magjack1* connectors (RJ45). The following table details the pin out of the connector.

Table 73. Magjack Connector (RJ45, 10/100/1000) Pin Out (J6A2)

Pin	Signal Name	Pin	Signal Name
1	LAN_V_1P8	10	LAN_MDI_0*
2	LAN_MDI_2*	11	LAN_MDI_0
3	LAN_MDI_2	12	LAN_V_1P8
4	LAN_MDI_1	13	LAN_LINK_100*
5	LAN_MDI_1*	14	LAN_LINK
6	LAN_V_1P8	15	LAN_LINK_UP*
7	LAN_V_1P8	16	LAN_ACTLED*
8	LAN_MDI_3	17	GND
9	LAN_MDI_3*	18	GND

Table 74. Magjack Connector (RJ45, 10/100) Pin Out (J5A1)

Pin	Signal Name	Pin	Signal Name
1	Bypass cap to GND	10	NIC2_TDN
2	NIC2_MDI_MINUS2	11	NIC2_TDP
3	NIC2_MDI_PLUS2	12	Bypass cap to GND
4	NIC2_RDP	13	NIC2_SPEED_LED*
5	NIC2_RDN	14	3.3V Stdby/LINK_1000*
6	Bypass cap to GND	15	NIC2_LINK_LED#
7	Bypass cap to GND	16	NIC2_ACT_LED#
8	NIC2_MDI_PLUS3	17	GND
9	NIC2_MDI_MINUS3	18	GND

Table 75. Triple USB Pin Out (J9A2)

Pin	Signal Name	Pin	Signal Name
1	USB_BACK_PWR1	9	USB_BACK_PWR3
2	USB_BACK1_R#	10	USB_BACK3_R#
3	USB_BACK1_R	11	USB_BACK3_R
4	GND	12	GND
5	USB_BACK_PWR2	13	GND
6	USB_BACK2_R#	14	GND
7	USB_BACK2_R	15	GND
8	GND	16	GND

7.6 SATA/SATA RAID Connectors

The SE7210TP1-E board provides two SATA/SATA RAID connectors. The pin out for both connectors is identical and is listed in the following table.

Table 76. SATA 7-pin Connectors Pin Out (J3G1, J3G2)

Pin	Signal Name
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7, 8, 9	Ground

7.7 6300ESB I/O IDE Connectors

The SE7210TP1-E board provides two 40-pin, low-density 6300ESB I/O IDE connectors. The pin out for both connectors is identical and is listed in the following table.

Table 77. 6300ESB I/O IDE 40-pin Connector Pin Out (J4J2, J4J3)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Ground
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Not connected
33	PDA1 (Address 1)	34	GPIO_DMA66_Detect_Pri (GPIO_DMA66_Detect_Sec)
35	PDA0 (Address 0)	36	PDA2 (Address 2)
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	HD_LED_PRI*/HD_LED_SEC*	40	Ground

7.8 Front Panel USB Header

A header on the server board provides an option to support one additional USB connector. The pin out of the header is detailed in the following table.

Table 78. Front Panel USB Connector Pin-out (J5G1)

Pin	Signal Name	Pin	Signal Name
1	USB_FNT1_PWR	2	USB_FNT1_PWR
3	NC	4	USB_FRONT1*
5	NC	6	USB_FRONT1
7	Ground	8	Ground
9	Key	10	USB_ OC_FNT_R1

Note: USB ports may be assigned as needed.

7.9 Floppy Connector

The Intel Server Board SE7210TP1-E provides a 34-pin connector interface to the floppy drive controller. The following table details the pin out of the 34-pin floppy connector.

Table 79. 34-pin Floppy Connector Pin Out (J3H1)

Pin	Signal Name	Pin	Signal Name
1	GND	2	DENSEL
3	Key	4	NC
5	Key	6	DRVDEN1
7	GND	8	FDINDX#
9	GND	10	MTR0# (Motor Enable A)
11	GND	12	NC
13	GND	14	DS0# (Drive Select A)
15	GND	16	NC
17	NC	18	DIR# (Stepper Motor Direction)
19	GND	20	STEP# (Step Pulse)
21	GND	22	WDATA# (Write Data)
23	GND	24	WGATE# (Write Enable)
25	GND	26	TRK0# (Track 0)
27	NC	28	WRTPRT# (Write Protect)
29	GND	30	RDATA# (Read Data)
31	GND	32	HDSEL# (Side 1 Select)
33	GND	34	DSKCHG# (Diskette Change)

7.10 Serial Port Connector

The Intel Server Board SE7210TP1-E has one 9-pin D-sub serial port connector and one 2 x 5 serial port connector. The following tables detail the pin outs of these two ports.

Table 80. 9-pin Serial A Port Pin Out (J8A1)

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	RXD (Receive Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	GND
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

Table 81. 10-pin Header Serial B Port Pin Out (J8A2)

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	DSR (Data Set Ready)
3	RXD (Receive Data)
4	RTS (Request to Send)
5	TXD (Transmit Data)
6	CTS (Clear to Send)
7	DTR (Data Terminal Ready)
8	RI (Ring indicator)
9	GND
10	Key

7.11 Keyboard and Mouse Connector

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch* circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the server should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

Table 82. Keyboard /Mouse PS/2 Connector Pin Out (J9A1)

Connector	Pin	Signal Name
Keyboard	1	Data
	2	NC
	3	GND
	4	+5 V (Fused)
	5	Clock
	6	NC
Mouse	7	Data
	8	NC
	9	GND
	10	+5 V (Fused)
	11	Clock
	12	NC
	13	NC
	14	NC
	15	NC
	16	NC
	17	NC

7.12 Miscellaneous Headers

7.12.1 Fan Headers

The Intel Server Board SE7210TP1-E provides seven 3-pin fan headers. All fans use direct 12 volts. The six system fans and one processor fan are wired to the input of the Hardware Management (ADM1027 or ADT7463/SIO) and are monitored by Intel Server Management.

Table 83. Three-Pin Fan Headers Pin-Out

Pin	Signal Name	Type	Description
1	GND	Power	GROUND is the power supply ground
2	FAN_FRONT1_PWR FAN_FRONT2_PWR FAN_REAR_PWR	Power	12 V
3	Fan Tach	Out	FAN_TACH signal is connected to the Hardware Management (ADM1027or ADT7463/ SIO) to monitor the fan speed

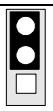
7.13 System Recovery and Update Jumper

⚠ CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the server before changing a jumper setting. Otherwise, the board could be damaged.

This 3-pin jumper block determines the BIOS Setup program mode. Table 84 describes the jumper settings for the two modes: normal and recovery.

Table 84. BIOS Setup Configuration Jumper Settings (J1D1)

Function/Mode	Jumper Setting	Configuration
Normal Boot	13-14 	The BIOS uses current configuration information and passwords for booting.
Recovery	14-15 	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

7.14 Clear CMOS Jumper

⚠ CAUTION
Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the server before changing a jumper setting. Otherwise, the board could be damaged.

This 3-pin jumper block allows the user to clear CMOS. Table 85 describes the jumper settings for the two modes: normal and clear CMOS. When the jumper is set to Clear CMOS mode and the server is powered-up, the contents of the CMOS are cleared.

Table 85. Clear CMOS Jumper Settings (J1D1)

Function/Mode	Jumper Setting	Configuration
Normal	1-2 	Normal Operation.
Clear CMOS	2-3 	Clears contents of CMOS area.

7.15 PASSWORD Jumper

⚠ CAUTION
Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the server before changing a jumper setting. Otherwise, the board could be damaged.

This 3-pin jumper block allows the user to clear PASSWORD. Table 86 describes the jumper settings for the two modes: normal and clear PASSWORD. When the jumper is set to Clear PASSWORD mode and the server is powered-up, the contents of the PASSWORD are cleared.

Table 86. PASSWORD Jumper Settings (J1D1)

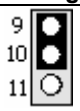
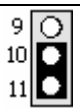
Function/Mode	Jumper Setting	Configuration
Normal	5-6 	Normal Operation.
Clear PASSWORD	6-7 	Clears contents of PASSWORD area.

7.16 Write protected Jumper

⚠ CAUTION
Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the server before changing a jumper setting. Otherwise, the board could be damaged.

This 3-pin jumper block allows the user to BIOS write protected. Table 89 describes the jumper settings for the two modes: normal and BIOS BOOT-BLOCK WRITE ENABLE. When the jumper is set to BIOS BOOT-BLOCK WRITE ENABLE mode and the server is powered-up, the BIOS update can be executed.

Table 87. BIOS WRITE PROTECTED Jumper Settings (J1D1)

Function/Mode	Jumper Setting	Configuration
WRITE PROTECTED	9-10 	Normal Operation.
BIOS BOOT-BLOCK WRITE ENABLE	10-11 	BIOS BOOT-BLOCK WRITE ENABLE

8. Environmental Specifications

8.1 Absolute Maximum Ratings

Operating a Server Board SE7210TP1-E at conditions, beyond those shown in the following table, may cause permanent damage to the system. The table is provided for stress testing purposes only. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 88. Absolute Maximum Ratings

Operating Temperature	5 degrees C to 50 degrees C [1]
Storage Temperature	-55 degrees C to +150 degrees C
Voltage on any signal with respect to ground	-0.3 V to Vdd + 0.3V [2]
3.3 V Supply Voltage with Respect to ground	-0.3 V to 3.63 V
5 V Supply Voltage with Respect to ground	-0.3 V to 5.5 V

Notes:
1. Chassis design must provide proper airflow to avoid exceeding the Intel® Pentium® 4 processor maximum case temperature.
2. VDD means supply voltage for the device.

8.2 SE7210TP1-E Power Budget

The following table shows the power consumed on each supply line for an Intel Server Board SE7210TP1-E that is configured with one Intel Pentium 4 processor (pulling max current), all PCI slots full and pulling max amount of current, memory completely full, USB pulling max current, and fans assuming max current. The numbers provided in the table should be used for reference purposes only. Different hardware configurations will produce different numbers. The numbers in the table reflect a common usage model operating at higher-than-average stress levels.

Table 89. SE7210TP1-E Power Budget

Device(s)	3.3V	+5V	+12V	-12V	5V Standby	
Processors	0	0	10.73			
Memory DIMMs	0	10.44	0			
Server board	4.96	4.633	0.25	0.1	1.8	
Fans	0	0	0.8			
Keyboard/Mouse	0	0.14	0			
PCI slots	13.65	3	0.5			
Total Current	18.61	18.213	12.28	0.1	1.8	**Total**
Total Power	61.413	91.065	147.36	1.2	9	310.038

8.3 Product Regulatory Compliance

8.3.1 Product Safety Compliance

The SE7210TP1-E complies with the following safety requirements:

- UL 1950 - CSA 950 (US/Canada)
- EN 60 950 (European Union)
- IEC60 950 (International)
- CE – Low Voltage Directive (73/23/EEC) (European Union)
- EMKO-TSE (74-SEC) 207/94 (Nordics)
- GOST R 50377-92 (Russia)

8.3.2 Product EMC Compliance

The SE7210TP1-E has been has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations when installed in a compatible Intel host system. For information on compatible host system(s), contact your local Intel representative.

- FCC (Class A Verification) – Radiated & Conducted Emissions (USA)
- ICES-003 (Class A) – Radiated & Conducted Emissions (Canada)
- CISPR 22, 3rd Edition (Class A) – Radiated & Conducted Emissions (International)
- EN55022 (Class A) – Radiated & Conducted Emissions (European Union)
- EN55024 (Immunity) (European Union)
- CE – EMC Directive (89/336/EEC) (European Union)
- VCCI (Class A) – Radiated & Conducted Emissions (Japan)
- AS/NZS 3548 (Class A) – Radiated & Conducted Emissions (Australia / New Zealand)
- RRL (Class A) Radiated & Conducted Emissions (Korea)
- BSMI CNS13438 (Class A) Radiated & Conducted Emissions (Taiwan)
- GOST R 29216-91 (Class A) Radiated & Conducted Emissions (Russia)
- GOST R 50628-95 (Immunity) (Russia)

8.3.3 Product Regulatory Compliance Markings

This product is provided with the following product certification markings:

Product Certification Markings

UL Recognition Mark	
CE Mark	
Russian GOST Mark	
Australian C-Tick Mark	
BSMI DOC Marking	
BSMI EMC Warning	警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策
RRL MIC Mark	

8.4 Electromagnetic Compatibility Notices

8.4.1 FCC (USA)

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class A or B limits may be attached to this server product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.
All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

8.4.2 INDUSTRY CANADA (ICES-003)

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled: "Digital Apparatus," ICES-003 of the Canadian Department of Communications.
Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Apparelis Numériques", NMB-003 édictee par le Ministre Canadian des Communications.

8.4.3 Europe (CE Declaration of Conformity)

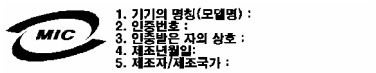
This product has been tested in accordance to, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

8.4.4 Taiwan Declaration of Conformity

This product has been tested and complies with CNS13438. The product has been marked with the BSMI DOC mark to illustrate compliance.

8.4.5 Korean RRL Compliance

This product has been tested and complies with MIC Notices No. 1997-41 and 1997-42. The product has been marked with the MIC logo to illustrate compliance.



The English translation for the above is as follows:
1. Type of Equipment (Model Name): SE7210TP1-E
2. Certification No.: Contact Intel Representative
3. Name of Certification Recipient: Intel
4. Date of Manufacturer: Marked on Product
5. Manufacturer / Nation : Intel

8.4.6 Australia / New Zealand

This product has been tested and complies with AS/NZS 3548. The product has been marked with the C-Tick mark to illustrate compliance.

8.5 Replacing the Back-Up Battery

The lithium battery on the server board powers the RTC for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

⚠ WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

⚠ ADVARSEL**!**
Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

⚠ ADVARSEL
Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

⚠ VARNING
Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

⚠ VAROITUS
Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

8.6 Calculated Mean Time Between Failures (MTBF)

The MTBF (Mean Time Between Failures) for the Intel Server Board SE7210TP1-E as configured from the factory is shown in the table below.

Product Code	Calculated MTBF	Operating Temperature
SE7210TP1	110,894 hours	55 degrees C
SE7210TP1SCSI	103,568 hours	55 degrees C

8.7 Mechanical Specifications

The following figure shows the Intel Server Board SE7210TP1-E general-purpose chassis I/O shield mechanical drawing. If the Intel Server Board SE7210TP1-E is used in a 1U chassis, the user will need to obtain the I/O shield directly from the chassis vendor.

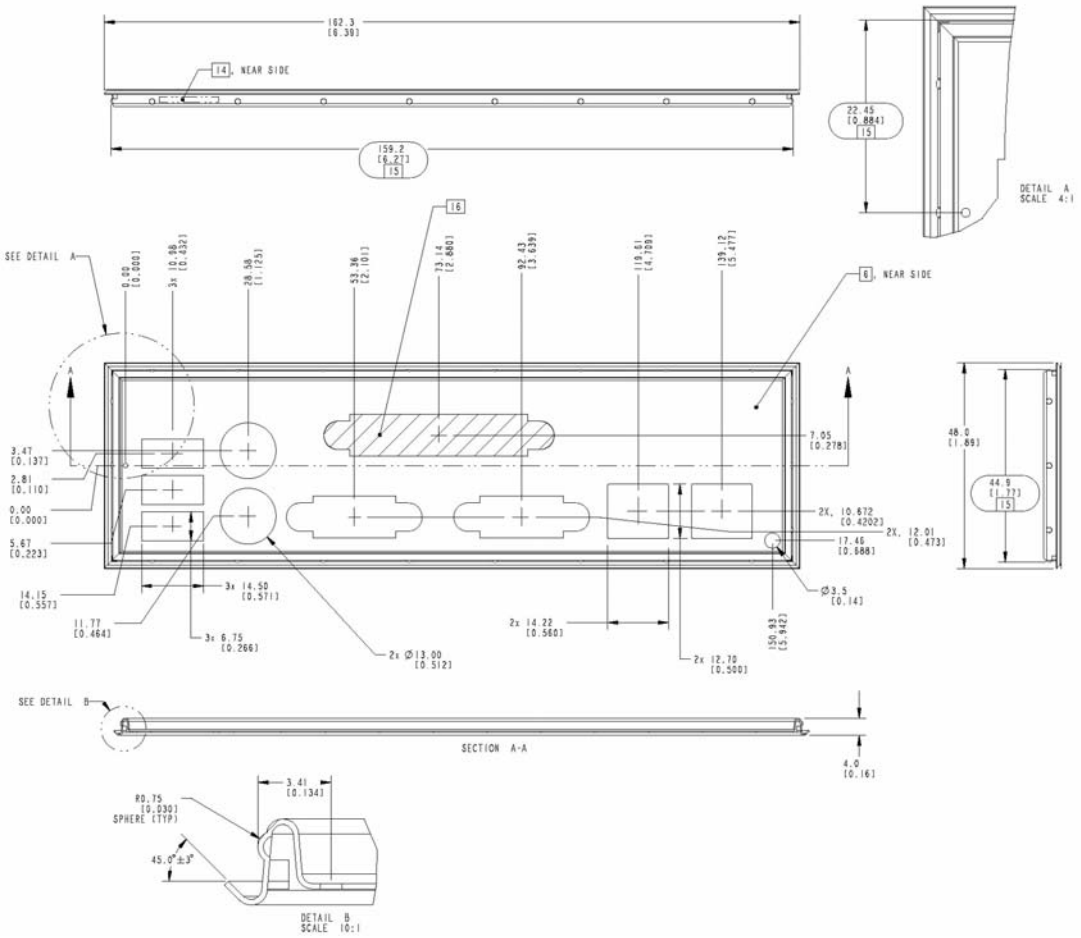


Figure 14. Intel Server Board SE7210TP1-E I/O Shield Drawing

Appendix A: Glossary of Terms

This appendix contains important terms used in the preceding chapters. For ease of use, numeric entries are listed first (e.g., “82460GX”) with alpha entries following (e.g., “AGP 4x”). Acronyms are then entered in their respective place, with non-acronyms following.

Term	Definition
ACPI	Advanced Configuration and Power Interface
ASIC	Application Specific Integrated Circuit
BIOS	Basic input/output system
Byte	8-bit quantity.
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DCD	Data Carrier Detect
DMA	Direct Memory Access
ECC	Error Correcting Code
EMC	Electromagnetic Compatibility
EPS	External Product Specification
ESCD	Extended System Configuration Data
FDC	Floppy Disk Controller
FIFO	First-In, First-Out
FRU	Field replaceable unit
GB	1024 MB.
GPIO	General purpose I/O
GUID	Globally Unique ID
Hz	Hertz (1 cycle/second)
HDG	Hardware Design Guide
I^2C	Inter-integrated circuit bus
IA	Intel® architecture
IRQ	Interrupt Request
ITP	In-target probe
KB	1024 bytes
LAN	Local area network
LBA	Logical Block Address
LCD	Liquid crystal display
LPC	Low pin count
MB	1024 KB
MBE	Multi-Bit Error
Ms	milliseconds
MTBF	Mean Time Between Failures
NIC	Network Interface Card
NMI	Non-maskable Interrupt
OEM	Original equipment manufacturer
PBGA	Pin Ball Grid Array
PERR	Parity Error

Term	Definition
PIO	Programmable I/O
PME	Power Management Event
PnP	Plug and Play
POST	Power-on Self Test
PWM	Pulse-Width Modulator
RAM	Random Access Memory
RI	Ring Indicate
ROM	Read Only Memory
RTC	Real Time Clock
SBE	Single-Bit Error
SCI	System Configuration Interrupt
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic RAM
SEL	System event log
SERR	System Error
SM	Server Management
SMI	Server management interrupt. SMI is the highest priority nonmaskable interrupt
SMM	System Management Mode
SMS	System Management Software
SPD	Serial Presence Detect
SSI	Server Standards Infrastructure
TPS	Technical Product Specification
UART	Universal asynchronous receiver and transmitter
USB	Universal Serial Bus
VGA	Video Graphic Adapter
VRM	Voltage Regulator Module
Word	16-bit quantity