# Intel® Server System SR1640TH

## *Technical Product Specification*

*Intel order number: E94847-001*


**Revision 1.0**

**March 2010**

**Enterprise Platforms and Services Marketing**

# Revision History

| Date | Revision Number | Modifications |
|---|---|---|
| March 26, 2010 | 1.0 | Initial release. |
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# 1. Introduction

This Technical Product Specification (TPS) provides system specific information detailing the features, functionality, and high-level architecture of the Intel® Server System SR1640TH including the server board S3420TH inside system.

In addition, you can obtain design-level information for specific sub-systems by ordering the External Product Specifications (EPS) or External Design Specifications (EDS) for a given sub-system. EPS and EDS documents are not publicly available. They are only made available under NDA with Intel and must be ordered through your local Intel representative. For a complete list of available documents, refer to the *Reference Documents* section at the end of this document.

The Intel® Server System SR1640TH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Refer to the *Intel® Server System SR1640TH Specification Update* for published errata.

## 1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Functional Architecture
- Chapter 3 – Power Sub-System
- Chapter 4 – Cooling Sub-System
- Chapter 5 – Hard Disk Driver Support
- Chapter 6 – Front Panel Control and Indicators
- Chapter 7 – Configuration Jumpers
- Chapter 8 – Environmental and Regulatory Specifications
- Appendix A – Integration and Usage Tips
- Appendix B – Integrated BMC sensor tables
- Appendix C – POST code LED decoders
- Appendix D – POST Code Errors
- Glossary
- Reference Documents

## 1.2 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

# 2. Functional Architecture

The Intel® Server System SR1640TH is a rack mount 1U server system, purpose-built for high-density and lowest total cost of ownership in dense computing and hosting/IPDC applications. The system is integrated with two dedicated Intel® Server Boards S3420TH, each board contains 2 computing nodes. The two server boards in Intel® Server System SR1640TH are installed in two system trays each. There are totally four 3.5 inch fixed SAS or SATA hard drives bays in system, each system tray contains two HDD bays, supporting total four computing nodes respectively.

This chapter provides a high-level overview of the system features. The following chapters provide greater detail for each major system component or feature.

**Table 1. System Feature Set**

| Feature | Description |
|---|---|
| Server board | Intel® 3420 Platform Controller Hub (PCH) based dual-node server board S3420TH. Two identical boards are in one SR1640TH system. |
| Processor | Each node supports one Intel® Xeon® Processor 3400 series and Intel® Core™ i3 processors in FC-LGA 1156 Socket B package with up to 95 W Thermal Design Power (TDP) .<br>2.5GT/s point-to-point DMI interface to PCH<br>VRD 11.1 is supported. |
| Memory | Four DDR3 DIMMs slots per processor across two memory channels, total eight DIMMs per board.<br>For one node:<br>DDR3 1333/1066/800M UDIMM or RDIMM.<br>2 Memory Channels, 2 DIMM slots per channel<br>8GB (dual rank with 1Gb) max with X8 ECC UDIMM<br>16GB (quad rank with 1Gb) max RDIMM |
| Chipset | Intel® Chipset which includes the following components:<br>Intel® 3420 chipset Platform Controller Hub (PCH)<br>ServerEngines* Pilot II controller (integrated BMC), supports the following functions.<br>Integrated 2D video controller<br>Super IO on LPC<br>Baseboard Management Controller (BMC) based on ARM946E-S |
| Hard Disk Drive Supported | One fixed 3.5-inch SATA/SAS HDD per node, total four 3.5-inch HDDs are supported in system. |
| System Connectors / Headers | External I/O connectors per node:<br>One DB-15 Video connectors<br>Two RJ-45 connectors for 10/100/1000 LAN (82574L based GE NIC, one port connects to iBMC under share mode)<br>Two USB 2.0 connectors<br>One RJ-45 10/100 LAN port dedicated for management<br>Internal connectors/headers per node:<br>Two USB 2.0 ports with headers on motherboard<br>One USB 2.0 port with headers dedicated for internal USB flash<br>One RMM3 Lite-V connector to support optional Intel® Remote Management Module 3 Lite-V module<br>One SAS 4i connector for SATAII ports (shared by two nodes and two SATAII ports from each node) |

| Feature | Description |
|---|---|
| | Three 8-pin system FAN headers per board<br>One power supply connector with PMBus enabled, shared by two nodes |
| System Fan Support | Three sets of axial FAN per board<br>Total six sets of system FANs in chassis |
| Add-in Adapter Support | No support for add-in card |
| On-board Video | **On-board Server Engines* Pilot II Controller**<br>ServerEngine iBMC<br>External 64MB DDR2 667MHz Memory |
| LAN Support | Two 10/100/1000 ports provided by Intel® 82574L connected to PCI-E x1 interface to processor.<br>One Gigabit Ethernet connects to iBMC through NC-SI interface (shared mode)<br>Two 10/100/1000 Base-TX interfaces through RJ45 connectors with integrated magnetic<br>One 10/100M PHY (KSZ8041NL) connected to iBMC through RMII interface as dedicated management port. |
| System Power | Dual 450-W power supply, 80 plus silver with PFC, configured as one power supply per board. |
| System Management | **On-board Server Engines* Pilot II Controller.**<br>Integrated Baseboard Management Controller (Integrated BMC), IPMI 2.0 compliant<br>Processor on die temperature monitoring thru PECI interface to iBMC<br>Board temperature measurement<br>Fan speed monitoring & control<br>Voltage monitoring<br>IPMI2.0 based server management<br>Power management via PMBus |

The Intel® Server System SR1640TH system is supporting all Intel® Xeon® 3400 series and Intel® Core™ i3 processors with TDP 95 W and below. Supported processor list can be found at: http://support.intel.com/support/motherboards/server/SR1640TH/

## 2.1 System Views

There are 2 trays in SR1640TH system chassis. Each tray contains one computing board with system FANs and control panel.

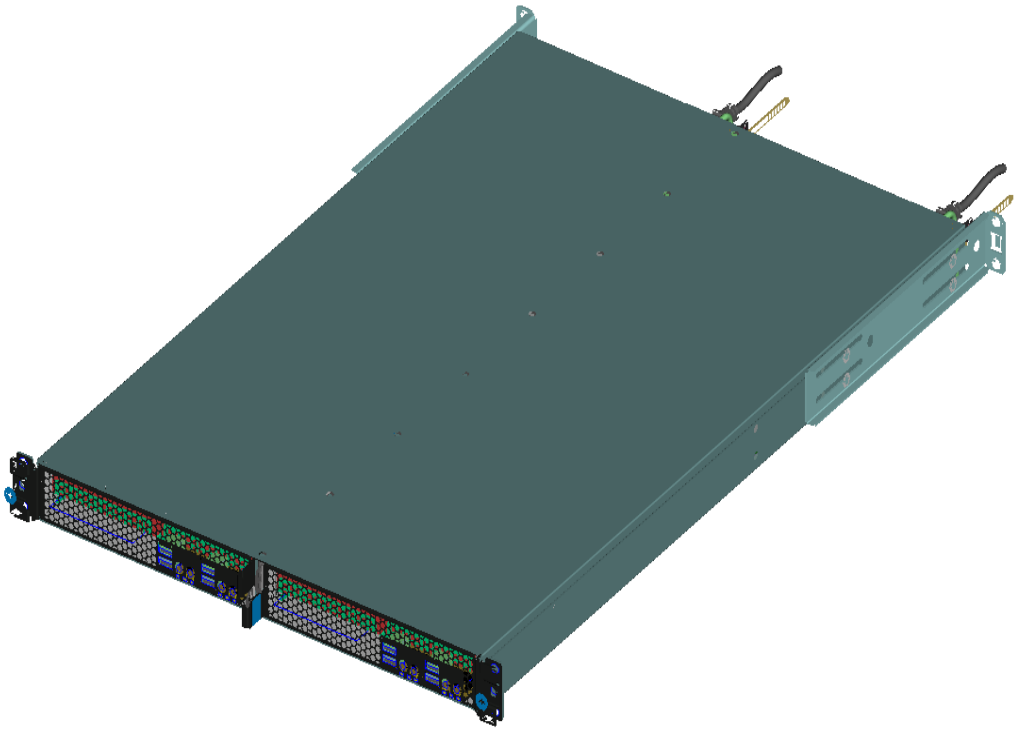


**Figure 1. System Overview**

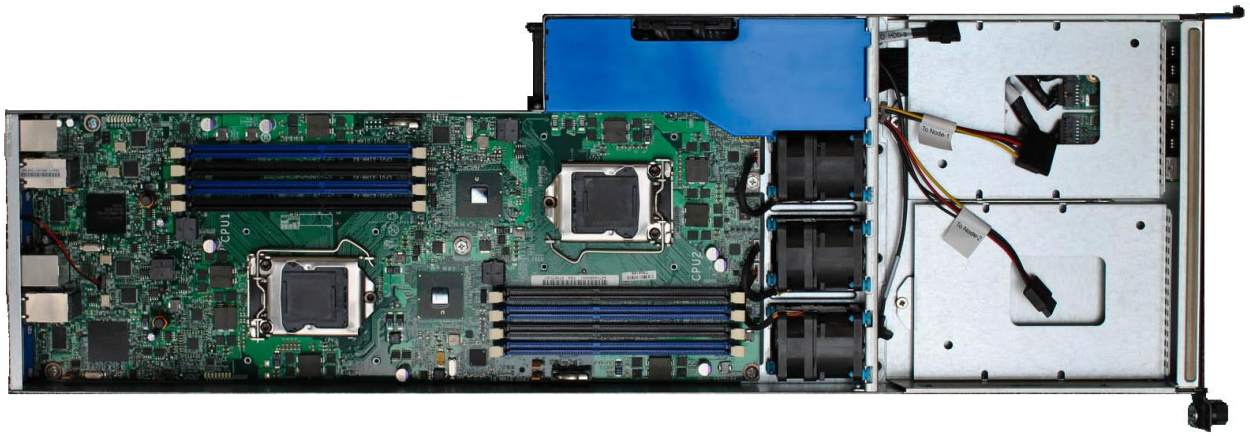


**Figure 2. Single tray overview (Left Tray)**

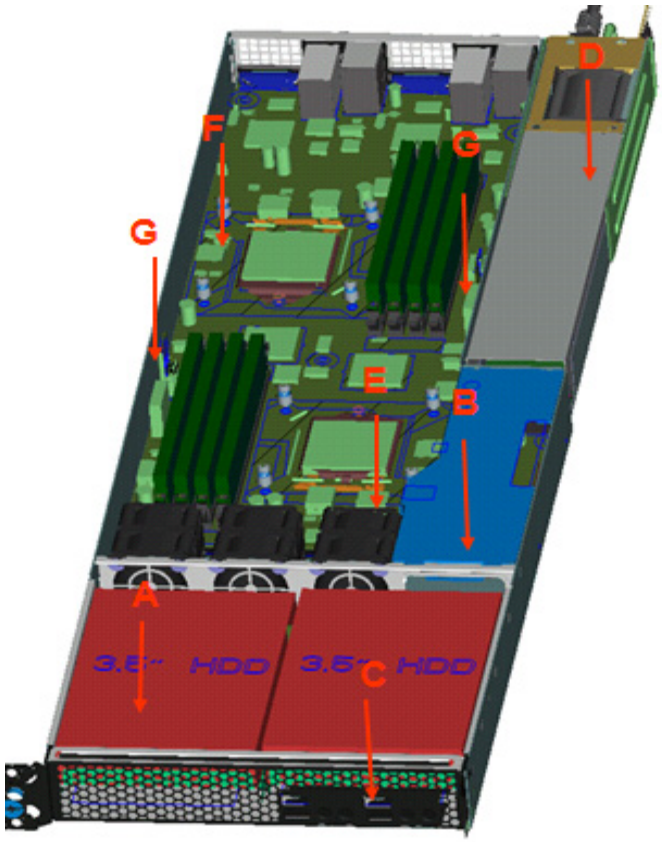
**Figure 3. System trays overview with power supply units**

## 2.2 System Dimensions

**Table 2. Chassis Dimensions**

| | | |
|---|---|---|
| Height | 44 mm | 1.73 inches |
| Width without rails | 440 mm | 17.32 inches |
| Width with rails | 456.6 mm | 17.97 inches |
| Depth without CMA | 690 mm | 26.77 inches |
| Weight<br>Chassis – basic configured (0 drives)<br>Chassis – fully configured (4 drives) | <br>14.6 kg<br>17.8 kg | <br>32.19 lbs<br>39.25 lbs |

## 2.3 System Components




| | | | |
|---|---|---|---|
| **A** | Fixed 3.5 inch HDD bays | **F** | Dual-node server board S3420TH |
| **B** | Air duct | **G** | RMM3 Lite-V module (optional) |
| **C** | Front control pane | | |
| **D** | Power supply unit | | |
| **E** | System Fans Module | | |

**Figure 4. System tray Components**

## 2.4 Server Board Overview

Intel® Server System SR1640TH supports two dual-node server board S3420TH in chassis. The following sections provide an overview of the server board feature sets.

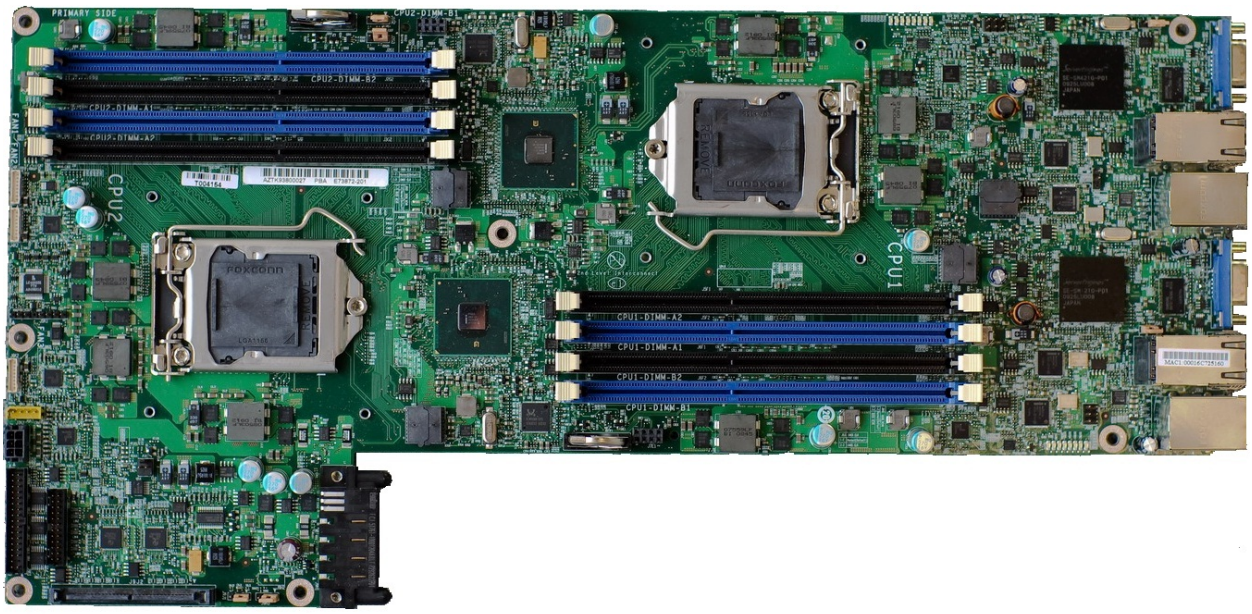



**Figure 5. Single server board S3420TH view**

### 2.4.1 Server board architecture

The server board included in Intel® Server System SR1640TH is a compact-optimized dual-node entry server board. It is intended for any front-end application in iPDC or high-dense rack mount installation. This product targets high power efficiency and low cost with good performance. Below is the block diagram of the server board.

The architecture and design of the server board S3420TH is based on the Intel® 3420 Chipset. The chipset is designed for systems based on the Intel® Xeon® processor in the FC-LGA 1156 socket package. The chipset contains two main components:

- Intel® 3420 Chipset(PCH)
- Server Engines* Pilot II Controller

This chapter provides a high-level description of the functionality associated with each chipset component and the architectural blocks that make up the server board.

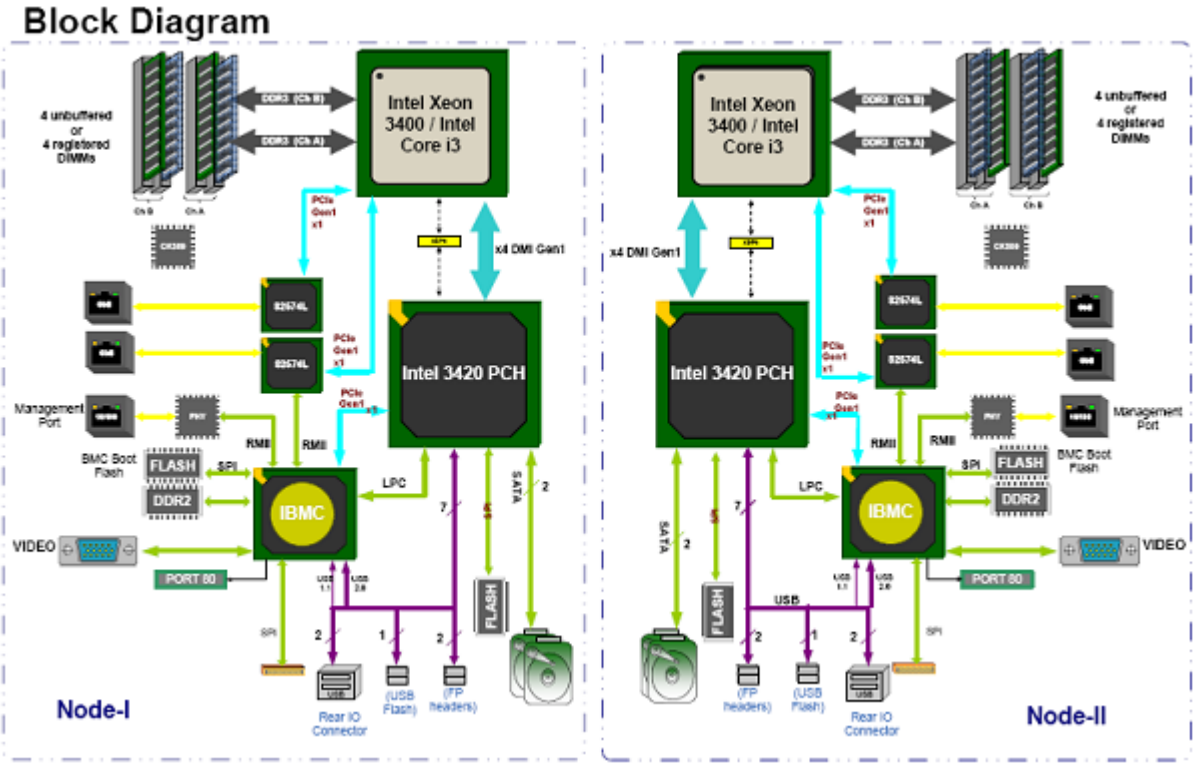



**Figure 6. Server board S3420TH block diagram**

By high density design philosophy, there are two computing nodes on one server board S3420TH. These two nodes are identical in logic, but they are separated on design without any link between them, including any power rail. Two nodes share one PSU and three system fans.

### 2.4.2 Processor sub-system

The Intel® Server Board S3420TH supports the following processor:

- Intel® Xeon® 3400 Processor series
- Intel® Core™ i3 processor

The Intel® Xeon® 3400 Series processors are made up of multi-core processors based on the 45 nm processor technology. The Intel® Core™ i3 processor is made up of dual core processor based on the 32 nm processor technology.

#### 2.4.2.1 Intel® Xeon® 3400 Processor

The Intel® Xeon® 3400 Series processors highly integrated solution variant is composed of four Nehalem-based processor cores.

- FC-LGA 1156 socket package with 2.5 GT/s.
- Up to 95 W Thermal Design Power (TDP); processors with higher TDP are not supported.

The server board does not support previous generations of the Intel® Xeon® processors.

#### 2.4.2.2 Intel® Core™ i3 Processor

The Intel® Core™ i3 Series processors highly integrated solution variant is composed of two processor cores.

- FC-LGA 1156 socket package with 2.5 GT/s.
- Up to 95 W Thermal Design Power (TDP); processors with higher TDP are not supported.

Please get the detail supported processor list from Intel website.

#### 2.4.2.3 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is featured on certain processors in the Intel® Xeon® Processor 3400 Series. Intel® Turbo Boost Technology opportunistically and automatically allows the processor to run faster than the marked frequency if the processor is operating below power, temperature, and current limits. This results in increased performance for both multi-threaded and single-threaded workloads.

Intel® Turbo Boost Technology operation:

- Turbo Boost operates under Operating System control – It is only entered when the operating system requests the highest (P0) performance state.
- Turbo Boost operation can be enabled or disabled by BIOS.
- Turbo Boost converts any available power and thermal headroom into higher frequency on active cores. At nominal marked processor frequency, many applications consume less than the rated processor power draw.
- Turbo Boost availability is independent of the number of active cores.
- Maximum Turbo Boost frequency depends on the number of active cores and varies by processor configuration.
- The amount of time the system spends in Turbo Boost operation depends on workload, operating environment, and platform design.

If the processor supports the Intel® Turbo Boost Technology feature, the BIOS Setup provides an option to enable or disable this feature. The default state is enabled.

#### 2.4.2.4 Simultaneous Multithreading (SMT)

Most Intel® Xeon® processors support Simultaneous Multithreading (SMT). The BIOS detects processors that support this feature and enables the feature during POST.

If the processor supports this feature, the BIOS Setup provides an option to enable or disable this feature. The default is enabled.

#### 2.4.2.5 Enhanced Intel SpeedStep® Technology

Intel® Xeon® processors support the Geyserville3 feature of the Enhanced Intel SpeedStep® technology. This feature changes the processor operating ratio and voltage similar to the Thermal Monitor 1 (TM1) feature. The BIOS implements the Geyserville3 feature in conjunction with the TM1 feature. The BIOS enables a combination of TM1 and TM2 according to the processor BIOS writer's guide.

### 2.4.3 Memory Subsystem

The Intel® Xeon® 3400 series processor has an Integrated Memory Controller (IMC) in its package. Each Intel® Xeon® 3400 series processor produces up to two DDR3 channels of

memory. Each DDR3 channel in the IMC supports up to two DDR3 RDIMM/UDIMM slots. The DDR3 RDIMM frequency can be 800/1066/1333 MHz. DDR3 UDIMM frequency can be 1066/1333 MHz. All RDIMMs and UDIMMs include ECC (Error Correction Code) operation. Various speeds and memory technologies are supported.

The Intel® Core™ i3 series processor has an Integrated Memory Controller (IMC) supports DDR3 protocols with two independent, 64-bit wide channels each accessing one or two DIMMs. **Only DDR3 UDIMM can be supported with the Intel® Core™ i3 series processor.**

RAS (Reliability, Availability, and Serviceability) is not supported on the server board S3420TH in Intel® Server System SR1640TH.

#### 2.4.3.1 Memory Sizing and Configuration

The server board S3420TH in Intel® Server System SR1640TH supports various memory module sizes and configurations. These combinations of sizes and configurations are valid only for DDR3 DIMMs approved by Intel® Corporation.

Server board BIOS supports:

- DIMM sizes of 1 GB, 2 GB, and 4 GB.
- DIMMs composed of DRAM using 2 Gb technology.
- DRAMs organized as single rank, dual rank, or quad rank DIMMS.
- DIMM speeds of 800, 1066, or 1333 MT/s.
- Registered or Unregistered (unbuffered) DIMMs (RDIMMs or UDIMMs).

**Note**: UDIMMs should be ECC, and may or may not have thermal sensors; RDIMMs must have ECC and must have thermal sensors.

Server board S3420TH BIOS has the below limitations:

- 256 Mb technology, x4 DRAM on UDIMM, and quad rank UDIMM are NOT supported
- x16 DRAM on UDIMM is not supported on combo routing
- Memory suppliers not productizing native 800 ECC UDIMMs
- Intel® Xeon® 3400 Series support all timings defined by JEDEC.
- 256 Mb/512 Mb technology, x4 and x16 DRAMs on RDIMM are NOT supported
- All channels in a system will run at the fastest common frequency
- No mixing of registered and unbuffered DIMMs
- No mixing of different ranks or speeds on UDIMM or RDIMM.

#### 2.4.3.2 Post Error Codes

The range {0xE0 - 0xEF} of POST codes is used for memory errors in early POST. In late POST, this range is used for reporting other system errors.

- **0xE8 - No Usable Memory Error**: If no memory is available, the system emits POST Diagnostic LED code 0xE8 and halts the system.
- **0xE8 - Configuration Error**: If a DDR3 DIMM has no SPD information, the BIOS treats the DIMM slot as if no DDR3 DIMM is present on it. Therefore, if this is the only DDR3 DIMM installed in the system, the BIOS halts with POST Diagnostic LED code 0xE8 (no usable memory) and halts the system.

- **0xEB - Memory Test Error**: If a DDR3 DIMM or a set of DDR3 DIMMs on the same memory channel (row) fails HW Memory BIST but usable memory remains available, the BIOS emits a beep code and displays POST Diagnostic LED code 0xEB momentarily during the beeping and then continues POST. If all of the memory fails HW Memory BIST, the system acts as if no memory is available, beeping and halting with the POST Diagnostic LED code 0xE8 (No Usable Memory) displayed.
- **0xEA - Channel Training Error**: If the memory initialization process is unable to properly perform the DQ/DQS training on a memory channel, the BIOS emits a beep code and displays POST Diagnostic LED code 0xEA momentarily during the beeping. If there is usable memory in the system on other channels, POST memory initialization continues. Otherwise, the system halts with POST Diagnostic LED code 0xEA staying displayed.
- **0xED - Population Error**: If the installed memory contains a mix of RDIMMs and UDIMMs, the system halts with POST Diagnostic LED code 0xED.
- **0xEE - Mismatch Error**: If more than two quad-ranked DIMMs are installed on any channel in the system, the system halts with POST Diagnostic LED code 0xEE.

#### 2.4.3.3 Publishing System Memory

The BIOS displays the Total Memory of the system during POST if Quiet Boot is disabled in the BIOS setup. This is the total size of memory discovered by the BIOS during POST, and is the sum of the individual sizes of installed DDR3 DIMMs in the system.

The BIOS displays the Effective Memory of the system in the BIOS Setup. The term Effective Memory refers to the total size of all active DDR3 DIMMs (not disabled) and not used as redundant units.

The BIOS provides the total memory of the system in the main page of the BIOS setup. This total is the same as the amount described by the first bullet in this section.

If Quiet Boot is disabled, the BIOS displays the total system memory on the diagnostic screen at the end of POST. This total is the same as the amount described by the first bullet in this section.

The BIOS provides the total amount of memory in the system.

##### 2.4.3.3.1 Memory Reservation for Memory-mapped Functions

A region of size 40 MB of memory below 4 GB is always reserved for mapping chipset, processor, and BIOS (flash) spaces as memory-mapped I/O regions. This region appears as a loss of memory to the operating system. In addition to this loss, the BIOS creates another reserved region for memory-mapped PCIe functions, including a standard 64 MB or 256 MB of standard PCI Express* MMIO configuration space.

If PAE is turned on in the operating system, the operating system reclaims all these reserved regions.

In addition to this memory reservation, the BIOS creates another reserved region for memory-mapped PCI Express* functions, including a standard 64 MB or 256 MB of standard PCI Express* Memory Mapped I/O (MMIO) configuration space. This is based on the selection of Maximize Memory below 4 GB in the BIOS Setup.

If this is set to Enabled, the BIOS maximizes usage of memory below 4 GB for an operating system without PAE capability by limiting PCI Express* Extended Configuration Space to 64 buses rather than the standard 256 buses. This is done using the MAX_BUS_NUMBER

feature offered by the Intel® S3420 I/O Hub and a variably-sized Memory Mapped I/O region for the PCI Express* functions.

#### 2.4.3.3.2 High-Memory Reclaim

When 4 GB or more of physical memory is installed (physical memory is the memory installed as DDR3 DIMMs), the reserved memory is lost. However, the Intel® 3420 chipset provides a feature called high-memory reclaim, which allows the BIOS and operating system to remap the lost physical memory into system memory above 4 GB (the system memory is the memory the processor can see).

The BIOS always enables high-memory reclaim if it discovers installed physical memory equal to or greater than 4 GB. For the operating system, the reclaimed memory is recoverable only if the PAE feature in the processor is supported and enabled. Most operating systems support this feature. For details, see the relevant operating system manuals.

#### 2.4.3.3.3 ECC Support

Only ECC memory is supported on server board S3420TH.

### 2.4.3.4 Memory Map and Population Rules

The following nomenclature is followed for DIMM sockets:

**Table 3. Standard Platform DIMM Nomenclature**

| Channel A | | Channel B | |
|---|---|---|---|
| A1 | A2 | B1 | B2 |

#### 2.4.3.4.1 TableMemory Subsystem Operating Frequency Determination

The rules for determining the operating frequency of the memory channels are simple, but not necessarily straightforward. There are several limiting factors, including the number of DIMMs on a channel and organization of the DIMM - that is, either single-rank (SR), dual-rank (DR), or quad-rank (QR):

- The speed of the processor's IMC is the maximum speed possible.
- The speed of the slowest component – the slowest DIMM or the IMC – determines the maximum frequency, subject to further limitations.
- A single 1333-MHz DIMM (SR or DR) on a channel may run at full 1333-MHz speed.
- If two SR/DR DIMMs are installed on a channel, the speed is limited to 1066 MHZ.
- A single QR RDIMM on a channel is limited to 1066 MHz.
- Two QR RDIMMs or a mix of QR + SR/DR on a channel is limited to 800 MHz.

#### 2.4.3.4.2 Memory Subsystem Nomenclature

1. DIMMs are organized into physical slots on DDR3 memory channels that belong to processor sockets.
2. The memory channels are identified as channels A, B.
3. For Intel® Xeon® 3400 Series, each socket can support a maximum of four DIMM sockets (two DIMM sockets per channel), which can support a maximum of four DIMM sockets.
4. The Intel® Xeon® 3400 Series processor on the Server Board of Intel® Server System SR1640TH is populated on the processor socket. It has an Integrated Memory Controller (IMC). The IMC provides two DDR3 channels and groups DIMMs on the board into an autonomous memory.

5. The DIMM identifiers on the silkscreen on the board provide information about the channel and the processor socket to which they belong. For example, DIMM_A1 is the first slot on channel A.

#### 2.4.3.4.3 Memory Upgrade Rules

Upgrading the system memory requires careful positioning of the DDR3 DIMMs based on the following factors:

- Existing DDR3 DIMM population
- DDR3 DIMM characteristics
- Optimization techniques used by the Intel® Xeon® 3400 processor to maximize memory bandwidth

In the Independent Channel mode, all DDR3 channels operate independently. Slot-to-slot DIMM matching is not required across channels (for example, A1 and B1 do not have to match each other in terms of size, organization, and timing). DIMMs within a channel do not have to match in terms of size and organization, but they operate in the minimal common frequency. Also, Independent Channel mode can be used to support single DIMM configuration in channel A and in the Single Channel mode.

You must observe the following general rules when selecting and configuring memory to obtain the best performance from the system.

1. DDR3 RDIMMs must always be populated using a fill-farthest method.
2. DDR3 UDIMMs must always be populated on DIMM A1/A2/B1/B2.
3. Intel® Xeon® 3400 Series Processors support either RDIMMs or UDIMMs.
4. RDIMM and UDIMM CANNOT be mixed.
5. The minimal memory set is {DIMMA1}.
6. DDR3 DIMMs on adjacent slots on the same channel do not need to be identical.

Intel® Server Systems SR1640TH that use the Intel® 3420 chipset support two slots per DDR3 channel, two DDR3 channels per processor socket.

#### 2.4.3.4.4 Memory Configuration Table

**Table 4. Memory Configuration Table**

| | Channel A | | Channel B | |
|---|---|---|---|---|
| | A1 | A2 | B1 | B2 |
| RDIMM | X | | | |
| | X | X | | |
| | X | | X | |
| | X | X | X | |
| | X | X | X | X |
| UDIMM | X | | | |
| | X | X | | |
| | X | | X | |
| | X | X | X | |
| | X | X | X | X |

This table defines half of the valid memory configurations. You can exchange Channel A DIMMs with the DIMMs on Channel B to get another half.

#### 2.4.3.4.5 UDIMM Configuration rules

**Table 5. UDIMM memory configuration rule**

| DIMM slots per channel | DIMMs populated per channel | Speed | Ranks per channel |
|---|---|---|---|
| 2 | 1 | 1066, 1333 | Single Rank, Dual Rank |
| 2 | 2 | 1066, 1333 | Single Rank, Dual Rank |

To get the maximum memory size on UDIMM, you get the detail information from below table.

**Table 6. UDIMM Maximum configuration**

| Max Memory Possible | 1Gb DRAM Technology | 2Gb DRAM Technology |
|---|---|---|
| Single Rank UDIMM | 4GB<br>(4x 1GB DIMMs) | 8GB<br>(4x 2GB DIMMs) |
| Dual Rank UDIMMs | 8GB<br>(4x 2GB DIMMs) | 16GB<br>(4x 4GB DIMMs) |

Server boards in Intel® Server System SR1640TH have the following limitations on UDIMM.

- Not support 800MHz ECC UDIMMs
- No support for LV DIMMs
- 256Mb technology, x4 DRAM on UDIMM and quad rank UDIMM are NOT supported
- x16 DRAM is not supported on combo routing
- All channels in a system will run at the fastest common frequency
- No mixing of registered and unbuffered DIMMs
- Non-ECC UDIMMs not supported
- Mixing ECC and non-ECC UDIMMs anywhere on the platform will prevent the system to boot/function correctly

#### 2.4.3.4.6 RDIMM Configuration rules

**Table 7. RDIMM memory configuration rule**

| DIMM slots per channel | DIMMs populated per channel | Speed | Ranks per channel |
|---|---|---|---|
| 2 | 1 | 1066, 1333 | Single Rank, Dual Rank |
| 2 | 1 | 1066 | Quad Rank |
| 2 | 2 | 1066, 1333 | Single Rank, Dual Rank |
| 2 | 2 | 800* | Quad Rank |

To get the maximum memory size on RDIMM, you get the detail information from the following table.

**Table 8. RDIMM Maximum configuration**

| Max Memory Possible | 1Gb DRAM Technology | 2Gb DRAM Technology |
|---|---|---|
| Single Rank RDIMM | 4GB<br>(4x 1GB DIMMs) | 8GB<br>(4x 2GB DIMMs) |
| Dual Rank RDIMMs | 8GB<br>(4x 2GB DIMMs) | 16GB<br>(4x 4GB DIMMs) |
| Quad Rank RDIMMs | 16GB<br>(4x 4GB DIMMs) | NA |

Also, the server boards in Intel® Server System SR1640TH have the following limitations on RDIMM;

- No support for LV DIMMs
- 256Mb/512Mb technology, x4 and x16 DRAMs on RDIMM are NOT supported
- All channels in a system will run at the fastest common frequency
- No mixing of registered and unbuffered DIMMs

**Note:** 1066MHz RDIMMs run at 800MHz.

### 2.4.4 Intel® 3420 PCH

The Intel® 3420 Chipset component is the Platform Controller Hub (PCH). The PCH is designed for use with Intel® processor in a UP server platform. The role of the PCH on the server board S3420TH is to manage the flow of information between its eleven interfaces:

- DMI interface to Processor
- PCI Express* Interface
- PCI Interface
- SATA Interface
- USB Host Interface
- SMBus Host Interface
- SPI Interface
- LPC interface to IBMC
- JTAG interface
- LAN interface
- ACPI interface

### 2.4.5 I/O Sub-system

Intel® 3420 Chipset PCH provides extensive I/O support.

#### 2.4.5.1 PCI Express Interface

There is no PCI-E extensive slot available on the server board S3420TH in Intel® Server System SR1640TH.

#### 2.4.5.2 Serial ATA Support

The Intel® 3420 Chipset has two integrated SATA host controllers that support independent DMA operation on up to six ports and supports data transfer rates of up to 3.0 GB/s (300 MB/s). The SATA controller contains two modes of operation – a legacy mode using I/O space and an AHCI mode using memory space.

Software that uses legacy mode does not have AHCI capabilities. The Intel® 3420 Chipset supports the Serial ATA Specification, Revision 1.0a. The Intel® 3420 Chipset also supports several optional sections of the Serial ATA II: Extensions to Serial ATA 1.0 Specification, Revision 1.0 (AHCI support is required for some elements).

There are two SATA ports implemented for each computing node on the server board S3420TH. Each of them is dedicated to one 3.5 inch HDD bay, using customized SATA cable.

#### 2.4.5.3 USB 2.0 Support

On the Intel® 3420 Chipset, the USB controller functionality is provided by the dual EHCI controllers with an interface for up to ten USB 2.0 ports. All ports are high-speed, full-speed, and low-speed capable.

- Two external connectors are located on the back edge of the server board.
- Two internal headers are provided on the board for each node, each supporting two front panel USB 2.0 ports.

##### 2.4.5.3.1 Native USB Support

During the power-on self test (POST), the BIOS initializes and configures the USB subsystem. The BIOS is capable of initializing and using the following types of USB devices.

- USB Specification-compliant keyboards
- USB Specification-compliant mouse
- USB Specification-compliant storage devices that utilize bulk-only transport mechanism

USB devices are scanned to determine if they are required for booting.

The BIOS supports USB 2.0 mode of operation, and as such supports USB 1.1 and USB 2.0 compliant devices and host controllers.

During the pre-boot phase, the BIOS automatically supports the hot addition and hot removal of USB devices and a short beep is emitted to indicate such an action. For example, if a USB device is hot plugged, the BIOS detects the device insertion, initializes the device, and makes it available to the user. During POST, when the USB controller is initialized, it emits a short beep for each USB device plugged into the system as they were all just “hot added”.

Only on-board USB controllers are initialized by BIOS. This does not prevent the operating system from supporting any available USB controllers including add-in cards.

##### 2.4.5.3.2 Legacy USB Support

The BIOS supports PS/2 emulation of USB keyboards and mouse. During POST, the BIOS initializes and configures the root hub ports and searches for a keyboard and/or a mouse on the USB hub and then enables the devices that are recognized.

### 2.4.6 Integrated Baseboard Management Controller

The server boards S3420TH in Intel® Server System SR1640TH have the integrated baseboard management controller.

The ServerEngines* LLC Pilot II Integrated BMC is provided by an embedded ARM9 controller and associated peripheral functionality that is required for IPMI-based server management. Firmware usage of these hardware features is platform-dependant.

The following is a summary of the Integrated BMC management hardware features used by the ServerEngines* LLC Pilot II Integrated BMC:

- 250 MHz 32-bit ARM9 Processor
- Memory Management Unit (MMU)
- Two 10/100 Ethernet Controllers with NC-SI support
- 16-bit DDR2 667 MHz interface
- Dedicated RTC
- 12 10-bit ADCs
- Eight Fan Tachometers
- Four PWMs
- Battery-backed Chassis Intrusion I/O Register
- JTAG Master
- Six $I^2C$ interfaces
- General-purpose I/O Ports (16 direct, 64 serial)

Additionally, the ServerEngines* Pilot II part integrates a super I/O module with the following features:

- KCS/BT Interface
- Two 16C550 Serial Ports
- Serial IRQ Support
- 12 GPIO Ports (shared with BMC)
- LPC to SPI Bridge
- SMI and PME Support

The Pilot II contains an integrated KVMS subsystem and graphics controller with the following features:

- USB 2.0 for keyboard, mouse, and storage devices
- USB 1.1 interface for legacy PS/2 to USB bridging
- Hardware Video Compression for text and graphics
- Hardware encryption
- 2D Graphics Acceleration
- DDR2 graphics memory interface
- Up to 1600x1200 pixel resolution
- PCI Express* x1 support

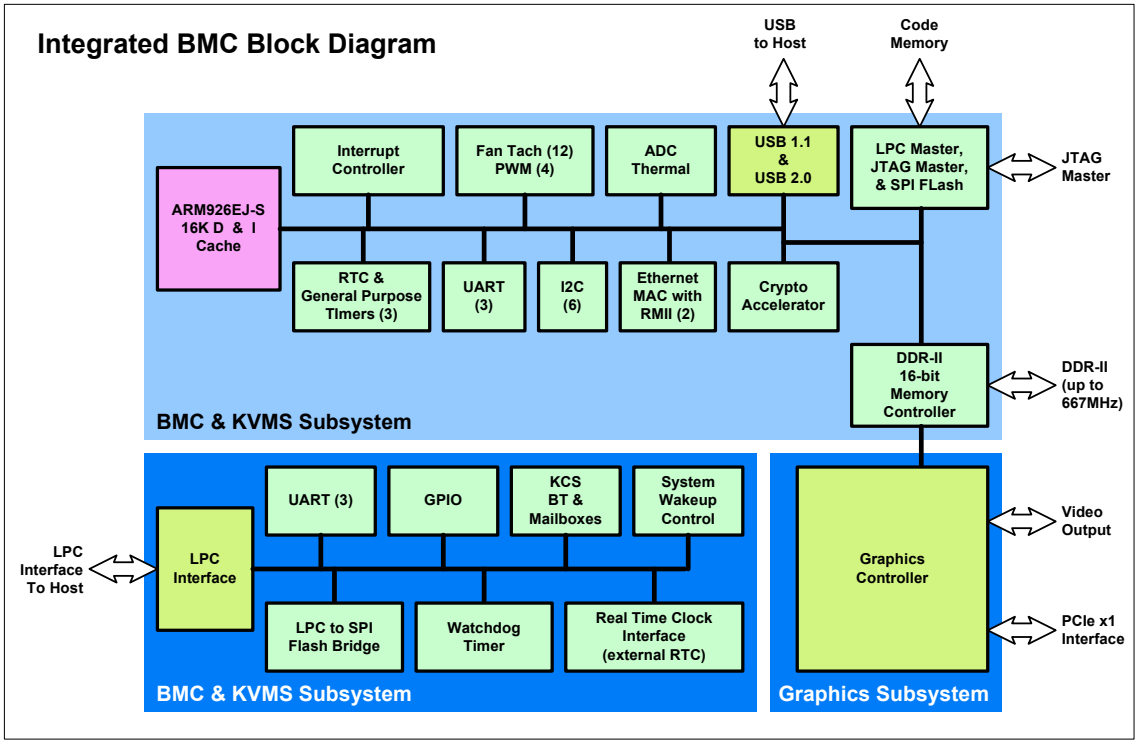



**Figure 7. Integrated BMC Hardware**

### 2.4.6.1 Integrated BMC Embedded LAN Channel

The Integrated BMC hardware includes two dedicated 10/100 network interfaces.

**Interface 1:** This interface is available from either of the available NIC ports in system that can be shared with the host. Only one NIC may be enabled for management traffic at any time. To change the NIC enabled for management traffic, please use the "Write LAN Channel Port" OEM IPMI command. The default active interface is port 1 (NIC1).

**Interface 2:** This interface is available from the optional RMM3 Lite-V module which is a dedicated management NIC that is not shared with the host.

For these channels, support can be enabled for IPMI-over-LAN and DHCP.

For security reasons, embedded LAN channels have the following default settings:

- IP Address: Static
- All users disabled

### 2.4.6.2 Optional RMM3 Lite-V module

RMM3 Lite-V module serves two purposes:

Give the customer the option to add a dedicated management 100 Mbit LAN interface to the product.

Provide additional flash space, enabling the Advanced Management functions to support WS-MAN and CIMON.

**Table 9. Optional RMM3 Advanced Management Board Features**

| Feature | Description |
|---|---|
| KVM Redirection | Remote console access via keyboard, video, and mouse redirection over LAN. |
| USB Media Redirection | Remote USB media access over LAN. |
| WS-MAN | Full SMASH profiles for WS-MAN based consoles. |

#### 2.4.6.3 Serial Ports

The server board S3420TH does not support serial port.

#### 2.4.6.4 Floppy Disk Controller

The server board does not support a floppy disk controller interface. However, the system BIOS recognizes USB floppy devices.

#### 2.4.6.5 Keyboard and Mouse Support

The server board does not support PS/2 interface keyboards and mouse. However, the system BIOS recognizes USB specification-compliant keyboard and mouse.

#### 2.4.6.6 Wake-up Control

The super I/O contains functionality that allows various events to power on and power off the system.

### 2.4.7 Video Support

The server board includes video controllers for each node in an on-board Server Engines* Integrated Baseboard Management Controller along with 64 MB of video DDR2 memory. 8MB is usable/accessible for iBMC video/graphic display functions. The graphics controller internally has access to larger memory for the internal operation. The SVGA subsystem supports a variety of modes, up to 1600 x 1200 resolution in 8 / 16 / 32 bpp modes under 2D. It also supports both CRT and LCD monitors up to a 100 Hz vertical refresh rate.

The video is accessed using a standard 15-pin VGA connector found on the back edge of the server board. The on-board video controller can be disabled using the BIOS Setup utility or when an add-in video card is detected. The system BIOS provides the option for dual-video operation when an add-in video card is configured in the system.

The integrated video controller supports all standard IBM VGA modes. The following table shows the 2D modes supported for both CRT and LCD.

**Table 10. Video Modes**

| 2D Mode | Refresh Rate (Hz) | 2D Video Mode Support | | |
|---|---|---|---|---|
| | | 8 bpp | 16 bpp | 32 bpp |
| 640x480 | 60, 72, 75, 85, 90, 100, 120, 160, 200 | Supported | Supported | Supported |
| 800x600 | 60, 70, 72, 75, 85, 90, 100, 120,160 | Supported | Supported | Supported |
| 1024x768 | 60, 70, 72, 75,85,90,100 | Supported | Supported | Supported |
| 1152x864 | 43,47,60,70,75,80,85 | Supported | Supported | Supported |
| 1280x1024 | 60,70,74,75 | Supported | Supported | Supported |
| 1600x1200 | 52 | Supported | Supported | Supported |

### 2.4.8 Network Interface Controller (NIC)

The server boards S3420TH in Intel® Server System SR1640TH support three network interfaces, two is provided from the onboard Intel® 82574L GbE PCI Express* network controllers; the third one is the onboard 10/100Mbps KSZ8041NL Network controller, only enabled by RMM3 Lite-V module for management.

#### 2.4.8.1 GigE Controller 82574L

The 82574 family (82574L and 82574IT) are single, compact, low-power components that offer a fully-integrated Gigabit Ethernet Media Access Control (MAC) and Physical Layer (PHY) port. The 82574 uses the PCI Express* architecture and provides a single-port implementation in a relatively small area so it can be used for server and client configurations as a LAN on Motherboard (LOM) design.
External interfaces provided on the 82574:

PCIe Rev. 2.0 (2.5 GHz) x1
MDI (Copper) standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASETX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab)
NC-SI or SMBus connection to a Manageability Controller (MC)
EEE 1149.1 JTAG (note that BSDL testing is NOT supported)

#### 2.4.8.2 Dedicated 10/100Mbps management port

The KSZ8041NL network PHY is connected to iBMC through RMMII interface as dedicated management port. This port can only work with Intel® RMM3 Lite-V module installed.

#### 2.4.8.3 MAC Address Definition

Each computing node in Intel® Server System SR1640HT has the following four MAC addresses assigned to it at the Intel factory:

- NIC 1 MAC address
- NIC 2 MAC address – Assigned the NIC 1 MAC address +1
- Integrated BMC LAN Channel MAC address – Assigned the NIC 1 MAC address +2
- Intel® Remote Management Module 3 (Intel® RMM3 Lite-V) MAC address – Assigned the NIC 1 MAC address +3

### 2.4.9 Intel® Virtualization Technology for Directed I/O (Intel® VT-d)

The Intel® 3420 PCH provides hardware support for implementation of Intel® Virtualization Technology with Directed I/O (Intel® VT-d). Intel VT-d Technology consists of technology components that support the virtualization of platforms based on Intel® Architecture Processor. Intel VT-d Technology enables multiple operating systems and applications to run in dependent partitions. A partition behaves like a virtual machine (VM) and provides isolation and protection across partitions. Each partition is allocated its own subset of host physical memory.

The Intel® Virtualization Technology is designed to support multiple software environments sharing the same hardware resources. The Intel® Virtualization Technology can be enabled or disabled in the BIOS setup. The default behavior is disabled.

**Note:** If the setup options are changed to enable or disable the Virtualization Technology setting in the processor, the user must perform an AC power cycle for the changes to take effect.

## 2.5 Platform Management

The platform management subsystem is based on the Integrated BMC features of the ServerEngines* Pilot II. The onboard platform management subsystem consists of communication buses, sensors, system BIOS, and server management firmware. The following diagram provides an overview of the Server Management Bus (SMBUS) architecture used on this server board.

### 2.5.1 Feature Support

#### 2.5.1.1 IPMI 2.0 Features

- Integrated Baseboard Management Controller (Integrated BMC).
- IPMI Watchdog timer.
- Messaging support, including command bridging and user/session support.
- Chassis device functionality, including power/reset control and BIOS boot flags support.
- Event receiver device: The Integrated BMC receives and processes events from other platform subsystems.
- Field replaceable unit (FRU) inventory device functionality: The Integrated BMC supports access to system FRU devices using IPMI FRU commands.
- System event log (SEL) device functionality: The Integrated BMC supports and provides access to a SEL.
- Sensor device record (SDR) repository device functionality: The Integrated BMC supports storage and access of system SDRs.
- Sensor device and sensor scanning/monitoring: The Integrated BMC provides IPMI management of sensors. It polls sensors to monitor and report system health.
- IPMI interfaces.
    - Host interfaces include system management software (SMS) with receive message queue support and server management mode (SMM).
    - Terminal mode serial interface
    - IPMB interface
    - LAN interface that supports the IPMI-over-LAN protocol (RMCP, RMCP+)
- Serial-over-LAN (SOL)
- ACPI state synchronization: The Integrated BMC tracks ACPI state changes provided by the BIOS.
- Integrated Baseboard Management Controller (Integrated BMC) self test: The Integrated BMC performs initialization and run-time self tests, and makes results available to external entities.

For more information, refer to the IPMI 2.0 Specification.

#### 2.5.1.2 Non-IPMI Features

The Integrated BMC supports the following non-IPMI features. This list does not preclude support for future enhancements or additions.

- In-circuit Integrated BMC firmware update.
- Fault resilient booting (FRB): FRB2 is supported by the watchdog timer functionality
- Chassis intrusion detection and chassis intrusion cable presence detection.
- Basic fan control using TControl version 2 SDRs.
- Acoustic management: Support for multiple fan profiles.
- Signal testing support: The Integrated Baseboard Management Controller (Integrated BMC) provides test commands for setting and getting platform signal states.

- The Integrated Baseboard Management Controller (Integrated BMC) generates diagnostic beep codes for fault conditions.
- System GUID storage and retrieval.
- Front panel management: The Integrated Baseboard Management Controller (Integrated BMC) controls the system status LED and chassis ID LED. It supports secure lockout of certain front panel functionality and monitors button presses. The chassis ID LED is turned on using a front panel button or a command.
- Power state retention
- Power fault analysis
- Intel® Light-Guided Diagnostics
- Power unit management: Support for power unit sensor. The Integrated Baseboard Management Controller (Integrated BMC) handles power-good dropout conditions.
- DIMM temperature monitoring: New sensors and improved acoustic management using closed-loop fan control algorithm taking into account DIMM temperature readings.
- Address Resolution Protocol (ARP): The Integrated BMC sends and responds to ARPs (supported on embedded NICs)
- Dynamic Host Configuration Protocol (DHCP): The Integrated BMC performs DHCP (supported on embedded NICs).
- Platform environment control interface (PECI) thermal management support.
- E-mail alerting
- Embedded web server
- Integrated KVM
- Integrated Remote Media Redirection
- Lightweight Directory Authentication Protocol (LDAP) support

### 2.5.2 Optional Advanced Management Feature Support

This section explains the advanced management features supported by the Integrated Baseboard Management Controller (Integrated BMC) firmware.

#### 2.5.2.1 Enabling Advanced Management Features

The Integrated BMC enables the advanced management features only when it detects the presence of the Intel® Remote Management Module 3 Lite-V (Intel® RMM3 Lite-V) module. Without the Intel® RMM3 Lite-V Module, the advanced features are dormant.

The Intel® RMM3 Lite-V module provides the Integrated BMC through dedicated network interface. The dedicated interface consumes its own LAN channel. Additionally, the Intel® RMM3 Lite-V provides additional flash storage for advanced features like Web Services for Management (WS-MAN).

#### 2.5.2.2 Keyboard, Video, Mouse (KVM) Redirection

The Integrated BMC firmware supports keyboard, video, and mouse redirection over LAN. This feature is available remotely from the embedded web server as a Java applet. This feature is enabled only when the Intel® RMM3 Lite-V is present. The client system must have a Java Runtime Environment (JRE) version 5.0 or later to run the KVM or media redirection applets.

##### 2.5.2.2.1 Keyboard and Mouse

The keyboard and mouse are emulated by the Integrated BMC as USB human interface devices.

#### 2.5.2.2.2 Video

Video output from the KVM subsystem is equivalent to the video output on the local console. Video redirection is available after video is initialized by the system BIOS. The KVM video resolution and refresh rates will always match the values set in the operating system.

#### 2.5.2.2.3 Availability

The default inactivity timeout is 30 minutes; however, this can be changed through the embedded web server. Remote KVM activation does not disable the local system keyboard, video, or mouse. Unless the feature is disabled locally, remote KVM is not deactivated by local system input.

KVM sessions persist across system reset but not across an AC power loss.

### 2.5.2.3 Media Redirection

The embedded web server provides a Java applet to enable remote media redirection. This may be used in conjunction with the remote KVM feature or as a standalone applet.

The media redirection feature is intended to allow system administrators or users to mount a remote IDE or USB CD-ROM, floppy drive, or a USB flash disk as a remote device to the server. Once mounted, the remote device appears just like a local device to the server, allowing system administrators or users to install software (including operating systems), copy files, update the BIOS, and so forth, or boot the server from this device.

The following capabilities are supported:

- The operation of remotely mounted devices is independent of the local devices on the server. Both remote and local devices are usable in parallel
- Either IDE (CD-ROM, floppy) or USB devices can be mounted as a remote device to the server.
- It is possible to boot all supported operating systems from the remotely mounted device and to boot from disk IMAGE (*.IMG) and CD-ROM or DVD-ROM ISO files. Refer to the Tested/supported Operating System List for more information.
- It is possible to mount at least two devices concurrently.
- The mounted device is visible to (and useable by) the managed system's operating system and BIOS in both pre-boot and post-boot states.
- The mounted device shows up in the BIOS boot order and it is possible to change the BIOS boot order to boot from this remote device.
- It is possible to install an operating system on a bare metal server (no operating system present) using the remotely mounted device. This may also require the use of KVM-r to configure the operating system during install.

If either a virtual IDE or virtual floppy device is remotely attached during system boot, both virtual IDE and virtual floppy are presented as bootable devices. It is not possible to present only a single mounted device type to the system BIOS.

The default inactivity timeout is 30 minutes, but may be changed through the embedded web server.

Media redirection sessions persist across system reset but not across an AC power loss.

### 2.5.2.4 Web Services for Management (WS-MAN)

The Integrated BMC firmware supports the Web Services for Management (WS-MAN) specification, version 1.0.

#### 2.5.2.5 Local Directory Authentication Protocol (LDAP)

The Integrated BMC firmware supports the Local Directory Authentication Protocol (LDAP) protocol for user authentication.

**Note**: IPMI users/passwords and sessions are not supported over LDAP.

#### 2.5.2.6 Embedded Webserver

The Integrated BMC provides an embedded web server for out-of-band management. User authentication is handled by IPMI user names and passwords. Base functionality for the embedded web server includes:

- Power Control – Limited control based on IPMI user privilege.
- Sensor Reading – Limited access based on IPMI user privilege.
- SEL Reading – Limited access based on IPMI user privilege.
- KVM/Media Redirection – Limited access based on IPMI user privilege. Only available when the Intel® RMM3 Lite-V module is present.
- IPMI User Management – Limited access based on IPMI user privilege.

The web server is available on all enabled LAN channels.

See Appendix B for Integrated BMC core sensors.

### 2.5.3 Management Engine (ME)

Intel Management Engine is tied to essential platform functionality. This Management Engine firmware includes the following applications:

- Platform Clocks – Tune PCH clock silicon to the parameters of a specific board, configure clocks at run time, power management clocks.
- Thermal Report – ME FW reports thermal and power information available only on PECI to host accessible registers / Embedded Controller via SMBus.

### 2.5.4 SMBIOS

#### 2.5.4.1 Data Storage

BIOS retrieve the SMBIOS data from flash during POST, and it builds the SMBIOS type 1, 2, 3 into SMBIOS table and then transfers the control to operating system. Operating system and system management software can use the SMBIOS table for system management purpose.

### 2.5.5 Event log and Viewer

#### 2.5.5.1 Event Log Viewer in Setup

On Intel® Server System SR1640TH, there is a dedicated utility to view the event log. There is one page in BIOS setup for event log viewer. It is located in Error Manager Page.

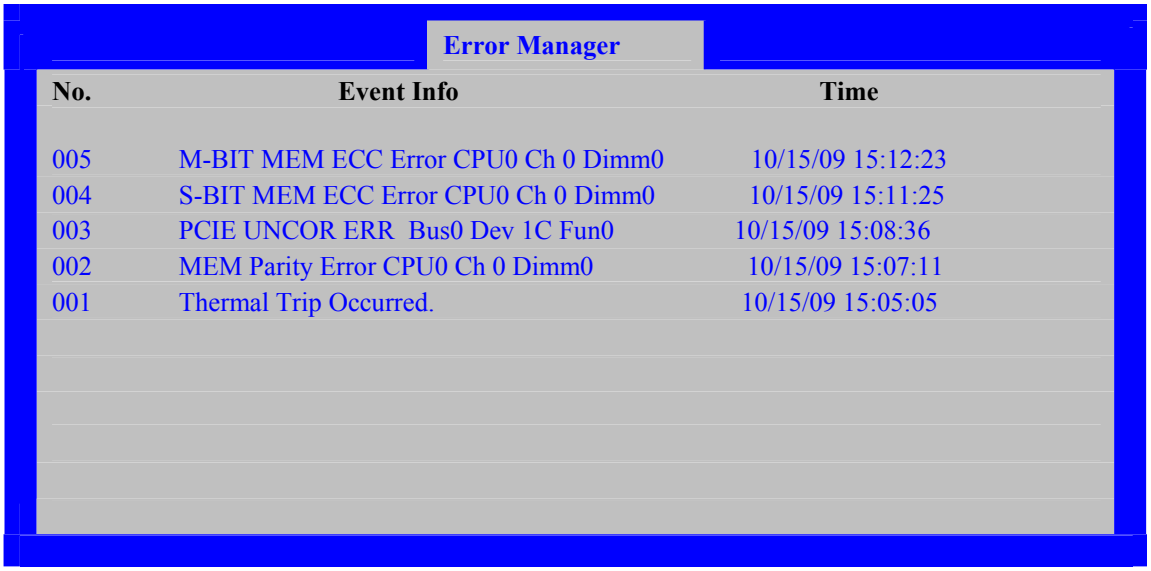



**Figure 8. Example of Event Log Viewer**

The Event log viewer is at another page than the BIOS error manager. The event log viewer can display many log in one page. Each event log is displayed in one line. The latest one is on the top. When there are more event logs on one page, Page Up and Page Down keys can be used. There is a scroll bar to allow end-users to view the logs from top to bottom.

## 2.6 BIOS User Interface

### 2.6.1 Logo / Diagnostic Screen

The logo / Diagnostic Screen displays in one of two forms:

- If Quiet Boot is enabled in the BIOS setup, a logo splash screen displays. By default, Quiet Boot is enabled in the BIOS setup. If the logo displays during POST, press <Esc> to hide the logo and display the diagnostic screen.
- If a logo is not present in the flash ROM or if Quiet Boot is disabled in the system configuration, the summary and diagnostic screen displays.

The diagnostic screen displays the following information:

- BIOS ID
- Platform name
- Total memory detected (Total size of all installed DDR3 DIMMs)
- Processor information (Intel branded string, speed, and number of physical processor identified)
- Keyboards detected (if plugged in)
- Mouse devices detected (if plugged in)

### 2.6.2 BIOS Boot Popup Menu

The BIOS Boot Specification (BBS) provides for a Boot Popup Menu invoked by pressing the <F6> key during POST. The BBS popup menu displays all available boot devices. The list order in the popup menu is not the same as the boot order in the BIOS setup; it simply lists the bootable devices from which the system can be booted.

When a User Password or Administrator Password is active in Setup, the password is to access the Boot Popup Menu.

### 2.6.3 BIOS Setup utility

The BIOS setup utility is a text-based utility that allows the user to configure the system and view current settings and environment information for the platform devices. The Setup utility controls the platform's built-in devices, boot manager, and error manager.

The BIOS setup interface consists of a number of pages or screens. Each page contains information or links to other pages. The advanced tab in Setup displays a list of general categories as links. These links lead to pages containing a specific category's configuration.

The following sections describe the look and behavior for platform setup.

### 2.6.4 Operation

The BIOS Setup has the following features:

- Localization - The BIOS Setup uses the Unicode standard and is capable of displaying setup forms in all languages currently included in the Unicode standard. The Intel® server board BIOS is only available in English.
- Console Redirection - The BIOS Setup is functional through console redirection over various terminal emulation standards. This may limit some functionality for compatibility (for example, color usage or some keys or key sequences or support of pointing devices).

#### 2.6.4.1 Setup Page Layout

The setup page layout is sectioned into functional areas. Each occupies a specific area of the screen and has dedicated functionality. The following table lists and describes each functional area.

**Table 11. BIOS Setup Page Layout**

| Functional Area | Description |
|---|---|
| Title Bar | The title bar is located at the top of the screen and displays the title of the form (page) the user is currently viewing. It may also display navigational information. |
| Setup Item List | The Setup Item List is a set of controllable and informational items. Each item in the list occupies the left column of the screen.<br>A Setup Item may also open a new window with more options for that functionality on the board. |
| Item Specific Help Area | The Item Specific Help area is located on the right side of the screen and contains help text for the highlighted Setup Item. Help information may include the meaning and usage of the item, allowable values, effects of the options, and so forth. |
| Keyboard Command Bar | The Keyboard Command Bar is located at the bottom right of the screen and continuously displays help for keyboard special keys and navigation keys. |

#### 2.6.4.2 Entering BIOS Setup

To enter the BIOS Setup, press the F2 function key during boot time when the OEM or Intel logo displays. The following message displays on the diagnostics screen and under the Quiet Boot logo screen:

```
Press <F2> to enter setup
```

When the Setup is entered, the Main screen displays. However, serious errors cause the system to display the Error Manager screen instead of the Main screen.

#### 2.6.4.3 Keyboard Commands

The bottom right portion of the Setup screen provides a list of commands used to navigate through the Setup utility. These commands display at all times.

Each Setup menu page contains a number of features. Each feature is associated with a value field except those used for informative purposes. Each value field contains configurable parameters. Depending on the security option chosen and, in effect, by the password, a menu feature's value may or may not be changed. If a value cannot be changed, its field is made inaccessible and appears grayed out.

**Table 12. BIOS Setup: Keyboard Command Bar**

| Key | Option | Description |
|---|---|---|
| <Enter> | Execute Command | The <Enter> key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected option has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the <Enter> key selects the currently highlighted item, undoes the pick list, and returns the focus to the parent menu. |
| <Esc> | Exit | The <Esc> key provides a mechanism for backing out of any field. When the <Esc> key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered.<br>When the <Esc> key is pressed in any sub-menu, the parent menu is re-entered. When the <Esc> key is pressed in any major menu, the exit confirmation window is displayed and the user is asked whether changes can be discarded. If "No" is selected and the <Enter> key is pressed, or if the <Esc> key is pressed, the user is returned to where they were before <Esc> was pressed, without affecting any existing settings. If "Yes" is selected and the <Enter> key is pressed, the setup is exited and the BIOS returns to the main System Options Menu screen. |
| | Select Item | The up arrow is used to select the previous value in a pick list, or the previous option in a menu item's option list. The selected item must then be activated by pressing the <Enter> key. |
| | Select Item | The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the <Enter> key. |
| | Select Menu | The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed. |
| <Tab> | Select Field | The <Tab> key is used to move between fields. For example, <Tab> can be used to move from hours to minutes in the time item in the main menu. |
| - | Change Value | The minus key on the keypad is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list. |
| + | Change Value | The plus key on the keypad is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list. On 106-key Japanese keyboards, the plus key has a different scan code than the plus key on the other keyboards, but will have the same effect. |
| <F9> | Setup Defaults | Pressing <F9> causes the following to display:<br>Load Optimized Defaults?<br>Yes No<br>If "Yes" is highlighted and <Enter> is pressed, all Setup fields are set to their default values. If "No" is highlighted and <Enter> is pressed, or if the <Esc> key is pressed, the user is returned to where they were before <F9> was pressed without affecting any existing field values. |
| <F10> | Save and Exit | Pressing <F10> causes the following message to display:<br>Save configuration and reset?<br>Yes No<br>If "Yes" is highlighted and <Enter> is pressed, all changes are saved and the Setup is exited. If "No" is highlighted and <Enter> is pressed, or the <Esc> key is pressed, the user is returned to where they were before <F10> was pressed without affecting any existing values. |

#### 2.6.4.4 Menu Selection Bar

The Menu Selection Bar is located at the top of the BIOS Setup Utility screen. It displays the major menu selections available to the user. By using the left and right arrow keys, the user

can select the menus listed here. Some menus are hidden and become available by scrolling off the left or right of the current selections.

### 2.6.5 Server Platform Setup Utility Screens

The following sections describe the screens available for the configuration of a server platform. In these sections, tables are used to describe the contents of each screen. These tables follow the following guidelines:

- The Setup Item, Options, and Help Text columns in the tables document the text and values displayed on the BIOS Setup screens.
- In the Options column, the default values display in bold. These values are not displayed in bold on the BIOS Setup screen; the bold text in this document serves as a reference point.
- The Comments column provides additional information where it may be helpful. This information does not display on the BIOS Setup screens.
- Information enclosed in angular brackets (< >) in the screen shots identifies text that can vary, depending on the option(s) installed. For example, <Current Date> is replaced by the actual current date.
- Information enclosed in square brackets ([ ]) in the tables identifies areas where the user must type in text instead of selecting from a provided option.
- Whenever information is changed (except Date and Time), the system requires a save and reboot to take place. Pressing <ESC> discards the changes and boots the system according to the boot order set from the last boot.

#### 2.6.5.1 Main Screen

The Main screen is the first screen displayed when the BIOS Setup is entered, unless an error occurred. If an error occurred, the Error Manager screen displays instead.

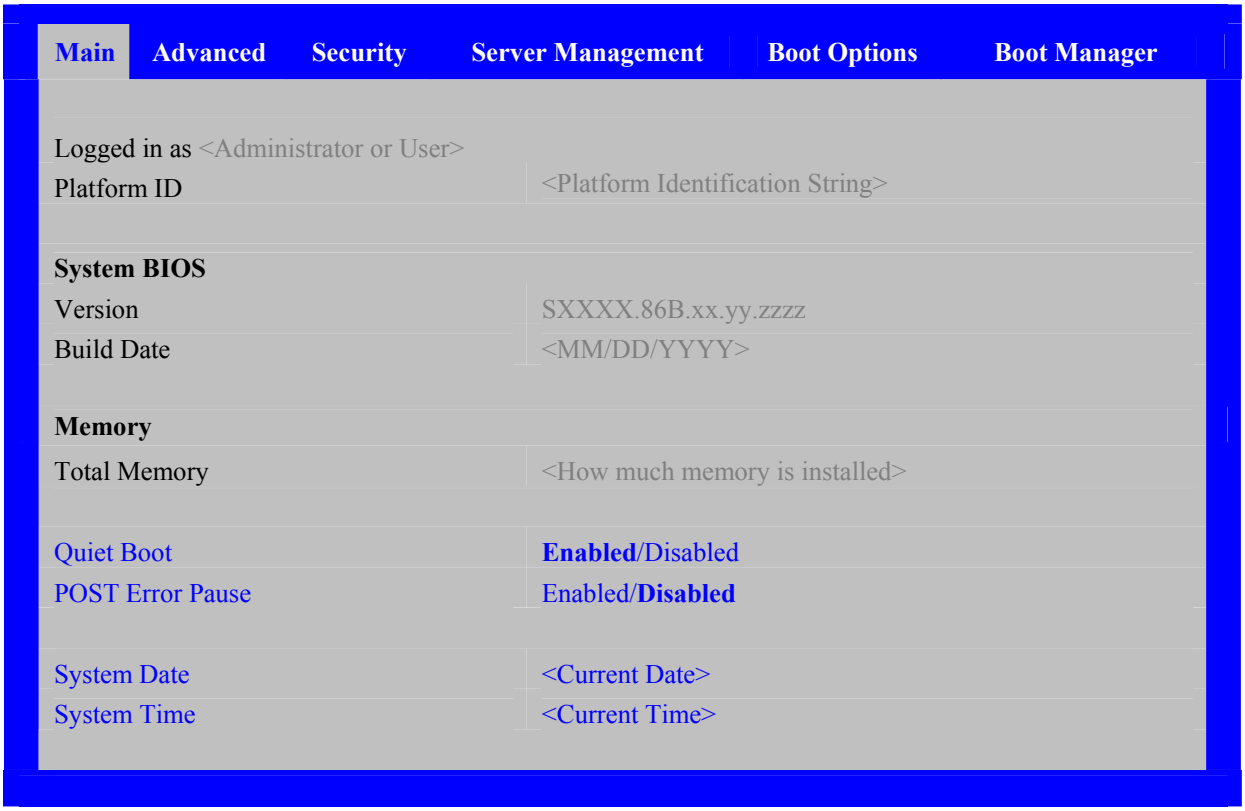



**Figure 9. Setup Utility – Main Screen Display**

**Table 13. Setup Utility – Main Screen Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Logged in as | | | **Information only.** Displays password level that setup is running in: Administrator or User. With no passwords set, Administrator is the default mode. |
| Platform ID | | | **Information only.** Displays the Platform ID as S3420TH |
| System BIOS | | | |
| Version | | | **Information only.** Displays the current BIOS version.<br>xx = major version<br>yy = minor version<br>zzzz = build number |
| Build Date | | | **Information only.** Displays the current BIOS build date. |
| Memory | | | |
| Size | | | **Information only.** Displays the total physical memory installed in the system, in MB or GB. The term physical memory indicates the total memory discovered in the form of installed DDR3 DIMMs. |
| Quiet Boot | Enabled<br>Disabled | [Enabled] – Display the logo screen during POST.<br><br>[Disabled] – Display the diagnostic screen during POST. | |
| POST Error Pause | Enabled<br>Disabled | [Enabled] – Go to the Error Manager for critical POST errors.<br>[Disabled] – Attempt to boot and do not go to the Error Manager for critical POST errors. | If enabled, the POST Error Pause option takes the system to the error manager to review the errors when major errors occur. Minor and fatal error displays are not affected by this setting. |
| System Date | [Day of week MM/DD/YYYY] | System Date has configurable fields for Month, Day, and Year.<br>Use [Enter] or [Tab] key to select the next field.<br>Use [+] or [-] key to modify the selected field. | |
| System Time | [HH:MM:SS] | System Time has configurable fields for Hours, Minutes, and Seconds.<br>Hours are in 24-hour format.<br>Use [Enter] or [Tab] key to select the next field.<br>Use [+] or [-] key to modify the selected field. | |

### 2.6.5.2 Advanced Screen

The **Advanced** screen provides an access point to configure several options. On this screen, the user selects the option they want to configure. Configurations are performed on the selected screen, and not directly on the Advanced screen.

To access this screen from the Main screen, press the right arrow until the **Advanced** screen is chosen.

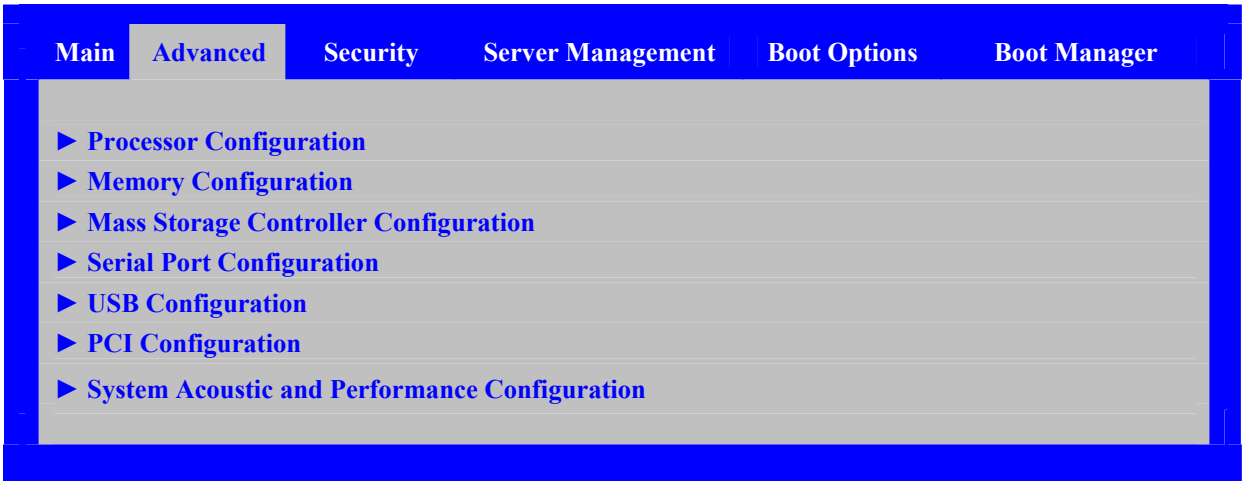



**Figure 10. Setup Utility – Advanced Screen Display**

**Table 14. Setup Utility – Advanced Screen Display Fields**

| Setup Item | Help Text |
|---|---|
| Processor Configuration | View/Configure processor information and settings. |
| Memory Configuration | View/Configure memory information and settings. |
| Mass Storage Controller Configuration | View/Configure mass storage controller information and settings. |
| Serial Port Configuration | View/Configure serial port information and settings. |
| USB Configuration | View/Configure USB information and settings. |
| PCI Configuration | View/Configure PCI information and settings. |
| System Acoustic and Performance Configuration | View/Configure system acoustic and performance information and settings. |

#### 2.6.5.2.1 Processor Screen

The Processor screen allows the user to view the processor core frequency, system bus frequency, and to enable or disable several processor options. This screen also allows the user to view information about a specific processor.

To access this screen from the Main screen, select **Advanced** > **Processor**.

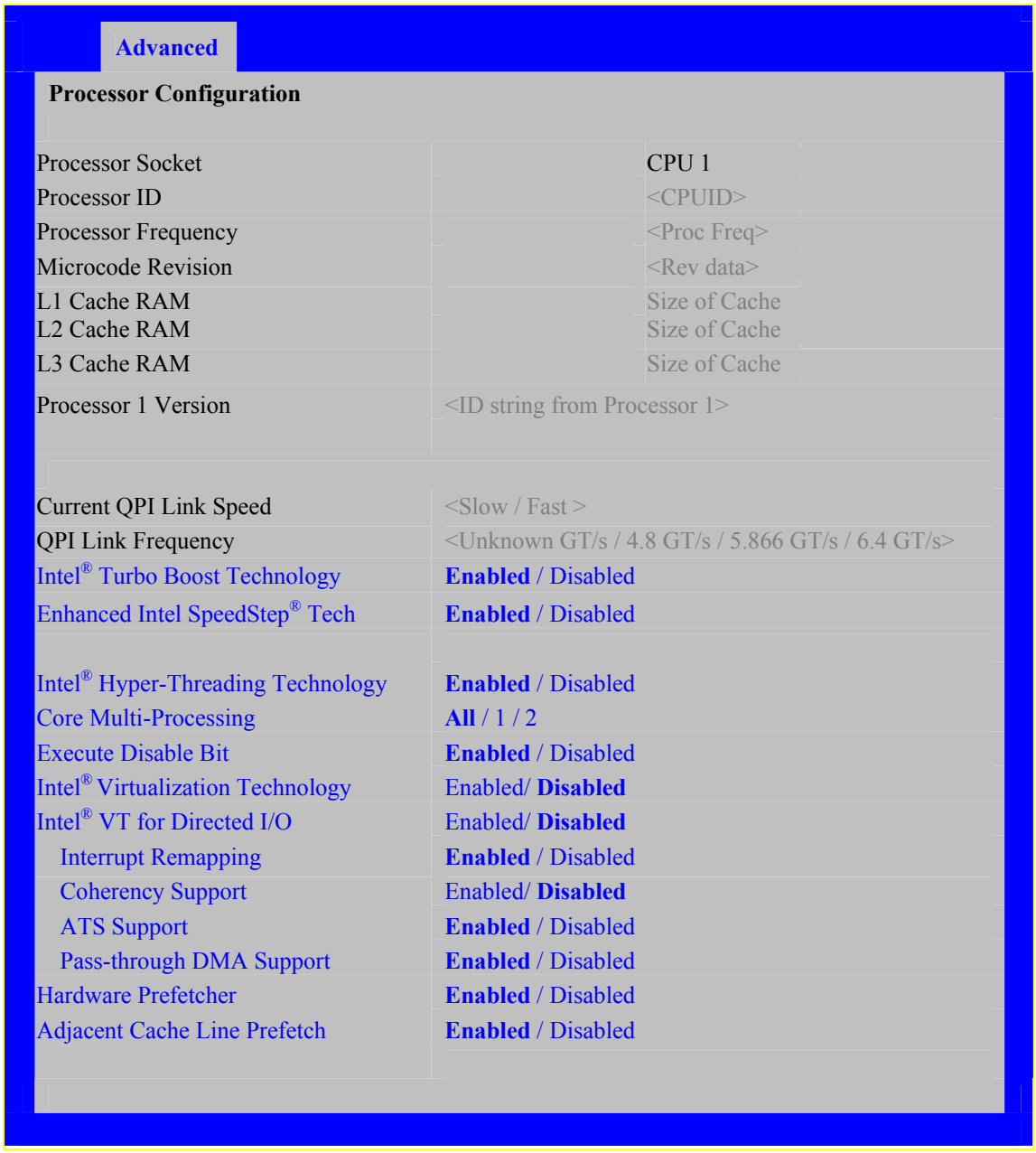



**Figure 11. Setup Utility – Processor Configuration Screen Display**

**Table 15. Setup Utility – Processor Configuration Screen Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Processor ID | | | **Information only.** Processor CPUID. |
| Processor Frequency | | | **Information only.** Current frequency of the processor. |
| Core Frequency | | | **Information only.** Frequency at which the processor are currently running. |
| Microcode Revision | | | **Information only.** Revision of the loaded microcode. |
| L1 Cache RAM | | | **Information only.** Size of the Processor L1 Cache. |
| L2 Cache RAM | | | **Information only.** Size of the Processor L2 Cache |
| L3 Cache RAM | | | **Information only.** Size of the Processor L3 Cache. |

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Processor Version | | | **Information only.** ID string from the Processor. |
| Current QPI Link Speed | | | **Information only.** Current speed that the QPI Link is using. |
| QPI Link Frequency | | | **Information only.** Current frequency that the QPI Link is using. |
| Intel® Turbo Boost Technology | Enabled<br>Disabled | Intel® Turbo Boost Technology allows the processor to automatically increase its frequency if it is running below power, temperature, and current specifications. | This option is only visible if all processor in the system support Intel® Turbo Boost Technology. |
| Enhanced Intel SpeedStep® Technology | Enabled<br>Disabled | Enhanced Intel SpeedStep® Technology allows the system to dynamically adjust processor voltage and core frequency, which can result in decreased average power consumption and decreased average heat production.<br>Contact your OS vendor regarding OS support of this feature. | |
| Intel® Hyper-Threading Technology | Enabled<br>Disabled | Intel® HT Technology allows multithreaded software applications to execute threads in parallel within the processor.<br>Contact your OS vendor regarding OS support of this feature. | |
| Core Multi-Processing | All<br>1<br>2 | Enable 1, 2 or All cores of installed processor packages. | |
| Execute Disable Bit | Enabled<br>Disabled | Execute Disable Bit can help prevent certain classes of malicious buffer overflow attacks.<br>Contact your OS vendor regarding OS support of this feature. | |
| Intel® Virtualization Technology | Enabled<br>Disabled | Intel® Virtualization Technology allows a platform to run multiple operating systems and applications in independent partitions.<br>**Note**: A change to this option requires the system to be powered off and then back on before the setting takes effect. | |
| Intel® Virtualization Technology for Directed I/O | Enabled<br>Disabled | Enable/Disable Intel® Virtualization Technology for Directed I/O.<br>Report the I/O device assignment to VMM through DMAR ACPI Tables | |
| Interrupt Remapping | Enabled<br>Disabled | Enable/Disable Intel® VT-d Interrupt Remapping support. | Only visible when Intel® Virtualization Technology for Directed I/O is enabled. |
| Coherency Support | Enabled<br>Disabled | Enable/Disable Intel® VT-d Coherency support. | Only visible when Intel® Virtualization Technology for Directed I/O is enabled. |
| ATS Support | Enabled<br>Disabled | Enable/Disable Intel® VT-d Address Translation Services (ATS) support. | Only visible when Intel® Virtualization Technology for Directed I/O is enabled. |
| Pass-through DMA Support | Enabled<br>Disabled | Enable/Disable Intel® VT-d Pass-through DMA support. | Only visible when Intel® Virtualization Technology for Directed I/O is enabled. |
| Hardware Prefetcher | Enabled<br>Disabled | Hardware Prefetcher is a speculative prefetch unit within the processor(s).<br>**Note**: Modifying this setting may affect system performance. | |
| Adjacent Cache Line Prefetch | Enabled<br>Disabled | [Enabled] - Cache lines are fetched in pairs (even line + odd line).<br>[Disabled] - Only the current cache line required is fetched.<br>**Note**: Modifying this setting may affect system performance. | |

#### 2.6.5.2.2 Memory Screen

The Memory screen allows the user to view details about the system memory DDR3 DIMMs installed. This screen also allows the user to open the Configure Memory RAS and Performance screen.

To access this screen from the Main screen, select **Advanced** > **Memory**.

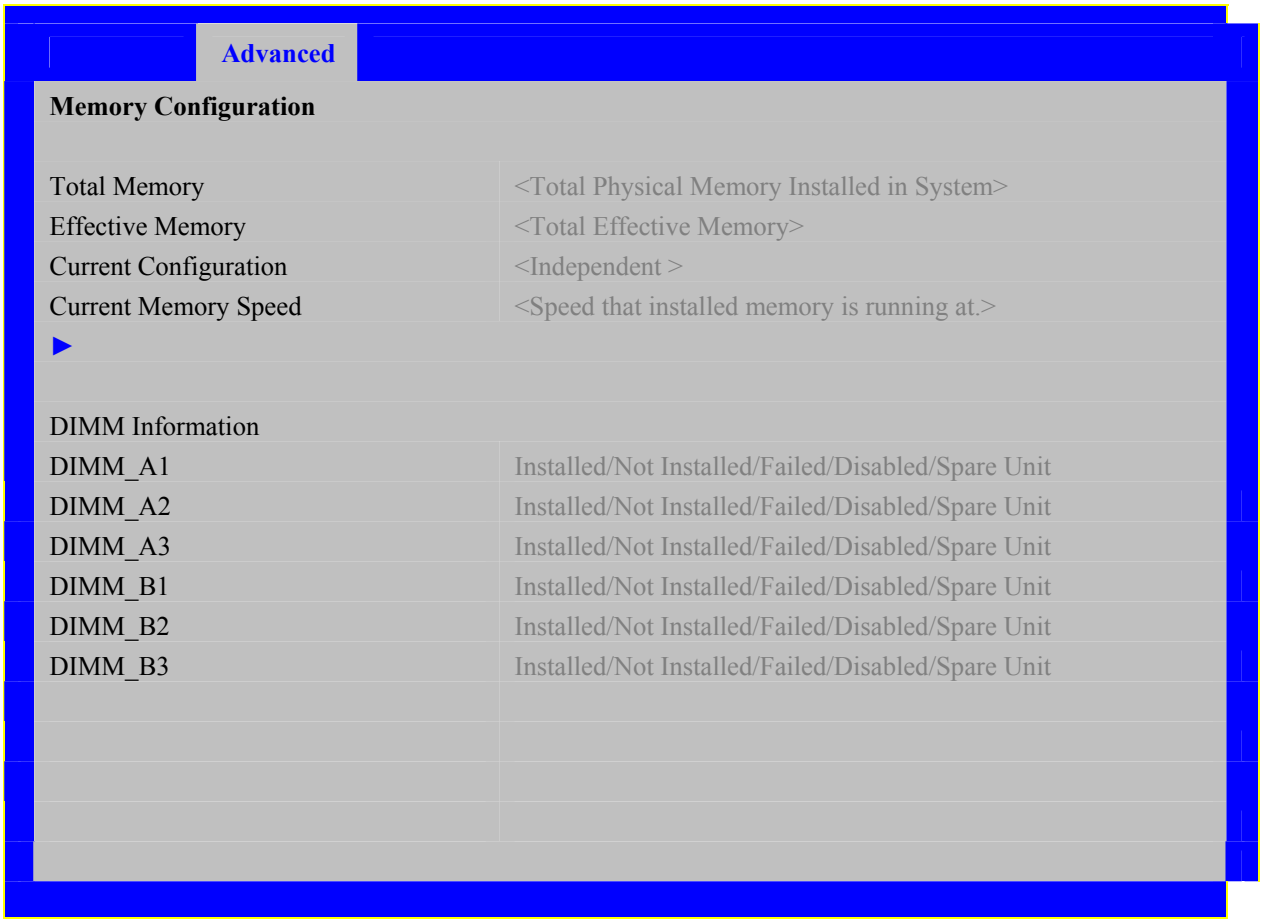



**Figure 12. Setup Utility – Memory Configuration Screen Display**

**Table 16. Setup Utility – Memory Configuration Screen Fields**

| Setup Item | Comments |
|---|---|
| Total Memory | **Information only.** The amount of memory available in the system in the form of installed DDR3 DIMMs in units of MB or GB. |
| Effective Memory | **Information only.** The amount of memory available to the operating system in MB or GB.<br>The Effective Memory is the difference between the Total Physical Memory and the sum of all memory reserved for internal usage, RAS redundancy and SMRAM. This difference includes the sum of all DDR3 DIMMs that failed Memory BIST during POST, or were disabled by the BIOS during memory discovery phase to optimize memory configuration. |
| Current Configuration | **Information only.** Displays one of the following:<br>**Independent Mode**: System memory is configured for optimal performance and efficiency and no RAS is enabled.<br>**Sparing Mode:** System memory is configured for RAS with optimal effective memory. |
| Current Memory Speed | **Information only.** Displays the speed the memory is running at. |

| Setup Item | Comments |
|---|---|
| DIMM_ XY | Displays the state of each DIMM socket present on the board. Each DIMM socket field reflects one of the following possible states:<br>**Installed**: There is a DDR3 DIMM installed in this slot.<br>**Not Installed**: There is no DDR3 DIMM installed in this slot.<br>**Disabled**: The DDR3 DIMM installed in this slot was disabled by the BIOS to optimize memory configuration.<br>**Failed**: The DDR3 DIMM installed in this slot is faulty / malfunctioning.<br>**Spare Unit**: The DDR3 DIMM is functioning as a spare unit for memory RAS purposes.<br>**Note**: X denotes the Channel Identifier and Y denote the DIMM Identifier within the Channel. |

#### 2.6.5.2.3 Mass Storage Controller Screen

The Mass Storage screen allows the user to configure the SATA/SAS controller when it is present on the baseboard, midplane, or backplane of an Intel system.

To access this screen from the Main menu, select **Advanced** > **Mass Storage**.

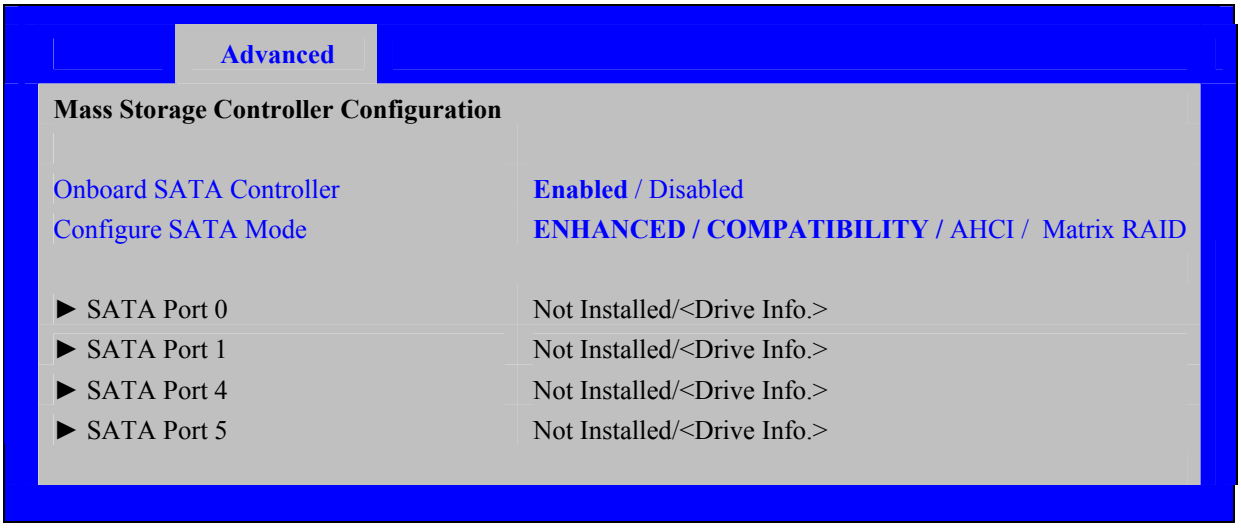



**Figure 13. Setup Utility – Mass Storage Controller Configuration Screen Display**

**Table 17. Setup Utility – Mass Storage Controller Configuration Screen Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Onboard SATA Controller | **Enabled**<br>Disabled | Onboard Serial ATA (SATA) controller. | |
| SATA Mode | **ENHANCED**<br>Compatibility<br>AHCI<br>Matrix RAID | [ENHANCED] - Supports up to 6 SATA ports with IDE Native Mode.<br>[COMPATIBILITY] - Supports up to 4 SATA ports[0/1/2/3] with IDE Legacy mode and 2 SATA ports[4/5] with IDE Native Mode.<br>[AHCI] - Supports all SATA ports using the Advanced Host Controller Interface.<br>Intel® Matrix RAID Technology with Software RAID levels 0/1/10 and 5. | Disappears when the Onboard SATA Controller is disabled. |

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| SATA Port 0 | < Not Installed / Drive information> | | **Information only.** This field is unavailable when RAID Mode is enabled. |
| SATA Port 1 | < Not Installed / Drive information> | | **Information only.** This field is unavailable when RAID Mode is enabled. |
| SATA Port 4 | < Not Installed / Drive information> | | **Information only.** This field is unavailable when RAID Mode is enabled. |
| SATA Port 5 | < Not Installed / Drive information> | | **Information only.** This field is unavailable when RAID Mode is enabled. |

#### 2.6.5.2.4 USB Configuration Screen

The USB Configuration screen allows the user to configure the USB controller options.

To access this screen from the Main screen, select **Advanced** > **USB Configuration.**

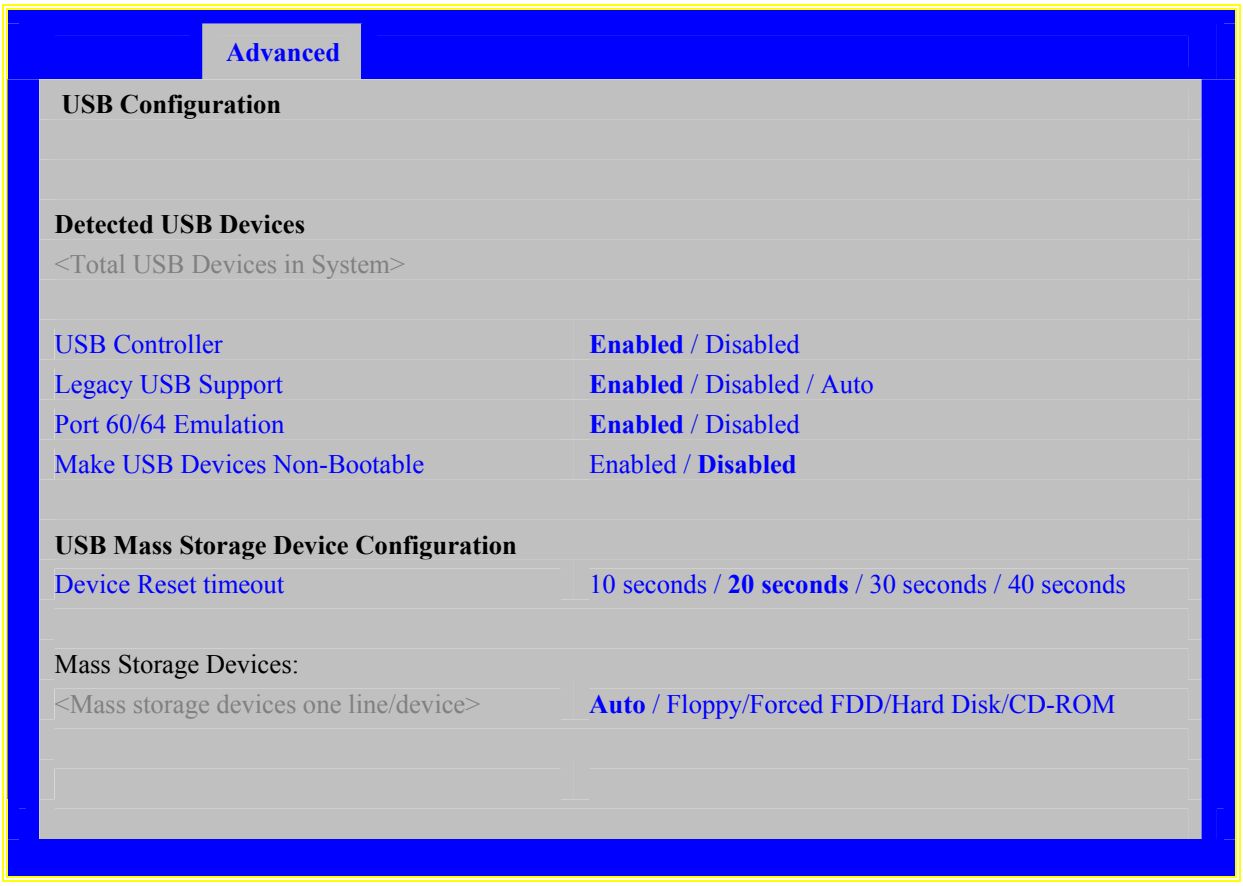



**Figure 14. Setup Utility – USB Controller Configuration Screen Display**

**Table 18. Setup Utility – USB Controller Configuration Screen Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Detected USB Devices | | | Information only. Shows the number of USB devices in the system. |
| USB Controller | **Enabled**<br>Disabled | [Enabled] - All onboard USB controllers are turned on and accessible by the OS.<br>[Disabled] - All onboard USB controllers are turned off and inaccessible by the OS. | |

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Legacy USB Support | **Enabled**<br>Disabled<br>Auto | USB device boot support and PS/2 emulation for USB keyboard and USB mouse devices.<br>[Auto] - Legacy USB support is enabled if a USB device is attached. | Grayed out if the USB Controller is disabled. |
| Port 60/64 Emulation | **Enabled**<br>Disabled | I/O port 60h/64h emulation support.<br>**Note**: This may be needed for legacy USB keyboard support when using an OS that is USB unaware. | Grayed out if the USB Controller is disabled. |
| Make USB Devices Non-Bootable | Enabled<br>**Disabled** | Exclude USB in Boot Table.<br>[Enabled] - This removes all USB Mass Storage devices as Boot options.<br>[Disabled] - This allows all USB Mass Storage devices as Boot options. | Grayed out if the USB Controller is disabled. |
| Device Reset timeout | 10 sec<br>**20 sec**<br>30 sec<br>40 sec | USB Mass Storage device Start Unit command timeout.<br>Setting to a larger value provides more time for a mass storage device to be ready, if needed. | Grayed out if the USB Controller is disabled. |
| One line for each mass storage device in system | **Auto**<br>Floppy<br>Forced FDD<br>Hard Disk<br>CD-ROM | [Auto] - USB devices less than 530 MB are emulated as floppies.<br>[Forced FDD] - HDD formatted drive are emulated as a FDD (e.g., ZIP drive). | Hidden if no USB Mass storage devices are installed.<br>Grayed out if the USB Controller is disabled.<br>This setup screen can show a maximum of eight devices on this screen. If more than eight devices are installed in the system, the USB Devices Enabled shows the correct count, but only displays the first eight devices here. |

#### 2.6.5.2.5 PCI Screen

The PCI Screen allows the user to configure the PCI add-in cards, onboard NIC controllers, and video options.

To access this screen from the Main screen, select **Advanced** > **PCI**.

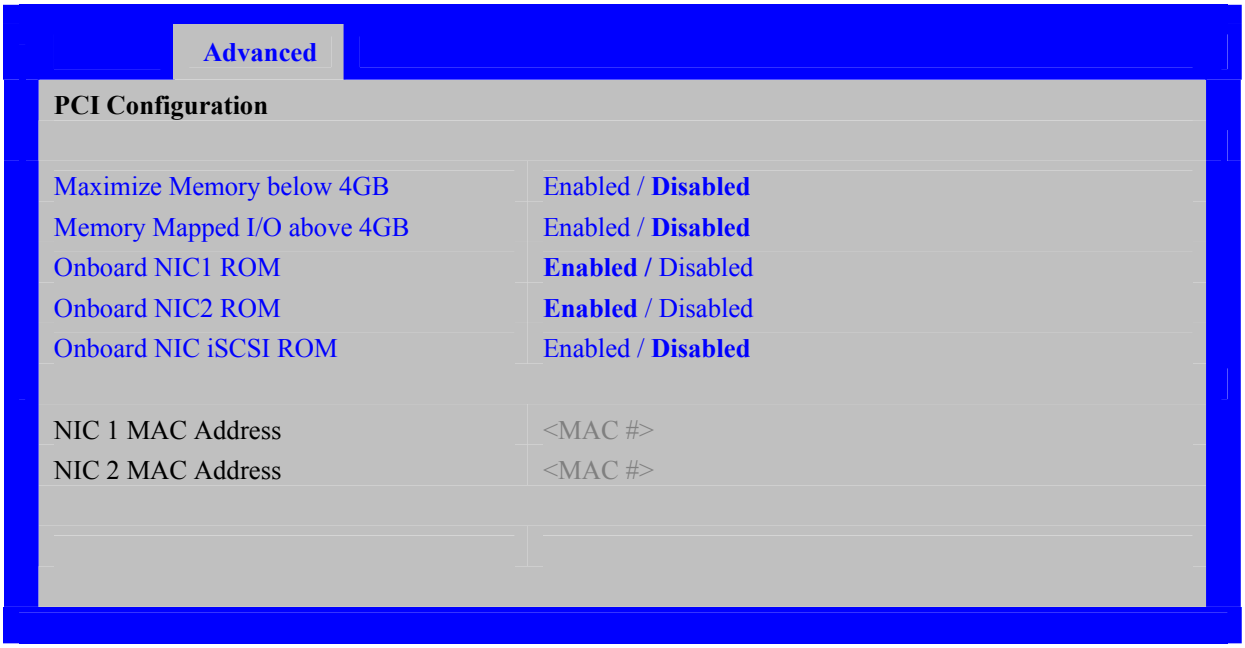



**Figure 15. Setup Utility – PCI Configuration Screen Display**

**Table 19. Setup Utility – PCI Configuration Screen Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Maximize Memory below 4GB | Enabled<br>**Disabled** | If enabled. the BIOS maximizes usage of memory below 4 GB for OS without PAE by limiting PCIE Extended Configuration Space to 64 buses. | |
| Memory Mapped I/O above 4GB | **Enabled**<br>Disabled | Enable or disable memory mapped I/O of 64-bit PCI devices to 4 GB or greater address space. | |
| Onboard NIC1 ROM | **Enabled**<br>Disabled | If enabled. loads the embedded option ROM for the onboard network controllers.<br>**Warning:** If [Disabled] is selected, NIC1 cannot be used to boot or wake the system. | |
| Onboard NIC2 ROM | **Enabled**<br>Disabled | If enabled. loads the embedded option ROM for the onboard network controllers.<br>**Warning:** If [Disabled] is selected, NIC2 cannot be used to boot or wake the system. | |
| Onboard NIC iSCSI ROM | Enabled<br>**Disabled** | If enabled. loads the embedded option ROM for the onboard network controllers.<br><br>**Warning:** If [Disabled] is selected, NIC1 and NIC2 cannot be used to boot or wake the system. | This option is grayed out and not accessible if either the NIC1 or NIC2 ROMs are enabled.<br>**Note:** This option is not available on some models. |
| NIC 1 MAC Address | No entry allowed | | **Information only.** 12 hex digits of the MAC address. |
| NIC 2 MAC Address | No entry allowed | | **Information only.** 12 hex digits of the MAC address. |

#### 2.6.5.2.6 System Acoustic and Performance Configuration

The System Acoustic and Performance Configuration screen allows the user to configure the thermal characteristics of the system.

To access this screen from the Main screen, select **Advanced** > **System Acoustic and Performance Configuration**.

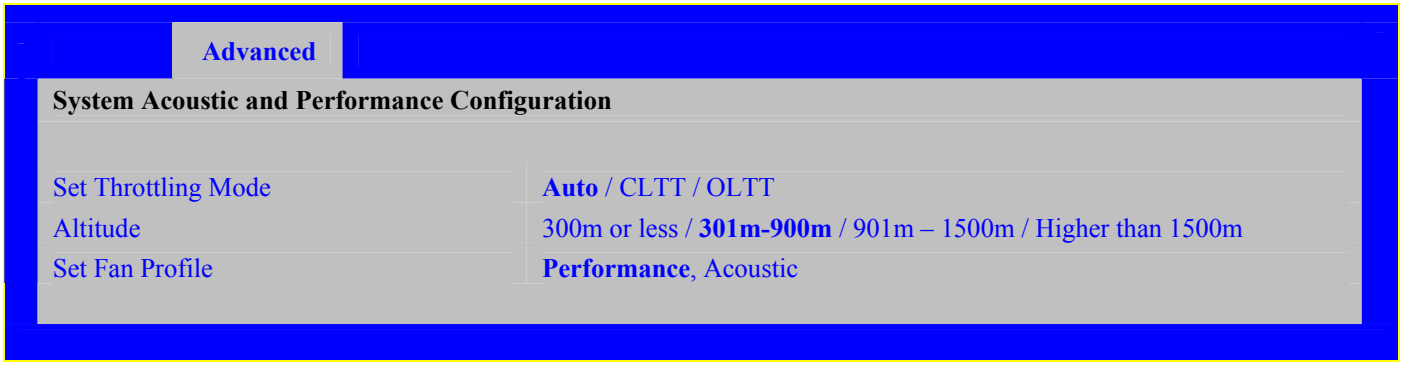



**Figure 16. Setup Utility – System Acoustic and Performance Configuration Screen Display**

**Table 20. Setup Utility – System Acoustic and Performance Configuration Screen Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Set Throttling Mode | **Auto**<br>CLTT<br>OLTT | [Auto] – Auto Throttling mode.<br>[CLTT] – Closed Loop Thermal Throttling Mode.<br>[OLTT] – Open Loop Thermal Throttling Mode. | **Note:** The OLTT option is shown for **informational purposes only.** If the user selects OLTT, the BIOS overrides that selection if the system can support CLTT. OLTT is configured only when UDIMMs without Thermal Sensors are installed. |
| Altitude | 300m or less<br>**301m-900m**<br>901m-1500m<br>Higher than 1500m | [300m or less] (980ft or less)<br>Optimal performance setting near sea level.<br>[301m - 900m] (980ft - 2950ft)<br>Optimal performance setting at moderate elevation.<br>[901m – 1500m] (2950ft – 4920ft)<br>Optimal performance setting at high elevation.<br>[Higher than 1500m] (4920ft or greater)<br>Optimal performance setting at the highest elevations. | |
| Set Fan Profile | **Performance**<br>Acoustics | [Performance] - Fan control provides primary system cooling before attempting to throttle memory.<br>[Acoustic] - The system will favor using throttling of memory over boosting fans to cool the system if thermal thresholds are met. | This option is grayed out if CLTT is enabled. |

### 2.6.5.3 Security Screen

The Security screen allows the user to enable and set the user and administrative password and to lock out the front panel buttons so they cannot be used.

Trusted Platform Module (TPM) security is NOT supported on the Server Board S3420TH.

To access this screen from the Main screen, select **Security**.

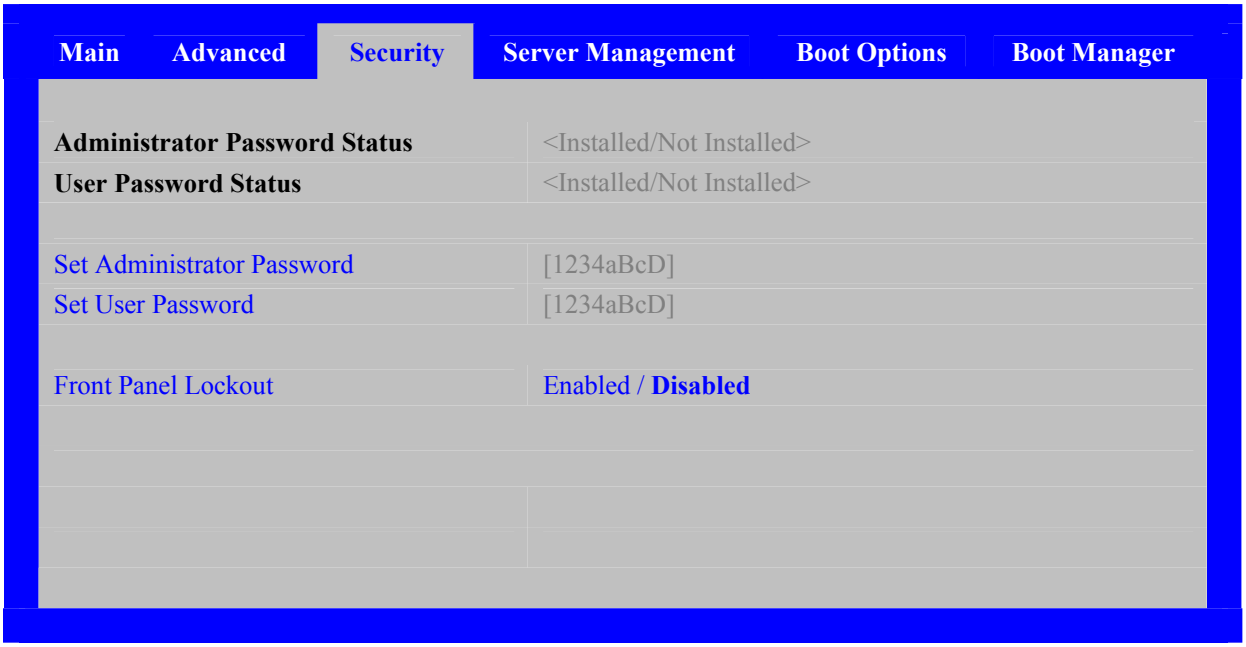



**Figure 17. Setup Utility – Security Configuration Screen Display**

**Table 21. Setup Utility – Security Configuration Screen Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Administrator Password Status | <Installed<br>Not Installed> | | **Information only.** Indicates the status of the administrator password. |
| User Password Status | <Installed<br>Not Installed> | | **Information only.** Indicates the status of the user password. |
| Set Administrator Password | [123aBcD] | Administrator password is used to control change access in BIOS Setup Utility.<br>Only alphanumeric characters can be used. Maximum length is 7 characters. It is case sensitive.<br>**Note:** Administrator password must be set in order to use the user account. | This option is only to control access to the setup. Administrator has full access to all the setup items. Clearing the Administrator password also clears the user password. |
| Set User Password | [123aBcD] | User password is used to control entry access to BIOS Setup Utility.<br>Only alphanumeric characters can be used. Maximum length is 7 characters. It is case sensitive.<br>**Note:** Removing the administrator password also automatically removes the user password. | Available only if the administrator password is installed. This option only protects the setup.<br>User password only has limited access to the setup items. |
| Front Panel Lockout | Enabled<br>**Disabled** | If enabled, locks the power button and reset button on the system's front panel. If [Enabled] is selected, power and reset must be controlled via a system management interface. | |

#### 2.6.5.4 Server Management Screen

The Server Management screen allows the user to configure several server management features. This screen also provides an access point to the screens for configuring console redirection and displaying system information.

To access this screen from the Main screen, select **Server Management**.


**Figure 18. Setup Utility – Server Management Configuraiton Screen Display**

**Table 22. Setup Utility – Server Management Configuration Screen Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Assert NMI on SERR | **Enabled**<br>Disabled | On SERR, generate an NMI and log an error.<br>**Note**: [Enabled] must be selected for the Assert NMI on PERR setup option to be visible. | |
| Assert NMI on PERR | **Enabled**<br>Disabled | On PERR, generate an NMI and log an error.<br>**Note**: This option is only active if the Assert NMI on SERR option is [Enabled] selected. | |
| Resume on AC Power Loss | **Stay Off**<br>Last state<br>Reset | System action to take on AC power loss recovery.<br>[Stay Off] - System stays off.<br>[Last State] - System returns to the same state before the AC power loss.<br>[Reset] - System powers on. | |
| Clear System Event Log | Enabled<br>**Disabled** | If enabled, clears the System Event Log. All current entries will be lost.<br>**Note**: This option is reset to [Disabled] after a reboot. | |
| FRB-2 Enable | **Enabled**<br>Disabled | Fault Resilient Boot (FRB).<br>If enabled, the BIOS programs the BMC watchdog timer for approximately 6 minutes. If the BIOS does not complete POST before the timer expires, the BMC resets the system. | |
| O/S Boot Watchdog Timer | **Enabled**<br>Disabled | If enabled, the BIOS programs the watchdog timer with the timeout value selected. If the OS does not complete booting before the timer expires, the BMC resets the system and an error is logged.<br>Requires OS support or Intel Management Software. | |
| O/S Boot Watchdog Timer Policy | **Power Off**<br>Reset | If the OS boot watchdog timer is enabled, this is the system action taken if the watchdog timer expires.<br>[Reset] - System performs a reset.<br>[Power Off] - System powers off. | Grayed out when the O/S Boot Watchdog Timer is disabled. |
| O/S Boot Watchdog Timer Timeout | 5 minutes<br>**10 minutes**<br>15 minutes<br>20 minutes | If the OS watchdog timer is enabled, this is the timeout value used by the BIOS to configure the watchdog timer. | Grayed out when the O/S Boot Watchdog Timer is disabled. |

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Plug & Play BMC Detection | Enabled<br>**Disabled** | If enabled, the BMC is detectable by OSs that support plug and play loading of an IPMI driver. Do not enable if your OS does not support this driver. | |
| System Information | | View system information | Takes the user to the System Information screen. |
| BMC Configuration | | View/Configure BMC LAN channel and User settings | Takes the user to the BMC configuration screen.<br>Information only. |

#### 2.6.5.5 Server Management System Information Screen

The Server Management System Information screen allows the user to view part numbers, serial numbers, and firmware revisions.

To access this screen from the Main screen, select **Server Management** > **System Information**.

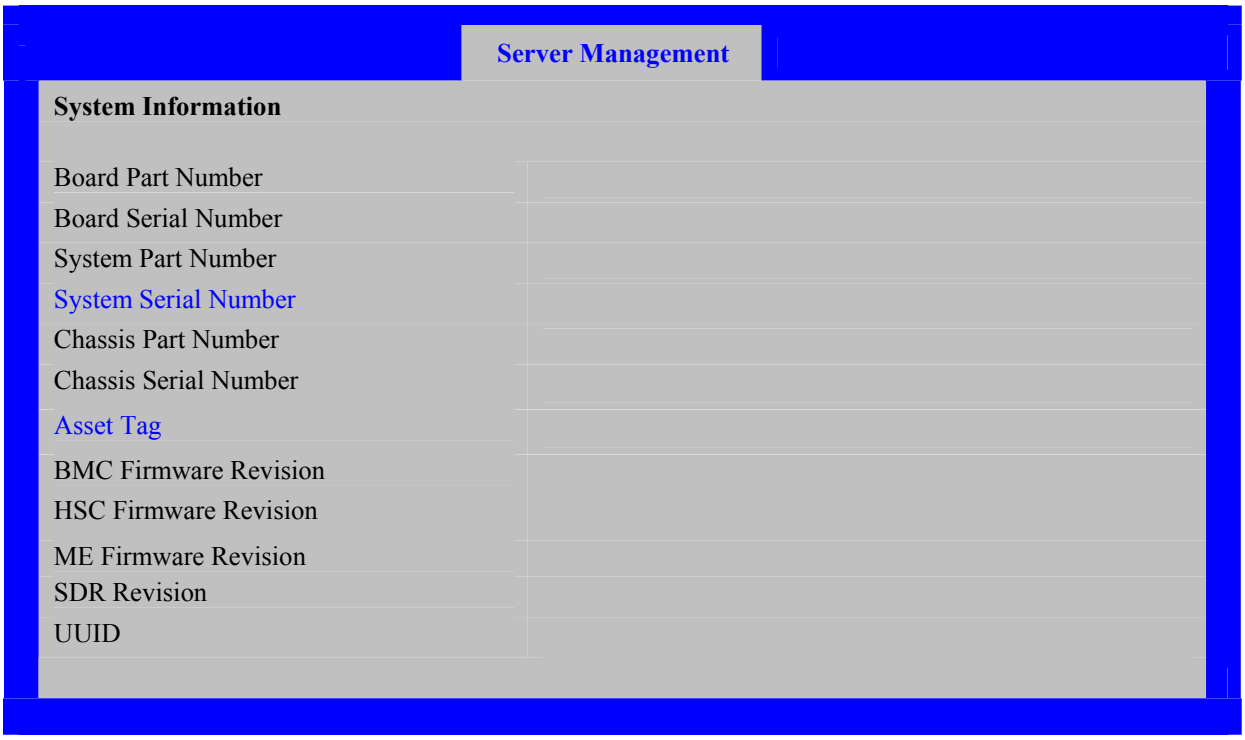



**Figure 19. Setup Utility – Server Management System Information Screen Display**

**Table 23. Setup Utility – Server Management System Information Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Board Part Number | | | **Information only** |
| Board Serial Number | | | **Information only** |
| System Part Number | | | **Information only.** |
| System Serial Number | | Press <Enter> to edit system Serial Number and then use Backspace to delete existing value.<br>Maximum length is 20 characters | **Information only.** |
| Chassis Part Number | | | **Information only.** |
| Chassis Serial Number | | | **Information only.** |

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Asset Tag | | Press <Enter> to edit system Serial Number and then use Backspace to delete existing value.<br>Maximum length is 20 characters | **Information only.** |
| BMC Firmware Revision | | | **Information only** |
| HSC Firmware Revision | | | **Information only.** If there is no HSC installed, the Firmware Revision Number appears as **"0,00"**. |
| ME Firmware Revision | | | **Information only.** |
| SDR Revision | | | **Information only** |
| UUID | | | **Information only** |

#### 2.6.5.6 BMC Configuration

The Server Management System Information screen allows the user to view part numbers, serial numbers, and firmware revisions.

The BMC configuration screen allows you to configure the BMC Baseboard, RMM3 LAN channel and User settings. User can configure first five BMC user's settings.

**Information only:** BMC configuration screen will not available on some models.

To access this screen from the Main screen, select **Server Management** >**BMC Configuration.**

**Figure 20. Setup Utility – BMC configuration Screen Display**

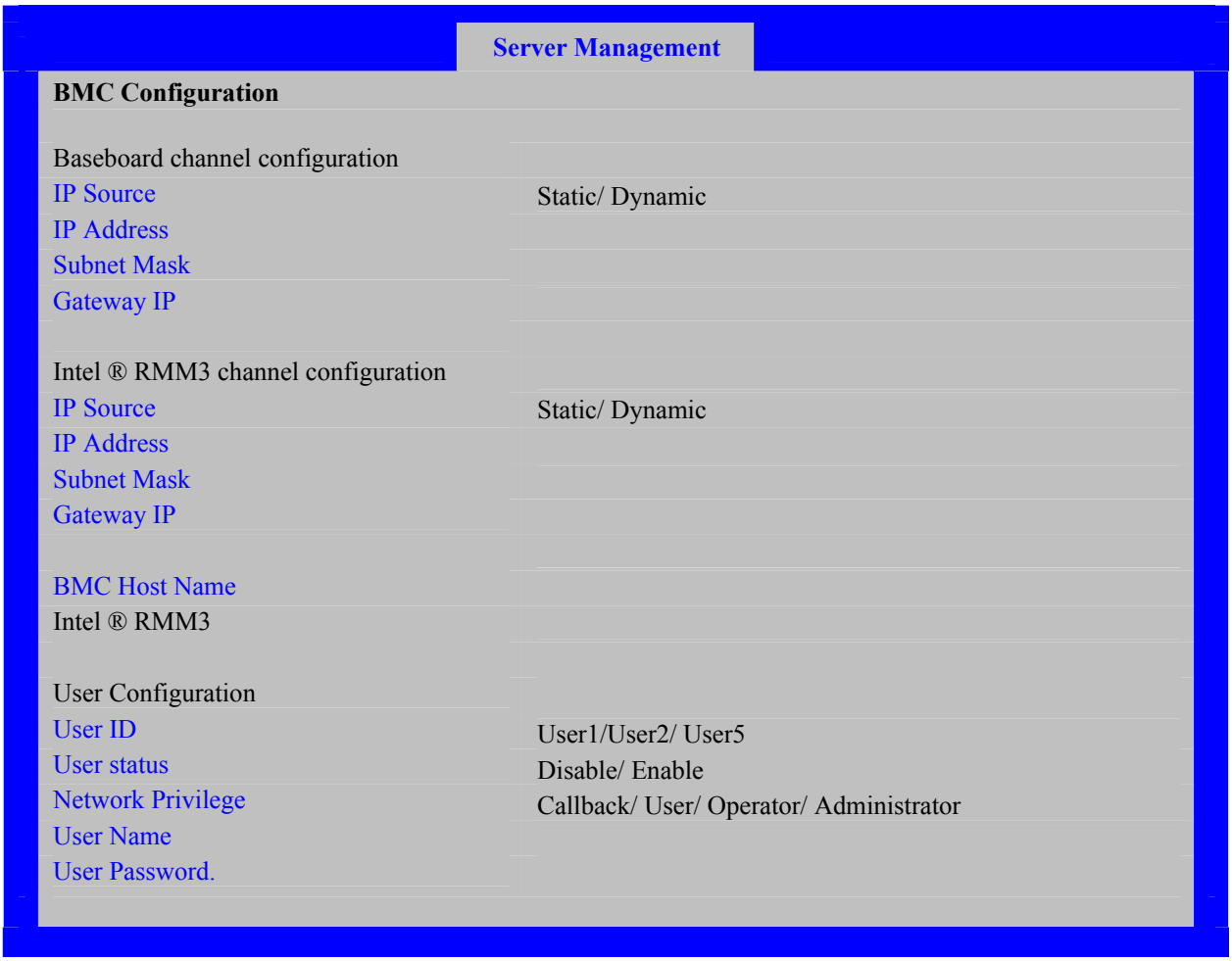



**Table 24. Setup Utility – BMC configuration Screen Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| IP source | Static<br>Dynamic | Select BMC IP source. When Static option is selected, IP address, subnet mask and gateway are editable. When Dynamic option selected, these fields are read-only and IP is address acquired automatically (DHCP). | |
| IP address | | View / Edit IP address. Press <Enter> to edit. | |
| Subnet Mask | | View / Edit subnet address. Press <Enter> to edit. | |
| Gateway Mask | | View / Edit Gateway IP address. Press <Enter> to edit. | |
| BMC Host Name | | View / Edit BMC host name. Press <Enter> to edit. | Available only when IP source for any one channel is dynamic option. |
| User ID | User1<br>User2<br>User3<br>User4<br>User5 | Select the user id to configure. | |
| User Status | Enable<br>Disable | Enable / Disable LAN access for selected user. Also enables/disables SOL, KVM media redirection. | |
| User Name | | Press <Enter> to edit user name. User name is string of 4 to 15 alphanumeric characters. User | |

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| | | name must begin with an alphabetic character. | |
| User Password | | Press <Enter> Key to enter password. Only alphanumeric characters can be used. Maximum length is 15 characters and case sensitive.<br>**Note: Password entered will override any previously set password. | This filed will not indicate whether there is password set already. |

### 2.6.5.7 Boot Options Screen

The Boot Options screen displays any bootable media encountered during POST, and allows the user to configure the preferred boot device.

To access this screen from the Main screen, select **Boot Options**.


**Figure 21. Setup Utility – Boot Options Screen Display**

**Table 25. Setup Utility – Boot Options Screen Fields**

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| Boot Timeout | 0 - 65535 | The number of seconds the BIOS should pause at the end of POST to allow the user to press the [F2] key for entering the BIOS Setup utility.<br>Valid values are 0-65535. Zero is the default. A value of 65535 causes the system to go to the Boot Manager menu and wait for user input for every system boot. | After entering the preferred timeout, press the Enter key to register that timeout value to the system. These settings are in seconds. |
| Boot Option #x | Available boot | Set system boot order by selecting the | |

| Setup Item | Options | Help Text | Comments |
|---|---|---|---|
| | devices. | boot option for this position. | |
| Hard Disk Order | | Set the order of the legacy devices in this group. | Visible when one or more hard disk drives are in the system. |
| CDROM Order | | Set the order of the legacy devices in this group. | Visible when one or more CD-ROM drives are in the system. |
| Floppy Order | | Set the order of the legacy devices in this group. | Visible when one or more floppy drives are in the system. |
| Network Device Order | | Set the order of the legacy devices in this group. | Visible when one or more of these devices are available in the system. |
| BEV Device Order | | Set the order of the legacy devices in this group. | Visible when one or more of these devices are available in the system. |
| Add New Boot Option | | Add a new EFI boot option to the boot order. | This option is only visible if an EFI bootable device is available to the system (for example, a USB drive). |
| Delete Boot Option | | Remove an EFI boot option from the boot order. | If the EFI shell is deleted, you can restore it by setting CMOS defaults (F9). |
| EFI Optimized Boot | Enabled<br>**Disabled** | If enabled, the BIOS only loads modules required for booting EFI-aware Operating Systems. | |
| Boot Option Retry | Enabled<br>**Disabled** | If enabled, this continually retries non-EFI-based boot options without waiting for user input. | |

If all types of bootable devices are installed in the system, the default boot order is:

1. CD/DVD-ROM
2. Floppy Disk Drive
3. Hard Disk Drive
4. PXE Network Device
5. BEV (Boot Entry Vector) Device
6. EFI Shell and EFI Boot paths

#### 2.6.5.7.1 Add New Boot Option Screen

The Add New Boot Option screen allows the user to add boot option to the boot order.

To access this screen from the Main screen, select **Boot Options** > **Add New Boot Options**.

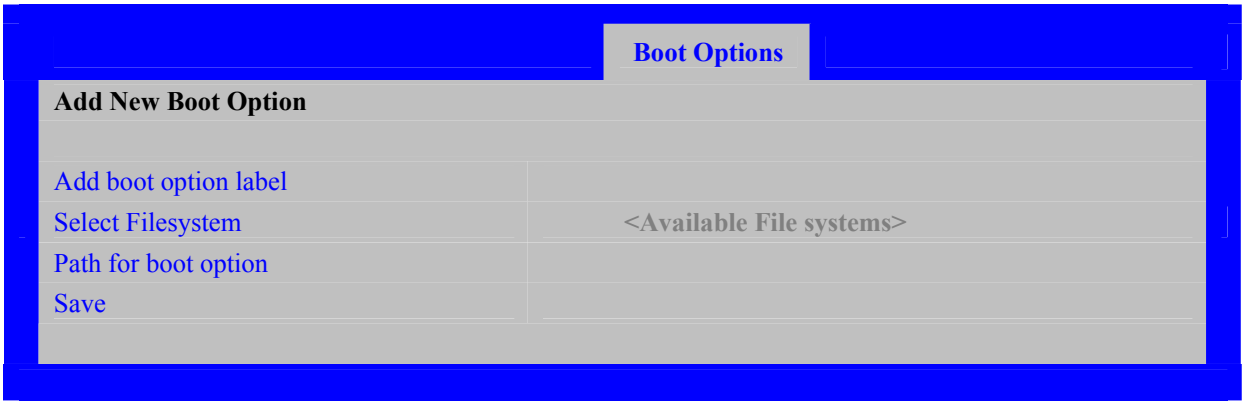



**Figure 22. Setup Utility – Add New Boot Options Screen Display**

**Table 26. Setup Utility – Add New Boot Options Screen Fields**

| Setup Item | Options | Help Text |
|---|---|---|
| Add boot option label | | Create the label for the new boot option. |
| Select Filesystem | Select one from list provided. | Select one filesystem from the list. |
| Path for boot option | | Enter the path to boot option in the format: \path\filename.efi |
| Save | | Save the boot option. |

#### 2.6.5.7.2 Delete Boot Option Screen

The Delete Boot Option screen allows the user to remove an EFI boot option from the boot order.

To access this screen from the Main screen, select **Boot Options** > **Delete Boot Options**.

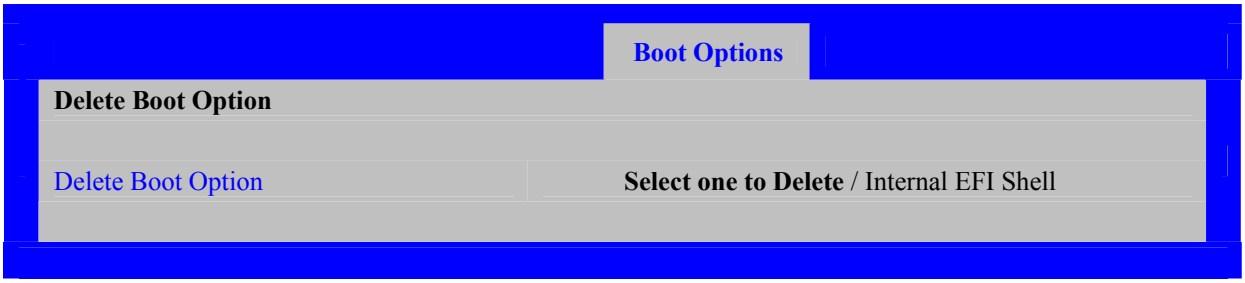



**Figure 23. Setup Utility – Delete Boot Option Screen Display**

**Table 27. Setup Utility – Delete Boot Option Fields**

| Setup Item | Options | Help Text |
|---|---|---|
| Delete Boot Option | Select one to Delete Internal EFI Shell | Remove an EFI boot option from the boot order. |

#### 2.6.5.7.3 Hard Disk Order Screen

The Hard Disk Order screen allows the user to control the hard disks.

To access this screen from the Main screen, choose **Boot Options** > **Hard Disk Order**.

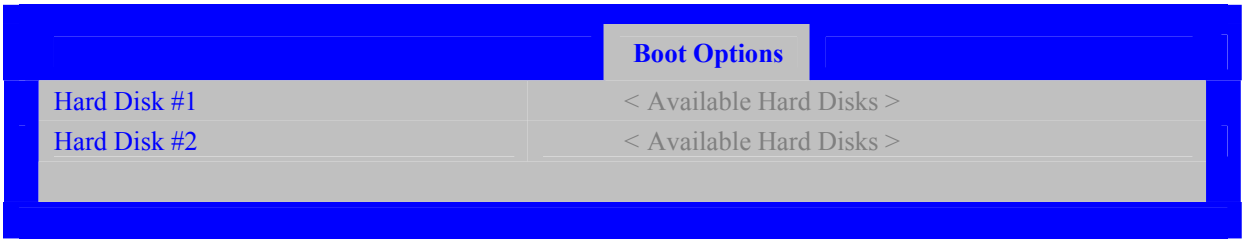



**Figure 24. Setup Utility — Hard Disk Order Screen Display**

**Table 28. Setup Utility — Hard Disk Order Fields**

| Setup Item | Options | Help Text |
|---|---|---|
| Hard Disk #1 | Available Legacy devices for this Device group. | Set system boot order by selecting the boot option for this position. |

| Setup Item | Options | Help Text |
|---|---|---|
| Hard Disk #2 | Available Legacy devices for this Device group. | Set system boot order by selecting the boot option for this position. |

#### 2.6.5.7.4 CDROM Order Screen

The CDROM Order screen allows the user to control the CDROM devices.

To access this screen from the Main screen, select **Boot Options** > **CDROM Order**.

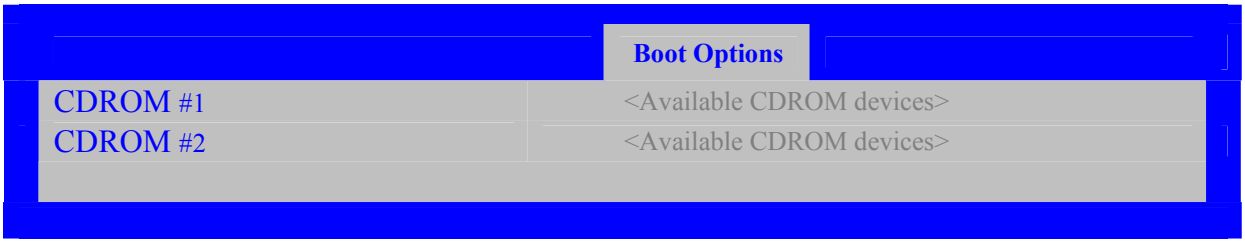



**Figure 25. Setup Utility – CDROM Order Screen Display**

**Table 29. Setup Utility – CDROM Order Fields**

| Setup Item | Options | Help Text |
|---|---|---|
| CDROM #1 | Available Legacy devices for this Device group. | Set system boot order by selecting the boot option for this position. |
| CDROM #2 | Available Legacy devices for this Device group. | Set system boot order by selecting the boot option for this position. |

#### 2.6.5.7.5 Floppy Order Screen

The Floppy Order screen allows the user to control the floppy drives.

To access this screen from the Main screen, choose **Boot Options** > **Floppy Order**.

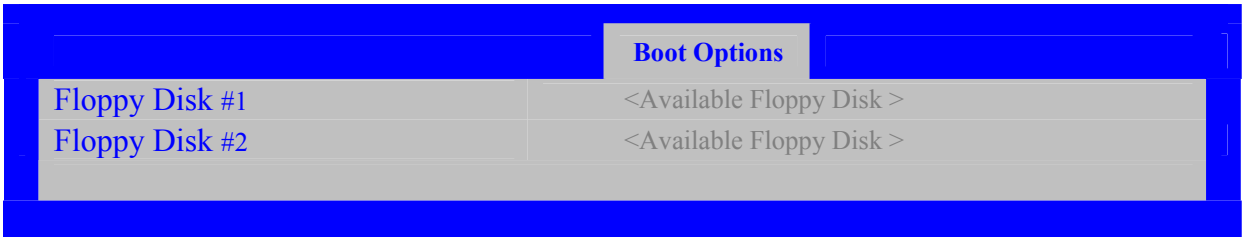



**Figure 26. Setup Utility — Floppy Order Screen Display**

**Table 30. Setup Utility — Floppy Order Fields**

| Setup Item | Options | Help Text |
|---|---|---|
| Floppy Disk #1 | Available Legacy devices for this Device group. | Set system boot order by selecting the boot option for this position. |

| Setup Item | Options | Help Text |
|---|---|---|
| Floppy Disk #2 | Available Legacy devices for this Device group. | Set system boot order by selecting the boot option for this position. |

#### 2.6.5.7.6 Network Device Order Screen

The Network Device Order screen allows the user to control the network bootable devices.

To access this screen from the Main screen, select **Boot Options** > **Network Device Order**.

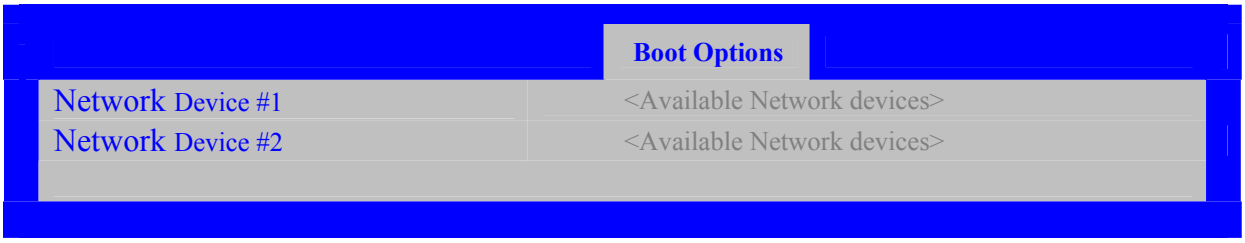



**Figure 27. Setup Utility – Network Device Order Screen Display**

**Table 31. Setup Utility – Network Device Order Fields**

| Setup Item | Options | Help Text |
|---|---|---|
| Network Device #1 | Available Legacy devices for this Device group. | Set system boot order by selecting the boot option for this position. |
| Network Device #2 | Available Legacy devices for this Device group. | Set system boot order by selecting the boot option for this position. |

#### 2.6.5.7.7 BEV Device Order Screen

The BEV Device Order screen allows the user to control the BEV bootable devices.

To access this screen from the Main screen, select **Boot Options** > **BEV Device Order**.

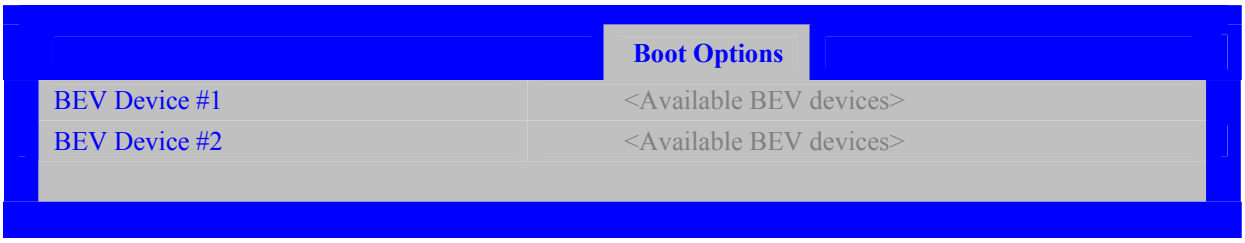



**Figure 28. Setup Utility – Network Device Order Screen Display**

**Table 32. Setup Utility – Network Device Order Fields**

| Setup Item | Options | Help Text |
|---|---|---|
| BEV Device #1 | Available Legacy devices for this Device group. | Set system boot order by selecting the boot option for this position. |

| Setup Item | Options | Help Text |
|---|---|---|
| BEV Device #2 | Available Legacy devices for this Device group. | Set system boot order by selecting the boot option for this position. |

### 2.6.5.8 Boot Manager Screen

The Boot Manager screen allows the user to view a list of devices available for booting, and to select a boot device for immediately booting the system.

To access this screen from the Main screen, select **Boot Manager**.

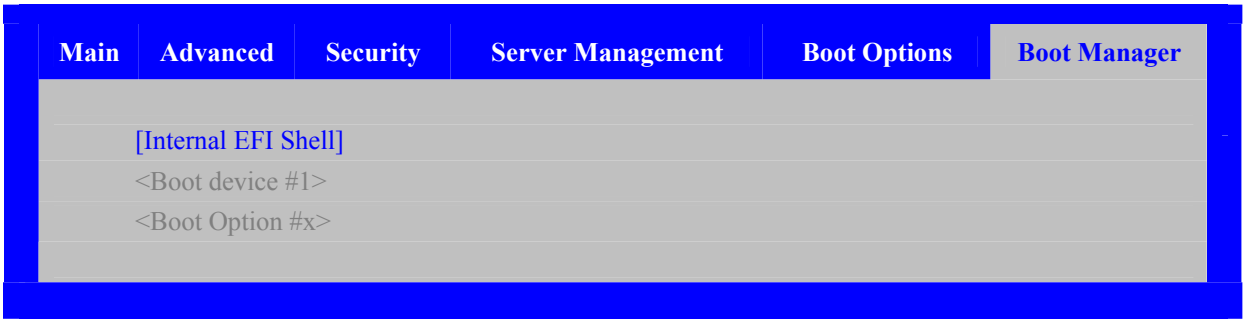



**Figure 29. Setup Utility – Boot Manager Screen Display**

**Table 33. Setup Utility – Boot Manager Screen Fields**

| Setup Item | Help Text |
|---|---|
| Internal EFI Shell | Select this option to boot now.<br>**Note:** This list is not the system boot option order. Use the Boot Options menu to view and configure the system boot option order. |
| Boot Device #x | Select this option to boot now.<br>**Note:** This list is not the system boot option order. Use the Boot Options menu to view and configure the system boot option order. |

### 2.6.5.9 Error Manager Screen

The Error Manager screen displays any errors encountered during POST.

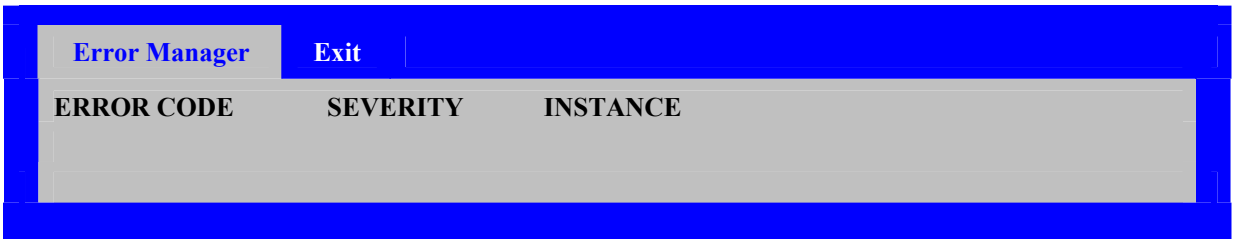



**Figure 30. Setup Utility – Error Manager Screen Display**

**Table 34. Setup Utility – Error Manager Screen Fields**

| Setup Item | Comments |
|---|---|
| Displays System Errors | **Information only**. Displays errors that occurred during the POST. |

### 2.6.5.10 Exit Screen

The Exit screen allows the user to choose whether to save or discard the configuration changes made on the other screens. It also allows the user to restore the server to the factory defaults or to save or restore them to set of user-defined default values. If Load Default Values is selected, the factory default settings (noted in bold in the tables in this chapter) are applied. If Load User Default Values is selected, the system is restored to previously saved user-defined default values.

.

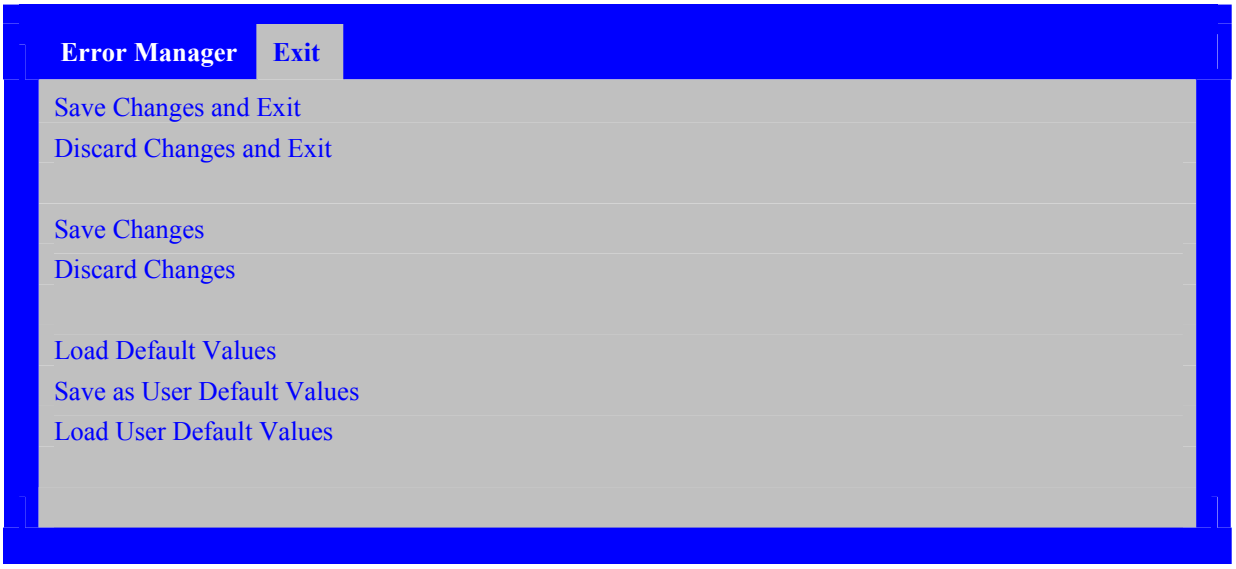



**Figure 31. Setup Utility – Error Manager Screen Display**

**Table 35. Setup Utility – Error Manager Screen Fields**

| Setup Item | Help Text | Comments |
|---|---|---|
| Save Changes and Exit | Exit the BIOS Setup utility after saving changes. The system reboots if required.<br>The [F10] key can also be used. | User is prompted for confirmation only if any of the setup fields were modified. |
| Discard Changes and Exit | Exit the BIOS Setup utility without saving changes.<br>The [Esc] key can also be used. | User is prompted for confirmation only if any of the setup fields were modified. |
| Save Changes | Save changes without exiting the BIOS Setup Utility.<br>**Note:** Saved changes may require a system reboot before taking effect. | User is prompted for confirmation only if any of the setup fields were modified. |
| Discard Changes | Discard changes made since the last Save Changes operation was performed. | User is prompted for confirmation only if any of the setup fields were modified. |
| Load Default Values | Load factory default values for all BIOS Setup utility options.<br>The [F9] key can also be used. | User is prompted for confirmation. |
| Save as User Default Values | Save current BIOS Setup utility values as custom user default values. If needed, the user default values can be restored via the Load User Default Values option below.<br>**Note:** Clearing the CMOS or NVRAM causes the user default values to be reset to the factory default values. | User is prompted for confirmation. |
| Load User Default Values | Load user default values. | User is prompted for confirmation. |

### 2.6.6 Loading BIOS Defaults

Different mechanisms exist for resetting the system configuration to the default values. When a request to reset the system configuration is detected, the BIOS loads the default system configuration values during the next POST. You can send the request to reset the system to the defaults in the following ways:

Pressing <F9> from within the BIOS Setup utility.

Moving the clear system configuration jumper.

IPMI command (set System Boot options command)

Int15 AX=DA209

Choosing Load User Defaults from the Exit page of the BIOS Setup loads user set defaults instead of the BIOS factory defaults.

The recommended steps to load the BIOS defaults are:

1. Power down the system (Do not remove AC power).
2. Move the Clear CMOS jumper from pins 1-2 to pins 2-3.
3. Move the Clear CMOS jumper from pins 2-3 to pins 1-2.
4. Power up the system.

## 2.7 Connector/Header Locations and Pin-outs

### 2.7.1 General Purpose Connectors

The following section provides detailed information regarding all connectors, headers, and jumpers on the server board. It lists all connector types available on the board and the corresponding reference designators printed on the silkscreen.

**Table 36. Board Connector Matrix**

| Name | Ref on MB | Connector Type | Pin Count |
|---|---|---|---|
| RMM3 Lite-V internal header | J1G1, J7E1 | Header | 8 |
| Front USB connector | J7K1 | Connector | 24 |
| Front Panel header | J8K1 | Header | 34 |
| SAS 4i connector | J9J2 | Connector | 32 |
| IPMB header | J6K1 | header | 4 |
| System Power connector | J9H1 | connector | 44 |
| Board Identity LED connector | J3B1 | connector | 3 |
| FAN connector | J4K1, J6K2, J4K2 | connector | 8 |
| Power connector to HDD | J7K2 | connector | 6 |

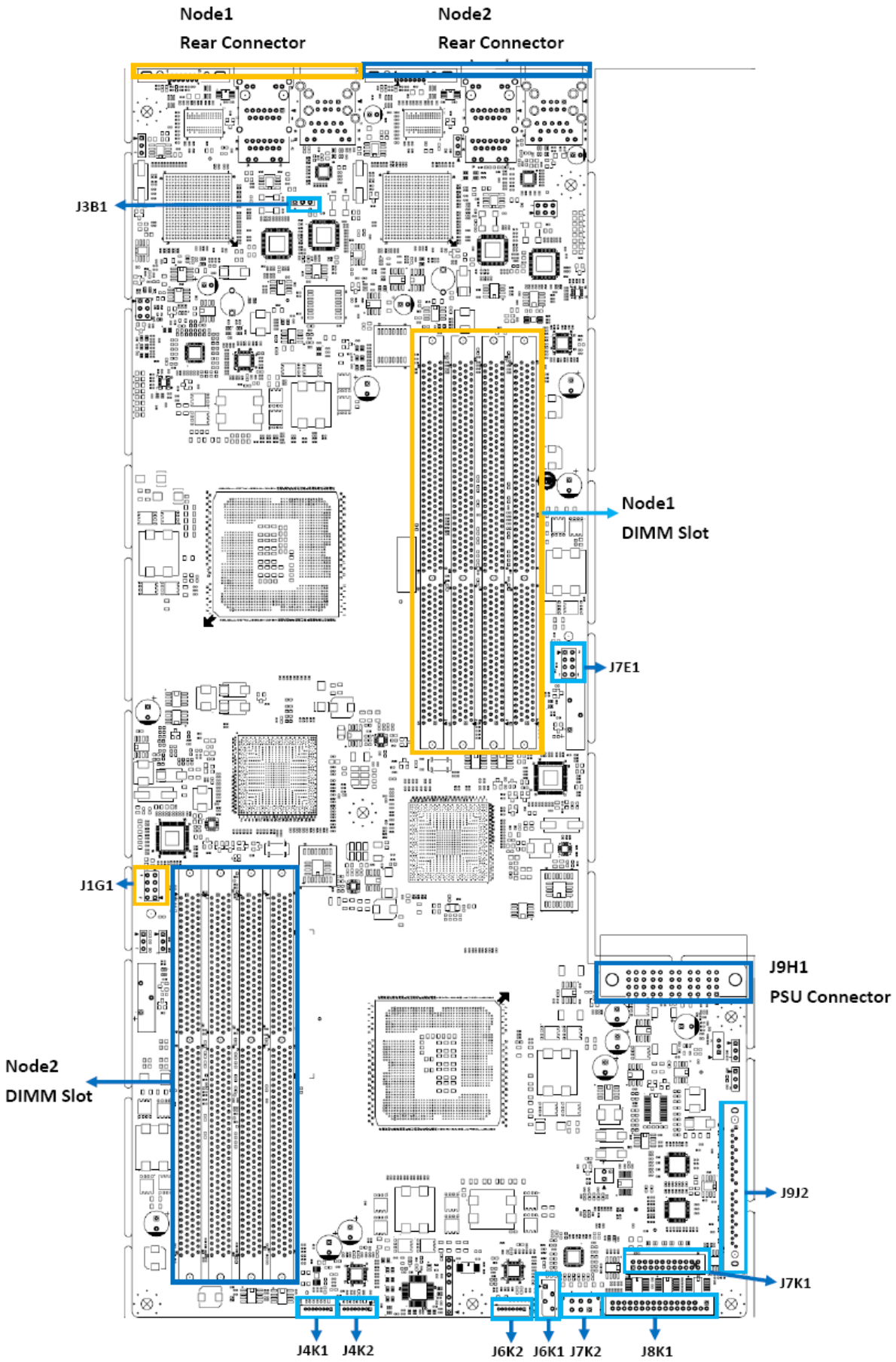
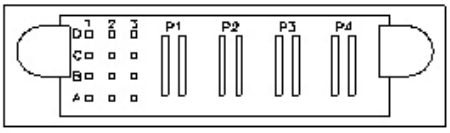



**Figure 32. Connector locations on server board S3420TH**

#### 2.7.1.1 Power Connectors

The main power supply connection uses a special designed connector (J9H1) to provide power to both nodes on the same board.




| SIGNAL PINS | | | | POWER BLADE | | | |
|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | P1 | P2 | P3 | P4 |
| D | A0 | PWOK | +5VSB | RTN | RTN | +12V | +12V |
| C | 12VLS | +15Vcc | +12VRS | | | | |
| B | PS-ON | SCL | B/P FAIL | | | | |
| A | PS-KILL/A1 | SDA | +5VSB | | | | |

**Figure 33. Connector Pin-out**

**Table 37. Power connector pin-out (J9H1)**

| Signal | Description | Signal | Description |
|---|---|---|---|
| 12VLS | +12V load share bus | PWOK | Power OK output |
| 5 VSB | 5V standby output | +12 VRS | 12V remote sense |
| PSON# | Power enable input | PS-KILL#/A1 | Supply fast shutdown/I2C address bit1 |
| B/P FAIL | B/P fail input | SCL | I2C clock signal |
| A0 | I2C address bit 0 | SDA | I2C data signal |
| +15VCC | B/P VCC | | |

#### 2.7.1.2 System Management Headers

##### 2.7.1.2.1 Intel® Remote Management Module 3 Lite-V (Intel® RMM3 Lite-V) Connector

A 8-pin Intel® RMM 3 Lite-V connector is included for every node on the server board S3420TH to support the optional Intel® Remote Management Module 3 Lite-V. This server board does not support third-party management card.

**Note:** This connector is not compatible with the Intel® Remote Management Module 3 (Intel® RMM3), or Intel® Remote Management Module 3 Lite (Intel® RMM3 Lite).

**Table 38. RMM3 Lite-V Internal header pin-out (J1G1, J7E1)**

| Pin # | Signal | Pin # | Signal |
|---|---|---|---|
| 1 | Key | 5 | GND |
| 2 | SPI_IBMC_BK_CS_N | 6 | SPI_IBMC_BK_CLK |
| 3 | P3V3_AUX | 7 | FM_RMM3_PRESENT_N |
| 4 | SPI_IBMC_BK_DO | 8 | SPI_IBMC_BK_DI |

##### 2.7.1.2.2 IPMB Header

**Table 39. IPMB header pin-out (J6K1)**

| Pin # | Signal | Pin # | Signal |
|---|---|---|---|
| 1 | SMB_IPMB_5VSB_DAT_node1 | 3 | SMB_IPMB_5VSB_CLK_node1 |
| 2 | SMB_IPMB_5VSB_DAT_node2 | 4 | SMB_IPMB_5VSB_CLK_node2 |

### 2.7.1.3 Front Control Panel Connector

The server board S3420TH provides a 34-pin front panel connector (J8K1). The following table provides the pin-out for this connector.

**Table 40. Front Control Panel header pin-out (J8K1)**

| Pin # | Signal | Pin # | Signal |
|---|---|---|---|
| 1 | P3V3_AUX | 2 | P5V_STBY_SYS |
| 3 | KEY | 4 | P3V3_AUX_node2 |
| 5 | P3V3 | 6 | P3V3_node2 |
| 7 | FP_ID_N_LED_node1 | 8 | FP_ID_N_LED_node2 |
| 9 | LED_Status_Green_N | 10 | LED_Status_Green_N_node2 |
| 11 | LED_Status_Amber_N | 12 | LED_Status_Amber_N_node2 |
| 13 | LED_NIC1_ACT_BUF_N | 14 | LED_NIC1_ACT_BUF_N_node2 |
| 15 | NC | 16 | NC |
| 17 | SMB_SENS_3V3SB_DAT | 18 | SMB_SENS_3V3SB_DAT_node2 |
| 19 | SMB_SENS_3V3SB_CLK | 20 | SMB_SENS_3V3SB_CLK_node2 |
| 21 | LED_NIC2_ACT_BUF_N | 22 | LED_NIC2_ACT_BUF_N_node2 |
| 23 | NC | 24 | NC |
| 25 | FP_PWR_LED_N | 26 | FP_PWR_LED_N_node2 |
| 27 | FP_PWR_BTN_N | 28 | FP_PWR_BTN_N_node2 |
| 29 | RST_FP_BTN_N | 30 | RST_FP_BTN_N_node2 |
| 31 | FP_ID_BTN_N | 32 | FP_ID_BTN_N_node2 |
| 33 | GND | 34 | GND |

### 2.7.1.4 Front Panel USB Connector

The server board S3420TH provides a 24-pin front panel USB connector (J7K1). The following table provides the pin-out for this connector.

**Table 41. Front Panel USB header pin-out (J7K1)**

| Pin # | Signal | Pin # | Signal |
|---|---|---|---|
| 1 | P5V | 2 | P5V_node2 |
| 3 | P5V_USB_PWR24 | 4 | P5V_USB_PWR24_node2 |
| 5 | P5V_USB_PWR24 | 6 | P5V_USB_PWR24_node2 |
| 7 | USB_PCH_2_FB_DN | 8 | USB_PCH_2_FB_DN_node2 |
| 9 | USB_PCH_2_FB_DP | 10 | USB_PCH_2_FB_DP_node2 |
| 11 | GND | 12 | GND |
| 13 | USB_PCH_4_FB_DN | 14 | USB_PCH_4_FB_DN_node2 |
| 15 | USB_PCH_4_FB_DP | 16 | USB_PCH_4_FB_DP_node2 |
| 17 | GND | 18 | GND |
| 19 | USB_PCH_8_FB_DN | 20 | USB_PCH_8_FB_DN_node2 |
| 21 | USB_PCH_8_FB_DP | 22 | USB_PCH_8_FB_DP |
| 23 | GND | 24 | GND |

### 2.7.1.5 SAS 4i Connector

The server board S3420TH provides a 32-pin SATA/SAS connector (J9J2) for HDD connection. The following table provides the pin-out for this connector.

**Table 42. SAS 4i connector pin-out (J9J2)**

| Pin # | Signal | Pin # | Signal |
|---|---|---|---|
| 1 | GND | 17 | SGPIO_PCH_SCLK_R |
| 2 | SATA0_J_RXP_Node2 | 18 | SGPIO_PCH_SLOAD_R |
| 3 | SATA0_J_RXN_Node2 | 19 | SGPIO_PCH_SDATA0_R |
| 4 | GND | 20 | GND |
| 5 | SATA0_J_TXN_Node2 | 21 | SATA0_J_RXP |
| 6 | SATA0_J_TXP_Node2 | 22 | SATA0_J_RXN |
| 7 | GND | 23 | GND |
| 8 | SATA1_J_RXP_Node2 | 24 | SATA0_J_TXN |
| 9 | SATA1_J_RXN_Node2 | 25 | SATA0_J_TXP |
| 10 | GND | 26 | GND |
| 11 | SATA1_J_TXN_Node2 | 27 | SATA1_J_RXP |
| 12 | SATA1_J_TXP_Node2 | 28 | SATA1_J_RXN |
| 13 | GND | 29 | GND |
| 14 | SGPIO_PCH_SCLK_R_Node2 | 30 | SATA1_J_TXN |
| 15 | SGPIO_PCH_SLOAD_R_Node2 | 31 | SATA1_J_TXP |
| 16 | SGPIO_PCH_SDATA0_R_Node2 | 32 | GND |

### 2.7.1.6 Board Identification LED Connector

The server board S3420TH provides a 3-pin connector (J3B1) for Board ID LED connection. The following table provides the pin-out for this connector.

**Table 43. Board Identification LED connector pin-out (J3B1)**

| Pin # | Signal |
|---|---|
| 1 | ID_LED_signal |
| 2 | 5VDC |
| 3 | Key Pin |

### 2.7.1.7 System cooling FAN connectors

The server board S3420TH provides three 8-pin connectors (J4K1, J6K2, J4K2) for Board cooling FAN sets connection. The following table provides the pin-out for this connector.

**Table 44. System FAN connector pin-out (J4K1, J6K2, J4K2)**

| Pin # | Signal |
|---|---|
| 1 | FAN_PWM |
| 2 | P12V_SYS |
| 3 | FAN_SYS_TACH |
| 4 | GND |
| 5 | GND |
| 6 | FAN_SYS_TACH |
| 7 | P12V_SYS |
| 8 | FAN_PWM |

#### 2.7.1.8 Power to backplane connectors

The server board S3420TH provides a 6-pin connector (J7K2) for providing power to SATA HDD directly. The following table provides the pin-out for this connector.

**Table 45. Power to backplane connector pin-out (J7K2)**

| Pin # | Signal | Pin # | Signal |
|---|---|---|---|
| 1 | +5VDC_node2 | 4 | +5VDC_node1 |
| 2 | +12VDC_node2 | 5 | +12VDC_node1 |
| 3 | GND | 6 | GND |

### 2.7.2 Board Jumpers

The following summary list provides description of board jumpers and their functions.

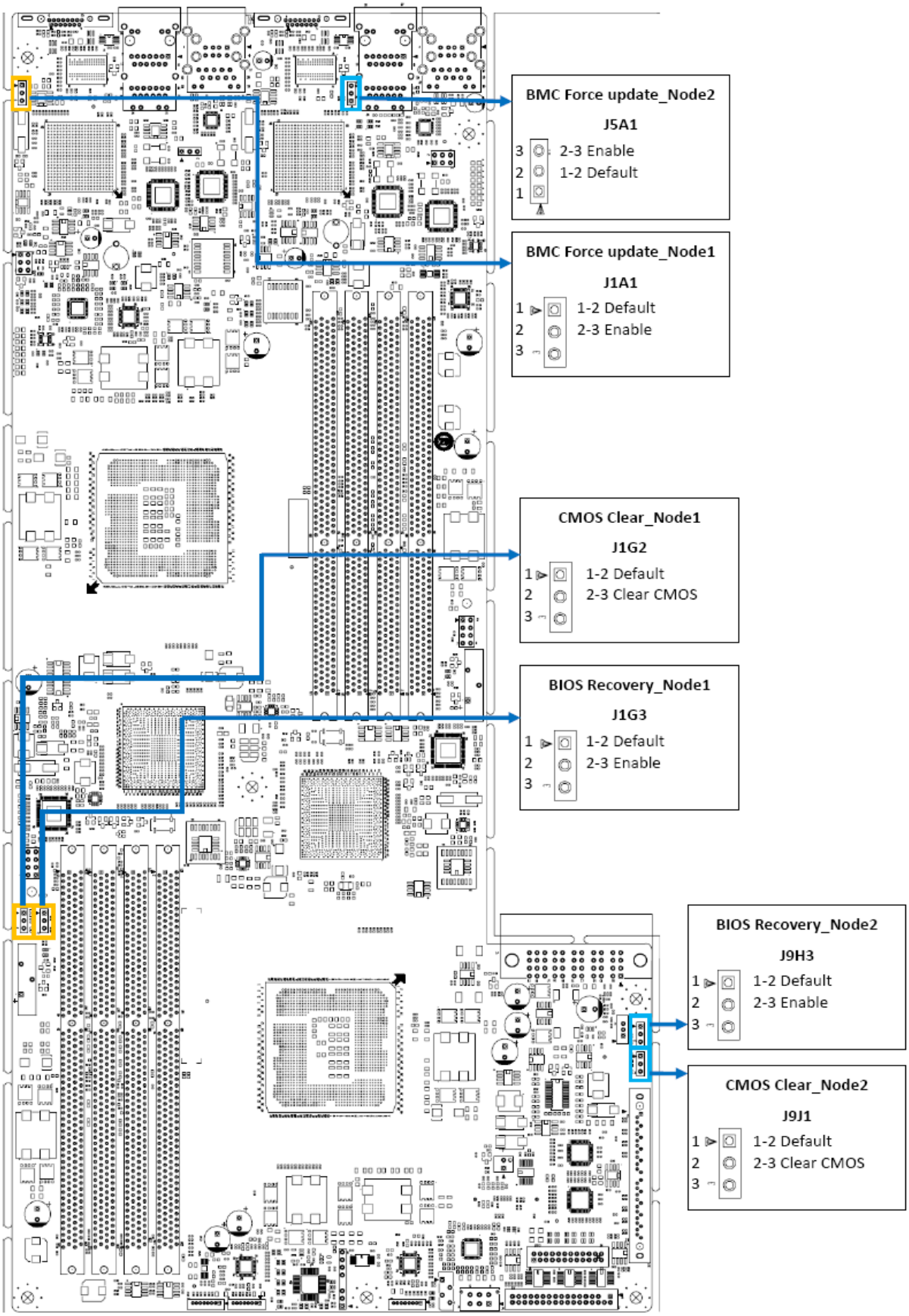



**Figure 34. Jumper locations on board**

#### 2.7.2.1 CMOS Clear (J1G2, J9J1)

When enabled, all CMOS settings will be reset to default.

**Table 46. CMOS Clear (J1G2, J9J1)**

| Name | Pin To Pin | Function | Description |
|---|---|---|---|
| Default | 1-2 | Normal operation | |
| Reset | 2-3 | CMOS Clear | |

#### 2.7.2.2 BIOS Recovery (J1G3, J9H3)

Provide a manual mode of BIOS recovery configures.

**Table 47. BIOS Recovery (J1G3, J9H3)**

| Name | Pin To Pin | Function | Description |
|---|---|---|---|
| Default | 1-2 | Normal operation | |
| Recovery | 2-3 | Recovery | BIOS recovery from other media |

#### 2.7.2.3 BMC Force Update (J1A1, J5A1)

Provide a manual mode of BIOS recovery configures.

**Table 48. BMC Force Update (J1A1, J5A1)**

| Name | Pin To Pin | Function | Description |
|---|---|---|---|
| Default | 1-2 | Normal operation | |
| Enable | 2-3 | Enable | BMC force update |

### 2.7.3 Board LED

**Port 80 LED Displays (Diagnositc LED)**

This Port 80 LEDs provide on board decoding and display of software debug information. The Port 80 interface for the LPC bus is implemented as shown in the table below

**Table 49. Port 80/81 Display Interface on LPC Bus**

| LSB | | | MSB | | | |
|---|---|---|---|---|---|---|
| | | | | | | |
| DS6A1 | DS7A3 | DS7A2 | DS7A1 | POST CODE | | COLOR |
| Q4 | Q5 | Q6 | Q7 | HIGH NIBBLE | | RED |
| Q0 | Q1 | Q2 | Q3 | LOW NIBBLE | | GREEN |
| 0 | 0 | 0 | 0 | 0 | 0 | OFF |
| 0 | 0 | 0 | 0 | | | |
| 0 | 0 | 0 | 0 | 0 | F | GREEN |
| 1 | 1 | 1 | 1 | | | |
| 1 | 1 | 1 | 1 | F | 0 | RED |
| 0 | 0 | 0 | 0 | | | |
| 1 | 1 | 1 | 1 | F | F | AMBER |

| LSB | | | MSB | | | |
|---|---|---|---|---|---|---|
| | | | | | | |
| 1 | 1 | 1 | 1 | | | |

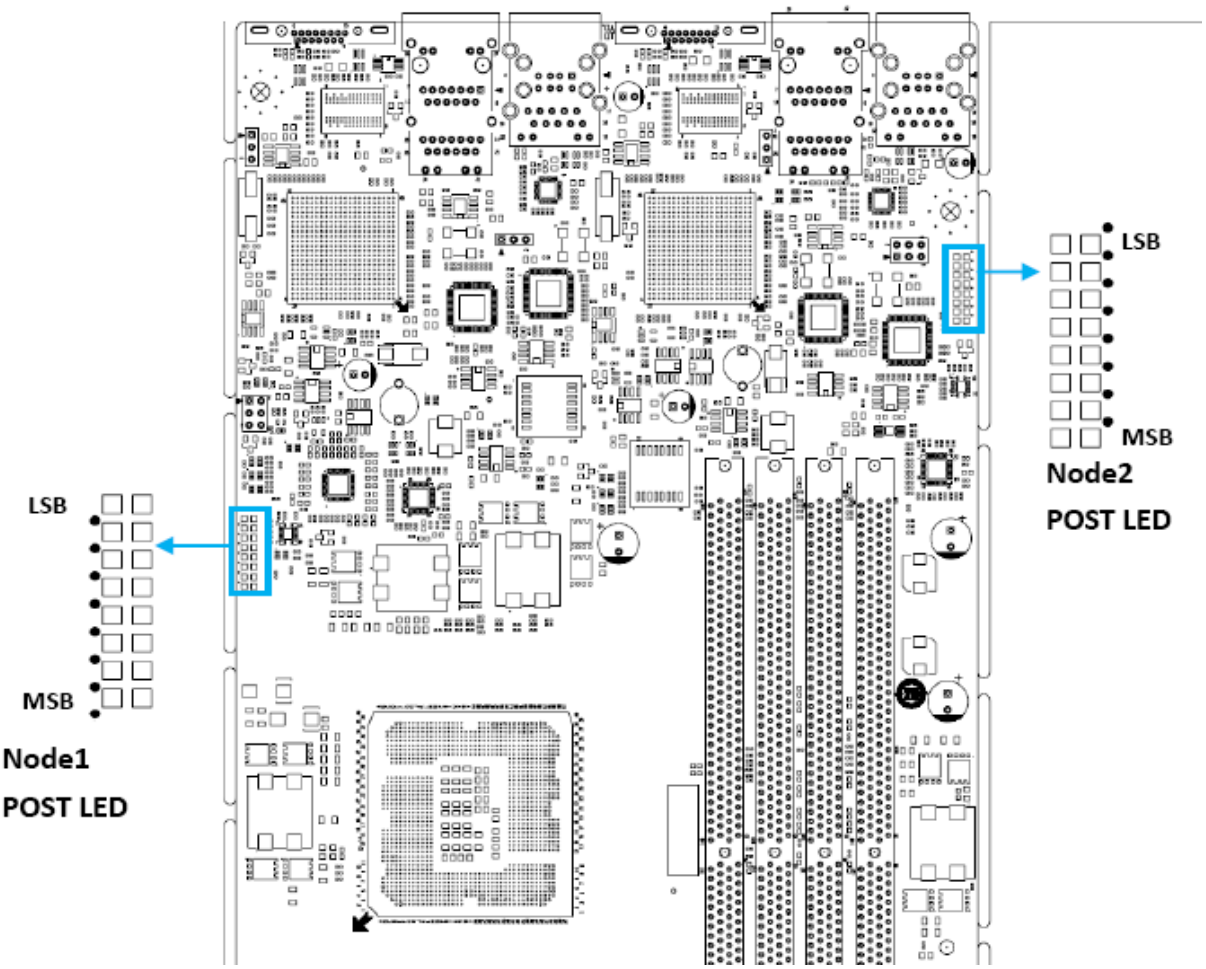


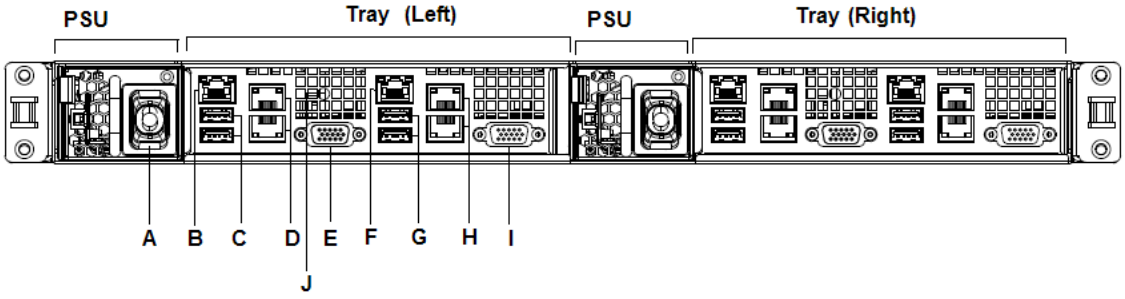

**Figure 35. Board diagnostic LED locations**

## 2.8 System IO feature

Intel® Server System SR1640TH has two identical trays in the chassis. Each tray contains one 2-node computing board S3420TH inside, powered by a single 450W power supply unit. The two trays have identical IO ports on front and rear panel.

The two trays are installed horizontally in the chassis, but they are not right-left swappable.

Below picture shows the IO ports on the rear panel. Only IO ports on left tray are presented. IO ports on right tray are identical to left ones.




| | | | |
|---|---|---|---|
| A | AC Power Receptacle | F | Node1: RMM3 Lite-V management port |
| B | Node 2: RMM3 Lite management port | G | Node 1: USB ports |
| C | Node 2: USB ports | H | Node 1: NIC1(lower) and NIC2(upper) connectors |
| D | Node 2: NIC1(lower) and NIC2(upper) connectors | I | Node 1: Video connector |
| E | Node 2: Video connector | J | Tray Identification LED |

**Figure 36. Back Panel Feature Overview (left tray)**

***Important Note:*** *The* ***Intel® Server System SR1640TH*** *requires the use of shielded LAN cable to comply with Emission/Immunity regulatory requirements. Use of non shield cables* ***may result in*** *product non-compliance.*

## 2.9 Rack and Cabinet Mounting Options

The Intel® Server System SR1640TH is designed to support 19 inches wide by up to 30 inches deep server cabinets. The system is shipped with customized fix mount kit to support installation in standard EIA-310-D racks.

# 3. Power Sub-System

The system includes two 450-W power supply units, which are 80 plus energy efficiency, demonstrating climate saver with silver rating.

## 3.1 Mechanism overview

The casing dimension is W 50.5 mm x L 300 mm x H 40.2 mm. This mechanism shall withstand the specified mechanical shock and vibration requirements.

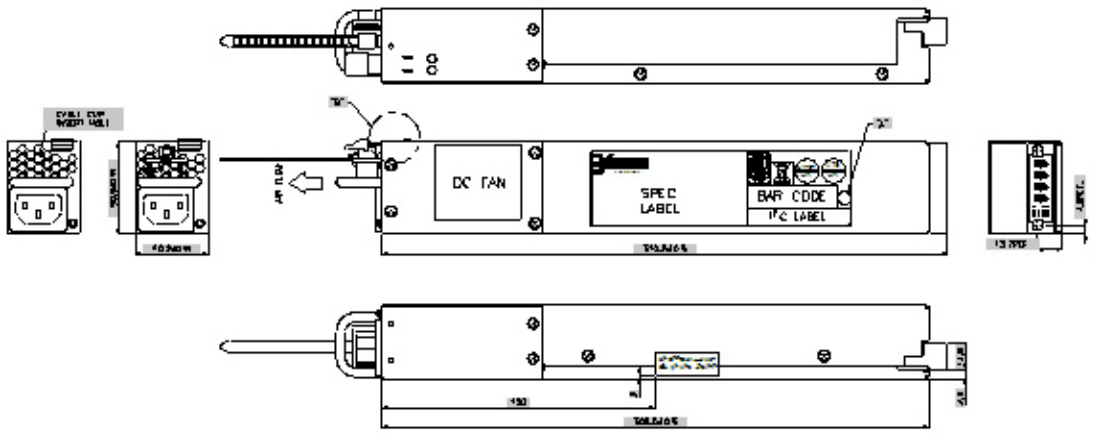
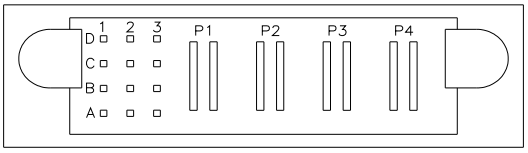



**Figure 37. Power Supply Mechanical Drawing**

## 3.2 Output connectors

The power supply unit provides a cable free with connectors to the system board each. You can find the connectors (explained in the following table), and connectors' pin definitions in the power supply specification. The DC output connector is compliant with FCI#51731-042LF or equivalent.

**Table 50. Output connector definition**




| SIGNAL PINS | | | | POWER BLADE | | | |
|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | P1 | P2 | P3 | P4 |
| D | A0 | PWOK | +5VSB | RTN | RTN | +12V | +12V |
| C | 12VLS | +15Vcc | +12VRS | | | | |
| B | PS−ON | SCL | B/P FAIL | | | | |
| A | PS−KILL/A1 | SDA | +5VSB | | | | |

CONNECTOR PIN−OUT

**Note:** Signals that can be defined as low true or high true use the following convention:

Signal# = low true.

**Table 51. Output signal definition**

| Signal | Description | Signal | Description |
|---|---|---|---|
| 12VLS | +12V load share bus | PWOK | Power OK output |
| 5 VSB | 5V standby output | +12 VRS | 12V remote sense |
| PSON# | Power enable input | PS-KILL#/A1 | Supply fast shutdown/I2C address bit1 |
| B/P FAIL | B/P fail input | SCL | I2C clock signal |
| A0 | I2C address bit 0 | SDA | I2C data signal |
| +15VCC | B/P VCC | | |

## 3.3 Efficiency

The Efficiency should meet at least Climate Saver 2 / 80Plus Silver rating, specified in below table. The efficiency should be measured at 230VAC and with external fan power source at specified loading, according to Climate Saver / 80Plus efficiency measurement specifications.

**Table 52. Power Supply Efficiency**

| Input | 20% of maximum | 50% of maximum | 100% of maximum |
|---|---|---|---|
| 230 VAC | >85% | >89% | >85% |

**Table 53. FAN power loss**

| **Input230VAC/LOAD** | 20% | 50% | 100% |
|---|---|---|---|
| **FAN (POWER LOSS)** | 2W | 5W | 10W |

The minimum efficiency at 100-264VAC for the Max load shall be at least 83%.

## 3.4 AC Input Voltage Specification

### 3.4.1 Input voltage and frequency

The power supply can auto-sense the input voltage, and operate in the range between 90VAC to 264VAC. It shall be capable of supplying the rated power as specified in Table 1 in the voltage range of 90VAC to 264VAC.

**Table 54. Rated output power for each input voltage range**

| Input voltage range | Nominal voltage | Max power |
|---|---|---|
| 90-132 VAC | 115 VAC | 450 Watts |
| 180-264 VAC | 230 VAC | 450 Watts |

The power supply shall operate at any input frequency between 47 Hz and 63 Hz.

### 3.4.2 Input current

The maximum input current shall be 15A for each input voltage range as in below table.

**Table 55. Maximum input current**

| Input voltage | Input current | Max power |
|---|---|---|
| 100-132 VAC | 8 A | 450 Watts |
| 180-264 VAC | 4 A | 450 Watts |

### 3.4.3 Input current harmonics

The input current drawn on the power line shall not exceed the limits set by IEC-61000-3-2 and JEIDA MIT1 standards.

### 3.4.4 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. Sag conditions are also commonly referred to as a “brown-out”. These conditions are defined as the AC line voltage dropping below nominal voltage conditions. Surge refers to conditions when the AC line voltage rises above nominal voltage.

The power supply meets the requirements under the following AC line sag and surge conditions.

**Table 56. AC Line Sag Transient Performance**

| AC Line Sag | | | | |
|---|---|---|---|---|
| Duration | Sag | Operating AC Voltage | Line Frequency | Performance Criteria |
| Continuous | 10% | Nominal AC Voltage ranges | 50/60 Hz | No loss of function or performance |
| 0 to 1 AC cycle | 100% | Nominal AC Voltage ranges | 60 Hz | Loss of function acceptable, self recoverable |
| > 1 AC cycle | >10% | Nominal AC Voltage ranges | 50/60 Hz | Loss of function acceptable, self recoverable |
| 0 to 1/2 AC cycle | 30% | Mid-point of Nominal AC Voltage | 50/60 Hz | Loss of function acceptable, self recoverable |

**Table 57. AC Line Surge Transient Performance**

| AC Line Surge | | | | |
|---|---|---|---|---|
| Duration | Surge | Operating AC Voltage | Line Frequency | Performance Criteria |
| Continuous | 10% | Nominal AC Voltages | 50/60 Hz | No loss of function or performance |
| 0 to ½ AC cycle | 30% | Mid-point of nominal AC Voltages | 50/60 Hz | No loss of function or performance |

### 3.4.5 Susceptibility Requirements

The power supply meets the following electrical immunity requirements:

**Table 58. Performance Criteria**

| Level | Description |
|---|---|
| A | The apparatus shall continue to operate as intended. No degradation of performance. |
| B | The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits. |
| C | Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls. |

#### 3.4.5.1 Electrostatic Discharge Susceptibility

The power supply complies with the limits defined in EN 55024: 1998 using the IEC 61000-4-2:1995 test standard and performance criteria B defined in Annex B of CISPR 24.Tested to meet the level 3 requirement.

#### 3.4.5.2 Fast Transient/Burst

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-5:1995 test standard and performance criteria B defined in Annex B of CISPR 24. Test to meet the level 3 requirement.

#### 3.4.5.3 Radiated Immunity

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-3:1995 test standard and performance criteria A defined in Annex B of CISPR 24.

#### 3.4.5.4 Surge Immunity

The power supply was tested with the system for immunity to AC Ringwave and AC Unidirectional wave, both up to 2kV, per EN 55024:1998, EN 61000-4-4, level 3:1995 and ANSI C62.45: 1992.

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-4:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

### 3.4.6 AC Line Fast Transient (EFT) Specification

The power supply meets the *EN61000-4-5* directive and any additional requirements in *IEC1000-4-5* and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
The surge-withstand test must not produce damage to the power supply.
The power supply shall meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

### 3.4.7 AC Line Dropout / Holdup

An AC line **dropout** is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout, the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits.

If the AC dropout lasts longer than the holdup time, the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration shall not cause damage to the power supply.

### 3.4.8 AC Line Leakage Current

The maximum leakage current to ground for each power supply is 3.5 mA when tested at 240 VAC 60 Hz.

### 3.4.9 Power Recovery

The power supply will recover automatically after an AC power failure. AC power failure is defined as any loss of AC power that exceeds the dropout criteria.

#### 3.4.9.1 Voltage Brown Out

The power supply should withstand a brownout and recover from it without any damage stated in below table.

| 0~115 VAC | Shutdown | Recover |
|---|---|---|
| Full Load | 75 VAC | 88 VAC |

#### 3.4.9.2 Voltage Interruptions

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

### 3.4.10 AC Line Inrush

The maximum ac line inrush current shall be 60A peak at an input voltage of 264VAC. Inrush current shall be measured at an ambient temperature of 25 deg C after the input voltage has been removed from the power supply for a minimum of 10 minutes.

### 3.4.11 AC Line Fuse

The power supply shall incorporate one input fuse on the line side for input over-current protection to prevent damage to the power supply and meet product safety requirements. Fuses should be slow blow type or equivalent to prevent nuisance trips. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

### 3.4.12 Power Factor Correction

The input power factor shall be greater than 0.98/115Vac and 0.94/230Vac over all input voltages at loads greater than 50% of the power supply's rated output.

## 3.5 DC output voltage specification

### 3.5.1 Output Rating

Each DC output shall be capable of supplying the output current shown in below table:

**Table 59. DC output rating**

| Output | MIN | MAX |
|---|---|---|
| + 5VSB | 0 A | 3 A |

| Output | MIN | MAX |
|---|---|---|
| +12V | 2 A | 37 A |

### 3.5.2 Remote Sensing (+12VRS)

The power supply system output shall have remote sense (12VRS) to compensate for drops in the system for the +12V output. The remote sense input impedance to the power supply shall be greater than 200 ohms on +12VRS. Remote sense shall be able to compensate for a minimum of 400mV drop on the +12V output. The current in any remote sense line shall be less than 5mA to minimum voltage sensing errors.

### 3.5.3 No load operation

The power supply shall meet all requirements except for the transient loading requirements when operated at no load on all outputs.

### 3.5.4 Regulation, ripple and noise

The power supply shall meet the regulation, ripple and noise limit under all operating conditions (AC line, transient loading and output loading). The regulation shall be measured at the output connector of the power supply, subject to the cross loading conditions in the following table.

**Table 60. Output voltage regulation**

| | Output voltage limits (Vdc) | | | |
|---|---|---|---|---|
| Output | Minimum | Nominal | Maximum | REG |
| +12V | 11.64V | 12V | 12.36V | +/-3% |
| +5VSB | 4.75V | 5V | 5.25V | +/-5% |

### 3.5.5 Ripple and noise

Ripple and noise are measured with 0.1uF of ceramic capacitance and 10uF of tantalum capacitance on each of the power supply output connector terminal. The ripple and noise shall be met over all load ranges and AC line voltages. The output noise requirements shall apply over a 0 Hz to 20 MHz bandwidth.

**Table 61. Ripple and noise**

| Output | +12V | 5VSB |
|---|---|---|
| Maximum ripple/nose | 150mVp-p | 50mVp-p |

### 3.5.6 Transient loading

The power supply shall operate within specified limits and meet regulation requirements over the following transient loading conditions anywhere within the specified load range of the power supply. This shall be tested with no additional bulk capacitance added to the load.

**Table 62. Transient loading**

| Output | Step size | Slew rate | Capacitive Load |
|---|---|---|---|
| +12V | 60% OF MAX. | 0.5A/usec | 2200uF |
| +5VSB | 25% OF MAX. | 0.5A/usec | 1uF |

**Note**: While testing the transient loading, the 12V limit is ±5%

### 3.5.7 Capacitive load

The power supply shall operate within specifications over the capacitive load range defined.

**Table 63. Capacitive load**

| Output | Min | Max |
|---|---|---|
| +12V | 10uF | 11,000uF |
| +5VSB | 1uF | 350uF |

### 3.5.8 Maximum load change

The power supply shall continue to operate normally when there is a step change 1 A/uS between minimum load and maximum load.

### 3.5.9 Output voltage rise time

The turn on waveform for the +12V output shall be monotonic with less then 5% of overshoot. The rise time from 10% (1.2V) to 90% (10.8V) shall be less then 50msec for a single power supply.

### 3.5.10 Output voltage hold-up time

Upon loss of input voltage (at nominal), the output voltages shall remain in regulation for at least 16msec.

### 3.5.11 Overshoot

Any output overshoot at turn on shall be less than 10% of the nominal output value. Any overshoot shall recover to within the specified regulation in less than 0.5mS.

### 3.5.12 Temperature coefficient

After operating for 30 minutes or longer at 25° C ambient, the output voltages shall not change by more than 0.05 % per degree C for any given line and load conditions.

## 3.6 Protection Circuits

The 5VSB output shall remain on if the failure does not involve this output. When a protection circuit shuts down a power supply all the LED show a failed status and shall be active, if the power supply latches off due to a protection circuit tripping. An AC cycle off for 15 sec and PSON cycle high for 1 sec shall reset the power supply. Else the Power should auto-recover, when the fail had been cleared or the power supply is within specifications again.

### 3.6.1 Over-Current/short circuit Protection (OCP)

The power supply shall have current limit to prevent the+12Voutput from exceeding the value shown in Table 10. The current limiting shall be of the constant current type for the +12V.
The power supply shall latch off. The latch will be cleared by togging the PSON# signal or by an AC power interruption. The power supply shall not be damaged power cycling in this condition.

**Table 64. Over-current Protection (OCP)**

| Voltage | Over current limit |
|---|---|
| +12 V | 110% min; 150% max |

### 3.6.2 Over-voltage Protection (OVP)

An over voltage condition shall be measured on the +12V output of the power supply DC connector. The power supply must shutdown and latch off when the +12V reaches the voltage shown in below table. The latch can be cleared by togging the PSON# signal or by an AC cycle off.

**Table 65. +12V Over-Voltage Protection (OVP) requirement**

| Output Voltage | MIN | MAX |
|---|---|---|
| +12V | +13.3V | +14.5V |

### 3.6.3 Over-temperature Protection (OTP)

The power supply shall be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an over temperature condition the PSU shall be shutdown with the exception of the 5VSB output. The power supply shall alert the system of the OTP condition via the power supply the fail LED indicator. The power supply will auto recover from this condition, when the temperature is within specification again. In case of a fan fail, the power supply will latch off.

Warning: 80° C (±6°)

Critical shut down: 90° C (±6°)

Re-start PSU: 75° C (±6°)

### 3.6.4 Thermal Fan Speed Control (External Control)

The power supply Fan shall be external control able through a HW pin on the connector. This function allows overwriting the MCU Fan control due to thermal stress at the PDB. In normal operation, the MCU controls the fan depending on Loading and internal temperature. The Pin B3 (B/P-Fail) controls the internal Fan duty depending on voltage level recognized, corresponding to below table.

**Table 66. Fan control**

| Voltage @ Pin B3 | Fan Duty |
|---|---|
| ≤1.25V | MCU controlled |
| 1.25V | 50% |
| 1.50V | 60% |
| 1.75V | 70% |
| 2.00V | 80% |
| 2.50V | 100% |

## 3.7 SMBus communication

The serial bus communication devices for MC and FRU data in the power supply shall be compatible with both SMBus 2.0 “high power” and I2C Vdd based power and drive. This bus shall operate at 5V. The SMBus pull-ups are located on the motherboard and shall be connected to 5V.

Two pins are allocated on the power supply. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Both pins are bi-directional and are used to form a serial bus. The device(s) in the power supply shall be located at an address(s) determined by addressing pins A0 and A1 on the power supply module. The circuits inside the power supply shall derive their 5V power from the 5Vsb bus through a buffer. Device(s) shall be powered from the system side of the 5VSB or’ing device. No pull-up resistors shall be on SCL or SDA inside the power supply. The pull-up resistors should be located external to the power supply on system/application side.

### 3.7.1 Power supply management controller (PSMC)

The PSMC device in the power supply shall derive its power of the 5Vsb output on the system side of the O'ring device and shall be grounded to return.

It shall be located at the address set by the A0 and A1 pins.

Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details on the power supply monitoring interface requirements and refer to followed section of supported features. The below table reflect the power module addresses complying with the position in the housing.

| PDB position and power module address | PM1/B0h | PM2/B2h | PM3/B4h | PM4/B6h |
|---|---|---|---|---|
| Pin A0 | 0 | 1 | 0 | 1 |
| Pin A1 | 0 | 0 | 1 | 1 |

### 3.7.2 Power supply field replacement unit (FRU) signals

The power supply shall support electronic access of FRU information over an $I^2C$ bus. Four pins at the power supply connector are allocated for this. They are named SCL, SDA, A0, A1. SCL is serial clock. SDA is serial data. These two bidirectional signals forms the basic communication lines over the $I^2C$ bus. A0, A1 are input address lines to the power supply. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting $I^2C$ address shall be per the table below.

The device used for this shall be powered from a 5V bias voltage derived from the +5 VSB output . No pull-up resistors shall be on SCL or SDA inside the power supply.

FRU data shall be stored starting in address location 8000h through 80FFh(ref). The FRU data format shall be compliant with the IPMI specifications. The current versions of these specifications are available at: http://developer.intel.com/design/servers/ipmi/spec.htm

### 3.7.3 Power Supply Status LED indicators

There will be a bi-color LED to indicate power supply status as shown below;

**Table 67. Power supply status**

| Power supply condition | Power supply LED |
|---|---|
| No AC power to PSU | OFF |
| AC present/only standby output on | Flashing GREEN |
| Power supply DC output ON and OK | GREEN |
| Power supply failure | RED |
| Power supply warning | Flashing RED/GREEN |

## 3.8 PSMC and PMBus compliance

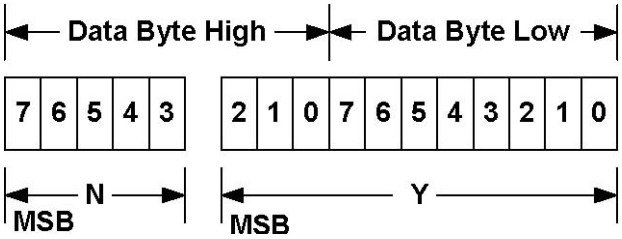
The PSMC monitoring and control function set shall comply to the PMBus Spec. Rev. 1.1 and above, which can be downloaded from the www.pmbus.org.

### 3.8.1 Hardware

The device in the power supply is compatible with both the SMBus 2.0 "high power" specification for $I^2C$ Vdd based power and drive (for Vdd = 3.3V). This bus operates at 3.3 V but is tolerant of 5 V signaling. It also operates at full 100 kbps SMBus speed without using clock stretching to slow down the bus.

### 3.8.2 Data Format

The data format for current, voltage, power, temperature, and fan speed are using the PMBus Literal format.




Literal data format: $X = Y \cdot 2^N$
X = the sensor value in volts, amps, watts, degrees C, or RPM
Y = mantissa. The mantissa is the variable components that changes as the sensor value changes. Y is a 16-bit unsigned value for the READ_VOUT command. For all other READ commands, Y is an 11-bit signed 2's compliment value. N = exponent. The exponents are fixed for each power supply and define the resolution for each sensor.

### 3.8.3 Function commands supported

The following PMBus commands are supported for the purpose of monitoring currents, voltages, power and status:

| | |
|---|---|
| MFR_ID | READ_IOUT |
| MFR_MODEL | READ_VOUT |
| MFR_IOUT_MAX | STATUS_CML |
| PMBUS_REVISION | STATUS_TEMPERATURE |
| READ_POUT | STATUS_FANS_1_2 |
| READ_PIN | STATUS_INPUT |
| READ_FAN_SPEED_n | MFR_REVISION |
| STAUTS_IOUT | CAPABLITY |
| STAUTS_VOUT | CLEAR_FAULTS |
| STATUS_WORD | ON_OFF_CONFIG |
| STATUS_BYTE | OPERATION |
| QUERY | PAGE |
| MFR_SERIAL | MFR_POUT_MA |

## 3.9 FRU data format

The information to be contained in the FRU device is shown in the following table

**Table 68. FRU device information**

| Area type | Description |
|---|---|
| Common header | As defined by the FRU document |
| Internal use area | Not required, do not reserve |
| Chassis info area | Not required, do not reserve |
| Board info area | Not required, do not reserve |

### 3.9.1 Product info area

Implement as defined by the IPMI FRU document. Product information shall be defined as follows:

**Table 69. Product Information**

| Field name | Field description |
|---|---|
| Manufacturer name | 3Y POWER |
| Product name | YM-2451C |
| Product part/model number | SUNNY451AMP200Rxx |
| Product version | A |
| Product serial number | 18 digit serial number |
| Asset tag | Not used, code is zero length byte |
| FRU file ID | Not required |
| PAD bytes | Added as necessary to allow for 8-byte offset to next area |

### 3.9.2 Multi-record area

Implement as defined by the IPMI FRU document. The following record types shall be used on this power supply:

Power supply information (Record type 0x00)

DC output (Record type 0x01)

No other record types are required for the power supply

## 3.10 AC Inlet Connector

The AC input connector is an *IEC 320 C-14* power inlet. This inlet is rated for 15 A / 250 VAC.

## 3.11 AC Power Cord Specification Requirements

The AC power cord used must meet the following specification requirements:

| | |
|---|---|
| Cable Type | SJT |
| Wire Size | 16 AWG |
| Temperature Rating | 105º C |
| Amperage Rating | 13A |
| Voltage Rating | 125V |

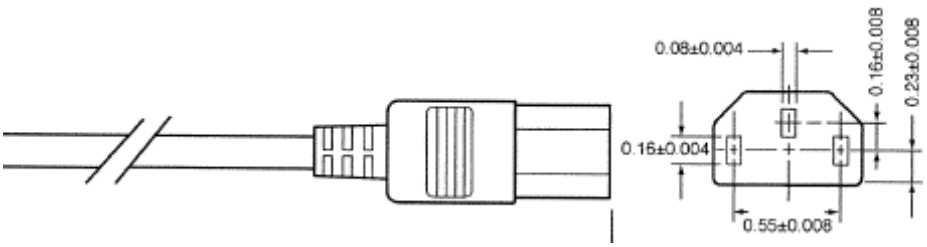



**Figure 38. AC Power Cord Specification Requirements**

# 4. Cooling Sub-System

Several components and configuration requirements make up the cooling sub-system of the chassis. These include processors, chipsets, VR heatsinks, system fan module, power supply fans, CPU air duct, and drive bay population. All are necessary to provide and regulate the air flow and air pressure needed to maintain the system's thermals when operating at or below the maximum specified thermal limits.

In order to maintain the necessary airflow within the system, you must properly install the air duct in each tray.

The chassis uses a variable fan speed control engine to provide adequate cooling for the system at various ambient temperature conditions, under various server workloads, and with the least amount of acoustic noise possible. The fans operate at the lowest speed for any given condition to minimize acoustics.

**Note:** The server system does not support redundant cooling fans. If any of the fans fail, you must power down the system as soon as possible to replace the fan.

## 4.1 CPU Heatsink

Four heatsinks are included in the system package. These heatsinks are designed for optimal cooling and performance. Each processor is cooled by a passive heatsink. To achieve better cooling performance, you must properly attach the heatsink bottom base with TIM (thermal interface material). ShinEtsu* G-751 or 7783D or Honeywell* PCM45F TIM is recommended. The mechanical performance of the heatsink must satisfy mechanical requirement of Intel® Xeon® processors. To keep chipsets and VR temperature at or below maximum temperature limit, the heatsink is required if necessary.

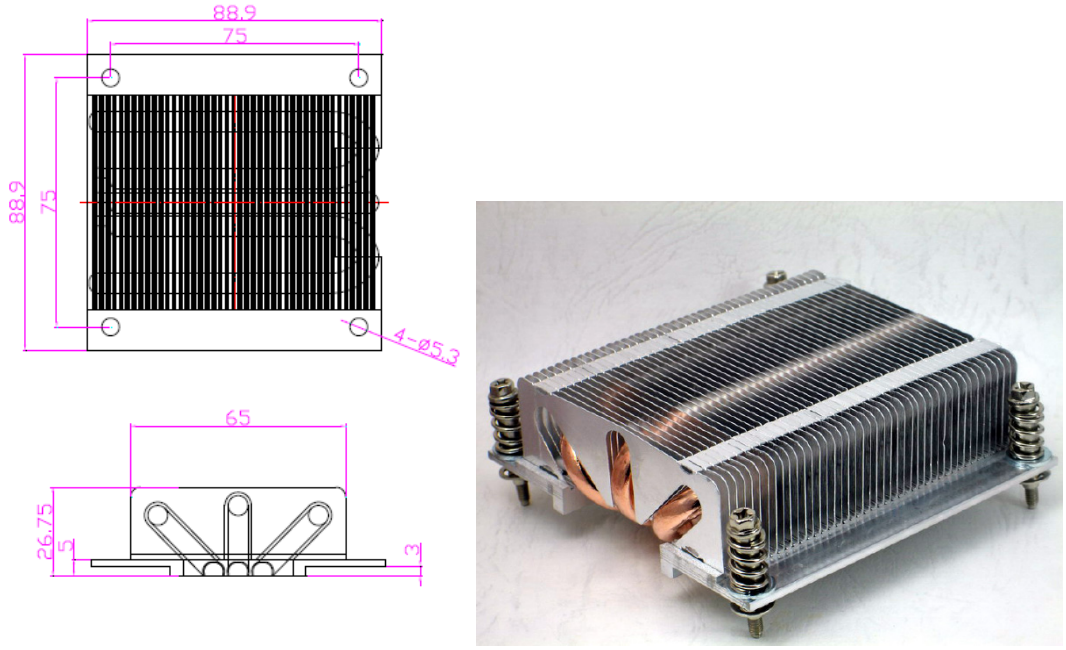



**Figure 39. CPU Heatsink Overview**

**Note:** The passive heatsink is the third part thermal solution for 1U rack chassis.

## 4.2 Three-Fan Module

The system tray includes a fan assembly consisting of three managed 40x40x48 mm dual-rotor, multi-speed fans. Three fans are using the same 8-pin fan connectors.

They provide the primary cooling for the processors, memory, and the hard drive bays on the front panel. Each fan is designed for tool-less insertion to or removal from the fan module housing.

The system fan module is designed for ease of use and supports several management features that the server board management system can use.

**Note:** The fans are NOT hot-swappable. You must turn off the system to replace a failed fan.

Each fan within the module is capable of supporting multiple speeds. Fan speed changes automatically when internal ambient temperature of the system or processor temperature changes. The fan speed control algorithm is programmed into the server board's BIOS.

Each fan connector within the module supplies a tachometer signal that allows the BMC to monitor the status of each fan. If one of the fans should fail, the system fault LED on front panel will light.

**Note:** There is a spare fan kit that contains six system cooling fans.

The fan connector pin-out definition is in chapter 2.7.1.7.

## 4.3 Power Supply Fan

Each power supply module supports one non-redundant 40 mm fan. The fans control the cooling of the power supply and some drive bays. These fans are not replaceable. Therefore, if a power supply fan fails, you must replace the whole power supply unit.

## 4.4 Air Duct Module

Each tray in the chassis requires the use of an air duct module to direct airflow over critical areas within the system. The following provides a summary and description of Air Duct Module.

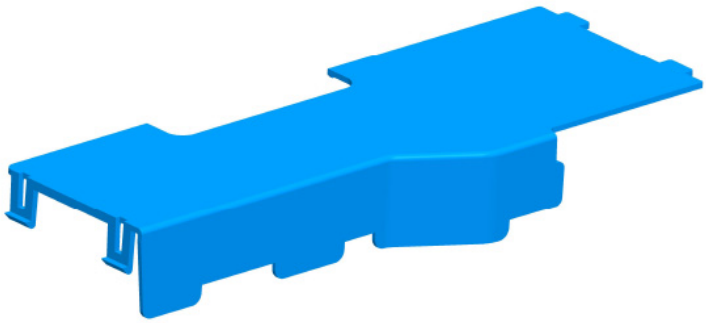


**Figure 40. Air Duct Module**

The figure below provides a description for Air Duct module assembling position.

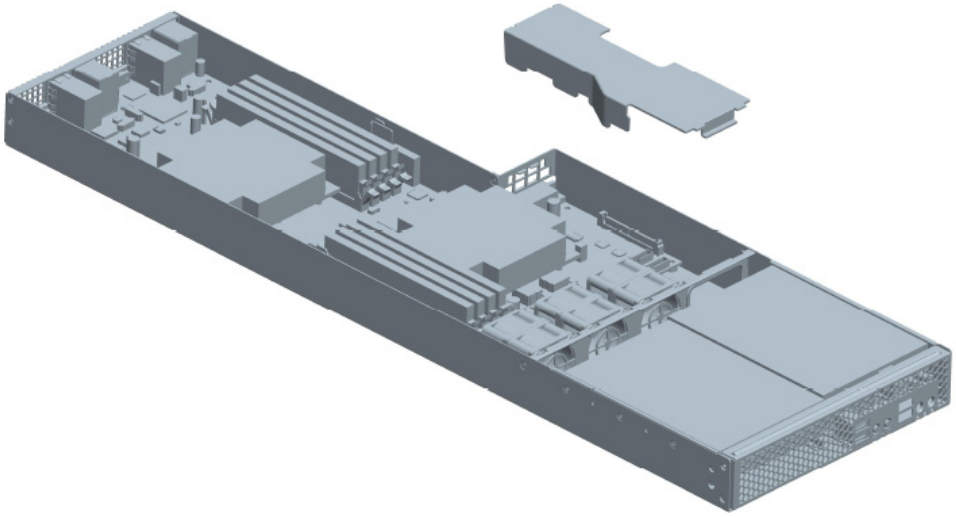


**Figure 41. Air Duct Module assembly process**

# 5. Hard Disk Drive Support

The server system provides four hard drive bays, each tray has two hard drive bays. Each hard drive bay can support one fix 3.5-inch SATA/SAS HDD.

## 5.1 Hard Disk Drive Bays

Each tray in the server system 1U chassis can support up to two carrier-mounted fix SATA or SAS 3.5-inch hard disk drives. The drives cannot be “electrically” hot-swapped while the system power is applied.

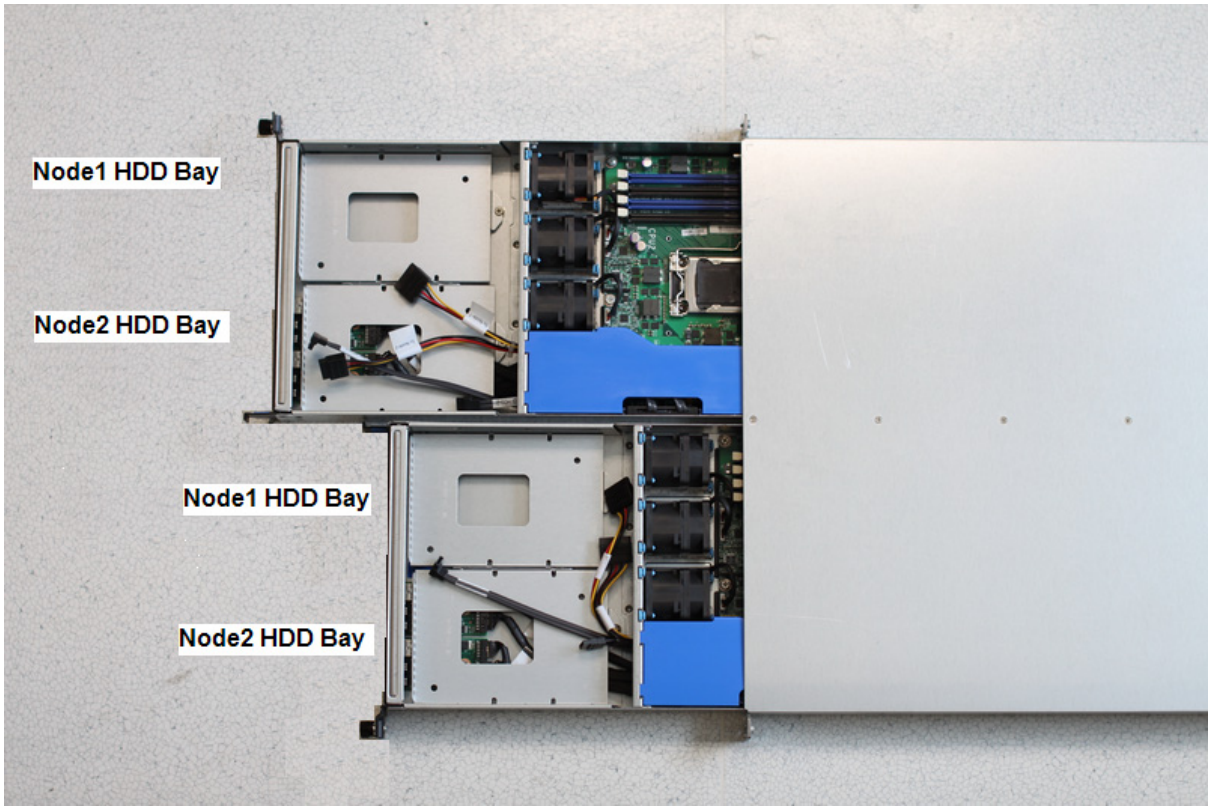



**Figure 42. HDD Bays in 2 trays**

If a failed drive needs replacing, it is recommended to power off the correspondent tray and replaces the failed hard drive.

## 5.2 Hard Drive Carrier

You can use hard drive carrier for 3.5-inch hard drive installation.

The hard drive carrier is fixed in the chassis tray. You have to remove it from tray to install the hard drive. To install the hard drive with carrier, see below illustration:

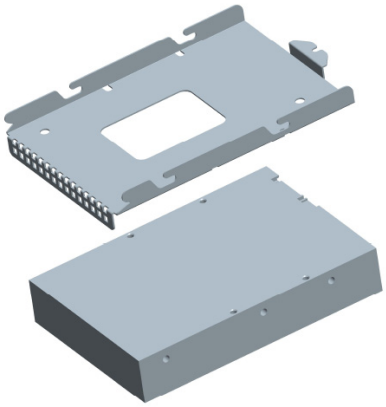


**Figure 43. 3.5-inch HDD Assembly Overview**

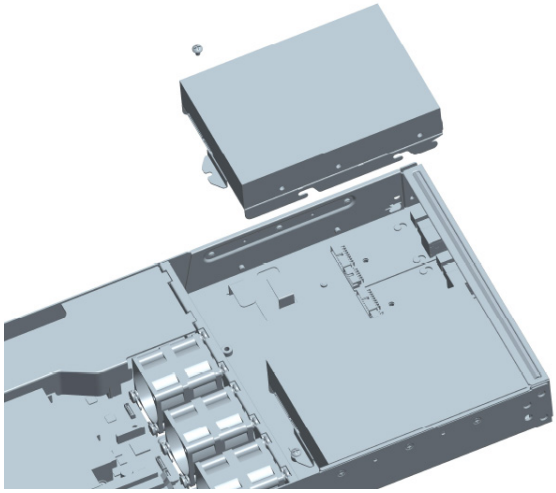
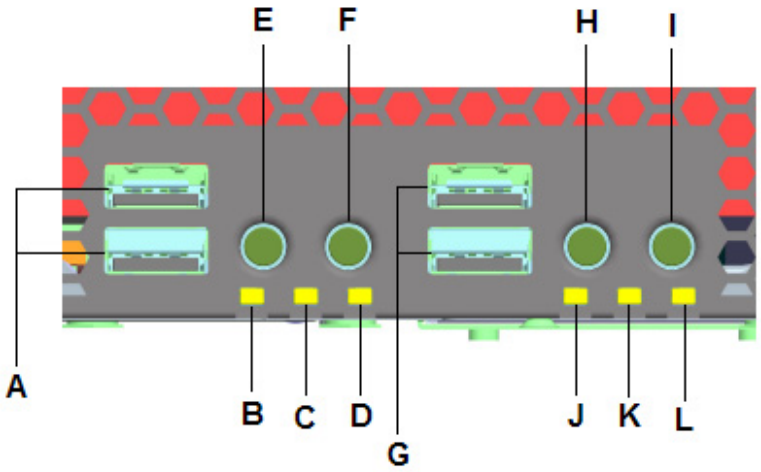


**Figure 44. Install HDD assembly into tray**

# 6. Front Panel Control and Indicators

The Intel® Server System SR1640TH Front Control Panel integrates control buttons, LEDs, and USB ports. The control panel assembly is pre-assembled and fixed to the chassis.




| | Node 1 | Node 2 |
|---|---|---|
| Power Button/Power LED | E | H |
| System ID Button/ID LED | F | I |
| Node USB ports | A | G |
| LAN 1 Activity LED | B | J |
| LAN 2 Activity LED | C | K |
| Node status LED | D | L |

**Figure 45. Front Control Panel**

## 6.1 Control Panel Button

The following table lists the control panel features and functions. The control panels features a system power button.

**Table 70. Front Control Button Function**

| Feature | Function |
|---|---|
| Power/Sleep Button | Toggles the system power on/off. This button also functions as a Sleep Button if enabled by an ACPI-compliant operating system. |
| System ID Button | Turn On/turn off ID LED |

## 6.2 Control Panel LED Indicators

The control panel houses five LEDs, which are viewable to display the system's operating status.

The following table identifies each LED and describes their functionality.

**Table 71. Front LED Indicator Functions**

| LED Indicator | Color | Condition | What it describes |
|---|---|---|---|
| Power | Green | On | Power On |
| | Green | Blink | Sleep (S1) |
| | - | Off | Power Off (also S4) |
| LAN 1 & LAN 2 | Green | On | LAN Link no Access |
| | Green | Blink | LAN Access |
| | - | Off | Idle |
| System ID | Blue | On | Unit Selected For Identification |
| | - | Off | No Identification |
| System Status | Green | On | System Ready / No Alarm |
| | Green | Blink | System ready, but degraded: redundancy lost such as PS or fan failure; non-critical temp/voltage threshold; battery failure; or predictive PS failure. |
| | Amber | On | Critical Alarm: Critical Power Modules Failure, Critical t FANs Failure, Voltage (Power Supply), critical Temperature and Voltage |
| | Amber | Blink | Non- Critical Alarm: redundant FAN Failure, redundant Power Module Failure, non-critical Temperature and voltage |
| | - | Off | AC power off: System unplugged AC power on: System powered off and in standby, no prior degraded\non-critical\critical state |

### 6.2.1 Power / Sleep LED

**Table 72. SSI Power LED Operation**

| State | Power Mode | LED | Description |
|---|---|---|---|
| Power Off | Non-ACPI | Off | System power is off and the BIOS has not initialized the chipset. |
| Power On | Non-ACPI | Solid On | System power is on but the BIOS has not yet initialized the chipset. |
| S5 | ACPI | Off | Mechanical is off and the operating system has not saved any context to the hard disk. |
| S1 Sleep | ACPI | Blink | DC power is still on. The operating system has saved context and gone into a level of low-power state. |
| S0 | ACPI | Solid On | System and the operating system are up and running. |

**Note**: Blink rate is approximately 1Hz at 50% duty cycle.

### 6.2.2 System Status LED

**Table 73. System Status LED Operation**

| Color | State | Criticality | Description |
|---|---|---|---|
| Off | N/A | Not ready | AC power off or BMC initialization completes if no degraded, non-critical, critical, or non-recoverable conditions exist after AC plug in |
| Amber | Solid On | Not ready | Pre DC Power On – 15-20 second BMC Initialization when AC is applied to the server. The system will not POST until BMC initialization completes. |
| Green | Solid on | Ok | System ready |
| Green | Blink | Degraded | BIOS detected<br>1. Unable to use all of the installed memory (more than one DIMM installed).[1]<br>2. In a mirrored configuration, when memory mirroring takes place and system loses memory redundancy. This is not covered by (2). [1] |

| Color | State | Criticality | Description |
|---|---|---|---|
| | | | 3. PCI Express* correctable link errors.<br>Integrated BMC detected<br>1. Redundancy loss such as a power supply or fan. Applies only if the associated platform subsystem has redundancy capabilities.<br>2. CPU disabled – if there are two CPUs and one CPU is disabled.<br>3. Fan alarm – Fan failure. Number of operational fans should be more than minimum number needed to cool the system.<br>4. Non-critical threshold crossed – Temperature, voltage, power nozzle, power gauge, and PROCHOT2 (Therm Ctrl) sensors.<br>5. Battery failure.<br>6. Predictive failure when the system has redundant power supplies. |
| Amber | Blink | Non-critical | Non-fatal alarm – system is likely to fail<br>**BIOS Detected**<br>1. In non-mirroring mode, if the threshold of ten correctable errors is crossed within the window.[1]<br>2. PCI Express* uncorrectable link errors.<br>**Integrated BMC Detected**<br>1. Critical threshold crossed – Voltage, temperature, power nozzle, power gauge, and PROCHOT (Therm Ctrl) sensors.<br>2. VRD Hot asserted.<br>3. Minimum number of fans to cool the system are not present or have failed. |
| Amber | Solid on | Critical, non-recoverable | Fatal alarm – system has failed or shutdown<br>**BIOS Detected**<br>1. DIMM failure when there is one DIMM present and no good memory is present.[1]<br>2. Run-time memory uncorrectable error in non-redundant mode.[1]<br>3. CPU configuration error (for instance, processor stepping mismatch).<br>**Integrated BMC Detected**<br>1. CPU CATERR signal asserted.<br>2. CPU 1 is missing.<br>3. CPU THERMTRIP.<br>4. No power good – power fault.<br>Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies are present). |

**Notes:**

1. The BIOS detects these conditions and sends a *Set Fault Indication* command to the Integrated BMC to provide the contribution to the system status LED

2. Blink rate is ~ 1Hz at 50% duty cycle.

#### 6.2.2.1 System Status LED – BMC Initialization

When AC power is first applied to the system and 5V-STBY is present, the BMC controller on the server board requires 15-20 seconds to initialize. During this time, the system status LED will be solid on, both amber and green. Once BMC initialization has completed, the status LED will stay green solid on. If power button is pressed before BMC initialization completes, the system will not boot to POST.

### 6.2.3 System Identification LED

The system ID LED provides a visual indication of a system being serviced. The state of the system ID LED is affected by the following:

- Toggled by the system ID button

- Controlled by *the Chassis Identify command* (IPMI)
- Controlled by *the Chassis Identify LED command* (OEM)

**Table 74. System ID LED Indicator States**

| State | LED State |
|---|---|
| Identify active via button | Solid on |
| Identify active via command | ~1 Hz blink |
| Off | Off |

There is no precedence or lock-out mechanism for the control sources. When a new request arrives, all previous requests are terminated. For example, if the system ID LED is blinking and the system ID button is pressed, then the system ID LED changes to solid on. If the button is pressed again with no intervening commands, the system ID LED turns off.

# 7. Configuration Jumpers

The following chapter provides a summary and description of configuration, test, and debug jumpers on the server board S3420TH, which is used in Intel® Server System SR1640TH.

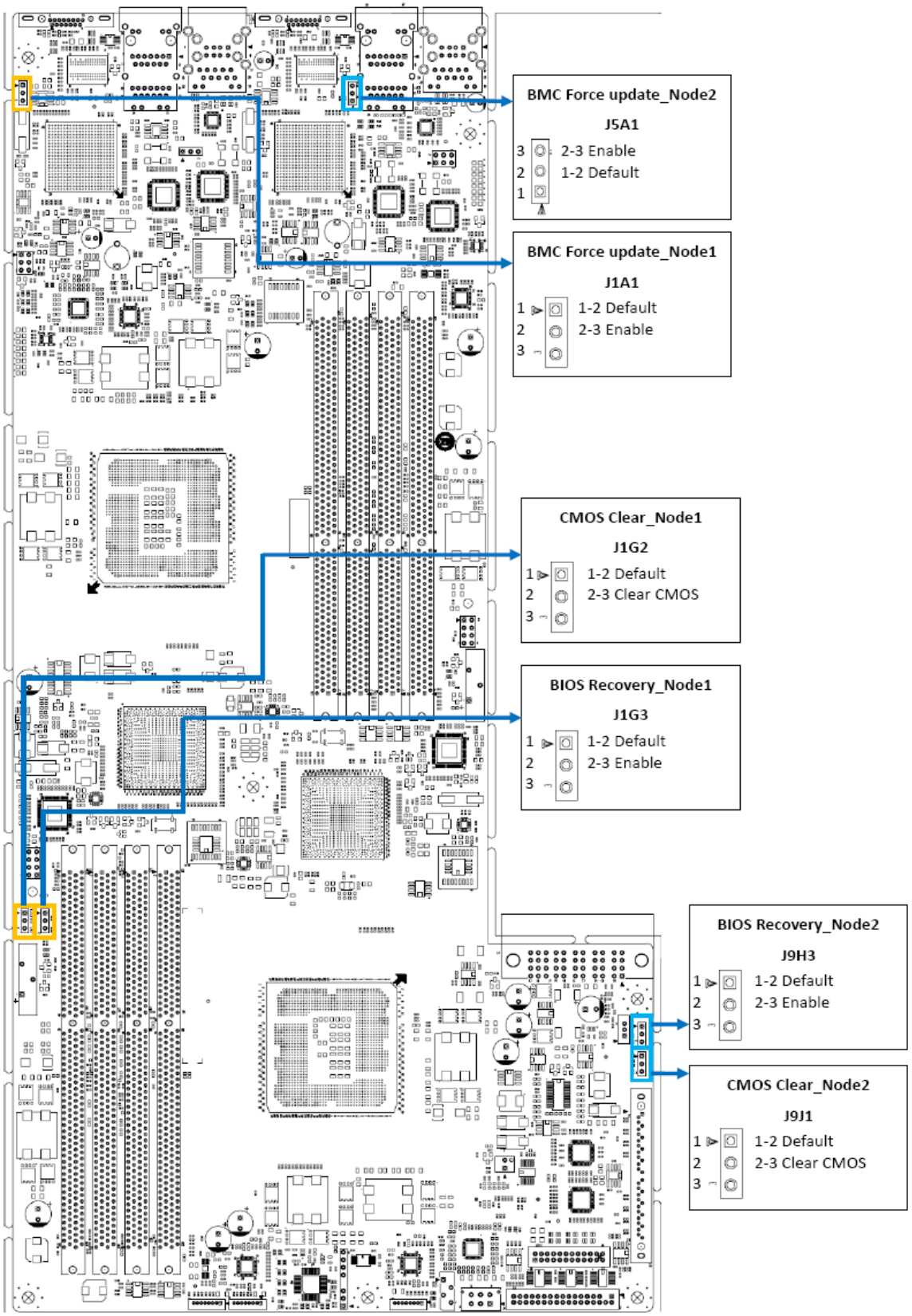



**Figure 46. Jumper location on Server Board S3420TH**

## 7.1 Force IBMC Update (J1A1, J5A1)

When performing a standard BMC firmware update procedure, the update utility places the BMC into an update mode, allowing the firmware to load safely onto the flash device. In the unlikely event the BMC firmware update process fails due to the BMC not being in the proper update state, the server board provides a BMC Force Update jumper (J1A1 for node 1, J5A1 for node 2) that forces the BMC into the proper update state. You must complete the following procedure in the event the standard BMC firmware update process fails.

**Table 75. Force IBMC Update Jumper**

| Jumper Position | Mode of Operation | Note |
|---|---|---|
| 1-2 | Normal | |
| 2-3 | Update | |

1. Power down and remove the AC power cord.
2. Open the server chassis. Refer to your server chassis documentation for instructions.
3. Move the jumper from the default operating position, covering pins 1 and 2, to the enabled position, covering pins 2 and 3.
4. Close the server chassis.
5. Reconnect the AC cord and power up the server.
6. Perform the BMC firmware update procedure as documented in the README.TXT file included in the given BMC firmware update package. After the successful completion of the firmware update process, the firmware update utility may generate an error stating the BMC is still in update mode.
7. Power down and remove the AC power cord.
8. Open the server chassis.
9. Move the jumper from the enabled position, covering pins 2 and 3 to the disabled position, covering pins 1 and 2.
10. Close the server chassis.
11. Reconnect the AC cord and power up the server.

**Note:** Normal BMC functionality is disabled when the Force BMC Update jumper is set to the enabled position. You should never run the server with the BMC Force Update jumper set in this position. You should only use this jumper setting when the standard firmware update process fails. This jumper should remain in the default / disabled position when the server is running normally.

## 7.2 BIOS Recovery Mode (J1G3, J9H3)

BIOS recovery jumper is used to repair the system BIOS from flash corruption in the main BIOS and Boot Block. This 3-pin jumper is used to reload the BIOS when the image is suspected to be corrupted. For instructions on how to recover the BIOS, refer to the specific BIOS release notes.

**Table 76. BIOS Recovery Mode Jumper**

| Jumper Position | Mode of Operation | Note |
|---|---|---|
| 1-2 | Normal | |
| 2-3 | Recovery | |

## 7.3 Clearing the CMOS (J1G2, J9J1)

This jumper is used to clean the current BIOS settings and reset to factory default.

**Table 77. Clear CMOS Jumper**

| Jumper Position | Mode of Operation | Note |
|---|---|---|
| 1-2 | Normal | |
| 2-3 | Reset BIOS Configuration | |

## Steps for clearing the CMOS

1. Power down server.
2. Pull out the tray and PSU.
3. Connect tray and PSU outside chassis. Plug in the power cord to PSU.
4. Move the jumper (J1B4) from the default operating position, covering pins 1 and 2, to the reset / clear position, covering pins 2 and 3.
5. Wait five seconds.
6. Remove AC power.
7. Move the jumper back to default position, covering pins 1 and 2.
8. Close the server chassis.
9. Power up the server.

The CMOS settings are now cleared.

**Note:** Removing AC Power before performing the CMOS Clear operation causes the system to automatically power up and immediately power down, after the procedure is followed and AC power is re-applied. If this happens, remove the AC power cord again, wait 30 seconds, and re-install the AC power cord. Power up system and proceed to the <F2> BIOS Setup Utility to reset the preferred settings.

# 8. Environmental and Regulatory Specifications

## 8.1 System Level Environmental Limits

The following table defines the system level operating and non-operating environmental limits.

**Table 78. System Office Environmental Summary**

| Parameter | Limits |
|---|---|
| Operating Temperature | +10 C to +35 C with the maximum rate of change not to exceed 10 C per hour |
| Non-Operating Temperature | -40 C to +70 C |
| Non-Operating Humidity | 50%- 90%, non-condensing with a maximum wet bulb of 28 C |
| Acoustic noise | Sound Pressure: 55 dBA (Rackmount) in an idle state at typical office ambient temperature. (23 C +/- 2 C) Sound Power: 7.0 BA in an idle state at typical office ambient temperature. (23 +/- 2 degrees C) |
| Shock, operating | Half sine, 2 g peak, 11 mSec |
| Shock, unpackaged | Trapezoidal, 25 g, velocity change 136 inches/sec (□40 lbs to > 80 lbs) |
| Shock, packaged | Non-palletized free fall in height 24 inches (□40 lbs to > 80 lbs) |
| Vibration, unpackaged | 5 Hz to 500 Hz, 2.20 g RMS random |
| Shock, operating | Half sine, 2 g peak, 11 mSec |
| ESD | +/-15kV except I/O port +/-8KV per Intel® Environmental test specification |
| System Cooling Requirement in BTU/Hr | 2050 BTU/hour |
| EMI operating | Required to meet EMI emission requirements, tested as part of system |

## 8.2 Serviceability and Availability

The system is designed to be serviced by qualified technical personnel only.

The desired Mean Time To Repair (MTTR) the system is 15 minutes, which includes diagnosing the system's problem. To meet this goal, the system enclosure and hardware was designed to minimize the MTTR.

The following are the maximum times a trained field service technician should take to perform the listed system maintenance procedures after diagnosing the system and identifying the failed component(s).

| Activity | Time Estimate |
|---|---|
| Plug out the tray | 10 sec |
| Remove and replace hard disk drive | 1 min |
| Remove and replace power supply module | 30 sec |
| Remove and replace system fan(each) | 1 min |
| Remove and replace server board(include cable routing) | 10 min |

## 8.3 Replacing the Back up Battery

The lithium battery on the server board powers the real time clock (RTC) for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

**WARNING**

**Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.**

**ADVARSEL!**

**Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.**

**ADVARSEL**

**Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.**

**VARNING**

**Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.**

**VAROITUS**

**Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.**

## 8.4 Product Regulatory Compliance

The server chassis product, when correctly integrated per this guide, complies with the following safety and electromagnetic compatibility (EMC) regulations.

**Intended Application** – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation.

**Notifications to Users on Product Regulatory Compliance and Maintaining Compliance –** To ensure regulatory compliance, you must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products / components will void the UL listing and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in the region(s) in which the product is sold.

To help ensure EMC compliance with your local regional rules and regulations, before computer integration, make sure that the chassis, power supply, and other modules have passed EMC testing using a server board with a microprocessor from the same family (or higher) and operating at the same (or higher) speed as the microprocessor used on this server board. The final configuration of your end system product may require additional EMC

compliance testing. For more information please contact your local Intel Representative. This is an FCC Class A device and its use is intended for a commercial type market place.

## 8.5 Use of Specified Regulated Components

To maintain the UL listing and compliance to other regulatory certifications and/or declarations, the following regulated components must be used and conditions adhered to. Interchanging or use of other component will void the UL listing and other product certifications and approvals.

Updated product information for configurations can be found on the Intel Server Builder Web site at the following URL: http://serverconfigurator.intel.com/default.aspx

Please contact your local Intel representative if you do not have access to Intel's Web address.,

**Server chassis** (base chassis is provided with power supply and fans) – NRTL listed.
**Server board –** you must use an Intel server board – UL recognized.
**Add-in boards –** must have a printed wiring board flammability rating of minimum UL94V-1. Add-in boards containing external power connectors and/or lithium batteries must be UL recognized or UL listed. Any add-in board containing modem telecommunication circuitry must be UL listed. In addition, the modem must have the appropriate telecommunications, safety, and EMC approvals for the region in which it is sold.
**Peripheral Storage Devices –** must be UL recognized or UL listed accessory and TUV or VDE licensed. Maximum power rating of any one device or combination of devices can not exceed manufacturer's specifications. Total server configuration is not to exceed the maximum loading conditions of the power supply.

The following table references Server Chassis Compliance and markings that may appear on the product. Markings below are typical markings however, may vary or be different based on how certification is obtained.

**Note:** Certifications Emissions requirements are to Class A.

**Table 79. Product Safety and Electromagnetic (EMC) Compliance**

| Compliance Regional Description | Compliance Reference | Compliance Reference Marking Example |
|---|---|---|
| Australia / New Zealand | AS/NZS CISPR22 (Emissions) | N232 |
| Argentina | IRAM Certification (Safety) | |
| Canada / USA | CSA 60950 – UL 60950-1 (Safety) Listing | 3178574 |
| | Industry Canada ICES-003 (Emissions) | CANADA ICES-003 CLASS A<br>CANADA NMB-003 CLASSE A |

| Compliance Regional Description | Compliance Reference | Compliance Reference Marking Example |
|---|---|---|
| | FCC<br>CFR 47, Part 15 (Emissions) | This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept interference receive, including interference that may cause undesired operation. |
| CENELEC Europe | Low Voltage Directive 2006/95/EC(Europe – EN60950-1);<br>EMC Directive 2004/108/EEC<br>EN55022 (Emissions)<br>EN55024 (Immunity)<br>EN61000-3-2 (Harmonics)<br>EN61000-3-3 (Voltage Flicker)<br>CE Declaration of Conformity | CE |
| Germany | GS Certification – EN60950-1 | Intertek GS |
| International | CB Certification – IEC60950-1<br>CISPR 22 / CISPR 24 | None Required |
| Japan | VCCI Certification | この装置は、クラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。VCCI-A |
| Korea | KCC Certification<br>MIC Notice No. 1997-41 (EMC) & 1997-42 (EMI) | 인증번호: CPU-SR1640(A) |
| Russia | GOST-R 50377-92 Certification<br>GOST R 29216-91 (Emissions)<br>GOST R 50628-95 (Immunity) | MO04 |
| Ukraine | Ukraine Certification | None Required |
| Taiwan | BSMI CNS13438 | R33025<br>警告使用者：<br>這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策 |

## 8.6 Electromagnetic Compatibility Notices

### 8.6.1 FCC Verification Statement (USA)

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

### 8.6.2 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

(English translation of the notice above) This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

### 8.6.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

### 8.6.4 Japan EMC Compatibility

Electromagnetic Compatibility Notices (International)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:

This is a Class A product based on the standard of the Voluntary Control Council For Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

### 8.6.5 BSMI (Taiwan)

The BSMI Certification number and the following warning is located on the product safety label which is located on the bottom side (pedestal orientation) or side (rack mount configuration).

警告使用者：

這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策。

### 8.6.6 KCC (Korea)

Following is the KCC certification information for Korea.

인증번호: CPU-SR1640 (A)

## 8.7 Rack Mount Installation Guidelines

Anchor the equipment rack: The equipment rack must be anchored to an unmovable support to prevent it from falling over when one or more servers are extended in front of the rack on

slides. You must also consider the weight of any other device installed in the rack. A crush hazard exists should the rack tilt forward which could cause serious injury.
Temperature: The temperature, in which the server operates when installed in an equipment rack, must not go below 5 °C (41 °F) or rise above 40 °C (104 °F). Extreme fluctuations in temperature can cause a variety of problems in your server.
Ventilation: The equipment rack must provide sufficient airflow to the front of the server to maintain proper cooling. The rack must also include ventilation sufficient to exhaust a maximum of 1023 BTUs (British Thermal Units) per hour for the server. The rack selected and the ventilation provided must be suitable to the environment in which the server will be used.

### 8.7.1 If AC power supplies are installed:

Mains AC power disconnection: The AC power cord(s) is considered the mains disconnect for the server and must be readily accessible when installed. If the individual server power cord(s) will not be readily accessible for disconnection then you are responsible for installing an AC power disconnect for the entire rack unit. This main disconnect must be readily accessible, and it must be labeled as controlling power to the entire rack, not just to the server(s).
Grounding the rack installation: To avoid the potential for an electrical shock hazard, you must include a third wire safety ground conductor with the rack installation. If the server power cord is plugged into an AC outlet that is part of the rack, then you must provide proper grounding for the rack itself. If the server power cord is plugged into a wall AC outlet, the safety ground conductor in the power cord provides proper grounding only for the server. You must provide additional, proper grounding for the rack and other devices installed in it.
Overcurrent protection: The server is designed for an AC line voltage source with up to 20 amperes of overcurrent protection per cord feed. If the power system for the equipment rack is installed on a branch circuit with more than 20 amperes of protection, you must provide supplemental protection for the server.

### 8.7.2 If DC power supplies are installed:

Connection with a DC (Direct Current) source should only be performed by trained service personnel. The server with DC input is to be installed in a Restricted Access Location in accordance with articles 110-16, 110-17, and 110-18 of the National Electric Code, ANSI/NFPA 70. The DC source must be electrically isolated by double or reinforced insulation from any hazardous AC source.
Main DC power disconnect: You are responsible for installing a properly rated DC power disconnect for the server system. This mains disconnect must be readily accessible, and it must be labeled as controlling power to the server. The circuit breaker of a centralized DC power system may be used as a disconnect device when easily accessible and should be rated no more than 10 amps.
Grounding the server: To avoid the potential for an electrical shock hazard, you must reliably connect an earth grounding conductor to the server. The earth grounding conductor must be a minimum 18AWG connected to the earth ground stud(s) on the rear of the server. The safety ground conductor should be connected to the chassis stud with a Listed closed two-hole crimp terminal having 5/8 inch pitch. The nuts on the chassis earth ground studs should be installed with a 10 in/lbs torque. The safety ground conductor provides proper grounding only for the server. You must provide additional, proper grounding for the rack and other devices installed in it.
Overcurrent protection: Overcurrent protection circuit breakers must be provided as part of each host equipment rack and must be incorporated in the field wiring between the DC source and the server. The branch circuit protection shall be rated minimum 75Vdc, 10 A maximum per feed pair. If the DC power system for the equipment rack is installed with more than 10 amperes of protection, you must provide supplemental protection for the server.

## 8.8 Power Cord Usage Guidelines

***Warning:*** *Do not attempt to modify or use an AC power cord set that is not the exact type required. You must use a power cord set that meets the following criteria:*

*• Rating: In the U.S. and Canada, cords must be UL (Underwriters Laboratories, Inc.) Listed/CSA (Canadian Standards Organization) Certified type SJT, 18-3 AWG (American Wire Gauge). Outside of the U.S. and Canada, cords must be flexible harmonized (<HAR>) or VDE (Verband Deutscher Electrotechniker, German Institute of Electrical Engineers) certified cord with 3 x 0.75 mm conductors rated 250 VAC (Volts Alternating Current).*

*• Connector, wall outlet end: Cords must be terminated in grounding-type male plug designed for use in your region. The connector must have certification marks showing certification by an agency acceptable in your region and for U.S. must be Listed and rated 125% of overall current rating of the server.*

*• Connector, server end: The connectors that plug into the AC receptacle on the server must be an approved IEC (International Electrotechnical Commission) 320, sheet C13, type female connector.*

*• Cord length and flexibility: Cords must be less than 4.5 meters (14.76 feet) long.*

## 8.9 Product Ecology Compliance

Intel has a system in place to restrict the use of banned substances in accordance with world wide product ecology regulatory requirements. The following is Intel's product ecology compliance criteria.

| Compliance Regional Description | Compliance Reference | Compliance Reference Marking Example |
|---|---|---|
| California | **CA. Lithium Perchlorate insert**<br>California Code of Regulations, Title 22, Division 4.5; Chapter 33: Best Management Practices for Perchlorate Materials. | Special handling may apply. See www.dtsc.ca.gov/hazardouswaste/perchlorate<br><br>This notice is required by California Code of Regulations, Title 22, Division 4.5; Chapter 33: Best Management Practices for Perchlorate Materials. This product / part includes a battery which contains Perchlorate material. |
| China | **China RoHS**<br>China RoHS (MII Measure 39)<br><br>Product marked with the Environmental Friendly Usage Period (EFUP) label of 20yrs, substance table in Simplified Chinese either placed with the product documentation or separate insert. |  |
| | **China Recycling (GB18455-2001)**<br>Mark requires to be applied to be retail product only. Marking applied to bulk packaging and single packages. Not applied to internal packaging such as plastics, foams, etc. |  |

| Compliance Regional Description | Compliance Reference | Compliance Reference Marking Example |
|---|---|---|
| Intel Internal Specification | All materials, parts and subassemblies must not contain restricted materials as defined in Intel's ***Environmental Product Content Specification*** of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm | None Required |
| Europe | **Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC** – Mark applied to system level products only. |  |
| | **European Directive 2002/95/EC** - Restriction of Hazardous Substances (RoHS) Threshold limits and banned substances are noted below.<br>Quantity limit of 0.1% by mass (1000 PPM) for:<br>Lead, Mercury, Hexavalent Chromium, Polybrominated Biphenyls Diphenyl Ethers (PBB/PBDE)<br>Quantity limit of 0.01% by mass (100 PPM) for:<br>Cadmium | None Required |
| Intel Internal Specification | All materials, parts and subassemblies must not contain restricted materials as defined in Intel's ***Environmental Product Content Specification*** of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm | None Required |
| International | **ISO11469** - Plastic parts weighing >25gm are intended to be marked with per ISO11469. | >PC/ABS< |
| | Recycling Markings – Fiberboard (FB) and Cardboard (CB) are marked with international recycling marks. Applied to outer bulk packaging and single package. |    |

## 8.10 Other Markings

| Compliance Description | Compliance Reference | Compliance Reference Marking Example |
|---|---|---|
| Stand-by Power | 60950 Safety Requirement<br>Applied to product is stand-by power switch is used. |  |
| Multiple Power Cords | 60950 Safety Requirement<br>Applied to product if more than one power cord is used. | English:<br>This unit has more than one power supply cord. To reduce the risk of electrical shock, disconnect (2) two power supply cords before servicing. |
| | | Simplified Chinese:<br>注意：<br>本设备包括多条电源系统电缆。为避免遭受电击，在进行维修之前应断开两（2）条电源系统电缆。 |
| | | Traditional Chinese: |

| Compliance Description | Compliance Reference | Compliance Reference Marking Example |
|---|---|---|
| | | 注意：<br>本設備包括多條電源系統電纜。為避免遭受電擊，在進行維修之前應斷開兩（2）條電源系統電纜。 |
| | | German:<br>Dieses Geräte hat mehr als ein Stromkabel. Um eine Gefahr des elektrischen Schlages zu verringern trennen sie beide (2) Stromkabeln bevor Instandhaltung. |
| Ground Connection | 60950 Deviation for Nordic Countries | Line1 :<br>"WARNING:"<br>Swedish on line2:<br>"Apparaten skall anslutas till jordat uttag, när den ansluts till ett nätverk."<br>Finnish on line 3:<br>"Laite on liitettävä suojamaadoituskoskettimilla varustettuun pistorasiaan."<br>English on line 4:<br>"Connect only to a properly earth grounded outlet." |
| Country of Origin | Logistic Requirements<br>Applied to products to indicate where product was made. | **Made in China** |

# Appendix A: Integration and Usage Tips

Before attempting to integrate and configure your system, you should reference this section, which provides a list of useful information.

- After the system is integrated with processors, memory, and peripheral devices, the FRUSDR utility **must** be run to load the proper Sensor Data Record data to the integrated Server Management subsystem. Failure to run this utility may prevent Server Management from accurately monitoring system health and may affect system performance. The FRUSDR utility for this server system can either be run from the Intel Deployment CDROM that came with your system, or can be downloaded from the Intel website referenced at the bottom of this page.

- To ensure the highest system reliability, make sure the latest system software is loaded on the server before deploying the system onto a live networking environment. This includes system BIOS, FRUSDR, BMC firmware, and hot-swap controller firmware. The system software can be updated using the Intel Deployment CDROM that came with your system or can be downloaded from the Intel website referenced at the bottom of this page.

- System fans are not hot-swappable.

- Only supported memory validated by Intel should be used in this server system. A list of supported memory can be found in the Intel® Server System SR1640TH Tested Memory List which can be downloaded from the Intel website referenced at the bottom of this page.

- This system supports the Intel® Xeon® processor 3400 sequence. You cannot use Intel® Xeon® processors not referenced on the supported processor list in this server system.

- You must use the CPU/memory air duct to maintain system thermals.

- To maintain system thermals, you must populate all hard drive bays with either a hard drive or drive blank.

- You must remove power from the system prior to opening the chassis for service

You can download the latest system documentation, drivers, and system software from the Intel Support website:

http://support.intel.com/support/motherboards/server/SR1640TH/

# Appendix B: Integrated BMC Sensor Tables

This appendix lists the sensor identification numbers and information about the sensor type, name, supported thresholds, assertion and de-assertion information, and a brief description of the sensor purpose. See the Intelligent Platform Management Interface Specification, Version 2.0, for sensor and event/reading-type table information.

- **Sensor Type**

  The Sensor Type values are the values enumerated in the Sensor Type Codes table in the IPMI specification. The Sensor Type provides the context in which to interpret the sensor, such as the physical entity or characteristic that is represented by this sensor.

- **Event / Reading Type**

  The Event/Reading Type values are from the Event/Reading Type Code Ranges and Generic Event/Reading Type Codes tables in the IPMI specification. Digital sensors are a specific type of discrete sensor, which have only two states.

- **Event Offset/Triggers**

  Event Thresholds are event-generating thresholds for threshold types of sensors.

  - [u,l][nr,c,nc]: upper non-recoverable, upper critical, upper non-critical, lower non-recoverable, lower critical, lower non-critical
  - uc, lc: upper critical, lower critical

  Event Triggers are supported event-generating offsets for discrete type sensors. The offsets can be found in the Generic Event/Reading Type Codes or Sensor Type Codes tables in the IPMI specification, depending on whether the sensor event/reading type is generic or a sensor-specific response.

- **Assertion / De-assertion Enables**

  Assertion and de-assertion indicators reveal the type of events the sensor generates:

  - As: Assertions
  - De: De-assertion

- **Readable Value / Offsets**

  - Readable Value indicates the type of value returned for threshold and other non-discrete type sensors.
  - Readable Offsets indicate the offsets for discrete sensors that are readable with the Get Sensor Reading command. Unless otherwise indicated, all event triggers are readable; Readable Offsets consist of the reading type offsets that do not generate events.

- **Event Data**

  Event data is the data that is included in an event message generated by the sensor. For threshold-based sensors, the following abbreviations are used:

  - R: Reading value
  - T: Threshold value

- **Rearm Sensors**

  The rearm is a request for the event status for a sensor to be rechecked and updated upon a transition between good and bad states. Rearming the sensors can be done manually or automatically. This column indicates the type supported by the sensor. The following abbreviations are used to describe a sensor:

  - A: Auto-rearm
  - M: Manual rearm

- **Default Hysteresis**

  The hysteresis setting applies to all thresholds of the sensor. This column provides the count of hysteresis for the sensor, which can be 1 or 2 (positive or negative hysteresis).

- **Criticality**

  Criticality is a classification of the severity and nature of the condition. It also controls the behavior of the Control Panel Status LED

- **Standby**

  Some sensors operate on standby power. These sensors may be accessed and / or generate events when the main (system) power is off, but AC power is present.

**Table 80. Integrated BMC Sensor Table**

| Sensor Name[3] | Sensor # | Platform Applicability | Sensor Type | Event / Reading Type | Event Offset Triggers | Contrib. To System Status | Assert / De-assert | Readable Value / Offsets | Event Data | Rearm | Stand-by |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IPMI Watchdog | 03h | All | Watchdog 2 23h | Sensor Specific 6Fh | 00 - Timer expired, status only<br>01 - Hard reset<br>02 - Power down<br>03 - Power cycle<br>08 - Timer interrupt | OK | As | – | Trig Offset | A | X |
| Physical Scrty | 04h | Chassis Intrusion is chassis-specific | Physical Security 05h | Sensor Specific 6Fh | 00 - Chassis intrusion | OK | As and De | – | Trig Offset | A | X |
| | | | | | 04 - LAN least lost | Degraded | | | | | |
| FP Interrupt (NMI) | 05h | All | Critical Interrupt 13h | Sensor Specific 6Fh | 00 - Front panel NMI / diagnostic interrupt | OK | As | – | Trig Offset | A | – |
| System Event Log | 07h | All | Event Logging Disabled 10h | Sensor Specific 6Fh | 02 - Log area reset / cleared | OK | As | – | Trig Offset | A | X |
| System Event (System Event) | 08h | All | System Event 12h | Sensor Specific 6Fh | 04 – PEF action | OK | As | - | Trig Offset | A,I | X |
| BB +1.05 PCH | 10h | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded<br>c = Non-fatal | As and De | Analog | R, T | A | – |

| Sensor Name[3] | Sensor # | Platform Applicability | Sensor Type | Event / Reading Type | Event Offset Triggers | Contrib. To System Status | Assert / De-assert | Readable Value / Offsets | Event Data | Rearm | Stand-by |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BB +1.1V P1 Vccp | 11h | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | – |
| BB +1.1V P2 Vccp | 12h | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | – |
| BB +1.5V P1 DDR3 | 13h | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | – |
| BB +1.5V P2 DDR3 | 14h | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | – |
| BB +1.8V AUX | 15h | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | X |
| BB +3.3V | 16h | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | – |
| BB +3.3V STBY | 17h | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | X |
| BB Vbat | 18h | All | Voltage 02h | Generic 05h | 01 - Limit exceeded | Non-fatal | As and De | – | Trig Offset | A | X |
| BB +5.0V | 19h | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | – |
| BB +5.0V STBY | 1Ah | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | X |
| BB +12.0V | 1Bh | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | – |
| BB -12.0V | 1Ch | All | Voltage 02h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | – |
| Server board Temp | 20h | All | Temperature 01h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | X |

| Sensor Name[3] | Sensor # | Platform Applicability | Sensor Type | Event / Reading Type | Event Offset Triggers | Contrib. To System Status | Assert / De-assert | Readable Value / Offsets | Event Data | Rearm | Stand-by |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Front panel temp | 21h | All | Temperature 01h | Threshold 01h | [u,l] [c,nc] | nc = Degraded c = Non-fatal | As and De | Analog | R, T | A | X |
| PCH Thermal Margin | 22h | All | Temperature 01h | Threshold 01h | - | - | - | Analog | - | - | - |
| Processor MEMTHRM MRGN | 23h | All | Temperature 01h | Threshold 01h | - | - | - | Analog | - | - | - |
| Fan Tach Sensors | 30h–34h | Chassis-specific | Fan 04h | Threshold 01h | [l] [c,nc] | nc = Degraded c = Non-fatal[2] | As and De | Analog | R, T | M | |
| Processor Therm Margin | 62h | All | Temperature 01h | Threshold 01h | – | – | – | Analog | – | – | – |
| Processor Therm Ctrl % | 64h | All | Temperature 01h | Threshold 01h | [u] [c] | Non-fatal | As and De | Analog | Trig Offset | A | – |
| Processor VRD Temp | 66h | All | Temperature 01h | Digital Discrete 05h | 01 - Limit exceeded | Fatal | As and De | – | Trig Offset | M | – |
| CATERR | 68h | All | Processor 07h | Digital Discrete 03h | 01 – State Asserted | Non-fatal | As and De | – | Trig Offset | M | – |
| PCH Thermal Trip | 6Ah | All | Temperature 01h | Digital Discrete 03h | 01 – State Asserted | Fatal | As and De | – | Trig Offset | M | – |

# Appendix C: POST Code LED Decoder

During the system boot process, the BIOS executes a number of platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the POST code to the POST Code Diagnostic LEDs on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, you can use the diagnostic LEDs to identify the last POST process executed.

Each POST code is represented by the eight amber diagnostic LEDs. The POST codes are divided into two nibbles, an upper nibble and a lower nibble. The upper nibble bits are represented by diagnostic LEDs #4, #5, #6, and #7. The lower nibble bits are represented by diagnostics LEDs #0, #1, #2, and #3. If the bit is set in the upper and lower nibbles, then the corresponding LED is lit. If the bit is clear, then the corresponding LED is off.

The diagnostic LED #7 is labeled as “MSB” (Most Significant Bit), and the diagnostic LED #0 is labeled as “LSB” (Least Significant Bit).

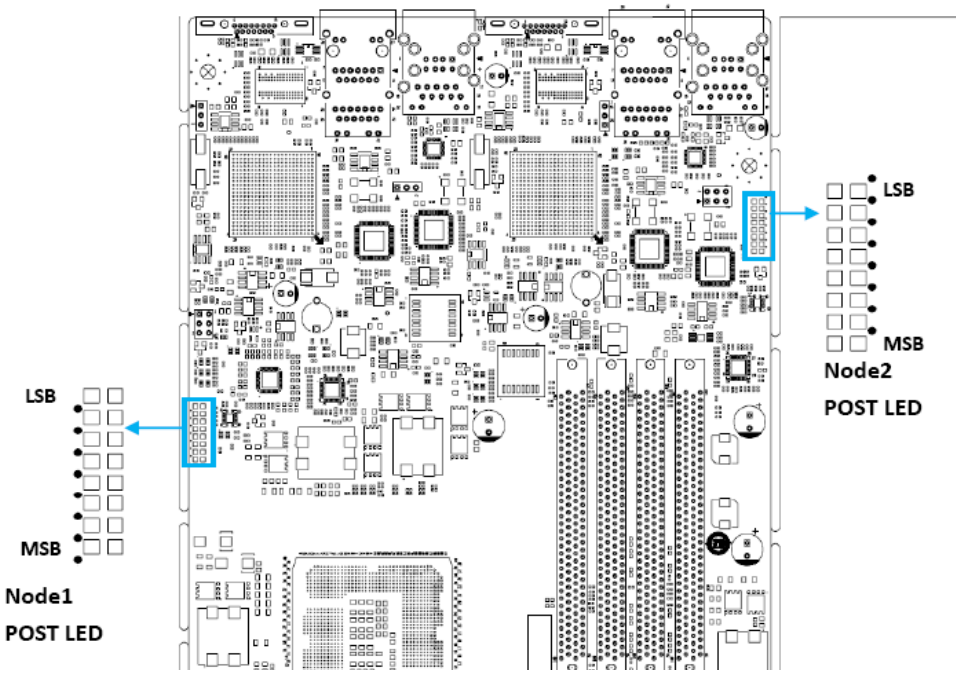



**Figure 47. Diagnostic LED Placement Diagram**

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

**Table 81. POST Progress Code LED Example**

| LEDs | Upper Nibble LEDs | | | | Lower Nibble LEDs | | | |
|---|---|---|---|---|---|---|---|---|
| | MSB | | | | | | | LSB |
| | LED #7 | LED #6 | LED #5 | LED #4 | LED #3 | LED #2 | LED #1 | LED #0 |
| | 8h | 4h | 2h | 1h | 8h | 4h | 2h | 1h |
| **Status** | ON | OFF | ON | OFF | ON | ON | OFF | OFF |
| **Results** | **1** | 0 | **1** | 0 | **1** | **1** | 0 | 0 |
| | **Ah** | | | | **Ch** | | | |

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh.

## Table 82. POST Progress Code LED Example

| Checkpoint | Diagnostic LED Decoder O = On, X=Off | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|
| | Upper Nibble | | | | Lower Nibble | | | | |
| | MSB | | | | | | | LSB | |
| | 8h | 4h | 2h | 1h | 8h | 4h | 2h | 1h | |
| LED | #7 | #6 | #5 | #4 | #3 | #2 | #1 | #0 | |
| Host Processor | | | | | | | | | |
| 0x04h | X | X | X | X | X | O | X | X | Early processor initialization (flat32.asm) where system BSP is selected |
| 0x10h | X | X | X | O | X | X | X | X | Power-on initialization of the host processor (Boot Strap Processor) |
| 0x11h | X | X | X | O | X | X | X | O | Host processor cache initialization (including AP) |
| 0x12h | X | X | X | O | X | X | O | X | Starting application processor initialization |
| 0x13h | X | X | X | O | X | X | O | O | SMM initialization |
| Chipset | | | | | | | | | |
| 0x21h | X | X | O | X | X | X | X | O | Initializing a chipset component |
| Memory | | | | | | | | | |
| 0x22h | X | X | O | X | X | X | O | X | Reading configuration data from memory (SPD on FBDIMM) |
| 0x23h | X | X | O | X | X | X | O | O | Detecting presence of memory |
| 0x24h | X | X | O | X | X | O | X | X | Programming timing parameters in the memory controller |
| 0x25h | X | X | O | X | X | O | X | O | Configuring memory parameters in the memory controller |
| 0x26h | X | X | O | X | X | O | O | X | Optimizing memory controller settings |
| 0x27h | X | X | O | X | X | O | O | O | Initializing memory, such as ECC init |
| 0x28h | X | X | O | X | O | X | X | X | Testing memory |
| PCI Bus | | | | | | | | | |
| 0x50h | X | O | X | O | X | X | X | X | Enumerating PCI buses |
| 0x51h | X | O | X | O | X | X | X | O | Allocating resources to PCI buses |
| 0x52h | X | O | X | O | X | X | O | X | Hot Plug PCI controller initialization |
| 0x53h | X | O | X | O | X | X | O | O | Reserved for PCI bus |
| 0x54h | X | O | X | O | X | O | X | X | Reserved for PCI bus |
| 0x55h | X | O | X | O | X | O | X | O | Reserved for PCI bus |
| 0x56h | X | O | X | O | X | O | O | X | Reserved for PCI bus |
| 0x57h | X | O | X | O | X | O | O | O | Reserved for PCI bus |
| USB | | | | | | | | | |
| 0x58h | X | O | X | O | O | X | X | X | Resetting USB bus |
| 0x59h | X | O | X | O | O | X | X | O | Reserved for USB devices |
| ATA/ATAPI/SATA | | | | | | | | | |
| 0x5Ah | X | O | X | O | O | X | O | X | Resetting SATA bus and all devices |
| 0x5Bh | X | O | X | O | O | X | O | O | Detecting the presence of ATA device |
| 0x5Ch | X | O | X | O | O | O | X | X | Enable SMART if supported by ATA device |
| 0x5Dh | X | O | X | O | O | O | X | O | Reserved for ATA |
| SMBUS | | | | | | | | | |
| 0x5Eh | X | O | X | O | O | O | O | X | Resetting SMBUS |
| 0x5Fh | X | O | X | O | O | O | O | O | Reserved for SMBUS |
| Local Console | | | | | | | | | |
| 0x70h | X | O | O | O | X | X | X | X | Resetting the video controller (VGA) |
| 0x71h | X | O | O | O | X | X | X | O | Disabling the video controller (VGA) |
| 0x72h | X | O | O | O | X | X | O | X | Enabling the video controller (VGA) |
| Remote Console | | | | | | | | | |
| 0x78h | X | O | O | O | O | X | X | X | Resetting the console controller |
| 0x79h | X | O | O | O | O | X | X | O | Disabling the console controller |
| 0x7Ah | X | O | O | O | O | X | O | X | Enabling the console controller |
| Keyboard (only USB) | | | | | | | | | |
| 0x90h | O | X | X | O | X | X | X | X | Resetting the keyboard |
| 0x91h | O | X | X | O | X | X | X | O | Disabling the keyboard |
| 0x92h | O | X | X | O | X | X | O | X | Detecting the presence of the keyboard |
| 0x93h | O | X | X | O | X | X | O | O | Enabling the keyboard |
| 0x94h | O | X | X | O | X | O | X | X | Clearing keyboard input buffer |
| 0x95h | O | X | X | O | X | O | X | O | Reserved for keyboard |
| Mouse (only USB) | | | | | | | | | |
| 0x98h | O | X | X | O | X | X | O | X | Resetting the mouse |

| Checkpoint | Diagnostic LED Decoder O = On, X=Off | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|
| | Upper Nibble | | | | Lower Nibble | | | | |
| | MSB | | | | | | | LSB | |
| | 8h | 4h | 2h | 1h | 8h | 4h | 2h | 1h | |
| LED | #7 | #6 | #5 | #4 | #3 | #2 | #1 | #0 | |
| 0x99h | O | X | X | O | X | X | O | O | Detecting the mouse |
| 0x9Ah | O | X | X | O | X | O | O | X | Detecting the presence of mouse |
| 0x9Bh | O | X | X | O | X | O | O | O | Enabling the mouse |
| Fixed Media | | | | | | | | | |
| 0xB0h | O | X | O | O | X | X | X | X | Resetting fixed media device |
| 0xB1h | O | X | O | O | X | X | X | O | Disabling fixed media device |
| 0xB2h | O | X | O | O | X | X | O | X | Detecting presence of a fixed media device (SATA hard drive detection, etc.) |
| 0xB3h | O | X | O | O | X | X | O | O | Enabling / configuring a fixed media device |
| Removable Media | | | | | | | | | |
| 0xB8h | O | X | O | O | O | X | X | X | Resetting removable media device |
| 0xB9h | O | X | O | O | O | X | X | O | Disabling removable media device |
| 0xBAh | O | X | O | O | O | X | O | X | Detecting presence of a removable media device (SATA CDROM detection, etc.) |
| 0xBCh | O | X | O | O | O | O | X | X | Enabling / configuring a removable media device |
| Boot Device Selection (BDS) | | | | | | | | | |
| 0xD0 | O | O | X | O | X | X | X | X | Entered the Boot Device Selection phase (BDS) |
| 0xD1 | O | O | X | O | X | X | X | O | Return to last good boot device |
| 0xD2 | O | O | X | O | X | X | O | X | Setup boot device selection policy |
| 0xD3 | O | O | X | O | X | X | O | O | Connect boot device controller |
| 0xD4 | O | O | X | O | X | O | X | X | Attempt flash update boot mode |
| 0xD5 | O | O | X | O | X | O | X | O | Transfer control to EFI boot |
| 0xD6 | O | O | X | O | X | O | O | X | Trying to boot device selection |
| 0xDF | O | O | X | O | O | O | O | O | Reserved for boot device selection |
| Pre-EFI Initialization (PEI) Core | | | | | | | | | |
| 0xE0h | O | O | O | X | X | X | X | X | Entered Pre-EFI Initialization phase (PEI) |
| 0xE1h | O | O | O | X | X | X | X | O | Started dispatching early initialization modules (PEIM) |
| 0xE2h | O | O | O | X | X | X | O | X | Initial memory found, configured, and installed correctly |
| 0xE3h | O | O | O | X | X | X | O | O | Transfer control to the DXE Core |
| Driver eXecution Environment (DXE) Core | | | | | | | | | |
| 0xE4h | O | O | O | X | X | O | X | X | Entered EFI driver execution phase (DXE) |
| 0xE5h | O | O | O | X | X | O | X | O | Started dispatching drivers |
| 0xE6h | O | O | O | X | X | O | O | X | Started connecting drivers |
| DXE Drivers | | | | | | | | | |
| 0xE7h | O | O | O | X | O | O | X | O | Waiting for user input |
| 0xE8h | O | O | O | X | O | X | X | X | Checking password |
| 0xE9h | O | O | O | X | O | X | X | O | Entering BIOS setup |
| 0xEAh | O | O | O | X | O | O | X | X | Flash Update |
| 0xEEh | O | O | O | X | O | O | X | X | Calling Int 19. One beep unless silent boot is enabled. |
| 0xEFh | O | O | O | X | O | O | X | O | Unrecoverable boot failure |
| Pre-EFI Initialization Module (PEIM) / Recovery | | | | | | | | | |
| 0x30h | X | X | O | O | X | X | X | X | Crisis recovery has been initiated because of a user request |
| 0x31h | X | X | O | O | X | X | X | O | Crisis recovery has been initiated by software (corrupt flash) |
| 0x34h | X | X | O | O | X | O | X | X | Loading crisis recovery capsule |
| 0x35h | X | X | O | O | X | O | X | O | Handing off control to the crisis recovery capsule |
| 0x3Fh | X | X | O | O | O | O | O | O | Crisis recovery capsule failed integrity check of capsule descriptors |
| Runtime Phase / EFI Operating System Boot | | | | | | | | | |
| 0XF2h | O | O | O | O | X | X | O | X | Signal that the OS has switched to virtual memory mode |
| 0XF4h | O | O | O | O | X | O | X | X | Entering the sleep state |
| 0XF5h | O | O | O | O | X | O | X | O | Exiting the sleep state |
| 0XF8h | O | O | O | O | O | X | X | X | Operating system has requested EFI to close boot services has been cancelled. |
| Progress Code | | | | | | | | | |
| 0XF9h | O | X | X | O | X | X | X | X | Resetting the keyboard |
| 0xFAh | O | X | X | O | X | X | X | O | Disabling the keyboard |

# Appendix D: POST Code Errors

Whenever possible, the BIOS outputs the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The Response section in the following table is divided into three types:

**No Pause:** The message is displayed on the local Video screen during POST or in the Error Manager. The system continues booting with a degraded state. The user may want to replace the erroneous unit. The setup POST error Pause setting does not have any effect with this error.

**Pause:** The message is displayed on the Error Manager screen, and an error is logged to the SEL. The setup POST error Pause setting determines whether the system pauses to the Error Manager for this type of error, where the user can take immediate corrective action or choose to continue booting.

**Halt:** The message is displayed on the Error Manager screen, an error is logged to the SEL, and the system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system. The setup POST error Pause setting does not have any effect with this error.

**Table 83. POST Error Message and Handling**

| Error Code | Error Message | Response |
|---|---|---|
| 0012 | CMOS date/time not set | Pause |
| 0048 | Password check failed | Halt |
| 0108 | Keyboard component encountered a locked error | No Pause |
| 0109 | Keyboard component encountered a stuck key error | No Pause |
| 0113 | Fixed Media The SAS RAID firmware cannot run properly. The user should attempt to re-flash the firmware. | Pause |
| 0140 | PCI component encountered a PERR error | Pause |
| 0141 | PCI resource conflict | Pause |
| 0146 | PCI out of resources error | Pause |
| 0192 | L3 cache size mismatch | Halt |
| 0194 | CPUID, processor family are different | Halt |
| 0195 | Front side bus mismatch | Pause |
| 0196 | Processor model mismatch | Pause |
| 0197 | Processor speed mismatch | Pause |
| 0198 | Processor family is unsupported | Pause |
| 019F | Processor and chipset stepping configuration is unsupported | Pause |
| 5220 | CMOS/NVRAM configuration cleared | Pause |
| 5221 | Password cleared by jumper | Pause |
| 5224 | Password clear jumper is set | Pause |
| 8110 | Processor 01 internal error (IERR) on last boot | Pause |
| 8111 | Processor 02 internal error (IERR) on last boot | Pause |
| 8120 | Processor 01 thermal trip error on last boot | Pause |
| 8121 | Processor 02 thermal trip error on last boot | Pause |
| 8130 | Processor 01 disabled | Pause |
| 8131 | Processor 02 disabled | Pause |
| 8140 | Processor 01 Failed FRB-3 Timer. | No Pause |
| 8141 | Processor 02 Failed FRB-3 Timer. | No Pause |
| 8160 | Processor 01 unable to apply BIOS update | Pause |
| 8161 | Processor 02 unable to apply BIOS update | Pause |
| 8170 | Processor 01 failed Self Test (BIST). | Pause |

| Error Code | Error Message | Response |
|---|---|---|
| 8171 | Processor 02 failed Self Test (BIST). | Pause |
| 8180 | Processor 01 BIOS does not support the current stepping for processor | No Pause |
| 8181 | Processor 02 BIOS does not support the current stepping for processor | No Pause |
| 8190 | Watchdog timer failed on last boot | Pause |
| 8198 | Operating system boot watchdog timer expired on last boot | Pause |
| 8300 | Integrated Baseboard Management Controller failed self-test | Pause |
| 84F2 | Integrated Baseboard Management Controller failed to respond | Pause |
| 84F3 | Integrated Baseboard Management Controller in update mode | Pause |
| 84F4 | Sensor data record empty | Pause |
| 84FF | System event log full | No Pause |
| 8500 | Memory component could not be configured in the selected RAS mode. | Pause |
| 8520 | DIMM_A1 failed Self Test (BIST). | Pause |
| 8521 | DIMM_A2 failed Self Test (BIST). | Pause |
| 8522 | DIMM_A3 failed Self Test (BIST). | Pause |
| 8523 | DIMM_A4 failed Self Test (BIST). | Pause |
| 8524 | DIMM_B1 failed Self Test (BIST). | Pause |
| 8525 | DIMM_B2 failed Self Test (BIST). | Pause |
| 8526 | DIMM_B3 failed Self Test (BIST). | Pause |
| 8527 | DIMM_B4 failed Self Test (BIST). | Pause |
| 8528 | DIMM_C1 failed Self Test (BIST). | Pause |
| 8529 | DIMM_C2 failed Self Test (BIST). | Pause |
| 852A | DIMM_C3 failed Self Test (BIST). | Pause |
| 852B | DIMM_C4 failed Self Test (BIST). | Pause |
| 852C | DIMM_D1 failed Self Test (BIST). | Pause |
| 852D | DIMM_D2 failed Self Test (BIST). | Pause |
| 852E | DIMM_D3 failed Self Test (BIST). | Pause |
| 852F | DIMM_D4 failed Self Test (BIST). | Pause |
| 8540 | DIMM_A1 Disabled. | Pause |
| 8541 | DIMM_A2 Disabled. | Pause |
| 8542 | DIMM_A3 Disabled. | Pause |
| 8543 | DIMM_A4 Disabled. | Pause |
| 8544 | DIMM_B1 Disabled. | Pause |
| 8545 | DIMM_B2 Disabled. | Pause |
| 8546 | DIMM_B3 Disabled. | Pause |
| 8547 | DIMM_B4 Disabled. | Pause |
| 8548 | DIMM_C1 Disabled. | Pause |
| 8549 | DIMM_C2 Disabled. | Pause |
| 854A | DIMM_C3 Disabled. | Pause |
| 854B | DIMM_C4 Disabled. | Pause |
| 854C | DIMM_D1 Disabled. | Pause |
| 854D | DIMM_D2 Disabled. | Pause |
| 854E | DIMM_D3 Disabled. | Pause |
| 854F | DIMM_D4 Disabled. | Pause |
| 8560 | DIMM_A1 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 8561 | DIMM_A2 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 8562 | DIMM_A3 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 8563 | DIMM_A4 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 8564 | DIMM_B1 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 8565 | DIMM_B2 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 8566 | DIMM_B3 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 8567 | DIMM_B4 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 8568 | DIMM_C1 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 8569 | DIMM_C2 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 856A | DIMM_C3 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 856B | DIMM_C4 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 856C | DIMM_D1 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 856D | DIMM_D2 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 856E | DIMM_D3 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 856F | DIMM_D4 Component encountered a Serial Presence Detection (SPD) fail error. | Pause |
| 8580 | DIMM_A1 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 8581 | DIMM_A2 Correctable ECC error encountered. | Pause after 10 Occurrence |

| Error Code | Error Message | Response |
|---|---|---|
| 8582 | DIMM_A3 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 8583 | DIMM_A4 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 8584 | DIMM_B1 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 8585 | DIMM_B2 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 8586 | DIMM_B3 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 8587 | DIMM_B4 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 8588 | DIMM_C1 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 8589 | DIMM_C2 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 858A | DIMM_C3 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 858B | DIMM_C4 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 858C | DIMM_D1 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 858D | DIMM_D2 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 858E | DIMM_D3 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 858F | DIMM_D4 Correctable ECC error encountered. | Pause after 10 Occurrence |
| 85A0 | DIMM_A1 Uncorrectable ECC error encountered. | Pause |
| 85A1 | DIMM_A2 Uncorrectable ECC error encountered. | Pause |
| 85A2 | DIMM_A3 Uncorrectable ECC error encountered. | Pause |
| 85A3 | DIMM_A4 Uncorrectable ECC error encountered. | Pause |
| 85A4 | DIMM_B1 Uncorrectable ECC error encountered. | Pause |
| 85A5 | DIMM_B2 Uncorrectable ECC error encountered. | Pause |
| 85A6 | DIMM_B3 Uncorrectable ECC error encountered. | Pause |
| 85A7 | DIMM_B4 Uncorrectable ECC error encountered. | Pause |
| 85A8 | DIMM_C1 Uncorrectable ECC error encountered. | Pause |
| 85A9 | DIMM_C2 Uncorrectable ECC error encountered. | Pause |
| 85AA | DIMM_C3 Uncorrectable ECC error encountered. | Pause |
| 85AB | DIMM_C4 Uncorrectable ECC error encountered. | Pause |
| 85AC | DIMM_D1 Uncorrectable ECC error encountered. | Pause |
| 85AD | DIMM_D2 Uncorrectable ECC error encountered. | Pause |
| 85AE | DIMM_D3 Uncorrectable ECC error encountered. | Pause |
| 85AF | DIMM_D4 Uncorrectable ECC error encountered. | Pause |
| 8601 | Override jumper is set to force boot from lower alternate BIOS bank of flash ROM | No Pause |
| 8602 | WatchDog timer expired (secondary BIOS may be bad!) | No Pause |
| 8603 | Secondary BIOS checksum fail | No Pause |
| 8604 | Chipset Reclaim of non critical variables complete. | No Pause |
| 9000 | Unspecified processor component has encountered a non specific error. | Pause |
| 9223 | Keyboard component was not detected. | No Pause |
| 9226 | Keyboard component encountered a controller error. | No Pause |
| 9243 | Mouse component was not detected. | No Pause |
| 9246 | Mouse component encountered a controller error. | No Pause |
| 9266 | Local Console component encountered a controller error. | No Pause |
| 9268 | Local Console component encountered an output error. | No Pause |
| 9269 | Local Console component encountered a resource conflict error. | No Pause |
| 9286 | Remote Console component encountered a controller error. | No Pause |
| 9287 | Remote Console component encountered an input error. | No Pause |
| 9288 | Remote Console component encountered an output error. | No Pause |
| 92A3 | Serial port component was not detected | Pause |
| 92A9 | Serial port component encountered a resource conflict error | Pause |
| 92C6 | Serial Port controller error | No Pause |
| 92C7 | Serial Port component encountered an input error. | No Pause |

| Error Code | Error Message | Response |
|---|---|---|
| 92C8 | Serial Port component encountered an output error. | No Pause |
| 94C6 | LPC component encountered a controller error. | No Pause |
| 94C9 | LPC component encountered a resource conflict error. | Pause |
| 9506 | ATA/ATPI component encountered a controller error. | No Pause |
| 95A6 | PCI component encountered a controller error. | No Pause |
| 95A7 | PCI component encountered a read error. | No Pause |
| 95A8 | PCI component encountered a write error. | No Pause |
| 9609 | Unspecified software component encountered a start error. | No Pause |
| 9641 | PEI Core component encountered a load error. | No Pause |
| 9667 | PEI module component encountered an illegal software state error. | Halt |
| 9687 | DXE core component encountered an illegal software state error. | Halt |
| 96A7 | DXE boot services driver component encountered an illegal software state error. | Halt |
| 96AB | DXE boot services driver component encountered invalid configuration. | No Pause |
| 96E7 | SMM driver component encountered an illegal software state error. | Halt |
| 0xA022 | Processor component encountered a mismatch error. | Pause |
| 0xA027 | Processor component encountered a low voltage error. | No Pause |
| 0xA028 | Processor component encountered a high voltage error. | No Pause |
| 0xA421 | PCI component encountered a SERR error. | Halt |
| 0xA500 | ATA/ATPI ATA bus SMART not supported. | No Pause |
| 0xA501 | ATA/ATPI ATA SMART is disabled. | No Pause |
| 0xA5A0 | PCI Express* component encountered a PERR error. | No Pause |
| 0xA5A1 | PCI Express* component encountered a SERR error. | Halt |
| 0xA5A4 | PCI Express* IBIST error. | Pause |
| 0xA6A0 | DXE boot services driver Not enough memory available to shadow a legacy option ROM. | No Pause |

## POST Error Beep Codes

The following table lists POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user-visible code on POST Progress LEDs.

**Table 84. POST Error Beep Codes**

| Beeps | Error Message | POST Progress Code | Description |
|---|---|---|---|
| 3 | Memory error | Multiple | System halted because a fatal error related to the memory was detected. |

# Glossary

| Term | Definition |
|---|---|
| ACPI | Advanced Configuration and Power Interface |
| AP | Application Processor |
| APIC | Advanced Programmable Interrupt Control |
| ASIC | Application Specific Integrated Circuit |
| ASMI | Advanced Server Management Interface |
| BIOS | Basic Input/Output System |
| BIST | Built-In Self Test |
| BMC | Baseboard Management Controller |
| Bridge | Circuitry connecting one computer bus to another, allowing an agent on one to access the other |
| BSP | Bootstrap Processor |
| Byte | 8-bit quantity. |
| CBC | Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.) |
| CEK | Common Enabling Kit |
| CHAP | Challenge Handshake Authentication Protocol |
| CMOS | In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board. |
| DPC | Direct Platform Control |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| EHCI | Enhanced Host Controller Interface |
| EMP | Emergency Management Port |
| EPS | External Product Specification |
| ESB2-E | Enterprise South Bridge 2 |
| FBD | Fully Buffered DIMM |
| FMB | Flexible Mother Board |
| FRB | Fault Resilient Booting |
| FRU | Field Replaceable Unit |
| FSB | Front Side Bus |
| GB | 1024MB |
| GPIO | General Purpose I/O |
| GTL | Gunning Transceiver Logic |
| HSC | Hot-Swap Controller |
| Hz | Hertz (1 cycle/second) |
| $I^2C$ | Inter-Integrated Circuit Bus |
| IA | Intel® Architecture |
| IBF | Input Buffer |
| ICH | I/O Controller Hub |
| ICMB | Intelligent Chassis Management Bus |
| IERR | Internal Error |
| IFB | I/O and Firmware Bridge |
| INTR | Interrupt |
| IP | Internet Protocol |
| IPMB | Intelligent Platform Management Bus |
| IPMI | Intelligent Platform Management Interface |
| IR | Infrared |
| ITP | In-Target Probe |
| KB | 1024 bytes |
| KCS | Keyboard Controller Style |

| Term | Definition |
|---|---|
| LAN | Local Area Network |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diode |
| LPC | Low Pin Count |
| LUN | Logical Unit Number |
| MAC | Media Access Control |
| MB | 1024KB |
| MCH | Memory Controller Hub |
| MD2 | Message Digest 2 – Hashing Algorithm |
| MD5 | Message Digest 5 – Hashing Algorithm – Higher Security |
| ms | milliseconds |
| MTTR | Memory Type Range Register |
| Mux | Multiplexor |
| NIC | Network Interface Controller |
| NMI | Nonmaskable Interrupt |
| OBF | Output Buffer |
| OEM | Original Equipment Manufacturer |
| Ohm | Unit of electrical resistance |
| PEF | Platform Event Filtering |
| PEP | Platform Event Paging |
| PIA | Platform Information Area (This feature configures the firmware for the platform hardware) |
| PLD | Programmable Logic Device |
| PMI | Platform Management Interrupt |
| POST | Power-On Self Test |
| PSMI | Power Supply Management Interface |
| PWM | Pulse-Width Modulation |
| RAM | Random Access Memory |
| RASUM | Reliability, Availability, Serviceability, Usability, and Manageability |
| RISC | Reduced Instruction Set Computing |
| RMM2 | Remote Management Module – 2nd generation |
| RMM2 NIC | Remote Management Module – 2nd generation dedicated management NIC |
| ROM | Read Only Memory |
| RTC | Real-Time Clock (Component of ICH peripheral chip on the server board) |
| SDR | Sensor Data Record |
| SECC | Single Edge Connector Cartridge |
| SEEPROM | Serial Electrically Erasable Programmable Read-Only Memory |
| SEL | System Event Log |
| SIO | Server Input/Output |
| SMI | Server Management Interrupt (SMI is the highest priority nonmaskable interrupt) |
| SMM | Server Management Mode |
| SMS | Server Management Software |
| SNMP | Simple Network Management Protocol |
| TBD | To Be Determined |
| TIM | Thermal Interface Material |
| UART | Universal Asynchronous Receiver/Transmitter |
| UDP | User Datagram Protocol |
| UHCI | Universal Host Controller Interface |
| UTC | Universal time coordinate |
| VID | Voltage Identification |

| Term | Definition |
|---|---|
| VRD | Voltage Regulator Down |
| Word | 16-bit quantity |
| ZIF | Zero Insertion Force |

# Reference Documents

Refer to the following documents for additional information:

*Intel® Dynamic PowerTechnology Node Manager 1.5 External Interface Specification using IPMI, 2007*. Intel Corporation.

*Node Power and Thermal Management Architecture Specification v1.5, rev.0.79. 2007*, Intel Corporation.

*Intel® Server System Integrated Baseboard Management Controller Core External Product Specification, 2007 Intel* Corporation.

*Intel® Thurley Server Platform Services IPMI Commands Specification, 2007.* Intel Corporation.

*Intelligent Platform Management Bus Communications Protocol Specification, Version 1.0, 1998*. Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation.

*Platform Environmental Control Interface (PECI) Specification, Version 2.0*. Intel Corporation

*Platform Management FRU Information Storage Definition, Version 1.0, Revision 1.2, 2002.* Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation. http://developer.intel.com/design/servers/ipmi/spec.htm

ACPI 3.0: http://www.acpi.info/spec.htm

IPMI 2.0

*Data Center Management Interface Specification v1.0*, May 1, 2008.: www.intel.com/go/dcmi

*PCI Bus Power Management Interface Specification 1.1*: http://www.pcisig.com/

*PCI Express* Base Specification Rev 2.0* Dec06: http://www.pcisig.com/

*PCI Express* Card Electromechanical Specification Rev 2.0*: http://www.pcisig.com/

PMBus*: http://pmbus.org

SATA 2.6: http://www.sata-io.org/

SMBIOS 2.4

SSI-EEB 3.0: http://www.ssiforum.org

USB 1.1: http://www.usb.org

USB 2.0: http://www.usb.org

Microsoft Windows* Logo/SDG 3.0