

Intel[®] Server Platforms SR6850HW4/M

Technical Product Specification

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Revision History

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| May 2005 | 1.0 | Initial release. |
| October 2005 1.1 Updated for Intel® Server Platform SR6850HW4/M support. | | |
| April 2006 | 1.2 | Updated for SAS (Serial Attach SCSI) support. |

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1. Product Overview

This product specification details the features of the Intel[®] Server Platforms SR6850HW4 and SR6850HW4/M. Reliability, low cost, time to market, modularity, high performance, and management features are primary considerations in the design.

The Intel® Server Platforms SR6850HW4 and SR6850HW4/M support up to four Dual-Core Intel® Xeon® Processors 7000 sequence or four 64-bit Intel® Xeon® Processors MP with up to 8MB L3 cache and incorporate features that clearly differentiate them as high availability server platforms. Building on previous server platforms, the Intel® Server Platforms SR6850HW4 and SR6850HW4/M introduce redundant memory and networking in addition to the enterprise features of hot-swap power, cooling, PCI slots, and hard disk drives. Advanced server management features are also included to remotely monitor and manage the server. Finally, the server has two optional mass storage expansion features. Throughout this specification, the generic term server platform is used to indicate both or either of the Intel® Server Platforms SR6850HW4 and SR6850HW4/M, unless otherwise noted.

This document is organized into eleven sections:

Section 1: Product Overview

An overview of this document.

Section 2: System Overview

An overview of the system hardware.

Section 3: System Chassis and Sub-Assemblies

An overview of the chassis and major sub-assemblies.

Section 4: Cables and Connectors

Describes the cables and connectors specific to the server platform.

Section 5: Power Supply

Describes the power supplies used in the server platform.

Section 6: Power Distribution Board

Describes the power distribution board used in the server platform.

Section 7: SCSI Backplane Board

Describes the SCSI backplane board used in the server platform.

Section 8: SAS Backplane Board

Describes the SAS backplane board used in the server platform.

Section 9: Front Panel I/O and Control Boards

Describes the front panel I/O board and control boards used in the server platform.

Section 10: SATA-to-IDE Converter Boards

Describes the SATA-to-IDE converter board used in the server platform.

Section Error! Reference source not found.: **Regulatory Specifications** Describes system compliance to regulatory specifications.

2. System Overview

This section describes the features of the Intel® Server Platforms SR6850HW4 and SR6850HW4/M.

2.1 System Feature Overview

Table 1 provides a list and brief description of the features of the Intel® Server Platforms SR6850HW4 and SR6850HW4/M, which utilize either the Intel® Server Board Set SE8500HW4 or Intel® Server Board Set SE8501HW4.

Table 1. Server Platform Feature List

| Feature | Description |
|------------------------------|--|
| Compact, high-density system | Rack-mount server with a height of 6U (10.5 inches) and a depth of 28 inches (706mm) |
| Configuration flexibility | One to four Intel® Xeon® processors MP with up to 8MB L3 cache, or |
| | One to four Dual-Core Intel® Xeon® processors 7000 sequence |
| | Two Ultra320* SCSI ports |
| | Two gigabit Ethernet ports |
| | Ten 1-inch hot-swap Ultra320* SCSI hard disk drives |
| | Seven PCI adapters (Four PCI Express* hot-plug, one PCI-X* 133MHz hot-plug, two PCI-X* 100Mhz) |
| | 64GB Double Data Rate2 (DDR2) 400 MHz Synchronous Dynamic Random Access Memory (SDRAM), ECC Registered |
| | Customizable bezel |
| | Optional system-specific 2Gbps Fibre Channel Module |
| | Optional RAID On Motherboard (ROMB) with DDR2 DIMM for disk cache and optional RAID Smart Battery (RSB) for cache battery backup |
| | Either button or LCD front panel |
| | Either Intel [®] Management Module – Advanced Edition or Intel [®] Management Module – Professional Edition |
| Serviceability | Tool-less design features |
| | Front access to hot-swap hard disk drives |
| | Top access to hot-plug PCI slots, cooling, and Hot-Swap Memory Boards |
| | Rear access to hot-swap power supplies |
| | Status and fault indicator LEDs |
| | Front and rear viewable System ID switches and LEDs |
| | Top viewable memory configuration and status LEDs |
| | Processor failure LEDs |
| | Detailed configuration label on top cover |
| | Color-coded parts to identify hot-swap and non-hot-swap serviceable components |
| Availability | Two 1570W power supplies in a redundant (1+1) configuration with separate power cords |
| | Four Hot-Plug Memory Boards |
| Manageability | Remote management |
| | Intelligent Platform Management Interface (IPMI) 2.0 compliant |
| | Wired For Management (WfM) 2.0 compliant |

| Feature | Description | | |
|-----------------------|---|---|--|
| | Emergency Management Port (EMP) – IPMI over serial or modem | | |
| | Extensive system sensors and monitoring | | |
| | Remote diagnostics support via serial and LAN ports | | |
| | Web management console | | |
| | With Intel® Management Module - Advanced Edition: | | |
| | Dedicated out-of-band management RJ45 port (telnet, embedded web server, DNS, DHCP) | | |
| | KVM console redirection and remote viewer | | |
| | Full SNMP access | | |
| Front panel interface | Switches: Power, Reset, NMI, System ID | LEDs: Power, System ID, System status, LAN1 and LAN2 Activity, Hard drives status | |
| | Ports: Video connector, Three USB 2.0 | Optional LCD | |

2.2 Introduction

The platform supports sockets for up to four 64-bit Intel® Xeon® Processors MP or Dual-Core Intel® Xeon® processors 7000 sequence, and up to 64GB of memory, ten hot-swap hard disk drives, seven PCI slots, two different server management modules, two different front control panels, and two optional mass storage expansions. The server can be configured for rack mounting, as shipped, or in a pedestal configuration, with an optional accessory kit.

Figure 1, Figure 2 and Figure 3 show front and rear views of the platform.

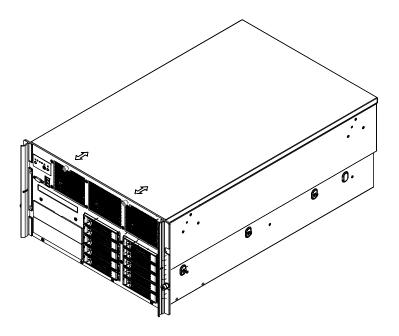


Figure 1. Isometric View of Server Platform with Bezel Removed

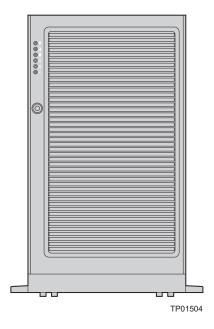


Figure 2. Front View of Server Platform with Bezel and Pedestal Conversion Kit Installed

The Intel® Server Platforms SR6850HW4 and SR6850HW4/M include the Intel® Server Board Sets SE8500HW4 and SE8501HW4 respectively, and each with the respective Intel® E8500 and E8501 chipset. To provide structural support the platforms' mainboard is mounted on a sheet metal tray that is installed at the rear of the chassis, above the power supplies.

Up to four memory boards can be installed with the Intel® Server Board Set SE8501HW4 mainboard. The memory boards attach perpendicular to the mainboard. These contain four DDR2 400HMz SDRAM DIMM slots each. With four memory boards installed, the system supports up to 64GB of memory (using 4GB DIMMs).

The hard drive bay, located at the front of platform, provides a bay for ten hot-swap 1-inch Ultra320* SCSI hard disk drives. SCSI hard disk drives plug into a vertical SCSI Backplane Board at the rear of hard disk drive bay. One Slimline* (½-inch high) optical drive bay and one full-height 5¼-inch SCSI tape device bay are also located at the front of the platform.

The cooling subsystem requires six hot-swap system fan modules. Each fan module contains a status LED that illuminates in the event of a fan failure. The fan modules are accessible from the top of the system when the top cover is removed and connected into the SCSI backplane board.

The front control panel provides video, USB, buttons, status LEDs, and an optional LCD, that are used for monitoring and managing the platform. The front bezel is an optional cosmetic accessory that is installed with snap-on features. The bezel can be customized to meet integrator-specific industrial design requirements, including color and imprint.

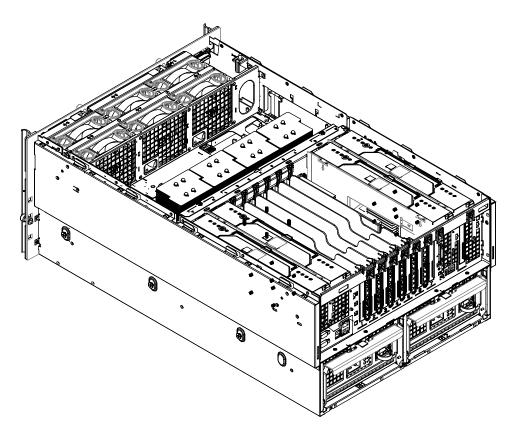


Figure 3. Server Platform, Isometric Rear View with Top Cover Removed

The power supply modules are located at the rear of the system below the Intel[®] Server Board Set SE8501HW4 mainboard and plug directly into connectors on the horizontally oriented Power Distribution Board. The system supports two hot-swap power supply modules in a 1+1 redundant configuration or one hot-swap power supply and a power bay fan module in a non-redundant state.

Upon removal of the top cover, the user has access to the processors, memory boards, PCI adapters, Intel[®] Management Module board, and optional mass storage features.

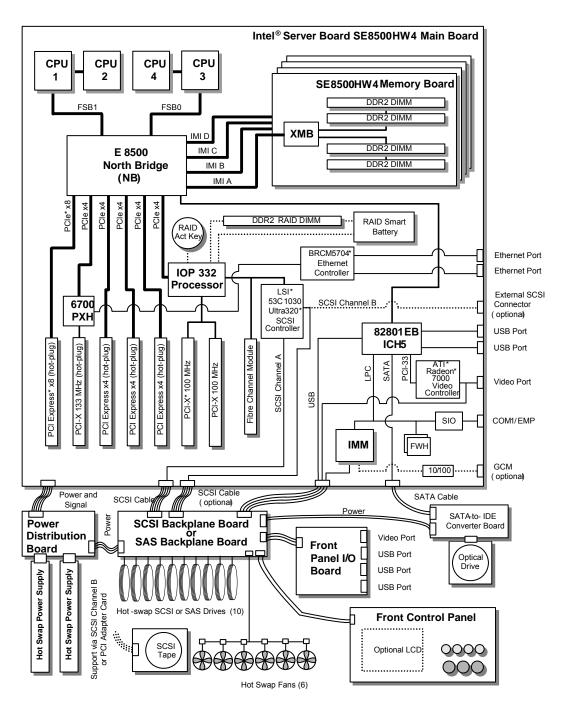


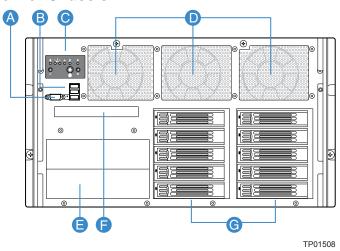
Figure 4. Server Platform Chassis Block Diagram

2.3 External Chassis Features - Front

Figure 5 shows the front view of the platforms with the bezel removed. The front provides access to the following components:

- Buttons and LEDs (with optional LCD)
- Video and USB connectors
- Hard drive bay, optical drive, SCSI tape device

2.3.1 Front View of Chassis



| Item | Description | |
|------|--|--|
| Α | Video connector | |
| В | USB 2.0 ports (three) | |
| С | Front control panel (button control panel shown) | |
| D | Hot-swap fans (six) | |
| Е | 5 ¼ peripheral bay (full height) | |
| F | Optical drive bay | |
| G | Hot-swap SCSI hard disk drives (ten) | |

Figure 5. Front View of Server Platform, Bezel Removed

2.3.2 Front Control Panel

The front control panel contains system control buttons and LED status indicators. It also contains one video connector, three USB 2.0 ports, NMI button, and the system speaker. The front bezel must be removed to access the front control panel switches and connectors. All LEDs are visible with the front bezel installed. See Section 8 or a description of the front panel boards.

2.3.3 Hot-swap Hard Disk Drive and Peripheral Device Bays

The hard disk drive and peripheral device bays can accommodate the following devices:

- Ten 1-inch hot-swap Ultra320* SCSI hard disk drives
- One ½-inch optical drive (installed with base system)
- Two half-height or one full-height 5¼-inch SCSI tape device

Note: Cooling and EMI constraints do not allow installation of an IDE hard disk drive in the tape device bay.

The SCSI backplane board supports Low Voltage Differential (LVD) SCSI drives only. Single-Ended (SE) devices are supported off the secondary external SCSI channel on the Intel[®] Server Board Set SE8501HW4 mainboard. SE devices are not supported in the hot-swap hard disk drive bays in the front of the system, or validated by Intel.

The optical drive and SCSI tape device(s) are not hot-swap devices. System power must be turned off when installing or removing these drives. The drive bay depths limit the physical size of the drive depth to approximately 12 inches in the upper drive bay and 9.45 inches in the lower drive bay. Some cables may require to be gently repositioned to create unobstructed clearance. For the lower drive bay, use care if the stiff power cable requires adjustment to not overstress the connector ends.

Because hard disk drives have different cooling, power, and vibration characteristics, Intel will validate specific hard disk drive types in the platforms. See the *Intel*[®] *Server Board Set SE8501HW4 Tested Hardware and Operating System List* and the *Intel*[®] *Server Board Set SE8500HW4 Tested Hardware and Operating System List* for the qualified drives.

The hard disk drive carriers supplied with the system accommodate 3½-inch x 1-inch SCSI hard disk drives. The hard disk drive is attached to the carrier with four Phillips*-head screws. The carrier is retained in the chassis by a locking handle.

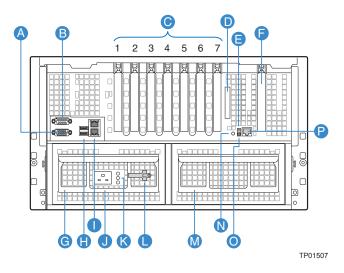
The SCSI backplane board contains a dual color LED for each hard drive to display status. The LED signal is transmitted to the front of the system via a light pipe integrated in the hard drive carrier.

Due to the required cable length and bus performance, the Intel® Server Board Set SE8501HW4 mainboard contains a Serial ATA (SATA) connecter instead of a Parallel ATA (PATA) connector. The optical drive connects to the SATA-to-IDE converter board, which converts the SATA signal to an IDE signal for the 1/2-inch optical drive. The optical drive is installed in a sheet metal bracket and then installed in the platforms.

See Section 7 for a description of the SCSI backplane board. See Section 10 for descriptions of the SATA-to-IDE converter board.

2.4 External Chassis Features - Rear

Figure 6 shows the rear view of the platforms. The user-accessible connectors, PCI slots, and power supply modules located at the rear of the system are described in the following sections.



| Item | Description | | |
|------|--|--|--|
| Α | Video connector | | |
| В | Serial port connector | | |
| С | PCI slots | | |
| | Slot 1 PCI Express* x8 (hot-plug) | | |
| | Slot 2 PCI-X* 133Mhz, 64-bit (hot-plug) | | |
| | Slot 3 PCI Express x4 (hot-plug) | | |
| | Slot 4 PCI Express* x4 (hot-plug) | | |
| | Slot 5 PCI Express* x4 (hot-plug) | | |
| | Slot 6 PCI-X* 100Mhz, 64-bit (not hot-plug) | | |
| | Slot 7 PCI-X* 100Mhz, 64-bit (not hot-plug) | | |
| D | External SCSI connector | | |
| E | System ID LED (blue) | | |
| F | Fibre Channel Module slot (optional accessory) | | |
| G | Power supply unit | | |
| Н | USB 2.0 ports (two) | | |
| I | LAN ports, RJ45 connector (LAN1 on top, LAN2 on bottom) | | |
| J | AC input power connector (C19, IEC-32) | | |
| K | Power supply unit status LEDs | | |
| L | Power cord retention featurek | | |
| M | Active fan power supply blank | | |
| N | System ID button | | |
| 0 | DC jack (Not used) | | |
| Р | Dedicated server management port, RJ45 connector (used with the Intel® Management Module - Advanced) | | |

Figure 6. Rear View of the Intel® Server Platforms SR6850HW4 and SR6850HW4/M

2.5 Internal Chassis Features

2.5.1 Intel® Server Board Set SE8501HW4 Mainboard

The Intel® Server Board Set SE8501HW4 mainboard supports the following features:

- Four sockets for Dual-Core Intel[®] Xeon[®] processors 7000 sequence or 64-bit Intel[®] Xeon[®] processors MP with up to 8MB L3 cache
- Four PCI Express* x16 memory board connectors
 - Four independent memory interface buses
 - Supports hot-remove and hot-add operations
- Dual 800 MT/s Front Side Buses (FSB) for Intel® Server Board Set SE8501HW4 Mainboard
- Dual 667 MT/s Front Side Buses (FSB) for Intel® Server Board Set SE8500HW4 Mainboard
- Intel[®] E8500 chipset North Bridge (NB) with two shared 64-bit FSB interfaces configured for symmetric multiprocessing (SMP)
- Intel[®] E8500 chipset eXtended Memory Bridge (XMB) for support of memory hot-plug
- Intel[®] 6700 PXH 64-bit Hub which acts as the bridge between the NB and PCI-X* bus
- Intel® 82801EB I/O Controller Hub 5 (ICH5) which provides USB 2.0 and SATA
- Intel[®] IOP332 storage I/O Processor for mass storage and PCI-X* slots
- LSI Logic* 53C1030 Ultra320* SCSI Controller: provides two independent Ultra320* SCSI interfaces
- Broadcom* BRCM5704 NetXtreme* Gigabit Ethernet controller: provides two ports on the rear of the Mainboard
- ATI Radeon* 7000 video controller
 - 16MB embedded SDRAM
 - Mirrored to both the rear and front I/O ports by default
- Advanced I/O slots including PCI Express* and PCI-X* and support circuits:
 - One hot-plug PCI Express* x8 slot
 - Three hot-plug PCI Express* x4 slots
 - One hot-plug 64-bit PCI-X* 133MHz slot
 - Two 64-bit PCI-X* 100MHz slots (not hot-plug)
- Buttons and LED indicators for PCI hot-plug slots
- Low-pin Count (LPC) Super I/O* enables the serial port/EMP
- USB 2.0 support
 - Two ports at the rear of chassis
 - Three ports on front of the chassis
- 4MB Flash capacity to support rolling BIOS updates
- Optional ROMB support: provides two channels of RAID 0, 1, 5, 10 or 50 (SCSI ROMB)
- Optional custom Fibre Channel Module: provides two optical connectors
- Server management support via the Intel[®] Management Module connector

See the Intel[®] Server Board Set SE8501HW4 Technical Product Specification for a description of this board.

2.5.2 Intel[®] Server Board Set SE8501HW4 Memory Board

Each memory board supports the following features:

- PCI Express* x16 card edge connector that plugs into the Intel[®] Server Board Set SE8501HW4 mainboard
- Intel[®] E8501 chipset eXtended Memory Bridge (XMB)
 - Four DDR2 400HMz DIMM slots for registered ECC memory
 - Support for both single-rank and dual-rank DIMMs
 - Two DDR2 400MT/s buses
 - Independent Memory Interface (IMI), a high-speed differential bus
 - LED error indicators for each DIMM and an attention LED for hot-plug events
 - LED indicator for both memory mirroring and RAID configurations
- Memory hot-plug at the card level, based on the PCI hot-plug model
 - Field Replaceable Unit (FRU) device
 - Two temperature sensors
- Safety mechanism for instant power shut-down to the memory board when not properly removed or inserted

Memory boards labeled 667/800 support processors of both Front Side Bus speeds, 667MT/S and 800MT/S. The memory boards not labeled only support 667MT/S. See the *Intel® Server Board Set SE8501HW4 Technical Product Specification* for descriptions of this board.

2.5.3 Power Distribution Board

The Power Distribution Board is located horizontally, below the Intel® Server Board Set SE8501HW4 mainboard in the middle-rear of the chassis. It has two connectors for the hot-swap power supply modules and provides 12V, standby power and server management signals to the Intel® Server Board Set SE8501HW4 mainboard and SCSI backplane board. The power distribution circuitry reports quantity, quality, and location of the installed power supplies through I²C server management. See Section 6 for a description of this board.

2.5.4 SCSI Backplane Board

The SCSI backplane board mounts vertically in the front of the system and contains ten industry-standard hot-swap Single Connector Attach 2 (SCA-2) connectors (80-pin). Ultra320* (or slower) Low Voltage Differential (LVD) SCSI hard disk drives can be installed in the system. The backplane accepts 15,000-RPM (and slower) hard disk drives. Single-Ended (SE) SCSI devices are not supported in the hot-swap hard disk drive bay.

The SCSI backplane board performs the tasks associated with hot-swapping of the hard disk drives and enclosure (chassis) monitoring and management, as specified in the SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification. The SAF-TE-specified features supported by the SCSI backplane board include, but are not limited to, the following:

- Monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages are as follows: activate a drive fault indicator; power down a drive that has failed; and report backplane temperature.
- SAF-TE intelligent agent acts as proxy for "dumb" I²C devices (that have no bus mastering capability) during intrachassis communications.

The SCSI backplane board connects to the Intel® Server Board Set SE8501HW4 mainboard, provides power, and signals to the front of the chassis. See Section 7 for a description of this board.

2.5.5 Front Panel I/O Board

The Front Panel I/O Board mounts horizontally in the front left of the system and communicates with the SCSI backplane board. The board contains a video connector, three USB ports and an NMI button. See Section 8 for a description of this board.

2.5.6 Front Panel Control Board

Two different front panel control boards are supported, the standard control panel and the Intel[®] Local Control Panel (iLCP). Both mount vertically into the chassis and connect to the front panel I/O board via a cable. Each module houses the system operating buttons, LEDs and the Intel[®] Local Control Panel has an iLCD. See Section 8 for a description of these boards.

2.5.7 SATA-to-IDE Converter Board

The SATA-to-IDE converter board attaches to the optical drive carrier, receives the SATA signal from the Intel® Server Board Set SE8501HW4 mainboard via a SATA cable, and converts it to IDE signals routed to the optical drive. See Section 10 for a description of this board.

2.5.8 Intel[®] Management Module

The Intel® Management Module mounts onto the Intel® Server Board Set SE8501HW4 mainboard and contains the Baseboard Management Controller (BMC) that provides server management support. There are two versions, the Intel® Management Module - Professional Edition and the Intel® Management Module - Advanced Edition. The Intel® Management Module - Advanced Edition adds more support for remote management. The platforms will not boot without one of these modules installed. See the Intel® Management Module Installation and User's Guide or the Intel® Management Module Technical Product Specification for a description of this part.

2.5.9 Fibre Channel Module

The Intel® Server Board Set SE8501HW4 mainboard supports the Intel® Fibre Channel Module as a mass storage expansion option. The card is based on the Qlogic* ISP2322 FC PCI-X* controller and plugs into a reversed PCI Express* x16 slot on the Intel® Server Board Set SE8501HW4 mainboard. See the Intel® Fibre Channel Module User's Guide for descriptions of this board.

2.5.10 RAID On Motherboard (ROMB)

The Intel® Server Board Set SE8501HW4 mainboard supports a RAID On Motherboard (ROMB) solution via the Intel® IOP332 I/O Processor in conjunction with the LSI Logic* 53C1030 SCSI controller. To enable this option the Intel® RAID Activation Key and a DDR2-400 MHz DIMM are required. The optional Intel® RAID Smart Battery is also available to maintain the contents of the DIMM in the event of power loss.

2.5.11 Intel[®] Integrated Server RAID Adapter SROMBSAS18e

The Intel® Integrated Server RAID Adapter SROMBSAS18e is an add-in SAS ROMB card available only for the SAS models of the Intel® Server Platforms SR4850HW4/M, and SR6850HW4/M. The Adapter has three modes.

- Native SAS (including SATA) mode with support for up to 120 drives via expander support.
- Intel® Integrated Server RAID providing intelligent RAID 0,1,5,10,50 (with future RAID 6 support) by the addition of the AXXRAK18E and RAM.

Note: This card is specially hardware keyed which restricts it to PCI-Express* slot 3, 4, or 5 for proper operation.

The SROMBSAS18e card includes

- Four external SAS/SATA ports (via a SFF8470 connector)
- Four internal SAS/SATA ports (via a SFF8086/7compact wide connector)
- Data throughput capabilities up to 3.0 Gbps via point to point links
- One DDRII DIMM socket capable of supporting up to 1 GB of registered ECC 400MHz SDRAM.
- An iButton* socket to hold the add in key to enable hardware Intel[®] Integrated Server
- A buzzer to provide audible warnings.
- A battery cable header from the optional Intel® RAID Smart Battery (RSB) which provides power to the RAM cache in case of AC power failure.
- The LSI* 1068 SAS controller providing firmware, watchdog timer, and connection to both the I²C and PCI-Express* bus.
- The Intel[®] IOP333 I/O controller provides offloading of RAID calculations from the CPU.
- Support for enclosure management through the I²C bus.
- Cascaded power conversion from the PCI rail to the required voltages of the card components.

2.5.12 Power Supply Module

Two hot-swap power supply modules are installed side by side at the rear of the chassis. Each supply has its own AC input power connector and is rated at 1570W over an input range of 100-240 VAC.

The power subsystem is configured as follows:

- With two power supply modules installed, a fully configured system has (1+1) power redundancy.
- With one supply module installed, the system does not have redundant power but will still run a fully configured system.

Note: When only one power supply module is installed, the active fan module is required in the unpopulated power supply slot for proper system cooling.

One power supply module is capable of handling the maximum power requirements for fully configured platforms, which includes four processors, 64 GB of memory, seven PCI add-in cards, ten hot-swap hard disk drives, an optical drive, a Fibre Channel Module, ROMB options installed, and a SCSI tape device.

When two power supply modules are installed, the user can replace a failed power supply module without affecting the system functionality. Power supplies have three LEDs to identify failure, power good and AC OK.

The power subsystem receives AC power through two power cords. When two power supply modules and two power cords are installed, the system has (1+1) power cord redundancy and can be powered by two separate AC sources. In this configuration, the system will continue to function without interruption if one of the AC sources fails. See Section 5 for more information.

Note: The total power requirement for the platforms exceeds the 240 VA energy hazard limits that define an operator accessible area. As a result, only qualified technical individuals should access the processor and non-hot-plug I/O areas while the system is energized. Power cords should be removed from the system before accessing non-hot-plug areas.

2.5.12.1 System Power Budget

The table below shows a summary of the system power budget. The power budget lists each major voltage rail in columns and each major subsystem of the product in rows. The worst-case power per subsystem is listed for each voltage rail. The total power per voltage rail, the power supply specification, and the margin available are shown at the bottom of the table.

| Subsystem | Quantity | +3.3V | +5V | +12V (Total) | +3.3V _{stby} |
|---------------------------------------|----------|-------|------|--------------|-----------------------|
| Mainboard | 1 | 49W | 27W | 147W | 15W |
| SCSI backplane board Board | 1 | | 2.5W | 2.5W | |
| Front Panel I/O Board and front panel | 1ea | 2W | | 2W | |
| Processors | 4 | | | 448W | |
| Memory | 16 | 4W | | 192W | |
| Fans | 6 | | | 173W | |
| Hard disk drives | 10 | | 28W | 84W | |
| ½ inch optical drive | 1 | | 1W | 6W | |
| SCSI tape device | 1 | | 3W | 7W | |
| PCI-X* slots | 3 | | | 45W | |
| PCI Express* slots | 4 | | | 80W | |
| Fibre channel module | 1 | | | 15W | |
| System Total | | | | 1189.5W | 15W |
| Power subsystem spec | | | | 1570W | 16.5W |
| Margin | | | | 380.5W | 1.5W |

Table 2. System Power Budget

Notes:

- 1. 3.3V and 5V are derived from the 12V single switched output of the power supply modules. The 12V column includes the 3.3V and 5V power.
- 2. 3.3V_{stby} is the standby output of the power supply modules.

2.5.13 Cooling Subsystem

Primary cooling is generated by six fans, located at the top front of the chassis. It connects to the SCSI backplane board for power and server management. Air flows in through the front and exhausts out the rear of the chassis. The chassis has several air baffles to duct the air over critical parts, including processors, memory, and peripherals. Processor heat sinks or processor heat sink blanks, and memory boards or memory board blanks must be installed in each corresponding area to ensure proper airflow.

The system fans are sized to provide cooling for a fully configured system. The cooling system is designed using a worst-case analysis and appropriate fan speeds were chosen to meet acoustic and thermal requirements. Server management controls fan speed based on ambient and component temperatures. To ensure proper cooling, failed fans should be replaced within 1 minute.

2.6 New Platform Features

2.6.1 Advanced Memory Performance and Protection

The Intel® Server Board Set SE8501HW4 supports several new memory features that allow flexibility in performance, redundancy and the ability to upgrade. The System BIOS can be configured as follows:

- Maximum performance, where memory is up to four-way interleaved
- Maximum compatibility, where memory can be hot-added
- Memory mirroring, where two or four boards are used to keep a copy of system memory
- Memory RAID, where four boards are used in a RAID4-like mode
- Memory sparing, where a portion of each memory board is reserved for failover.

Hot-replace means the user can replace a memory board with another memory board of identical total size. This operation is supported in maximum compatibility, memory RAID and memory mirroring modes.

Hot-add means the user can add a memory board to a previously unoccupied slot. This requires operating system support and is supported in memory compatibility and memory mirroring modes.

Hot-removal means the user can remove a memory board. This operation is supported in memory RAID and memory mirroring modes.

Hot upgrade means the user can replace an existing memory board with a memory board that contains more memory capacity. A hot upgrade is not a unique operation, it is implemented as a hot-remove followed by a hot-add. This requires operating system support and is supported by the memory RAID mode only.

See the Intel[®] Server Board Set SE8501HW4 Technical Product Specification for more details on these new features.

2.6.2 Rolling BIOS

The Intel® Server Board Set SE8501HW4 mainboard supports two BIOS images to be stored in Flash. This provides a mechanism for BIOS updates without a system reboot as well as failover to an alternate image in the event of BIOS corruption. The system runs with the current BIOS until a reboot, after which time the updated BIOS is used. See the *Intel® Server Board Set SE8501HW4 Technical Product Specification* for more details on this feature.

2.7 Server Management

The management subsystem conforms to the *IPMI v2.0 Specification*. The server management features are implemented using two microcontrollers: the Intel® Management Module that plugs into the Intel® Server Board Set SE8501HW4 mainboard, and the SCSI hot-swap controller on the SCSI backplane board. The functions of each component are summarized in the following sections.

2.7.1 Intel[®] Management Module

The Intel® Management Module has a Baseboard Management Controller (BMC) microcontroller and associated circuitry. The Intel® Management Module contains flash memory that holds the operation code and the BMC configuration settings. The Intel® Management Module monitors platform management events and logs their occurrence on the onboard non-volatile System Event Log (SEL). This includes events such as over-temperature and over-voltage conditions, fan failures, etcetra The Intel® Management Module also provides the interface to this monitored information so system management software can poll and retrieve the present status of the platform.

The Intel® Management Module also provides the interface to the non-volatile Sensor Data Record (SDR) repository. SDRs provide a set of information that system management software can use to automatically configure itself for the number and type of IPMI sensors (e.g., temperature sensors, voltage sensors, etcetra) in the system.

The following is a list of the major functions for the Intel[®] Management Module:

- System power control
 - ACPI power control
 - ACPI sleep support
 - Minimum power off time
- System reset control
- System initialization
 - Processor temperature and voltage threshold setting
 - Fault Resilient Booting (FRB)
- Front panel user interface
 - System status (green) LED control
 - System status (amber) LED control
 - System ID LED control
 - Reset button control
 - Power button control
 - SDINT button control
 - System ID Button control
- System fan management
- System management watchdog timer
- System Event Log (SEL) interface up to 3,200 entries

- Sensor Data Record (SDR) repository interface
- SDR/SEL timestamp clock
- FRU inventory device
- Diagnostics and beep code generation
- Event message generation and reception
- Platform Event Paging and Platform Event Filtering (PEP and PEF)
- Dial page alerting
- Alert over LAN and serial/PPP
- Serial over LAN (SOL)
- Terminal Mode (TM)
- Battery monitoring
- Sensor monitoring
 - Temperature
 - Voltage
 - Fan speed
 - Processor status
 - Power supplies
- Processor Information ROM (PIROM) and Scratch Electrically Erasable Programmable ROM (SEEPROM) access
- IPMB communication interface
- Emergency Management Port (EMP) interface IPMI messaging over Serial/Modem.
 This feature is also referred to as DPC (Direct Platform Control) over Serial/Modem
- Inter-Chassis Management Bus (ICMB) interface IPMI messaging between chassis
- Additional features with Intel[®] Management Module Advanced Edition installed:
 - Dedicated (Out-Of-Band) LAN interface through the Generic Communication Module (GCM) on the rear of chassis (Intel[®] Management Module – Advanced Edition)
 - BMC-resident SNMP support for Out-Of-Band access using third party applications such as HP* Openview*
 - Embedded web server to access system health, view the SEL and issue IPMI commands
 - Embedded Command Line Interface (using telnet server running on the BMC) to allow direct access to the BMC
 - Alerting via email
 - Keyboard, Video, Mouse (KVM) console redirection and remote viewer

See the Intel® Management Module Technical Product Specification for more information.

2.7.2 Hot-swap Controller

Two hot-swap controllers are on the SCSI backplane board. The primary function of each hot-swap controller is as follows:

- Implements the SAF-TE command set
- Controls the SCSI hard disk drive power, activity and fault LEDs
- Provides a path for management information via the SCSI bus
- Retrieves hard disk drive fault status, SCSI backplane board temperature, and fan failure information via IPMB
- Queries the status of the power distribution board by retrieving information from the Intel[®] Management Module via IPMB
- Controls hard disk drive power-on and power-down, facilitating hot-swapping

2.8 Reliability, Availability, Serviceability, Usability, Manageability (RASUM)

The platforms support the following reliability, availability, serviceability, usability and manageability (RASUM) features:

Reliability features

- Machine check architecture
- Error Checking Code (ECC) in main memory and processor caches
- ECC, parity, and protocol checking on the FSB
- Parity on the Hub Link (HL-1.5) interface
- Parity checking on PCI buses
- RAID On Motherboard (ROMB) with the Intel[®] RAID Smart Battery which provides battery back-up to the DDR2-400 MHz DIMM for disk cache
- Voltage and temperature monitoring throughout the system

Availability features

- Hot-plug PCI Express* and PCI-X*
- Hot-Plug memory boards
- Redundant hot-swap power supplies
- Redundant power cords
- Redundant hot-swap system fans
- Hot-swap SCSI hard drives
- Teaming and failover Ethernet ports

Serviceability features

- Tool-less installation and removal of major sub-assemblies
- Color-coded parts to identify serviceable components
 - Green: Hot-swap or hot-plug components
 - Blue: Non-hot-swap components
- System ID buttons and LEDs
- LED indicators for system health, configured options, and activity

Usability features

- Tool-less design features
- External access to hot-swap hard disk drives, power supplies, LEDs and switches
- Front and rear viewable System ID switches and LEDs
- Detailed configuration label on top cover
- Color-coded parts to identify hot-swap and non-hot-swap serviceable components

Manageability features

- Remote management via serial and LAN
- IPMI 2.0 and WfM 2.0 compliance
- Remote diagnostics via serial and LAN
- Remote management via KVM and dedicated LAN (Intel[®] Management Module Advanced Edition)

All boards are connected by a server management I²C bus to satisfy the system RASUM requirements.

2.9 Expansion Support

Table 3 summarizes the expansion support provided by the platform.

Table 3. Expansion Support

| Quantity | Туре |
|----------|--|
| 4 | Dual-Core Intel® Xeon® processors 7000 Sequence |
| 7 | PCI expansion bus slots |
| 10 | Single connector attachment (SCA-2) Ultra320* SCSI or SAS hard disk drive bays |
| 1 | 5 1/4-inch full-height drive bay |
| 1 | External SCSI connector |
| 16 | DDR2 400HMz SDRAM registered ECC DIMM module sockets (four per memory module) |
| 1 | SCSI RAID On MotherBoard (ROMB) socket, DDR2 DIMM socket and battery connector |
| 1 | Fibre Channel module connector (with two FCAL 2GBps connectors) |

2.10 Specifications

2.10.1 Environmental Specifications Summary

The platforms should be tested to the environmental specifications as indicated in Table 4.

Table 4. Environmental Specifications Summary

| Environment | Specification | | | |
|--|---|------------------|--|--|
| Temperature operating | 10°C to 35°C | 50°F to 95°F | | |
| Temperature non-operating | -40°C to 70°C | -40°F to 158°F | | |
| Altitude | -30 to 1,500 m | -100 to 5,000 ft | | |
| Humidity non-operating | 95%, non-condensing at temperatures of 25°C (77°F) to 30°C (86°F) | | | |
| Vibration non-operating | 2.2 Grms, 10 minutes per axis on each of the three axes | | | |
| Shock operating | Half-sine 2 G, 11 ms pulse, 100 pulses in each direction, on each of the three axes | | | |
| Shock non-operating | Trapezoidal, 25 G, two drops on each of six faces | | | |
| | V : 175 inches/sec on bottom face drop, 90 inches/sec on other 5 faces | | | |
| Safety | UL60 950, CSA60 950, AS/NZS 3562, GB4943-1995, EN60 950 and 73/23/EEC, IEC 60 950, EMKO-TSE (74-SEC) 207/94, GOST-R 50377-92 | | | |
| Emissions | Certified to FCC Class A; tested to CISPR 22 Class A, EN 55022 Class A and 89/336/EEC, VCCI Class A, AS/NZS 3548 Class A, ICES-003 Class A, GB9254-1998, MIC Notice 1997-42 Class A, GOST-R 29216-91 Class A, BSMI CNS13438 | | | |
| Immunity | Verified to comply with EN55024, CISPR 24, GB9254-1998, MIC Notice 1997-41, GOST-R 50628-95 | | | |
| Electrostatic discharge | Tested to ESD levels up to 15 kilovolts (kV) air discharge and up to 8 kV contact discharge without physical damage | | | |
| Acoustic | Sound pressure: < 55 dBA at ambient temperature < 23° C measured at bystander, floor standing position | | | |
| Sound power: < 7.0 BA at ambient temperature < 23° C measured using the Method | | | | |
| | GOST MsanPiN 001-96 | | | |

See Section **Error! Reference source not found.** for more information on environmental specifications.

2.10.2 Physical Specifications

Table 5 describes the physical specifications of the platforms.

Table 5. Physical Specifications

| Specification | Value | | | |
|----------------------|-------------|--------|--|--|
| Height – 6U | 10.5 inches | 262 mm | | |
| Width | 17.6 inches | 447 mm | | |
| Depth | 27.8 inches | 706 mm | | |
| Front clearance | 3 inches | 76 mm | | |
| Side clearance | 1 inch | 25 mm | | |
| Rear clearance | 6 inches | 152 mm | | |
| Weight (full config) | 130 lbs | 60 kg | | |

Note: The system weight is an estimate for a fully configured system and will vary depending on number of peripheral devices and add-in cards, and the number of processors and DIMMs installed in the system.

3. Server System Chassis and Assemblies

This section provides an overview of the chassis and assembly pieces that reside within the system. This section is divided into the following areas:

Section 3.1: Chassis, Rails and Top Cover

Section 3.2: Power and Fans

Section 3.3: Fan Subsystem

Section 3.4 Mainboard Assembly

Section 3.5: Peripherals Bay and Front Panel

Section 3.6: Front Bezel

3.1 Chassis, Rails and Top Cover

3.1.1 Chassis

The platforms utilize a standard 19-inch EIA chassis that is 6U high x 28 inches deep. The chassis can be rack-mounted or used as a pedestal system. Rack mounting the platform requires a 6U x 19 inches x 34 inches deep space, with the extra six inches required for cable management. When used in a rack, the chassis can be mounted with an optional rail kit and cable management arm. Pedestal operation requires a pedestal conversion kit that consists of a different bezel, floor supports/wheels and a cosmetic cover.

The 6U height is defined by standard EIA rack units where 1U = 1.75 inches. The 28-inch depth is measured from the front mounting flange to the back of the PCI slots. This measurement does not include cables or the bezel.

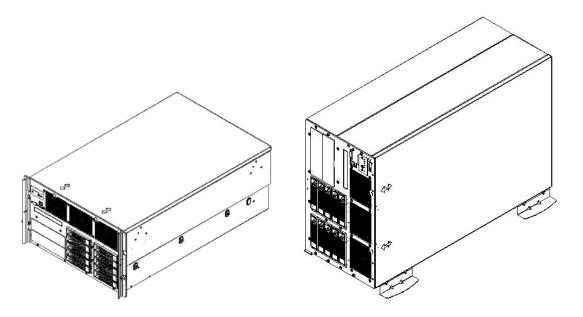


Figure 7. Server Platforms Rack and Pedestal Configurations, Bezel Removed

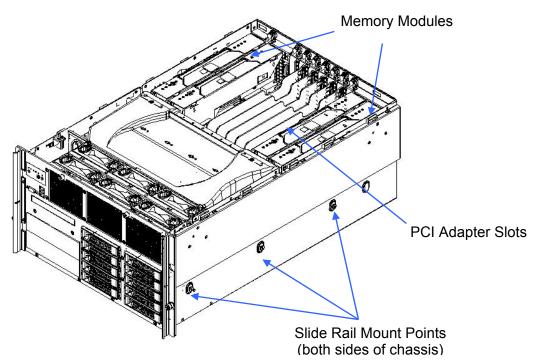


Figure 8. Server Platform, Bezel and Top Cover Removed

3.1.2 Slide Rails

The platforms accommodate slide rails to mount the chassis into a standard 19-inch rack. The slide rails attach to stude on the slides of the chassis using keyhole features on the slide rails. No loose hardware is needed. Intel produces two accessories common to enterprise servers:

- AXXRAIL3U7U, which attaches to the provided mounts, or any 3U to 7U server that has mounts in these locations
- AXXCMA3U7U, which attaches to the rail accessory to provide a cable management arm

3.1.3 Top Cover

The top cover is a one-piece design. It attaches to the chassis with a series of slots in the sides of the chassis that align with tabs in the top cover. To install the top cover, the tabs drop into the slots and the cover slides forward. Two captive non-knurled screws on the faceplate secure the top cover in place. A tool is required to remove or install these screws. In addition, the cover has a label on the bottom side that describes system layout, jumpers and a summary of common tasks.

3.2 Power and Fans

The power bay provides space for two power supply modules/blanks and for the Power Distribution Board. It is an integral member of the chassis structure. Each power supply in the power bay is approximately 7.7 inches (W) x 14.2 inches (D) x 4.1 inches (H). The redundant AC power inputs are external to the system.

The Power Distribution Board distributes the power in two ways. First, a connector on the back edge of the board mates to the power supplies. Second, a cable routes +12V power to the SCSI Backplane Board and +3.3V_{stby}, +12V power and signals to the Intel[®] Server Board Set SE8501HW4 mainboard. The AC power is filtered with a combination 15A power plug integrated with a filter.

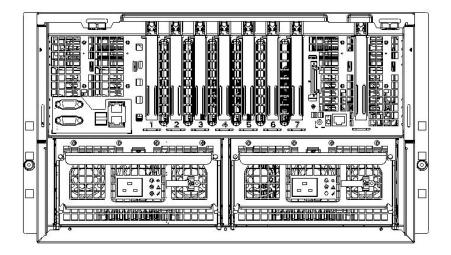
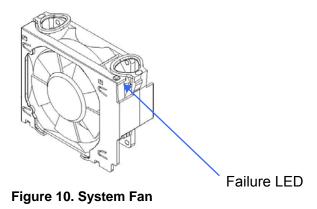


Figure 9. Rear of Server Platform, Power Supplies Installed

3.3 Fan Subsystem

The six system fans are accessible for hot-swap operations at the top of the chassis. The fan assembly has an integrated amber LED wired to the top of the assembly. This LED lights when the fan is not functioning within its specification. The fan connector extends from the bottom of the fan assembly and mates into floating connectors routed to the platforms SCSI backplane board.



3.4 Mainboard Assembly

The Intel® Server Board Set SE8501HW4 mainboard mounts to a sheet metal tray with four metal springs from the Intel Component Enabling Kit (CEK) and four non-captive screws. The Intel® Server Board Set SE8501HW4 mainboard assembly is mounted in the chassis with slot and tab hooks. It is secured into the chassis by a single captive fastener.

Memory boards mount vertically on the left and right side of the board however, processors and heat sinks mount in the front.

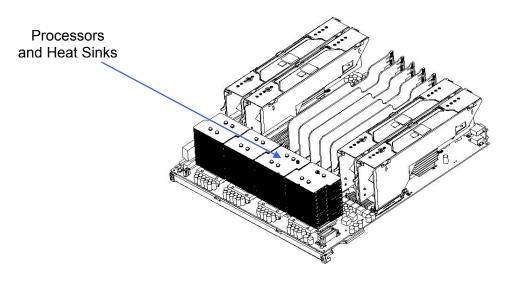


Figure 11. Mainboard and Sheet Metal Tray, Assembly

3.5 Peripheral Bay and Front Panel

The peripheral bay is a sheet metal enclosure with features to mount the hot-swap SCSI hard disk drives, 5½-inch device, and an optical drive. The SCSI backplane board has slots on it that slide into hooks on the peripheral bay. A plunger and captive thumbscrew secure the SCSI Backplane Board and Front Panel I/O Board to the peripheral bay.

3.5.1 Hot-Swap Hard Disk Drive Carrier

The hot-swap hard disk drive carrier is an assembly that provides guides for installing hard disk drives. The carrier has an integrated light pipe to transfer the LED indicator from the SCSI backplane board to the front of the drive carrier and an insertion/extraction mechanism. The hard drive bezel can be customized to meet integrator-specific industrial design requirements, by changing the color and imprint.

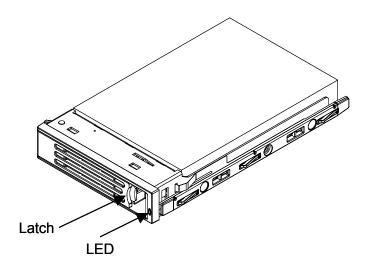


Figure 12. Hot-Swap Hard Drive Carrier

3.5.2 Optical Drive Carrier

The optical drive is installed in a sheet metal bracket. The SATA-to-IDE converter board is plugged into the IDE connector at the back of the optical device. This assembly is then installed into the chassis.

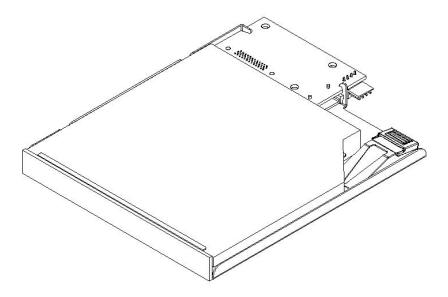


Figure 13. Optical Drive Carrier with SATA-to-IDE Converter Board

3.5.3 Front Panel

The server platforms require a standard button control panel, providing basic functionality, or an Intel[®] Local Control Panel, which adds an LCD for integration with server management features. Both front panels contain on/off buttons, switches and LED status indicators. The front panel is retained in the chassis by two clips and connects to the SCSI backplane via a cable.

The on/off button for these server platforms must be pushed in or triggered to power on the server from a powered off state. From a power on state, the on/off button needs to be held for approximately four continuous seconds in order to force a shutdown while running a fully booted OS. Without OS control the momentary triggering of the on/off button may transition the server platform to the off state.

In the upper left of the chassis front, there is also a video connector, NMI button, and three-port USB 2.0 connector.

See Section 9 for more information on the front panel area.

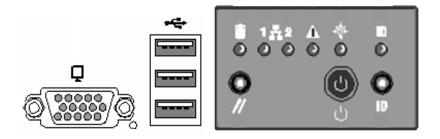


Figure 14. Front Panel with Button Control Panel

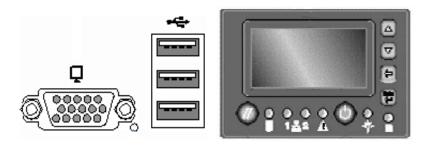


Figure 15. Front Panel with Intel[®] Local Control Panel

3.6 Front Bezel

The front bezel is an optional one-piece cosmetic accessory that is installed with snap-on features. The bezel can be customized to meet integrator-specific industrial design requirements, by changing the color and imprint. The bezel design allows adequate airflow to cool system components and has light pipes to allow front panel LEDs to be visible from the front of the server. Removing the bezel exposes peripherals, front panel switches and I/O connectors.

Two black plastic pull handles cover the EIA mounting flanges and enable a user to slide the chassis in and out of a rack.



Figure 16. Front Bezels (Rack and Pedestal)

4. Cables and Connectors

This section describes cables and connectors specific to the platforms. This section includes an overview diagram of the platforms' interconnections, and tables that describe the signals and-pin-outs for user accessible connectors. Sections that follow will cover platform-specific board cables and connectors. See the *Intel® Server Board Set SE8501HW4 Technical Product Specification* for other connector signal descriptions and-pin-outs. This section is organized as follows:

Section 4.1: Cable and System Interconnect Descriptions

Provides a list of the connectors and cables in the system.

Section 4.2: User-accessible I/O Connectors

Describes the form-factor and-pin-out of user-accessible interconnects.

The block diagram in Figure 17 provides an overview of the cables and their relation to system boards in the platform.

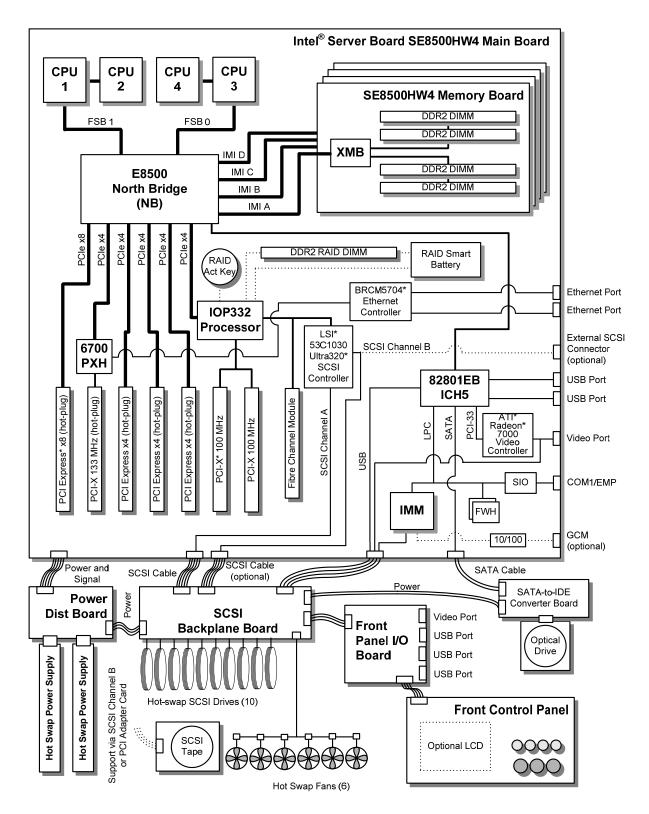


Figure 17. Server Platform Interconnect Diagram

4.1 Cable and System Interconnect Descriptions

Table 6 and Table 7 list cables and connectors used in the assembly of the platforms.

Table 6. Cable Descriptions

| Туре | Quantity | From | То | Cable Description |
|----------|----------|-----------------------|---|---|
| Signal | 1 | Mainboard | SCSI backplane board | 100-pin (multi-signal function) |
| Signal | 1 | SCSI backplane board | Front Panel I/O Board | 30-pin (multi-signal function) |
| SCSI | 2 | Mainboard | SCSI backplane board | 68-pin internal SCSI |
| SCSI | 1 | Mainboard | Rear panel | 68-pin VHDCI SCSI (optional) |
| SATA | 1 | Mainboard | SATA-to-IDE converter board | 7-pin SATA |
| DC Power | 1 | SCSI backplane board | SATA-to-IDE converter board SCSI tape device | 4-pin power (mini connector) 4-pin power |
| Signal | 1 | Front Panel I/O Board | Front panel | 50-pin (multi-signal function) |
| Switch | 1 | Mainboard | Chassis intrusion switch | 3-pin switch |

Table 7. Connector Descriptions

| System Component | Туре | Quantity | From | То | Interconnect Description |
|------------------|--|----------|-----------|---|------------------------------------|
| Mainboard | Processors | 4 | Mainboard | Processor | 604-pin ZIF sockets |
| | PCI Express* | 4 | Mainboard | Memory board connector | 164-pin Card Edge Connectors |
| | Memory | 1 | Mainboard | ROMB DIMM | 240-pin Card Edge Connector |
| | PCI Express* | 1 | Mainboard | Fibre Channel Module | 164-pin Card Edge Connector |
| | VRM | 1 | Mainboard | L3cache VRM9DO module | 62-pin Card Edge Connector |
| | VRM | 2 | Mainboard | VRM10.2 module | 54-pin power connectors |
| | PCI-X* | 3 | Mainboard | PCI-X* adapters | 188-pin Card Edge Connectors |
| | PCI Express* | 4 | Mainboard | PCI Express* adapters | 98-pin Card Edge Connectors |
| | Intel [®] Management Module | 1 | Mainboard | Intel [®] Management Module | 120-pin connector |

| System Component | Туре | Quantity | From | То | Interconnect Description |
|---------------------|----------------------|----------|----------------------|-----------------------------|---|
| | ICMB | 1 | Mainboard | Internal interface | 1 x 5 Header connector |
| | IPMB | 1 | Mainboard | Internal interface | 1 x 3 Header connector |
| | Chassis Intrusion | 1 | Mainboard | Top cover switch | 1 x 3 Header connector |
| | USB | 1 | Mainboard | Rear panel | 1 x 4-pin double stacked USB connector |
| | USB | 1 | Mainboard | Internal interface | 1 x 4-pin connector |
| | Video | 1 | Mainboard | Rear panel, monitor | 15-pin, monitor device |
| | COM1/EMP | 1 | Mainboard | Rear panel | 9-pin Emergency Management Port (DB9) |
| | COM2 | 1 | Mainboard | Internal interface | 2 x 5-pin header |
| | Ethernet | 1 | Mainboard | Rear panel | Double stacked RJ45 connector ports |
| | SCSI | 2 | Mainboard | Internal SCSI channels | 68-pin SCSI connectors |
| | Signal | 1 | Mainboard | SCSI backplane board | 100-pin connector |
| | Ethernet | 1 | Mainboard | External interface | RJ45 connector port, GCM |
| | DC power and signal | 1 | Mainboard | RAID Smart Battery | 2 x 10-pin header |
| | SATA signal | 1 | Mainboard | SATA-to-IDE converter board | 1 x 7-pin connector (standard SATA) |
| | DC power | 2 | Mainboard | Power distribution board | 1 x 12-pin connectors |
| | DC signal | 1 | Mainboard | Power distribution board | 2 x 15-pin header |
| Memory Board | Memory | 1 | Memory board | Mainboard | 164-pin Card Edge Connector (x16 PCle*) |
| | Memory | 4 | Memory board | DDR2 DIMMs | 240-pin Card Edge Connector (4 per board) |
| SCSI Backplane | SCA2 | 10 | SCSI backplane board | Hot-swap hard disk drive | 80-pin SCA2 connectors |
| Board Board | SCSI | 2 | SCSI backplane board | Mainboard | 68-pin SCSI connectors |
| | Signal | 1 | SCSI backplane board | Mainboard | 100-pin connector |

| System Component | Туре | Quantity | From | То | Interconnect Description |
|---|---------------------|----------|---|--|--|
| | DC power and signal | 2 | SCSI backplane board | Fans | 2 x 14-pin headers |
| | DC power | 1 | SCSI backplane board | SATA-to-IDE converter board, Tape device | 1 x 4-pin header |
| | Signal | 1 | SCSI backplane board | Front panel I/O board | 34-pin connector |
| | DC power | 1 | SCSI backplane board | Power distribution board | 1 x 12-pin connector |
| Front Panel I/O Board | Signal | 1 | Front panel I/O board | SCSI backplane board | 30-pin header |
| | Video | 1 | Front panel I/O board | Front panel, monitor | 15-pin, monitor device |
| | USB | 1 | Front panel I/O board | Front panel | 1x4-pin triple stacked USB connector |
| | Front panel | 1 | Front panel I/O board | Button Control Panel or Intel® Local Control Panel | 50-pin header |
| SATA-to-IDE Converter | Signal | 1 | SATA-to-IDE converter board | Optical device | 50-pin JAE (IDE) |
| Board | SATA | 1 | SATA-to-IDE converter board | Mainboard | 1 x 7-pin connector (standard SATA) |
| | DC power | 1 | SATA-to-IDE converter board | SCSI backplane board | 1 x 4-pin header (mini connector) |
| Fan module | DC power and signal | 6 | Fan | SCSI backplane board | 2 x 6-pin header |
| Button Control Panel or Intel [®] Local Control Panel | Signal | 1 | Button control panel or Intel [®] Local Control Panel | SCSI backplane board | 50-pin header |
| Power Distribution | DC power and signal | 2 | Power distribution board | Power supply | 34-blade connector |
| Board | DC power | 2 | Power distribution board | Mainboard | 1 x 12-pin connector |
| | Signal | 1 | Power distribution board | Mainboard | 2 x 15-pin header |
| | DC power | 1 | Power distribution board | SCSI backplane board | 1 x 12-pin connector |
| Power Supply | DC power and signal | 1 | Power supply | Power distribution board | 34-blade connector |
| | AC power | 1 | Power supply | External interface | IEC filtered 15A receptacle |

4.2 User-accessible I/O Connectors

4.2.1 Video Connectors

The Intel[®] Server Board Set SE8501HW4 mainboard and platforms' front panel I/O board provide a video port interface with a standard VGA-compatible, 15-pin connector.

Signal Name and Description Video Connector Pin VID_R (analog color signal red) VID_G (analog color signal green) 2 VID_B (analog color signal blue) 3 4 No connection GND 5 GND 6 **GND** 8 GND 9 No connection 10 GND 11 No connection 12 MONID1 (to support DDCx, Display Data Channel* standard) VID HSYNC (horizontal sync) 13 14 VID VSYNC (vertical sync) 15 MONID2 (to support DDCx, Display Data Channel standard)

Table 8. Video Connector Pin-out

4.2.2 USB 2.0 Connectors

The Intel® Server Board Set SE8501HW4 mainboard provides a double-stacked USB port at the rear panel and one vertical USB port located in the middle of the mainboard. The platforms' front panel I/O board provides three stacked USB port connectors via a USB hub controller. These built-in USB ports permit the direct connection of six USB peripherals without an external hub. If more devices are required, an external hub can be connected to any of the built-in ports.

Pin Signal **USB Connectors** Fused Voltage Controlled Current (VCC) (+5 V with over-Α1 current monitoring) USBPxM (differential data line) A2 USBPxP (differential data line) A3 **Dual Stacked USB Connector on Rear Panel** GND (ground) A4 В1 Fused VCC (+5 V with over-current monitoring) USBPxM (differential data line) B2 B3 USBPxP (differential data line) B4 GND (ground) **Triple Stacked USB Connector on Front Panel**

Table 9. Dual USB Connector Pin-out

4.2.3 Etherent Connectors

The Intel® Server Board Set SE8501HW4 mainboard provides a dual-RJ45 connector for Ethernet connection.

Table 10. Dual Ethernet Stacked Connector

| Pin | Signal | Description |
|-------------------------|--|---|
| | | LED Signals |
| 27 | DNW_LINKB10_N | Lower (Port 1) green status LED cathode signal indicating Port 1 activity |
| 28 | DNW1_ACT_N_R | Lower (Port 1) green status LED anode to 100-ohm pullup to 3.3V Standby |
| 29 | DNW_LINKB100_N | Lower (Port 1) green speed LED cathode, yellow LED anode |
| 30 | LANB1000_N_R | Lower (Port 1) yellow speed LED cathode, green LED anode |
| 31 | DNW_LINKA10_N | Upper (Port 2) green status LED cathode signal indicating Port 2 activity |
| 32 | DNW0_ACT_N_R | Upper (Port 2) green status LED anode to 100-ohm pullup to 3.3V Standby |
| 33 | DNW_LINKA100_N | Upper (Port 2) green speed LED cathode, yellow LED anode |
| 34 | LANA1000_N_R | Upper (Port 2) yellow speed LED cathode, green LED anode |
| Etherr | net Signals | |
| 15 | DNW_MDIB_DP<0> | Port 1 transceiver 0 positive of differential pair |
| 21 | DNW_MDIB_DN<0> | Port 1 transceiver 0 negative of differential pair |
| 23 | DNW_MDIB_DP<1> | Port 1 transceiver 1 positive of differential pair |
| 16 | DNW_MDIB_DN<1> | Port 1 transceiver 1 negative of differential pair |
| 18 | DNW_MDIB_DP<2> Port 1 transceiver 2 positive of differential pair | |
| 24 | DNW_MDIB_DN<2>> Port 1 transceiver 2 negative of differential pair | |
| 26 | DNW_MDIB_DP<3> | Port 1 transceiver 3 positive of differential pair |
| 19 | DNW_MDIB_DN<3> | Port 1 transceiver 3 negative of differential pair |
| 6 | DNW_MDIA_DP<0> | Port 2 transceiver 0 positive of differential pair |
| 13 | DNW_MDIA_DN<0> Port 2 transceiver 0 negative of differential pair | |
| 11 | DNW_MDIA_DP<1> | Port 2 transceiver 1 positive of differential pair |
| 5 | DNW_MDIA_DN<1> | Port 2 transceiver 1 negative of differential pair |
| 3 | DNW_MDIA_DP<2> | Port 2 transceiver 2 positive of differential pair |
| 10 | DNW_MDIA_DN<2> | Port 2 transceiver 2 negative of differential pair |
| 8 | DNW_MDIA_DP<3> | Port 2 transceiver 3 positive of differential pair |
| 2 | DNW_MDIA_DN<3> | Port 2 transceiver 3 negative of differential pair |
| | | Power Signals |
| 4, 7, 9 14, 17 25 | | |
| 1, 20, 36, 37 | | Ground |

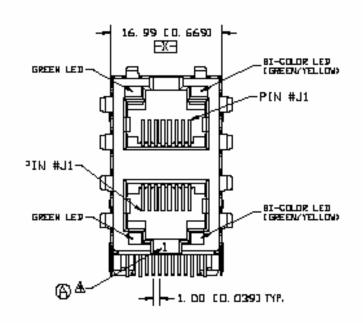


Figure 18. Dual Stacked Ethernet Connector

The mainboard also provides an RJ45 connector that connects to the Intel[®] Management Module - Advanced Edition for out-of-band server management features. This out-of-band connector is also referred to as the Generic Communication Module (GCM), or server management Ethernet controller.

Table 11. Server Management Ethernet Connector

| Pin | Signal | Description | Server Management Ethernet Connector |
|-----|-----------------------|--------------------|--------------------------------------|
| 1 | GCM_NIC_RDM | | |
| 2 | GCM_NIC_RDP | | |
| 3 | | Magnetics Tap | |
| 4 | | Magnetics Tap | |
| 5 | | Magnetics Tap | Green LED Yellow LED |
| 6 | | Magnetics Tap | |
| 7 | GCM_NIC_TDM | | 1 |
| 8 | GCM_NIC_TDP | | |
| A1 | TP_GMC_RJ45_YEL_LED_A | Yellow LED Anode | |
| C1 | TP_GMC_RJ45_YEL_LED_C | Yellow LED Cathode | |
| A2 | GMC_NIC_ACTLED_N | Green LED Anode | |
| C2 | GMC_NIC_ACTLED_R_N | Green LED Cathode | |

4.2.4 External 68-pin Ultra320* SCSI VHDCI Connector

As an option, the platforms can support a shielded external SCSI connection. This SCSI port is controlled by the SCSI controller component located on the Intel® Server Board Set SE8501HW4 mainboard. This interconnect is a VHDCI connector at the rear panel.

Table 12. Ultra 320* SCSI VHDCI Connector-pin-out

| 1 | Pin | Signal Name | Ultra 320* SCSI VHDCI Connector | Pin | Signal Name |
|--|-----|-------------|---------------------------------|-----|-------------|
| The matrix of | 1 | +DB(12) | | 35 | -DB(12) |
| 4 | 2 | +DB(13) | 35 68 | 36 | -DB(13) |
| **1 | 3 | +DB(14) | | 37 | -DB(14) |
| Solid Soli | 4 | +DB(15) | L | 38 | -DB(15) |
| 7 +DB(1) 8 +DB(2) 9 +DB(3) 10 +DB(4) 11 +DB(5) 12 +DB(6) 13 +DB(7) 14 +P_CRCA 15 GND 16 DIFFSENS 17 TERMPWR 18 TERMPWR 19 NC 20 GND 21 +ATN 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) | 5 | +DB(P1) | 1 34 | 39 | -DB(P1) |
| 8 +DB(2) 9 +DB(3) 10 +DB(4) 11 +DB(5) 12 +DB(6) 13 +DB(7) 14 +P_CRCA 15 GND 16 DIFFSENS 17 TERMPWR 18 TERMPWR 19 NC 20 GND 21 +ATN 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) | 6 | +DB(0) | | 40 | -DB(0) |
| 9 +DB(3) 10 +DB(4) 11 +DB(5) 12 +DB(6) 13 +DB(7) 14 +P_CRCA 15 GND 16 DIFFSENS 17 TERMPWR 18 TERMPWR 19 NC 20 GND 21 +ATN 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) | 7 | +DB(1) | | 41 | -DB(1) |
| 10 | 8 | +DB(2) | | 42 | -DB(2) |
| 11 | 9 | +DB(3) | | 43 | -DB(3) |
| 12 | 10 | +DB(4) | | 44 | -DB(4) |
| 13 | 11 | +DB(5) | | 45 | -DB(5) |
| 14 +P_CRCA 15 GND 16 DIFFSENS 17 TERMPWR 18 TERMPWR 19 NC 20 GND 21 +ATN 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) | 12 | +DB(6) | | 46 | -DB(6) |
| 15 | 13 | +DB(7) | | 47 | -DB(7) |
| 16 DIFFSENS 17 TERMPWR 18 TERMPWR 19 NC 20 GND 21 +ATN 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) | 14 | +P_CRCA | | 48 | +P_CRCA |
| 17 TERMPWR 18 TERMPWR 19 NC 20 GND 21 +ATN 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) | 15 | GND | | 49 | GND |
| 18 TERMPWR 19 NC 20 GND 21 +ATN 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) | 16 | DIFFSENS | | 50 | GND |
| 19 NC 20 GND 21 +ATN 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) 53 NC 54 GND 55 -ATN 56 GND 57 -BSY 58 -ACK 59 -RST 60 -MSG 61 -SEL 62 -C/D 63 -REQ 65 -DB(8) 65 -DB(9) 66 -DB(9) | 17 | TERMPWR | | 51 | TERMPWR |
| 20 GND 21 +ATN 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) 54 GND 55 GND 55 -ATN 55 -ACK 58 -ACK 58 -ACK 60 -MSG 60 -MSG 61 -SEL 62 -C/D 62 -C/D 64 -I/O 65 -DB(8) 66 -DB(9) 67 -DB(10) | 18 | TERMPWR | | 52 | TERMPWR |
| 21 +ATN 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) 55 -ATN 56 GND 57 -BSY 57 -BSY 60 -MSG 60 -MSG 60 -MSG 61 -SEL 62 -C/D 62 -C/D 64 -I/O 65 -DB(8) 66 -DB(9) 67 -DB(10) | 19 | NC | | 53 | NC |
| 22 GND 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) | 20 | GND | | 54 | GND |
| 23 +BSY 24 +ACK 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) 57 -BSY 58 -ACK 59 -RST 60 -MSG 60 -MSG 61 -SEL 62 -C/D 63 -REQ 64 -I/O 64 -I/O 65 -DB(9) 66 -DB(9) 67 -DB(10) | 21 | +ATN | | 55 | -ATN |
| 24 | 22 | GND | | 56 | GND |
| 25 +RST 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) 59 -RST 60 -MSG 60 -MSG 60 -CD 60 -MSG 61 -SEL 62 -C/D 63 -REQ 64 -I/O 64 -I/O 65 -DB(8) 66 -DB(9) 67 -DB(10) | 23 | +BSY | | 57 | -BSY |
| 26 +MSG 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) 60 -MSG 61 -SEL 62 -C/D 62 -C/D 63 -REQ 64 -I/O 65 -DB(8) 66 -DB(9) 67 -DB(10) | 24 | +ACK | | 58 | -ACK |
| 27 +SEL 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) 61 -SEL 62 -C/D 63 -REQ 64 -I/O 65 -DB(8) 66 -DB(9) 67 -DB(10) | 25 | +RST | | 59 | -RST |
| 28 +C/D 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) 62 -C/D 63 -REQ 64 -I/O 65 -DB(8) 66 -DB(9) 67 -DB(10) | 26 | +MSG | | 60 | -MSG |
| 29 +REQ 30 +I/O 31 +DB(8) 32 +DB(9) 33 +DB(10) 63 -REQ 64 -I/O 65 -DB(8) 66 -DB(9) 67 -DB(10) | 27 | +SEL | | 61 | -SEL |
| 30 +I/O 64 -I/O 65 -DB(8) 65 -DB(9) 66 -DB(9) 67 -DB(10) | 28 | +C/D | | 62 | -C/D |
| 31 +DB(8) 32 +DB(9) 33 +DB(10) 65 -DB(8) 66 -DB(9) 67 -DB(10) | 29 | +REQ | | 63 | -REQ |
| 32 +DB(9) 33 +DB(10) 66 -DB(9) 67 -DB(10) | 30 | +I/O | | 64 | -I/O |
| 33 +DB(10) 67 -DB(10) | 31 | +DB(8) | | 65 | -DB(8) |
| | 32 | +DB(9) | | 66 | -DB(9) |
| 34 +DB(11) 68 -DB(11) | 33 | +DB(10) | | 67 | -DB(10) |
| | 34 | +DB(11) | | 68 | -DB(11) |

4.2.5 Internal 68-pin SCSI Connectors

The Intel® Server Board Set SE8501HW4 mainboard has two unshielded 68-pin SCSI connectors for SCSI channel A and B.

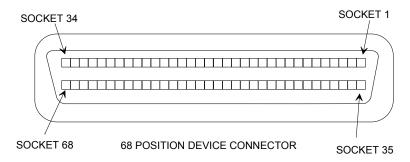


Figure 19. 68-Pin SCSI Connector Non-shielded

Table 13. 68-Pin SCSI Connector Pin-out

| Connector-pin | Signal Name | Connector-pin | Signal Name |
|---------------|---------------------|---------------|-------------------|
| 1 | SCSI(A:B)_DB_P12 | 35 | SCSI(A:B)_DB_N12 |
| 2 | SCSI(A:B)_DB_P13 | 36 | SCSI(A:B)_DB_N13 |
| 3 | SCSI(A:B)_DB_P14 | 37 | SCSI(A:B)_DB_N14 |
| 4 | SCSI(A:B)_DB_P15 | 38 | SCSI(A:B)_DB_N15 |
| 5 | SCSI(A:B)_DB_PP1 | 39 | SCSI(A:B)_DB_NP1 |
| 6 | SCSI(A:B)_DB_P0 | 40 | SCSI(A:B)_DB_N0 |
| 7 | SCSI(A:B)_DB_P1 | 41 | SCSI(A:B)_DB_N1 |
| 8 | SCSI(A:B)_DB_P2 | 42 | SCSI(A:B)_DB_N2 |
| 9 | SCSI(A:B)_DB_P3 | 43 | SCSI(A:B)_DB_N3 |
| 10 | SCSI(A:B)_DB_P4 | 44 | SCSI(A:B)_DB_N4 |
| 11 | SCSI(A:B)_DB_P5 | 45 | SCSI(A:B)_DB_N5 |
| 12 | SCSI(A:B)_DB_P6 | 46 | SCSI(A:B)_DB_N6 |
| 13 | SCSI(A:B)_DB_P7 | 47 | SCSI(A:B)_DB_N7 |
| 14 | SCSI(A:B)_DP0_P | 48 | SCSI(A:B)_DP0_N |
| 15 | GND | 49 | GND |
| 16 | SCSI(A:B)_DIFFSENSE | 50 | GND |
| 17 | SCSI(A:B)_TERMPWR | 51 | SCSI(A:B)_TERMPWR |
| 18 | SCSI(A:B)_TERMPWR | 52 | SCSI(A:B)_TERMPWR |
| 19 | RESERVED (NC) | 53 | RESERVED |
| 20 | GND | 54 | GND |
| 21 | SCSI(A:B)_ATN_P | 55 | SCSI(A:B)_ATN_N |
| 22 | GND | 56 | GND |
| 23 | SCSI(A:B)_BSY_P | 57 | SCSI(A:B)_BSY_N |
| 24 | SCSI(A:B)_ACK_P | 58 | SCSI(A:B)_ACK_N |
| 25 | SCSI(A:B)_RST_P | 59 | SCSI(A:B)_RST_N |

| Connector-pin | Signal Name | Connector-pin | Signal Name |
|---------------|------------------|---------------|------------------|
| 26 | SCSI(A:B)_MSG_P | 60 | SCSI(A:B)_MSG_N |
| 27 | SCSI(A:B)_SEL_P | 61 | SCSI(A:B)_SEL_N |
| 28 | SCSI(A:B)_CD_P | 62 | SCSI(A:B)_CD_N |
| 29 | SCSI(A:B)_REQ_P | 63 | SCSI(A:B)_REQ_N |
| 30 | SCSI(A:B)_IO_P | 64 | SCSI(A:B)_IO_N |
| 31 | SCSI(A:B)_DB_P8 | 65 | SCSI(A:B)_DB_N8 |
| 32 | SCSI(A:B)_DB_P9 | 66 | SCSI(A:B)_DB_N9 |
| 33 | SCSI(A:B)_DB_P10 | 67 | SCSI(A:B)_DB_N10 |
| 34 | SCSI(A:B)_DB_P11 | 68 | SCSI(A:B)_DB_N11 |

4.2.6 80-pin SCA2 Hard Disk Drive Connectors

The platforms SCSI Backplane Board have ten SCA2 connectors.

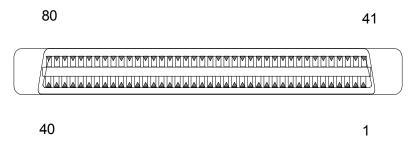


Figure 20. Intel® Server Board Set SE8500HW4 Main Board

Signal Name Pin Signal Name Pin Signal Name Pin Signal Name Pin +12V 21 LVD_DB7_N 41 GND 61 LVD DB7 P +12V 22 42 GND 62 LVD_DB6_P 2 LVD_DB6_N 3 +12V 23 GND 63 LVD DB5 N 43 LVD DB5 P 4 +12V 24 LVD DB4 N 44 SCSI MATED 64 LVD DB4 P 5 NC 25 LVD_DB3_N 45 NC 65 LVD_DB3_P NC 26 66 6 LVD DB2 N 46 DIFFSENSE LVD DB2 P 7 LVD_DB11_N 27 LVD_DB1_N 47 LVD_DB11_P 67 LVD_DB1_P 28 8 LVD DB10 N 48 LVD DB10 P 68 LVD DB0 P LVD DB0 N LVD_DB9_N 29 LVD_DBP1_N 49 LVD_DB9_P 69 LVD_DBP1_P LVD_DB8_N LVD_DB15_P 10 30 LVD_DB15_N 50 LVD_DB8_P 70 11 31 71 LVD IO N LVD_DB14_N 51 LVD IO P LVD DB14 P 12 LVD_REQ_N 32 LVD_DB13_N 52 LVD_REQ_P 72 LVD_DB13_P 13 33 LVD DB12 N 53 73 LVD DB12 P LVD CD N LVD CD P 14 LVD_SEL_N 34 +5V 54 LVD_SEL_P 74 SCSI_MATED 15 LVD_MSG_N 35 +5V 55 LVD_MSG_P 75 **GND** 76 16 LVD RST N 36 +5V 56 LVD RST P **GND**

Table 14. SCA2 Drive Connector Pin-out

| Pin | Signal Name |
|-----|-------------|-----|-------------|-----|-------------|-----|-------------|
| 17 | LVD_ACK_N | 37 | NC | 57 | LVD_ACK_P | 77 | SCSI_ACT |
| 18 | LVD_BSY_N | 38 | GND | 58 | LVD_BSY_P | 78 | NC |
| 19 | LVD_ATN_N | 39 | SCSI_ID (0) | 59 | LVD_ATN_P | 79 | SCSI_ID(1) |
| 20 | LVD_DBP_N | 40 | SCSI_ID (2) | 60 | LVD_DBP_P | 80 | SCSI_ID(3) |

4.2.7 AC Power Input Connectors

An IEC320 15A receptacle is located on each power supply. An appropriately sized power cord and AC main power source are required. See Section 5 for system voltage, frequency, and current draw specifications. An external AC cord retention feature is supported by the chassis but is not supplied by Intel. Please refer to the Intel[®] Server Platform SR6850HW4 Power Cord Enabling Specification to assist in the procurement of power cords for the platform.

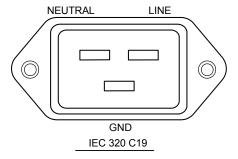


Figure 21. AC Power Input Connector

4.2.8 3-pin Chassis Intrusion Connector

See the table below for 3-pin chassis intrusion connector information.

Table 15. 3-pin Chassis Intrusion Connector

| Pin | Signal | | | | |
|-----|---------------------------|--|--|--|--|
| 1 | Intrusion event | | | | |
| 2 | GND | | | | |
| 3 | Intrusion button attached | | | | |

4.2.9 12-pin Power Distribution Board Power Connector

The Intel® Server Platform SR4850HW4/SR6850HW4 power distribution board has three power connectors, two for the Intel® Server Board Set SE8501HW4 mainboard and one for the platforms' SCSI backplane board.

Table 16. Power Connector Pin-out

| Pins Signal | |
|-------------|------|
| 1-6 | GND |
| 7-12 | +12V |

4.2.10 30-pin Power Distribution Board to Mainboard Connector

See the table below for the 30-pin power distribution board to mainboard connector information.

Table 17. 30-pin Power Distribution Board to Mainboard Connector

| Pins | Signal Description | |
|--------------------|----------------------|--|
| 1,17,25,30 | GND | |
| 6,7,10,12,14,15,24 | 3.3V _{stby} | |
| 2 | PS1 present | |
| 3 | PS2 AC good | |
| 4 | PS Fan control | |
| 5 | PS1 AC good | |
| 8 | PS1 AC range | |
| 9 | PS on | |
| 11 | I ² C SCL | |
| 13 | I ² C SDA | |
| 16 | 12V Sense return | |
| 18 | PS 90% utilization | |
| 19 | PS 74% utilization | |
| 20 | PS 45% utilization | |
| 21 | PS 37% utilization | |
| 22 | Int alert | |
| 23 | PS2 AC range | |
| 26 | PS1 AC good | |
| 27 | 12V Sense | |
| 28 | PS1 power OK | |
| 29 | PS2 present | |

4.2.11 30-pin SCSI Backplane Board Board to Front Panel I/O Board Connector

Please, see the table below for the 30-pin SCSI backplane board to front panel I/O board connector information.

Table 18. Front Panel I/O Board Connector Signal Description

| Pins | Signal Description |
|--------------|--------------------|
| 1,7,10,26,28 | Ground |
| 19,21,23,25 | 5V |
| 2 | USB Hub DPD1 |
| 3 | USB Hub DMD1 |
| 5 | USB Hub DPD2 |
| 6 | USB Hub DMD2 |
| 8 | USB Hub DPD3 |

| Pins | Signal Description | | |
|------|--------------------------------------|--|--|
| 9 | USB Hub DMD3 | | |
| 11 | USB1 overcurrent output, active high | | |
| 12 | USB2 overcurrent | | |
| 13 | USB3 overcurrent | | |
| 14 | NMI button, active low | | |
| 15 | Video DCC out SCLCK | | |
| 16 | Video DCC out SDA | | |
| 17 | Video vertical sync | | |
| 18 | Video horizontal sync | | |
| 20 | Video red | | |
| 22 | Video green | | |
| 24 | Video blue | | |
| 27 | Speaker drive, active high | | |
| 29 | Monitor presence, active low | | |
| 30 | Unused, keying-pin | | |

4.2.12 100-pin Mainboard to SCSI Backplane Board Board Connector

Please, see the tables below for the 100-pin mainboard to SCSI backplane board connector information.

Table 19. 100-pin Connector Pin-out (Unused and Ground)

| Pin Numbers | Signal Descriptions |
|---|------------------------|
| 1,3,7,10,14,20,27,42,51,52,54,58,62,65,73,77,79,82,83,85,87,89,91,93,95,100 | Ground |
| 4,6,8,12,13,15,17,19,22,24,26,29,31,33,35,37,41,44,46,48,50,53,56,59,61,66,68,70,72 | Unused |

Table 20. 100-pin Connector-pin-out (Signals)

| Pin Number | Signal Name | Signal Description | |
|---------------|----------------|--|--|
| 2 | GND - RESISTOR | Ground through zero ohm resistor | |
| 5 | GND - RESISTOR | Ground through zero ohm resistor | |
| 9 | GND - RESISTOR | Ground through zero ohm resistor | |
| 11 | GND - RESISTOR | Ground through zero ohm resistor | |
| 16 | FAN1_TACH | Fan 1 Tachometer signal – edges per revolution | |
| 18 | FAN2_TACH | Fan 2 Tachometer signal – edges per revolution | |
| 21 | FAN3_TACH | Fan 3 Tachometer signal – edges per revolution | |
| 23 | FAN4_TACH | Fan 4 Tachometer signal – edges per revolution | |
| 25 | RESET_BTN | Front panel reset button signal | |
| 28 | FAN5_TACH | Fan 5 Tachometer signal – edges per revolution | |
| 30 | FAN6_TACH | Fan 6 Tachometer signal – edges per revolution | |

| Pin Number | Signal Name | Signal Description | | |
|---------------|------------------------|--|--|--|
| 32 | FAN_PWM1 | Zone 1 Fan PWM control signal | | |
| 34 | 5VSTANDBY | 5V standby to front panel | | |
| 36 | BP_D2D_EN | Backplane D2D enable | | |
| 38 | 5VSTANDBY | 5Vstandby to front panel | | |
| 39 | ICH5_PDD8 | IDE primary disk data 8 | | |
| 40 | HD_ACT_N | SATA Hard Drive Activity | | |
| 43 | BP_PWRGOOD | Backplane power good signal | | |
| 45 | PCI_RST_BP_N | PCI reset to backplane | | |
| 47 | CP_PWR_LED | Control Panel Power LED signal | | |
| 49 | CP_SPKR_OUT_N | Speaker signal to front panel | | |
| 55 | NIC1_LED | NIC 1 activity LED signal | | |
| 57 | ID_LED | ID LED Signal | | |
| 60 | CP_BTN_PWR_ON | Control panel Power Button signal | | |
| 63 | SYS_STATUS_AMB_LED | System Status amber LED signal | | |
| 64 | CD_PRES_N | CD drive presence signal | | |
| 67 | CP_ID_BUTTON_RAW | Control panel ID button signal | | |
| 69 | CP_BTN_NMI | Control panel NMI button | | |
| 71 | NIC2_LED | NIC2 activity LED signal | | |
| 74 | I2C_IPMB_SCL | IPMB I ² C bus clock | | |
| 75 | BP_PRES_N | SCSI Backplane Board Board presence signal, indicates System Board interlock is achieved | | |
| 76 | I2C_IPMB_SDA | IPMB I ² C bus data | | |
| 78 | SYS_PWRGD4 | Mainboard power good signal to SCSI Backplane Board Board | | |
| 80 | USB_FRONT_N | USB port 2 differential negative signal to front bezel | | |
| 81 | USB_FRONT_P | USB port 2 differential positive signal to front bezel | | |
| 84 | VID_RED_FRONT | Video DAC 2 RED signal | | |
| 86 | VID_BLUE_FRONT | Video DAC 2 BLUE signal | | |
| 88 | VID_GREEN_FRONT | Video DAC 2 GREEN signal | | |
| 90 | VID_HS_OUT_FRONT | Video DAC 2 Horizontal Synchronization signal | | |
| 92 | VID_VS_OUT_FRONT | Video DAC 2 Vertical synchronization signal | | |
| 94 | VID_DDC_OUT_SCLK_FRONT | Video Monitor detection I ² C bus clock | | |
| 96 | VID_DDC_OUT_SDA_FRONT | Video monitor detection I ² C bus data | | |
| 97 | I2C_CP_SDA | Control panel I ² C bus data (I ₂ C segment 2) | | |
| 98 | SYS_STATUS_GRN_LED | System status green LED signal | | |
| 99 | I2C_CP_SCL | Control panel I ² C bus data (I ² C segment 2) | | |

4.2.13 Peripheral Power Connector

The platforms' SCSI backplane board provides a standard power connector to drive both the SCSI tape device and optical drive.

Table 21. Peripheral Power Connector

| Pins Signal | |
|-------------|-----|
| 1 | 12V |
| 2,3 | GND |
| 4 | 5V |

4.2.14 Fan Connectors

Two fan power connectors on the platforms' SCSI backplane board control and supply the power for the six system fans.

Table 22. 12-pin Fan Power and Control

| Pins | Signal | |
|-------------|-----------|--|
| 7, 10 | 12V | |
| 1, 4, 9, 12 | GND | |
| 8, 11 | FAN_PWM | |
| 2 | FAN1_TACH | |
| 3 | FAN1_AMB | |
| 5 | FAN2_TACH | |
| 6 | FAN2_AMB | |

Table 23. 24-pin Fan Power and Control J6E1

| Pins | Signal | |
|-----------------------------|-----------|--|
| 13, 16, 19, 22 | 12V | |
| | | |
| | | |
| | | |
| 1 4 7 10 15 19 21 24 | GND | |
| 1, 4, 7, 10, 15, 18, 21 ,24 | _ | |
| 14, 17, 20, 23 | FAN_PWM | |
| 2 | FAN3_TACH | |
| 3 | FAN3_AMB | |
| 5 | FAN4_TACH | |
| 6 | FAN4_AMB | |
| 8 | FAN5_TACH | |
| 9 | FAN5_AMB | |
| 11 | FAN6_TACH | |
| 12 | FAN6_AMB | |

4.2.15 50-pin Front Panel Control Module Connector

This connector is used between the platforms' front panel I/O board and standard button control panel or Intel® Local Control Panel.

Table 24. Front Panel Control Module Connector Signal Description

| PIN | Signal Description | PIN | Signal Description |
|-----|--------------------------------------|-----|----------------------------------|
| 1 | +5V Standby | 26 | Not used |
| 2 | +5V Standby | 27 | LAN1 link |
| 3 | +5V | 28 | LAN1 activity |
| 4 | Hard drive activity, | 29 | GND |
| 5 | System status | 30 | Front panel NMI button, Not used |
| 6 | Not used | 31 | Not used |
| 7 | System status | 32 | Not used |
| 8 | +5V Standby | 33 | Not used |
| 9 | +5V Standby | 34 | Not used |
| 10 | Power LED | 35 | Not used |
| 11 | Hard drive activity pull up | 36 | Not used |
| 12 | I ² C IPMB SDA | 37 | Not used |
| 13 | GND | 38 | Not used |
| 14 | I ² C IPMB SCL | 39 | Not used |
| 15 | System ID LED | 40 | Not used |
| 16 | Power button input, active low | 41 | GND |
| 17 | LAN2 link | 42 | Not used |
| 18 | Hard drive fault | 43 | GND |
| 19 | LAN2 activity | 44 | Not used |
| 20 | Front panel reset button, active low | 45 | GND |
| 21 | Not used | 46 | Not used |
| 22 | GND | 47 | GND |
| 23 | Not used | 48 | Not used |
| 24 | Front panel ID button, active low | 49 | GND |
| 25 | Not used | 50 | Not used |

4.2.16 SATA-to-IDE Converter Board Connector

The platforms' SATA-to-IDE converter board connects to an optical drive with this connector.

Table 25. SATA-to-IDE Converter Board Connector

| Pin | Signal | Signal | Pin |
|-----|------------|------------|-----|
| 1 | Audio L-Ch | Audio R-Ch | 2 |
| 3 | Audio GND | GND | 4 |
| 5 | RESET- | DD8 | 6 |
| 7 | DD7 | DD9 | 8 |
| 9 | DD6 | DD10 | 10 |
| 11 | DD5 | DD11 | 12 |
| 13 | DD4 | DD12 | 14 |
| 15 | DD3 | DD13 | 16 |
| 17 | DD2 | DD14 | 18 |
| 19 | DD1 | DD15 | 20 |
| 21 | DD0 | DMARQ | 22 |
| 23 | GND | /DIOR | 24 |
| 25 | DIOW- | GND | 26 |
| 27 | IORDY | /DMACK | 28 |
| 29 | INTRQ | /IOCS16 | 30 |
| 31 | DA1 | /PDIAG | 32 |
| 33 | DA0 | DA2 | 34 |
| 35 | /CS1FX | /CS3FX | 36 |
| 37 | /DASP | +5V | 38 |
| 39 | +5V | +5V | 40 |
| 41 | +5V | +5V | 42 |
| 43 | GND | GND | 44 |
| 45 | GND | GND | 46 |
| 47 | CSEL | GND | 48 |
| 49 | RESERVED | RESERVED | 50 |

4.2.17 SATA-to-IDE Converter Board Power Connector

Please, see the table below for the SATA-to-IDE converter board power connector information.

Table 26. SATA-To-IDE Converter Board Power Connector

| Pin | Signal | |
|-----|----------------------------|--|
| 1 | +5 VDC | |
| 2 | Ground | |
| 3 | Ground | |
| 4 | +12V (Not used on adapter) | |

4.2.18 SATA Connector

The Intel® Server Board Set SE8501HW4 mainboard has a SATA connector that is routed via a cable to the platforms' SATA-to-IDE converter board.

Table 27. SATA Signal Connector

| Pin | Signal |
|-----|--------|
| 1 | Ground |
| 2 | A+ |
| 3 | A- |
| 4 | Ground |
| 5 | B- |
| 6 | B+ |
| 7 | Ground |

5. Power Supply

This section describes the platforms' power supply. The platforms' power supply is current sharing with auto ranging input. The platforms' power supply is approximately 7.7 inches wide, 14.5 inches deep and 3.5 inches high. The unit mounts into the server with a latch.

The output rating of the power supply is 1570W when operated between 170VAC and 264VAC. The platform can run with a single power supply installed. For redundancy, two power supplies must be installed.

The platforms' power supply is shown in Figure 22.

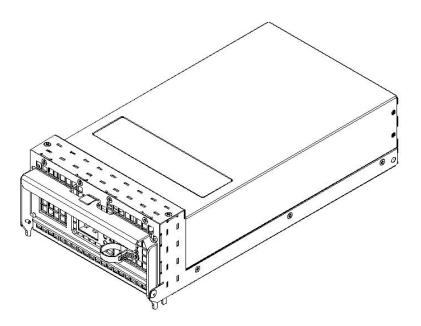


Figure 22. 1570W Power Supply

5.1 Mechanical Outline

The mechanical outline and dimensions are shown on the next page. The dimensions should be used only as a reference.



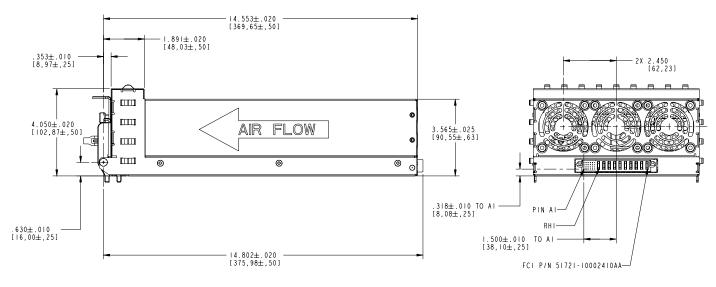


Figure 23. Power Supply Mechanical Specificatio

Revision 1.2 53

5.2 Power Supply Output Interface

5.2.1 Blade Connector

The power supply output power and control signals interface to the system power distribution board through an FCI PowerBlade* right-angle connector.

Table 28. PowerBlade-pin Assignment

| P1 | Pin | Signal Name | Amps per-pin |
|-----------------------------------|---------|-----------------------|--------------|
| FCI Powerblade* 51721- | PB RH1 | +12V return | 26 |
| 10002410AA or approved equivalent | PB RH2 | +12V return | 26 |
| equivalent | PB RH3 | +12V return | 26 |
| Mates to FCI 51741- | PB RH4 | +12V return | 26 |
| 10002410CC on Power | PB RH5 | +12V return | 26 |
| Distribution Board | PB RH6 | +12V | 26 |
| | PB RH7 | +12V | 26 |
| | PB RH8 | +12V | 26 |
| | PB RH9 | +12V | 26 |
| | PB RH10 | +12V | 26 |
| | A1 | PS_KILL | |
| | A2 | +12V current share | |
| | A3 | Return | |
| | A4 | +3.3V _{stby} | |
| | A5 | PS A0 | |
| | A6 | +3.3V _{stby} | |
| | B1 | Return | |
| | B2 | Not used | |
| | B3 | Return | |
| | B4 | +3.3V _{stby} | |
| | B5 | SDA | |
| | B6 | -PS_ON | |
| | C1 | Return | |
| | C2 | Not used | |
| | C3 | Return | |
| | C4 | +3.3V _{stby} | |
| | C5 | SCL | |
| | C6 | VIN_GOOD | |
| | D1 | -PS_Present | |
| | D2 | +12V_Sense | |
| | D3 | +12V_Rtn_Sense | |
| | D4 | +3.3V _{stby} | |
| | D5 | S_INT(Alert) | |
| | D6 | POK | |

5.3 AC Input Requirement

5.3.1 AC Input Voltage Specification

The power supply operates over the range and limits shown in Table 29.

Table 29. AC Input Rating

| Parameter | Minimum | Nominal | Maximum | Unit |
|-----------------|---------|---------|---------|--------|
| Vin (voltage) | 85 | 100/240 | 264 | VACrms |
| Vin (frequency) | 47 | 50/60 | 63 | Hz |
| lin (90VAC) | | | 16.7 | Arms |
| lin (100VAC) | | | 15.0 | Arms |
| lin (115VAC) | | | 16.0 | Arms |
| lin (180VAC) | | | 11.25 | Arms |
| Vin (turn-on) | 80 | | 85 | VACrms |
| Vin (turn-off) | 75 | | 80 | VACrms |

The main outputs of the power supply will turn off per Vin (turn-off). Any standby outputs may continue to operate at input AC voltages below Vin (turn-off).

5.3.2 Efficiency

The power supply has a minimum efficiency of 78% when operated under the maximum loading conditions of 90VAC-264VAC, and environmental conditions. The minimum efficiency is 77% when operated between 85-90VAC.

For loads less than maximum, the internal power dissipation cannot exceed 453W.

5.3.3 Input Over-Current Protection

The power supply has internal primary over-current protection. A normal-blow (fast blow), high-breaking-capacity fuse is placed in the input circuit.

5.3.4 Inrush Current

When input power is applied to the power supply, any initial current surge or spike of 10ms or less will not exceed 55A peak. Any additional inrush current surges or spikes in the form of AC cycles or multiple AC cycles greater than 10ms, and less than 150ms, will not exceed 25A peak.

For any conditions during turn-on, the inrush current will not open the primary input fuse or damage any other components.

5.3.5 Auto Restart

Although the power supply may power off under the conditions mentioned in Sections 5.3.3 and 5.3.4 is capable of restarting, either automatically or under program control after the disturbance. In addition, the power supply will not be in a latched state such that any of the operator buttons/buttons do not operate correctly after the disturbance. At no time will the AC power cord have to be removed to clear an error condition.

Auto restart conditions are tested from -40% to -100% AC under-voltage conditions for time intervals ranging from 25ms to 2sec. For each time interval, all of the under-voltage conditions listed below will be tested. These tests are performed at both the lowest and highest nominal operating voltages of the power supply.

Time intervals: 25ms, 40ms, 60ms, 90ms, 130ms, 200ms, 280ms, 400ms, 600ms, 900ms, 1.3sec, and 2.0sec

Under-voltage deviation from nominal AC voltage: -40%, -50%, -60%, -70%, -80%, -90%, -100%

5.3.6 Power Factor Correction (PFC)

The Power Factor Correction (PFC) is 0.97, or greater, for all specified AC input voltages with output loads greater than 90%.

The PFC is 0.75, or greater, for all specified AC input voltages with output loads greater than 50%.

5.3.7 AC Input Connector

The AC input receptacle is an IEC-320 16A rated for 250VAC minimum.

5.4 DC Output Requirements

The DC output voltages will remain within the regulation ranges shown in the Table 30 when measured at the load end of the connector.

Table 30. DC Output Voltage Regulation Limits

| Output Level | Minimum (V) | Nominal (V) | Maximum (V) |
|-----------------------|-------------|-------------|-------------|
| +12V | 11.64 | 12.00 | 12.60 |
| +3.3V _{stby} | 3.17 | 3.30 | 3.47 |

5.4.1 Hot-swap Functionality

Hot-swapping is the process of inserting and extracting a power supply from an operating power bay. During this process, the output voltages will remain within the limits specified in Table 30, and the system will continue to operate normally.

5.4.2 Output Current Rating

The combined continuous output power for all outputs will not exceed 1570W. Each output has a maximum and minimum current rating shown in Table 31.

Table 31. 1570W Load Ratings

| Output Level | Minimum (A) ¹ | Maximum (A) ¹ | Peak (A) ¹ |
|-----------------------|--------------------------|--------------------------|-----------------------|
| +12V ³ | 1.0 | 91.66 | 95.67 ² |
| +12V ⁴ | 1.0 | 112.5 | 117.00 ² |
| +12V ⁵ | 1.0 | 130.8 | 135.55 ² |
| +3.3V _{stby} | 0.0 | 5.0 | |

- Values are at the system level. For 1+1 redundant systems the load each supply provides is based on its current-sharing accuracy.
- 2. Peak +12V output power not to exceed 15 seconds in duration. Maximum duty cycle is 5%.
- 3. For 85-121VAC operation (100/110VAC rated).
- 4. For 103.5-139VAC operation (115/120/127VAC rated).
- 5. For 170VAC, and higher, operation (200/208/220/230/240VAC rated).

5.4.3 Over- and Under-Voltage Protection

The power supply provides latch mode over and under voltage protection as defined in the following table. A fault on any output will cause the rest of the outputs to latch off. See note number three below the table.

Table 32. Over and Under-voltage Limits

| Output Level | Under-voltage | | Over-v | oltage |
|--|---------------|-------------|-------------|-------------|
| | Minimum (V) | Maximum (V) | Minimum (V) | Maximum (V) |
| +12V | 10.5 | 11.0 | 13.5 | 15.0 |
| +3.3V _{stby} ^{1,2,3} | 2.77 | 3.00 | 3.76 | 4.3 |

Notes:

- 1. In standby mode, the power supply does not latch off due to an under-voltage condition.
- 2. In standby mode, the power supply may or may not latch off due to an over-voltage condition.
- 3. A fault on any output other than $+3.3V_{stby}$ will not cause the $+3.3V_{stby}$ to turn off. A fault on $+3.3V_{stby}$ Standby causes the other outputs to turn off.

5.4.4 Over-current Protection

Over-current is a fault condition defined as a 10A/s current ramp starting from full load applied to the output under test. A fault on any output causes the rest of the outputs to latch off. See note 3 below the following table.

Table 33. Over-current Protection Limits

| Output Level | Minimum (A) ^{2,4} | Maximum (A) ^{2,4} |
|---------------------|----------------------------|----------------------------|
| +3.3V Standby 1,3,5 | 5.3 | 6.2 |
| +12V ⁶ | 122 | 141 |
| +12V ⁷ | 142 | 163 |

Notes:

- 1. Output is Level III SELV and non-energy hazard complaint
- 2. The above current limits will be satisfied throughout the entire operating temperature range
- 3. A fault on any output other than $+3.3V_{stby}$ will not cause the $+3.3V_{stby}$ to turn off. A fault on $+3.3V_{stby}$ will cause the other outputs to turn off.
- 4. Dynamic loading must not cause a false over current when 2 supplies are in parallel.
- The +3.3V_{stby} output will not latch off. It must return to normal operation once the fault is removed. Current foldback method is preferred.
- 6. +12V OC limits change base on the state of AC_RANGE. This helps protect the power supply from over-loading the PFC stage. AC_RANGE low.
- 7. +12V OC limits change base on the state of AC_RANGE. This helps protect the power supply from over-loading the PFC stage. AC_RANGE high.

5.4.5 Short Circuit Protection

A short circuit, which is defined as an impedance of 0.1Ω , or less, applied to any output during start-up or while running will not cause any damage to the power supply (connectors, components, PCB traces, etcetra).

When the +3.3V_{stby} is shorted the output may go into "hiccup mode". When the +3.3V_{stby} attempts to restart the maximum peak current from the output must be less than 8.0A. The maximum average current, taking into account the "hiccup" duty cycle, must be less than 4.0A.

5.4.6 Reset After Shutdown

If the power supply latches into a shutdown state due to a fault condition on any output, the power supply will return to normal operation only after the fault has been removed and the power supply has been power-cycled. Power cycling is defined as either:

- Removing AC input power, waiting for +3.3V_{stby} to drop below 1.0V, then reapplying AC power. The time it takes for +3.3V_{stby} to drop below 1.0V shall not exceed 15 seconds.
- Cycling the state of PS_ON from on to off to on. The minimum cycle time is 1ms.

5.4.7 Current Sharing

Outputs of two supplies that are connected in parallel must meet the regulation requirements of a single supply. Under normal operation with two supplies running in parallel, the outputs must share the load current. If one of the supplies fails, the remaining supply must pick up the entire load without any of the outputs dropping out of regulation. A defective supply that is connected to the output voltage bus has no adverse effect on the operation of the remaining functional supply.

Table 34. Output Current Sharing

| Output Level | Output Sharing |
|-----------------------|----------------|
| +3.3V _{stby} | Not required |
| +12V | Active |

5.4.8 I²C Devices

All I^2C devices are powered from the cathode side of the +3.3 V_{stby} OR'ing diode. This allows the status and FRU data to be read from a power supply that is not powered on or has some other fault. Protection is provided so if a power supply fault occurs it does not take down the +3.3 V_{stby} bus.

Address locations should be determined by external settings through P1,-pin A5. The 0xA1 and 0xA2 address will be wired high on the power supply. (NE1617A does not have an 0xA2 address). The alert signal from (only) the I/O port will be through P1,-pin D5.

5.4.8.1 FRU Data

The power supply contains a serial EEPROM. The address is either 0xAC or 0xAE, depending on address bit 0xA0.

5.4.8.2 I/O Port Expander

The power supply contains a serial I/O port expander, Philips* PCF8575 or approved equivalent. The address is either 0x4C or 0x4E, depending on address bit 0xA0.

Table 35. I/O Port Expander Signals

| Signal Name | I/O Port |
|-------------|----------|
| -OC +12V | P0 |
| -Fan_Fault | P1 |
| -UV | P2 |
| -OV | P3 |
| VIN_GOOD | P4 |
| P_GOOD | P5 |
| -PS_STATUS | P6 |
| AC_PRFAIL | P7 |

| Signal Name | I/O Port |
|---------------|-------------|
| -PFC_OTP | P10 |
| POWER_LEVEL_1 | P11 |
| POWER_LEVEL_1 | P12 |
| POWER_LEVEL_1 | P13 |
| POWER_LEVEL_1 | P14 |
| High | P15,P16,P17 |

Table 36. I/O Port Expander Codes

| Signal Name | Normal Off | Normal On | +12V OC | AC Dropout | Low AC | No AC |
|-------------|------------|-----------|---------|------------|--------|-------|
| -OC +12V | 1 | 1 | 0 | 1 | 1 | 1 |
| Not Used | 1 | 1 | 1 | 1 | 1 | 1 |
| -UV | 1 | 1 | 1 or 0 | 1 | 1 | 1 |
| -OV | 1 | 1 | 1 | 1 | 1 | 1 |
| VIN_GOOD | 1 | 1 | 1 | 1 or 0 | 0 | 0 |
| P_GOOD | 0 | 1 | 0 | 0 | 0 | 0 |
| -PS_STATUS | 1 | 0 | 1 | 1 | 1 | 1 |
| -AC_PRFAIL | 1 | 1 | 1 | 0 | 1 | 1 |

Note: The No AC column refers to the status of the I/O port when only the external $+3.3_{\text{stby}}$ bus voltage is available.

5.4.8.3 Temperature Sensors

A Philips* NE1617A or equivalent temperature sensor is located near the air inlet of the supply. The address is either 0x34 or 0x9C depending on address bit 0xA0. A second sensor is near the exhaust outlet.

5.4.9 Fan Speed Control

The power supply provides forced air-cooling through three DC fans that have intake through the circular grill. The cooling fans are 60mm in diameter and 38mm in depth. The fans are mounted to the front (output connector), and exhaust through the rear (AC Inlet connector) of the PS case.

The power supply uses a fan speed controller that is based on the input Fan_Cntl. The input is an analog signal from 0.0V to 3.0V. Control of the fan is linear in relation to the Fan_Cntl signal.

Table 37. Power Supply Fan Voltage

| Fan_Cntl Voltage | Minimum Fan Voltage | Maximum Fan Voltage |
|------------------|---------------------|---------------------|
| 0.00V | 7.00V | 7.50V |
| 1.50V | 9.55V | 10.05V |
| 3.00V | 11.50V | 12.60V |

A fan fault is defined as a fan RPM below 1,000 \pm 200 RPM during normal operation. This fault is inhibited for 15 \pm 5 seconds when the power supply outputs are first powered on. This allows time for the fan to come up to speed and the fan detects circuitry to stabilize.

A fault on two fans turns off the power supply. See Section 5.2.

Note: Fan speed control must operate even if no AC is applied to the power supply. Fan power comes from the 12V bus after the OR'ing diode. The control circuit power comes from either the 12V bus and/or the $3.3V_{\text{stbv}}$ bus.

5.4.10 Power Supply Module LED indicators

There are three LEDs on the rear of the power supply, next to the AC input power connector.

5.4.10.1 Power Supply Fail

The amber power supply fail LED is driven by internal circuitry. It lights when a power rail has failed. The LED is not lit if the supply turns off due to PS_KILL. The LED illuminates even if the power supply is in a latched state. The only time during a fault when it does not illuminate is if the $+3.3V_{stbv}$ is lost.

5.4.10.2 Power Good

The green power good LED is driven by internal circuitry. It lights whenever PWRGD is asserted.

5.4.10.3 AC OK

The green AC OK LED is driven by internal circuitry. It lights whenever VIN_GOOD is asserted.

6. Power Distribution Board

This section describes the Intel[®] Server Platforms SR6850HW4 and SR6850/M power distribution board and is organized as follows:

Section 6.1: Introduction

An overview of the platforms' power distribution board and board layout.

Section 6.2: Signal Descriptions and-pin-outs

Summarizes the platforms' power distribution board internal signals and connector signals, and the connector signal-pin names and the signal descriptions.

6.1 Introduction

The platforms' power distribution board provides docking connectors for the hot-swap power supply modules. It distributes power to the Intel® Server Platform SR4850HW4 SCSI backplane board and Intel® Server Board Set SE8501HW4 mainboard as well as power consumption information to the Intel® Server Board Set SE8501HW4 mainboard via a group of comparators. The board contains EEPROM FRU information storage but has no logic on it; it is a pass-through board. The signals shared between the two power supplies are shown in the diagram

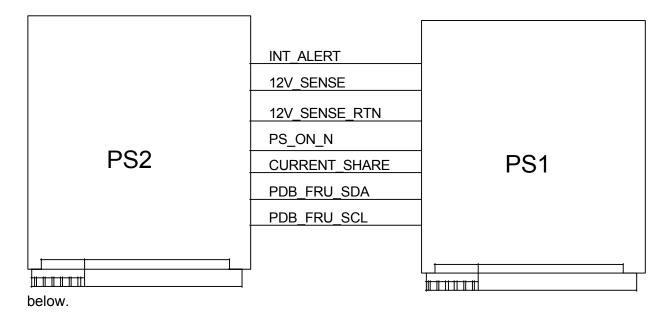


Figure 24. Power Supply Signal Sharing

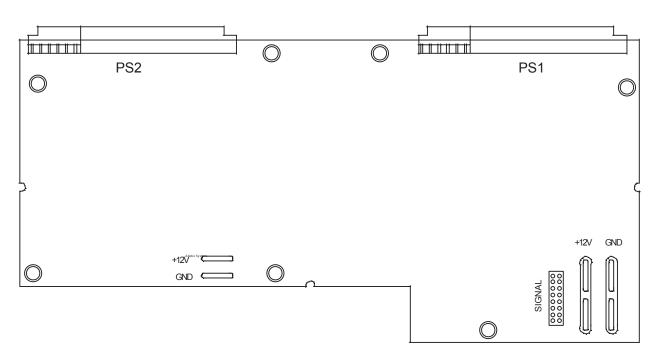


Figure 25. Power Distribution Board Layout

6.2 Signal Descriptions and-pin-outs

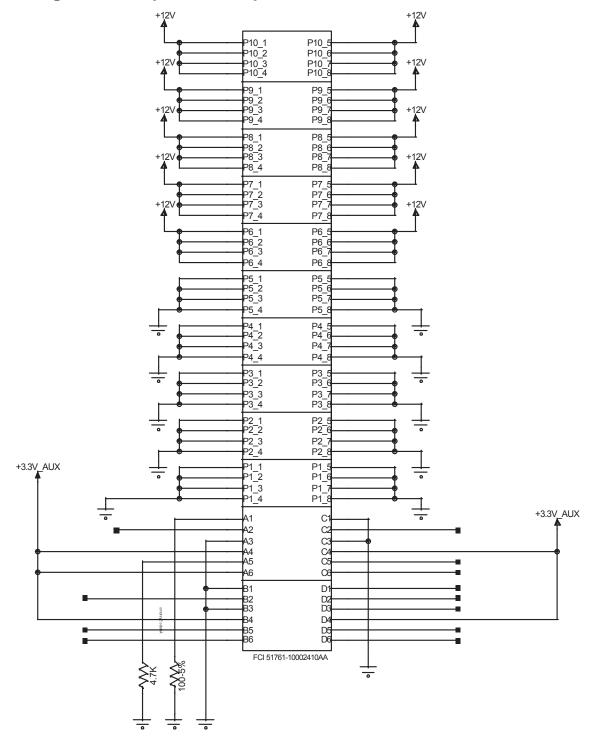


Figure 26. Power Distribution Board to Power Supply Module Docking Connector Signals

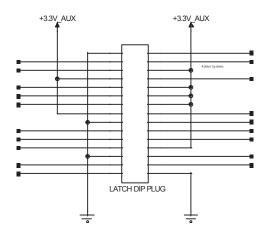


Figure 27. Mainboard Connector Signals

6.2.1 Remote On/Off (-PS_ON)

The power supply DC outputs are enabled when this signal is pulled low, below 0.8V. In the low state, the input will not source more than 1mA of current. The DC outputs are disabled when the input is driven higher than 2.4V, or open circuited.

Provisions for de-bouncing are included in the –PS_ON circuitry. This prevents the power supply from oscillating on and off at startup.

6.2.2 Power Good Signal (POK or P_GOOD)

A power good signal is asserted or driven high by the power supply to indicate that all outputs are valid. If any of the outputs fails, this output is driven low.

If AC main power is lost, or if a fan has failed, this signal must be driven low at least 1ms before any of the outputs go out of regulation.

The output is an open collector/drain. It is capable of driving the output below 0.4V with a load of 4mA. The output has an internal pull-up resistor of $1K\Omega$ between the output and $+3.3V_{stby}$. The pull-up is connected to the anode side of the $+3.3V_{stby}$ OR'ing diode.

This output also goes to I²C port P5.

6.2.3 VIN GOOD

This signal is asserted, driven high, by the power supply to indicate that the input voltage meets the minimum requirements of the input voltage range. Within 12ms after falling outside the input voltage requirements, the output must be driven low.

The output is an open collector/drain. It is capable of driving the output below 0.4V with a load of 4mA. The output has an internal pull-up resistor of $1K\Omega$ between the output and $+3.3V_{stby}$. The pull-up is connected to the anode side of the $+3.3V_{stby}$ OR'ing diode.

This output also goes to I²C port P4.

7. SCSI Backplane Board

This section describes the platforms' SCSI backplane board and is organized as follows:

Section 7.1: Introduction

Provides an overview of the platforms' SCSI backplane board, showing functional blocks and the board layout.

Section 7.2: Functional Architecture

Describes the platforms' SCSI backplane board functional blocks.

Section 7.3: Signal Descriptions

Summary of the platforms' SCSI backplane board internal signals and connector signals, and the connector signal-pin names and the signal descriptions.

Section 7.4: Electrical, Environmental, and Mechanical Specifications

Specifies operational parameters and considerations, and connector-pinouts.

7.1 Introduction

The platforms' SCSI backplane board supports up to ten hot-swap Ultra320* SCSI hard disk drives mounted into the chassis. The board provides drive status information and allows adding, removing and replacing hard disk drives without powering down the system. The following block diagram, architectural overview, and placement diagram provide an overview of the platforms' SCSI backplane board.

7.1.1 Block Diagram

The block diagram divides SCSI backplane board into physical and functional blocks. Arrows represent buses and signals. Blocks represent the physical and functional blocks.

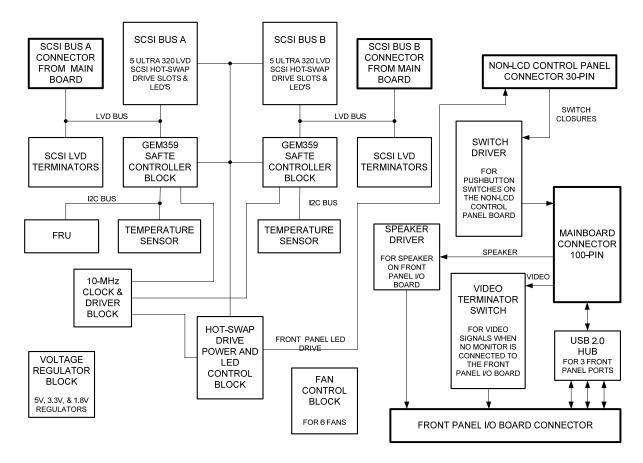


Figure 28. SCSI Backplane Board Block Diagram

7.1.2 Architectural Overview

The SCSI backplane board provides the following functions for the platform.

- Ultra320* SCSI bus passes SCSI signals between the hot-swap hard disk drives and the Intel® Server Board Sets SE8501HW4 and SE8500HW4 mainboards
 - Two standard 68-pin SCSI connector provides connection to the Intel[®] Server Board Set SE8501HW4 mainboard or Intel[®] Server Board Set SE8500HW4 mainboard
 - Ten 80-pin SCA-2 blind-mate connectors connect to SCSI hard disk drives
- Fault tolerant enclosure management
 - SAF-TE
 - SCSI power control
 - LED control logic
- Server management
 - I²C interface
 - I²C Serial CMOS EEPROM (FRU)
 - Temperature sensors (primary ambient for system)
- Voltage regulators
 - 12VDC to 5VDC
 - 5VDC to 3.3VDC
 - 5VDC to 1.8VDC
- System fan control
- USB 2.0 Hub
- Driver circuit for the platforms' front panel I/O board speaker
- Buffering for the buttons on the button control panel

7.1.3 Component Location

Figure 29 and shows the placement of the major components and connectors on the SCSI backplane board.

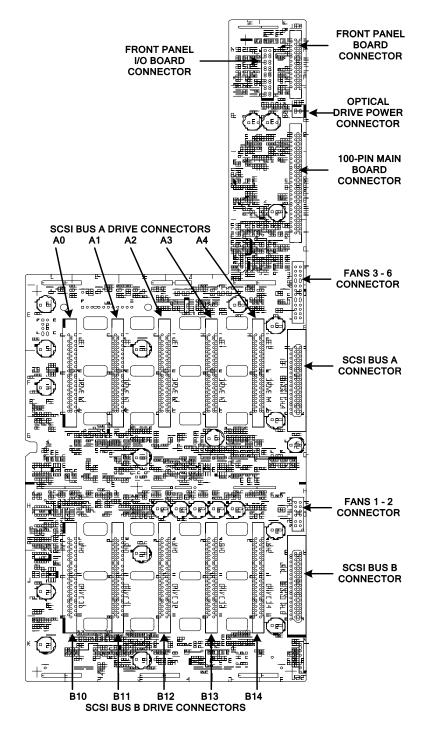


Figure 29. SCSI Backplane Board Component Placement (Primary Side)

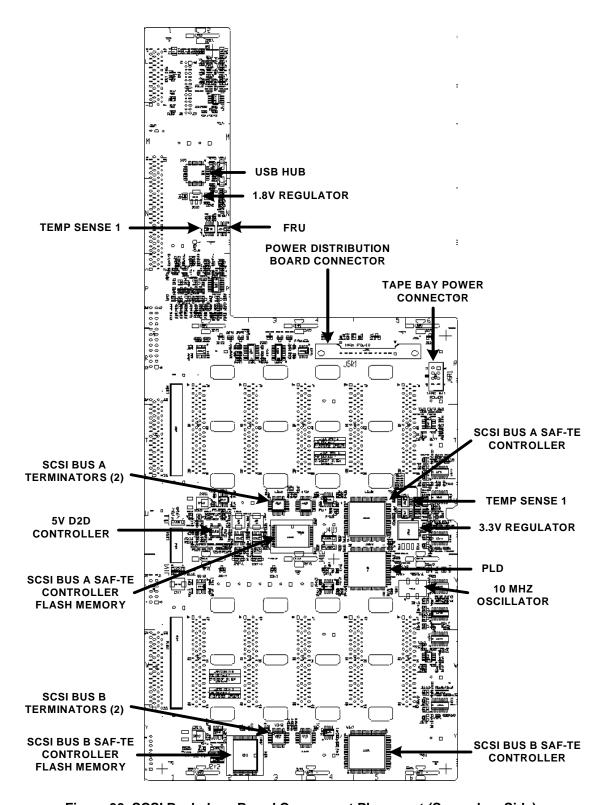


Figure 30. SCSI Backplane Board Component Placement (Secondary Side)

7.2 Functional Architecture

This section provides an architectural description of the platforms' SCSI backplane board functional blocks.

7.2.1 SCSI Buses

The SCSI backplane board passes the SCSI bus from the Intel® Server Board Set SE8501HW4 mainboard to the internal hot-swap SCSI hard disk drives. Each bus is Ultra320* SCSI low-voltage differential (LVD) capable. Single-ended (SE) drives are not supported in the hot-swap disk drive bay. Do not install an internal SE drive because the behavior of the drives is unpredictable and data corruption could result. This bus is comprised of 68 signals, operating at an 80MHz clock rate. The SCSI bus is capable of a 320MB data rate, from double transition (DT) data transfers on a two-byte wide bus. The bus attaches to the Intel® Server Board Set SE8501HW4 mainboard with a standard 68-pin SCSI connector.

320 MB/s = 2 byte bus * 80 MHz clock * double transitions.

Note: Drives and the SCSI controller on the Intel[®] Server Board Set SE8501HW4 mainboard negotiate the actual SCSI bus data rate.

7.2.2 SCSI Drive Power Control

SCSI power control is provided under control of the Programmable Logic Device (PLD). SCSI power control includes drive power switching, initial power-on charge pumping, over-current protection, system status notification, and drive status LEDs.

The system is notified when a hot-swap SCSI hard disk drive is detected. The SCSI backplane board applies power to the designated hot-swap SCSI hard disk drive and illuminates the status LED to provide visual indication of the event.

7.2.2.1 Internal SCSI Drive Power Switching

Each SCSI drive is supplied with +12V and +5V. Separate MOSFET switches are used to apply and remove +12V and +5V to each hot-swap SCSI hard disk drive.

7.2.2.2 Initial Power-on Charge Pumping

An initial current surge (up to 20A) is applied when power is first applied to a hot-swap SCSI hard disk drive. To reduce this initial current surge the SCSI backplane board charge pumps the drives for ~700µs. Charge pumping the hard disk drives keeps the average power-on current to approximately 3A.

7.2.2.3 Over-current Protection (OCP)

If either power rail for a drive exceeds 6A on 12V or 4.5A on 5V, the MOSFET switch for the out-of-spec rail is turned off. Removing power protects the MOSFET and the platform from damage if a short occurs on one of the power rails. After one-third of a second, the MOSFET is turned on to see if the short has been removed. It will continue turning on and checking for a short every one-third of a second until the system instructs the SCSI backplane board to remove power or until the fault disappears.

When the MOSFET is first enabled, the over current condition is not detected during the power-up period. This no-OCP period allows the initial current surge produced by many hot-swap SCSI hard disk drives. The power-up period is short enough to prevent damage to occur to the MOSFETS or the platform.

7.2.2.4 Power Control Interlock

The power control interlock prevents drives from powering on at the same time. Since only one hot-swap SCSI hard disk drive can power on at once, the board power requirements can be kept lower. Drives power on at one-third second intervals.

7.2.2.5 System Status Notification

Hot-swap SCSI hard disk drive status information is collected by the Qlogic* GEM359 SAF-TE controller for each bus. The controller passes the information to the server management via the global I²C bus and enclosure management information via the SCSI bus.

7.2.2.6 SCSI Status LEDs

The status LEDs give the user a visual indication of the status of each hot-swap SCSI hard disk drive. A single bi-color (amber and green) LED is present for each drive. The LEDs use a combination of color and blinking frequency to indicate multiple conditions.

The hot-swap SCSI hard disk drive status LEDs are located on the SCSI backplane board and projected out the front system by light pipes on the drive carrier. The states of the LEDs are described in Table 38.

 LED State
 Description

 Green on
 Drive is being initialized

 Green blinking
 Drive is active

 Amber on
 Drive/slot failure

 Amber slow blinking (~1Hz)
 Predictive drive/slot failure or array rebuild is in process

 Amber fast blinking (~2.5Hz)
 Array rebuild interrupted, rebuild on empty slot, or identify slot

Table 38. Hot-swap SCSI Hard Disk Drive LED Details

7.2.3 SCSI Enclosure Management

SCSI enclosure management allows the SCSI backplane board to report hot-swap SCSI hard disk drive status via the SCSI bus. This information is normally consumed by a RAID controller that supports enclosure management; the optional ROMB accessory supports this feature. The SCSI enclosure management subsystem consists of a Qlogic* GEM359 controller, flash, and PLD.

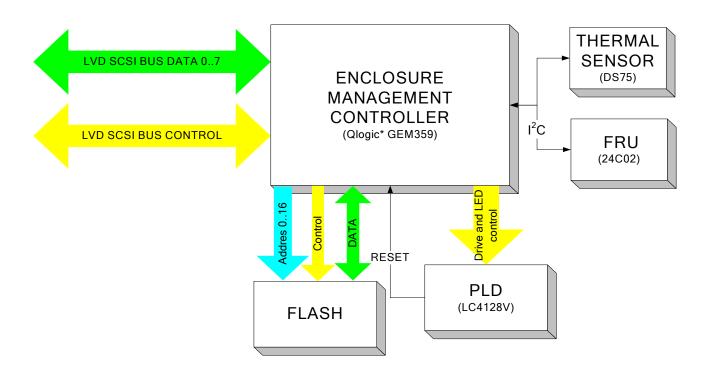


Figure 31. Enclosure Management Signal Flow Diagram

7.2.3.1 Qlogic* GEM359 Enclosure Management Controller

The GEM359s send board and drive information to both the SCSI and IPMB bus. The GEM359s also act on requests from both the SCSI bus and global I²C bus. GEM359s GPIOs send LED information to the PLD.

7.2.3.2 4-Mb Flash

The GEM359s code is stored in a 4-Megabit FLASH (512K x 8). The FLASH boot block is in the top 16k of the block. The boot block is write-protected. Non-protected FLASH can be updated through the IPMB bus.

7.2.3.3 PLD

The PLD governs the SCSI power control circuit and controls the LEDs. The PLD is an In-System Programmable (ISP) with an 8-pin header connector.

7.2.4 Server Management Interface

The SCSI backplane board supports the following server management features:

- Local I²C Interface
 - Field Replaceable Unit (FRU)
 - Temperature sensor
 - Microcontroller interface (Hot-swap Controller)
- System I²C Interface
 - Microcontroller IPMB interface
 - I²C/SM Bus (for fan monitoring)

7.2.4.1 Local I²C Bus

The Bus A local I²C bus connects the DS75 (or equivalent) thermal sensor and Atmel* AT24C02N (or equivalent) serial EEPROM (with FRU data) to the microcontroller. This thermal sensor is used by the BMC for the ambient temperature of the system.

7.2.4.2 Isolated Global I²C Bus (IPMB)

The global I²C bus connects the controllers to the system. The global I²C bus is isolated from the system until the system PWRGRD reaches the SCSI backplane board.

7.2.4.3 I²C I/O Bus

The I²C I/O bus connects the Intel[®] Server Board Set SE8501HW4 mainboard microcontroller to the platforms' front panel I/O board, fan control and the USB hub.

7.2.4.4 I²C Addresses

Four I²C devices and their addresses are listed in Table 39 and Table 40. The following I²C devices can be addressed on or through the SCSI backplane board:

- Hot-swap controller (HSC)
- FRU EEPROM
- Temperature sensor
- Fan controller

Table 39. I²C Local Bus Addresses

| Device | Address | Bus/Location | Description |
|---------|---------|---|---|
| AT24C02 | 0xA0 | 0xA0 Legacy I ² C/SCSI backplane board Private SCSI backplane board FRU EEPROM | |
| DS75 | 0x90 | Legacy I ² C /SCSI backplane board | Private SCSI backplane board temperature sensor |

Table 40. Global I²C Bus Addresses (IPMB Bus)

| Device | Address | Bus/Location | Description |
|--------------|---------|--|---------------------------------|
| Bus A GEM359 | 0xC0 | Legacy I ² C/SCSI backplane board | Microcontroller public IPMB bus |
| Bus B GEM359 | 0xC2 | Legacy I ² C/SCSI backplane board | Microcontroller public IPMB bus |

Table 41. I²C IO Bus Address

| Device | Address | Bus/Location | Description |
|---------|---------|--|--------------------------------|
| PCA9555 | 0x42 | Legacy I ² C/SCSI backplane board | Microcontroller public I/O bus |

7.2.5 Resets

The PCI_RST_BP_N signal from the Intel[®] Server Board Set SE8501HW4 mainboard via the 100-pin connector provides the principal reset for the logic on the SCSI backplane board. The signal resets the USB hub and SCSI drive power sequencing timing in the PLD. The PLD resets the GEM359s and their flash chips.

The PCA9555 device used to control the fans has an internal power-on reset that configures all its I/O-pins as inputs.

7.2.6 Connector Interlocks

7.2.6.1 Mainboard Cable Connector

The SCSI backplane board has an interlock on the 100-pin connector so the Intel[®] Server Board Set SE8501HW4 mainboard can detect its presence.

7.2.6.2 SCA-2 Connector

The SCSI backplane board uses an interlock to determine if a hot-swap SCSI hard disk drive is present. This interlock is defined by the SCSI_MATED# signals. Drive presence is used by enclosure management.

7.2.7 Clock Generation

The SCSI backplane board has a single, 10.0MHz, local clock. It supplies a 5V-rail clock input to the GEM359s and PLD. The clock is separately buffered by a 74LVT244.

The SMSC* USB20H04 USB hub has its own built-in 24MHz crystal oscillator that uses an external crystal.

7.2.8 Programmed Devices

Four programmed devices are on the SCSI backplane board:

- FLASH: Flash contains program code to be run by the onboard microcontroller, the HSC. Memory configuration: 512 K x 8.
- Field Replaceable Unit (FRU): The FRU is programmed at the factory. Memory configuration: 256 x 8 serial.
- USB hub circuit: The USB hub circuit has a serial EEPROM programmed with configuration data for the USB hub controller. Memory configuration: 256 x 8 serial.
- Programmable Logic Device (PLD): The PLD governs the SCSI power control circuit, controls LEDs, and provides a deglitching function for the Flash chips. The PLD is independently In-System-Programmable (ISP) with an 8-pin header connector.

7.3 Signal Descriptions

The following notations are used to describe the signal type, from the perspective of the platforms' SCSI Backplane Board:

- I Input-pin to the platforms' SCSI Backplane Board
- O Output-pin from the platforms' SCSI Backplane Board
- I/O Bi-directional (input/output)-pin
- PWR Power supply-pin

The signal description also includes the type of buffer used for the particular signal:

- LVD Low Voltage Differential SCSI
- SE Standard Single Ended SCSI
- TTL 5V TTL signals
- CMOS 5V CMOS signals
- Analog Typically a voltage reference or specialty power supply
- hs This suffix is added to indicate high-speed requirements that make modifications subject to review

7.3.1 Power from the Power Distribution Board

The SCSI backplane board receives only +12V from the Power Distribution Board through a 12-pin connector. These-pins are tied together and Table 42 provides a summary of the power connector-pins.

Table 42. Power Interface Signals

| Signal | Туре | Driver | Name and Description |
|--------|------|--------|---|
| +12V | 1 | PWR | +12 Volt supply from Power Distribution Board |

7.3.2 Front Panel Power Connector

Table 43 is a summary of the platforms' front panel I/O board power connector-pins.

Table 43. Front Panel I/O Board Power Interface Signals

| Signal | Туре | Driver | Name and Description |
|-----------------------|------|--------|---|
| +3.3V _{stby} | I | PWR | +3.3 Volt standby supply from Front Panel I/O Board |
| +3.3V | 0 | PWR | +3.3 Volt supply to Front Panel I/O Board |
| +5V | 0 | PWR | +5 Volt supply to Front Panel I/O Board |

7.3.3 Front Panel I/O Board Ribbon Cable Connector

The 30-pin platforms' front panel I/O board ribbon cable connector carries signals to and from the SCSI backplane board. Table 44 provides a description of the front panel I/O board ribbon cable connector. See Section 4 for pin-outs.

Table 44. Front Panel I/O Board Ribbon Connector Signal Description

| Signal | Type | Driver | Name and Description |
|------------------------|------|--------|---|
| FP_ID_BTN_N | I | Switch | ID button, ground when pressed |
| FP_PWR_BTN_N | I | Switch | Power button, ground when pressed |
| FP_RST_BTN_N | I | Switch | Reset button, ground when pressed |
| SYS_STATUS_GRN_LED_R_N | 0 | | Drives the front control panel system status green LED under mainboard control |
| SYS_STATUS_AMB_LED_R_N | 0 | | Drives the front control panel system status amber LED under mainboard control |
| FP_ID_LED_R_N | 0 | | Drives the front control panel ID blue LED under mainboard control |
| FP_PWR_LED_R_N | 0 | | Drives the front control panel power green LED under mainboard control |
| HDD_LED_ACT_R_N | 0 | | Drives the front control panel drive active green LED when either a SCSI drive or an SATA drive is active |
| HDD_LED_FLT_R_N | 0 | | Drives the front control panel drive fault amber LED to indicate a SCSI drive fault |
| NIC1_LINK_LED_R_N | 0 | | Drives the front control panel LAN1 green LED to indicate status of LAN1 on the mainboard |
| NIC2_LINK_LED_R_N | 0 | | Drives the front control panel LAN22 green LED to indicate status of LAN2 on the mainboard |
| I2C_IPMB_SCL | I/O | | This-pin supplies an isolated version of the global IPMB Bus clock to the front control panel. |
| I2C_IPMB_SDA | I/O | | This-pin supplies an isolated version of the global IPMB Bus data to the front control panel. |
| +5V | 0 | | Power for the front control panel |
| +5V STBY | 0 | | Power for the blue LED on the front control panel |
| GND | 0 | | Ground, signal common |

7.3.4 LVD SCSI 68-pin Connector

Each 68-pin LVD SCSI connector carries SCSI signals between the SCSI backplane board. The Intel® Server Board Sets SE8501HW4 and SE8500HW4 mainboards are unshielded. Table 45 provides a description of the LVD SCSI connector.

Table 45. LVD SCSI Connector Signal Description

| Signal | Type | Driver | Name and Description |
|-----------------------------------|------|--------|--|
| LVD_DB[150]_[P, N] | I/O | LVD hs | SCSI data bus. The data bits for the differential SCSI bus. |
| LVD_DBP_[P, N] LVD_DBP1_[P, N] | I/O | LVD hs | SCSI data parity. Support parity on the SCSI bus. DB_P0[P/N] supports parity for data [70]. DB_P1[P/N] supports parity for data [158]. |
| DIFFSENSE | I | Analog | Differential sense. The voltage level determines the operating mode of the target devices on the SCSI bus. If the voltage on the DIFFSENSE signal is from –0.35 V to +0.5 V the mode will be SE. If it is from +0.7 V to 1.9 V the mode will be LVD. |
| LVD_ATN_[P, N] | I/O | LVD hs | SCSI bus attention. Asserted by a SCSI device in initiator mode to alert the target that the initiator has a message to transfer. |
| LVD_BSY_[P, N] | I/O | LVD hs | SCSI bus busy. Indicate that the SCSI bus is being used. Can be driven by both the initiator and the target device. |
| LVD_ACK_[P, N] | I/O | LVD hs | SCSI bus acknowledge. Driven by an initiator, indicating an acknowledgement for a SCSI data transfer. |
| LVD_RST_[P, N] | I/O | LVD hs | SCSI bus reset. Indicate a SCSI bus reset condition. |
| LVD_MSG_[P, N] | I/O | LVD hs | SCSI bus message phase. Driven by a SCSI target to indicate it is in the Message Phase. |
| LVD_SEL_[P, N] | I/O | LVD hs | SCSI bus select. Used by an initiator to select a target or by a target to reselect an initiator. |
| LVD_CD_[P, N] | I/O | LVD hs | SCSI bus control/data phase. Driven by a target, these-pins indicate that control or data information is being transferred over the SCSI bus. |
| LVD_REQ_[P, N] | I/O | LVD hs | SCSI bus request. Driven by a target, these-pins indicate a request for a SCSI data-transfer handshake. |
| LVD_IO_[P, N] | I/O | LVD hs | SCSI bus I/O phase. Driven by the target, these-pins control the direction of data transfer on the SCSI bus. When asserted, this signal indicates input to the initiator. When not asserted, this signal indicates output from the initiator. |
| GND | I/O | PWR | Ground. Provide secondary ground reference. |

7.3.5 SCA2 80-pin Drive Connectors

The SCA2 connector carries power and signal between the SCSI backplane board and hot-swap SCSI hard disk drives. The LVD SCSI bus signals are driven by either the Intel® Server Board Set SE8501HW4 mainboard SCSI controller, the LVD transceiver, or the hot-swap SCSI hard disk drives. Table 46 provides a description of each signal on the SCSI connectors.

Table 46. LVD SCSI Bus Signals

| Signal | Type | Driver | Name and Description |
|--------------------|------|----------|--|
| LVD_DB[150]_[P, N] | I/O | LVD hs | SCSI data bus. Along with the DBP[1/0][P/N]-pins they form the bidirectional SCSI data bus. |
| LVD_DBP_[P, N] | I/O | LVD hs | SCSI data parity. Support parity on the SCSI bus. |
| LVD_DBP1_[P, N] | | | DBP[P/N] supports parity for data [70] |
| | | | DBP1[P/N] supports parity for data [158] |
| DIFFSENSE | I | Analog | Differential sense. Monitor the DIFFSENSE signal from the terminator. The voltage level determines the operating mode of the target devices on the SCSI bus. If the voltage on the DIFFSENSE signal is from –0.35V to +0.5V the mode will be SE. If it is from +0.7V to 1.9V the mode will be LVD. |
| LVD_ATN_[P, N] | I/O | LVD hs | SCSI bus attention. Asserted by a SCSI device in initiator mode to alert the target that the initiator has a message to transfer. |
| LVD_BSY_[P, N] | I/O | LVD hs | SCSI bus busy. In SE mode, these-pins are bi-directional and are asserted to gain use of the SCSI bus and to indicate that that SCSI bus is in use. |
| LVD_ACK_[P, N] | I/O | LVD hs | SCSI bus acknowledge. Asserted by a SCSI device in initiator mode to acknowledge the target's request for a data transfer. |
| LVD_RST_[P, N] | I/O | LVD hs | SCSI bus reset. In SE mode, these-pins are bi-directional and are asserted when all the SCSI devices attached to the SCSI bus need to be reset. |
| LVD_MSG_[P, N] | I/O | LVD hs | SCSI bus message phase. Asserted by a SCSI device in target mode to indicate the Message In or Message Out phase. |
| LVD_SEL_[P, N] | I/O | LVD hs | SCSI bus select. In SE mode, these-pins are bi-directional and are asserted by the controller when attempting to select or reselect a SCSI device. |
| LVD_CD_[P, N] | I/O | LVD hs | SCSI bus control/data phase. Asserted or de-asserted by a SCSI device in target mode to indicate that control or data information is being transferred over the SCSI bus |
| LVD_REQ_[P, N] | I/O | LVD hs | SCSI bus request. Asserted by a SCSI device in target mode to indicate that the target is requesting a data transfer over the SCSI bus. |
| LVD_IO_[P, N] | I/O | LVD hs | SCSI bus I/O phase. Asserted by a SCSI device in target mode to indicate the direction of data movement on the SCSI bus between the target and the initiator. |
| SCSI_ID | 0 | GND/OPEN | SCSI ID. Sets internal SCSI ID depending on slot. Drive 1 has SCSI address 0. Drive 2 has SCSI address 1 and so on. |
| SCSI_MATED_L [1-5] | I/O | TTL | SCSI MATED. Determine if SCSI is present and has proper contact. |
| GND | I/O | PWR | Ground. Provide secondary ground reference. |
| +12V | 0 | PWR | +12 Volt supply. Max 1A of continuous current/6A peak current. |
| +5V | 0 | PWR | +5 Volt supply. Max 1.4A of continuous current/6A peak current. |

7.3.6 Fans

Each fan has an integral amber LED with a grounded cathode. This provides a small current to a transistor that drives the FAN[10..1]_PRES signal. This signal is read by server management through U2P1, and the PCA9555 I²C Port. Server management can also use U2P1 to turn on a FAN[10..1]_LED signal. FET drivers boost the current through the LED to brighten it.

The FAN_PWM signal from the mainboard controls the fan speed. The FAN[10..1]_TACH signal is shaped by an FET buffer and driven to the mainboard as FAN[10..1]_TACH_BUFF for determination of fan speed.

7.3.7 Internal Logic Signals

Table 47 is a summary of the signals that route between logic on the SCSI backplane board.

Table 47. Internal Logic Signals

| | Signal | Туре | Driver | Name and Description |
|--------------------------|----------------------|------|--------|--|
| Clks | CLK_10MHz | 0 | CMOS | 10-MHz clock that is used by the GEM359 and PLD. |
| | ADDR<160> | 0 | CMOS | Address/bus. Address bus for the FLASH. |
| | PROM_VPP_L | 0 | CMOS | FLASH PROGRAM VOLTAGE ENABLE. Driven by the GEM359 to all FLASH to be programmed. |
| GEM359 Logic | PROM_OE_L | 0 | CMOS | FLASH output enable. Driven by the GEM359 to enable the FLASH for writing data on the bus. |
| Control | PROM_CE_L | 0 | CMOS | FLASH output enable. Driven by the PLD to enable the FLASH. |
| | PROM_WE_L | I | CMOS | FLASH chip enable. Driven by the GEM359 to enable writing to the FLASH. |
| | KCK_5V_L [1-10] | 0 | Analog | 5 Volt kick start. Primes 5 Volt FET to start delivering power to a drive. |
| | KCK_12V_L [1- 10] | 0 | Analog | 12 Volt kick start. Primes 12 Volt FET, to start delivering power to a drive. |
| | FLT_5V_L [1-10] | I | CMOS | 5 Volt hot-swap fault. Indicates greater than 5A of current drawn from 5V rail. |
| SCSI Power Control | FLT_12V_L [1-10] | I | CMOS | 12 Volt hot-swap fault. Indicates greater than 5A of current drawn from 12V rail. |
| Control | STP_5V_L[1-10] | I | Analog | 5 Volt stop. Stops 5 Volt FET from delivering power to a drive. |
| | STP_12V_L[1-10] | I | Analog | 12 Volt stop. Stops 12 Volt FET from delivering power to a drive. |
| | PWR_TIMER | 0 | Analog | Power timer. Starts one second timer for FET reset. |
| | TMR_DONE | I | Analog | Timer done. One second reset timer complete. |
| | FAN_PRES[1-6] | I | Analog | Fan is present on system |
| Fan | FAN_LED[1-6] | I | Analog | LED signal when fan was off line |
| Control | FAN_TACH[1-6] | I | Analog | Fan speed |

7.4 Electrical, Environmental, and Mechanical Specifications

This section specifies the operational parameters and physical characteristics for the platforms' SCSI backplane board. Further topics in this section specify normal operating conditions, mechanical specifications and connector interfaces to the board.

7.4.1 Electrical Specifications

The power budget for the SCSI backplane board and-pin-outs of the external interface connectors are defined in the following table.

Table 48. Electrical Specifications

| Feature | Absolute Maximum Rating |
|---|---|
| Voltage of any signal with respect to ground | -0.3V to Vcc ¹ to Vcc ¹ +0.3V |
| +3.3V _{stby} supply with respect to ground | -0.3V to +3.465V |
| +3 .3V supply with respect to ground | -0.3V to +3.465V |
| +5V supply with respect to ground | -0.3V to +5.25V |
| +12V supply with respect to ground | -0.3V to +12.6V |

Note: 1. Vcc refers to the supply voltage for the device.

7.4.1.1 Power Consumption

Table 49 shows the power consumed on each supply line for the SCSI backplane board.

Table 49. Maximum Power Consumption

| Devices | Power Dissipation | Ext/Int |
|----------------------|----------------------|---------|
| 12V | 180W | Ext |
| 5V | 100W | Int |
| 3.3V | 0.5W | Int |
| 3.3V _{stby} | 0.5W | Ext |
| 1.8V | 0.2W | Int |

Note: The numbers in the table are provided only to show design limits. Power consumption will vary, depending on the exact configuration.

7.4.1.2 Hot-Swap SCSI Hard Disk Drive Supplied Power

Hot-swap SCSI hard disk drives must fall within the power limits shown in Table 50. The SCSI backplane board works with drives that meet the following requirements.

Table 50. SCSI Backplane Board Power Limits per Drive

| Device constraint | +5 V | +12 V |
|-----------------------|-------|-------|
| Peak start current | 0.73A | 1.5A |
| Max operating current | 0.81A | 1.15A |
| Average idle | 0.68A | 0.61A |

7.4.1.3 Power Supply Requirements

The external and internal power supply must meet the following requirements:

- Rise time of less than 50ms (for all voltages).
- Delay of 5ms (minimum) from valid power-to-power good.

See Table 51 for voltage regulation requirements.

Table 51. DC Voltage Regulation

| DC Voltage | Acceptable Tolerance |
|-----------------------|----------------------|
| +5V | ± 5% |
| +12V | ± 5% |
| +3.3V | ± 5% |
| +3.3V _{stby} | ± 5% |
| +1.8V | ± 5% |

7.4.2 Mechanical Specifications

The board outline dimensions are 16.5 inches x 6.380 inches. The board thickness is 0.093 inches +.008/-.005 inches. All dimensions are in inches.

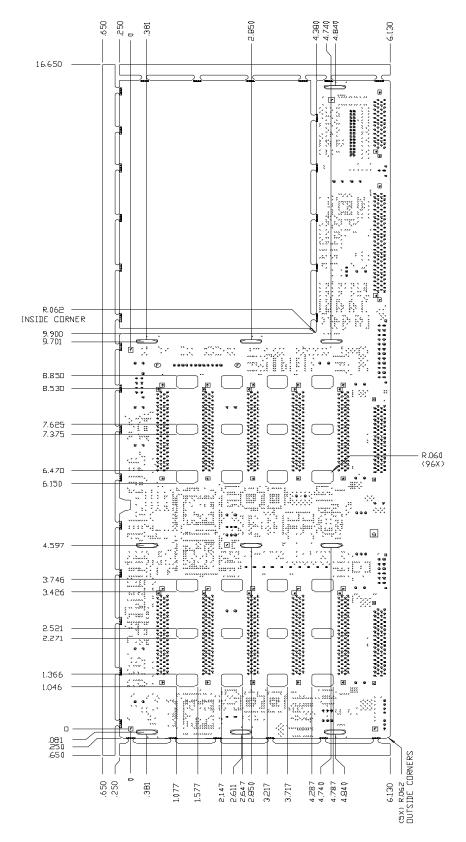


Figure 32. SCSI Backplane Board Component Placement (Primary Side)

8. SAS Backplane Board

This section describes the SAS (Serial Attach SCSI) Intel[®] Server Platforms SR6850HW4 and SR6850HW4/M backplane board. This section is organized as follows:

Section 8.1: Introduction

Provides an overview of the SAS backplane board showing functional blocks and board layout.

Section 8.2: Functional Architecture

Describes the SAS backplane board's functional blocks.

Section 8.3: Signal Descriptions

Summary of the SAS backplane board's internal signals and connector signals, the connector signal pin names and the signal descriptions. Signal mnemonics appear throughout this chapter.

Section 8.4: Electrical, Environmental, and Mechanical Specifications

Specifies operational parameters and considerations, and connector pinouts.

8.1 Introduction

The SAS backplane board is designed to give the end-user support for up to ten SAS hard drives in the Intel® Server Platform SR6850HW4/M chassis. The SAS option is not available for the Intel® Server Platform SR6850HW4. The SAS design enables easy use and replacement of the SAS hard drives without powering down the system. The following block diagram, architectural overview, and placement diagram will give a general idea of how the SAS backplane board works.

8.1.1 Block Diagram

The block diagram below breaks down the SAS backplane board into physical and functional blocks. Arrows represent buses and signals. Blocks represent the physical and functional blocks.

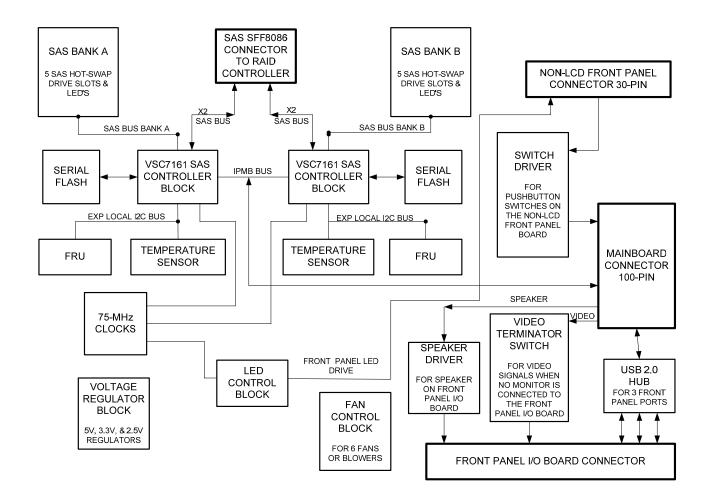


Figure 33. Intel® Server Platforms SR6850HW4 and SR6850HW4/M SAS Backplane Board Block Diagram

8.1.2 Architectural Overview

The Intel® Server Platform SR6850HW4/M SAS backplane board provides several functions for the system.

- 3Gbit SAS port expanders provide high speed serial data paths from the ten attached SAS hard drives to the mainboard via the Intel[®] SASROMB18E controller card.
 - SAS data between drives and mainboard are routed across a 4-port internal SAS cable. The board connects the backplane to the Intel® SASROMB18E controller card. This card is a PCI-Express* SAS RAID controller card plugged into one of the mainboard's PCI-Express* slots.
 - Two SAS expanders, each supporting five drives, are used to control SAS traffic flow between the drives and the Intel® SASROMB18E controller card.
- Enclosure Management.
 - SAS enclosure management per SES-2
 - Fault LED control logic
- Server management I²C interface
 - Fan presence sensing and fan fault LED control
 - I²C Serial EEPROM (FRU)
 - Temperature sensors
 - Expander controller firmware update capability
 - Interconnect for optional LCD front panel control board
- Voltage regulators
 - 12VDC to 5VDC
 - 5VDC to 3.3VDC
 - 5VDC to 2.5VDC
- System fan control for six fans
- USB 2.0 Hub
- Front panel control board video interconnect and termination
- Driver circuit for speaker on front panel I/O board
- Pushbutton signal buffering
- Power connectors for DVD and tape drive bay cables

8.1.3 Board Assembly

The following figures show the 2D view of the Intel $^{\$}$ Server Platform SR6850HW4/M SAS backplane board top and bottom assemblies.

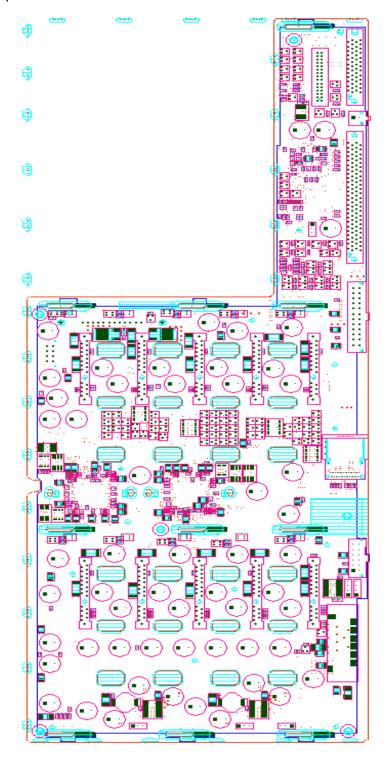


Figure 34. SAS Backplane Board Top Assembly

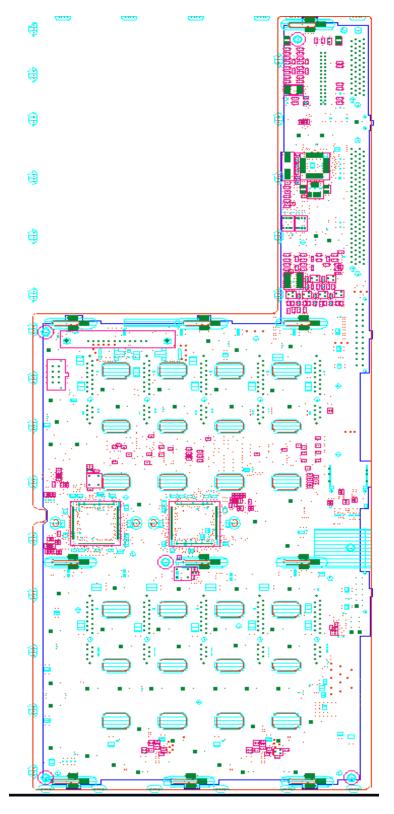


Figure 35. SAS Backplane Board Bottom Assembly

8.2 Functional Architecture

This section provides a more detailed architectural description of the Intel[®] Server Platform SR6850HW4/M SAS backplane board's functional blocks.

8.2.1 SAS Buses

The SAS buses are indirectly connected to the mainboard via the Intel® SASROMB18E Controller card. The card is plugged into the PCI-Express* slot on the mainboard. As a result, the Intel® SASROMB18E controller provides all SAS functionality and interfacing to the Intel® Server Platform SR6850HW4/M SAS backplane board. The Intel® Server Platform SR6850HW4/M SAS backplane board utilizes SAS expander devices to route data to/from each of the ten internal SAS drives from/to the controller.

Data movement between the SAS expanders on the SAS backplane board and the controller is achieved through the high-speed cable assembly. The cable assembly connects the Intel[®] SASROMB18E Controller card to the SAS backplane board. There are a total of four separate SAS busses or lanes that are contained within the high-speed cable assembly.

An SFF8087 mini connector is used to terminate each end of the cable assembly to the Intel® SASROMB18E Controller card and SAS backplane board. Each SAS lane operates in full-duplex serial mode and contains dedicated transmit and receive differential pairs for a total of eight differential pairs on the cable. As the four lanes converge on the SAS backplane board, two of the four lanes are routed to the primary SAS expander. The remaining two lanes are routed to the secondary expander. Each expander, in turn, routes data to the five SAS drives that are connected to its ports.

Each SAS expander consists of ten identical SAS ports:

- Two SAS ports are connected to the SFF8087 mini connector that routes data to/from the SAS controller card.
- Five of the ten SAS ports are used to connect to the five hot-pluggable SAS hard drives with each drive having a dedicated port.
- The remaining three ports for each expander are reserved.

All SAS channels on the backplane board are capable of 3Gbps data transmission on both transmit and receive paths. During system power-on and hot drive insertion, SAS data rates are negotiated to operate at 1.5Gbps or 3.0Gbps.

8.2.2 SAS Expander Functionality

The two SAS expanders on the backplane board contain embedded 32-bit RISC processors. These processors are used to control and monitor SAS hard drive functions and enclosure management functionality to satisfy SES-2 requirements. In addition, the expanders provide status and control of drive behavior such as link speed auto detection and negotiation, fault indication and error reporting.

Each expander uses its local I²C bus to maintain direct communication to on-board temperature sensors and EEPROMs that store FRU and SAS related data. In turn, temperature data and system FRU information are monitored and reported back to the mainboard via the IMPB bus.

Firmware updates for each SAS expander and the FRU can also be reprogrammed via the IMPB. The expanders offer the ability to individually control the output voltage at each of the ten attached ports. In addition the expanders provide reprogrammable pre-emphasis to optimize input signal quality. If a SAS hard drive is detected, the system will be notified. The SAS backplane board will apply power to the designated internal SAS hard drive. Status LEDs will provide the user with visual indicators for the hot-pluggable SAS hard drives.

8.2.2.1 Expander SPI Flash

Firmware for the Vitesse* VSC7161 SAS expander is stored in an 8-Megabit (Mb) SPI FLASH memory device. The SAS backplane board also has provisions to perform future firmware backup and revisioning by supporting a secondary SPI flash for each of the two on-board expanders. In addition, SAS related information and PHY specific configuration data can be stored in the secondary flash location. Each flash device can be updated via the IPMB bus.

8.2.3 SAS Drive Functionality

The SAS backplane board provides connections for a maximum of ten SAS hard drives. Each drive can be inserted and removed while the system is powered-on. Automatic detection and rate negotiation are performed after each insertion. The SAS backplane board provides +5V and +12V to each drive connector and supports in-rush current limiting to 300mA during hot-swapping.

8.2.4 Power Control Interlock

The power control interlock is part of the SAS specification. This prevents drives from powering on at the same time. Since only one drive can power on at once the board power requirements can be kept lower.

8.2.4.1 System Status Notification

Internal SAS hard drive status information is collected by the SAS expander. The information can be monitored by accessing each expander's serial port. Output drive strength and input preemphasis may also be controlled via the serial port. In addition, any drive data can be routed to server management via the IPMB.

8.2.4.2 SAS Status LEDs

The SAS status LEDs provide end-users with a visual indication of the drives' condition. There is a single bi-color (amber and green) LED for each drive. The LEDs use a combination of color and blinking frequency to indicate multiple conditions.

The hard drive status LEDs are located on the SAS backplane board and projected out the front of the carrier via light pipes. The states of the LEDs are described in the following table.

| LED State | Description |
|------------------------------|---|
| Green Oo | The hard drive is configured and ready for access. |
| Green blinking | The hard drive is active. |
| Amber on | Hard drive/slot failure. |
| Amber slow blinking (~1Hz) | A predictive hard drive/slot failure or rebuild in process |
| Amber fast blinking (~2.5Hz) | Hard drive rebuild interrupted, rebuild on empty slot, or identify slot |

Table 52. SAS Hard Drive LED Details

8.2.5 SAS Enclosure Management

SAS enclosure management allows the SAS backplane board to report SAS drive status and backplane temperature readings to a SAS RAID controller that interfaces with enclosure management. The SAS enclosure management subsystem consists of the two SAS expanders, and associated SPI Flash and EEPROM memory devices.

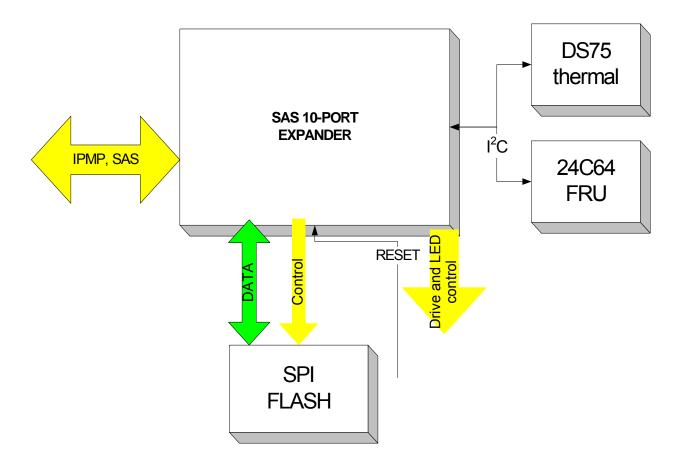


Figure 36. Enclosure Management Signal Flow Diagram

8.2.6 Server Management Interface

The SAS backplane board supports the following server management features:

Local I²C Interface

- SAS backplane field replaceable Unit (FRU).
- SAS backplane temperature sensor
 - One temperature sensor is attached to the local I²C bus of each of the two expanders.
- Micro-controller interface

System I²C Interface

Micro-controller IPMB interface.

8.2.6.1 Local I²C Bus

The Bus A local I²C bus connects the DS75 (or equivalent) thermal sensor and Atmel* AT24C64N (or equivalent) serial EEPROM (with FRU data) to the Bus A controller. Bus B's local I²C bus is connected the same as above.

8.2.6.2 Isolated Global I²C Bus (IPMB)

The global I²C bus connects the on-board SAS expanders to the server mainboard. The bus is isolated from the expanders until the PCI_RST_BP_N signal from the mainboard is deasserted.

The IPMB bus also goes to the front panel control connector for use with an LCD display.

8.2.6.3 I²C I/O Bus

The I2C_CP Bus connects the system server management controller to the PCA9555 device used for fan sensing and LEF control. The bus address list is provided in Table 53.

8.2.6.4 I²C Addresses

Four I²C devices and their addresses are listed in Table 53 through Table 55. There are seven I²C devices that can be addressed on the Intel[®] Server Platforms SR6850HW4 and SR6850HW4/M SAS backplane board.

- Hot swap micro controllers
- Intel[®] Server Platform SR6850HW4/M SAS backplane FRU EEPROM
- Intel[®] Server Platform SR6850HW4/M SAS backplane temperature sensors

Table 53. I²C Local Bus Addresses

| Device | Address | Bus | Description |
|---------|---------|--------------------|---|
| AT24C64 | 0xA0 | Expander local bus | Private SAS backplane FRU EEPROM on bus A local bus. (Bus B local bus also supports an identical device.) |
| DS75 | 0x90 | Expander local bus | Private SAS backplane temperature sensor for each expander |

Table 54. Global I²C Bus Addresses (IPMB Bus)

| Device | Address | Bus | Description |
|----------------|---------|-----------------------|----------------------------------|
| Bus A Expander | 0xC0 | IPMB system interface | Micro controller public IPMB bus |
| Bus B Expander | 0xC2 | IPMB system interface | Micro controller public IPMB bus |

Table 55. I²C IO Bus Addresses

| Device | Address | Bus | Description |
|---------|---------|-------------------------|--------------------------------|
| PCA9555 | 0x42 | I ² C_CP bus | Micro controller public IO bus |

8.2.7 Resets

The principal reset for logic on the SAS backplane board is supplied by the PCI_RST_BP_N signal from the mainboard via the 100-pin connector. The signal resets the USB Hub and the two SAS expanders.

The PCA9555 device being used to control the fans has an internal power-on reset that configures all its I/O pins as inputs.

8.2.8 Connector Interlocks

8.2.8.1 Baseboard Cable Connector

The SAS backplane board has an interlock on the 100-pin connector therefore, the mainboard can detect its presence.

8.2.9 Clock Generation

The SAS backplane board requires two separate clock frequencies to support SAS and USB operations. Two separate and independent 75MHZ HCMOS oscillators are used to drive the two SAS expanders. In addition, a 24MHz crystal is used to drive operation of the on-board USB Hub.

8.2.10 Programmed Devices

There are six programmed devices on the SAS backplane board.

8.2.10.1 Flash Memory

Each SAS expander uses two flash memory devices, a primary and secondary. The primary flash memory devices contain program code to be run by each onboard expander. The secondary flash devices can be used to perform program code backup and store additional SAS information.

Memory configuration: 64Mb SPI

8.2.10.2 Field Replaceable Unit (FRU)

The FRU is a serial EEPROM programmed at ATE.

Memory Configuration: 512Kb serial

8.2.10.3 USB EEPROM

The USB hub circuit has a serial EEPROM programmed at ATE with configuration data for the USB hub controller.

Memory Configuration: 256 x 8 serial

8.3 Signal Descriptions

The following notations are used to describe the signal type, from the perspective of the Intel[®] Server Platforms SR6850HW4 and SR6850HW4/M SAS backplane board:

I Input pin to the SAS backplane board

O Output pin from the SAS backplane board

I/O Bi-directional (input/output) pin

PWR Power supply pin

The signal description also includes the type of buffer used for the particular signal:

LVD Low Voltage Differential

TTL 5V TTL signals

CMOS 5V CMOS signals

3.3V CMOS 3.3V CMOS signals

Analog Typically a voltage reference or specialty power supply

hs This suffix is added to indicate high speed requirements that would

make any modifications subject to detailed review

8.3.1 Power Bay Connector

The Intel® Server Platforms SR6850HW4 and SR6850HW4/M SAS backplane board receives only +12V from the power distribution board thru a 12-pin connector. Table 56 is a summary of power connector pins, including the signal mnemonic, the name and description.

Table 56. Power Bay Interface Signals - J6P1

| Signal | Туре | Driver | Name and Description |
|--------|------|--------|---------------------------------|
| +12V | PWR | PWR | +12 Volt supply from power bay. |
| GND | PWR | PWR | Ground |

8.3.2 Front Panel Control Ribbon Cable Connector

The 50-pin front panel control ribbon cable connector carries signals between the Intel® Server Platforms SR6850HW4 and SR6850HW4/M SAS backplane and front panel control. Table 57 provides a description of the front panel control ribbon cable connector.

Table 57. Front Panel Control Ribbon Connector Signal Description – J6A1

| | Signal | Typ e | Name and Description | |
|------------------|----------------------------|----------|--|--|
| | FP_ID_BTN_N | I | ID pushbutton, ground when pressed. | |
| Switches | FP_PWR_BTN_N | I | Power pushbutton, ground when pressed. | |
| | FP_RST_BTN_N | I | Reset pushbutton, ground when pressed. | |
| | SYS_STATUS_GRN_LED_R_ N | 0 | Drives the front panel control system status green LED under mainboard control. | |
| | SYS_STATUS_AMB_LED_R_N | 0 | Drives the front panel control system status amber LED under mainboard control. | |
| | FP_ID_LED_R_N | 0 | Drives the front panel control I ID blue LED under mainboard control. | |
| | FP_PWR_LED_R_N | 0 | Drives the front panel control power green LED under mainboard control. | |
| LED Ctrl | HDD_LED_ACT_R_N | 0 | Drives the front panel control drive active green LED when either a SAS drive or an IDE drive is active. | |
| | HDD_LED_FLT_R_N | 0 | Drives the front panel control drive fault amber LED to indicate a SAS drive fault. | |
| | NIC1_LINK_LED_R_N | 0 | Drives the front panel control NIC1 green LED to indicate status of NIC1 on the mainboard. | |
| | NIC2_LINK_LED_R_N | 0 | Drives the front panel control NIC2 green LED to indicate status of NIC2 on the mainboard. | |
| I ² C | I2C_IPMB_SCL | I/O | This pin supplies an isolated version of the global IPMB Bus clock to the front panel control. | |
| | I2C_IPMB_SDA | I/O | This pin supplies an isolated version of the global IPMB Bus data to the front panel control. | |
| | +5V | 0 | Power for the front panel control. | |
| Power | +5V STBY | 0 | Power for the blue LED on the front panel control. | |
| | GND | 0 | Ground, signal common. | |

8.3.3 SAS 36-pin Connector

The SAS mini 4i 36-pin SFF8087 connector is used to carry four lanes of SAS signals to/from the SAS RAID controller card. Table 58 provides a description of the mini 4i SAS Connector.

Table 58. LVD SCSI Connector Signal Description – J6F1 (Bus A) and J6K1 (Bus B)

| Signal | Type | Driver | Name and Description |
|-------------------------|------|--------|--------------------------------------|
| HBA_EXPD0_PHY9_RX[P, N] | 1 | LVD hs | SAS RX DATA. Expander0 Lane0 RX data |
| HBA_EXPD0_PHY9_TX[P, N] | 0 | LVD hs | SAS TX DATA. Expander0 Lane0 TX data |
| HBA_EXPD0_PHY8_RX[P, N] | 1 | LVD hs | SAS RX DATA. Expander0 Lane1 RX data |
| HBA_EXPD0_PHY8_TX[P, N] | 0 | LVD hs | SAS TX DATA. Expander0 Lane1 TX data |
| HBA_EXPD1_PHY9_RX[P, N] | 1 | LVD hs | SAS RX DATA. Expander1 Lane0 RX data |
| HBA_EXPD1_PHY9_TX[P, N] | 0 | LVD hs | SAS TX DATA. Expander1 Lane0 TX data |
| HBA_EXPD1_PHY8_RX[P, N] | 1 | LVD hs | SAS RX DATA. Expander1 Lane1 RX data |
| HBA_EXPD1_PHY8_TX[P, N] | 0 | LVD hs | SAS TX DATA. Expander1 Lane1 TX data |
| GND | PWR | PWR | Ground. |

8.3.4 SAS Drive 22-pin Connectors

The Intel® Server Platforms SR6850HW4 and SR6850HW4/M SAS backplane board implements an extended height 22-pin SATA connector in order to accommodate the limited reach of the mating SAS drives. The backplane board provides ten identical drive connectors, five on bank A and five on Bank B. The SAS drives mate directly to the 22-pin connector. Table 59 provides a description of each signal on the SAS drive connectors.

Table 59. LVD SCSI Bus Signals – J1E1, J2E1, J3E1, J5E1, J6E2, J1H1, J2H1, J3H1, J5H1, and J6H3

| Signal | Type | Driver | Name and Description |
|-------------------------|------|--------|--|
| DRV[A,B] [04]_RX_[P, N] | I | LVD hs | SAS RX DATA. RX differential data from the drives |
| DRV[A,B] [04]_TX_[P, N] | 0 | LVD hs | SAS TX DATA. TX differential data to the drives |
| HD[A,B] [04]_PRESENT_L | I | TTL | SAS DRIVE DETECT. Active low presense detect |
| HD[A,B] [04]_ACT_LED_L | 0 | TTL | SAS ACTIVITY DETECT. Active low readiness indicator. Low-to-high transition to indicate activity |
| GND | PWR | PWR | Ground. |
| P12V | PWR | PWR | +12 Volt supply. Maximum 1 amp of continuous current. Maximum 4 amps peak current. |
| P5V | PWR | PWR | +5 Volt supply. Maximum 1.4 amps of continuous current. Maximum 4 amps peak current. |

8.3.5 Fan Signals

There are two fan power connectors on the SAS backplane board. The connectors control and supply the power for six fans in the system.

Table 60. Fan Power and Control J6G1

| J6G1 12 Pins | Туре | Signal |
|-----------------|------|-----------|
| 7, 10 | 0 | 12V |
| 1, 4, 9, 12 | 0 | GND |
| 2 | I | FAN1_TACH |
| 5 | I | FAN2_TACH |
| 8, 11 | 0 | FAN_PWM |
| 3 | I/O | FAN1_AMB |
| 6 | I/O | FAN2_AMB |

Table 61. Fan Power and Control J6E1

| J6E1 24 Pins | Туре | Signal |
|-----------------------------|------|-----------|
| 13, 16, 19, 22 | 0 | 12V |
| 1, 4, 7, 10, 15, 18, 21, 24 | 0 | GND |
| 2 | 1 | FAN3_TACH |
| 5 | 1 | FAN4_TACH |
| 8 | 1 | FAN5_TACH |
| 11 | I | FAN6_TACH |
| 14, 17, 20, 23 | 0 | FAN_PWM |
| 3 | I/O | FAN3_AMB |
| 6 | I/O | FAN4_AMB |
| 9 | I/O | FAN5_AMB |
| 12 | I/O | FAN6_AMB |

Each fan has an integral amber LED whose cathode is grounded, providing a small current to a transistor which drives the FAN[10..1]_PRES signal. This signal is read by server management through U2P1, the PCA9555 I²C Port. Server management can also use U2P1 to turn on a FAN[10..1]_LED signal. FET drivers then boost the current through the LED to make it bright.

The FAN_PWM signal from the mainboard controls the fan speed. The FAN[10..1]_TACH signal is shaped by an FET buffer and driven to the mainboard as FAN[10..1]_TACH_BUFF for determination of fan speed.

8.3.6 Internal Logic Signals

Table 62 is a summary of the signals that route between logic devices on the SAS backplane board.

Table 62. Internal Logic Signals

| | Signal | Туре | Driver | Name and Description |
|-------------------|-----------------|------|--------|---|
| Clks | CLK_75MHZ_EXPD0 | 0 | CMOS | 75-MHz Clock. Expander0 75MHZ clock |
| | CLK_75MHZ_EXPD1 | 0 | CMOS | 75-MHz Clock. Expander1 75MHZ clock |
| | EXPD0_SDO | I/O | CMOS | SPI DATA. Expander0 FLASH data |
| | EXPD0_SCK | 0 | CMOS | SPI CLOCK. Expander0 FLASH clock |
| | EXPD0_SCSPN | 0 | CMOS | SPI CHIP SELECT. Expander0 FLASH select |
| Expander | EXPD0_WP0_N | 0 | CMOS | SPI WRITE PROTECT. Active low Expander0 FLASH write protect |
| Memory Control | EXPD1_SDO | I/O | CMOS | SPI DATA. Expander1 FLASH data |
| Control | EXPD1_SCK | 0 | CMOS | SPI CLOCK. Expander1 FLASH clock |
| | EXPD1_SCSPN | 0 | CMOS | SPI CHIP SELECT. Expander1 FLASH select |
| | EXPD1_WP0_N | 0 | CMOS | SPI WRITE PROTECT. Active low Expander1 FLASH write protect |
| | EXPD0_SCSSN | 0 | CMOS | SPI CHIP SELECT. Expander0 secondary FLASH select |
| | EXPD0_WP1_N | 0 | CMOS | SPI WRITE PROTECT. Active low Expander0 secondary FLASH write protect |
| | EXPD1_SCSSN | 0 | CMOS | SPI CHIP SELECT. Expander1 secondary FLASH select |
| | EXPD1_WP1_N | 0 | CMOS | SPI WRITE PROTECT. Active low Expander1 secondary FLASH write protect |
| | EXPD1_SCSPN | 0 | CMOS | SPI CHIP SELECT. Expander1 FLASH select |
| | EXPD1_WP0_N | 0 | CMOS | SPI WRITE PROTECT. Active low Expander1 FLASH write protect |
| | FAN[61]_PRES | I | TTL | Fan is present on system |
| Fan Control | FAN[61]_LED | I | CMOS | LED signal from baseboard when fan is off line |
| | FAN[61]_TACH | I | Analog | Fan is installed |

8.4 Electrical, Environmental, and Mechanical Specifications

This section specifies the operational parameters and physical characteristics for the SAS backplane board.

8.4.1 Electrical Specifications

The power budget for the SAS backplane board and pin-outs of the external interface connectors are defined here.

Table 63. Electrical Specifications

| Feature | Absolute Maximum Rating |
|---|---|
| Voltage of any signal with respect to ground | -0.3 V to Vcc ¹ to Vcc ¹ +0.3 V |
| +2.5 Volt supply with respect to ground | -0.25 V to +2.75 V |
| +3.3 Volt standby supply with respect to ground | -0.3 V to +3.465 V |
| +3 .3 Volt supply with respect to ground | -0.3 V to +3.465 V |
| +5 Volt supply with respect to ground | -0.3 V to +5.25 V |
| +12 Volt supply with respect to ground | -0.3 V to +12.6 V |

Note: 1. Vcc means supply voltage for the device.

Table 64 shows the power consumed on each supply line for the SAS backplane board. Since P5V, P2V5 and P3V3 are derived from the input, 12V supply power dissipation on the 12V rail will also include the power dissipation from the other three rails.

Table 64. Maximum Power Consumption

| Devices | Power Dissipation |
|---------------|-------------------|
| 12 V | 251.7W |
| 5 V | 70W |
| 3.3 V | 8.5W |
| 2.5 V | 5.2W |
| 3.3 V Standby | 0.5W |
| 5 V Standby | 0.5W |

Note: Table 64 is provided only to show design limits. Actual power consumption will vary depending on the exact configuration.

8.4.1.1 SAS Drive Supplied Power

The SAS drives installed in the system must fall within power limits shown in Table 65. The backplane board is designed to work with the Fujitsu* MAU3XXXRC SAS drives. However, drives that meet the following requirements can be used.

Table 65. SAS Backplane Power Limits per Drive

| Device Constraint | +5 V | +12 V |
|-----------------------|-----------|-----------|
| Peak start current | 0.73 amps | 3.0 amps |
| Max operating current | 1.0 amps | 1.0 amps |
| Average idle | 0.45 amps | 0.75 amps |

8.4.1.2 Power Supply Requirements

The external and internal power supply must meet the following requirements:

- Rise time of less than 50 ms (for all voltages).
- Delay of 5 ms (minimum) from valid power-to-power good.
- See Table 66 for voltage regulation requirements.

Table 66. DC Voltage Regulation

| DC Voltage | Acceptable Tolerance |
|----------------|----------------------|
| +5 V | ± 5% |
| +12 V | ± 5% |
| +3.3 V | ± 5% |
| +3.3 V standby | ± 5% |
| +2.5 V | ± 5% |

8.4.1.3 Power Bay Connector Pin-out

The power bay connector delivers power from the power cage to the backplane board.

Table 67. Power Bay Connector Pin-out – J6P1

| Pins | Signal |
|-----------|--------|
| 1 thru 6 | GND |
| 7 thru 12 | +12V |

8.4.1.4 Tape Drive Connector Pin-out

The tape drive connector delivers power from the backplane board to optional tape drive devices.

Table 68. Tape Drive Connector Pin-out - J6R1

| Pins | Signal |
|------------|--------|
| 1, 5 | +12V |
| 4, 8 | +5V |
| 2, 3, 6, 7 | GND |

8.4.2 DVD Power Connector

The DVD power connector provides power to the DVD disk drive. Other signals for the drive connect directly with the mainboard.

Table 69. DVD Power Connector - J6B1

| | Signal |
|---|--------|
| 1 | +5V |
| 2 | GND |

8.4.2.1 SAS Connector Pin-outs

The internal SAS SFF8087 connector is a shielded 36-pin connector.

Table 70. 36-Pin SAS 4i internal Connector Pin-out - J6F1

| Signal | Connector Pin | Connector Pin | Signal Name |
|--------|---------------|---------------|-------------|
| GND | A1 | B1 | GND |
| RX0_P | A2 | B2 | TX0_P |
| RX0_N | A3 | B3 | TX0_N |
| GND | A4 | B4 | GND |
| RX1_P | A5 | B5 | TX1_P |
| RX1_N | A6 | B6 | TX1_N |
| GND | A7 | B7 | GND |
| NC | A8 | B8 | NC |
| NC | A9 | B9 | NC |
| GND | A10 | B10 | GND |
| GND | A11 | B11 | GND |
| GND | A12 | B12 | GND |
| RX2_P | A13 | B13 | TX2_P |
| RX2_N | A14 | B14 | TX2_N |
| GND | A15 | B15 | GND |
| RX3_P | A16 | B16 | TX3_P |
| RX3_N | A17 | B17 | TX3_N |
| GND | A18 | B18 | GND |

Table 71. SAS Drive Connector Pin-out – J6E2, J5E1, J3E1, J2E1, J1E1, J2H1, J1H1, J5H1, J3H1, and J6H3

| Pin | Signal | Pin | Signal |
|-----|--------|-----|-----------|
| S1 | GND | P1 | NC |
| S2 | RXP | P2 | NC |
| S3 | RXN | P3 | NC |
| S4 | GND | P4 | GND |
| S5 | TXN | P5 | GND |
| S6 | TXP | P6 | PRESENT_N |
| S7 | GND | P7 | +5V |
| | | P8 | +5V |
| | | P9 | +5V |
| | | P10 | +5V |
| | | P11 | ACT_N |
| | | P12 | +12V |
| | | P13 | +12V |
| | | P14 | +12V |
| | | P15 | +12V |

8.4.3 Mechanical Specifications

Figure 37 shows the mechanical specifications and the connector positions for the SAS Backplane. The board outline dimensions are 16.5 inches x 6.380 inches. The board thickness is 0.093 inches +.008/-.005 inches. All dimensions are in inches.

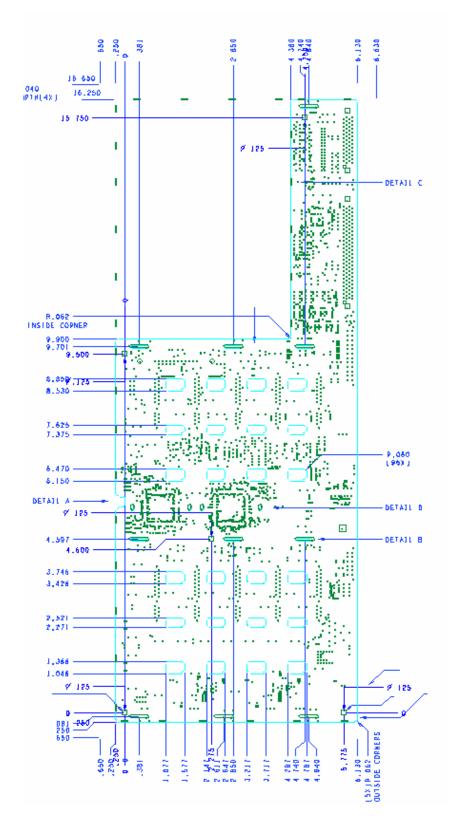


Figure 37. Mechanical Drawing

9. Front Panel I/O and Control Boards

This section describes the Intel® Server Platforms SR6850HW4 and SR6850HW4/M front panel I/O board and is organized as follows:

Section 9.1: Introduction

Provides an overview of the platforms' front panel I/O board, showing functional blocks and board layout.

Section 9.2: Functional Architecture

Describes the platforms' front panel I/O board functional blocks.

Section 9.3: Signal Descriptions

Summary of the internal and connector signals, and the connector signal-pin names and descriptions. Signal mnemonics appear throughout this section.

Section 9.4: Electrical, Environmental and Mechanical Specifications

Specifies operational parameters and considerations, and connector-pinouts.

Section 9.5: Front Panel Control Module

Describes the two different front panel control modules available in the Intel® Server Platforms SR6850HW4 and SR6850HW4/M.

9.1 Introduction

The server platform front panel I/O board provides access to the video and USB interfaces. It also interfaces to the front panel control module that contains the front control panel buttons, LEDs and optional LCD window. Circuitry on the platforms' front panel I/O board consists of video filters, USB filters, USB port power bulk capacitors with fusing, and a piezoelectric speaker.

9.1.1 Block Diagram

The following block diagram divides the front panel I/O board into physical and functional blocks. Arrows represent buses and signals. Blocks represent the physical and functional circuits. Figure 38 illustrates the general architecture of the front panel.

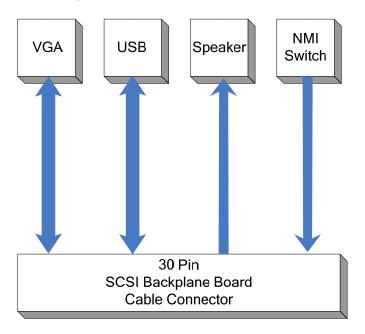


Figure 38. Front Panel I/O Board Block Diagram

9.1.2 Architectural Overview

The front panel I/O board provides three main functions for the platform. The first function is to provide filtered video and USB signals to the front panel connector. The second is to provide a speaker. The third is to provide a system NMI button.

Functional blocks are as follows:

- USB ports
 - External front control panel connector for three USB 2.0 ports
 - Filtering for the USB signals
 - Bulk capacitance and fused power for USB ports
- Video connector
 - External front control panel 15-pin VGA connector
 - Required safety fusing and EMI filtering
- Speaker
 - Audible beep-code and alarm speaker
- NMI button

9.1.3 Component Location

The following figure shows the placement of the major components and connectors on the front panel I/O board. Figure 40 provides a three-dimensional view of the board.

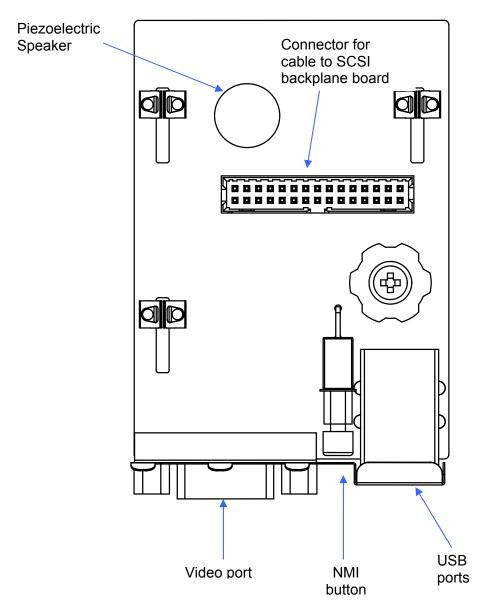


Figure 39. Front Panel I/O Board Placement Diagram

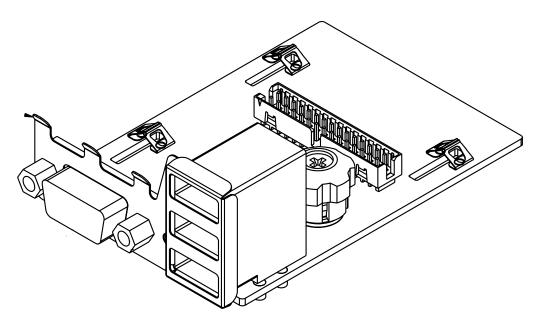


Figure 40. Front Panel I/O Board

9.2 Functional Architecture

This section provides an architectural description of the platforms' front panel I/O board functional blocks.

9.2.1 VGA

The front panel I/O board passes the VGA video signals from the platforms' SCSI backplane board connector to the front panel I/O board. The video signals originate on the Intel® Server Platform SE8501HW4 mainboard and route to the platforms' SCSI backplane board through a 100-pin cable.

Using the default operating system video driver options, the VGA signal is mirrored between the rear panel and the front panel of the platform. This design consideration was made to facilitate user debug of an operating system hard failure. When the system is in a failure state, a portable monitor can be attached to the front of the system to determine root cause. Since this is an enterprise server, Intel is not validating the video driver configured with the front panel I/O board VGA connector in a non-mirrored, extended desktop state.

9.2.2 USB

The front panel I/O board passes the high-speed USB 2.0 signals from the platforms' SCSI backplane board to the three USB ports on the front of the system.

9.2.3 NMI Button

The front panel I/O board has an NMI button; this signal is routed to the 30-pin platforms' SCSI backplane board connector.

9.3 Signal Descriptions

The following notations are used to describe the signal type, from the perspective of the platforms' front panel I/O board:

I Input-pin to the platforms' front panel I/O board
 O Output-pin from the platforms' front panel I/O board

I/O Bi-directional (input/output)-pin

PWR Power supply-pin

The signal description also includes the type of buffer used for the particular signal:

TTL 5V TTL signals
 CMOS 5V CMOS signals
 3.3V CMOS 3.3V CMOS signals

Analog Typically a voltage reference or specialty power supply

hs This suffix is added to indicate high-speed requirements that would make

modifications subject to review

9.3.1 USB Connector

Table 72 provides a summary of power connector-pins, including the signal mnemonic, the name, and a brief description.

Table 72. USB Connector

| | Signal | Type | Driver | Name and Description |
|-------------|------------------|------|--------|----------------------|
| | USB_FB_OC1 | | | Connector, TOP |
| USB port | USB_P1_CONN_M | I/O | | |
| 1(J6K1) | USB_P1_CONN_P | I/O | | |
| | USB_P1_CABLE_GND | | | |
| | USB_FB_OC2 | | | Connector, CENTER |
| USB port | USB_P2_CONN_M | I/O | | |
| 2(J5K1) | USB_P2_CONN_P | I/O | | |
| | USB_P2_CABLE_GND | | | |
| | USB_FB_OC3 | | | Connector, BOTTOM |
| USB port | USB_P3_CONN_M | I/O | | |
| 3(J6K1) | USB_P3_CONN_P | I/O | | |
| | USB_P3_CABLE_GND | | | |

9.3.2 Front Panel VGA Connector

The front panel I/O board provides a video port interface with a standard VGA-compatible, 15-pin connector. Onboard video is supplied by the ATI* Radeon* 7000 component, with 16MB of on-chip memory. The signal is mirrored between the Front Panel I/O Board and the rear panel of the Intel® Server Board Set SE8501HW4 mainboard. See Section 4 for-pin-outs.

Signal Type RED 0 **GREEN** 0 **RGB** BLUE 0 **VGA HSYNC** 0 VSYNC 0 VID SCL O I²C VID_SDA I/O V PRES L VIDPWR 0

Table 73. VGA Connector Signal Description

9.4 Electrical, Environmental, and Mechanical Specifications

This section specifies the board-level operational parameters and physical characteristics for the platforms' Front Panel I/O Board. Further topics in this section specify normal operating conditions for the front panel, mechanical specifications, and connector interfaces to the board.

9.4.1 Electrical Specifications

The power budget for the front panel I/O board is defined in Table 74.

Table 74. Electrical Specifications

| Feature | Absolute Maximum Rating |
|--|---|
| Voltage of any signal with respect to ground | -0.3V to Vcc ¹ to Vcc ¹ +0.3V |
| +5V supply with respect to ground | -0.3V to +5.25V |

Note: 1. Vcc means supply voltage for the device.

9.4.1.1 Power Consumption

The front panel I/O board consumes no power. The +5 volt power consumption is for the three USB ports and is shown in Table 75.

Table 75. Maximum Power Consumption

| Devices | Power Dissipation | | | |
|---------|-------------------|--|--|--|
| +5V | 1.5W | | | |

Note: The numbers in the table are provided only to show design limits. Power consumption will vary depending on the exact configuration.

9.4.1.2 Power Supply Requirements

The power supply must meet the following requirements:

- Rise time of less than 50ms (for all voltages).
- Delay of 5ms (minimum) from valid power-to-power good.
- See the following table for voltage regulation requirements.

Table 76. DC Voltage Regulation

| DC Voltage | Acceptable Tolerance | | | | |
|------------|----------------------|--|--|--|--|
| +5V | ± 5% | | | | |

9.4.2 Connector Specifications

Table 77 shows the reference designators, quantity, manufacturer, and part numbers for connectors on the front panel I/O board. See manufacturer's documentation for information.

Table 77. Server Platforms Front Panel I/O Board Connector Specifications

| Item | Reference Designator(s) | Quantity | Manufacturer and Part Number (or equivalent) | Description |
|------|-------------------------|----------|--|--------------------------------------|
| 1 | J3 | 1 | Foxconn* UB11123-M1 | USB Three Ports |
| 2 | J2 | 1 | Foxconn* DZ11A91-G5 | VGA DB-15 connector |
| 3 | J1 | 1 | Foxconn* HL54157-E3 | 30-pin SCSI Backplane Board Board |

9.4.3 Cooling Requirements

The front panel I/O board does not dissipate significant heat. Cooling is not required to maintain ambient temperatures.

9.5 Front Panel Control Module

The platforms support the standard button control panel, providing basic functionality, or an Intel[®] Local Control Panel (iLCP), which adds an LCD and more server management features. Both front panels contain switches and LED status indicators. Both front panels are retained in the chassis sheet metal by two clips and connect to the platforms' front panel I/O board via a 30-pin flat cable.

9.5.1 Button Control Panel

Button control panel features are shown in Figure 41 and described in **Error! Reference source not found.** Please refer to the *Intel*[®] *Button Control Panel Technical Product Specification* for more information.

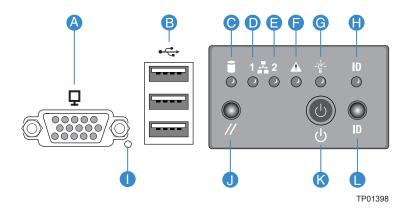


Figure 41. Button Control Panel Features

| Item | Feature | Description | | | | |
|------|-------------------------|---|---|--|--|--|
| Α | Video Display Connector | Part of the I/O panel, not part of the Button Control Panel | | | | |
| В | USB Connectors | Part of the I/O panel, r | not part of the Button | n Control Panel | | |
| С | Hard Drive Activity LED | Indicates hard drive ad | ctivity and fault statu | IS. | | |
| | (green/amber) | LED | State | Description | | |
| | | Green, on | | A hard drive is being initialized. | | |
| | | Green, blinking | | A hard drive is active. | | |
| | | Amber, on | | Hard drive/slot failure. | | |
| | | Amber, slow blinking (~1Hz) | A predictive hard drive/slot failure or rebuild in process. | | | |
| | | Amber, fast blinking (~2.5Hz) | | Hard drive rebuild interrupted or rebuild on empty slot. | | |
| D, E | LAN1, LAN2 Status LEDs | Indicates LAN activity status. | | | | |

| Item | Feature | Description | | | | |
|------|-------------------------|---|---------------|-----------------------|---------|--|
| | (green) | LED | | State | | Description |
| | | Off | | Idle | | |
| | | On | | Inactive | | No access |
| | | Blinking | | Active | | Access |
| F | System Status/Fault LED | Indicates s | system statu | S. | | |
| | (green/amber) | LED | | State | | Description |
| | | Off | | Not ready | | AC Power Off, POST error |
| | | Green, on | | Ready | | System booted and ready |
| | | Green, blir | nking | Degraded | | Processor or DIMM disabled |
| | | Amber, on | | Critical Alarr | m | Critical power supply, blower, voltage, or temperature failure. |
| | | Amber, blinking | | Non-Critical Alarm | | Redundant power supply or blower failure, non- critical blower, voltage, and temperature failure. |
| G | System Power LED | Indicates s | system power | er status. | | |
| | (green) | LED | State | | ACPI | |
| | | Off | Power off | | | No |
| | | On | Power on | | | No |
| | | Off | | S5 | | Yes |
| | | Blinking | | S1 | | Yes |
| | | On | | S0 | | Yes |
| Н | System ID LED (blue) | Identifies t | he system v | ia server mana | agem | ent or locally. |
| | | Off | Not active | | | |
| | | On | Active via | | | nnot be turned off by ver Management |
| | | Blinking Active via Managem | | | | nnot be turned off by tch |
| I | NMI button | Asserts NMI. Part of the I/O panel, not part of the Button Control Panel | | | | |
| J | System reset button | Press to reset the system. | | | | |
| К | System power button | Press to turn the system power on or off. Required to be pressed for four continuous seconds if under OS control to force transition to off state. Outside of OS control, a momentary button press will toggle the power state from off to on or on to off. | | | | |
| L | System ID button | Press to tu | ırn the syste | m ID LED on o | or off. | |

9.5.2 Intel[®] Local Control Panel

Intel[®] Local Control Panel features are shown in **Error! Reference source not found.** and described in the table below. Please refer to the *Intel[®] Local Control Panel Technical Product Specification* for more information.

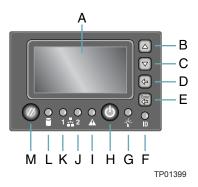


Figure 42. Intel[®] Local Control Panel Features Diagram

| Label | Button/LED | Function | | | | | |
|-------|--------------------------|---|-----------------|----------------------|--|--|--|
| Α | LCD | Display of text | | | | | |
| В | Scroll up button | Press to scroll up on the LCD | | | | | |
| С | Scroll down button | Press to s | croll dov | vn on the LCD |) | | |
| D | Back button | Press to m | nove to t | he previous L | .CD so | creen | |
| Е | Select button | Press to e | nter a c | ommand or se | elect a | n option on the LCD | |
| F | System ID LED (blue) | Helps ider | tify the | system via se | rver m | nanagement or locally | |
| | | Off | Not a | ctive | | | |
| | | On | Active | via switch | | nnot be turned off by Server nagement | |
| | | Blinking | | via Server gement | Cannot be turned off by switch | | |
| G | System power LED (green) | Indicates s | system p | ower status. | | | |
| | | Off | | Power off | | ACPI: No | |
| | | On | | Power on | | ACPI: No | |
| | | Off | | S4 / S5 | | ACPI: Yes | |
| | | Blinking | | S1 | | ACPI: Yes | |
| | | On | | S0 | | Yes | |
| Н | System power button | Press to turn the system power on or off. Required to be pressed for four continuous seconds if under OS control to force transition to off state. Outside of OS control, a momentary button press will toggle the power state from off to on or on to off. | | | | | |
| 1 | System Status/Fault LED | Indicates | system s | status | | | |
| | (green/amber) | Off Not ready | | Not ready | | AC power off, POST error | |
| | | Green, on | Green, on Ready | | | System booted and ready | |
| | | Green, blinking Degr | | Degraded | | Processor or DIMM disabled | |
| | Amber, on | | Critical Alar | m | Critical power supply, blower, voltage, or temperature failure | | |

| Label | Button/LED | Function | | | | |
|-------|-------------------------------------|---|----------------------------|---|--|--|
| | | Amber, blinking | Non-Critical Alarm | Redundant power supply or blower failure. Non-critical blower, voltage, | | |
| | | | | or temperature failure. | | |
| J, K | LAN1, LAN2 Status LEDs | Indicates LAN act | ivity status | _ | | |
| | (green) | Off | Idle | | | |
| | | On | Inactive | No access | | |
| | | Blinking | Active | Access | | |
| L | Hard Drive Status LED (green/amber) | Indicates hard drive activity and fault status. | | | | |
| | | Green | On | A hard drive is being initialized | | |
| | | Green | Blinking | A hard drive is active | | |
| | | Amber | On | Hard drive/slot failure | | |
| | | Amber | Slow blinking (~1 Hz) | A predictive hard drive/slot failure or rebuild in process | | |
| | | Amber | Fast blinking (~2.5 Hz) | Hard drive rebuild interrupted or rebuild on empty slot | | |
| М | System Reset button | Resets the systen | า | | | |

9.5.3 System ID Buttons and LEDs

The system contains two system ID buttons and two blue system ID LEDs. The LEDs are used to easily identify a platform. This feature is useful when several platforms are racked or installed near each other and a specific system needs to be serviced. One button/LED pair is located on the front control panel and a second button/LED pair is located at the rear of the platform.

The system ID LEDs can be turned on and off either by the system ID buttons or remotely through server management software. If the LEDs are activated by the system LED button, they must be turned off with the button; they cannot be turned off remotely through software. If the LEDs are activated through software, they must be turned off through software, not by pressing the system LED button.

Table 78. System ID LED Details

| LED State | Description | |
|-----------|--------------------------------------|--|
| Off | System ID inactive. | |
| On | System ID active via button. | |
| Blinking | System ID active via remote command. | |

10. SATA-to-IDE Converter Board

This section describes the platforms' SATA-to-IDE converter board to support an optical drive. This board connects a JAE Slimline peripheral 50-pin Slimline Form Factor (SFF) IDE connector on an optical drive to a 7-position SATA signal connector. The power for the optical drive and the converter board is delivered through a 4-pin mini-power connector. The SATA-to-IDE converter board should be removed when a SATA optical device has been qualified for the system.

Please refer to the *Tested Hardware Operating System List (THOL)* for more information on the specific optical drives Intel has validated in the platform. DVD-ROM drives will be qualified for the platform, but since this is an enterprise server, DVD video playback will not be validated.

10.1 Mechanical Outline

The following figures show mechanical outline drawings of the platforms' SATA-to-IDE converter board and an optical drive.

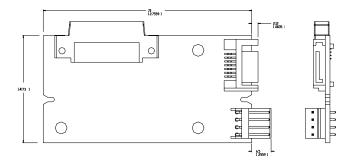


Figure 43. SATA-to-IDE Converter Board Mechanical Outline

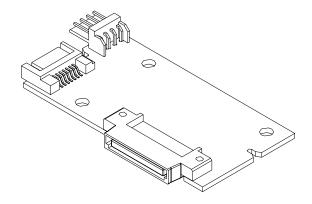


Figure 44. SATA-to-IDE Converter Board

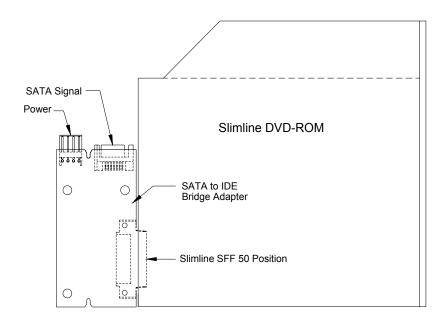


Figure 45. SATA-to-IDE Converter Board with Attached Optical Drive

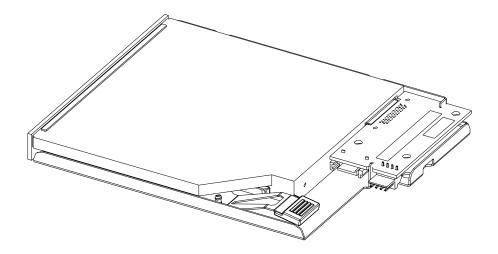


Figure 46. SATA-to-IDE Converter Board with Attached Optical Drive

11. Regulatory and Certification Information



A WARNING

To ensure regulatory compliance, you must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products / components will void the UL listing and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in the region(s) in which the product is sold.

To help ensure EMC compliance with your local regional rules and regulations, before computer integration, make sure that the chassis, power supply, and other modules have passed EMC testing using a server board with a microprocessor from the same family (or higher) and operating at the same (or higher) speed as the microprocessor used on this server board. The final configuration of your end system product may require additional EMC compliance testing. For more information please contact your local Intel Representative.

This is an FCC Class A device. Integration of it into a Class B chassis does not result in a Class B device.

11.1 Product Regulatory Compliance

The Server Chassis product, when correctly integrated per this guide, complies with the following safety and electromagnetic compatibility (EMC) regulations.

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation.

11.1.1 **Product Safety Compliance**

UL60950 - CSA 60950(USA / Canada)

EN60950 (Europe)

IEC60950 (International)

CB Certificate & Report, IEC60950 (report to include all country national deviations)

GS License (Germany)

GOST R 50377-92 - License (Russia)

Belarus License (Belarus)

Ukraine License (Ukraine)

CE - Low Voltage Directive 73/23/EEE (Europe)

IRAM Certification (Argentina)

GB4943- CNCA Certification (China)

11.1.2 Product EMC Compliance – Class A Compliance

Note: <u>Legally</u> the product is required to comply with Class A emission requirements as it is intended for a commercial type market place. Intel targets 10db margin to Class A Limits

FCC /ICES-003 - Emissions (USA/Canada) Verification

CISPR 22 - Emissions (International)

EN55022 - Emissions (Europe)

EN55024 - Immunity (Europe)

EN61000-3-2 - Harmonics (Europe)

EN61000-3-3 - Voltage Flicker (Europe)

CE – EMC Directive 89/336/EEC (Europe)

VCCI Emissions (Japan)

AS/NZS 3548 Emissions (Australia / New Zealand)

BSMI CNS13438 Emissions (Taiwan)

GOST R 29216-91 Emissions (Russia)

GOST R 50628-95 Immunity (Russia)

Belarus License (Belarus)

Ukraine License (Ukraine)

RRL MIC Notice No. 1997-41 (EMC) & 1997-42 (EMI) (Korea)

GB 9254 - CNCA Certification (China)

GB 17625 - (Harmonics) CNCA Certification (China)

11.1.3 Certifications / Registrations / Declarations

UL Certification (US/Canada)

CE Declaration of Conformity (CENELEC Europe)

FCC/ICES-003 Class A Attestation (USA/Canada)

VCCI Certification (Japan)

C-Tick Declaration of Conformity (Australia)

MED Declaration of Conformity (New Zealand)

BSMI Certification (Taiwan)

GOST R Certification / License (Russia)

Belarus Certification / License (Belarus)

RRL Certification (Korea)

IRAM Certification (Argentina)

CNCA Certification (China)

Ecology Declaration (International)

11.1.4 RoHS

Intel has a system in place to restrict the use of banned substances in accordance with the European Directive 2002/95/EC. Compliance is based on declaration that materials banned in the RoHS Directive are either (1) below all applicable substance threshold limits or (2) an approved/pending RoHS exemption applies.

Note: RoHS implementing details are not fully defined and may change.

Threshold limits and banned substances are noted below.

Quantity limit of 0.1% by mass (1000 PPM) for:

- Lead
- Mercury
- Hexavalent Chromium
- Polybrominated Biphenyls Diphenyl Ethers (PBDE)

Quantity limit of 0.01% by mass (100 PPM) for:

Cadmium

11.2 Product Regulatory Compliance Markings

The Intel Server Chassis product bears the following regulatory marks.

| Regulatory Compliance | Region | Marking |
|---|----------------------------|---|
| cULus Listing Marks | USA/Canada | CULUSTED LTS9761 |
| GS Mark | Germany | |
| CE Mark | Europe | CE |
| FCC Marking (Class A) | USA | This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation. Manufactured by Intel Corporation |
| EMC Marking (Class A) | Canada | CANADA ICES-003 CLASS A CANADA NMB-003 CLASSE A |
| C-Tick Mark | Australia / New Zealand | C N232 |
| VCCI Marking (Class A) | Japan | この装置は、クラス A 情報技術 装置です。この装置を家庭環境で 使用すると電波妨害を引き起こす ことがあります。この場合には使 用者が適切な対策を講ずるよう要 求されることがあります。VCCI-A |
| BSMI Certification Number & Class A Warning | Taiwan | 图33025 警告使用者: 這是甲類的資訊產品,在居住的環境中使用時, 可能會造成射頻干擾,在這種情況下,使用者會 |
| GOST R Marking | Russia | 被要求採取某些適當的對策 |
| RRL MIC Mark | Korea | MIC |

| Regulatory Compliance | Region | Marking |
|--|--------|----------------------------------|
| | | 인증번호: CPU- <i>Model Name</i> (A) |
| China Compulsory Certification Mark | China | ((() |

11.3 Electromagnetic Compatibility Notices

11.3.1 FCC Verification Statement (USA)

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Intel Corporation 5200 N.E. Elam Young Parkway Hillsboro, OR 97124-6497 Phone: 1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class A or B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

11.3.2 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

English translation of the notice above:

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

11.3.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

11.3.4 **VCCI** (Japan)

この装置は、情報処理装置等電波障害自主規制協議会(VCCI)の基準に基づくクラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:

This is a Class A product based on the standard of the Voluntary Control Council for Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

11.3.5 **BSMI** (Taiwan)

The BSMI Certification Marking and EMC warning is located on the outside rear area of the product.

警告使用者:

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這是甲類的資訊產品,在居住的環境中使用時,可能會造成射頻干擾,在這種情況下,使用者會被要求採取某些適當的對策

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11.3.6 RRL (Korea)

Following is the RRL certification information for Korea.



English translation of the notice above:

- 1. Type of Equipment (Model Name): On License and Product
- 2. Certification No.: On RRL certificate. Obtain certificate from local Intel representative
- 3. Name of Certification Recipient: Intel Corporation
- 4. Date of Manufacturer: Refer to date code on product
- 5. Manufacturer/Nation: Intel Corporation/Refer to country of origin marked on product

11.3.7 CNCA (CCC-China)

The CCC Certification Marking and EMC warning is located on the outside rear area of the product.

声明

此为**A**级产品,在生活环境中,该产品可能会造成无线电干扰。在这种情况下,可能需要用户对其干扰采取可行的措施。

11.4 Regulated Specified Components

To maintain the UL listing and compliance to other regulatory certifications and/or declarations, the following regulated components must be used and conditions adhered to. Interchanging or use of other component will void the UL listing and other product certifications and approvals.

Updated product information for configurations can be found on the Intel Server Builder Web site at the following URL:

http://channel.intel.com/go/serverbuilder

If you do not have access to Intel's Web address, please contact your local Intel representative.

- Server Chassis (base chassis is provided with power supply and fans)
 UL listed.
- Server board you must use an Intel server board—UL recognized.
- Add-in boards must have a printed wiring board flammability rating of minimum UL94V-1. Add-in boards containing external power connectors and/or lithium batteries must be UL recognized or UL listed. Any add-in board containing modem telecommunication circuitry must be UL listed. In addition, the modem must have the appropriate telecommunications, safety, and EMC approvals for the region in which it is sold.
- Peripheral Storage Devices must be UL recognized or UL listed accessory and TUV or VDE licensed. Maximum power rating of any one device is 19 watts. Total server configuration is not to exceed the maximum loading conditions of the power supply.

Glossary

This appendix contains important terms used in the preceding sections. Acronyms are then entered in their respective place, with non-acronyms following.

| Word / Acronym | Definition |
|----------------|---|
| ACPI | Advanced configuration and power interface |
| BIOS | Basic Input / Output System |
| BMC | Baseboard management controller |
| CE | Community European |
| CISPR | International Special Committee on Radio Interference |
| CMOS | Complementary metal-oxide semiconductor |
| CSA | Canadian Standards Organization |
| DB | Data bus |
| dBA | Deciel acoustic |
| DDR2 | Double data rate |
| DIMM | Dual in-Line memory module |
| DMA | Direct memory access |
| ECC | Error checking and correcting |
| EEPROM | Electrically erasable programmable ROM |
| EMI | Electromagnetic interference |
| EMP | Emergency Management Port |
| EPS | External Product Specification |
| ESD | Electro static discharge |
| FCC | Federal Communications Commission |
| FRB | Fault resilient booting |
| FRU | Field replaceable unit |
| FSB | Front side bus |
| FWH | Firmware hub |
| GND | Ground |
| GUI | Graphical user interface |
| HDD | Hard disk drive |
| HL | Hub-link |
| HSC | Hot-swap controller |
| I/O | Input / Output |
| ICMB | Intelligent Chassis Management Bus |
| IDE | Integrated device electronics |
| IEC | International Electrotechnical Commission |
| IMB | Intelligent management bus |
| IPMB | Intelligent platform management bus |
| IPMI | Intelligent platform management interface |
| ISP | In-system programmable |
| ITE | Information technology equipment |
| ITP | In-target probe |

| Word / Acronym | Definition |
|----------------|--|
| JTAG | Joint Test Action Group |
| LAN | Local area network |
| LED | Light emitting diode |
| LPC | Low-pin count |
| LVDS | Low voltage differential SCSI |
| NIC | Network interface card |
| OEM | Original equipment manufacturer |
| OS | Operating system |
| OTP | Over-temperature protection |
| PCI | Peripheral component interconnect |
| PDB | Power Distribution Board |
| PEF | Platform event filtering |
| PEP | Platform event paging |
| PFC | Power factor correction |
| PIROM | Processor information ROM |
| PLD | Programmable logic device |
| PWM | Pulse width modulator |
| RAID | Redundant array of independent disks |
| RAS | Reliability, availability, and serviceability |
| RPM | Revolutions per minute |
| SAF-TE | SCSI accessed fault-tolerant enclosure |
| SCA | Single connector attachment |
| SCL | Serial clock |
| SCSI | Small computer systems interface |
| SDA | Serial data |
| SDINT | System diagnostic interrupt |
| SDR | Sensor data record |
| SDRAM | Synchronous dynamic RAM |
| SE | Single-ended |
| SEEPROM | Serial dlectrically erasable programmable read-only memory |
| SEL | System event log |
| SMP | Symmetric multiprocessing |
| TTL | Transistor-transistor logic |
| USB | Universal serial bus |
| UV | Under-voltage |
| VAC | Alternating current (AC) voltage |
| VCC | Voltage controlled current |
| VCCI | Voluntary Control Council for Interference by Information Technology Equipment |
| VGA | Video graphics array |
| VID | Voltage ID |
| VRM | Voltage regulator module |
| VSB | Voltage standby |
| WfM | Wired for management |
| | |

Reference Documents

See the following documents for additional information:

- Intel[®] Server Board Set SE8501HW4 Technical Product Specification
- Intel[®] Server Platforms SR6850HW4 Power Cord Enabling Specification
- SCSI Accessed Fault-Tolerant Enclosures Interface Specification (SAF-TE)
- Intel[®] Server Board SE8501HW4 Tested Hardware and Operating System List (THOL)
- Intel[®] Local Control Panel Technical Product Specification
- Intel[®] Button Control Panel Technical Product Specification
- Intel[®] Management Module Installation and User's Guide
- IPMI Specification, Version 2.0