Intel® Server System SR870BN4

Technical Product Specification

Revision 2.0

April 10, 2003

Enterprise Platforms and Services Division

Revision History

Date	Revision Number	Modifications
9/20/2001	1.0	Initial release.
4/10/2003	2.0	Update to SRA phase.

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1. Introduction

This document provides an overview of the Intel® Server System SR870BN4 and includes information on chassis hardware, cables, connectors, power subsystem, system boards, and regulatory requirements.

1.1 Document Structure and Outline

This document is organized into the following chapters:

Chapter 1: Introduction
Provides an overview of this document.

Chapter 2: System Overview
Provides an overview of the system hardware.

Chapter 3: System Chassis and Sub-Assemblies
Provides an overview of the chassis and major sub-assemblies.

Chapter 4: Cables and Connectors
Describes the cables and connectors used to interconnect the S870BN4 board set and the server system components.

Chapter 5: Power Subsystem
Describes the specifications for the power supplies.

Chapter 6: Front Panel Board
Describes the front panel board used in the SR870BN4 server system.

Chapter 7: SCSI Backplane Board
Describes the SCSI backplane board used in the SR870BN4 server system.

Chapter 8: Power Distribution Board
Describes the power distribution board used in the SR870BN4 server system.

Chapter 9: Hot-Plug Indicator Board
Describes the Peripheral Component Interconnect (PCI) Hot-Plug Indicator Board (HPIB) used in the SR870BN4 server system.

Chapter 10: Peripheral Adapter Boards
Describes the Integrated Device Electronics (IDE) peripheral device adapter boards used in the SR870BN4 server system.

Chapter 11: Intelligent Chassis Management Bus (ICMB) Board
Describes the optional ICMB board used in the SR870BN4 server system.

Chapter 12: Regulatory Specifications
Describes system compliance to regulatory specifications.

2. System Overview

This chapter describes the features of the SR870BN4 server system. This chapter is organized into the following sections:

Section 2.1: System Feature Summary
Provides a list and brief description of the features of the SR870BN4 server system.

Section 2.2: Introduction
Provides an overview and block diagram of the SR870BN4 server system.

Section 2.3: External Chassis Features - Front
Describes features located at the front of the SR870BN4 system chassis in detail (buttons, switches, bezel, etc.).

Section 2.4: External Chassis Features - Rear
Describes features located at the rear of the SR870BN4 system chassis in detail (user-accessible connectors).

Section 2.5: External Chassis Features - Top
Describes serviceability Light Emitting Diodes (LEDs) visible through the top cover of the SR870BN4 system chassis.

Section 2.6: System Board Set
Provides an overview of the SR870BN4 system board set.

Section 2.7: Power Subsystem
Provides an overview of the SR870BN4 power subsystem.

Section 2.8: Cooling Subsystem
Describes the SR870BN4 cooling subsystem.

Section 2.10: Server Management
Describes the server management features of the SR870BN4 server system.

Section 2.11: Reliability, Availability and Serviceability (RAS)
Describes the reliability, availability, and serviceability features of the SR870BN4 server system.

Section 2.12: Expansion Support
Describes the expansion support features of the SR870BN4 server system.

Section 2.13: Specifications
Describes the environmental and physical specifications of the SR870BN4 server system.

2.1 System Feature Summary

Table 1 provides a list and brief description of the features of the SR870BN4 server system.

Table 1. Intel® Server System SR870BN4 Feature List

Feature	Description
Compact, high-density system	Rack-mount server with a height of 4U (7 inches) and a depth of 28 inches
Configuration flexibility	1-4 way capability in low profile and cost effective packaging Stand-alone system including external I/O slots/disk expansion as needs grow Intel® Itanium® 2 processor support 32-GB Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) memory support
Serviceability	Front access to hot-swap hard disk drives Top access to hot-plug PCI slots and hot-swap fans Rear access to hot-swap power supplies Cable-less interconnect between all major subsystems Dockable processor/memory subsystem, I/O subsystem, peripheral bay, power bay, and front panel Dockable LS-240 and DVD or CD (CD-ROM, CD-RW) drives Interlock status indicator LEDs for critical system interconnects System power and reset status LEDs System ID switch on front panel and LEDs on front and back Color-coded parts to identify hot-swap and non-hot-swap serviceable components
Availability	Eight 64-bit, hot-plug PCI-X slots Two hot-swap 1200-W power supplies in a redundant (1+1, 220 V) configuration with dual redundant power cords (1+1, 220 V) Four hot-swap system fans in a redundant (3+1) configuration Three hot-swap 1-inch Ultra*-320 SCSI hard disk drives
Manageability	Remote management Emergency Management Port (EMP) Intelligent Platform Management Interface (IPMI) 1.5 compliant Wired For Management (WfM) 2.0 compliant External server management via ICMB Remote diagnostics support
Upgradeability and investment protection	Supports Intel® Itanium® 2 processor family Field upgradeable to next generation Itanium® 2 processors Multi-generational chassis
System-level scalability	Up to 32-GB DDR SDRAM (using 2-GB DIMMs) One to four Itanium 2 processors External I/O (8 slots)/disk expansion External SCSI connector
Front panel	System ID switch and LED System Diagnostic Interrupt (SDINT) switch System Reset switch System Power switch and LED Power LED Power Fault LED Cooling Fault LED General Fault LED

2.2 Introduction

The SR870BN4 server system is a compact, high-density, rack mount server system with support for one to four Intel® Itanium® 2 processors and 32-GB DDR SDRAM memory.

The SR870BN4 server system supports several high availability features such as hot-plug PCI, hot-swap and redundant power supply modules, hot-swap and redundant fans for cooling, and hot-swap hard disk drives.

The modular design of the SR870BN4 system provides high serviceability features such as dockable processor/memory subsystem, I/O subsystem, peripheral bay, power bay, and peripheral (LS-240 and DVD/CD) devices. Cable-less interconnects are used between all major subsystems. Additional serviceability features include LED indicators to provide system identification, reset and power status, and interlock status for critical system interconnects. Color-coded parts identify hot-swap and non-hot-swap serviceable components. The scaleable architecture of the SR870BN4 system supports Symmetric Multiprocessing (SMP) and a variety of operating systems.

Figure 1 and Figure 2 show the front and rear isometric views of the system.

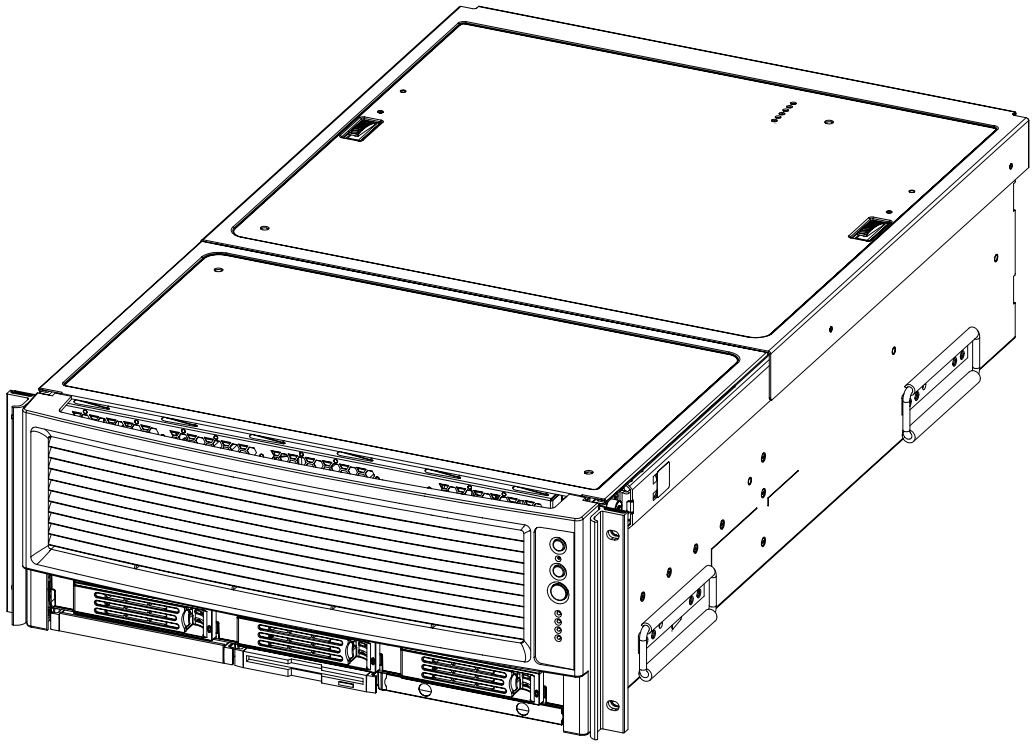


Figure 1. Intel® Server System SR870BN4 (Front Isometric View)

The SR870BN4 system is based on the S870BN4 board set and the Intel® E8870 chipset. The processor board contains sockets for installing up to four Itanium 2 processors and supports up to four power pods.

It contains connectors for two memory mezzanine boards. Each memory board contains eight DDR SDRAM DIMM slots and supports up to 16 GB of memory. The I/O baseboard contains eight 64-bit PCI slots and a connector for the I/O riser card. The I/O riser card contains input/output (I/O) ports and various integrated controllers.

The processor board and two memory boards are installed horizontally in the processor/ memory subsystem. The processor/memory subsystem docks in from the front of the chassis and mates with the midplane board mounted vertically in the middle of the chassis. Color-coded levers are provided on each side of the processor/memory subsystem for ease of insertion and extraction.

The I/O baseboard is installed horizontally in the I/O subsystem. The I/O riser card plugs into a connector provided on the I/O baseboard. The I/O subsystem docks in from the rear of the chassis and mates with the backside of the midplane board. Color-coded levers are provided for ease of insertion and extraction.

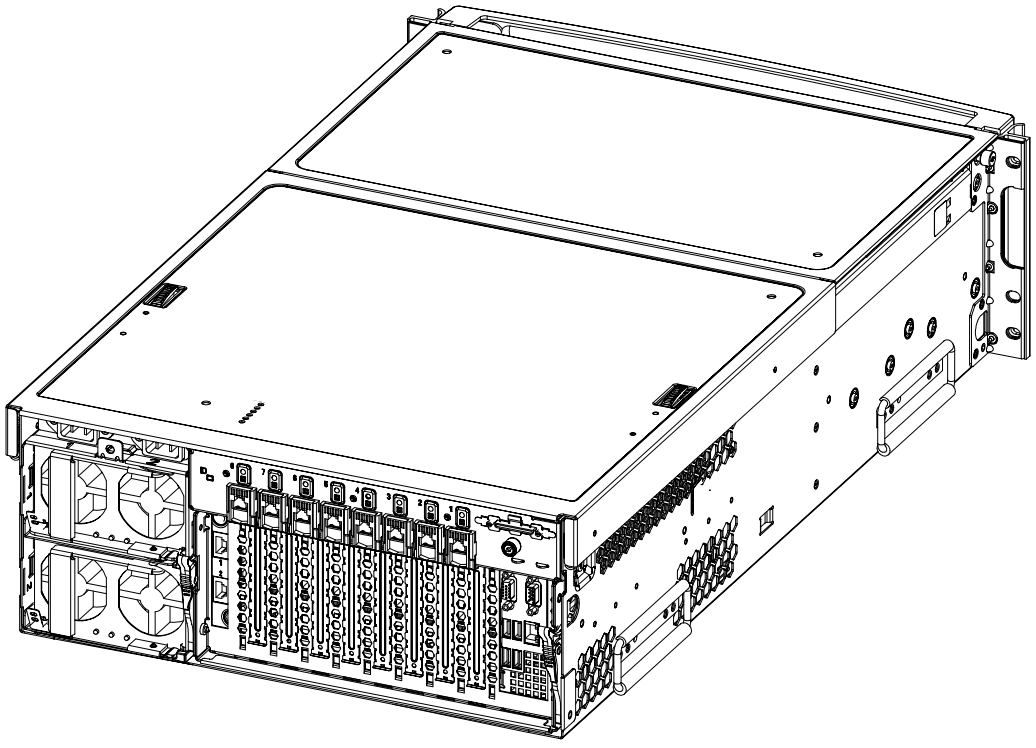


Figure 2. Intel® Server System SR870BN4 (Rear Isometric View)

The peripheral bay consists of the SCSI backplane board, three 1-inch SCSI hard disk drive bays and two slim-line (½-inch) removable media drive bays. One removable media bay supports either a slim-line DVD, CD-ROM, or CD-RW device and the other bay supports a slim-line LS-240 device. The peripheral bay docks in from the front of the system below the processor/ memory subsystem and mates with the midplane board. Color-coded levers are provided for ease of insertion and extraction.

The front panel is located on the right of the processor/memory subsystem and provides user interface for system management via switches and status indicator LEDs. The front panel board contains a card-edge connector that mates with the midplane board. Additional status indicator LEDs are located on the processor/memory subsystem, the I/O subsystem, the peripheral bay, the system fans, and the power supply modules.

The power subsystem consists of the power supply modules, the embedded and plug-in DC-to-DC converters (D2Ds) and processor power pods located on the board set, and the power distribution board. The power supply modules and the power distribution board are installed in the power bay, which mates with the midplane board from the rear of the chassis. The system supports up to two Server System Infrastructure (SSI)-compliant hot-swap power supply modules.

The cooling subsystem contains a hot-swap, redundant (3+1) system fan array installed in the fan bay and the fans in the power supply modules. The fan bay is integrated in the I/O subsystem and is located behind the midplane board. Each system fan contains an individual status indicator LED. A fan failure is also indicated by the cooling fault LED located on the front panel.

The front bezel is installed with snap-on features and can be customized to meet Original Equipment Manufacturer (OEM) industrial design requirements. The bezel design allows adequate airflow to cool system components. It also contains openings to provide access to removable media devices and hot-swap hard disk drives.

Figure 3 shows a block diagram of the SR870BN4 server system.

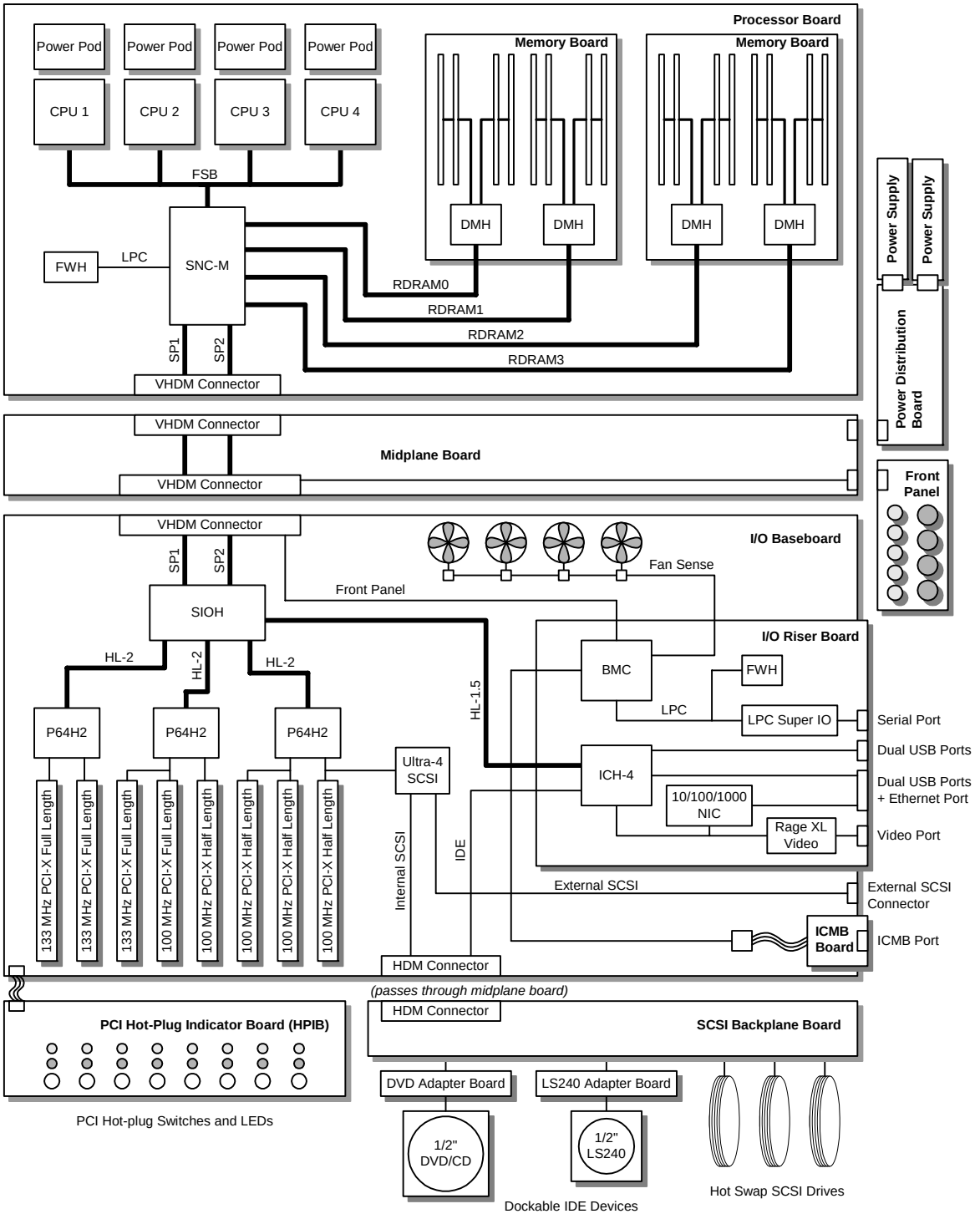


Figure 3. Intel® Server System SR870BN4 Block Diagram

2.3 External Chassis Features – Front

Figure 4 shows the front view of the system with an LS-240 drive installed. Future systems may not include the LS-240 drive, as shown in Figure 5. The remainder of this document will refer to a system with an LS-240 drive. Please tailor the information according to your configuration.

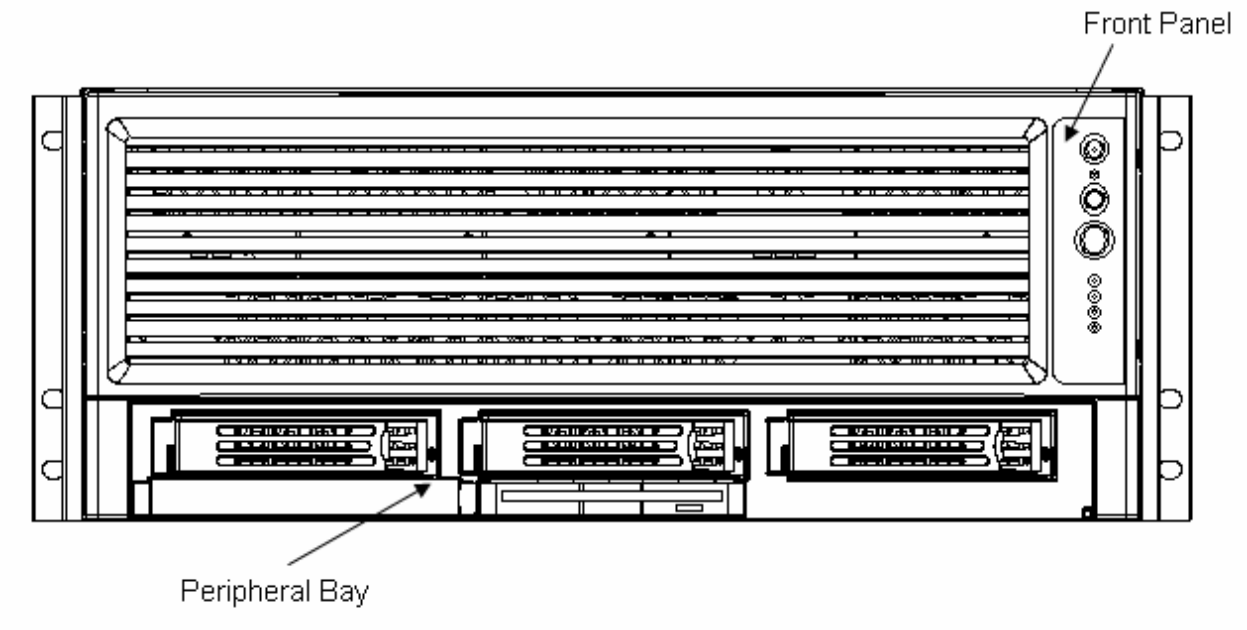


Figure 4. Front View of Intel® Server System SR870BN4 with LS-240 Drive

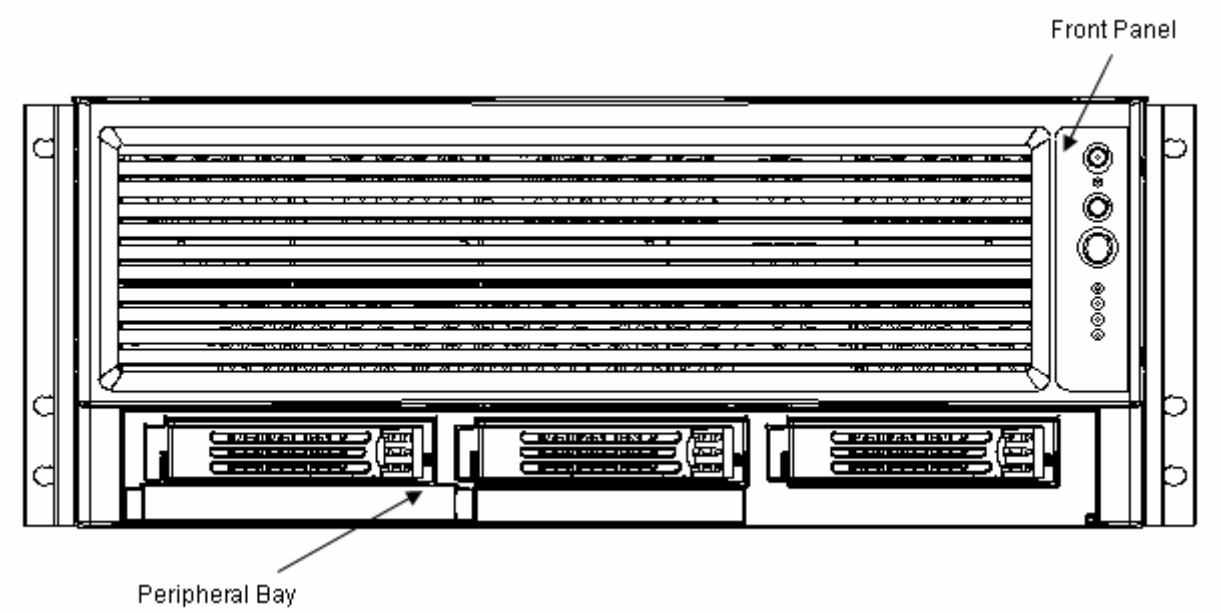


Figure 5. Front View of Intel® Server System SR870BN4 without LS-240 Drive

Figure 6 shows the front view of the system with the front bezel removed. The front bezel provides access to the following user-accessible areas:

- Front panel
- Peripheral bay
- Processor/memory subsystem serviceability LEDs

These areas are described in detail in the following sections.

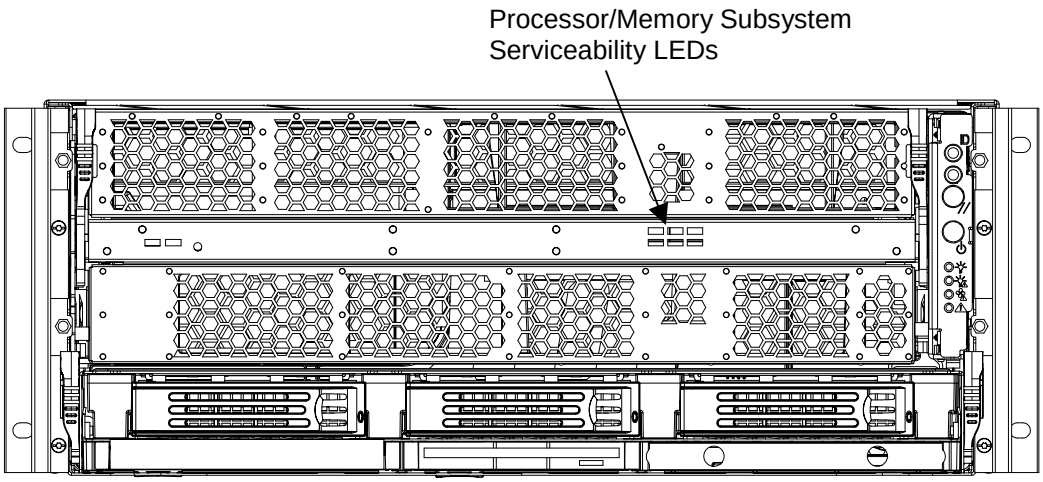


Figure 6. Front View of Intel® Server System SR870BN4 (Shown with Bezel Removed)

2.3.1 Front Panel

The front panel contains system control switches and status indicators. It also contains a speaker. Front panel features are shown in Figure 7 and described in Table 2. Refer to Chapter 6 for a detailed description of the front panel board.

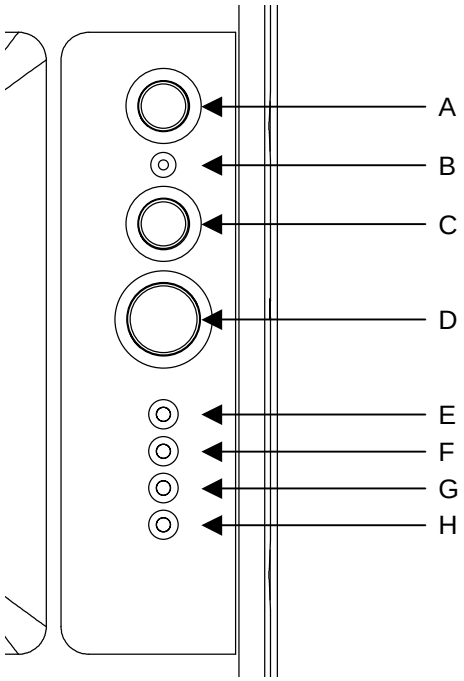


Figure 7. Front Panel Features

Table 2. Front Panel Details

Item	Feature	Description
Front Panel Switches		

Item	Feature	Description		
A	System ID switch and LED	Toggle switch for blue System ID LEDs (one LED is integrated in the switch and a second LED is located on the rear panel of the system). Pressing the switch turns the blue LEDs on Solid; pressing the switch again turns them off. See Section 2.3.1.1 for details.		
B	SDINT (System Diagnostic Interrupt) switch	Asserts SDINT. This switch is accessible through a small opening and requires a narrow tool to activate.		
C	System Reset switch	Resets the system.		
D	System Power switch and LED	Toggles the system power. The LED integrated in this switch is not visible if the front bezel is installed. There is also a second Power LED (Item E) located on the front panel.		
Front Panel LED Indicators				
E	Power LED (green)	Indicates system DC power status and ACPI state.		
		LED	***State***	***ACPI***
		Off	Power off	No
		On	Power on	No
		Off	S4 / S5	Yes
		On	S0	Yes
F	Power Fault LED (yellow)	Indicates power subsystem fault status.		
		LED	***State***	***Description***
		Off	Power OK	No power failures detected
		On	Power Fault	Power supply or voltage failure detected
		Blinking	Power Control Fault	BMC attempts to power on system, but detects power is staying off
G	Cooling Fault LED (yellow)	Indicates cooling subsystem fault status.		
		LED	***State***	***Description***
		Off	Cooling OK	No cooling fault detected
		On	Cooling Fault	Critical threshold exceeded for a fan or temperature sensor
		Blinking	Cooling Warning	Non-critical threshold exceeded for a fan or temperature sensor
H	General Fault LED (yellow)	Indicates a PCI Hot-Plug (PHP) fault.		

2.3.1.1 System ID Switch and LEDs

The system contains a System ID switch located on the front panel and two blue System ID LEDs. One LED is integrated in the System ID switch and a second LED is located at the rear of the system. The System ID LEDs can be activated either by the System ID switch or remotely via server management software to easily locate/identify the system.

Table 3. System ID LED Details

LED State	Description
Off	System ID inactive.
On	System ID active via switch.

Blinking	System ID active via remote command.

Pressing the switch turns the LEDs on solid. Pressing the switch again turns them off.

If activated remotely via server management software, the LEDs will blink for a maximum of 4 minutes. Server management would need to send additional commands to keep the LEDs blinking longer than 4 minutes.

If the LEDs were activated by the switch, they cannot be turned off remotely. If the LEDs were activated remotely, the switch cannot turn them off.

2.3.2 Peripheral Bay

Peripheral bay, shown in Figure 8, consists of the following:

- SCSI backplane board
- Three 1-inch hot-swap Ultra-320 SCSI hard disk drive bays
- Two removable media device bays

3 One ½-inch IDE DVD-ROM, CD-ROM or CD-RW drive

4 One ½-inch IDE LS-240 drive

Note: Installation of an IDE hard disk drive in removable media bays is not supported due to cooling and Electromagnetic Interference (EMI) constraints.

Note: The SR870BN4 peripheral bay supports LVD SCSI drives only. SE devices are supported off the secondary external SCSI channel but are NOT supported in the three hot-swap bays in the SR870BN4 peripheral bay.

Note: IDE devices, such as LS-240 and DVD/CD drives, are not hot-swap devices. System power must be turned off when installing or removing these drives.

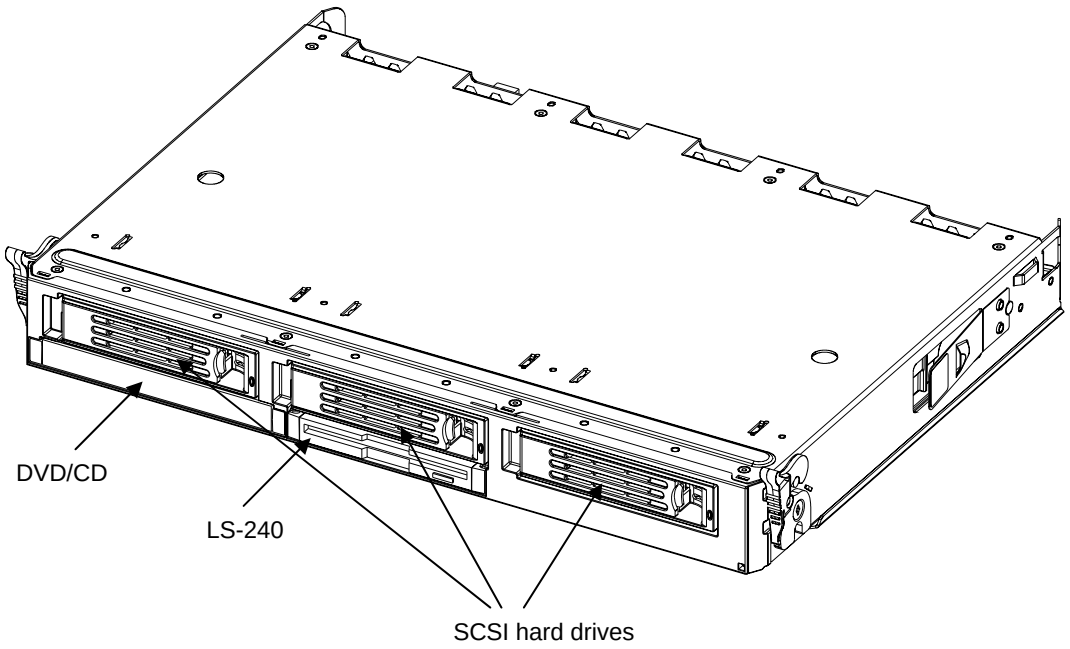


Figure 8. Peripheral Bay

The SCSI backplane board blind mates with the midplane board via the High Density Metric (HDM) connector. It contains three industry standard 80-pin Single Connector Attachment (SCA)-2 connectors for hot-swap hard disk drives. Ultra 320 (or slower) SCSI technology SCA-type hard disk drives can be installed in this bay. The backplane is designed to accept 15,000-RPM (and slower) hard disk drives. SR870BN4 peripheral bay is designed to support Low Voltage Differential (LVD) SCSI disk drives only. Single-Ended (SE) SCSI devices are not supported in the P-Bay, however SE devices are supported off the secondary external SCSI channel.

Note: Because all hard disk drives have different cooling, power, and vibration characteristics, Intel will validate specific hard disk drive types in the SR870BN4 system. Refer to the *SR870BN4 Hardware & Operating System Validation List* for a list of these drives.

Hard drive carriers (described in Chapter 3) that accommodate 3.5-inch by 1.0-inch SCSI disk drives are required as part of the hot-swap implementation. The disk drive is attached to the carrier with four fasteners, and is retained in the chassis by a locking handle.

The SCSI backplane board contains a dual color LED for each hard drive to display status as described in Table 4. The LED signal is transmitted to the front of the system via a light pipe integrated in the hard drive carrier.

Table 4. SCSI Hard Drive LED Details

LED State	Description
Green, solid	The hard drive is powered.
Green, blinking	The hard drive is active.
Yellow/Green blinking	Indicates a hard drive fault and hard drive is powered.
Yellow/Blank blinking	Indicates a hard drive fault and hard drive is not powered.

The SCSI backplane board contains two blind mate connectors for dockable ½-inch IDE peripheral devices (DVD/CD or LS-240). The DVD or CD drive docks into the left connector and the LS-240 drive docks into the right connector. The slim-line LS-240 and DVD/CD drives and the adapter boards are installed in plastic carriers as described in Chapter 3 and are inserted from the front of the peripheral bay. System power must be turned off and the peripheral bay must be removed when removing or installing these drives.

The SCSI backplane board performs the tasks associated with hot-swapping of the hard disk drives and enclosure (chassis) monitoring and management, as specified in the *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification*. The SAF-TE-specified features supported by the SCSI backplane board include, but are not limited to, the following:

- Monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages include: activate a drive fault indicator; power down a drive that has failed; and report backplane temperature.
- SAF-TE intelligent agent, which acts as proxy for "dumb" I^2C* devices (that have no bus mastering capability) during intrachassis communications.

Refer to Chapter 7 for a detailed description of the SCSI backplane board.

2.3.3 Processor/Memory Subsystem Serviceability LEDs

The serviceability status indicator LEDs contained in the processor/memory subsystem are shown in Figure 9 (also see Figure 6) and described in Table 5. These LEDs provide processor presence status and interlock status for memory board connection to the processor board through the MegArray* connectors.

Figure 10 shows the processor slot and memory board labels.

The front bezel must be removed to view these LEDs. Since these LEDs are powered by standby voltage, they provide status as long as AC power is supplied to the system. **There are two additional LEDs and a switch on the processor board which are not used in the SR870BN4 system and are not visible/accessible through the front bezel.**

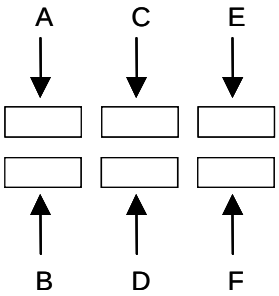


Figure 9. Processor/Memory Subsystem Serviceability LEDs

Table 5. Processor/Memory Subsystem Serviceability LEDs Details

Item	Feature	Description
A	Processor 1 Present (green)	On – Processor 1 is present and installed properly Off – Processor 1 not detected
B	Processor 2 Present (green)	On – Processor 2 is present and installed properly Off – Processor 2 not detected
C	Processor 3 Present (green)	On – Processor 3 is present and installed properly Off – Processor 3 not detected
D	Processor 4 Present (green)	On – Processor 4 is present and installed properly Off – Processor 4 not detected
E	Memory Board – 1 Interlock to Processor Board (green)	On (default) – Memory board – 1 is inserted properly into the processor board Off – Memory board – 1 to processor board interlock not detected
F	Memory Board – 2 Interlock to Processor Board (green)	On (default) – Memory board – 2 is inserted properly into the processor board Off – Memory board – 2 to processor board interlock not detected

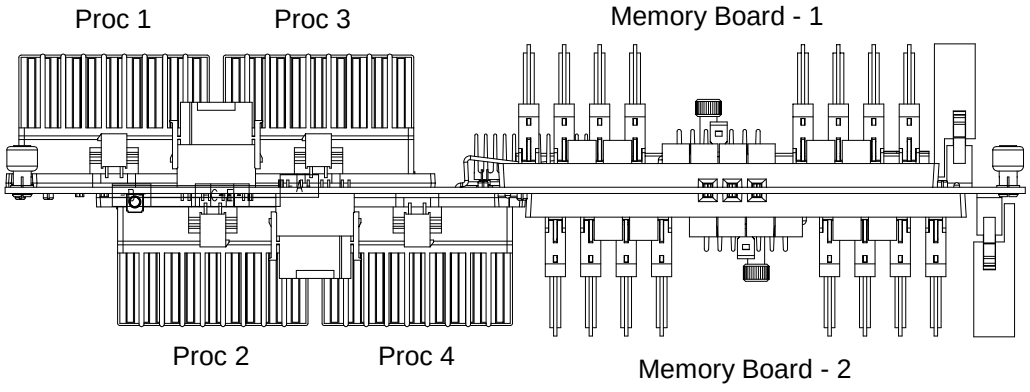


Figure 10. Front View of Processor/Memory Board Assembly

2.4 External Chassis Features – Rear

Figure 11 shows the rear view of the system. The user-accessible connectors and power supply modules are located at the rear of the system. Switches and LEDs for PHP are also located at the rear of the system.

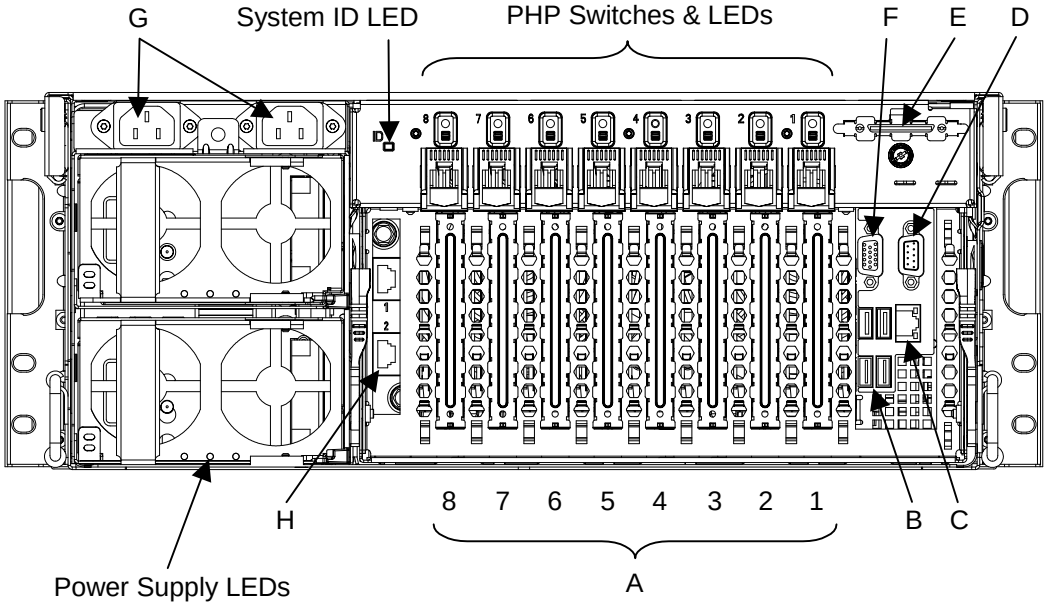


Figure 11. Rear View of System

2.4.1 User-Accessible Connectors

Table 6 lists the user-accessible connectors in the SR870BN4 system.

Table 6. User-Accessible Connectors

Item	Description	
A	PCI Slots[1] (all PCI slots support hot-plug)	
	Slot 1	100 MHz, 64-bit PCI-X slot, half length
	Slot 2	100 MHz, 64-bit PCI-X slot, half length
	Slot 3	100 MHz, 64-bit PCI-X slot, half length
	Slot 4	100 MHz, 64-bit PCI-X slot, half length
	Slot 5	100 MHz, 64-bit PCI-X slot, full length
	Slot 6	133 MHz, 64-bit PCI-X slot, full length
	Slot 7	133 MHz, 64-bit PCI-X slot, full length
	Slot 8	133 MHz, 64-bit PCI-X slot, full length
B	Four USB ports, 4-pin connectors	
C	Ethernet port, RJ45 connector	

Item	Description
D	Serial port[2], 9-pin RS-232 connector
E	External SCSI connector[3] (optional)
F	Video port, standard VGA compatible, 15-pin connector
G	Two AC input power connectors
H	ICMB connectors in/out (optional) ICMB port 1, SEMCONN 6-pin connector ICMB port 2, SEMCONN 6-pin connector

Notes: 1. PCI slots support 3.3 V signal adapter cards only.
2. EMP access is provided via shared serial port.
3. External SCSI bus supports both LVDS and SE signals via the external SCSI connector.

2.4.2 Switches and LEDs at the Rear of the System

Table 7 lists switches and LEDs located at the rear of the system.

Table 7. Switches and LEDs at the Rear of the System

Item	Description
System ID LED (blue)	Identifies the system. Is activated either by the System ID switch located on the front panel or remotely via server management. See Section 2.3.1.1 for details.
PCI Hot-plug Switches and LEDs	
Attention Switch	Notifies PCI hot-plug system software (ACPI PHP ASL) that a PCI hot-plug operation is about to take place. WARNING: Verify in BIOS release notes that this feature is supported before using the Attention button.
MRL (Manually-operated Retention Latch) Switch	Disables power to the PCI slot if a PCI card is present.
Green LED	On – PCI slot is powered Off – PCI slot is powered down
Amber LED	On – PCI slot or card fault condition
Power Supply LEDs	
Power LED (green)	See Section 5.6.11 for details
Failure LED (amber)	See Section 5.6.11 for details
Predictive Failure LED (amber)	See Section 5.6.11 for details
Ethernet Port LEDs	
Status LED (green)	On – Ethernet link is detected Off – Ethernet link not found Blinking – Ethernet link is active
Speed LED (green/amber)	Ethernet speed indicator Amber – 1000 Mbps Green – 100 Mbps Off – 10 Mbps

2.5 External Chassis Features – Top

Figure 12 shows a top view of the system. The system top cover is divided into two sections. The rear section slides backward and provides access to the hot-plug PCI slots and hot-swap

system fans. The serviceability status indicator LEDs, located on the I/O baseboard, are visible through holes in the system top cover.

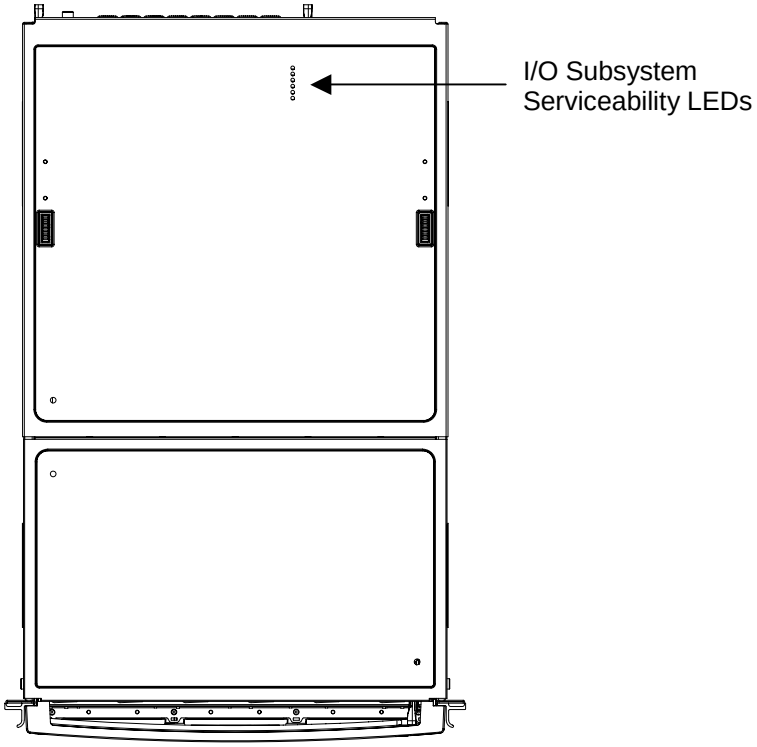


Figure 12. Top View of System

2.5.1 System Fan Status LEDs

Each system fan contains an integrated status LED as shown in Figure 13. The color of this LED is amber and it turns on if a system fan failure occurs. Slide the rear section of the top cover backward to view these LEDs.

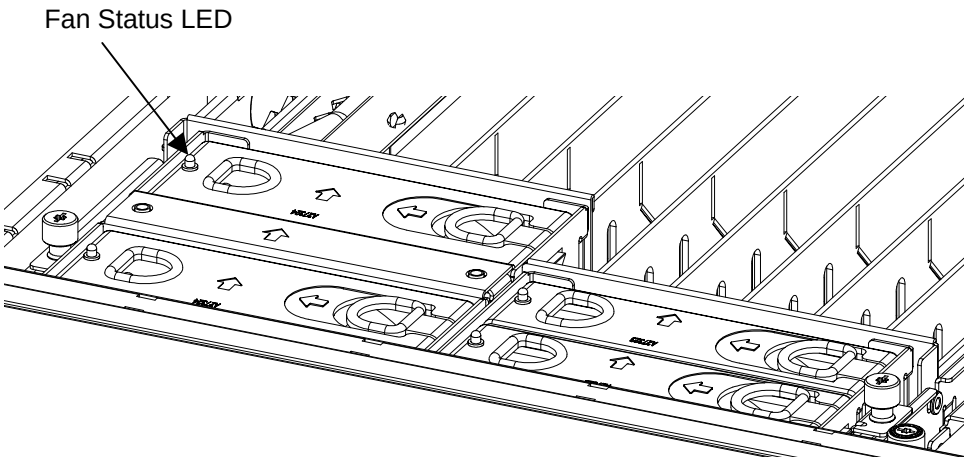


Figure 13. System Fan Status LED

2.5.2 I/O Subsystem Serviceability LEDs

These LEDs, shown in Figure 14 (also see Figure 12), provide system power, system reset, and interlock status for various system interconnects as described in Table 8. They are located on the I/O baseboard and are visible via light-pipes through holes in the rear section of the system top cover. Since these LEDs are powered by standby voltage, they provide status as long as AC power is supplied to the system.

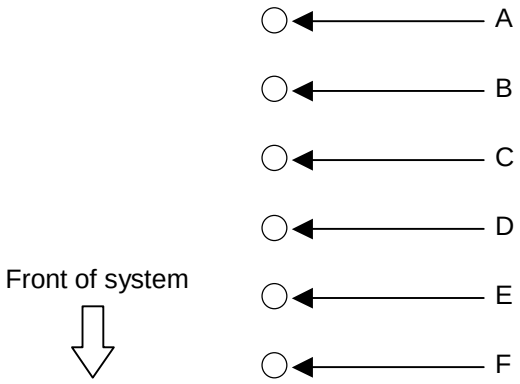


Figure 14. I/O Subsystem Serviceability LEDs

Table 8. I/O Subsystem Serviceability LEDs Details

Item	Feature	Description
A	System Reset Status (amber)	On – system reset asserted Off (default) – system reset not asserted
B	System Power Good (green)	On (default) – system power within normal operational range if system is turned on Off – system power failure
C	I/O Baseboard Interlock to Midplane Board (green)	On (default) – I/O subsystem inserted properly into midplane board Off – I/O subsystem to midplane board interlock not detected
D	I/O Riser Interlock to I/O Baseboard (green)	On (default) – I/O riser inserted properly into I/O baseboard Off – I/O riser to I/O baseboard interlock not detected
E	Processor/Memory Subsystem Interlock to Midplane Board (green)	On (default) – processor/memory subsystem inserted properly into midplane board Off – processor/memory subsystem to midplane board interlock not detected
F	SCSI Backplane Board Interlock to Midplane Board (green)	On (default) – SCSI backplane board inserted properly into midplane board Off – SCSI backplane board to midplane board interlock not detected

2.6 System Board Set

This section highlights the main features of the S870BN4 board set. Refer to the *S870BN4 Board Set External Product Specification* for a detailed description of the board set.

Figure 3 shows the functional blocks of the S870BN4 board set. Major components of the board set include:

- Intel® Itanium® 2 processors
- Intel ® E8870 chipset
- High-capacity DDR SDRAM memory
- High-bandwidth I/O subsystem supporting PCI and PCI-X

The S870BN4 board set contains the following boards:

- Processor board
- Two memory boards
- I/O baseboard
- I/O riser card
- Midplane board

In addition, the SR870BN4 server contains the following system boards:

- Front panel board
- SCSI backplane board
- Power distribution board
- PCI HPIB
- Peripheral adapter boards
- ICMB Board (optional)

The first five boards listed above are described in detail in *S870BN4 Board Set Technical Product Specification*. The remaining board is described in detail in Chapters 6-11 of this document.

2.6.1 Processor Board

The processor board supports the following features:

- Four Intel® Itanium® 2 processor sockets
- Four Intel® Itanium® 2 processor power pod sites
- SNC (Scalable Node Controller) of the Intel® E8870 chip set
- 3-MB Flash using three Firmware Hub (FWH) components
- Two MegArray* memory connectors (400-pin), supporting two Rambus* channels each
- VHDM midplane connector for the following:

5 Two scalability ports

6 Sideband signals

7 Power: 48 V, 12 V standby, 3.3 V standby

- Insertion/ejection mechanism for MegArray* connectors
- Retention mechanism for processors and power pods
- In-Target Probe (ITP) port (processor board components only)
- 2 x 200 MHz Front Side Bus (FSB)
- Four 400-MHz Rambus channels for memory interface
- Core ratio programming via the SNC-M
- Server management logic support
- Joint Test Action Group (JTAG)/boundary scan support through ITP or external source
- Clock buffering
- Two I^2C system management buses (SMBus)
- Three connectors for VID 2.5/3.3 V SSI plug-in A-D2Ds

8 Two 48 V to 2.5 V plug-in D2D for DDR memory support

9 One 48 V to 3.3 V plug-in D2D

- Embedded D2D converters
- Serviceability LEDs

Two processor sockets and one memory connector are mounted on the secondary side of the processor board. **The processor board also contains a switch and two additional LEDs on the front left edge, which are not used in the SR870BN4 server system**.

2.6.2 Memory Board

The main components of the memory board are:

- Eight 184-pin, DDR-SDRAM DIMM sockets
- Two DDR Memory Hub (DMH) components of the Intel® E8870 chip set
- MegArray* connector for mating with the processor board
- An integrated 2.5 V to 1.25 V D2D converter
- DDR termination
- I^2C logic

10 Field Replaceable Unit (FRU) device ID accessed through a private I^2C* bus

- Temperature sensors

DIMM sites accept 184-pin registered 2.5 V DDR-SDRAM DIMMs.

Note: DIMM sites must be populated according to a set of defined rules. Refer to the Memory Board chapter of *S870BN4 Board Set Technical Product Specification* for details.

2.6.3 I/O Baseboard

The I/O baseboard connects to two scalability ports through the midplane board. The I/O baseboard supports the following features:

- One Server I/O Hub (SIOH) component of the Intel E8870 chip set
- Three P64H2 components
- Eight hot-plug PCI slots

11 Three 64-bit, 133 MHz PCI-X, full length

12 One 64-bit, 100 MHz PCI-X, full length

13 Four 64-bit, 100 MHz PCI-X, half length

- Connector for I/O riser board
- SCSI 320 controller
- ITP connector (I/O baseboard components)
- Two 5-V T-D2D connectors
- Two VID 3.3-V T-D2D connectors
- Integrated D2Ds
- VHDM midplane connector
- Four connectors for hot-swap system fans
- Clock generation and distribution
- Reset generation and distribution
- Server management logic

2.6.4 I/O Riser Card

The I/O riser interfaces to the I/O baseboard through an 8-bit Hub-Link (HL) 1.5 bus and supports the following features:

One I/O Control Hub 4 (ICH4) component

14 Four Universal Serial Bus (USB) ports

15 One IDE interface routed through the I/O board connector supporting two ATA33 devices

Network Interface Card (NIC) 10/100/1000 Ethernet controller

16 One Ethernet port

Low Pin Count (LPC) Super I/O*

17 One serial port

4 MB of Flash using four FWH components

BMC server management controller

ICMB controller integrated in the BMC

Integrated ATI Rage* XL video controller and memory

18 Video port

- Power control - Advanced Configuration and Power Interface (ACPI)
- Speaker control
- Integrated standby voltage D2Ds generating 3.3 V standby and 5 V standby

2.6.5 Midplane Board

The passive midplane board contains the following features:

- VHDM connector for the processor/memory subsystem
- VHDM connector for the I/O subsystem
- One HDM connector for routing the SCSI bus, the IDE bus, and miscellaneous signals between the I/O board and the SCSI backplane
- Routing of four scalability ports
- 48 V power distribution
- 12 V standby distribution
- 3.3 V standby distribution
- 12 V distribution from the SCSI backplane board to the I/O board and power distribution board
- Power distribution board connector
- Front panel connector

2.6.6 Front Panel Board

The front panel board contains switches, LEDs, and speaker for system interface as described in Section 2.3.1. Refer to Chapter 6 for a detailed description of this board.

2.6.7 SCSI Backplane Board

The SCSI backplane board supports three LVDS hard drives. Its features include:

- Three SCA connectors for hot-swap 1-inch SCSI hard drives
- One blind-mate connector for dockable slim-line IDE LS-240 device

- One blind-mate connector for dockable slim-line IDE DVD or CD device
- SCSI accessed fault-tolerant enclosures (SAF-TE) logic
- 48 V to 12 V integrated D2D converter
- 12 V to 5 V integrated D2D converter
- 5 V to 2.5 V linear regulator

Refer to Chapter 7 for a detailed description of this board.

2.6.8 Power Distribution Board

The power distribution board docks into the midplane board and provides the interface with the 48 V hot-swap power supply modules. The 48 V and 12 V standby are then delivered to the midplane board. The power distribution board supports up to two power supplies. In the event of a power supply failure, the power supply fans are powered by 12 V generated on the SCSI backplane board, which is routed back to this board through the midplane board. Refer to Chapter 8 for a detailed description of this board.

2.6.9 PCI Hot-Plug Indicator Board (HPIB)

The PCI hot-plug indicator board is located above the PCI slots in the I/O subsystem. It contains the LEDs and switches required for PCI hot-plug support. These LEDs are visible from the rear of the chassis and internal to the chassis. This board also contains the System ID LED visible from the rear of the system. Refer to Chapter 9 for a detailed description of this board.

2.6.10 Peripheral Adapter Boards

The DVD/CD and LS-240 adapter boards provide the interface between the ½-inch IDE peripheral devices (LS-240, DVD/CD) and the SCSI backplane board. These boards are described in detail in Chapter 10.

2.6.11 ICMB Board (optional)

This board is optional and contains two 6-pin SEMCONN* ICMB connectors for external interface. Refer to Chapter 11 for more details.

2.7 Power Subsystem

The SR870BN4 power subsystem is based on an SSI distributed power architecture. It contains the SSI power supply modules, the embedded and plug-in D2D converters, the processor power pods, and the power distribution board. The main power from the power supplies is distributed over a 48 V rail. This allows for greater power to be delivered using less current and thus smaller power connectors. The 48 V power is converted locally at point-of-load on the board set using either embedded or plug-in D2Ds. This results in tighter voltage regulation and better control of power under local conditions.

The total power requirement for the SR870BN4 server system exceeds the 240 VA energy hazard limit that defines an operator-accessible area. As a result, only qualified technical individuals should access the processor, memory, and non-hot-plug I/O subsystem areas while the system is energized.

2.7.1 Power Supply

The 48 V hot-swap, SSI-compliant power supply modules are rated at 1200 W over an input range of 180-264 VAC and at 700 W over an input range of 90-132 Alternating Current Voltage (VAC). They are accessed from the rear of the chassis. The power subsystem can be configured as following:

- Two power supply modules installed, (1+1) redundancy at 220 VAC for a fully configured system
- One power supply module installed, non-redundant for a fully configured system

Note: Proper system cooling requires the population of both power supply bays either by a power supply module or by a filler panel.

One power supply module connected to 220 VAC is capable of handling the worst-case power requirements for a fully configured SR870BN4 server system. This includes four Intel® Itanium® 2 processors, 32 GB of memory, eight PCI add-in cards, three hard disk drives, a DVD or CD drive, and an LS-240 drive. When connected to 110 VAC, two power supply modules are needed to handle the worst-case power requirements for a fully configured system.

When the system is configured with two power supply modules, the hot-swap feature allows the user to replace a failed power supply module without affecting the system functionality.

Each power supply module requires one power cord to supply AC power to the system. When two power supply modules and two power cords are installed, the system supports (1+1) power cord redundancy at 220 VAC. This feature allows the system to be powered by two separate AC sources. In this configuration, the system will continue to function without interruption if one of the AC sources fails.

Refer to *Chapter 5: Power Subsystem* of this document for detailed specifications.

2.7.2 Plug-in DC to DC (D2D) Converter

In addition to the embedded D2Ds on the board set to perform various voltage conversions, the SR870BN4 uses two types of plug-in D2D converters (called T-D2Ds): 5 V output and Voltage ID (VID) (2.5 or 3.3 V output). A control bit set by the board determines output voltage on the VID D2D. The T-D2Ds contain an LED for failure indication. The processor board supports three VID T-D2Ds (one 3.3 V and two 2.5 V). The I/O baseboard supports two 5 V and two VID (3.3 V) T-D2Ds. Each T-D2D powers a separate plane on the boards; therefore all T-D2D slots must be populated. The T-D2Ds plug into 70-pin connectors, which are compatible with SSI Advanced D2D (A-D2D) specification. Refer to *DC-DC Converter Specifications* for detailed information on the T-D2Ds.

2.7.3 Processor Power Pod

A dedicated power pod supplies power to each processor. The input connector of the power pod is connected to the 48 V power rail on the processor board via a short Y-cable. One Y-cable supports two power pods mounted on the same side of the processor board. The output connector of the power pod mates directly with the processor package.

2.8 Cooling Subsystem

A combination of system fans installed in the fan bay and power supply fans provides the airflow necessary to cool the SR870BN4 system components. A series pair of 120 X 38 mm system fans cools the processors and part of the I/O subsystem. The rest of the processor/memory and I/O subsystem components, hard drives, and power supplies are cooled by a series pair of 120 X 25 mm system fans along with the power supply fans. Figure 15 describes the cooling subsystem layout.

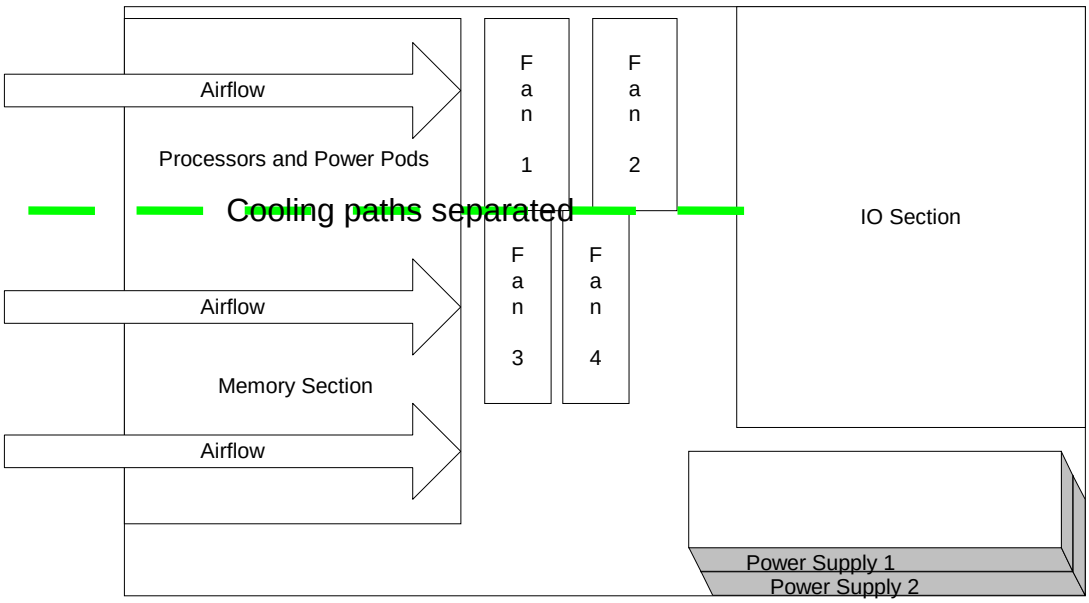


Figure 15. Cooling Subsystem Layout

The cooling subsystem is designed to be redundant and capable of being hot-swapped. In the event of a cooling component failure the system is cooled such that all components will continue to meet their temperature specifications. Following a failure, the failed cooling component can be hot-swapped, while cooling for the system is maintained.

The SR870BN4 supports only a fully populated system fan configuration. Configurations with both power supplies are cooling-redundant. The system will continue to meet thermal specifications with either a system fan or a power supply failure (for those systems with two power supplies).

Hot-swap system fans drop into the fan bay and interface with connectors on the I/O baseboard. Each system fan contains a status LED. A system fan failure is indicated by the corresponding fan LED and also by the Cooling Fault LED on the front panel. All system fans have tachometer output and internal speed control.

To maintain adequate cooling for system components, system fans must be hot-swapped within a two-minute period (this period only applies to the time that the fan or power supply is physically removed, not from the time of failure).

2.8.1 System Acoustic Description

The SR870BN4 system meets acoustic requirements defined in the *Intel Environmental Standards Handbook.* These specifications must be met only up to limited room temperatures and not under failure conditions. To enable the system to meet these specifications requires that the fans run at a lower speed when the room ambient temperature is below a pre-determined value and there are no failures. This value is referred to as the acoustic threshold. Only the fully configured system will be tested and must meet the acoustic specifications.

2.8.2 System Thermal Control

To enable the system to meet all thermal and acoustic requirements, system actions must be taken in the event of cooling failures and high ambient temperature. The thermal control system performs these functions using both hardware and firmware.

To ensure that all system components meet their specifications, higher fan speeds (fan boost) must be applied when the following conditions occur:

- Room ambient exceeds the acoustic threshold, or
- A system fan or power supply fan failure occurs.

Thermal sensors are placed on the processor, memory, I/O, and SCSI boards either on the chip set or on board locations. The sensed temperatures are used for fan speed control and to provide the user with indicators of system thermal performance.

2.8.2.1 Fan Boost Due to High Ambient Temperature

In the case of room ambient excursion above the acoustic threshold, all system and power supply fans increase to high speed. Fan speed will return to low speed only after the room ambient temperature falls below the acoustic threshold minus a hysteresis value.

A sensor on the processor board measures unheated air coming from the surrounding room. This sensor determines whether an ambient excursion above the acoustic threshold has occurred and controls the fan speed (although all sensors could theoretically control fan speed, only this one sensor controls the speed due to its narrow threshold range).

In a 1+0 power supply configuration, the power supply fan speed also increases based on high ambient temperature as determined by exceeding the acoustic threshold.

2.8.2.2 Fan Boost Due to Fan or Power Supply Failure

The system can continue to operate and meet all thermal requirements if a single failure occurs.

Failure is detected when a fan's speed falls below a lower threshold. The power supplies have their own internal circuitry for detecting and notifying the system of a power supply fan failure.

If a power supply fails for any reason (including loss of AC power) the inactive power supply's fans are powered by the 12 V input from the system.

After detection of the fan or power supply failure, all fan speeds are changed to boost levels. Following a failure, all fans remain at high speed until the failed fan or power supply is replaced. Replacement of the failed fan is detected by a change in state of the fan presence signal.

Following the replacement as detected by the fan presence, fan failure monitoring at the lower speed levels is reactivated.

2.9 PCI Hot-Plug (PHP)

2.9.1 Description

The PHP feature allows the user to add, remove, and replace a standard PCI adapter card while the system is running and without powering down the system.

- "Hot Add" allows the user to add a PCI card to the system. The system BIOS needs to reserve PCI resource space for the added adapter card upon boot.
- "Hot Remove" allows the user to remove a PCI card from the system.

A PCI hot-plug operation requires support from the OS and the BIOS, apart from the hardware support to control the power and signals of each slot. It is a requirement that PHP functionality be based on open standards (e.g., ACPI).

2.9.2 Hardware Components

The hardware technology and methods for the implementation of PCI hot-plug conform to the *PCI Hot-plug Specification*. The basic hardware components of the SR870BN4 PHP system are:

- Power cycling and reset generation hardware that complies with the *PCI Local Bus Specification*, Revision 2.2.
- Bus isolation switches to physically disconnect the PHP capable card from the PCI bus. These switches are located on the I/O baseboard between each PHP PCI slot. Single slot buses do not use the bus isolation switches; instead, the hot-plug controller drives all lines low when the slot is un-powered. All bi-directional lines and all card inputs are low when the slot is un-powered. JTAG, TMS and TDI are floated.
- Two pairs of LED indicators for each PCI slot located on the HPIB to provide service personnel with positive slot identification. One pair of LEDs is visible from above the I/O subsystem when the top cover is removed; the other pair of LEDs is visible from the rear of the system through holes in the chassis. A lit green LED indicates that power is applied to the PCI slot. A lit amber LED indicates a fault condition with the PCI slot or card.
- An attention push-button switch for each PCI slot located on the HPIB, used to gain the attention of software to recognize a newly added card or to recognize a request to remove a card. This switch requires a narrow tool for access.
- An Manually-operated Retention Latch (MRL) switch that contains a rocker and a Hall-effect sensor are provided for each PCI slot. When the MRL switch is opened, it disables power to the corresponding PCI slot.
- Protection hardware to isolate the live components of the system from the PCI card being inserted/removed. Mechanical barriers prevent access to non-PHP areas of the system.
- A controller element that controls the above hardware and provides an interface for system software.

2.9.3 Software Components

The main software components of the SR870BN4 PHP system are described below.

2.9.3.1 PHP User Interface

- OS specific.
- Either integrated with the OS or a stand-alone PHP Graphical User Interface (GUI).
- Provides user with access to PHP functions.
- Receives user input and sends requests to the OS-specific Plug and Play mechanism.
- Displays the status of the PCI slot.

2.9.3.2 Plug and Play Mechanism

- OS specific.
- Mediates between the user interface and the PHP ACPI Source Language (ASL) code and is responsible for configuring, loading, and unloading the adapter driver component.
- Reports adapter card status to the PHP user interface.

2.9.3.3 BIOS

- Responsible for initialization of the PHP hardware components.
- ACPI PHP ASL code, integrated in the BIOS, controls PHP hardware components and communicates desired actions to/from the OS-specific Plug and Play mechanism.

2.9.3.4 Adapter Drivers

An adapter card must be qualified by Intel to guarantee proper hot-plug functionality. A limited number of network and storage adapters will be qualified initially. For more information on which adapter cards have been qualified, refer to the *SR870BN4 Hardware & Operating System Validation List* and/or the *SR870BN4 Tested Hardware and Operating System List*.

Refer to the *PCI Hot-plug Specification* for additional details on PHP implementation.

2.10 Server Management

The SR870BN4 server management subsystem is based on the IPMI specifications and conforms to the *IPMI v1.5 Specification*. The server management features are implemented using two microcontrollers: the Sahalee Baseboard Management Controller (BMC) on the I/O riser card, and the SCSI hot-swap controller on the SCSI backplane board. The ICMB controller is integrated in the Sahalee BMC and provides an interface to the external ICMB via the ICMB board. The functions of each component are summarized in the following sections.

The firmware of each microcontroller is field-upgradeable using the *Server Management Firmware Update Utility*. Refer to the *SR870BN4 Server Management External Architecture Specification* for more details.

2.10.1 Baseboard Management Controller (BMC)

The BMC is comprised of a Sahalee microcontroller and associated circuitry located on the I/O riser board. The primary purpose of the BMC is to autonomously monitor for system platform management events, and log their occurrence in the non-volatile System Event Log (SEL). This includes events such as over-temperature and over-voltage conditions, fan failures, etc. The BMC also provides the interface to the monitored information so system management software can poll and retrieve the present status of the platform.

The BMC also provides the interface to the non-volatile Sensor Data Record (SDR) Repository. Sensor Data Records provide a set of information that system management software can use to automatically configure itself for the number and type of IPMI sensors (e.g., temperature sensors, voltage sensors, etc.) in the system.

The following is a list of the major functions for the BMC:

- System Power Control

19 ACPI Power Control

20 ACPI Sleep Support

21 Minimum Power Off Time

- System Reset Control
- System Initialization

22 Processor Temperature and Voltage Threshold Setting

23 Fault Resilient Booting (FRB)

- Front Panel User Interface

24 Power LED control

25 Power Fault LED control

26 Cooling Fault LED control

27 General Fault LED control

28 System ID LED control

29 Reset Button control

30 Power Button control

31 SDINT Button control

32 System ID Button control

33 CMOS Clearing

- System Fan Management
- System Management Watchdog Timer
- System Event Log (SEL) interface
- Sensor Data Record (SDR) Repository interface
- SDR/SEL Timestamp Clock
- FRU Inventory Device
- Diagnostics and Beep Code generation
- Event Message Generation and Reception
- Platform Event Filtering (PEF)
- Dial Page Alerting

- Alert over LAN
- Alert over Serial/PPP
- Processor Core Ratio programming
- Battery monitoring
- Sensor monitoring

34 Temperature monitoring
35 Voltage monitoring
36 Fan monitoring
37 Processor Presence monitoring
38 Interlock Status monitoring
39 Power Supply monitoring
40 Hot-plug PCI Slot monitoring

- Itanium® 2 processor Processor Information ROM (PIROM) and Scratch Electrically Erasable Programmable ROM (EEPROM) access
- IPMB Communication interface
- EMP interface
- LAN interface
- ICMB interface

Refer to the *SR870BN4 Baseboard Management Controller External Product Specification* for further details.

2.10.2 Hot Swap Controller (HSC)

The Hot Swap Controller (HSC) resides on the SCSI backplane board. The primary functions of the HSC are as follows:

- Implements the SAF-TE command set
- Controls the SCSI Hard Drive fault LEDs
- Provides a path for management information via the SCSI bus
- Retrieves hard disk drive fault status, SCSI backplane temperature, and fan failure information via IPMB
- Queries the status of the power distribution board by retrieving information from the Sahalee server management controller via IPMB
- Controls hard disk drive power-on and power-down, facilitating hot-swapping

2.10.3 Intelligent Chassis Management Bus (ICMB)

The ICMB is an inter-chassis management bus that provides management functions for ‘clustered’ or ‘grouped’ host systems and external peripheral chassis by transferring IPMI messages between different chassis. Since ICMB provides a way to deliver IPMI messages to the BMC, functions such as power and reset control, SEL, SDR, FRU and sensor access are available, along with the ability to deliver IPMI messages to other BMC interfaces such as the System Interface and IPMB. Refer to the *Intelligent Chassis Management Bus (ICMB) Bridge Specification* for additional information.

ICMB bridge controller functionality is integrated into the Sahalee BMC. The SR870BN4 provides two 6-pin SEMCONN (Type A) ICMB connectors located on the ICMB board.

The ICMB specification provides for optional point-to-point Connector ID signals and associated commands that can be used to determine which connectors are being used to interconnect systems and chassis. The SR870BN4 includes support for two Connector ID signals (one per connector).

2.11 Reliability, Availability and Serviceability (RAS)

The SR870BN4 server system supports the following reliability, availability, and serviceability (RAS) features:

- **Reliability features**
  - Machine check architecture
  - Error checking code (ECC) in main memory and processor caches
  - ECC, parity, and protocol checking on the FSB
  - ECC on SP data; parity on SP FLITs; link level retries on SP bus
  - ECC on HL-2.0 interface; parity on the HL-1.5 interface
  - Parity checking on PCI buses
  - Voltage and temperature monitoring throughout the system

- **Availability features**
  - Redundant hot-swap power supplies
  - Dual redundant power cords
  - Hot-plug PCI
  - Hot-swap SCSI hard drives
  - Redundant hot-swap system fans

- **Serviceability features**
  - Modular design
  - Tool-less installation and removal of major modules
  - Cable-less interconnect between all major subsystems
    41 Processor/memory subsystem to midplane board
    42 I/O susystem to midplane board
    43 Peripheral bay to midplane board
    44 Power bay to midplane board
    45 Front panel to midplane board
  - Dockable processor/memory subsystem
  - Dockable I/O subsystem
  - Dockable peripheral bay
  - Dockable power bay
  - Dockable IDE peripheral (DVD/CD and LS-240) devices
  - Dockable front panel

- Color coded parts to identify serviceable components
  - Green – Hot-swap or hot-plug components
  - Blue – Non-hot-swap components
- System ID switch on front panel and blue System ID LEDs on the front and rear of the system
- Status LEDs (powered by standby voltage) to indicate
  - Processor module presence
  - Memory board connector interlock
  - Processor/memory subsystem connector interlock
  - I/O subsystem connector interlock
  - SCSI backplane board connector interlock
  - I/O riser card connector interlock

Note: System errors routed to the PCI bus SERR# are elevated to machine check errors.

Note: All boards are connected by a server management bus to satisfy the system RAS requirements.

Note: System must be turned off and all AC power cords must be disconnected to service non-hot-swap components.

2.12 Expansion Support

Table 9 summarizes the expansion support provided by the SR870BN4 server system.

Table 9. SR870BN4 Server System Expansion Support

Quantity	Item
3	64-bit, 133 MHz hot-plug PCI-X expansion bus slots
5	64-bit, 100 MHz hot-plug PCI-X expansion bus slots
3	Ultra 160/320 SCA-2 hard disk drive bays
16	DDR SDRAM Registered DIMM slots

2.13 Specifications

2.13.1 Environmental Specifications

The SR870BN4 server system will be tested to the environmental specifications as indicated in Table 10.

Table 10. Environmental Specifications Summary

Environment	Specification
Temperature operating	10 °C to 35 °C (50 °F to 95 °F)
Temperature non-operating	-40 °C to 70 °C (-40 °F to 158 °F)

Altitude	-30 to 1,500 m (-100 to 5,000 ft)
Humidity non-operating	95 %, non-condensing at temperatures of 25 °C (77 °F) to 30 °C (86 °F)
Vibration non-operating	2.2 Grms, 10 minutes per axis on each of the three axes
Shock operating	Half-sine 2 G, 11 ms pulse, 100 pulses in each direction, on each of the three axes
Shock non-operating	Trapezoidal, 25 G, two drops on each of six faces V : 175 inches/sec on bottom face drop, 90 inches/sec on other 5 faces
Safety	UL 1950, CSA 950, IEC 950, TUV/GS EN60950
Emissions	Certified to FCC Class A; tested to CISPR 22 Class A, EN 55022 Class A, VCCI Class A ITE, AS/NZS 3548 Class A
Immunity	Verified to comply with EN 55024
Electrostatic discharge	Tested to ESD levels up to 15 kilovolts (kV) air discharge and up to 8 kV contact discharge without physical damage
Acoustic	Sound pressure: < 60 dBA at ambient temperature < 28° C measured at bystander, floor standing position Sound power: < 6.7 BA at ambient temperature < 28° C measured using the Dome Method

2.13.2 Physical Specifications

Table 11 describes the physical specifications of the SR870BN4 server system.

Table 11. Physical Specifications

Specification	Value
Height	6.9 inches (178 mm)
Width	17.5 inches (445 mm)
Depth	28 inches (711 mm)
Front clearance	3 inches (76 mm)
Side clearance	1 inch (25 mm)
Rear clearance	6 inches (152 mm)
Weight[1]	106 lbs (48 kg)

Note: 1. The system weight listed above is an estimate for a fully configured system and will vary depending on number of peripheral devices and add-in cards, as well as the number of processors and DIMMs installed in the system.

3. System Chassis and Sub-Assemblies

This chapter describes the SR870BN4 system chassis and sub-assemblies that reside within the chassis. This chapter is organized into the following sections:

Section 3.1: Main Chassis

Section 3.2: Chassis Sheet Metal Enclosure

Section 3.3 Power Subsystem

Section 3.4: Processor/Memory Subsystem

Section 3.5: I/O Subsystem and Fan Bay

Section 3.6: Peripheral Bay

Section 3.7: Front Panel Assembly

Section 3.8: Top Cover

Section 3.9: Bezel

3.1 Main Chassis

The SR870BN4 system utilizes a standard 19-inch EIA chassis that is 4U high x 28.0-inches deep. The 4U height is defined by standard EIA rack units where 1U = 1.75-inches. ((4U x 1.75”/U) – 0.10” = 6.90”). The 28.0-inch depth does not include cables or bezel.

The chassis has been designed for serviceability and manufacturability. All major modules in the chassis are easily accessible. They can be inserted or extracted from the system without the use of tools. Hot-swap component replacement capability is provided for system fans, hard drives, power supplies, and PCI cards.

All system FRUs can be replaced without any loose hardware.

The following sections describe the sub-assemblies that complete the SR870BN4 server.

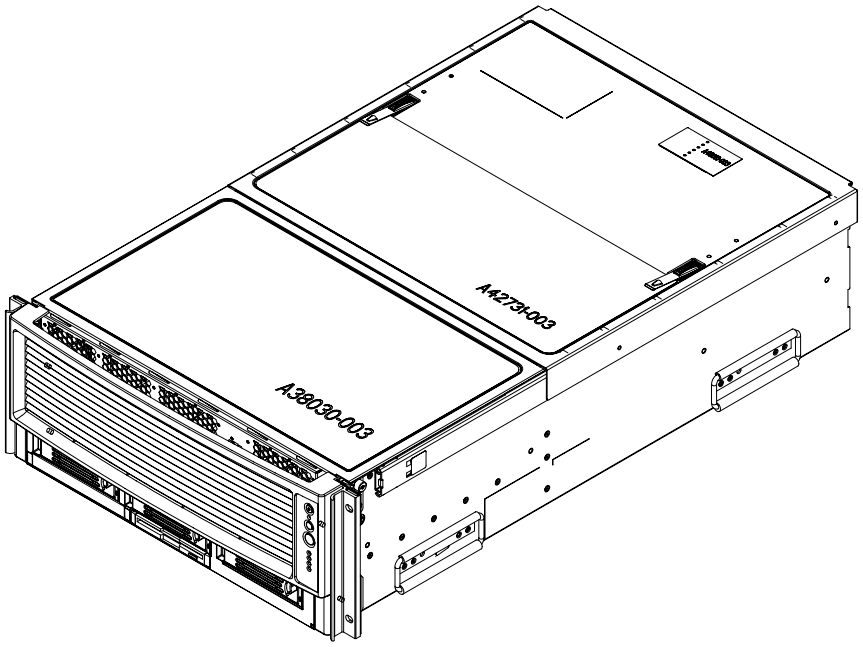


Figure 16. Intel® Server System SR870BN4 Chassis

3.2 Chassis Sheet Metal Enclosure

The base sheet metal enclosure consists of the 4U chassis and the top cover. The structural support for the midplane board and processor/memory subsystem are permanently attached to the chassis. The midplane board support is designed as a die-cast structure that is riveted to the chassis assembly.

3.2.1 Midplane Assembly

The midplane board is installed in the center of the chassis utilizing five plastic rivets, which mount the board to the die-cast support. The rivets are captive to the midplane board, which allow for easy installation of the board into the chassis.

Once the midplane board assembly is installed, all other system modules dock into the chassis.

3.2.2 Slide Rails/Chassis Handles

The SR870BN4 server chassis is designed to accommodate slide rails to mount the chassis into standard 19-inch racks. Four handles are provided on the sides of the chassis to aid with the installation of the chassis in a rack. The overall chassis width is 16.5-inches, which allows the handles to be permanently mounted to the chassis without interfering with the sliding of the chassis into a rack.

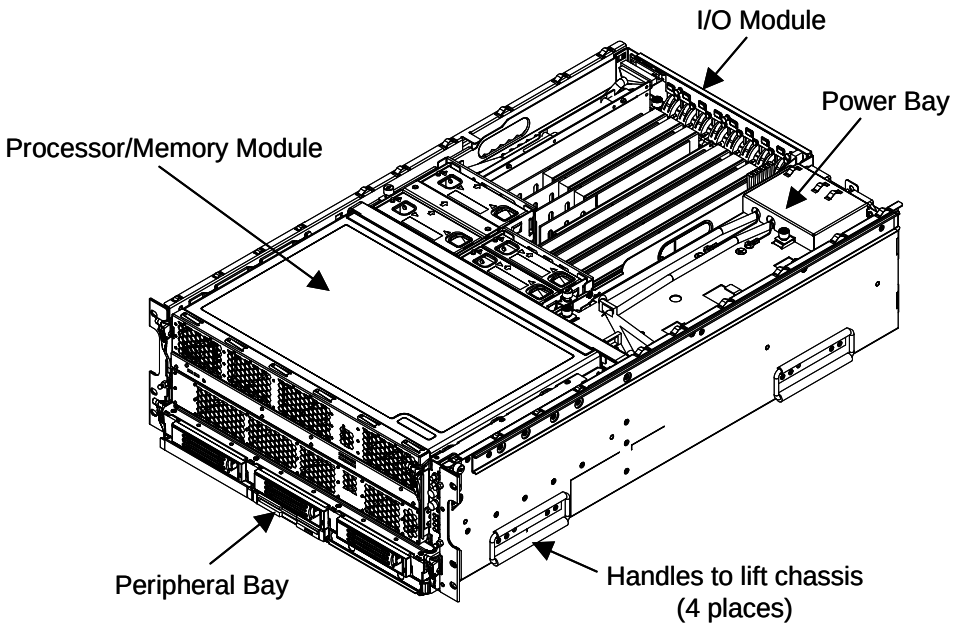


Figure 17. Front Isometric View

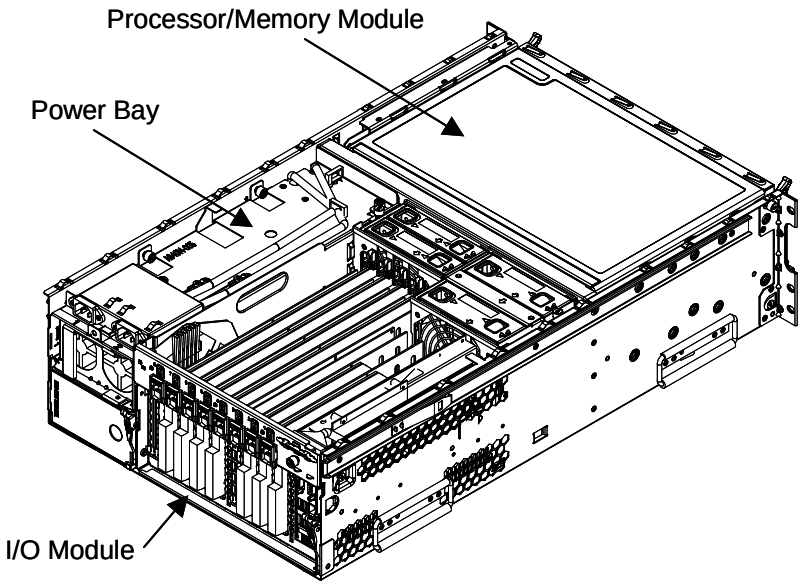


Figure 18. Rear Isometric View

3.3 Power Bay

The power bay mounts in the back of the chassis and provides space for two SSI-compliant 48 VDC power supplies. The redundant AC power inputs enter the bay above the power supplies. The AC power is filtered with a combination 15 Amp power plug/filter. The cables are routed across the top of the power supplies and mount behind the power supply.

The power distribution board mounts with one captive screw to the back of the power bay. The board docks into the midplane board as the power bay is installed in the chassis.

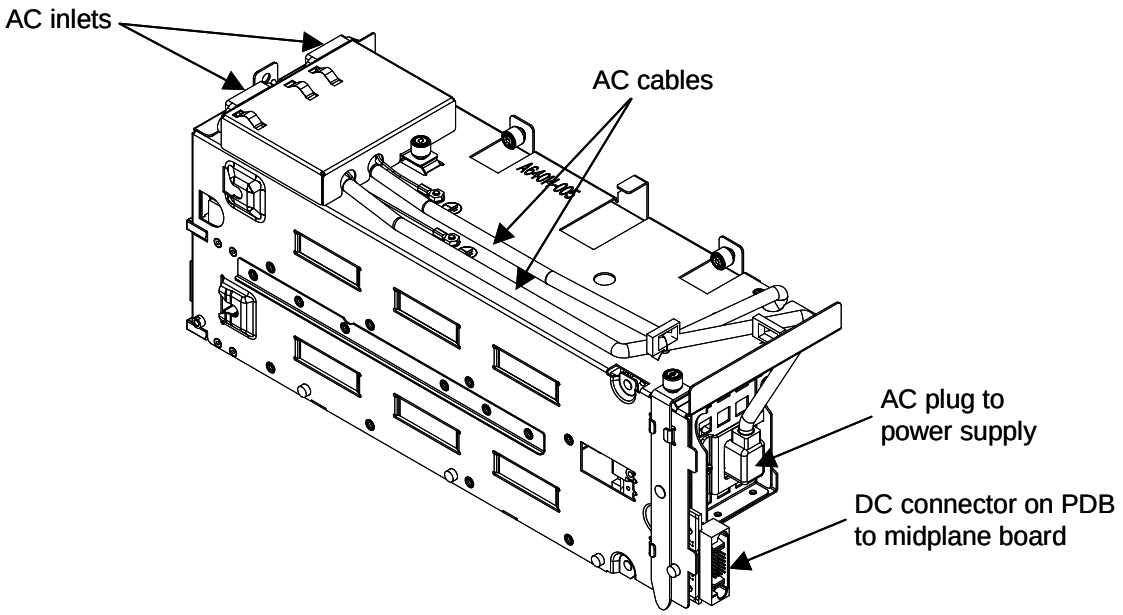


Figure 19. Power Bay

3.4 Processor/Memory Subsystem

The processor/memory subsystem is fabricated from a combination of structural foam and sheet metal.

The module has three primary pieces: the carrier frame, the top cover, and the bottom cover. The processor board is mounted to the assembly by opening the top cover and installing the board to the carrier frame using two captive screws. The processors, power pods, memory board, DIMMs, and D2Ds on the primary side of the board are installed while the top cover is open. The top cover is then closed and latched and the module is turned over. The bottom cover is opened to install the processors, power pods, memory board, DIMMs, and D2Ds on the secondary side of the board.

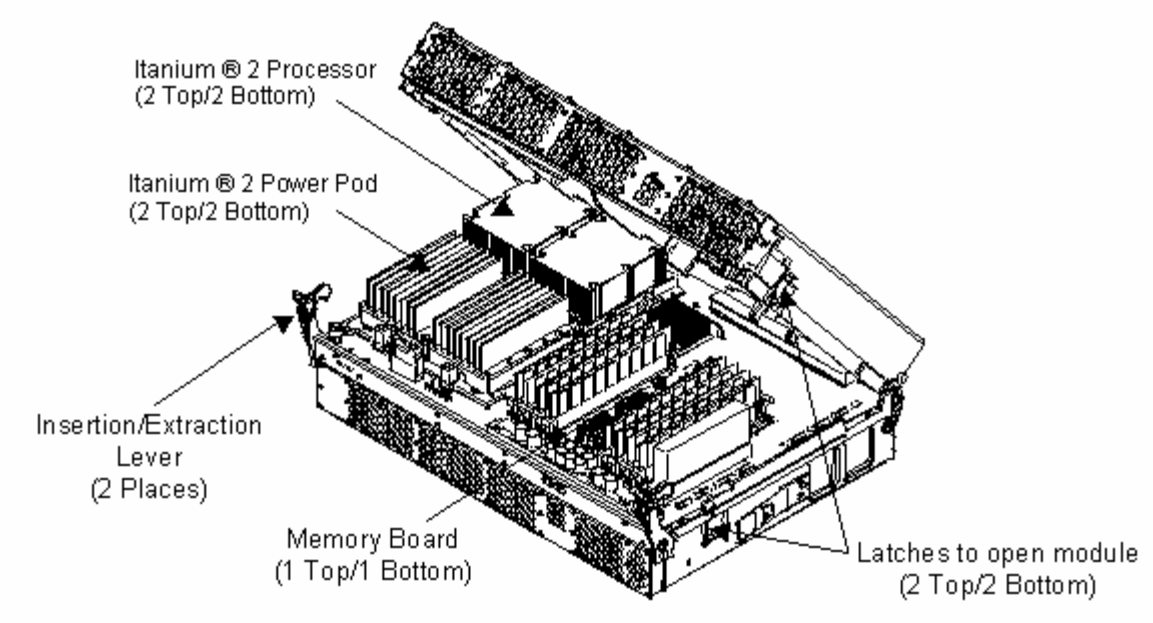


Figure 20. Processor/Memory Subsystem

The processor/memory module has been designed to meet three major requirements as described below.

3.4.1 Structural Support

The module provides structural support and protection for the processor and memory boards while mounted in the chassis and while installing components.

With the processor/memory subsystem weighing approximately 22 pounds (10 kilograms) when fully configured, it is necessary to provide significant structural support for the boards and components when mounted in the chassis and subjected to a shipping environment. This is achieved by mounting the processor and memory boards to the module frame and attaching structural foam covers, which clamp the boards in place under a compressive load. This method provides the structural support required to protect the boards during shock and vibration.

The processor/memory subsystem also provides protection for the boards and components when it is removed from the system and processors and DIMMs are being installed/replaced.

3.4.2 Airflow

The module provides proper airflow paths to cool the processors, power pods, chipset, DIMMs, D2Ds, and other components on the processor and memory boards.

Control of the airflow across the processors is critical to the thermal design of the system. The processor/memory subsystem provides distinct air channels for each processor/power pod heat sink, which seal to the system fans.

3.4.3 Serviceability

The module allows easy access to the processors, power pods, DIMMs, and D2Ds for upgrades and replacement of components.

Once the processor/memory subsystem is assembled, any replacements or upgrades can be easily performed by opening the top or bottom cover and accessing the desired component. Components on either side of the processor board can be accessed without removing any other components in the subsystem.

3.5 I/O Subsystem and Fan Bay

The I/O subsystem and fan bay assembly support the I/O baseboard, I/O riser card, and the four system fans. The fan bay is integrated into the I/O subsystem prior to inserting the assembly into the chassis.

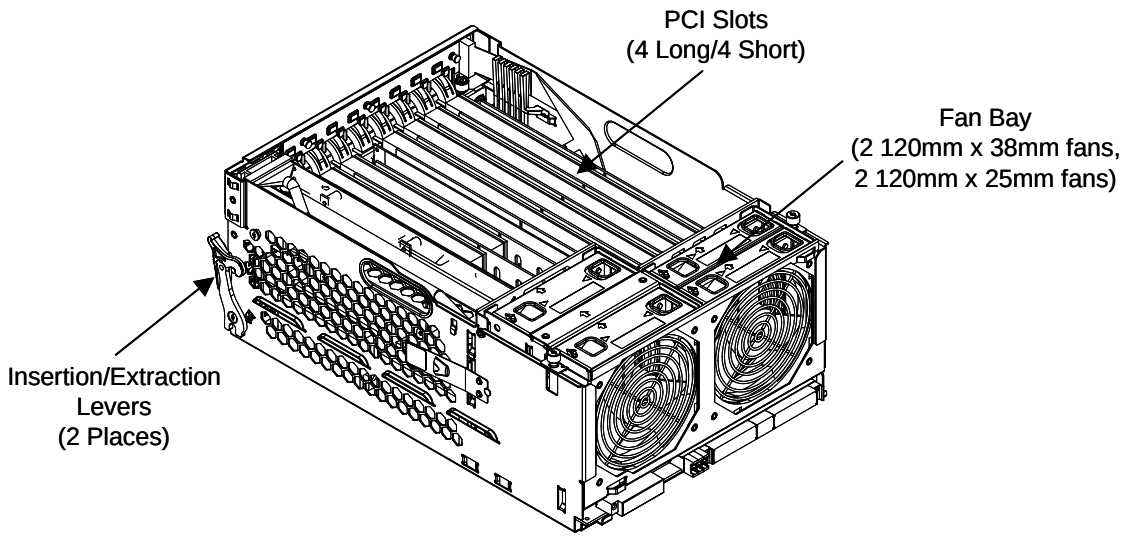


Figure 21. I/O Subsystem

3.5.1 I/O Subsystem

The I/O subsystem is assembled by mounting the I/O baseboard into the I/O sheet metal frame. This assembly utilizes hook features in the sheet metal frame that attach to slots in the I/O baseboard. Four captive screws on the I/O baseboard protective plastic cover are used to secure the board to the frame. The I/O baseboard supports four plug-in D2Ds, the I/O riser card, and eight PCI cards (four short/four long). A sheet metal bracket provides 240 VA protection to the D2D area of the board and also provides structural support to the I/O riser card and D2D's.

A SCSI cable (optional) plugs into the external SCSI connector on the I/O baseboard and is routed to the rear bulkhead. An ICMB board (optional) is mounted to a bracket that mounts to the I/O module with one captive screw and is cabled to the I/O baseboard.

3.5.2 Hot-plug PCI Mechanical Implementation

The mechanical implementation of the hot-plug PCI is achieved by using the following components:

- PCI HPIB
- MRL switch (also called a rocker mechanism)
- Plastic card guide/retention mechanism to secure the rear edge of each installed PCI card
- The 240 VA protective cover on the I/O baseboard and plastic dividers between the PCI slots

The HPIB is installed to the top rear of the I/O subsystem using four plastic rivets. The connection between the I/O baseboard and the HPIB is provided via a cable. A plastic cover over the surface of the I/O baseboard and plastic dividers between the PCI slots are provided to prevent shorting to the I/O baseboard or adjacent PCI cards during hot-swap operation.

The HPIB contains green (power) and amber (software/hardware fault/attention) LEDs, a Hall-effect switch actuated by the MRL switch, and an attention switch/push button. The HPIB is mounted in the chassis directly above the PCI cards. The LEDs can be seen from both inside and outside of the chassis. Each Hall-effect switch is installed on the HPIB so that it can be activated by the MRL as shown in Figure 22.

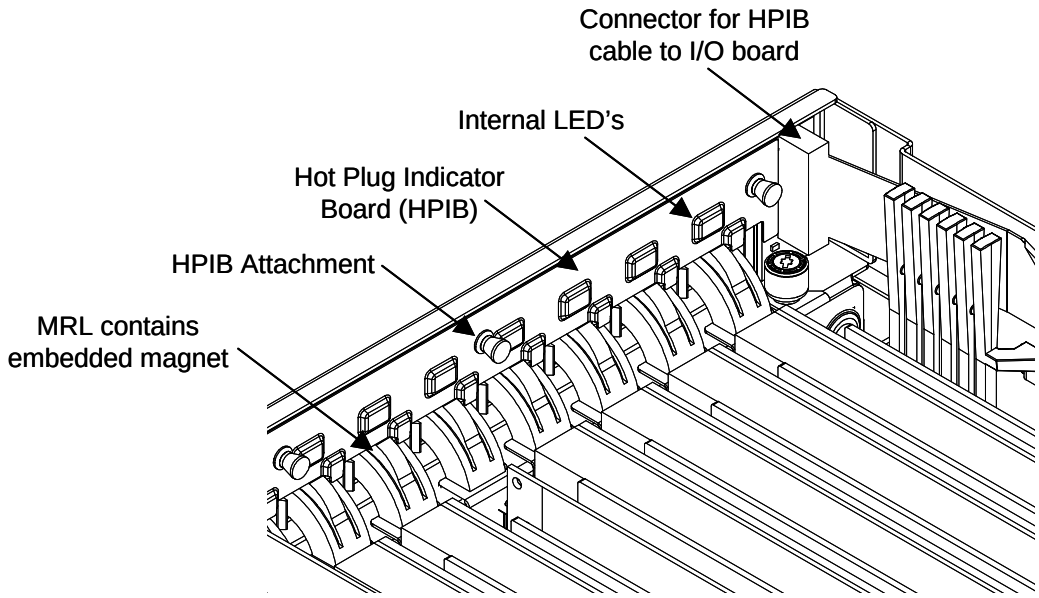


Figure 22. Hot-Plug PCI Rocker Mechanism

The MRL switch, in combination with the Hall-effect sensor, helps to activate the slot power switch as it enters the I/O subsystem. The rocker can only be released from within the chassis. This prevents unintentional power down of PCI slots when the system is powered up and the chassis has not yet been pulled out of the rack. The MRL also acts as a retention mechanism for the PCI card.

The opposite end of the PCI card is held in place by a plastic, snap-in locking card guide. The guide, installed on the center support bracket, has a built-in retention mechanism that secures the top-rear edge of a full-length PCI card.

3.5.3 Fan Bay

The fan bay houses four system fan Customer Replaceable Units (CRUs). Two 120 x 25-mm fans cool the memory boards in the processor/memory subsystem and cool the PCI slots in the I/O subsystem. Two 120 x 38-mm fans cool the processors and power pods in the processor/memory subsystem, and cool PCI slots and D2Ds in the I/O subsystem.

The fan bay attaches to the I/O subsystem prior to installing the I/O subsystem in the chassis. The fan CRUs plug directly into the connectors provided on the I/O baseboard.

3.5.4 Fan CRU

The system uses two different fan CRUs. Both are assembled using a standard fan that snaps into a molded plastic shell. The molded shell includes a color-coded plastic latch that indicates that the fan is hot-swappable. The assembly has an integrated amber LED wired to the top of the plastic shell that will turn on when the fan is not functioning within specifications. Standard wire finger guards are attached to both sides. The fan connector extends from the bottom bracket.

3.6 Peripheral Bay

The peripheral bay contains three 1-inch SCSI hard drives, one ½-inch DVD/CD drive, one ½-inch LS-240 drive and the SCSI backplane. The SCSI hard drives are hot-swappable. The DVD/CD and LS-240 drives dock in the bay, but are not hot-swappable. It is necessary to pull the peripheral bay partially out of the chassis to remove the DVD/CD and LS-240 devices. The peripheral bay is secured into the chassis by two insertion/extraction handles located on the sides of the bay.

The peripheral bay is a sheet metal enclosure with aluminum die-cast parts to guide the hard drives and molded plastic and sheet metal parts that hold the DVD/CD and LS-240 devices. The SCSI backplane board is installed through an opening in the bottom of the bay with three captive screws.

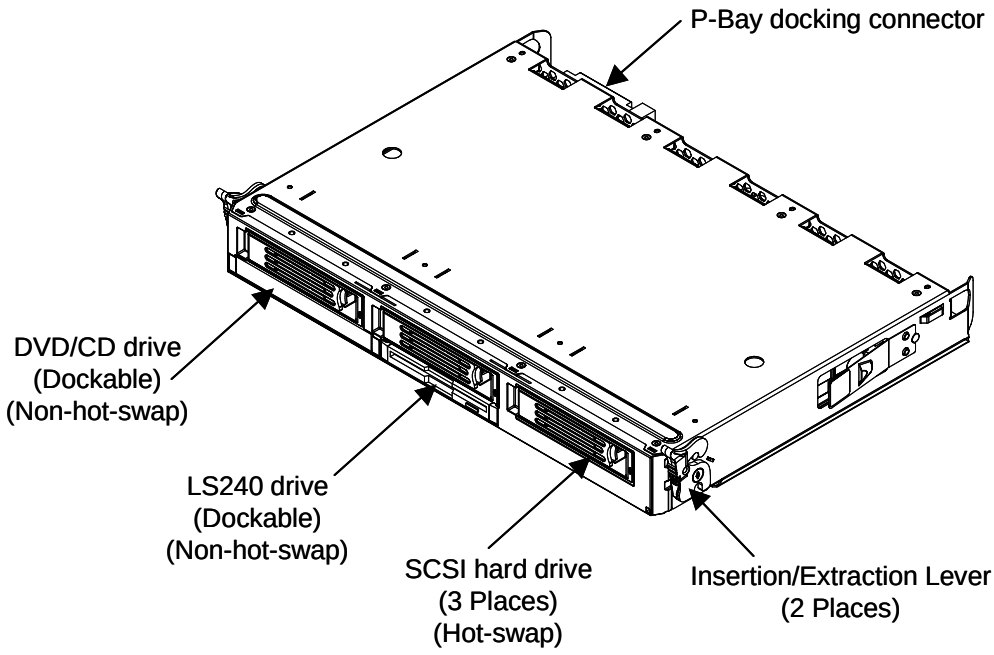


Figure 23. Peripheral Bay

3.6.1 Hard Drive Carrier

The hard drive carrier is a plastic assembly that provides guidance for hot-swapping. It contains an integrated light pipe to transfer the LED indicator light from the SCSI backplane to the front, and an insertion/extraction mechanism that includes a hard drive bezel, which can be customized.

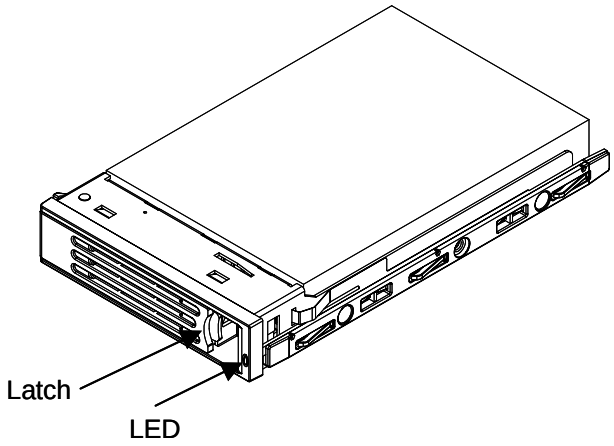


Figure 24. Hard Drive Carrier

3.6.2 DVD and LS-240 Carriers

Each DVD and LS-240 device is mounted to a plastic carrier with a sheet metal cover, along with an adapter board. These carriers allow the devices to be docked into the peripheral bay. An ejector button, located on the back edge of the carrier, allows easy removal once the peripheral bay is partially removed from the chassis.

Note: The DVD/CD and LS-240 devices dock into the peripheral bay, but are not hot-swappable.

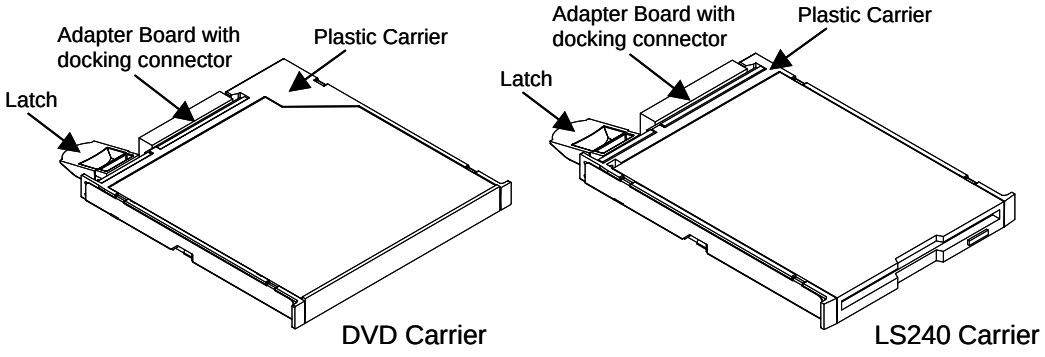


Figure 25. DVD Drive Carrier and LS-240 Drive Carrier

3.7 Front Panel Assembly

The front panel assembly consists of the front panel board and a sheet metal bracket on the front edge. The assembly docks into a card edge connector on the midplane board.

The switches and LED indicators on the front panel are described in Chapter 2.

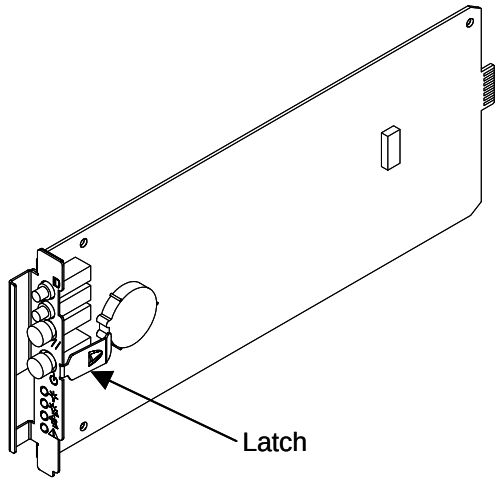


Figure 26. Front Panel Assembly

3.8 Top Cover

The chassis top cover is designed in two sections described below.

3.8.1 Front Section

The front section covers the processor/memory area and extends to the midplane support. The front section only needs to be removed to install/remove the midplane board. It does not need to be removed for any other service requirements. It is held in place with two captive screws.

3.8.2 Rear Section

The rear section of the top cover is designed to allow easy access to hot-swap fans and hot-plug PCI cards. The cover is attached with two rails that allow it to slide toward the rear of the chassis into the space in the rack that the chassis occupied. The cover includes two color-coded release buttons that lock it in the closed position.

The rear section is opened partially to access the hot-swap fans. It is extended fully to access the hot-plug PCI cards.

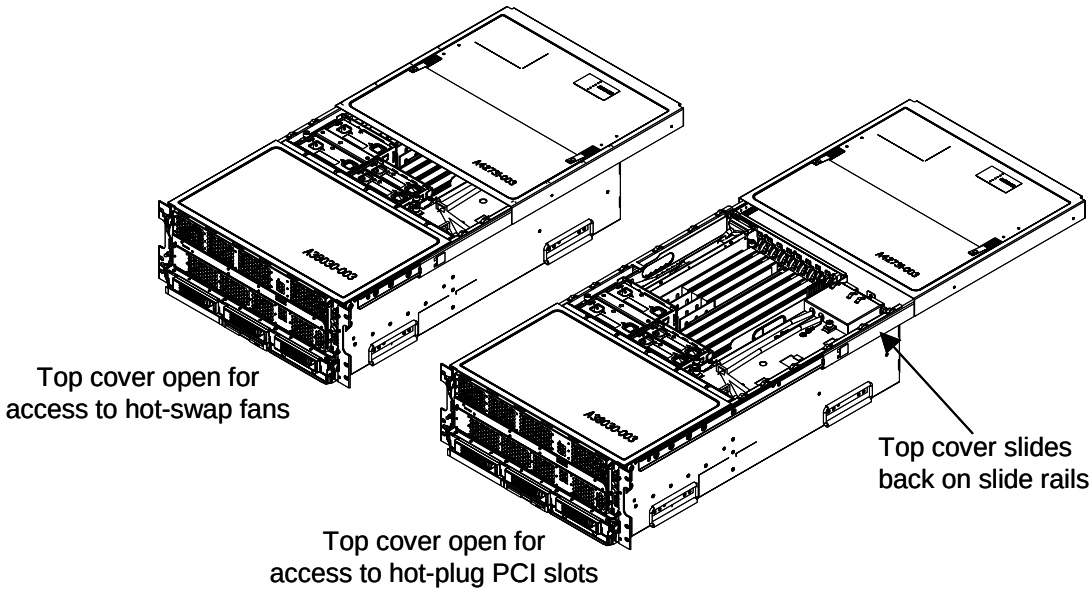


Figure 27. Top Covers

3.9 Front Bezel

The front bezel assembly is designed in two pieces.

A semi-permanent cover over the peripheral bay allows access through the bezel to the SCSI hard drives and the DVD/LS-240 drives. It can be removed, but does not need to be with normal server use. It hooks into features at the bottom of the P-Bay and has plastic snap features at the top edge.

The upper louver section of the bezel covers the front of the processor/memory module and the front panel. It also extends down over the P-Bay insertion/extraction levers. It has buttons and light pipes that interface with the front panel switches and LEDs. The upper louver section can be easily removed to access the processor/memory module, the peripheral bay insertion/extraction handles, and the front panel board.

Figure 28. Front Bezel

4. Cables and Connectors

This chapter describes interconnections between the various components of the SR870BN4 server system. Also, this chapter includes an overview diagram of the SR870BN4 server system interconnections, as well as tables describing the signals and pin-outs for the user accessible connectors. Refer to the *S870BN4 Board Set Technical Product Specification* for all other connector signal descriptions and pin-outs. This chapter is organized into the following sections:

Section 4.1: Interconnect Block Diagram
Provides an overview of system interconnects.

Section 4.2: Cable and System Interconnect Descriptions
Provides a list of all the connectors and cables in the system.

Section 4.3: User-Accessible Interconnects
Describes the form-factor and pin-out of user-accessible interconnects.

4.1 Interconnect Block Diagram

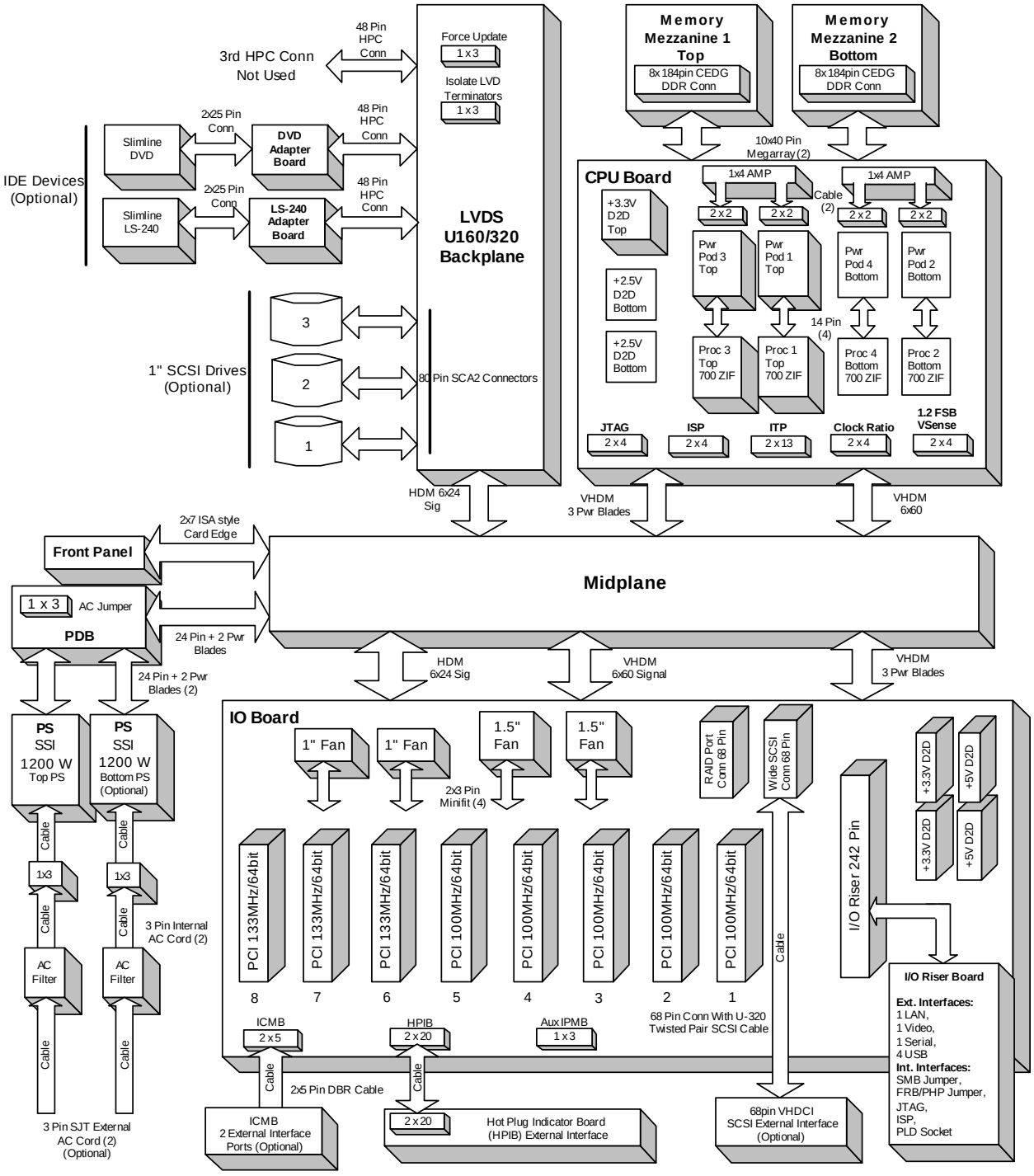


Figure 29. Intel® Server System SR870BN4 Interconnect Block Diagram

4.2 Cable and Interconnect Descriptions

The following table describes all cables and connectors of the SR870BN4 server system.

Table 12. Cable and Connector Descriptions

Type	Qty	From	To	Interconnect Description
Serial	1	I/O riser	External interface	9-pin serial port
USB	4	I/O riser	External interface	1x4 pin USB cables
Ethernet	1	I/O riser	External interface	RJ45 connector port
Video	1	I/O riser	External interface	15-pin, monitor device
I/O Riser Connector	1	I/O baseboard	I/O riser	Slot 1, 242—pin card edge connector
External Wide Ultra 320 SCSI, Port 2	1	I/O baseboard	External interface	68-pin solid core twisted pair round cable to panel mounted external interface connector
ICMB internal	1	I/O baseboard	ICMB board	2x5 pin ribbon cable
ICMB external	2	ICMB board	External interface	6-pin SEMCONN* connector to shielded ICMB cable
HPIB	1	I/O baseboard	HPIB board	2x20 flat ribbon cable
AC Distribution (Filter Side)	2	Power cord	Power supply cage	3-pin PVC double insulated power cordage (15-A AC filter on one side and 15A IEC320 Plug on Power Supply End)
AC Power	2	AC distribution (filter side)	External interface	Recommend 3-pin SJT power cord with IEC320-13 Receptacle
DC main power	2	Power supply	Power Distribution Board (PDB) board	4x6 pin signal + two blade SSI blind mate connector
DC main power	1	PDB board	Midplane	4x6 pin signal + two power blade SSI blind mate connector
AC Range Jumper	1	PDB board	Jumper	1x3 header
Server Management Bus (SMB) Jumper	1	I/O riser	Internal interface	1x5 header
FRB/PHP Jumper	1	I/O riser	Jumper	1x5 header
VHDM (I/O Baseboard)	1	I/O baseboard	Midplane	6x60 signal pins + three power blades
VHDM (Processor board)	1	Processor board	Midplane	6x60 signal pins + three power blades
HDM (SCSI backplane)	1	I/O baseboard	SCSI backplane	6x24 signal pins (**Note:** SCSI backplane side has four HDM power blades to midplane only)
+5-V D2D (I/O baseboard)	2	I/O baseboard	+5-V D2D	2x35 ISA card edge connector (keyed for 5 V)
+3.3-V D2D (I/O baseboard)	2	I/O baseboard	VID D2D	2x35 ISA card edge connector (keyed for VID)
64-bit PCI-X connector	8	I/O baseboard	PCI adapter card	188-pin PCI card edge connector

Type	Qty	From	To	Interconnect Description
System Fan	4	I/O baseboard	Fan module	2x3 Minifit Jr* blind mate connector
ITP	1	I/O baseboard	Internal interface	2x13 header
Aux IPMB	1	I/O baseboard	Internal interface	1x3 header
Front panel	1	Midplane	Front panel board	2x7 ISA card edge connector
Processor Signals	4	Processor	Processor board	700-pin Intel® Itanium® 2 Zero Insertion Force (ZIF) socket
Processor Power	4	Processor Power Pod	Processor	14-pin card edge connector
Processor Power Pod	2	Processor board	Processor Power Pod	Discrete cable (1x4 Mate-N-Lok on processor board and 1x4 Minifit Jr to processor power pod)
1.2 FSB VSENSE	1	Processor board	Internal interface	2x4 header
+3.3-V D2D (Processor board)	1	Processor board	VID D2D	2x35 ISA card edge connector (keyed for VID)
+2.5-V D2D (Processor board)	2	Processor board	VID D2D	2x35 ISA card edge connector (keyed for VID)
Clock Ratio	1	Processor board	Jumper	2x4 header
Memory Board Connector	2	Processor board	Memory board	400-pin MegArray* connector
Memory	16	Memory board	DDR memory	184-pin card edge connector
SCA-2 Hard Disk Drive (HDD) connectors	3	SCSI backplane	1-inch SCSI HDD	80-pin SCA-2 connector
Force update	1	SCSI backplane	Jumper	1x3 header
Isolate LVD terminators	1	SCSI backplane	Jumper	1x3 header
½-inch IDE adapter	3	SCSI backplane	½-inch DVD adapter or ½-inch LS-240 adapter	(NOTE: SCSI backplane has three connectors but only two are used in the SR870BN4 system)
½-inch DVD device	1	½-inch DVD adapter	½-inch DVD (or RW-CD) device	2x25 pin JAE* connector
½-inch LS-240 device	1	½-inch LS-240 adapter	½-inch LS-240 device	2x25 pin JAE connector

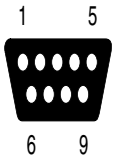
4.3 User-Accessible Interconnects

4.3.1 Serial Port

The I/O riser card provides one RS-232C serial port. The COM port connector is double stacked with a video port. The video connector is closest to the I/O riser printed board. The COM port uses D-subminiature 9-pin connectors.

The COM serial port can be used either as an EMP or as a normal serial port. As an EMP, COM is used as a communication path by the server management RS-232 connection to the Sahalee. This provides a level of emergency management through an external modem. The RS-232 connection can be monitored by the Sahalee when the system is in a powered down (standby) state. Additional information can be found in the *Emergency Management Port Interface External Product Summary*.

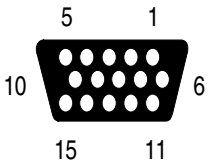
Table 13. COM Serial Connector Pin-out

Pin	Signal	COM Serial Connector
1	DCD_L (carrier detect)	
2	RXD (receive data)	
3	TXD (transmit data)	
4	DTR_L (data terminal ready)	
5	GND (ground)	
6	DSR_L (data set ready)	
7	RTS_L (request to send)	
8	CTS _L (clear to send)	
9	RI_L (ring indicator)	

4.3.2 Video Port

The I/O riser card provides a video port interface with a standard VGA-compatible, 15-pin connector. Onboard video is supplied by an ATI* Rage XL video controller with 4 MB of onboard video SDRAM.

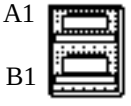
Table 14. Video Connector Pin-out

Pin	Signal	Video Connector
1	VID_R (analog color signal red)	
2	VID_G (analog color signal green)	
3	VID_B (analog color signal blue)	
4	No connection	
5	GND	
6	GND	
7	GND	
8	GND	
9	No connection	
10	GND	
11	No connection	
12	MONID1 (to support DDCx, " Display Data Channel ™ Standard)	
13	VID_HSYNC (horizontal sync)	
14	VID_VSYNC (vertical sync)	

4.3.3 Universal Serial Bus (USB) Interface

The I/O riser card provides two sets of double-stacked USB ports. USB Port 1 and Port 2 are the first double stack connector (Port 1 is closest to the I/O riser printed board). USB Port 3 and Port 4 are part of a larger connector, which houses the 82250 GY NIC port (Port 4 is closest to the I/O riser printed board). These built-in USB ports permit the direct connection of four USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports.

Table 15. Dual USB Connector Pin-out

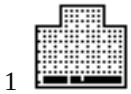
Pin	Signal	Dual USB Connector
A1	Fused Voltage Controlled Current (VCC) (+5 V /w overcurrent monitor of both port 1 and 2)	
A2	USBPxM (differential data line)	
A3	USBPxP (differential data line)	
A4	GND (ground)	
B1	Fused VCC (+5 V /w overcurrent monitor of both port 1 and 2)	
B2	USBPxM (differential data line)	
B3	USBPxP (differential data line)	
B4	GND (ground)	

Note: 'x' indicates port in question.

4.3.4 ICMB Connectors

The ICMB provides external access to Intelligent Management Bus (IMB) devices that are within the chassis. This makes it possible to externally access chassis management functions, alert logs, post-mortem data, etc. It also provides a mechanism for chassis power control. As an option, the server can be configured with an ICMB adapter board to provide two SEMCONN 6-pin connectors to allow daisy-chained cabling. The ICMB connectors support the connector ID feature. Additional information about the ICMB can be found in the *External Intelligent Management Bus Bridge External Program Specification,* Version 1.0 and in the *S870BN4 Board Set External Product Specification*.

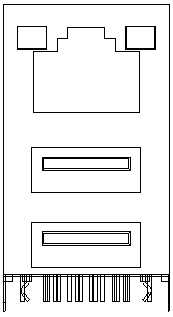
Table 16. ICMB Connector Pin-out

Pin	Signal	ICMB Connector
1	GND (ground)	
2	No connection	
3	Tx/Rx+ (differential data line)	
4	Tx/Rx- (differential data line)	
5	Conn ID+ (differential connector ID line)	
6	Conn ID- (differential connector ID line)	

4.3.5 Ethernet Connector

The I/O riser card provides one 10/100/1000 Ethernet port with a RJ45 network connector. The Ethernet port is controlled by the Intel® E82540 chipset component. The Ethernet connector is part of a larger connector housing two USB ports (the Ethernet connector is furthest away from the I/O riser printed board).

Table 17. Ethernet Connector Pin-out

Pin	Signal	Ethernet Connector
9	TDP (differential transfer data)	
10	TDN (differential transfer data)	
11	RDP (differential receive data)	
12	NIC termination	
13	NIC termination	
14	RDN (differential receive data)	
15	NIC termination	
16	NIC termination	
17	ACTLED (activity LED signal)	
18	LILED (link LED signal)	
19	+3.3-V standby (for LED)	
20	SPEEDLED (Speed LED signal)	

4.3.6 Ultra320 SCA-2 HDD Connector

The SCSI backplane board provides three SCA-2 connectors for hot-swapping Ultra320 hard drives. These SCSI ports are controlled by SCSI port 1 of the LSI* 53C1030 chipset component located on the I/O baseboard. The connector pin assignment is for the current draft *Small Form Factor-8046,* Revision 1.1 document.

Table 18. SCA-2 Connector Pin-out

80-pin Connector Contact and Signal Name		80-pin Connector Contact and Signal Name	
1	12-V Charge	12-V Ground	41
2	12-V Charge	12-V Ground	42
3	12-V Charge	12-V Ground	43
4	12-V Charge	Mated 1	44
5	Reserved/ESI-1	-EFW	45
6	Reserved/ESI-2	DIFFSNS	46
7	-DB(11)	+DB(11)	47
8	-DB(10)	+DB(10)	48
9	-DB(9)	+DB(9)	49
10	-DB(8)	+DB(8)	50
11	-I/O	+I/O	51
12	-REQ	+REQ	52
13	-C/D	+C/D	53
14	-SEL	+SEL	54
15	-MSG	+MSG	55
16	-RST	+RST	56
17	-ACK	+ACK	57
18	-BSY	+BSY	58
19	-ATN	+ATN	59
20	-P_CRCA	+P_CRCA	60
21	-DB(7)	+DB(7)	61
22	-DB(6)	+DB(6)	62
23	-DB(5)	+DB(5)	63
24	-DB(4)	+DB(4)	64
25	-DB(3)	+DB(3)	65
26	-DB(2)	+DB(2)	66
27	-DB(1)	+DB(1)	67
28	-DB(0)	+DB(0)	68
29	-DB(P1)	+DB(P1)	69
30	-DB(15)	+DB(15)	70
31	-DB(14)	+DB(14)	71
32	-DB(13)	+DB(13)	72
33	-DB(12)	+DB(12)	73
34	5-V Charge	Mated 2	74
35	5-V Charge	5-V Ground	75
36	5-V Charge	5-V Ground	76

80-pin Connector Contact and Signal Name		80-pin Connector Contact and Signal Name	
37	Spindle Sync	Active LED Out	77
38	MTRON	DLYD_START	78
39	SCSI ID (0)	SCSI ID (1)	79
40	SCSI ID (2)	SCSI ID (3)	80

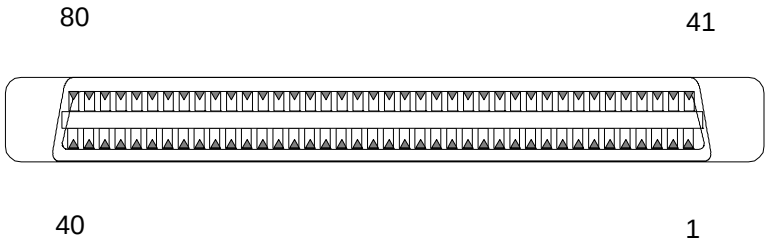


Figure 30. SCA-2 Connector

4.3.7 External Ultra 320 SCSI Connector

As an option, the server system can support a shielded external SCSI connection. This SCSI port is controlled by SCSI port 2 of the LSI* 53C1030 chipset component located on the I/O baseboard. To implement this feature, a twisted pair SCSI cable is first panel mounted to the D2D shield part of the chassis. Then, the other end is plugged into the corresponding connector down on the I/O baseboard.

Note: Only service personnel should access the D2D shield.

Table 19. Ultra 320 SCSI Connector Pin-out

Signal Name	Pin	Pin	Signal Name
+DB(12)	1	35	-DB(12)
+DB(13)	2	36	-DB(13)
+DB(14)	3	37	-DB(14)
+DB(15)	4	38	-DB(15)
+DB(P1)	5	39	-DB(P1)
+DB(0)	6	40	-DB(0)
+DB(1)	7	41	-DB(1)
+DB(2)	8	42	-DB(2)
+DB(3)	9	43	-DB(3)
+DB(4)	10	44	-DB(4)
+DB(5)	11	45	-DB(5)
+DB(6)	12	46	-DB(6)
+DB(7)	13	47	-DB(7)
+P_CRCA	14	48	+P_CRCA
GND	15	49	GND
DIFFSENS	16	50	GND

Signal Name	Pin	Pin	Signal Name
TERMPWR	17	51	TERMPWR
TERMPWR	18	52	TERMPWR
NC	19	53	NC
GND	20	54	GND
+ATN	21	55	-ATN
GND	22	56	GND
+BSY	23	57	-BSY
+ACK	24	58	-ACK
+RST	25	59	-RST
+MSG	26	60	-MSG
+SEL	27	61	-SEL
+C/D	28	62	-C/D
+REQ	29	63	-REQ
+I/O	30	64	-I/O
+DB(8)	31	65	-DB(8)
+DB(9)	32	66	-DB(9)
+DB(10)	33	67	-DB(10)
+DB(11)	34	68	-DB(11)

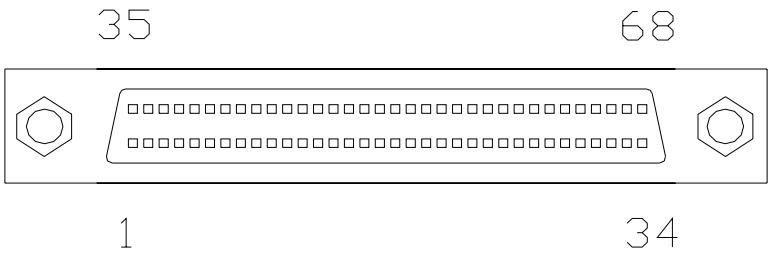


Figure 31. Ultra 320 SCSI Connector

4.3.8 AC Power Input

Two IEC320-C14 15A receptacles are provided at the rear of the server. It is recommended to use an appropriately-sized power cord and AC main. Refer to the power section of this document for system voltage, frequency, and current draw specifications. The bail lock external AC cord retention feature is built into the AC power input can. Bail lock wire is not supplied with the system.

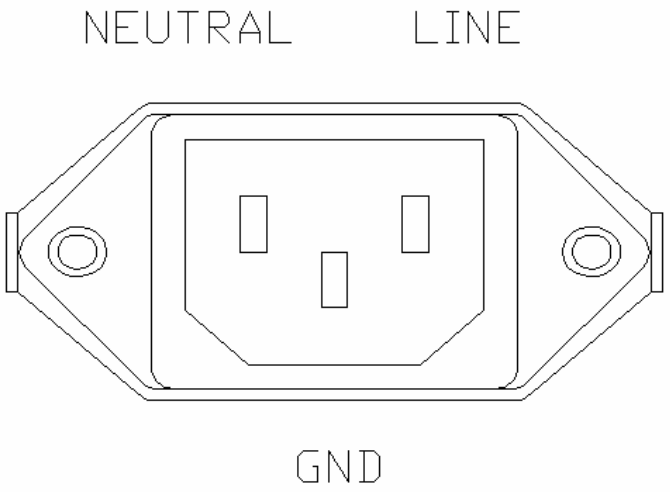


Figure 32. AC Power Input Connector

5. Power Subsystem

This chapter describes the requirements for a SSI-compliant, universal AC input with Power Factor Correction (PFC), Distributed Power Supply (DPS) 1200-W power supply.

The power supply is designed to work in parallel to form a N+1 hot-swap redundant power system, where N = 1 thru 5. In the SR870BN4, N=1. The power supply has two DC outputs: main 48 V and 12-V (standby). In an N+1 configuration, the 48-V outputs have active (forced) current sharing, and 12-VSB outputs have passive current sharing.

The AC input and DC output connectors are located on the end of the supply opposite the side where the handle is located. These connectors make contact with the system or power bay when the power supply is inserted. Each power supply contains its own cooling fan(s). The power supply has a dual rating of 1200 W maximum over an input range of 180-264 VAC, and 700 W minimum over an input range of 90-132 VAC.

The two externally enabled outputs have the following ratings:

- +48 Vdc at: 24.0 A @HI line /13.5 A @LO line
- +12 VdcSB at 4 A @any line

5.1.1 Fan Requirements

The power supply incorporates two 60-mm fans for self-cooling. The air comes in from the connector side, passes through the power supply, and exhausts on the fan side of the power supply.

The FANP signal is an input power pin to the power supply. It is used to provide power to the power supply fan in the case of a power supply failure or loss of AC power to the power supply. A failure inside the power supply shall not cause any disturbance on the power connected to FANP. The fan inside the power supply shall turn off if the power supply is disabled with the PSON# signal. The FANC signal shall still be able to control the fan speed when the power supply fan is being powered from FANP.

Table 20. FANC Signal Characteristics

Signal Type	Accepts input power from the system to operate the power supply fan when supply has failed or loss of AC.
FANP = 11.4 V to 13.0 V PSON# = Low Power Supply = ON	Fan(s) operating. No current draw from FANP. Fan powered internally.
FANP = 11.4 V to 13.0 V PSON# = High Power Supply = OFF or Failed or No AC	Fan(s) not operating. No current draw from FANP.
FANP = 11.4 V to 13.0 V PSON# = Low Power Supply = Failed or No AC	Fan(s) operating. Powered from FANP.

FANP = Open PSON# = Low Power Supply = ON	Fan(s) operating. Fan powered internally.	
FANP = Open PSON# = High Power Supply = OFF or Failed or No AC	Fan(s) not operating.	
FANP = Open PSON# = Low Power Supply = Failed or No AC	Fan(s) not operating.	
	Minimum	**Maximum**
FANP Voltage	11.4 V	13.0 V
FANP Peak Sink current; @ Power On, FANP = 12.5 V (600 msec max duration)		1.0 A
FANP Continuous Sink current; FANP = 12.5 V		600 mA

5.2 Interface Requirements

5.2.1 AC Inlet Connector

The power supply has a standard IEC inlet connector.

5.2.2 DC Output Connector(s)

DC power and control signals are interfaced to the system distribution and control subsystem via connectors, which dock with mating connectors when the power supply is inserted into the system Power Distribution Board (PDB).

The power supply must have a main 48-VDC output and a low current 12-VSB output. The 12-VSB output is always available when AC input power is applied to the power supply (with the exception of a fault condition that has opened the AC line fuse[s]). 12 VSB is used to power system components (i.e., server management) that must be available when the system is powered down.

5.3 Marking and Identification

The power supply marking must support the following requirements: safety agency requirements, government requirements (if required [e.g., point of manufacturing]), power supply vendor requirements, and Intel® manufacturing and field support requirements.

5.3.1 LED Labeling

The Power LED (green), the Predictive Failure LED (amber), and the Power Supply Failure LED (amber) are marked or labeled near the LED's with the following markings:

Power: **Predictive Failure:** **Fail:**



The LEDs are visible from the rear of the chassis when the power supply is installed in the system chassis. LEDs are located to meet all Electro Static Discharge (ESD) requirements.

5.4 Internal System Marking

The power supply is marked to support the safety agency requirements, government requirements (if required [e.g., point of manufacturing]), power supply vendor requirements, and Intel manufacturing and field support requirements. This marking is applied on an external surface of the power supply and is not to be visible from the exterior of the server system.

The power supply is marked with the international label to indicate that no user-serviceable parts are contained in the power supply. This label is shown in Figure 33. This label is printed on bright yellow vinyl label stock with black symbols.

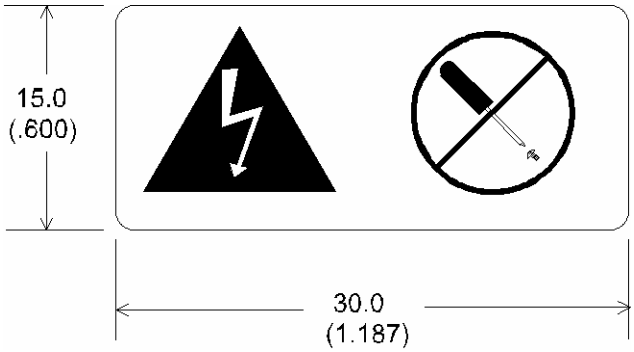


Figure 33. Service Label

Note: The temperature of the power supply chassis cannot exceed 70 C under all circumstances; otherwise, a UL international HOT SURFACE label must be added. This HOT SURFACE label, if required, will be placed in such a way that when the power supply is extracted from the system, the label will be visible before the operator has a chance to touch the hot surface of the power supply.

5.5 Electrical Requirements

5.5.1 Efficiency

The power supply has a minimum efficiency of 80% to its DC output pins at maximum load currents and at rated nominal input voltages and frequencies. The power supply has a minimum efficiency of 85% to its DC output pins at maximum load currents when the input voltage is higher than 180 Vac.

5.5.2 AC Input Voltage Specification

5.5.2.1 AC Input Voltage Ranges

The nominal input voltage ranges specified in AC volts rms are 100-120 and 200-240 Vac. The power supply incorporates a universal power input with active power factor correction, which reduces line harmonics in accordance with EN61000-3-2 and JEIDA MITI standards. The ratings are marked on the supply labels as referenced in Table 21 and Section 5.4: Internal System Marking.

Table 21. Input Voltage Requirements

Parameter	Minimum	Nominal	Maximum	Units
Vin (115)	90	100-120	132	Vrms
Vin (230)	180	200-240	264	Vrms
Vin Frequency	47	50/60	63	Hz
Input Current 220 Vac range	4	[5]	6	Amps

5.5.2.2 AC Line Dropout

AC line dropout condition is a transient condition defined when the line voltage input to the power supply drops to 0 volts. AC line dropout will not damage the power supply under any load conditions. While operating at full load, an AC line dropout condition, with a period equivalent to a complete cycle of AC input power frequency (i.e., 20 milliseconds at 50 Hz) or less, will not cause any out of regulation conditions, such as overshoot or undershoot, nor will it cause any nuisance trips of any of the power supply protection circuits.

5.5.2.3 AC Line Fuse

Both the LINE and NEUTRAL AC inputs are fused. AC line fusing is compliant with all safety agency requirements. AC inrush current will not cause the AC line fuses to blow under any conditions. Protection circuits in the power supply will not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions. The DC load short circuit protection circuits will shut down or limit power supply without causing the AC line fuse to blow.

5.5.2.4 Power Factor Correction

The power supply incorporates a power factor correction circuit.

The power supply is tested as described in *EN 61000-3-2: Electromagnetic Compatibility (EMC) Part 3: Limits- Section 2: Limits for Harmonic Current Emissions*, and must meet the harmonic current emissions limits specified for ITE equipment.

The power supply is tested as described in *JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment* and must meet the harmonic current emissions limits specified for ITE equipment.

5.5.3 DC Output Specification

The power supply DC output specification is met by a single supply or by two supplies, operating with their outputs directly paralleled. When operated in parallel, the supplies share the total load currents equally within the limits specified, and meet all performance requirements of individual supplies. Failure of a supply in a paralleled group, or removal of an operational or failed supply from a paralleled group will not cause DC output transients in excess of the limits specified. Adding an operational or failed supply to a paralleled group will not cause DC output transients in excess of the limits specified.

Table 22. DC Output Voltage Limits (Regulation)

Output	Minimum	Nominal	Maximum	Units	% Reg
48 VDC	+45.6	+48.0	+50.4	Volts	± 5%
12 VSB	+12.0	+12.5	+13.00	Volts	± 4%

5.5.3.1 DC Output Rating

The 48-VDC and 12-VSB outputs must meet ALL requirements over the loading and AC input conditions as shown in Table 23.

Table 23. DC Output Rating

Output	Minimum Load (Amps)	Maximum Load (Amps)	Input AC Voltage
48 VDC	1.0	24.0	180 - 264 VAC
12 VSB	0	4.0	
48 VDC	1.0	13.5	90 - 132 VAC
12 VSB	0	4.0	

The 48-VDC output shall have a peak output capacity of **15.0 A at Low Line and 26.0 A at High Line** for a maximum duration of **10 seconds**.

5.5.3.2 Remote Sense

The power supply has two outputs: +48 V and +12 VSB, both with no remote sensing.

5.5.3.3 Ripple and Noise

Ripple and noise are defined as periodic or random signals over the frequency band of 10 Hz to 20 MHz. The power supply DC output ripple and noise will not exceed the values shown in Table 24.

Table 24. Ripple and Noise

Output	48 VDC	12 VSB
Maximum Ripple and Noise pk-pk	480 mVp-p =1%	120 mVp-p =1%

5.5.3.4 Over-Voltage Protection

The power supply's over-voltage protection shall be locally sensed. The power supply shall shut down in a latch-off mode after an over voltage condition on 48-V output and/or 12-VSB output. This latch-on 48-V output can be cleared by toggling the PSON# signal or by an AC power interruption; the latch-on 12-VSB output can be cleared by an AC power interruption. The following table contains the over voltage limits. The values are measured at the output of the power supply DC connector.

Table 25. Over-Voltage Protection Requirements

Output	Maximum OVP Limit
48 VDC	55.0 V
12.5 VSB	15.0 V

5.5.3.5 Over-Current Protection

The power supply has a current limit to prevent the 48-VDC output from exceeding the value shown in Table 26. The current limiting shall be of the constant current type for both the 48-VDC and 12-VSB outputs.

The over current limit level for the 48-VDC output shall be maintained for a period of 2,600 msec minimum and 3,600 msec maximum. For loads greater than 600% of maximum rating on the 48-VDC output, the power supply may shutdown in less than 2,600 msec.

The over current limit for the 12-VSB output shall be maintained indefinitely, without shutting down the power supply, as long as the 12-VSB output is within regulation limits. If the 12-VSB output is below regulation limits due to current limit, the over current limit state shall be maintained for a period of 1,500 msec minimum and 2,500 msec maximum. For loads greater than 600% of maximum rating on the 12-VSB output, the power supply may shut down in less than 1,500 msec.

After this current limit time for the 48-VDC and 12-VSB outputs, the power supply shall latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition.

Table 26. Over Current Protection

Voltage	Over-current Limit (Iout limit)
48 VDC	110% minimum; 150% maximum
12 VSB	100% minimum; 125% maximum

5.5.3.6 Short Circuit Protection

The power supply will not be damaged by application of a short circuit to any DC output. Short circuits will not turn into the over-current protection process described in Section 5.5.3.5. A hard short circuit should turn off the power supply immediately. A hard short circuit is defined as when the load level is less than 10 milliohms.

5.5.3.7 48-V Load Share Requirements

The 48-VDC output shall have forced load sharing. The output must share within 6.7% at full load, as shown in the following example. All current sharing functions are implemented internal to the power supply by making use of the 48-LS signal. The system connects the 48-LS signals between the power supplies. The supplies must be able to load share with up to two power supplies in parallel, and operate in a hot-swap/redundant n+1 configuration where n=2.

Example: Power supply #1 = 15.0 A
Power supply #2 > 14.0 A and < 16.0 A

5.5.3.8 12-VSB Load Share Requirements

The 12-VSB output must be able to provide 4.0 A of output current for each additional power supply added in parallel. Each power supply in the system will deliver current up to the current limit point. At this point, the power supply will go into constant current mode and allow other power supplies in the system to deliver additional standby current.

Table 27. Standby Load Sharing

Number of Supplies in Parallel	12 VSB Load
1	4.0 A
2	8.0 A
3 or 4	12.0 A

5.6 Power Supply Control Signals

5.6.1 PSON# (Power Supply Enable *input*)

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the 48-VDC power rail. When this signal is not pulled low by the system, or left open, the 48-VDC output turns off. The 12-VSB output remains on. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply.

Table 28. PS-ON Signal Characteristic

Signal Type	Accepts an open collector/drain output from the system. Pull-up to VSB located in power supply.	
PSON# = Low, PSKILL = Low	ON	
PSON# = Open, PSKILL = Low or Open	OFF	
PSON# = Low, PSKILL = Open	OFF	
	Minimum	**Maximum**
Logic level low (power supply ON)	0 V	1.0 V
Logic level high (power supply OFF)	2.0 V	5.25 V
Source current, Vpson = low		4 mA
Power up delay: $T_{pson\_on\_delay}$	5 msec	400 msec
PWOK delay: T_{pson_pwok}		50 msec

5.6.2 PSKILL *input*

The purpose of the PSKill pin is to allow for hot-swapping of the power supply. The PSKill pin on the power supply is shorter than the other signal pins. When a power supply is operating in parallel with other power supplies and then extracted from the system, the PSKill pin will quickly turn off the power supply and prevent arcing of the DC output contacts. The DC output contacts must not arc under this condition. T_{PSKill} (shown in Table 29) is the minimum time delay from the PSKill pin un-mating to when the power pins un-mate. The power supply must discharge its output inductor within this time from the un-mating of the PSKill pin. When the PSKill signal is not pulled down or left opened (power supply is extracting from the system), the power supply should shutdown regardless of the condition of the PSON# signal. The mating pin of this signal in the system should be tied to ground. Internal to the power supply, the PSKill pin should be connected to a standby voltage through a pull-up resistor. Upon receiving a LOW state at the PSKill pin, the power supply will be allowed to turn on via the PSON# signal. A logic LOW on this pin by itself should not turn on the power outputs.

Table 29. PSKILL Signal Characteristics

Signal Type (Input Signal to Supply)	Accepts a ground output from the system. Pull-up to VSB located in the power supply.	
PSKILL = Low, PSON# = Low	ON	
PSKILL = Open, PSON# = Low or Open	OFF	
PSKILL = Low, PSON# = Open	OFF	
	Minimum	**Maximum**
Logic level low (power supply ON)	0 V	1.0 V
Logic level high (power supply OFF)	2.0 V	5.25 V
Source current, Vpskill = low		4 mA
Delay from PSKILL=High to power supply turned off (T_{PSKill})[1]		0 sec

Note: T_{PSKill} is the time from the PSKill signal de-asserting HIGH to the power supply's output inductor discharging.

5.6.3 AC Input Range Setting (ACRANGE *input*)

ACRange allows the power supply to meet the AC Brownout requirement over the 200-240 VAC input voltage range. Refer to Table 21. It communicates the AC input voltage range the power supply is operating at by setting the trip point for the ACOK# signal. If the signal is open, the power supply defaults to the 100-240 VAC input range. If the signal is pulled low, the range is set to 200-240 VAC.

Table 30. ACRange Signal Characteristic

Signal Type	Accepts an open collector/drain output from the system. Pull-up to VSB located in power supply.	
ACRange = Low	200-240 VAC	
ACRange = Open (Default)	100-240 VAC	
	Minimum	**Maximum**
Logic level low voltage (200-240 VAC)	0 V	1.0 V
Logic level high (100-240 VAC)	2.0 V	5.25 V
Source current, VACrange = low		4 mA

5.6.4 ACOK# Signal (*output*)

ACOK# allows the power supply to meet the AC Brownout requirement with multiple power supplies in parallel.

This signal is pulled LOW when the AC input voltage has reached the minimum level defined by the ACRange signal. The characteristic of the ACOK# signal is shown in Table 31.

The purpose of this signal is to synchronize the power-on timing of multiple power supplies within the system. The system will monitor the ACOK# signals. When enough ACOK# signals are active to allow the system to be powered on, the system will activate the PSON# signals to all power supplies.

Table 31. ACOK# Signal Characteristics

Signal Type	Open collector/drain output from the power supply. Pull-up to VSB located in system.	
ACOK# = Low	AC line voltage is OK	
ACOK# = High	AC line voltage is too Low	
	Minimum	**Maximum**
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 A		5.25 V
Sink current, ACOK# = low		4 mA
Sink current, ACOK# = high		50 A
ACOK# trip point for 200-240 VAC		175 VAC
ACOK# trip point for 100-240VAC		85 VAC
ACOK# Delay: T_{acok_delay}	20 msec	
ACOK# rise and fall time		100 sec

5.6.5 PWOK (Power Good *output*)

PWOK is a power good signal and will be pulled HIGH by the power supply to indicate that all the outputs are above the regulation limits of the power supply. When any output voltage falls below regulation limits, or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall be inhibited as long as any power supply output is in current limit.

Table 32. PWOK Signal Characteristics

Signal Type	Transistor collector/drain output from power supply. Pull-up to VSB located in power supply.	
PWOK = High	Power Good	
PWOK = Low	Power Not Good	
	MIN	**MAX**
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isource=2 mA	2.4 V	5.25 V
Sink current, PWOK = low		4 mA
Source current, PWOK = high		2 mA
PWOK delay: T_{pwok_on}	100 ms	1000 ms
PWOK rise and fall time		100 sec
Power down delay: T_{pwok_off}	1 ms	200 msec

5.6.6 Predictive Failure Signal (PRFL *output*)

This signal indicates that the power supply (or power supply fan) is reaching its end of life. The signal indicates a predictive failure when the power supply allows this signal to go HIGH.

Table 33. PRFL Signal Characteristics

Signal Type (Active Low)	Open collector/drain output from power supply. Pull-up to VSB located in system.	
PRFL = High	Failing	
PRFL = Low	OK	
	Minimum	**Maximum**
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 A		5.25 V
Sink current, FAIL = low		4 mA
Sink current, FAIL = high		50 A
PRFL rise and fall time		100 sec

5.6.7 Power Supply Failure (FAIL *output*)

In the event of a power supply failure (OVP at any output, Under-Voltage (UV) at any output, fan failure, or other failure), this signal is allowed to go HIGH by the power supply.

Table 34. FAIL Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located system.	
FAIL = High	Failed	
FAIL = Low	OK	
	Minimum	**Maximum**
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 A		5.25 V
Sink current, FAIL = low		4 mA
Sink current, FAIL = high		50 A
FAIL rise and fall time		100 sec

5.6.8 Power Supply Present Indicator (PRESENT# *output)*

The PRESENT# signal is used to sense the number of power supplies in the system (operational or not). This signal is connected to the power supply's output ground.

Table 35. PRESENT# Signal Characteristics

Signal Type	Output from power supply that is connected to ground. Pull-up to VSB located in system.	
PRESENT# = Low	Present	
PRESENT# = High	Not Present	
	Minimum	**Maximum**
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 A		5.25 V
Sink current, PRESENT# = low		4 mA
Sink current, PRESENT# = high		50 A

Practically, this signal is implemented by a piece of copper to ground inside the power supply. In the prior table, the system circuit implements anything beyond Logic LOW.

5.6.9 Fan Control (FANC *input*)

The requirements for the FANC signal are identical to that of the ATX specification. The FANC signal is a fan speed and Sleep mode control signal. A variable voltage on this pin controls the fan speed and shutdown. This signal allows the system to request control of the power supply fan. The control circuit in the system supplies voltage to this pin from 12 VDC to 0 VDC for the fan control request. If the FANC signal is left open, the fan control defaults to power supply control.

Table 36. FANC Signal Characteristic

Signal Type	Accepts an output voltage from the system. Pull-up to 12 V inside the power supply.	
FANC < 1 V	SLEEP mode[2]	
2 V < FANC < 3 V	Fan in LOW speed[1]	
3 V < FANC < 10.5 V	Fan ramps from LOW to HIGH speed[1]	
FANC > 10.5 V	Fan in HIGH speed[1]	
	Minimum	**Maximum**
Source current		2 mA
Fan SLEEP mode output power[2]		50 W
Fan LOW speed ambient temperature[3]		35 C

Notes: 1) This is a request from the system to the power supply to operate the fan at this condition. The power supply can override this request and increase the fan speed if the power supply requires more cooling. Refer to Note 2 for fan SLEEP mode requirements.

2) When the power supply fan is in SLEEP mode, the fan must be operating at its minimum RPM, which is slow enough to not output any noticeable audible levels. The power supply must be able to supply 0 W to 50 W of output power at 50 C ambient (on the 48 VDC output) in the power supply fan SLEEP mode condition without the power supply over-riding and turning the fan to LOW or HIGH speed.

3) This is the ambient temperature the power supply must be able to supply maximum load at LOW fan speed.

5.6.10 Power Supply Field Replacement Unit Signals

Five pins are allocated for the FRU information on the Power Supply connector. One pin is the Serial Clock (SCL). The second pin is used for Serial Data (SDA). Both pins are bi-directional and are used to form a serial I^2C bus.

The I^2C bus is 5 V tolerant. Pins 3 through 5 are address lines A0-A2 to indicate to the power supply's EEPROM which position the power supply occupies in the power bay.

The FRU circuits inside the power supply must be powered off of 12 VSB on the system side of the OR-ing device.

The EEPROM should be set up to accept writes. In the particular case of 24C02, the Write Control (or Write protect) pin should be tied to ground inside the power supply so that information can be written to the EEPROM. A0, A1, and A2 must be pulled High inside the power supply to the EEPROM 5-V bias voltage (derived from 12 VSB) through separate 10-k resistors.

5.6.11 LED Indicators

There will be a green POWER LED (PWR) to indicate that AC is applied to the Power Supply Unit (PSU) and Standby Voltages are available when blinking. This same LED should go solid to indicate that all the power outputs are available. There will be an amber Power Supply Fail LED (FAIL) to indicate that the Power Supply has failed, therefore a replacement of the unit is necessary. There will be an amber Predictive Fail LED (PFAIL) to indicate that the power supply is about to fail in the near future due to a poorly performing fan. This LED should be blinking to indicate the predictive failure condition and should be latched into blinking state once the condition has occurred. This latch can be cleared by toggling the PS-ON signal or by an AC power interruption of greater than one second. Refer to the following table for conditions of the LEDs.

Table 37. LED Indicators

Power Supply Condition	Power Supply LED's		
	PWR (green)	PFAIL (AMBER)	FAIL (AMBER)
No AC power to all PSU	OFF	OFF	OFF
Power supply failure or no AC power to this PSU only	OFF	OFF	ON
AC present / Standby Output On	Blinking	OFF	OFF
Power supply DC outputs ON and OK	ON	OFF	OFF
Current limit	ON	OFF	Blinking
Predictive failure	ON	Blinking/Latched	OFF

The LEDs shall be visible on the power supply surface that is opposite to the docking end. The LED location shall meet ESD requirements. LEDs shall be securely mounted in such a way that incidental pressure on the LED will not cause it to become displaced.

5.7 Environmental Requirements

5.7.1 Physical Environment

The power supply is located inside the SR870BN4 system assembly. The system may contain up to two power supplies in a 1+1 redundant power supply configuration.

5.7.2 Thermal Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an Over-Temperature Protection (OTP) condition, the PSU will be shutdown with the exception of the 12-VSB output. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically. The OTP circuit must have built-in hysteresis such that the power supply will not oscillate on and off due to temperature recovering condition. The power supply shall alert the system of the OTP condition via the power supply FAIL signal and the FAIL LED indicator.

5.8 Regulatory Agency Requirements

The power supply must have UL recognition, CSA or cUL certification to Level 3, or any NORDIC CENELEC-certified (such as SEMKO, NEMKO or SETI) markings demonstrating compliance. The power supply must also meet FCC Class B, VDE 0871 Level B, and CISPR Class B requirements.

6. Front Panel Board

This chapter describes the front panel board used in the SR870BN4 server system. This chapter is organized into the following sections:

Section 6.1: Introduction
Provides an overview of the front panel board.

Section 6.2: Functional Architecture
Describes the front panel features.

Section 6.3: Signal Descriptions
Describes connector pin-out (signal names and descriptions).

Section 6.4: Electrical, Environmental, and Mechanical Specifications
Specifies operational parameters and considerations.

6.1 Introduction

The front panel provides a means of mounting and electrical connection for switches and indicators accessible from the front of the chassis. The Power-On/Off and System Reset are examples of switches mounted on the front panel board, which are accessible at the front of the chassis. Power-on and System Power Fault LEDs are examples of indicators mounted on the front panel board, which are viewable at the front of the chassis.

6.2 Functional Architecture

The front panel has four switches, five LEDs and the system speaker as shown in Figure 34 and described in Table 38. The four switches control Power-On, Reset, SDINT, and the System ID function. The SDINT switch is accessible via a small hole in the front of the chassis and requires a small instrument to activate it. The power LED indicates system power in a steady green state and ACPI sleep mode in blinking green state. The other four LEDs indicate any system power faults, system cooling faults, system faults such as a hard drive failure, and the System ID function. A 14-position PCB edge connector provides control and status information to/from the baseboard.

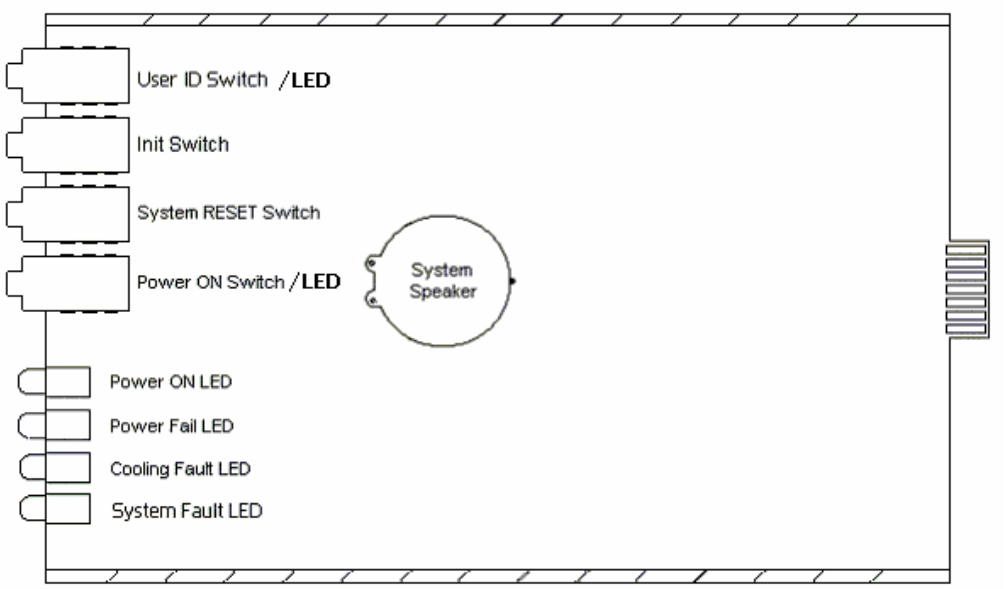


Figure 34. Front Panel Features

Table 38. Front Panel Features

Feature	Function
Switches:	
Power	Toggle system power
SDINT	Assert SDINT to baseboard
Reset	Reset system
System ID	Acknowledge System ID
LED Indicators:	
Power	Green indicates system power on, blinking green indicates system is in sleep mode
System Power Fault	Amber, indicates any System Power Faults
Cooling Fault	Amber, indicates any System Cooling Faults
General Fault	Amber, indicates any System failure
System ID	Blue, indicates System ID
Connectors:	
Baseboard	Edge-connector to baseboard signals

6.3 Signal Descriptions

A 14-position PCB edge connector provides control and status information to/from the front panel board via the midplane board. Table 39 describes the signals on the edge connector.

Table 39. Midplane / Front Panel Interface

Pin #	I/O	Signal Name	Description
1	O	COOL_FLT_LED_L	Cooling Fault LED Cathode
2	O	GEN_FLT_LED_L	General Fault LED Cathode
3	O	PWR_FLT_LED_L	Power Fail LED Cathode
4	O	ON_LED_L	Power On LED Cathode
5	O	ID_LED	System ID LED Anode
6	O	SPEAKER	Speaker Drive Signal
7	I	CHASS_ID	System ID Switch
8	PWR	GND	GND
9	PWR	GND	GND
10	PWR	+3.3V_STDBY	Vcc
11	PWR	+3.3V_STDBY	Vcc
12	I	SDINT_SW_L	SDINIT Switch
13	I	RESET_SW_L	Reset Switch
14	I	POWER_SW_L	Power On/Off Switch

6.4 Electrical, Environmental, and Mechanical Specifications

6.4.1 Electrical Specifications

Current limiting resistors will be implemented on the baseboard. The LEDs on the front panel are able to handle the continuous current shown in Table 40.

Table 40. LED Current Requirements

LED Name	Current	LED Color
PWR_LED	20 mA	GREEN
POWER_FAULT_LED	20 mA	AMBER
COOLING_FAULT_LED	20 mA	AMBER
GENERAL_FAULT_LED	20 mA	AMBER
USER_ID_LED	20 mA	BLUE

6.4.2 Environmental Specifications

The front panel meets the board level specifications as specified in the *Intel Environmental Standards Handbook*. Table 41 summarizes environmental limits, both operating and non-operating.

Table 41. Environmental Specifications

Temperature	**Specification**
Non-Operating	-40 C to 70 C
Operating Temperature	0 C to 55 C
Thermal Map	Must not exceed maximum Integrated Circuit (IC) junction temperature as specified in the Component Data Sheets (CPDs).
Thermal Shock	**Specification**
Non-Operating	-40 C to 70 C
Humidity	**Specification**
Non-Operating	92% Relative Humidity (RH) at +50 C
Vibration	**Specification**
Non-Operating	Random input, 0.01 g2/Hz at 5 Hz, sloping to 0.02 g2/Hz at 20 Hz, and maintaining 0.02 g2/Hz from 20 Hz to 500 Hz.
Shock	**Specification**
Non-Operating	50 g, 11 msec
ESD	**Specification**
Operating	Indirect (radiated) only. Test to 15 KV with limited errors and to 20 K with no damage.
EMI	**Specification**
Operating	Required to meet EMI emission requirements, tested as part of system.

6.4.3 MTBF Specification

A Mean Time Between Failure (MTBF) prediction for the front panel will be calculated in order to identify any potential reliability design issues related to the product.

The MTBF prediction reveals the inherent reliability of the product. For circuit boards, the MTBF prediction is based on the component hard failure rates. These hard failure rates are assumed to be random in nature and are derived from either component supplier's reliability test results or the BELLCORE* Reliability prediction procedure.

For the system MTBF predictions, the circuit boards, peripherals, power supply and other sub-assembly reliability data is reviewed and included into the system prediction. A calculated MTBF will be generated using the Intel/BELLCORE methodology as documented in Intel procedure 187677.

7. SCSI Backplane Board

This chapter describes the SR870BN4 SCSI backplane board. This chapter is organized into the following sections:

Section 7.1: Introduction
Provides an overview of the SCSI backplane board showing functional blocks and board layout.

Section 7.2: Functional Architecture
Describes the SCSI backplane's functional blocks.

Section 7.3: Signal Descriptions
Summary of the SCSI backplane's interior signals and connector signals, and the connector signal pin names and the signal descriptions. Signal mnemonics appear throughout this chapter.

Section 7.4: Electrical, Environmental, and Mechanical Specifications
Specifies operational parameters and considerations, and connector pin-outs.

7.1 Introduction

The SCSI backplane is designed to give the end user support for three SCSI hard drives, IDE DVD/CD, and an LS-240 drive. The intent of the design is to support greater than 4-way systems. The design enables easy use and replacement of the SCSI hard drives without powering down the system. The design also allows easy use and replacement of the IDE drives, however the system MUST be powered down to remove or insert IDE drives. The following block diagram, architectural overview, and placement diagram will give a general idea of how the SCSI back plane works.

7.1.1 Block Diagram

Figure 35 illustrates the general architecture of the SCSI backplane. The diagram breaks down the SCSI backplane into physical and functional blocks. Arrows represent buses and signals. Blocks represent the physical and functional blocks.

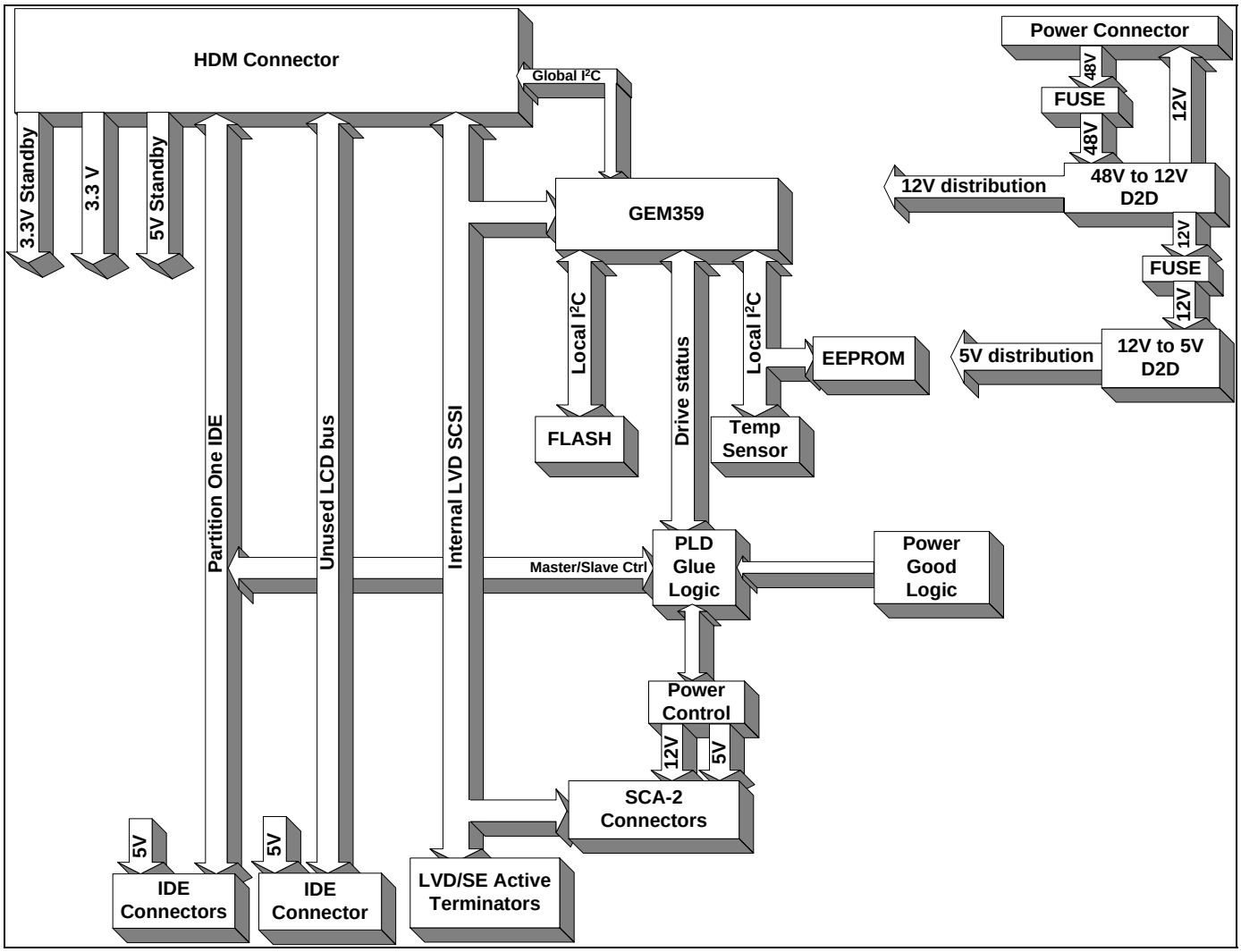


Figure 35. SCSI Backplane Block Diagram

7.1.2 Architectural Overview

The SR870BN4 SCSI backplane provides five main functions for the system. The backplane provides cascading power conversion from +48 V to +12 V, and +5 V. The second function is to pass the SCSI signals between the I/O board and the SCSI drives. The third function is to provide hooks for enclosure management. The fourth function is to pass the IDE signals between the I/O board and the DVD/LS-240 drives. The fifth function is to provide I^2C server management interface.

Functional blocks:

- Cascaded Power Conversion

54 +48 V to +12 V

55 +12 V to +5 V

- Ultra 320 LVD SCSI bus passes SCSI signals between the SCSI drives and the I/O board

56 One HDM connector from I/O board

57 Three 80-pin SCA-2 blind-mate connectors to mate with SCSI drives

- Fault Tolerant Enclosure Management.

58 SAF-TE

59 SCSI Power Control

60 LED control logic

- IDE bus passes IDE signals between the IDE drive and the I/O board

61 Two EuroCard blind-mate connectors. The connectors supply signals and power to IDE devices. Two connectors for the primary partition.

62 One HDM connector from I/O board

63 NOTE: IDE DRIVES ARE NOT HOT-SWAPPABLE

- Server management

64 I^2C interface

65 I^2C Serial CMOS EEPROM (FRU)

66 Temperature sensor

67 Power good detection

7.1.3 Component Location

Figure 36 shows the 3D placement of the major components and connectors on the SCSI backplane.

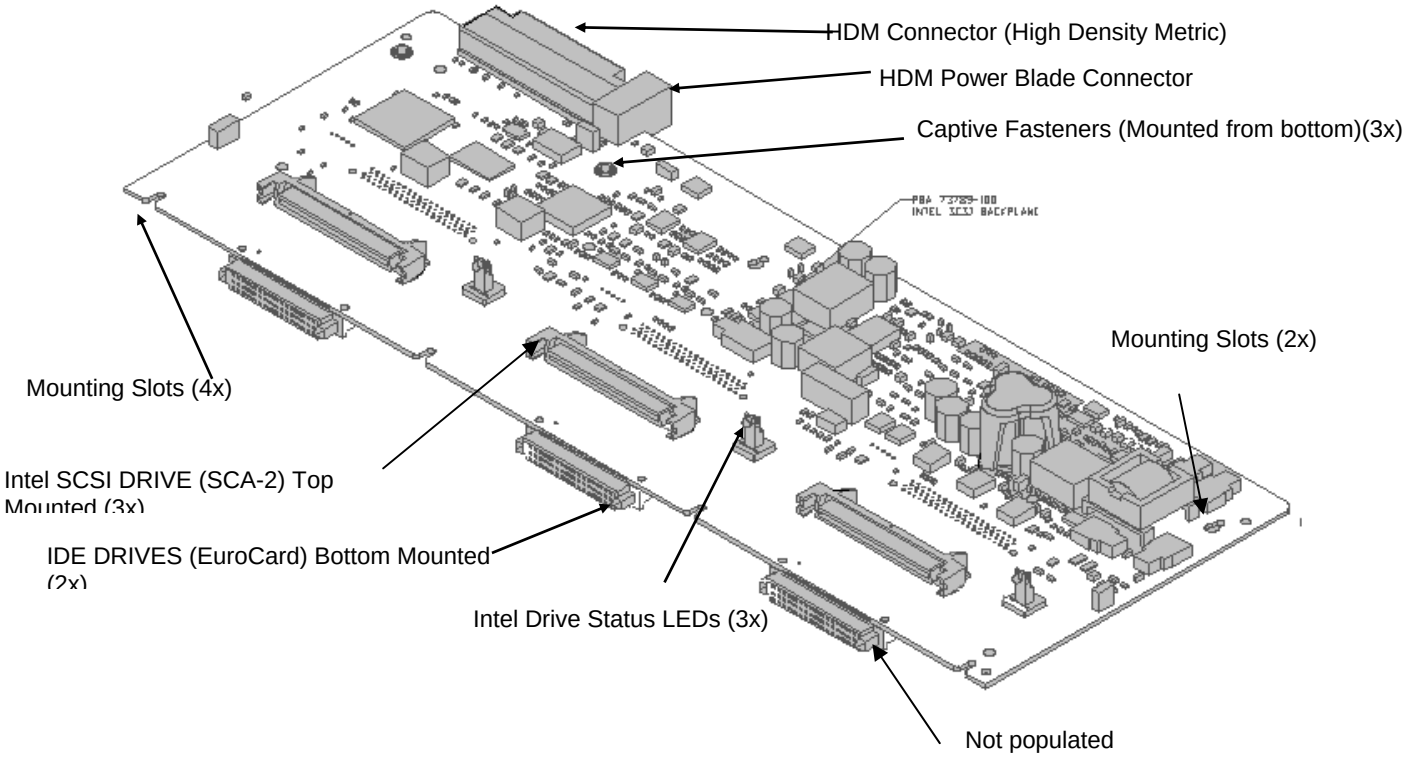


Figure 36. 3D SCSI Backplane Layout

7.2 Functional Architecture

This section provides a more detailed architectural description of the SCSI backplane's functional blocks.

7.2.1 Power Conversion

+48-V board input is cascaded to +12-V and +5-V supplies.

7.2.1.1 +48V to +12V DC to DC Converter

The 48-V to 12-V D2D converts the +48-V supply to +12 V. The generated +12 V is used by the local 12-V to 5-V D2D, internal SCSI drives, and the I/O board.

- Output rated at 12 V +/- 5% at a maximum of 10.5 amps continuous, 16 amps peak.
  The +12-V output will be between +11.4 V and +12.6 V. The circuit was designed to safely supply up to 16 amps of current without any damage to the circuit.

- Di/dt rated at 15A-20 A/uS.

  Pulse width modulator (PWM) provides 12-V regulation.
  Switching a continuous 48-V supply at approximately 80 KHz, produces +12 V.

- 48-V return to digital ground isolation.
  Transformer provides isolation between 48 return and digital/analog ground.

- Opto-isolator provides isolated feedback to the PWM.
  The PWM is protected from the 12-V output by an opto-isolator. The opto-isolator also maintains separation of 48 return and digital ground.

- 12-V sense input is used to sense the voltage on the I/O board.
  A feedback line is provided to regulate the voltage on the I/O board. The +12-V supply to the I/O board is looped back to the SCSI backplane via the 12-V sense line. If for test, the 12-V sense line is left unconnected then the +12-V output will be regulated to the local +12-V plane on the SCSI backplane.

- Over voltage protection at 13.3 V.
  When the over voltage threshold is exceeded, the PWM receives feedback to lower output voltage. The over voltage protection circuit will only be activated if the normal voltage detection/regulation circuit is defective.

- Over current protection at 16 amps.
  When the over current protection threshold is exceeded, the frequency of the PWM will be throttled back until the over current protection condition subsides. The D2D circuit is protected from any damage during a short.

- Voltage regulation starts when input voltage exceeds ~12.6 volts.

7.2.1.2 +12-V to +5-V DC to DC Converter

The 12-V to 5-V D2D converts the +12-V supply to +5 V. The generated +5 V is used by the local logic, internal SCSI drives, and internal DVD/LS-240 drives.

- Rated at 5 V +/- 5% at a maximum of 7.5 amps.

  The +12-V output will be between +4.75 V and +5.25 V. The circuit was designed to safely supply up to 10 amps of continuous current without any damage to the circuit.

- Di/dt rated at 15A-20 A/uS.

- Programmable synchronous-buck regulator controller provides 5-V regulation.

- Over voltage protection at ~ 5.25 V.

- Over current protection at 10 amps.

  When the over current protection threshold is exceeded, the regulator shuts down and the +5-V output drops to zero volts. The D2D OCP state is not reset until the +12 V is turned off and then back on (recycling system power). The OCP is filtered, an over current condition must be present for 0.1 mS to trigger OCP. The D2D circuit is protected from any damage during a short.

7.2.2 SCSI Bus

The SCSI backplane passes the SCSI bus from the I/O board to the internal SCSI drives. The SCSI bus is Ultra 320 (SPI-4) capable. SE drives are not supported. Do not install internal SE drives, as the behavior of the drives is unpredictable and data corruption could result. The bus is comprised of 68 signals. The bus clock is 80 MHz. The 320 MB data rate results from double transition (DT) data transfers on a two byte-wide bus. The SCSI bus attaches to the I/O board via a 144-pin High Density Metric (HDM) connector.

320 Mbytes/s = 2 byte bus * 80 MHz clock * double transitions.

Note: Drives and SCSI controller on the I/O board determine actual SCSI bus data rate.

7.2.2.1 SCSI Drive Power Control

SCSI power control is provided on the SR870BN4 SCSI backplane. SCSI power control includes SCSI drive power switching, initial power-on charge pumping, over-current protection, system status notification, and SCSI drive status LEDs.

If a SCSI drive is detected, the system will be notified. Status LEDs will provide the user with visual indicators for the internal SCSI drive.

Once the system is powered up, the user can request the system to stop SCSI bus activity. The system will ensure there is no SCSI bus activity. The user can then safely remove the internal SCSI drive. Upon reinserting an internal SCSI drive, the user must notify the system.

7.2.2.1.1 Internal SCSI Drive Power Switching

Each SCSI drive is supplied with +12 V and +5 V. Separate MOSFET switches apply the +12 V and +5 V to each internal SCSI drive.

7.2.2.1.2 Initial Power-on Charge Pumping

When power is first applied to a SCSI drive, there is a large initial current surge (up to 20 amps). To reduce this initial current surge, the SR870BN4 SCSI backplane charge pumps the drives for ~1.5 ms. Charge pumping the drives keeps the average power-on current at around three amps.

7.2.2.1.3 Over-current Protection

If either of the drive's power rails exceeds 5 amps, the MOSFET switch for the problematic rail will be turned off. Removing power will protect the MOSFET and system from damage in the event of a short on one of the power rails. After one third of a second, the MOSFET will be turned on to see if the short has been removed. Turning on and checking for a short every one third of a second will continue until the fault disappears.

During the charge pump period, the over current condition is not detected. This OCP disabled period allows the initial current surge produced by many SCSI drives. The pulses are short enough to not allow damage to occur to the MOSFETS or the system.

7.2.2.1.4 Power Control Inter-lock

The power control inter-lock prevents drives from powering on at the same time. Since only one drive can power on a time, the board power requirements can be kept lower. After one drive starts, the next drive will start one third of a second later.

7.2.2.1.5 System Status Notification

Internal SCSI drive status information is collected by the microcontroller. The microcontroller passes the information to the server management via the global I^2C bus, and Enclosure Management via the SCSI bus.

7.2.2.1.6 SCSI Status LEDs

The SR870BN4 SCSI backplane is configured with three through-hole mounted bi-color LEDs. The status LEDs give the user a visual indication of the drive's condition. There is a single LED for each drive. The LEDs are bi-colored and use a combination of color and blinking frequency to indicate multiple conditions. The LEDs are housed in a sturdy plastic stand-off and are through-hole mounted. See Table 43 for LED activity definitions. See Figure 37 for LED and light pipe cross section. See the *Firmware EPS* for definitions of the different blink rates.

Table 42. LED Specifications

LED Color	Peak Wavelength (nm)	Luminous Intensity Typical (mcd)	Luminous Intensity Max. (mcd)
Green	565	15	6.5
Yellow	585	14	6.0

Table 43. LED Activity Definitions

LED State	Drive Active	Fault Condition
Blinking Green	X	
Blinking Yellow/Green		X
Blinking Yellow/Blank		X
Blank		

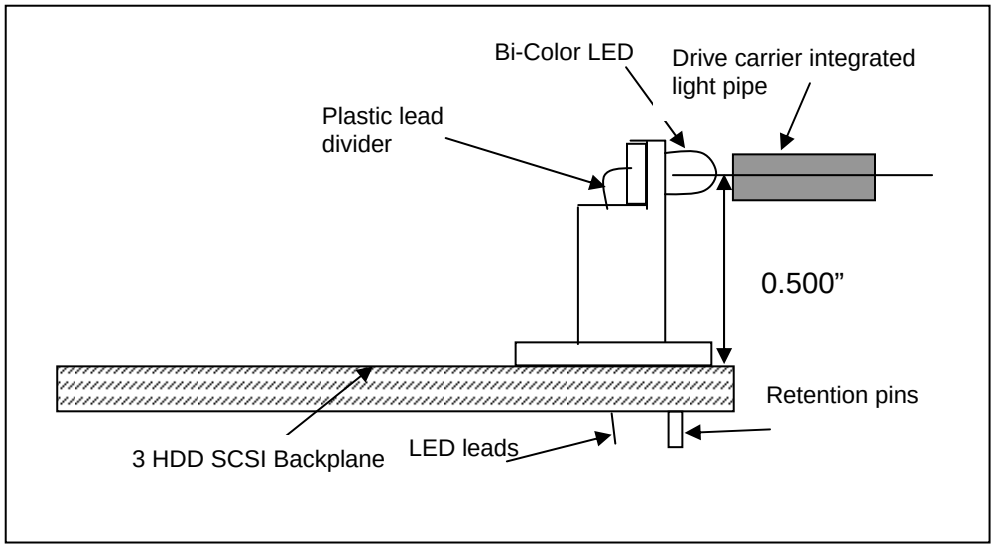


Figure 37. LED Cross-section (not to scale)

7.2.3 IDE Bus

The SCSI backplane passes an IDE bus from the I/O board to the internal IDE drives. The IDE bus is ULTRA DMA mode two (DMA33) capable. The IDE bus connects from the HDM connector (I/O board) to two EuroCard connectors. The connectors take the IDE signals to separate IDE adapter boards, and then to IDE devices. The connectors are spaced to allow a CD-RW drive and an LS-240 drive.

7.2.3.1 IDE Bus Master/Slave Selections

One IDE device per bus must always be set as master. The primary IDE bus can be configured in a couple of different ways so the SCSI backplane actively determines which device is set to master. See Table 44 to determine which device will be set to master depending on configuration. Master/slave is set by the Cable Select (CSEL) value. See Table 45 for CSEL setting.

Table 44. Master/Slave Setting

Drive 1	Drive 2	Master Device	Slave Device
Present	Present	Drive 0	Drive 1
Present	Absent	Drive 0	NA
Absent	Present	Drive 1	NA

Table 45. CSEL Setting

CSEL Value	Meaning
0	Master
1	Slave

7.2.3.2 EuroCard Connector

The EuroCard* connector is a blind-mate connector. This makes the IDE devices easy to install and remove. However, the IDE bus is not hot-swappable. Therefore the system must be powered down to remove or install drives.

NOTE: In the SR870BN4 system, the P-Bay must be partially removed before removing the IDE drive. This extra step was added because the IDE bus is NOT hot-swappable. Without this extra step, removing or installing the IDE drives would be too easy and encourage improper use.

7.2.4 SCSI Enclosure Management

SCSI Enclosure Management allows the SCSI backplane to report on SCSI drive status via the SCSI bus. Normally a RAID controller will interface with Enclosure Management. The SCSI Enclosure Management subsystem consists of a QLogic* GEM359 controller, Flash, and Programmable Logic Device (PLD). Refer to Figure 38 when reading the following subsystem descriptions.

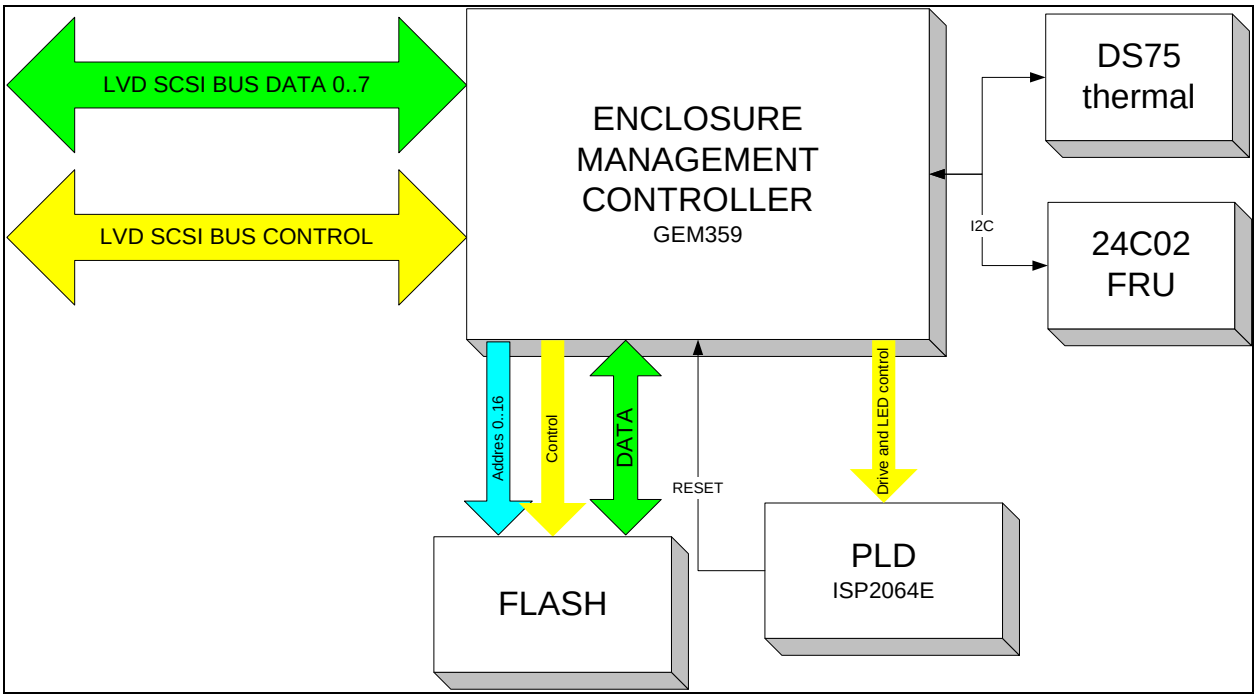


Figure 38. Enclosure Management Signal Flow Diagram

7.2.4.1 QLogic* GEM359 Enclosure Management Controller

The GEM359 sends acquired board information to the SCSI bus and IPMB. The GEM359 also acts on requests from both the SCSI bus and IPMB. GEM359 GPIOs send LED and drive power control to the PLD. Please see the *GEM359 Firmware EPS* for further information.

7.2.4.2 Four Meg Flash

The GEM359's code is stored in a 4 Meg Flash (512K x 8) component. The Flash boot block is in the top 16k of the block. The boot block is normally protected. Non-protected FLASH can be updated via the IPMB bus.

7.2.4.3 PLD

The PLD uses the LED information and drive control data to control the LEDs and SCSI power control circuits.

7.2.5 Server Management Interface

The SR870BN4 SCSI backplane will support the following server management features:

Local I^2C* Interface

- SCSI backplane FRU
- SCSI backplane temperature sensor
- Microcontroller interface

System I^2C* Interface

- Microcontroller IPMB interface

7.2.5.1 Local I^2C* Bus

The local I^2C bus connects the DS75* (or equivalent) thermal sensor and Atmel* AT24C02N (or equivalent) serial EEPROM to the microcontroller.

7.2.5.2 Global I^2C Bus (IPMB)

The global I^2C bus connects the microcontroller-controller to the system. The microcontroller-controller is isolated from the system until the system PWRGRD signal is asserted.

7.2.5.3 I^2C* Addresses

Three I^2C devices and their addresses are listed in Table 46 and Table 47. These I^2C devices can be addressed on or through the SCSI backplane.

- Hot-Swap microcontroller
- SCSI backplane FRU EEPROM
- SCSI backplane temperature sensor

Table 46. I^2C* Local Bus Addresses

Device	Address	Bus/Location	Description
Atmel* AT24C02	0xA0	Legacy I^2C/ SCSI backplane	Private SCSI backplane FRU EEPROM
DS75*	0x90	Legacy I^2C/ SCSI backplane	Private SCSI backplane temperature sensor

Table 47. I²C* Global Bus Addresses (IPMB Bus)

Device	Address	Bus/Location	Description
GEM359*	0xC0	Legacy I²C/ SCSI backplane	Microcontroller controller public IPMB bus

7.2.6 Power Good Circuit

Power good signals are positive logic signals reflecting the status of various power rails.

7.2.6.1 Power Good Outputs

On-board power good circuits monitor both the 12-V and 5-V rails. When the +5-V rail is within +/-5% of +5 V, the 5-volt power good signal is asserted. When the 12-V signal is greater than 12 V –5%, the 12-volt power good signal is asserted. Both detection circuits have built-in hysteresis to prevent chatter. The 5-V and 12-V power good signals are ANDED together (via the PLD) to generate the SCSI_V_GOOD output signal.

7.2.6.2 Power Good Inputs

The power good input tells the SCSI backplane that the all system D2Ds are powered up and working within specifications.

7.2.7 Reset Control

The Reset signal resets both the PLD flip-flops and the microcontroller. Reset is asserted on the S870BN4 SCSI backplane in three different conditions:

1. When system PWRGD is de-asserted.
2. When the ISP chain is enabled.
3. When either 5-V or 12-V power good signals are de-asserted.

7.2.8 Connector Interlocks

All connectors on the SCSI backplane have interlocks.

7.2.8.1 EuroCard Connector

Interlock is used by the SCSI backplane to determine if the IDE device is present. EuroCard interlock is defined by the MATED_IDE# signal. For information on how interlock is used to set CSEL, see Section 7.2.3.1.

7.2.8.2 HDM Connector

Interlock is used by the I/O board to determine if the SCSI backplane is properly mated. HDM interlock is defined by the HDM_MATED signal.

7.2.8.3 SCA-2 Connector

Interlock is used by the SCSI backplane to determine if the SCSI device is present. SCSI interlock is defined by the SCSI_MATED# signals. Drive presence is used by enclosure management.

7.2.9 Configuring Jumpers

This section describes jumper options on the SR870BN4 SCSI backplane. Figure 39 shows the jumper. Table 48 provides a summary of the different settings. The ONLY jumper that will be present on the production board is J7D1.

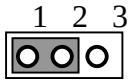


Figure 39. Jumper Settings on SCSI Backplane

Table 48. Configuration Jumper Settings

Jumper	Name	Description	1-2 Setting	2-3 Setting	Default Position
J7D1	Boot Recovery	If the Flash run time code is corrupted, stuffing this jumper allows the FLASH to be reprogramed.	Normal operation	Forces a boot recovery	No jumper (1-2)
J1B1	SE/LVD Terminator Isolation	SCSI bus has onboard terminators that can be isolated from the bus. Isolating terminators removes terminators from the bus.	Terminators Connected	Terminators Isolated	Not stuffed (1-2)
J7E1	20-Mhz clock control	24-Mhz clock feeding PLD and microcontroller controller can be enabled/disabled.	Clock enabled	Clock disabled	Not stuffed (1-2)

7.2.10 Clock Generation

There is a single local clock on the SR870BN4 SCSI backplane.

- 20.0 MHz – supplies clock input to the GEM359 and PLD

7.2.11 Programmable Devices

There are three programmable devices on the SR870BN4 SCSI backplane, as follows.

7.2.11.1 FLASH

Flash contains program code to be run by the onboard microcontroller.

- Memory configuration: 512 K x 8

7.2.11.2 Field Replaceable Unit (FRU)

The FRU is programmed at ATE.

- Memory Configuration: 2 k serial

7.2.11.3 Programmable Logic Device (PLD)

The PLD governs the SCSI power control circuit, controls LEDs, and controls primary IDE bus master/slave settings. The PLD is In-System Programmable (ISP) and is attached to an ISP chain through the HDM connector.

7.3 Signal Descriptions

The following notations are used to describe the signal type, from the perspective of the SR870BN4 SCSI backplane:

I	Input pin to the SCSI backplane
O	Output pin from the SCSI backplane
I/O	Bi-directional (input/output) pin
PWR	Power Supply pin

The signal description also includes the type of buffer used for the particular signal:

LVD	Low Voltage Differential SCSI
SE	Standard Single Ended SCSI
TTL	5V TTL signals
CMOS	5V CMOS signals
3.3V CMOS	3.3V CMOS signals
Analog	Typically a voltage reference or specialty power supply

7.3.1 HDM Power Connector

Table 49 provides a summary of the power connector pins, including the signal mnemonic, the name, and a brief description.

Table 49. Power Interface Signals – J8E1

Signal	Type	Driver	Name and Description
P48V_RTN	I	PWR	Isolated +48-V return.
P48V	I	PWR	+48-V supply. These pins provide distributed 48-V power.
P12V	O	PWR	+12-V supply for I/O board.

7.3.2 IDE Power Connector

Table 50 provides a summary of the power connector pins, including the signal mnemonic, the name, and a brief description. *This connector is only for testing*.

Table 50. IDE Power Connector – J3C1

Signal	Type	Driver	Name and Description
P5V	I	PWR	+5-V supply. This power rail should not be used in a deployed system. Only to be used for testing.
P12V	I	PWR	+12-V supply. This power rail should not be used in a deployed system. Only to be used for testing.
GND	I	PWR	GROUND. These pins provide Distributed Secondary Ground.

7.3.3 HDM Connector

The HDM connector carries signals between the SCSI back plane and I/O board. The signal groups are SCSI, Primary IDE, Secondary IDE, Power Good, and I^2C.

7.3.4 LVD SCSI Connectors

The LVD connector carries signals between the SCSI back plane and internal SCSI drives. The LVD SCSI bus's signals are driven by either the I/O baseboard SCSI controller, the LVD/SE transceiver, or the internal SCSI drives.

7.4 Electrical, Environmental, and Mechanical Specifications

This section specifies the operational parameters and physical characteristics for the SCSI backplane. This is a board-level specification only. System specifications are beyond the scope of this chapter.

Further topics in this section specify normal operating conditions for the SCSI backplane, and mechanical specifications for the module and connector interfaces to the board.

7.4.1 Electrical Specifications

The power budget for the SCSI back plane and pin-outs of the external interface connectors are defined here.

Table 51. Electrical Specifications

Feature	Absolute Maximum Rating
Voltage of any signal with respect to ground	-0.3 V to Vcc[1] to Vcc[1]+0.3 V
+5-V stby supply with respect to ground	-0.3 V to +5.25 V
+3.3-V stby supply with respect to ground	-0.3 V to +3.465 V
+3 V supply with respect to ground	-0.3 V to +3.465 V
+5-V supply with respect to ground	-0.3 V to +5.25 V
+12-V supply with respect to ground	-0.3 V to +12.6 V
+48-V supply with respect to +48V return	-0.3 V to +50.4 V

Note: 1. Vcc means supply voltage for the device.

7.4.1.1 Power Consumption

Table 52 shows the power consumed on each supply line for the SCSI backplane. Table 53 shows the power provided by the SCSI back plane and the rest of the system.

Note: The numbers in Table 52 and Table 53 are provided only to show design limits. Actual power consumption will vary depending on the exact configuration.

Table 52. SCSI Backplane Maximum Power Consumption

Devices	Power Dissipation
48 V	140.7 W
5 V Standby	0.1 W
3 V	1 W
3.3 V Standby	0.4W

Table 53. Recommended SCSI Backplane Power Consumption

Maximum (in Amps)		
Board/Device(s)	**+5 V**	**+12 V**
SCSI backplane	0.4	0.2
IDE Peripherals (2 drive)	2.5	0
Internal SCSI drives (3 drives)	2.4[1]	3.8[2]
5V regulator	0	2.6
I/O Board	0	2.1
Total	**5.3**	**8.7**

Notes:

1. Current consumed with three SCSI drives operating.
2. Current consumed with two SCSI drives operating and one SCSI drive starting up. When a SCSI drive starts, the current exceeds the current needed during normal operation

7.4.1.2 SCSI Drive Supplied Power

The SCSI backplane is designed to work with three Cheetah* X15-18LP ST318451 drives; limits are shown in Table 54. To allow for future growth the SCSI backplane has adequate margin to support three SCSI drives that meet the drive power requirements outlined in SPI4 rev 09. However, if upgrading to a drive not provided with the system check with Intel for a list of approved drives.

Table 54. SCSI Backplane Power Limits per Drive

Device constraint	+5 V	+12 V
Peak Start Current	0.73	1.5 amps
Max Operating Current	0.81	1.15 amps
Average Idle	0.68 amps	0.61 amps

7.4.1.3 Power Supply Requirements

The external and internal power supply must meet the following requirements:

- Rise time of less than 50 msec (for all voltages).
- Delay of 5 msec (minimum) from valid power to power good.
- See Table 55 for voltage regulation requirements.

Table 55. DC Voltage Regulation

DC Voltage	Acceptable Tolerance
+48	± 5%
+5 V standby	± 5%
+5 V	± 5%
+12 V	± 5%
+3.3 V	± 5%
+3.3 V standby	± 5%

7.4.2 Connector Specifications

Table 56 shows the reference designators, quantity, manufacturer, and part number for connectors on the baseboard. Refer to the manufacturer's documentation for more information.

Table 56. SCSI Backplane Connector Specifications

Item	Reference Designator(s)	Quantity	Manufacturer and Part Number (or equivalent)	Description
1	J8E1	1	Molex*, 073670-0550 Teradyne*, AM870-00164	144-pin HDM pin connector with 3-pin power module.
2	J7B1, J4B1, J2B1	3	FoxConn, LS24403-K94E	Intel® 80 pin SCA-2 blind mate connector.
4	J2L1, J5L1, J7L1	3	Tyco Electronics, 148607-4	48-pin EuroCard RA blind mate connector.
5	J3C1	1	Molex Connector Corp.*, 15-24-4342	4-pin IDE power connector for testing only.

8. Power Distribution Board

This chapter describes the SR870BN4 Power Distribution Board (PDB). This chapter is organized into the following sections:

Section 8.1: Introduction
Provides an overview of the PDB describing main features, a block diagram, and board placement diagram.

Section 8.2: Functional Architecture
Describes in detail the main features of the PDB.

Section 8.3: Signal Descriptions
Summary of the PDB signals with descriptions.

Section 8.4: Electrical, Environmental, and Mechanical Specifications
Specifies electrical, mechanical, and environmental parameters as well as connector pin-outs.

8.1 Introduction

The PDB is a four-layer printed-circuit board assembly serving as a power-share board for two 1200-W power supply modules. Power supply modules blind mate into the PDB. The PDB couples current-shared voltages (48V DC and a 12V DC standby) from the power supplies to the system, provides control signals from the system to the supplies, and makes status signals from each power supply available to server management via the I^2C bus. The acceptable range for AC input voltage to the power supply modules is determined by a jumper block on the PDB. The PDB mounts to the system using only one captive screw.

8.1.1 Main Features

The PDB has the following main features:

- Distribution of +48V and +12V standby power and signals to midplane board.
- Power supply fan control circuitry.
- Power supply enable and power supply good status circuitry.
- AC range functionality.
- Local 5V standby converter.
- Server management interface via I/0 expander for power supply status signals.

8.1.2 Block Diagram

Figure 40 illustrates the general architecture of the PDB.

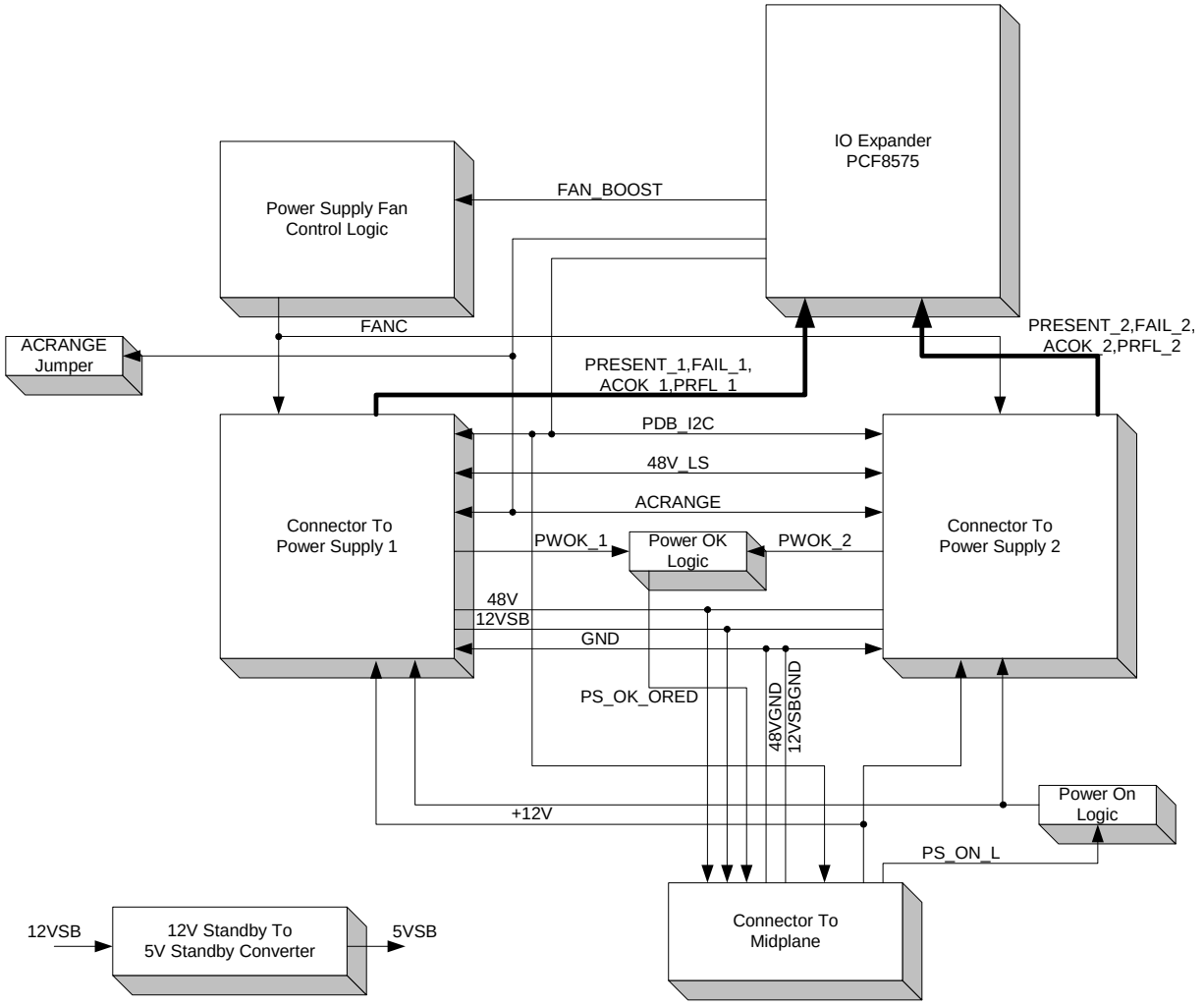


Figure 40. PDB Block Diagram

8.1.3 Placement Diagram

Figure 41 shows the placement of the components and connectors on the primary side of the PDB. There are no components or connectors on the secondary side.

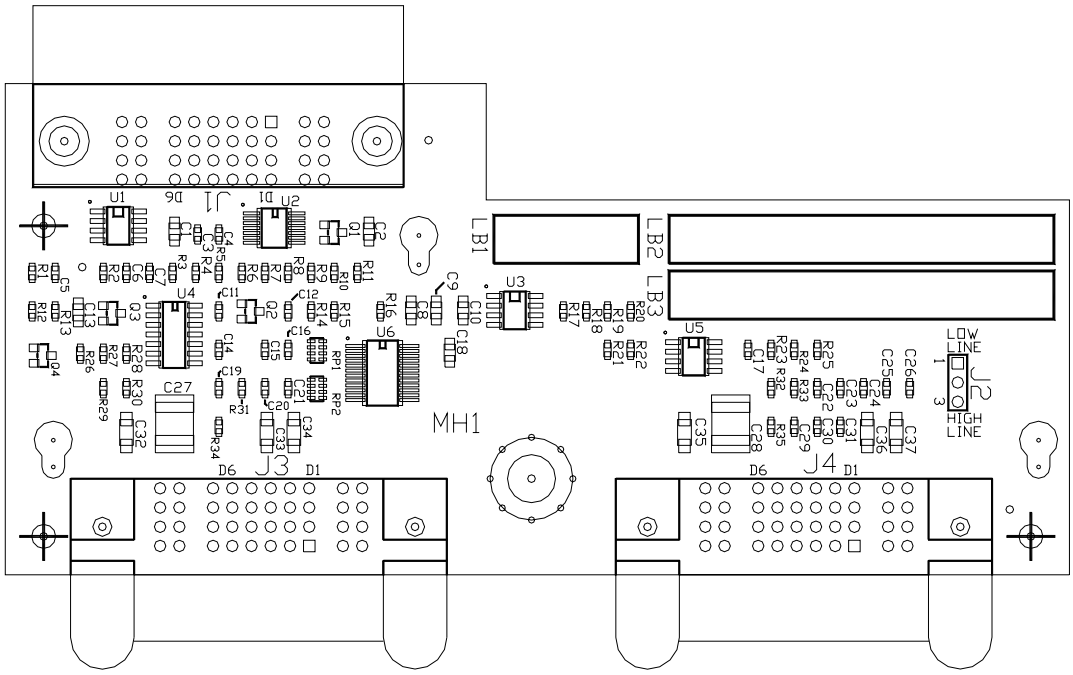


Figure 41. PDB Placement Primary Side

8.2 Functional Architecture

This section provides a more detailed description of the PDB features.

8.2.1 Power Distribution

+48 V and +12V standby from the power supply modules is directly connected to the midplane connectors. Primary +48V ground is tied together with +12V standby ground and chassis ground on the PDB. +12V is also provided to the power supply modules via the PDB. This ensures that even if a single power supply module fails, its fans have the capability to continue to operate on +12V from the system, thus providing continued cooling to upstream components such as memory DIMMS and D2Ds located on the processor module.

8.2.2 Power Supply Fan Control

The PDB has circuitry to change the speed of the power supply. The logic uses the FAN_BOOST input from server management via the I/O expander on the PDB, and may set the fans to operate at either low speed or high speed. The circuit supplies a voltage to the FANC pin of the power supply modules. A voltage of +12V to the power supply drives fans at high speed. The low voltage setting (V=+5.5volts) is determined by a hardware voltage divider circuit and cannot be adjusted via server management. The default is high speed.

8.2.3 Power Supply Enable and Power Good Status

The PDB receives, as an input, the PS_ON_L signal from the reset PLD on the I/O baseboard. Upon assertion of PS_ON_L from the I/O baseboard, the power supplies are forced to turn on. If the PS_ON_L signal from the I/O baseboard is de-asserted or is floating, the power supplies will shut off and remain off.

The PDB provides the PS_OK_ORED signal as an output to the reset PLD on the I/O baseboard and to the I/O expander on the PDB board. This signal results from a logic OR of the PS_OK signals from the two power supply modules. A power supply module asserts a PS_OK signal after all output voltages (+48V and +12V standby) are within regulation. The PS_OK_ORED signal can be monitored from the PCF8575 I/O expander.

8.2.4 AC Range Functionality

The PDB has a 1 x 3 jumper block (J2) that controls the trip point of the AC_OK signal for each power supply module, thereby dictating the AC input voltage the server should turn on at. Displayed in Figure 42 is the AC range jumper block PDB. The default setting with no jumper installed is the “low line” range (100-240 VAC). A jumper installed in the 1-2 position is “low line” range (100-240 VAC). A jumper installed in the 2-3 position is “high line” range (200-240 VAC).

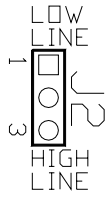


Figure 42. Jumper Settings on the PDB

Since the SR870BN4 server is 1+1 power supply redundant only in the “high line” range (200-240 VAC), adequate power at brownout recovery is always assured. However, if the jumper is set to the 100-240 VAC range, then brownout recovery is no longer assured. There are two reasons why brownout recovery is not guaranteed at the 100-240 VAC range:

1. AC current requirements for the server can potentially be too large to support a 1+1 power supply configuration when connecting to a “low line” AC main. A power supply module is limited to10 A at low line.

2. In a brownout recovery situation, the AC voltage slowly increases from 0 V to its nominal value. If the server is connected to a “high line” AC main, there is a good chance the AC mains will over-current trip when the system tries to turn on in the “low line” range.

8.2.5 Voltage Regulators

The PDB also has one local D2D linear regulator that converts +12V standby to +5V standby. 5V standby is used by the I/O expander, power supply fan control logic and for various signal pull-ups. The device has an input voltage range of +7V to +20V, a fixed output voltage of +5V, an output voltage tolerance of +/-5%, and a maximum output current of 100 mA.

8.2.6 Server Management Interface

The PDB has one PCF8575 I/O expander to make power supply module status signals accessible to server management. Consult the power supply module section of this document for a detailed description of the power supply status signals. PDB also allows server management to access power supply module FRU information.

Four I^2C devices are listed in Table 57 that may be addressed on or through the PDB.

Table 57. PDB Address Map

Device	Address	Bus/Location	Description
PS 1	0xA0/ 0xA1	I/O board I^2C / PDB	Power Supply 1 FRU Address
PS 2	0xA2/ 0xA3	I/O Board I^2C / PDB	Power Supply 2 FRU Address
PCF8575	0x44/ 0x45	I/O Board I^2C / PDB	Private PDB to I/O Board I^2C Expander

8.3 Electrical, Mechanical, and Environmental Specifications

This section specifies the operational parameters and physical characteristics for the PDB. This is a board-level specification only. System specifications are beyond the scope of this chapter.

Further topics in this section specify normal operating conditions for the PDB, and mechanical specifications for the module and connector interfaces to the board.

8.3.1 Electrical Specifications

The power budget for the PDB and pin outs of the external interface connectors are defined in the following table.

Table 58. Electrical Ratings for PDB

Feature	Absolute Maximum Rating
Voltage of any signal with respect to ground	-0.3 V to Vcc[1] to Vcc[1]+0.3 V
+5V standby supply with respect to ground	-0.3 V to +5.25 V
+12V standby supply with respect to ground	-0.3 V to +12.6 V
+12V supply with respect to ground	-0.3 V to +12.6 V
+48V supply with respect to G48V ground	-0.3 V to +50.4 V

Note: 1. Vcc means supply voltage for the device.

8.3.2 Power Dissipation

Table 59 shows the power dissipated by the PDB.

Table 59. PDB Maximum Power Consumption

Devices	Power Dissipation
48 V	2.4 W
12 V	0.5 W
12V standby	0.42 W
5V standby	0.35 W

Note: The numbers in Table 59 are provided only to show design limits. Actual power consumption will vary depending on the exact configuration.

8.3.3 Connector Specifications

Table 60 shows the reference designators, quantity, description, and part number for connectors on the baseboard.

Table 60. PDB Connector Specifications

Reference Designator(s)	Description
J3, J4	Power supply connector (4x6 signal+2 power blades)
J1	Midplane connector (4x6 signal+2 power blades)

9. Hot-Plug Indicator Board

This chapter describes the PCI Hot-Plug Indicator Board (HPIB) used in the SR870BN4 server system.

9.1 Introduction

The HPIB for PCI serves as a visual interface to the system administrator, giving PCI slot status.

9.2 Functionality

The HPIB provides status and interface to eight system PCI slots. For each slot there is one attention switch, four status LEDs, and a Hall-effect switch.

9.2.1 Attention switch

The attention switch is the first user point of contact during a PCI card hot-swap operation. By depressing the attention switch, server management is notified that a PCI hot-swap operation is about to take place.

9.2.2 Status LEDs

There are two pairs of status LEDs for each PCI slot. One pair is visible external to the system; the other pair is visible from inside the system. Each pair consists of a green and amber LED. The green LED is positioned closest to the top of the HPIB assembly, the amber LED directly below. LEDs are lined up on the center of each PCI slot. A lit green LED indicates that power is applied to the PCI slot. A lit amber LED indicates that server management or the device driver has an issue with the slot or the slot is populated.

9.2.3 Hall-Effect Switch

Each slot is equipped with a hall-effect sensor that monitors the position of the MRL switch. When the MRL is pushed back, releasing the PCI card, power is turned off to the slot. When the MRL is pushed forward, power is applied to the slot, and the green status LED turns on.

9.3 Mechanical Outline

Figure 43 shows the mechanical outline of the HPIB.

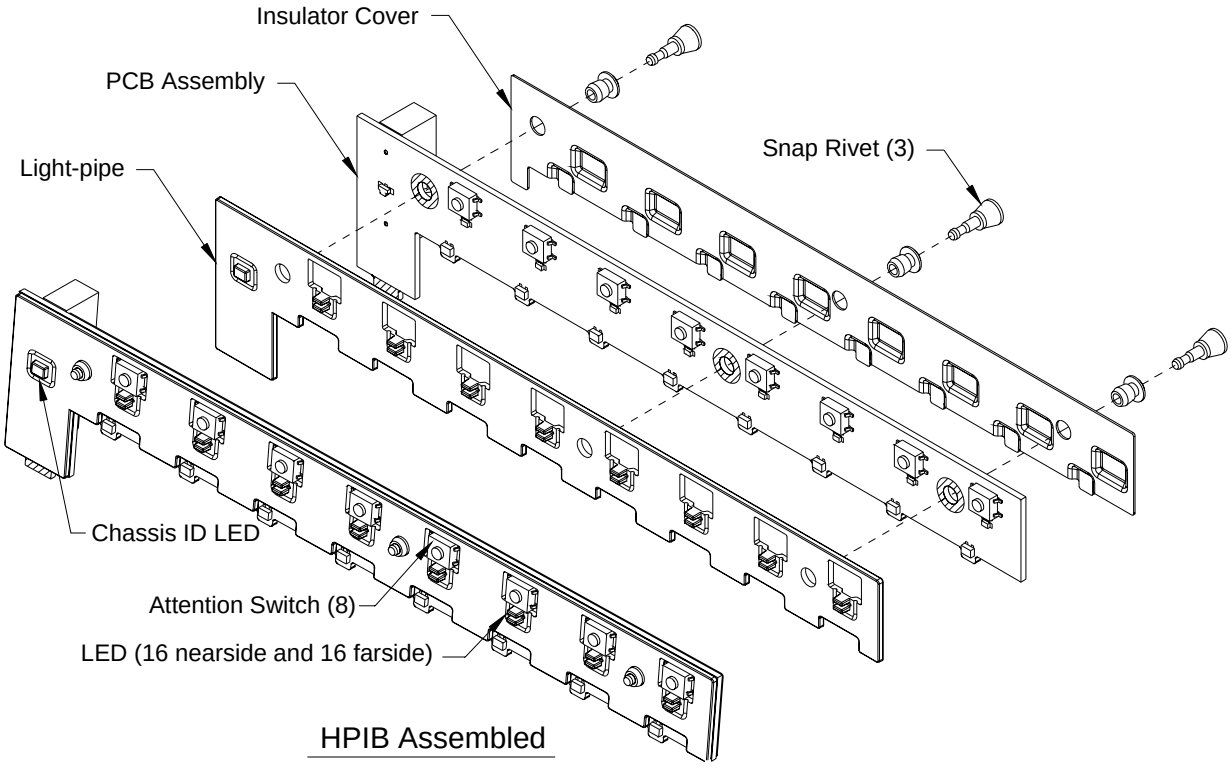


Figure 43. Mechanical Outline of PCI Hot-Plug Indicator Board (HPIB)

10. Peripheral Adapter Boards

This chapter describes the peripheral adapter boards used in the SR870BN4 server system.

10.1 DVD/CD and LS-240 Adapter Boards

The DVD/CD and LS-240 adapter boards serve as a medium to standardize the slim-line DVD/CD and LS-240 device pin outs and provide blind-mate features for mating with the SCSI backplane board.

10.2 Mechanical Outlines

Mechanical outline drawings of the LS-240 and DVD/CD adapter boards are shown in Figure 44. Both adapter boards are very close in size, however the LS-240 is red in color and the DVD/CD is green for easy identification. These boards are not compatible. Mixing adapter cards with incorrect peripherals will result in damage to the device.

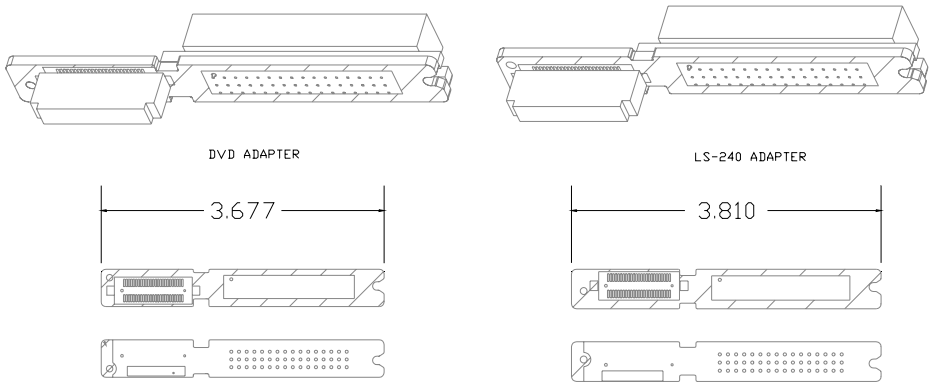


Figure 44. Mechanical Outline of Peripheral Adapter Boards

10.3 Special Features

The adapter boards have a MATED signal that is connected to the board VCC. When the board is connected to the SCSI backplane, the MATED signal is asserted. Logic on the SCSI backplane monitors the MATED signals of the two IDE peripherals that share the primary system IDE bus. The DVD/CD is always defaulted to Master, and when connected, the LS-240 will have Slave status. If only the LS-240 is populated, then the device will be set to Master. All Master/Slave configurations are done using CSEL logic, in accordance to X3-T13 ATAPI/ATA specifications.

11. Intelligent Chassis Management Bus (ICMB) Board

This chapter describes the optional Intelligent Chassis Management Bus (ICMB) board for use in the SR870BN4 server. This chapter is organized into the following sections:

Section 11.1: Introduction
Provides an overview of the ICMB board describing main features, a block diagram, and board placement diagram.

Section 11.2: Signal Descriptions
Summary of the ICMB board signals with descriptions.

Section 11.3: Electrical, Environmental, and Mechanical Specifications
Specifies electrical, mechanical, and environmental parameters as well as connector pin-outs.

11.1 Introduction

The ICMB board is a two-layer printed-circuit board assembly. ICMB signals are passed from external cables through the ICMB board to the I/O riser card via other system boards such as the I/O board and the HPIB board. The ICMB board supports the connector ID feature. See the *Intelligent Chassis Management Bus Specification*, V1.0 for more details about ICMB requirements. The ICMB board comes attached to a sheet metal bracket which is used for attachment to the system.

11.1.1 Main Features

The ICMB has the following main features:

- Two, 6-position SEMCONN vertical ICMB connections as the external interface
- Connector ID

11.1.2 Block Diagram

Figure 45 illustrates the general architecture of the ICMB board.

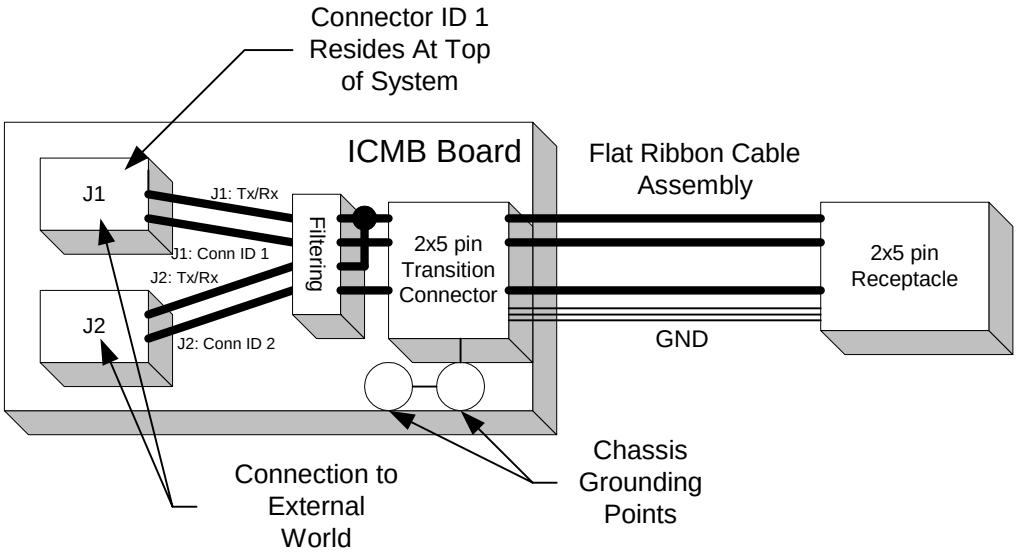


Figure 45. ICMB Board Block Diagram

11.1.3 Placement Diagram

Figure 46 shows the placement of the components and connectors on the primary side of the ICMB board. There are no components or connectors on the secondary side.

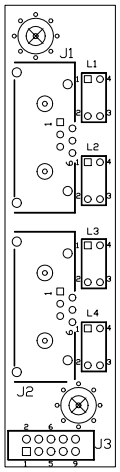


Figure 46. ICMB Board Placement Primary Side

11.2 Electrical, Mechanical, and Environmental Specifications

This section specifies the operational parameters and physical characteristics for the ICMB board. This is a board-level specification only. System specifications are beyond the scope of this chapter.

Further topics in this section specify normal operating conditions for the ICMB board and mechanical specifications for the module and connector interfaces to the board.

11.2.1 Electrical Specifications

The power budget for the ICMB board and pin-outs of the external interface connectors are defined here.

Table 61. Electrical Ratings for ICMB Board

Feature	Absolute Maximum Rating
Operating temperature	0 °C to +55 °C[1]
Storage temperature	-55 °C to +150 °C
Voltage of any signal with respect to ground	-0.3 V to Vcc[2] to Vcc[2]+0.3 V

Notes: 1. Chassis design must provide proper air flow.
2. Vcc means supply voltage for the device.

11.2.2 Power Consumption

Maximum short circuit current per signal pair is 34 mA for a total of 120 mA.

11.3 Connector Specifications

Table 62. ICMB Connector Specifications

Reference Designator(s)	Description
J1, J2	ICMB Connector (1x6 pins)
J3	Transition connector (2x5 pin). Note this connector is part of an integrated cable assembly.

12. Regulatory Specifications

The SR870BN4 server system meets the specifications and regulations for safety and EMC defined in this chapter.

12.1 Safety Compliance

USA/Canada:	UL 1950, 3rd Edition/CSA 22.2, No. 950-M93, 3rd Edition
Europe:	Low Voltage Directive, 73/23/EEC TUV/GS to EN60950 2nd Edition with Amendments, A1 = A2 + A3 + A4
International:	CB Certificate and Report to IEC 60950, 3rd Edition including EMKO-TSE (74-SEC) 207/94 and all national deviations

12.2 Electromagnetic Compatibility

USA	FCC 47 CFR Parts 2 and 15, Verified Class A Limit
Canada	IC ICES-003 Class A Limit
Europe	EMC Directive, 89/336/EEC EN55022, Class A Limit, Radiated and Conducted Emissions EN55024 ITE Specific Immunity Standard EN61000-4-2 ESD Immunity (level 2 contact discharge, level 3 air discharge) EN61000-4-3 Radiated Immunity (level 2) EN61000-4-4 Electrical Fast Transient (level 2) EN 6100-4-5 AC Surge EN6100-4-6 RF Conducted EN61000-4-8 Power Frequency Magnetic Fields EN61000-4-11 Voltage Dips and Interrupts EN61000-3-2 Harmonic Currents EN61000-3-3 Voltage Flicker
Australia/New Zealand	AS/NZS 3548, Class A Limit
Japan	VCCI Class A ITE (CISPR 22, Class A Limit). IEC 1000-3-2; Harmonic Currents
Taiwan	BSMI Class A
Korea	RRL, Class A
Russia	Gost Approval (EN55022, EN55024, EN60950)
International	CISPR 22, Class A Limit

12.3 CE Mark

The CE marking on this product indicates that it is in compliance with the European Union's EMC Directive 89/336/EEC, and Low Voltage Directive, 73/23/EEC.

12.4 Electromagnetic Compatibility Notice (USA)

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

12.5 Electromagnetic Compatibility Notices (International)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:
This is a Class A product based on the standard of the Voluntary Control Council for Interference by Information Technology Equipment (VCCI). If this equipment is used in a domestic environment, radio disturbance may arise. When such trouble occurs, the user may be required to take corrective actions.

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

English translation of the notice above:
This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

Glossary

This appendix contains important terms used in the preceding chapters. For ease of use, numeric entries are listed first (e.g., “82460GX”) with alpha entries following (e.g., “AGP 4x”). Acronyms are then entered in their respective place, with non-acronyms following.

Word / Acronym	Definition
ACPI	Advanced Configuration and Power Interface
A-D2D	Advanced D2D
ANSI	American National Standards Institute
ASL	ACPI Source Language
BIOS	Basic Input / Output System
BMC	Baseboard Management Controller
CE	Community European
CISPR	International Special Committee on Radio Interference
CMOS	Complementary Metal-Oxide Semi-Conductor
COM	Communications
CPD	Component Data Sheets
CRU	Customer Replaceable Unit
CSA	Canadian Standards Organization
D2D	DC-to-DC converter
DB	Data Bus
dBA	deciBel Acoustic
DDR	Double Data Rate
DIMM	Dual In-Line Memory Module
DMA	Direct Memory Access
DPC	Direct Platform Control
DPS	Distributed Power Supply
DSS	Decision Support System
DT	Double Transition
ECC	Error Checking and Correcting
EEPROM	Electrically Erasable Programmable ROM
EMI	Electromagnetic Interference
EMP	Emergency Management Port
EPS	External Product Specification
ESD	Electro Static Discharge
FCC	Federal Communications Commission
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
FWH	Firmware Hub
GND	Ground
GUI	Graphical User Interface
HDD	Hard Disk Drive
HDM	High Density Metric

Word / Acronym	Definition
HL	Hub-Link
HPC	High Pin Count
HPIB	Hot-Plug Indicator Board
HSC	Hot Swap Controller
I/O	Input / Output
IC	Integrated Circuit
ICH2	I/O Control Hub 2
ICMB	Intelligent Chassis Management Bus
IDE	Integrated Device Electronics
IEC	International Electrotechnical Commission
IMB	Intelligent Management Bus
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
ISA	Industry Standard Architecture
ISP	In System Programmable
ITE	Information Technology Equipment
ITP	In-Target Probe
JAE	Japan Aviation Electronics
JTAG	Joint Test Action Group
LAN	Local Area Network
LED	Light Emitting Diode
LPC	Low Pin Count
LVDS	Low Voltage Differential SCSI
MRH-D	Memory Repeater Hub – DDR
MTBF	Mean Time Between Failures
NIC	Network Interface Card
OEM	Original Equipment Manufacturer
OLTP	On-line Transaction Processing
OS	Operating System
OTP	Over-Temperature Protection
OVP	Over-Voltage Protection
PAL	Programmable Array Logic
PCI	Peripheral Component Interconnect
PDB	Power Distribution Board
PEF	Platform Event Filtering
PEP	Platform Event Paging
PFC	Power Factor Correction
PHP	PCI Hot-Plug
PIROM	Processor Information ROM
PLD	Programmable Logic Device
PSU	Power Supply Unit
PVC	Poly Vinyl Chloride – a plastic
PWM	Pulse Width Modulator
RAID	Redundant Array of Independent Disks

Word / Acronym	Definition
RAS	Reliability, Availability and Serviceability
RH	Relative Humidity
RPM	Revolutions Per Minute
SAF-TE	SCSI Accessed Fault-Tolerant Enclosure
SCA	Single Connector Attachment
SCL	Serial Clock
SCSI	Small Computer Systems Interface
SDA	Serial Data
SDINT	System Diagnostic Interrupt
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic RAM
SE	Single Ended
SEEPROM	Serial Electrically Erasable Programmable Read Only Memory
SEL	System Event Log
SIOH	Server I/O Hub
SMB	Server Management Bus
SMP	Symmetric Multiprocessing
SNC-M	Scalable Node Controller – McKinley
SSI	Server System Infrastructure
TTL	Transistor-Transistor Logic
USB	Universal Serial Bus
UV	Under-Voltage
VAC	Alternating current (AC) voltage
VCC	Voltage Controlled Current
VCCI	Voluntary Control Council for Interference by Information Technology Equipment
VGA	Video Graphics Array
VID	Voltage ID
VSB	Voltage StandBy
WfM	Wired For Management
ZIF	Zero Insertion Force

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