Intel® Server System SR9000MK4U

Technical Product Specification

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Enterprise Platforms and Services Division - Marketing

Revision History

Version	Revised Date	Description
1.0	November , 2006	Document released
1.1	November, 2006	Updated Appendix A

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1. Introduction

This Technical Product Specification (TPS) provides system-specific information about the features, functionality, and high-level architecture of the Intel® Server System SR9000MK4U.

1.1 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel-developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. System Overview

The Intel® Server System SR9000MK4U is a compact, high-density rack-mount server system that supports four Intel® Itanium® 2 Processor 9000 series and up to 256-GB DDR2 SDRAM memory. The system uses the Hitachi* CF-3e chipset.

The system features:

- Hot-plug PCI-X* and PCI Express* add-in cards
- Hot-swap, redundant power supply modules
- Hot-swap redundant cooling fans
- Hot-swap hard drives

The system supports symmetric multiprocessing (SMP).

Table 1. Intel® Server System SR9000MK4U

Feature	Description
Processors	Four mPGA700 sockets support Intel® Itanium® 2 Processor 9000 series with system bus speeds of 533 MHz and 667 MHz.
Memory	Up to 32 DIMM sockets (eight sockets per memory box) support DDR2 memory technology. It supports 240-pin DDR2-533 and DDR2-667 Registered ECC DIMMs for up to 256 GB total system memory. DIMMs must contain x4 bit DRAMs and be populated in sets of four.
Chipset	Hitachi* Cold Fusion-3e
On-board Connectors / Headers	▪ Mini D-sub 15-pin VGA port (Rear) ▪ RS-232 D-sub 9-pin Serial Port (Rear) ▪ Two RJ45 for 10 / 100 / 1000 Mb (Rear) ▪ Two RJ45 10 / 100 ports (Ether0: Management, Ether1: KVM) (Rear) ▪ Four USB 2.0 ports (Rear) ▪ Two USB 1.1 ports (Front) ▪ One ATA100 40-pin connector ▪ One SFF-8484 SAS x4 connector ▪ One KVM connector supports an optional KVM module ▪ Two 12-pin processor power connectors ▪ One debug connector
Add-in PCI Express* and PCI-X* cards	▪ Two hot-swap full-height PCI Express* x16 slots ▪ One hot-swap full-height PCI Express x8 slot ▪ One hot-swap full-height PCI Express x8 slot (with PCI Express x4 bandwidth) ▪ Two hot-swap full-height PCI-X* 64-bit slot with up to 133-MHz support
Video	On-board ATI* ES1000 video controller with 64 MB DDR SDRAM
Hard Drive Bays	Support for eight hot-swap SAS hard drives Slimline drive bay, populated with DVD/CD RW COMBO Drive (TEAC* DW-224E-R76)
LAN	10/100/1000 Intel® 82563 PHY (dual port) 10/100 Intel® 82551QM Fast Ethernet Controller (single port)
Fans	▪ 5+1 front hot-swap fans ▪ Two rear power supply fans
Power Supply	Two 1390-watt power supplies supporting 100-127 V or 200-240 V. Supports power supply redundancy in certain configurations
Form Factor (WxDxH)	441 mm x 765 mm x 176 mm
Weight (approx.)	28 kg
Server Management	Onboard baseboard management controller (BMC), based on IPMI 2.0. Supports ServerConductor software

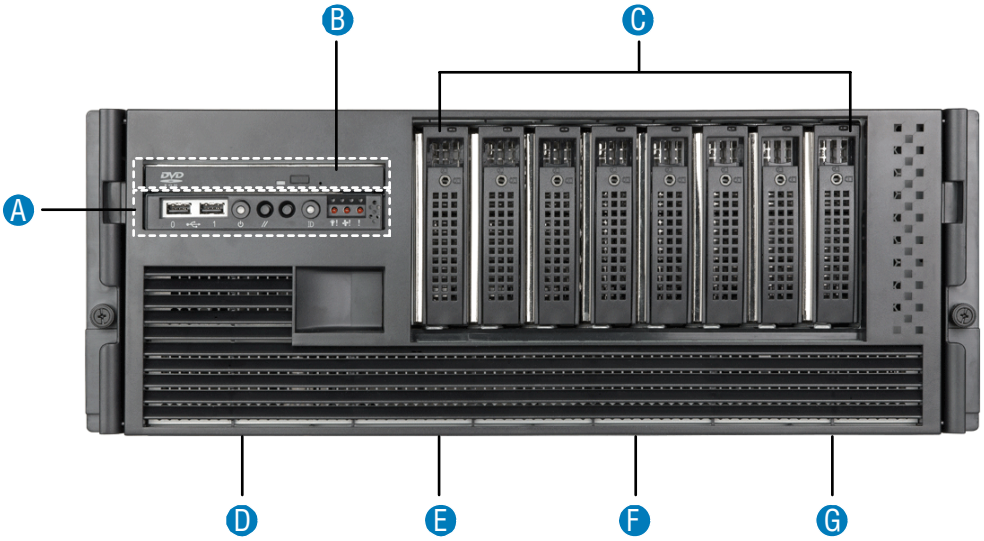
2.1 Physical Specifications

Characteristic	Specification
Height	176 mm (6.9 inches)
Width	441 mm (17.3 inches)
Depth	765 mm (30.1 inches)
Weight	Base: 21 kg (46.3 pounds) Maximum: 48 kg (105.8 pounds)
Heat dissipation	1390 watt

Figure 1. Physical Characteristics

2.2 Chassis Front

The figure below shows the front of the chassis with the snap-on bezel in place. The bezel provides access to the optical drive, front panel controls, and the hot-swap hard drives. The bezel must be removed to access the memory boxes.



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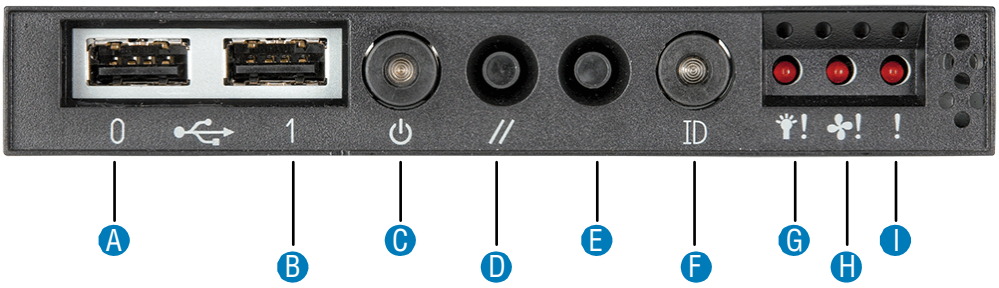
A. Front panel	E. Memory box 1
B. Optical drive	F. Memory box 2
C. Hard drives (HDD0 – HDD7, from left to right)	G. Memory box 3
D. Memory box 0	

Figure 2. Server System Front View

2.3 Front Panel

The front panel is below the slimline optical drive on the left side of the chassis front. The front panel provides buttons and status indicator LEDs.



A. USB port 0, USB 1.1	F. Identification button and blue ID LED
B. USB port 1, USB 1.1	G. Power fault LED
C. Power button and power LED	H. Cooling fault LED
D. Reset button	I. General fault LED
E. System diagnostic interrupt (SDINT) button	

Figure 3. Front Panel Controls and Indicators

2.3.1 Optical Drive Bay

The slimline optical drive (DVD-ROM / CD-ROM drive) is inserted from the front of the optical drive bay. The system power must be turned off to remove or install this drive.

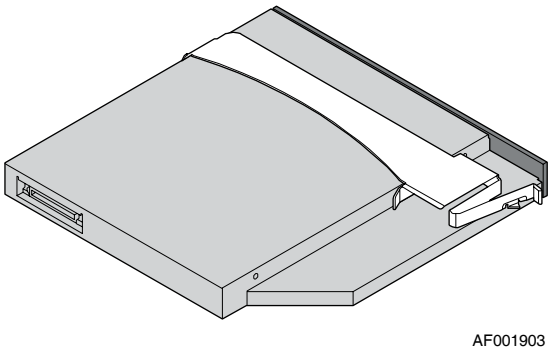


Figure 4. Optical Drive Bracket with Drive Installed

Note: *Intel validates specific DVD-ROM / CD-ROM drives. See the* Intel® Server System SR9000MK4U Tested Hardware and Operating System List *for a list of drives.*

2.3.2 Hot-swap Hard Drive Bay

The hot-swap hard drive carrier supports 15,000-RPM or slower SAS3G technology hard drives.

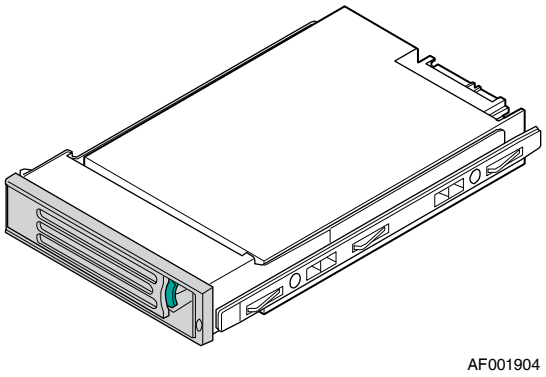


Figure 5. Hard Drive Carrier

The hard drive carriers contain light-pipes that allow dual-color LED indicators to display through the bezel.

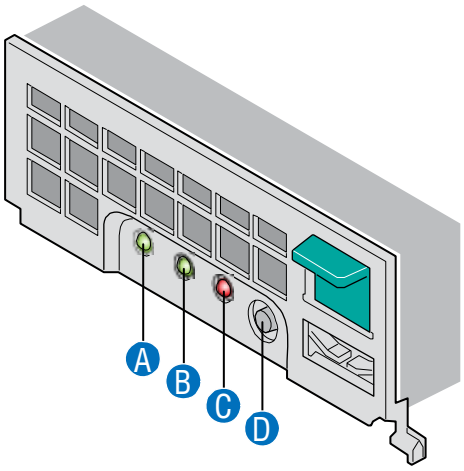
Table 2. Hard Drive LEDs

LED Color	State	Description
Green	On	Activity
	4 Hz blink	Locate
	1 Hz blink	Rebuild
Red	On	Error
Red / Green / Off	Blink	Hard drive insert Power on reset with or without hard drive

Note: *Intel validates specific hard drive types in the Server System SR9000MK4U. See the* Intel® Server System SR9000MK4U Tested Hardware and Operating System List *for a list of drives.*

2.3.3 Memory Box

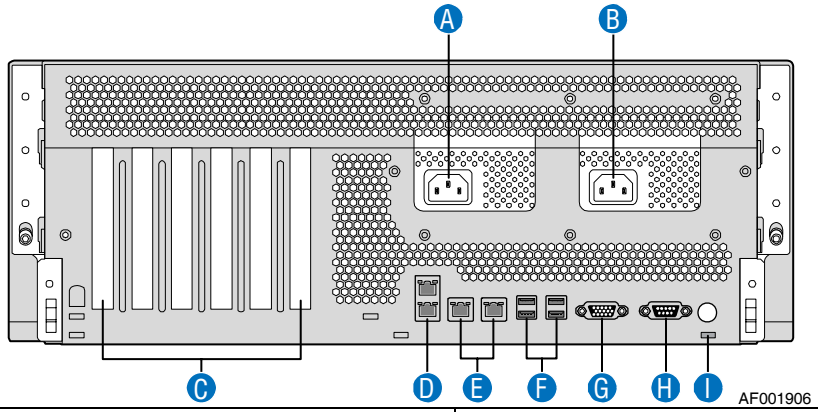
The server system supports up to four memory boxes (MMR). The memory boxes are accessible from the front of the system. When operating in mirror mode, the memory boxes support hot-swapping.



Callout	LED	LED State	Description
A	Memory Box Mirror LED	Green on	The memory box is operating in mirror mode.
		Off	The memory box is not operating in mirror mode.
B	Memory Box Power LED	Green on	The memory box is powered on.
		Off	The memory box is powered off.
C	Memory Box Attention LED	Orange on	An error has been detected in the memory box.
		Off	No error has been detected in the memory box or the memory box is powered off.
D	No LED	N/A	Hot-swap button. Press this button to initiate a hot-swap process.

Figure 6. Memory Box

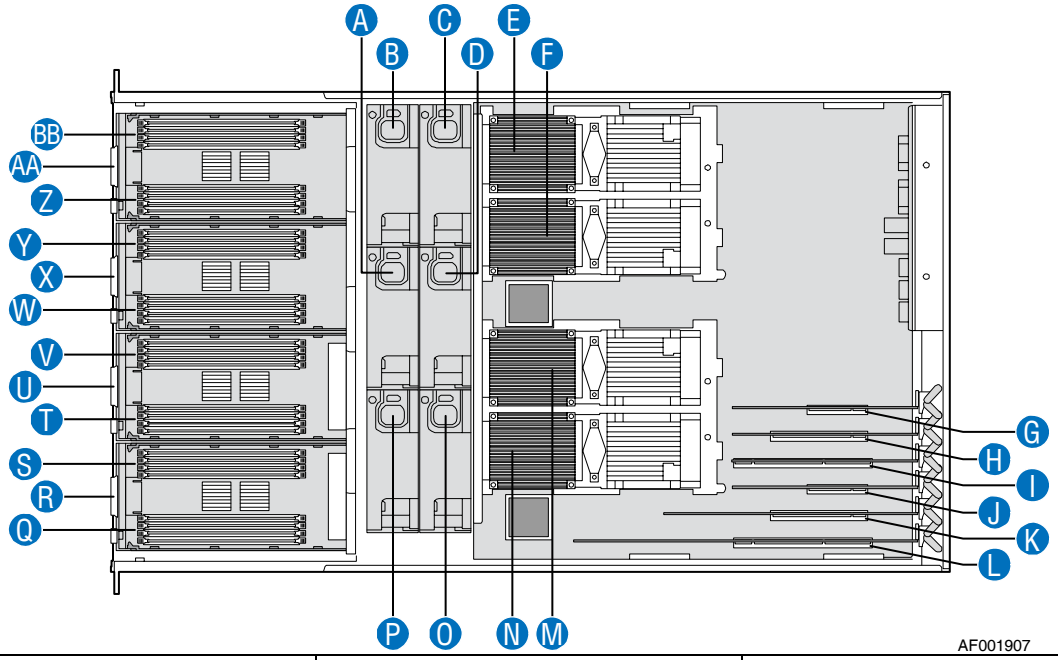
2.4 Chassis Rear



A	AC input power connector	
B	AC input power connector	
C	PCI slots	All slots support hot-plug PCI add-in cards. From left to right: ▪ Slot 6: 133 MHz, 64-bit PCI-X, full length ▪ Slot 5: PCI Express* x16, half-length ▪ Slot 4: PCI Express x8, half-length ▪ Slot 3: PCI-X* 133 MHZ, 64-bit, half length ▪ Slot 2: PCI Express x8, half-length
D	Dual Gb Ethernet ports	RJ45 connectors: ▪ GbE1: top ▪ GbE2: bottom
E	100 Mb Ethernet ports	RJ45 connectors: ▪ Ether0: left. Management LAN port ▪ Ether1: right. KVM LAN port
F	Four USB ports	4-pin connectors: ▪ Top left: RUSB3 ▪ Bottom left: RUSB2 ▪ Top right: RUSB1 ▪ Bottom right: RUSB0
G	Video port	Standard VGA compatible, 15-pin connector
H	Serial port	9-pin RS-232 connector
I	Identification button	Toggles chassis ID LED on/off

Figure 7. Chassis Rear View

2.5 Internal Chassis Features



A. System fan 2	K. PCI Express* x16, slot 5	U. Memory box 2
B. System fan 0	L. PCI-X* slot 6	V. DIMM sockets
C. System fan 1	M. Processor 2	W. DIMM sockets
D. System fan 3	N. Processor 3	X. Memory box 1
E. Processor 0	O. System fan 5	Y. DIMM sockets
F. Processor 1	P. System fan 4	Z. DIMM sockets
G. PCI Express x8, slot 1	Q. DIMM sockets	AA. Memory box 0
H. PCI Express x16, slot 2	R. Memory box 3	BB. DIMM sockets
I. PCI-X slot 3	S. DIMM sockets	
J. PCI Express x8, slot 4	T. DIMM sockets	

Figure 8. Open System, Top View

2.5.1 Power Supply Subsystem

The 12 V hot-swap power supply modules are rated at 1390 watts over an input range of 200-240 VAC, and at 990 watts over an input range of 100-127 VAC. The power supply module has +12 V and +5 Vsb outputs. The standby voltage, +5 Vsb, is active whenever AC input power is applied to the power supply.

The power supply module is connected directly to the server board and can be used in 1+1 redundant mode. Two power supplies must be installed and plugged in when a 110 V outlet is used. Hot-swapping is not available when 110 V is used.

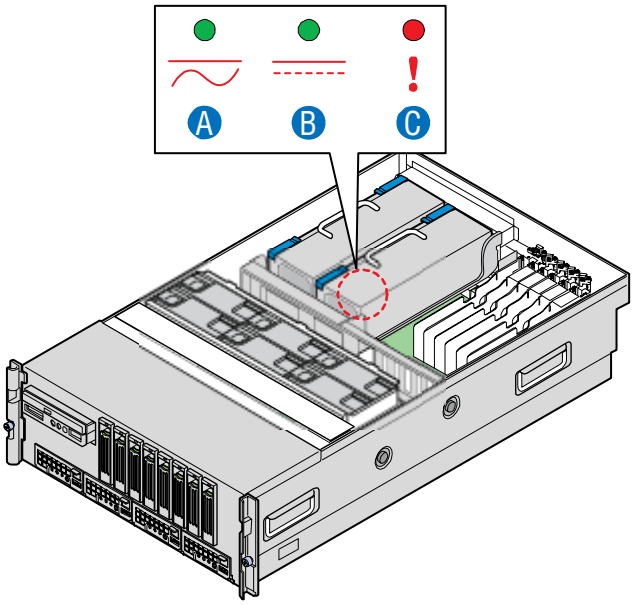
One power supply can be used when it is connected to a 220 V outlet.

Table 3. 1390 Watt Power Supply Configuration

AC Input	Current (see note)	Redundancy	Hot-swap	Remarks
200-240 VAC	9.5 A	Supported	Supported	Loading is restricted. Two power supplies must be installed to enable redundancy and hot-swap.
100-127 VAC	12 A	Not supported	Not supported	Loading is restricted. Two power supplies must be installed and plugged in.

Note: The current value is applied to one power supply.

Each power supply has three LEDs on the top.



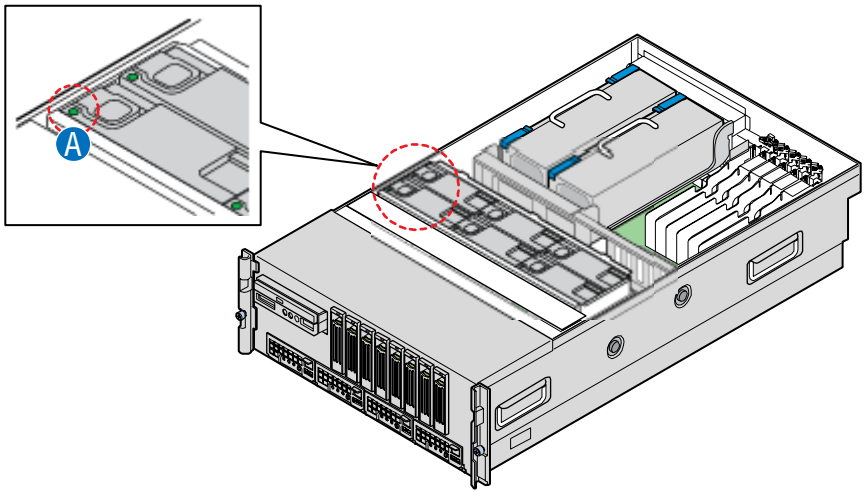
A. Input Good LED	Indicates the power is good when this green LED is on.
B. DC Output Good LED	Indicates the output power us good when this green LED is on.
C. Fault LED	Indicates a fault with the power supply when this red LED is on.

Figure 9. Power Supply LEDs

2.5.2 Cooling Subsystem

The server system is cooled with six 120 mm x 38 mm hot-swappable, 5+1 redundant fans. These fans provide sufficient airflow to cool the system components, processors, memory and chipset, even if one of the six fans fails.

Caution: *The chassis top cover must be installed for proper system cooling. Cooling fans should be hot-swapped within two minutes. This time period applies only to the time that the cooling fan is physically removed from the system, not from the time of failure.*

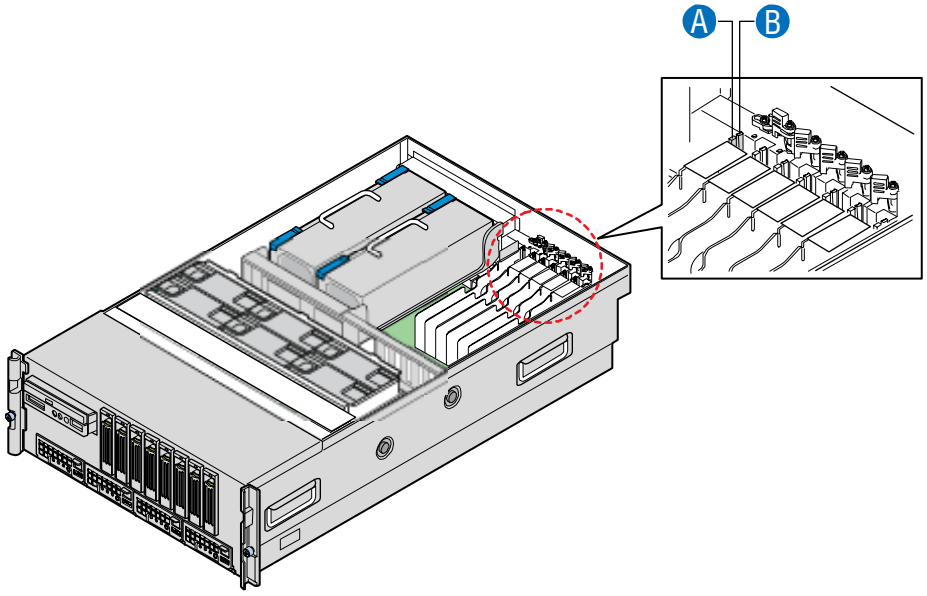


A. Cooling Fan LED	Indicates fan is working normally when the green LED is on. Indicates a fan fault when the LED is off.

Figure 10. Fan Fault LED

2.5.3 PCI Card Slots

Six PCI expansion slots are available. Each slot is equipped with an LED to indicate power and faults.



A. Power LED	Indicates PCI slot status is active.
B. Attention LED and lens switch	Indicates an error when this yellow LED is on. The lens switch is used for hot installs / removes.

Figure 11. PCI Slot LEDs

3. Functional Architecture

The board set consists of a main board, four memory box boards (installed in the memory boxes), a hard drive backplane, and a front panel board. In the block diagram, the circled numbers indicate connection points between the main board and the system boards.

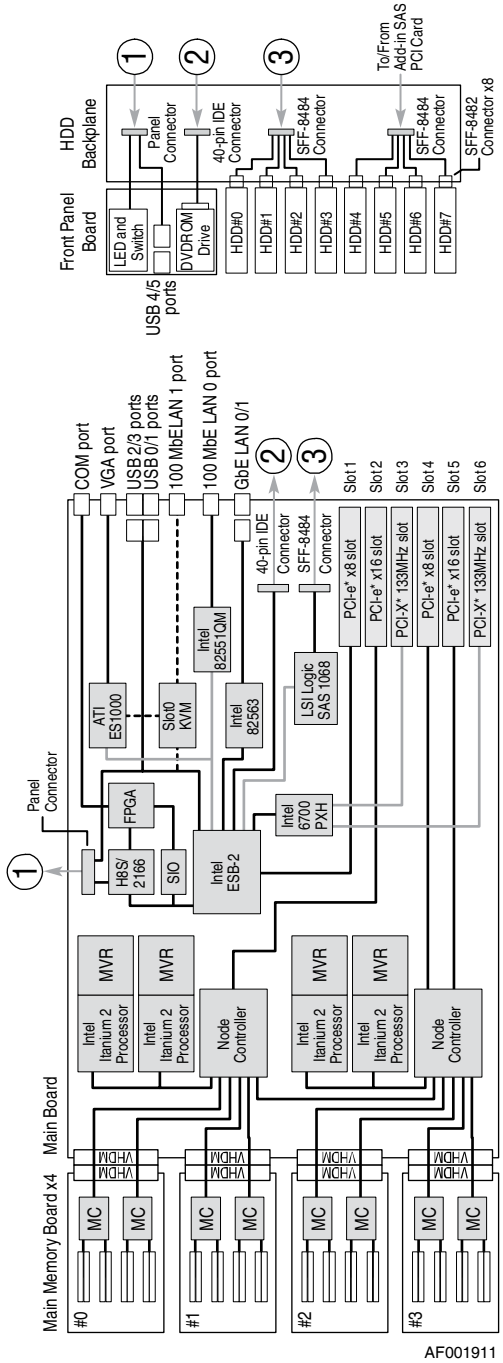


Figure 12. Server System Block Diagram

Name of Bus	Throughput	Qty	Description
Processor Bus (FSB BUS)	8.5 GB/sec (128-bit) at 533 MHz	2	Two Intel® Itanium® 2 Processor 9000 series per bus
NDC–NDC Bus	17 GB/sec (128-bit)	1	Node controller to node controller uni-directional link x2
NDC-MC Bus	2.1 GB/sec (32-bit)	8	4 MCs/NDC 2 NDCs/System
DIMM Bus	4.3 GB/sec (64-bit)	16	2 DIMM Buses/MC 4 MCs/NDC 2 NDCs/System
PCI Express* x16 links	8 GB/sec	2	
PCI Express x8 links	4 GB/sec	2	The slot connected to the ESB2 has performance equivalent to x 4.
PCI-X*	1 GB/sec	2	133 MHz
USB Port	1.5 Mbps / 12 Mbps / 480 Mbps	6	USB2.0 to rear connection/ USB1.1 to front connection

4. Server Board

The architecture and design of the server system utilizes the Hitachi* CF-3e chipset based on the Intel® Itanium® 2 Processor 9000 series with system bus speeds of 533 MHz or 667 MHz.

The chipset contains three main components:

- Two node controllers (NDC)
- The memory controllers in each of the memory boxes (MMR)
- The Intel® Enterprise South Bridge (ESB2).

The NDCs connect to the Enterprise South Bridge to control the system I/O. This section provides a high-level description of the functionality associated with each main server system component.

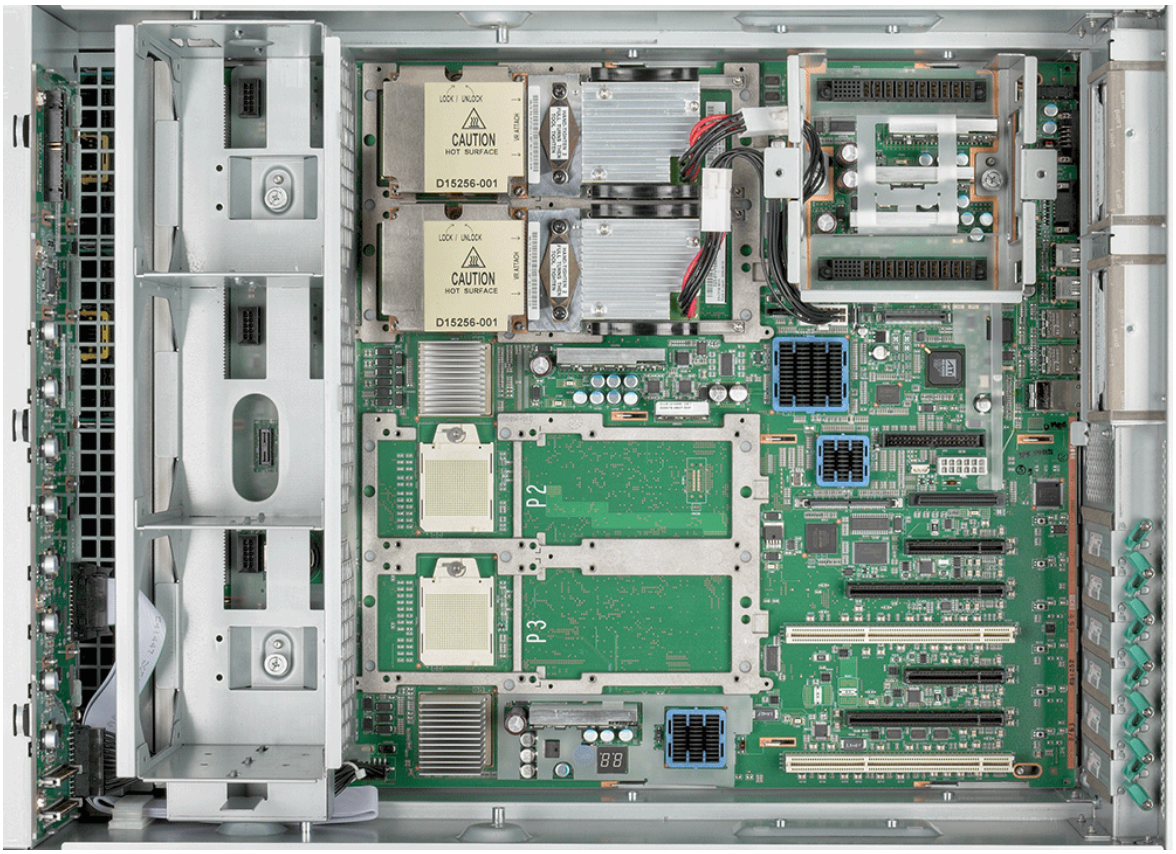


Figure 13. System Interior

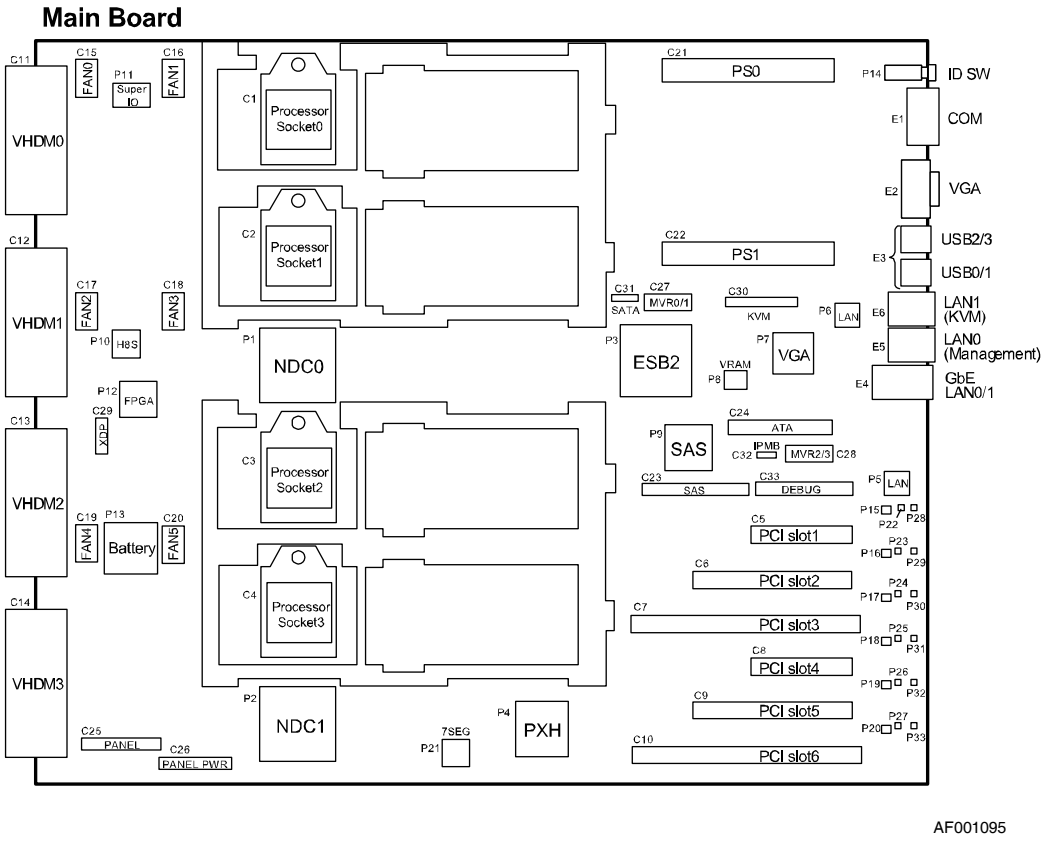


Figure 14. Main Board Layout

Table 4. Main Board Components

Board Location	Component	Description
P1/P2	Hitachi* NDC	Node Controller ▪ One Front Side Bus ▪ 533/667 MHz FSB support ▪ Two processors per bus ▪ Four interfaces connecting to the memory controller ▪ Three x8 PCI Express* ports ▪ Proprietary high-speed interface to link between two node controllers ▪ Optimized design for 667 MHz FSB to achieve low memory access latency ▪ Broadcast-based cache coherence control to minimize snoop transaction
P3	Intel® ESB2	Enterprise South Bridge

Board Location	Component	Description
P4	Intel® 6700PXH	64-bit PCI Hub: ▪ PCI bridging functions between the PCI Express* interface and the PCI bus ▪ One PCI Express interface (primary bus) ▪ x8 and x4 modes operation ▪ Maximum 2 GB/s in each direction simultaneously ▪ Two PCI / PCI-X* bus interfaces (secondary bus) ▪ PCI 2.3-compliant ▪ PCI-X 1.0 b-compliant
P5	Intel® 82563	Physical Layer Transceiver (PHY) component for 10/100/1000 Mbps operation ▪ IEEE 802.3 (10BASE-T), IEEE 802.3u (100BASE-TX), IEEE 802.3ab (1000BASE-T) ▪ Dual port
P6	Intel® 82551QM	Fast Ethernet PCI bus controller: ▪ IEEE 802.3 (10BASE-T), IEEE 802.3u (100BASE-TX), 32-bit PCI bus master interface
P7	ATI* ES1000	Graphics processing unit: ▪ 2D graphics accelerator ▪ PCI bus interface (PCI 2.2-compliant, 33 MHz)
P8	VRAM	64 MB VRAM for ATI* ES1000: ▪ Max resolution: Up to 1280 x 1024, 85 Hz ▪ Max color depth: Up to 32 bpp true color
P9	LSI Logic* SAS1068	PCI-X* to 3 Gb/s 8-port SAS controller. Four of the eight ports are used. ▪ 1.5 and 3 Gb/s SAS and SATA data transfer rates per port, full duplex ▪ 64-bit, 133 MHz PCI-X host interface ▪ Integrated RAID support ▪ Fusion-MPT* architecture ▪ Integrated Striping* technology (RAID0) ▪ Integrated Mirroring* technology (RAID1)
P10	H8S/2166	Baseboard management controller (BMC)
P11	SIO	Super I/O
P12	FPGA	Management interface and shared memory extension bridge
P13	Battery	CMOS backup
P14	ID SW	A button / LED combination that identifies a system. The first time the button is pressed, the LED turns on. If the button is pressed again, the LED blinks and turns off.
P15-P20	PCI-X / PCI Express* slot Attention SW	Attention switch used for swapping PCI cards
P21	7SEG LED	Indicates POST code
P22-P27	PCI-X / PCI Express* slot Power LED	LED to indicate an active PCI slot
P28-P33	PCI-X PCI Express slot Attention LED	LED to indicate an error other than a PCI slot condition

Table 5. Main Board External I/O Connectors

Board Location	Connector	Description
E1	Serial	RS232C D-sub 9-pin serial port
E2	VGA	Mini D-sub 15-pin video port
E3	USB 0/1/2/3	USB Type A port x4
E4	GbE LAN 0/1	RJ45 LAN port x2
E5	100 MbE LAN	RJ45 LAN port x1
E6	100 MbE LAN	Rj45 LAN port x1 (for KVM)

Table 6. Main Board Internal I/O Connectors

Board Location	Connector	Description
C1~C4	CPU 0/1/2/3	mPGA700 ZIF sockets
C5/C8	PCI slot 1/4	x8 PCI Express* slots
C6/C9	PCI slot 2/5	x16 PCI Express slots
C7/C10	PCI slot 3/6	64-bit 133 MHz PCI-X* slots
C11~C14	VHDM 0/1/2/3	
C15~C20	FAN 0/1/2/3/4/5	
C21/C22	PS 0/1	
C23	SAS	SFF-8484 (SAS internal x4 connector)
C24	ATA	40-pin IDE connector
C25	PNL	
C26	PNLPW	
C27/C28	MVR0/1, MVR2/3	
C29	XDP	
C30	KVM	
C31	SATA	
C32	IPMB	
C33	DEBUG	

4.1 Node Controller

The two system node controllers provide the primary interface between the processors, memory, and the system I/O. The node controllers include these core platform features:

- Front side bus with 533/667 MHz support
- Controls the system interface between the four processors and eight memory controllers
- PCI Express* ports including the Enterprise South Bridge Interface (ESI)
- Broadcast-based cache coherence control to minimize snoop transaction

4.1.1 System Bus Interface

The node controllers (NDCs) communicate across a front side bus interface that connects to the Intel® Itanium® 2 Processor 9000 series. The front side bus on the NDCs uses a 128-bit wide 533-Mhz or 667-Mhz data bus. The 533-MHz data bus is capable of transferring data at up to 8.5 GB/s. The NDCs each support four 32-bit wide buses, capable of addressing a total of 256 GB of memory.

4.1.2 Processor Support

The server system supports up to four Intel® Itanium® 2 Processor 9000 series, with system bus speeds of 533 MHz and 667 MHz and core frequencies starting at 1.42 GHz. Previous generations of the Intel® Itanium® 2 processor are not supported.

Note: *Only Intel® Itanium® 2 Processor 9000 series that support system bus speeds of 533 MHz and 667 MHz are supported in this server system.*

Table 7. Supported Processors

Processor Name	Processor #	Frequency		L3 Cache	Core	Power (TDP)
		Core	FSB			
Intel® Itanium® 2	9010	1.6 GHz	533	6 MB	1	75 W
Dual-Core Intel® Itanium® 2	9020	1.42 GHz	533	12 MB	2	104 W
	9030	1.6 GHz	533	8 MB	2	104 W
	9040	1.6 GHZ	533	18 MB	2	104 W
	9050	1.60 GHz	533	24 MB	2	104 W

4.1.3 Processor Installation Rules

All installed processors must be of identical revision, core voltage, and bus/core speed. When only one processor is installed, it must be in the socket labeled P0. No terminator is required in the empty processor sockets.

For instructions on installing and removing the processors, see the *Intel® Server System SR9000MK4U Product Guide.*

Table 8. Supported Processor Socket Configurations

Socket 0	Socket 1	Socket 2	Socket 3
Installed	Not Installed	Not Installed	Not Installed
Installed	Installed	Not Installed	Not Installed
Installed	Not Installed	Installed	Not Installed
Installed	Installed	Installed	Not Installed
Installed	Installed	Installed	Installed

4.2 Enterprise South Bridge (ESB2)

The Intel® ESB2-E is a multi-function device that provides four distinct functions: an I/O controller, a PCI-X* bridge, a GB Ethernet controller, and a baseboard management controller (BMC). Each function has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller.

The ESB2-E provides the gateway to all PC-compatible I/O devices and features. The server system uses these ESB2-E features:

- PCI-X* bus interface
- Dual GbE MAC
- Baseboard management controller (BMC)
- Single ATA interface, with Ultra DMA 100 capability
- Universal Serial Bus 2.0 (USB) interface
- Removable media drives
- LPC bus interface
- PC-compatible timer/counter and DMA controllers
- APIC and 8259 interrupt controller
- Power management
- System RTC
- General purpose I/O

4.2.1 PCI Express* / PCI-X* Card Slot

4.2.1.1 PCI Card Slot Specification

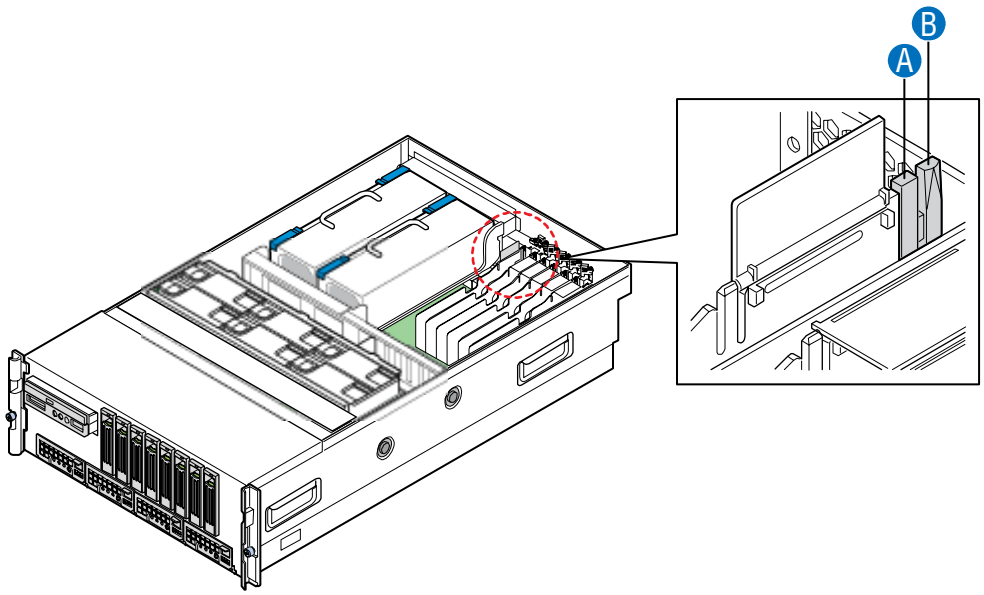
The primary I/O buses for the server board are PCI Express* and PCI-X* with six independent PCI bus segments. The PCI buses comply with the *PCI Local Bus Specification*, Revision 2.3.

Table 9. PCI Slot Specification

Slot #	Specification	Slot Restriction
Slot 1	PCI Express* X8	Short card slot (Length = 167.65mm) Hot-pluggable
Slot 2	PCI Express* X16	Short card slot (Length = 167.65mm) Hot-pluggable
Slot 3	PCI-X* (64-bit)133 MHz	Short card slot (Length = 167.64mm) Hot-pluggable
Slot 4	PCI Express* X8	Short card slot (Length = 167.65mm) Hot-pluggable
Slot 5	PCI Express* X16	240L card slot (Length = 240.00mm) Hot-pluggable
Slot 6	PCI-X* (64-bit) 133 MHz	Long card slot (Length = 312.00mm) Hot-pluggable

4.2.1.2 PCI Hot Swap

The server system supports hot swapping PCI adapter cards. Only PCI cards with one PCI-to-PCI bridge can be hot-swapped. Attention LEDs are on the server board at the rear of the chassis. If an error occurs these LEDs blink amber. A lever operates a push button on the server board to activate the hot swap procedure. See the *Intel® Server System SR9000MK4U Product Guide* for instructions to hot-swap a PCI card.



LED	Off	On (Solid)	Blinking
Power LED	All main voltage and data rails are removed from slot. PCI adapter may be added or removed	Normal power to slot. PCI adapter may NOT be added or removed	Slot power in transition (on-off or off-on). PCI adapter may NOT be added or removed
Attention LED	Normal operation	Slot on attention; power fault or operational problem present on the slot	Error has occurred

Figure 15. Lens Switch and PCI Card LED

4.2.2 Parallel ATA (PATA) Support

The integrated IDE controller of the ESB2-E ICH6 provides one IDE channel. It redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 100 MB/s. The IDE channel provides optical drive support. The SAL initializes and supports ATAPI devices such as LS-120/240, CD-ROM, CD-RW and DVD-ROM. The IDE channel is accessed through a single standard 40-pin IDE connector that provides the I/O signals.

4.2.3 USB 2.0 / USB 1.1 Support

The USB controller functionality integrated into ESB2-E can provide the server board with the interface for up to eight USB 2.0 ports. The server system has six USB ports. Four external USB 2.0 connectors are located on the back edge of the server board. Two external USB 1.1 connectors at the front of the chassis.

4.3 Video Support

The server board provides an ATI* ES1000 PCI graphics accelerator and 64 MB of video DDR SDRAM and support circuitry for an embedded SVGA video sub-system. The ATI ES1000 chip contains an SVGA video controller, clock generator, 2D engine, and RAMDAC in a 359-pin BGA.

The SVGA sub-system supports modes up to 1024 x 768 resolution in 8 / 16 / 32 bpp modes under 2D. It supports both CRT and LCD monitors up to a 100 Hz vertical refresh rate.

Video is accessed using a standard 15-pin VGA connector found on the back edge of the server board.

4.3.1 Video Modes

The ATI* ES1000 chip supports all standard IBM* VGA modes. The following table shows the 2D modes supported for both CRT and LCD.

Table 10. Video Modes

2D Mode	Refresh Rate (Hz)	2D Video Mode Support		
		8 bpp	16 bpp	32 bpp
640x480	60, 72, 75, 85, 90, 100, 120, 160, 200	Supported	Supported	Supported
800x600	60, 70, 72, 75, 85, 90, 100, 120, 160	Supported	Supported	Supported
1024x768	60, 70, 72, 75, 85, 90, 100	Supported	Supported	Supported
1152x864	43, 47, 60, 70, 75, 80, 85	Supported	Supported	Supported
1280x1024	60, 70, 74, 75	Supported	Supported	Supported

4.3.2 Video Memory Interface

The memory controller sub-system of the ES1000 arbitrates requests from the direct memory interface, the VGA graphics controller, the drawing co-processor, the display controller, the video scalar, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/co-processor drawing performance.

The server board supports a 64 MB DDR SDRAM device for video memory.

4.4 SAS Controller

The SAS1068 controller connects to the ESB2 through a PCI-X* link and supports the SAS protocol as described in the Serial Attached SCSI Standard, version 1.0. The controller supports SAS 1.1 features and a 32-bit external memory bus that provides an interface for Flash ROM and NVSRAM devices.

4.4.1 SAS RAID Support

RAID modes 0, 1, and 1E are supported.

4.5 Network Interface Controller (NIC)

There are two sources of network interface support: the Intel® 82563EB and the Intel® 82551QM. The primary source is provided from the built in Dual GbE MAC features of the ESB2 in conjunction with the Intel® 82563EB compact Physical Layer Transceiver (PHY). Together, they support dual LAN ports designed for 10/100/1000 Mbps operation.

The 82563EB device is based upon proven PHY technology integrated into Intel's gigabit Ethernet controllers. The physical layer circuitry provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The 82563EB device can transmit and receive data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps.

The secondary source is provided from the Intel® 82551QM Fast Ethernet PCI bus controller. This controller provides an interface for IEEE 802.3 (10BASE-T), IEEE 802.3u (100BASE-TX) through a 32-bit PCI bus master interface. The 82551QM can transmit and receive data at 100 Mbps or 10 Mbps. The controller is connected to one port intended for server management.

Each network interface controller (NIC) drives two LEDs located on each network interface connector.

Table 11. NIC LEDs

Item	LED	Color	State	Description
Gigabit Ether, ports GbE1 and GbE2	Activity / Link (right LED)	Green	On	Link
		Green	Blink	Active
		None	Off	No link
	Speed (left LED)	Yellow	On	1000
		Green	On	100
		None	Off	10
Fast Ether (Management LAN, KVM LAN), ports Ether0 and Ether1	Activity / Link (right LED)	Green	On	Link
		Green	Blink	Active
		None	Off	No link
	Speed (left LED)	Green	On	100
		None	Off	10

4.5.1 MAC Address Definition

Each Intel® Server System SR9000MK4U has three MAC addresses. Two are assigned to the ESB2 gigabit Ethernet ports and one is assigned to the management LAN port.

4.6 Debug Connector

This connector is for internal testing only.

4.7 KVM (Keyboard, Video, Mouse) (Optional Accessory)

TBD

Figure 16. KVM Card

The KVM card is an optional accessory.

Table 12. Remote KVM Card Specifications

Item	Specification		
Key features	Video Redirection	Input: standard DVO (1024x768, 24bit color) Output: Original protocol on TCP/IP LAN	
	Remote Keyboard	USB Keyboard (101 Keyboard) emulation	
	Remote Mouse	USB Mouse (2-botton mouse) emulation	
	Remote Storage	Remote FDD	USB FDD (1.4 MB) emulation
		Remote CD-ROM	USB CD-ROM emulation (Future support)
	IPMB	IPMI 1.5 IPMB to communicate with the BMC (IPMI 1.5 or higher)	
Key components	Micro Processor	Renesas SH-4 (HD6417751R) 200MHz 16 KB instruction cache, 32 KB operand cache	
	Main memory	ELPIDA SDRAM 32 MB	
	FLASH ROM (F/W)	Spansion FLASH ROM 16 MB)	
	Video capture FPGA	ALTERA EP1C6F256	
	LAN controller	Intel 82551QM	
	USB controller	Renesas* M66291 x 3 pieces	
	I2C controller	Philips* PCA9564	
Security	Login	Password security (User ID, password) CHAP (key length: 128-bit)	
	Fire Wall	IP address filtering	
		TCP port filtering	
Form Factor	Card size	70 mm x 60 mm	
	Connector	DFJ 80-pin connector (plug type)	

Table 13. Remote KVM Card Interface Specifications

Item	Specification				
Interface	LAN	Physical layer	IEEE 802.3 (100Base-TX, 10Base-T, auto-negotiation)		
		Protocol	TCP/IP: TCP destination port: 5001(default)		
		MAC address	00-00-87-xx-xx-xx (Vendor ID)		
	USB	USB specification 1.1 conformed			
		USB ID	Device	Vendor ID	Product ID
			USB Keyboard/Mouse	04A4h	005Ch
			USB FDD	04A4h	005Dh
			USB CD-ROM	04A4h	005Eh
	I2C	IPMI over LAN (82551QM)	Operating frequency	Standard mode（max 100 kHz）	
			Slave I2C address	CAh	
			Protocol	Intel82551QM spec conformed	
			Voltage Level	3.3V interface Clock, data, alert signal with 1 kohm pull-up register on KMV card	
		IPMB (PCA9564)	Operating frequency	Fast mode, max 400 KHz	
			Slave I2C address	30 h	
			Destination BMC address	20 h (default)	
			Protocol	IPMI specification 1.5	
			Voltage Level	3.3V interface (No pull-up register on KMV card	
	DVO	Support Screen	Resolution	1024 dot x 768 dot	
			Refresh rate	60 Hz	
			Color	(TBD)	
			Voltage Level	3.3V LVTTL	

5. Memory Box

The server system supports up to four memory boxes (MMR). Each MMR has eight DIMM sockets for a total of 32 sockets per system. The memory boxes are accessible from the front of the system. When operating in mirror-mode, the MMRs support hot-swapping.

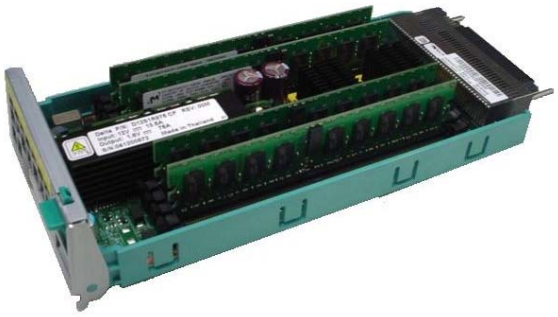
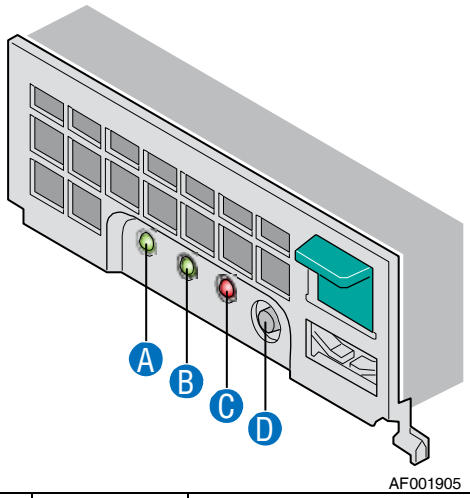


Figure 17. Memory Box

5.1 Memory Box LEDs



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A. Memory Box Mirror LED	Green on	The memory box is operating in mirror mode
	Off	The memory box is not operating in mirror mode
B. Memory Box Power LED	Green on	The memory box is powered on.
	Off	The memory box is powered off
C. Memory Box Attention LED	Orange on	An error has been detected in the memory box
	Off	No error has been detected on the memory box, or the memory box is powered off.
D. Memory Box Hot Swap Button		Press button to initiate memory box hot swap.

Figure 18. Memory Box Front View

5.2 Supported Memory Types

A minimum of four DDR2 533 or 667 MHz 512 MB Registered ECC DIMMs must be installed in each memory box to power on the system. All DIMMs must contain x4 bit DRAMs.

Table 14. Supported DIMM Module Types

Capacity / Module	Capacity / 1 Rank	Rank	Bank Qty	Row Adr	Column Adr	Chip Type	Frequency
512 MB	512 MB	1	4	14-bit	11-bit	256 Mb x4 type	533 Mbps is supported. 667 Mbps is supported
1 GB	512 MB	2	4	14-bit	11-bit	256 Mb x4 type	
1 GB	1 GB	1	4	14-bit	12-bit	512 Mb x4 type	
2 GB	1 GB	2	4	14-bit	12-bit	512 Mb x4 type	
2 GB	2 GB	1	8	14-bit	12-bit	1 Gb x4 type	
4 GB	2 GB	2	8	14-bit	12-bit	1 Gb x4 type	
4 GB	4 GB	1	8	15-bit	12-bit	2 Gb x4 type	
8 GB	4 GB	2	8	15-bit	12-bit	2 Gb x4 type	

***Note**: See the tested memory list for the part numbers of validated DIMMs.*

Table 15. DIMM I/F Frequencies and Latency

Operational FSB Frequency	DIMM Type		
	DIMM Frequency	DRAM Type	Speed Bin See Note
667 MHz	667 Mbps (CLK333 MHz)	DDR2-667	5-5-5
533 MHz	533 Mbps (CLK266 MHz)	DDR2-533	4-4-4

Note: Speed Bin=>CL-tRCD-tRP. As a DIMM type, a speed bin should be equal to or faster than the above table. “faster” means that each parameter in the speed bin is less than the value in the above table.

5.3 Memory Population Rules

The server system supports up to 32 DIMM modules. The DIMM modules are divided as follows: each system has two NDCs, each NDC can support up to four memory controllers (MC), and up to four DIMM modules can be connected to one memory controller.

5.3.1 Memory Operational Modes

The system has three memory operational modes: Single, Double, and Mirror. The mode that is applied depends on the number of MMRs connected to one NDC chip and whether mirror mode is enabled in SAL setup, as indicated in the table below.

Table 16. Memory Operational Mode

Memory Operational Mode	Number of MMR Connected to One NDC	SAL Setup of Mirror Mode	Redundancy and Hot-Swap Support	Explanation
Single	1	Disabled or enabled	No	One MMR is connected to one NDC. No redundancy. Throughput of data transfer is half of operational mode "Double."
Double	2	Disabled	No	Two MMRs are connected to one NDC. No redundancy. Throughput of data transfer is double of operational mode "Single."
Mirror	2	Enabled	Yes	Two MMRs are connected to one NDC and the same data is stored in these two MMR. So, two MMRs are running like a mirror of each other and are configured redundantly. Throughput of data transfer is half of operational mode "Double."

5.3.2 Memory Box Population

Each memory box houses either four or eight DIMMs. For a four-DIMM configuration, DIMMs should be installed into locations JD0A1, JD0B1, JD2B1 and JD2A1.

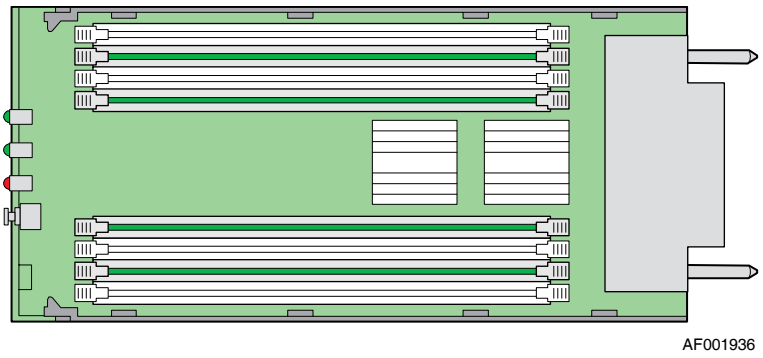


Figure 19. Memory Box

5.3.3 Memory Configuration

The following figures show the installation order and upgrade path for DIMMs, and the applicable mode for each configuration. In these figures, solid lines indicate installed memory boxes; dotted lines indicated locations of empty memory box sockets. Black boxes indicate installed DIMMs.

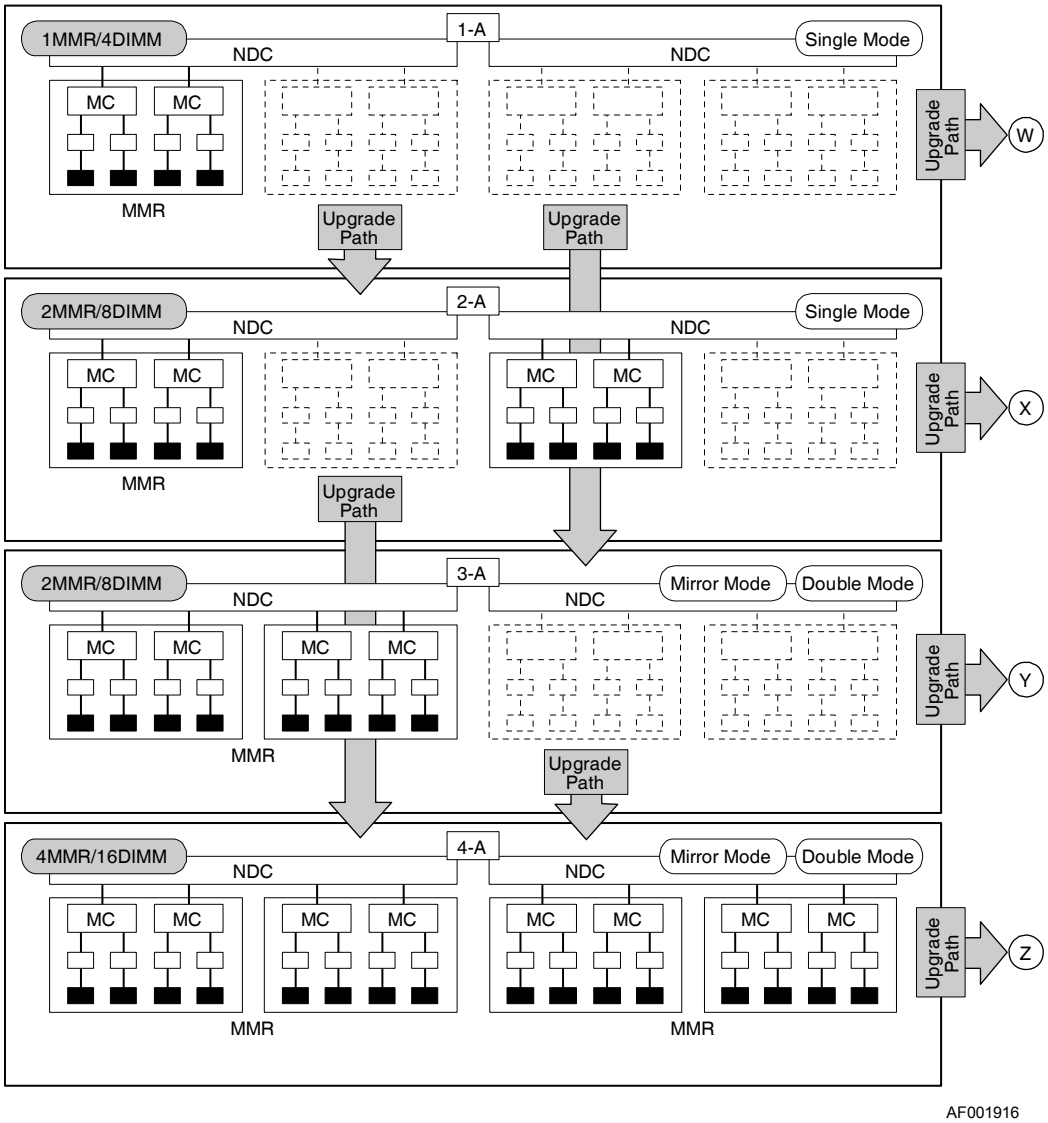
The first set of figures (1-A, 2-A, 3-A, 4-A) represent configurations in which four DIMMs are installed in each installed memory box. The paths to the right of the figures marked 'W', 'X', 'Y', and 'Z' show the upgrade to fully populated memory boxes (eight DIMMs in each memory box). These fully populated configurations are shown in the second set of figures (1-B, 2-B, 3-B, 4-B).

For example, configuration 1-A has only one MMR with four DIMMs installed, so only single mode is applicable. This configuration can be connected to three paths for upgrade, that is, to 2-A, 3-A. and 1-B.

In the paths to 2-A and 3-A, another memory box is needed. 2-A has a higher memory bandwidth than 3-A, because 2-A can use two NDC chips effectively. In 3-A, processors connected to the NDC linked to the MC with DIMMs installed can access all of the system memory with the shortest access time. Therefore, in some specialized situations, 3-A has a performance advantage to 2-A, such as in a two-socket installation.

In the path to 1-B no new memory box is needed and therefore has a lower cost for capacity addition.

Memory mirroring is applicable to 3-A, but not to 2-A nor 1-B.



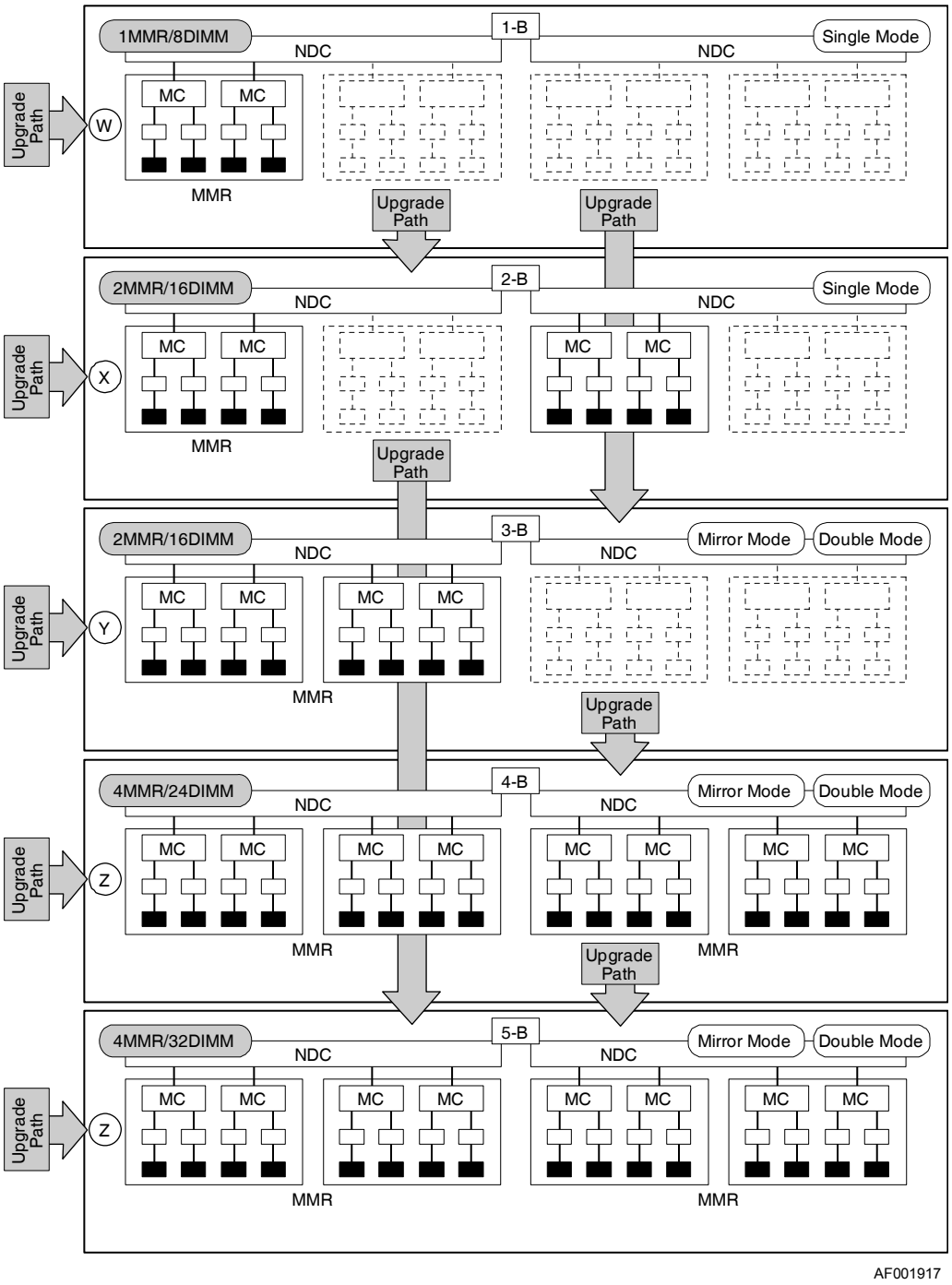


Figure 20. Memory Upgrade Paths

5.4 Memory RAS Function

The system supports the following functions for memory RAS (reliability, availability, serviceability).

Table 17. Memory RAS Functions

Function	Specification
ECC (S4EC-D4ED)	This facility corrects error of an adjacent 4-bit error in one set (four-DIMM group). This means all bits read from the single DRAM chip have failed. This function is equivalent to Chipkill*. When 4-bit pair is defined as one unit, the following functions are available Single unit error correction Double units error detection
Memory Chip Sparing	When the number of errors detected by ECC exceeds certain threshold, the chip of the target SDRAM is fenced and swapped with the normal spare SDRAM chip. The threshold detection, swapping, and memory data writing to the swapped spare SDRAM are performed by hardware automatically. Swapping is available up to two times per one set. The maximum of two chips can be swapped in one set (4-DIMM group).
Memory Mirroring	A pair of two memory boxes connected to one NDC chip can work as a mirror for each other.
Memory Box Hot Swap	If any DIMM or MC fails in Mirroring Mode, the memory box with a defective chip can be hot-swapped for the spare riser card. After replacement, the hardware and SAL copy the memory data to the memory of spare riser card and rebuild memory mirroring. Only 4U model supports this feature.
Memory Scrubbing	Periodically, dummy memory accesses are done in idle time, and when ECC errors are found, error-corrected data are written back to the same memory location from that data with ECC error are read out. This operation can prevent ECC uncorrectable error (multi-bit error) from occurred, and find faulty DIMMs faster.

6. Hard Drive Backplane

A hard drive backplane connects the hard drives to the rest of the system. The backplane supports up to eight hot-swap SAS drives. Four ports are connected to the on-board SAS controller and the remaining four ports can be used with an add-in SAS adapter. Through the on-board controller RAID 0, 1, and 1E are supported.

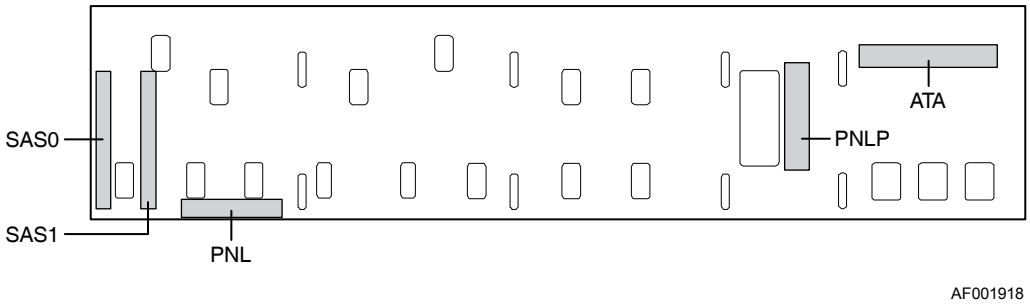


Figure 21. Hard Drive Backplane - Bottom View

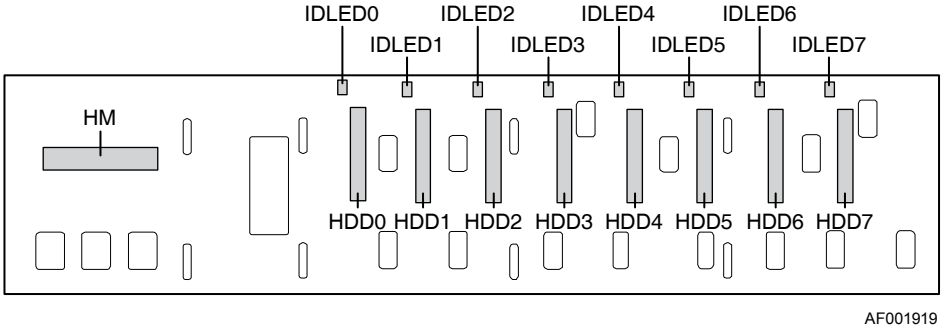


Figure 22. Hard Drive Backplane - Top View

Table 18. Hard Drive Backplane Connectors

Board Location	Connector	Description
C0	HDD 0, 1, 2, 3	SFF-8482 (SAS internal x1 connector)
C1	HDD 4, 5, 6, 7. See note below	SFF-8482 (SAS internal x1 connector)
C2	SAS0	SFF-8482 (SAS internal x1 connector)
C3	SAS1. See note below	SFF-8482 (SAS internal x1 connector)
C4	ATA	40-pin IDE connector
C5	PNL	
C6	PNLPW	

Note: This is available when an additional SAS PCI card is installed into a PCI slot.

The backplane uses the following connector specifications. Connectors meeting these specifications are required to connect an add-in PCI adapter to the backplane.

Table 19. SAS Connector Specifications and Application

Specifications	Application
SFF 8482	Hot Swap SAS drive connector
SFF 8484	Internal 4-wide connector

6.1 Hard Drive Configurations

The following figures show the supported connections between HDD 0-7 and the onboard SAS controller/PCI add-in card. The on-board SAS controller is connected to only four of the eight possible ports (HDD 0-3). HDDs 4-7 require the addition of a PCI SAS card.

A combination of the on-board SAS controller and add-in SAS PCI card is supported. When using a combination of the on-bard SAS controller and an add-in SAS PCI card, see the *Tested Hardware and Operating System List* for validated combinations.

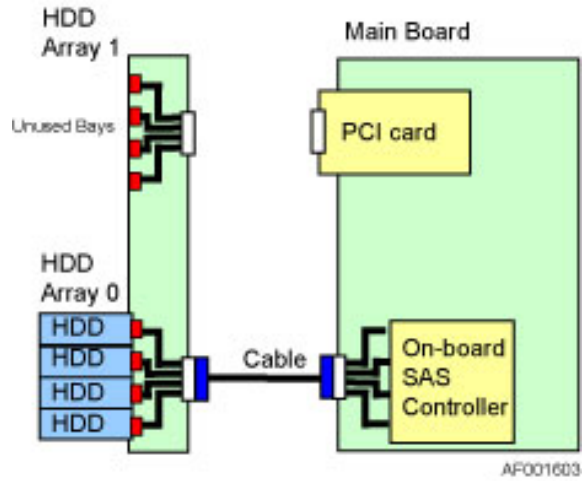


Figure 23. Four HDDs Connected to On-board Device

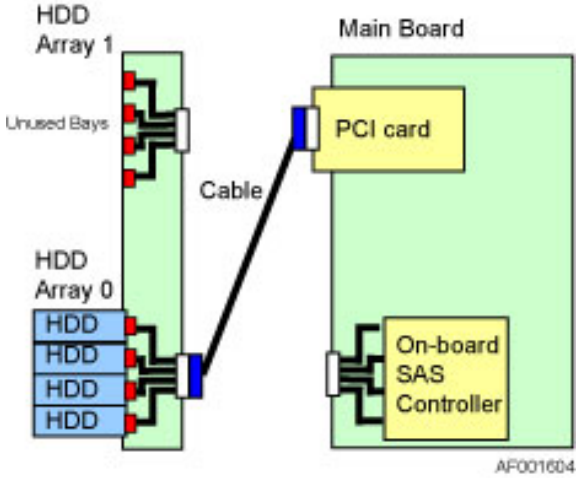


Figure 24. Four HDDs Connected to One PCI Card

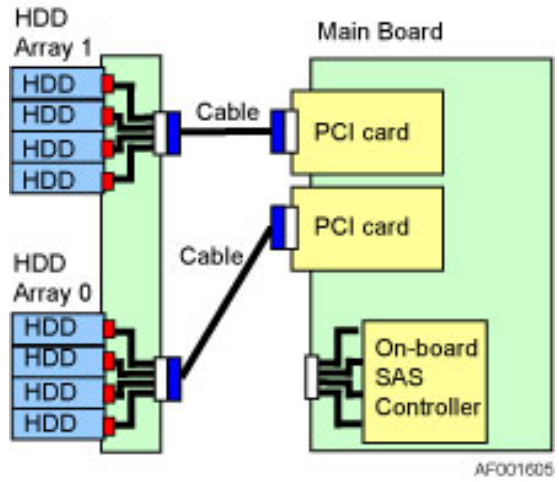


Figure 25. Eight HDDs Connected to Two PCI Cards

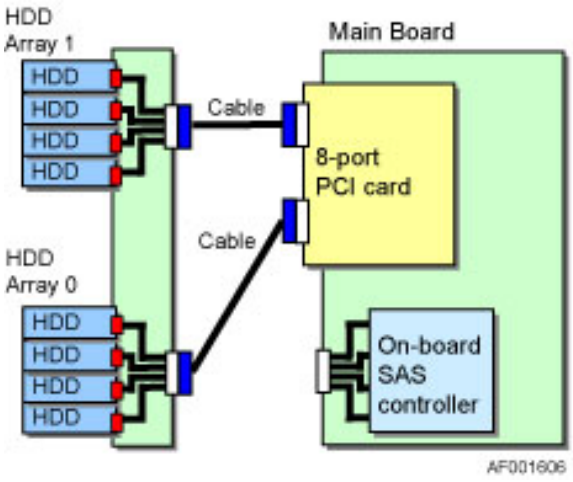


Figure 26. Eight HDDs Connected to One 8-port PCI Card

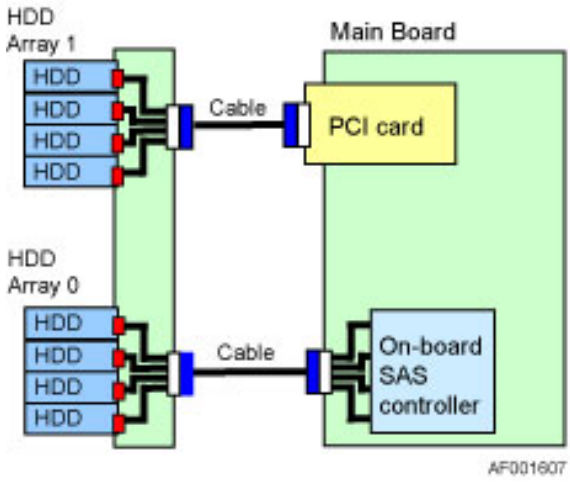
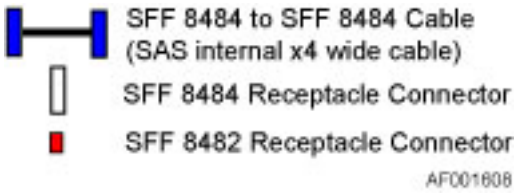
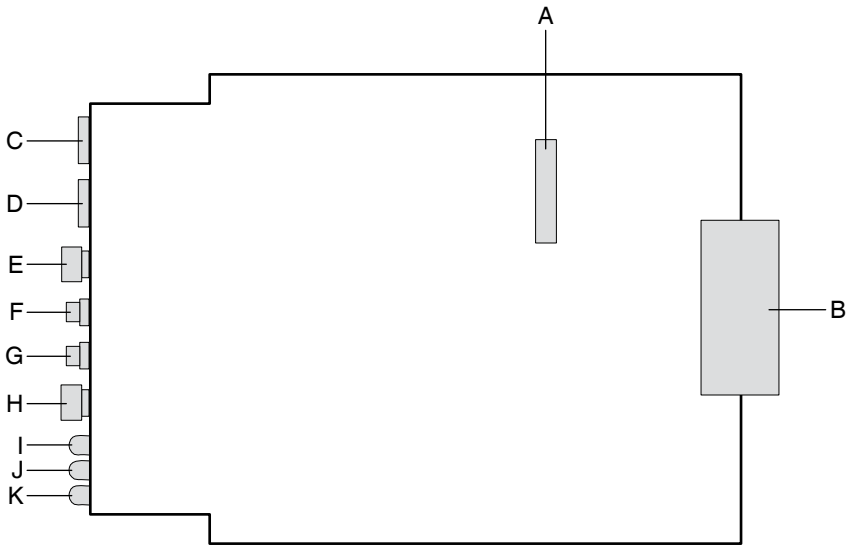


Figure 27. Eight HDDs Connected to On-board Device and PCI Card



7. Front Panel

The front panel has four buttons, five LEDs, and one buzzer.



Callout	Board Location	Component
A	C2	DVD
B	C1	HM
C	C3	USB4
D	C3	USB5
E	P1	Power button, power LED
F	P2	Reset button
G	P3	SDINT button (system diagnostic interrupt)
H	P4	Identification button, identification LED
I	P5	Power fault LED
J	P6	Colling fault LED
K	P7	General fault LED

Figure 28. Front Panel

Table 20. Front Panel LEDs

LED	Color	State	Description
Power LED	Green	On	ACPI S0 state
		Blink	System in power down process
		Off	ACPI S5 state
Cooling Fault LED	Red	On	Critical, non-recoverable over temperature or fan failure
		Blink	Non-critical over temperature condition or low fan speed
		Off	No fan failure, or the status that BMC does not detect any fan failure.
Power Fault LED	Red	On	Critical, non-recoverable power fault
		Blink	Non-critical power fault
		Off	No power failure, or the status that BMC does not detect any power failure.
General Fault LED	Red	On	Critical, non-recoverable other failure
		Blink	Non-critical other failure
		Off	No general failure, or the status that BMC does not detect any general failure.
Chassis ID LED	Blue	On/Off	This LED can be used to identify the server from the others by toggling on/off with the identification button.
		Blink	The system is in CMOS clear or FWH recovery mode.

7.1 Front Panel Panel Buttons

7.1.1 Power Button

By toggling the power button, the power is turned on and off.

7.1.2 Reset Button

When the reset button is pressed with the system power on, a hard reset is executed. The system must dump the BMC registers so it may take up to 15 seconds after pressing the button before the system resets. If the reset button is pressed for ten consecutive seconds while the system is powered off, the mode transfers to CMOS clear mode. CMOS clear mode is described in section 7.3.1.

7.1.3 System Diagnostic Interrupt (SDINT) Button

When the system is powered on and the SDINT button is pressed, a reset is executed. If the SDINT button is pressed for ten consecutive seconds while the system is powered off, the mode transfers to firmware hub (FWH) emergency recovery mode. FWH emergency recovery mode is described in section 7.3.2.

7.1.4 ID Button (Identification Button)

The BMC toggles the chassis ID LED on and off when the ID button is pressed. This button is also used to disarm the buzzer when the system has detected an event and the buzzer is sounding. When the buzzer is stopped, the status of the blue chassis ID LED does not change. For example: If the blue LED is lit and the alarm is sounding, after the ID button is pressed to disarm the buzzer, the blue LED remains lit.

7.2 Front Panel LEDs

7.2.1 Power LED

The power LED turns on when power-on is executed. The power LED blinks in a 1.2 second-cycle when a power-off is executed until the system turns off, at which point the power LED turns off.

7.2.2 Power Fault LED

If a serious power fault is detected, the power fault LED turns on. If the power fault is not critical, the power fault LED blinks in a 1.2-second cycle. When BMC power is turned on or the hardware is reset, the power fault LED turns off. Since the power can be off due to a power supply or voltage fault, the power fault LED does not turn off when BMC power is turned off.

7.2.3 Cooling Fault LED

When a critical fan or temperature fault is detected, the cooling fault LED turns on. Non-critical fan or temperature faults result in the cooling fault LED blinking in a 1.2-second cycle. When the BMC detects system power is applied or the system is reset, the cooling fault LED turns off. The cooling fault LED does not turn off when the BMC detects that the system power is turned off due to a faults with a fan or a high temperature condition.

7.2.4 General Fault LED

When serious general faults other than faults of a power source, voltage fan, or temperature are detected, the general fault LED turns on. Lesser general faults result in the LED blinking in a 1.2-second cycle. When BMC detects the system power is turned on or the hardware is reset, the general fault LED turns off. The general fault LED does not turn off when the BMC detects that the system power is turned off due to a critical general fault.

7.2.5 Chassis ID LED

Each time the ID button is pressed, the BMC toggles the blue chassis ID LED on or off. The BMC also toggles the ID LED when a device ID IPMI command is received. For example, the ID LED can be remotely activated on a failed system to help locate the physical system in a server room. When BMC enters CMOS clear mode or FWH emergency recovery mode, the chassis ID LED blinks. The blink patterns are as follows:

- CMOS clear mode: 1.8 seconds on and 0.6 seconds off
- FWH emergency recovery mode: 0.6 seconds on and 1.8 seconds off

An IPMI command is set up in the BMC so that SAL can control the blink of chassis ID LED. SAL makes chassis ID LED blink during the normal FWH recovery. In this case, the blink is 0.6 seconds on and 0.6 seconds off.

7.2.6 Buzzer

If a serious fault is detected, a buzzer sounds in addition to the appropriate LED lighting. When the serious fault is acknowledged by pressing the chassis ID button, the buzzer stops and the fault LED turns off.

7.3 Recovery Modes

This section describes the system recovery modes. These modes are mutually exclusive. A mode executed earlier is prioritized, so that two modes are never executed at the same time.

7.3.1 CMOS Clear Mode

When the reset button is pressed for ten consecutive seconds while the system is powered off, the chassis ID LED blinks for 1.8 seconds on and 0.6 seconds off, and the mode transfers to CMOS clear mode. When the power is turned on while the server is in this mode, the SAL clears the CMOS while booting the system. The CMOS clear mode can be canceled by pressing the reset button again before pressing the power on button.

7.3.2 Firmware Hub Emergency Recovery Mode

When the SDINT button is pressed for ten consecutive seconds while the system is powered off, the chassis ID LED blinks for 0.6 seconds on and 1.8 seconds off, and the mode transfers to FWH emergency recovery mode. When the power is turned on in this mode, the BMC switches the FWH boot bank from #0, for normal use, to #1, for emergency use. FWH emergency recovery mode can be cancelled by pressing the SDINT button again before pressing the power on button.

7.4 Front Panel Tests

7.4.1 LED Test

All LEDs turn on when the system first powers on. A LED fault is indicated if an LED does not turn on at boot.

7.4.2 Buzzer Test

There is an IPMI command to test the buzzer. This is the same command as the fault LED test command.

7.5 BMC Mode Indication

7.5.1 BMC Firmware Write Mode

All LEDs blink when the BMC mirrors the BMC firmware of the external flash ROM (BMC spool) into the built-in flash ROM (BMC bank).

7.5.2 BMC Firmware Damage Mode

When the BMC firmware checksum tests both the external flash ROM (BMC spool) and the built-in flash ROM (BMC bank), and finds both of them damaged; the BMC stops. All LEDS will be on and the buzzer will sound.

8. Connector / Header Locations

8.1 Board Connector Information

Table 21. Board Connector Matrix

Connector	Quantity	Reference Designators	Connector Type	Pin Count
Main Power	2	JPS0, JPS1	Power Connector	
CPU VR Power	2	JMVR0, JMVR1	Power Connector	12
KVM Connector	1	JKVM	Mezzanine	
SATA Connector	1	JB00T	Header	7
IDE Connector	1	JDVD	Connector	40
IPMB	1	JIPMB	Header	3
SAS cable connector	1	JHDD	Header	
Debug Connector	1	JHUDI	Header	
X8 PCI Express	2	JSLOT1, JSLOT4	Card Edge	
X16 PCI Express	2	JSLOT2, JSLOT5	Card Edge	
PCI-X	2	JSLOT3, JSLOT6	Card Edge	
Processor Socket	4	UCPU0, UCPU1, UCPU2, UCPU3	mPGA700	
Hot Swap Fan	6	JFAN0, JFAN1, JFAN2, JFAN3	Header	10
Front Panel Connector	1	JPANEL	Locking header	
Panel Power	1	JPNPWR	Header	24
XDP	1	JXDP	Header	
MMR Connector	4	JVH0, JVH1, JVH2, JVH3		
Stacked RJ45	2	JGBE	External LAN	
RJ45	2	JETHER, JETHER2	External LAN	
Stacked USB x2	2	J3701, J3702	External USB	4
VGA Connector	1	J3501	External DSub	15
Serial Port	2	JCOM	External DB9	9

Table 22. Front Panel Connector Matrix

Connector	Quantity	Reference Designators	Connector Type	Pin Count
Main connector	1	J01		110
Slim-line drive connector	1	J02	Right-angle header	
USB	2	J03, J04	USB connector	4

Table 23. Backplane Connector Matrix

Connector	Quantity	Reference Designators	Connector Type	Pin Count
P-ATA connector	1	JDVD	Connector	40
Backplane power connector	1	JPNLPW	Connector	24
Panel Connector	1	JPANEL	Connector	40
SAS cable connector	2	JS4P0, JS4P1	SFF-8484	
Front Panel connector	1	JHM		110
Hot Swap SAS headers	8	JSDR0, JSDR1, JSDR2, JSDR3, JSDR4, JSDR5, JSDR6, JSDR7	SFF-8482	

9. Power Supply

Figure 29. Power Supply

9.1 AC/DC Unit

The 12-volt hot-swap AC/DC units are rated at a maximum of 1390 watts over an input range of 200-240 VAC and at a maximum of 990 watts over an input range of 100-127 VAC. The AC/DC configuration is shown in Table 24.

This power supply has +12 V and +5 Vsb outputs. The standby voltage of +5 Vsb is active when AC power is applied to the power supply. This power supply is connected to system-board directly or via extension board, and can be used in 1+1 redundant mode when the input is 200-240 VAC.

Table 24. AC/DC Configuration

Item	Configuration (Load restrictions are required)	
AC Input	100-127 Vac	200-240 Vac
Redundancy	No (2+0)	Yes (1+1)
Hot-Swap	No	Yes
System Power	990 W	1390 W

9.1.1 AC Input Voltage Requirements

Table 25. AC Input Voltage Requirements

Range	Minimum	Nominal	Maximum
100 Vac Range	90 Vrms	100-127 Vrms	140 Vrms
200 Vac Range	180 Vrms	200-240 Vrms	264 Vrms

9.1.2 Inrush Current

After AC power is applied to the power supply the initial inrush current surge or spike of 100 us – 10 ms must not exceed a 50 amp peak.

9.1.3 Efficiency

The efficiency must be 80% or higher when the power supply is operating at a nominal input voltage and maximum load.

9.1.4 Input Harmonic Current Limits

Input harmonic current must meet the requirements of IEC 61000-3-2 / 61000-3-2.

9.1.5 DC Output Voltage

The output voltage tolerance must remain within the limits as specified in the following table for any valid input voltage and any combination of input frequency, output loading, output ripple voltage and setting accuracy. The ripple voltage is to be included within the tolerance bands. The tolerance range for each DC output level is given below.

Table 26. DC Output Voltage

Output Level	Minimum	Nominal	Maximum
+12 V	+11.64 V	+12.12 V	+12.60 V
+5 Vsb	+4.85 V	+5.05 V	+5.25 V

9.1.6 DC Output Current Rating

Table 27. DC Output Current Rating

Output Level	Minimum Load	Maximum Load	Input AC Range
+12 V	0.0 A	113.0 A	200 Vac Range
+5 Vsb	0.0 A	4.0 A	
+12 V	0.0 A	80.0 A	100 Vac Range
+5 Vsb	0.0 A	4.0 A	

9.1.7 Current Sharing

The +12 V output has a current sharing function. A "Current_Share12" pin for each current-sharing output level is connected to the equivalent pin on the other power supply, which is sharing the total load for that output level.

Output current difference between each power supply should be less than or equal to 10% of maximum load of output current.

In equation form, $[I_1-I_2] / I_{max} <= 0.1$

Where I_{max} is the maximum load rating of each power supply, and I_1, I_2 are the output currents of each power supply which is operating in redundant mode.

9.1.8 Output Over-Voltage Protection

The power supply detects, latches, and shuts down the output when an over-voltage fault occurs. If over-voltage is detected on the 12 V; the 12 V output is shut down and 5 Vsb is kept as output. Both the 5 Vsb and 12 V outputs are shut down if over-voltage is detected on the 5 Vsb. The power supply's over-voltage protection is locally sensed.

To reset the over-voltage latch for the 12 V voltage level the "-Output_Enable." must be toggled. To reset the over-voltage latch for the 5 Vsb the AC input must be removed from the power supply.

The output over-voltage protection function is to avoid a fire hazard; it is not to maintain normal operation of the system, even in a redundant configuration.

9.1.9 Output Over-Current Protection

The power supply detects, latches, and shuts down the output after a 200 ms – 400 ms delay when an over-current fault occurs. If an over-current is detected on the 12 V; the 12 V output is shut down and the 5 Vsb is maintained as output. If an over-current is detected on the 5 Vsb; the 5 Vsb and 12 V outputs are shut down.

To reset the over-voltage latch for the 12 V voltage level the "-Output_Enable" command must be toggled. To reset the over-voltage latch for the 5 Vsb the AC input must be removed from the power supply.

9.1.10 Output Short Circuit

A short circuit to the ground of any output does not cause physical damage to the power supply.

9.1.11 Thermal Fault

The power supply detects, latches, and shuts down the 5 Vsb and 12 V outputs when a thermal fault occurs. Unplug the AC input to reset the thermal fault latch.

9.1.12 AC/DC Unit Structure

See power supply unit for precise dimensions.

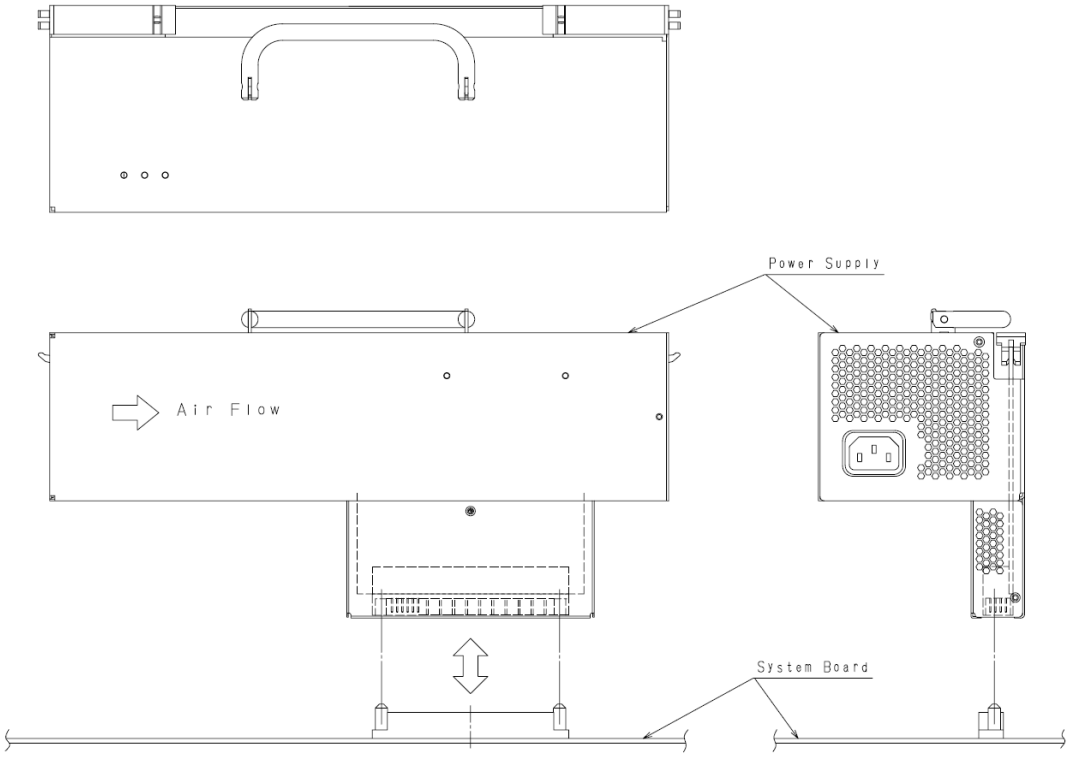
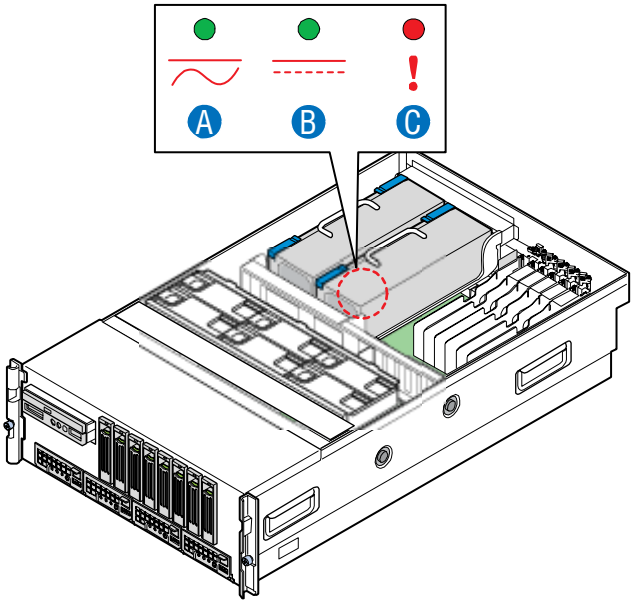


Figure 30. Power Supply Unit

9.1.13 LED Labeling

The LEDs are visible from the top of the power supply.



AF001970

A. Input Good LED	Indicates the power is good when this green LED is on.
B. DC Output Good LED	Indicates the output power us good when this green LED is on.
C. Fault LED	Indicates a fault with the power supply when this red LED is on.

9.1.14 AC/DC Unit Installation

The server system has two bays for AC units. The server requires both power supplies when supplied by 100-110 VAC power outlets. Power redundancy only exists when both power supplies are connected to 200-220 VAC power outlets. The power supply can be hot-swapped only when two power supplies are used and they are connected to 200-220 VAC outlets.

9.1.15 Hot-Swap Procedure

- Remove: AC/DC unit must be detached only when the system is in the standby or power-on condition. Before AC input is detached, the AC cord must be disconnected from the unit.
- Insert: Attach AC unit to the cabinet and then connect the AC code to the unit. Then the system power status must be standby or power-on.

9.1.16 AC/DC Unit Cooling

Each AC/DC unit has one non-redundant fan for cooling.

9.1.17 AC Inlet Connector

AC/DC unit has an IEC 320 C-14 standard power inlet, which is 10 A/250 VAC (International), 15 A/250 VAC (North America).

9.1.18 AC Line Fuse

Only the line is fused. Neutral is not fused. Fuses in line voltages meet all requirements necessary for obtaining UL, CSA, and IEC approvals.

9.1.19 AC Line Dropout

While operating normally, an AC line dropout condition, with the period of 20 milliseconds or less, must not break any regulations.

9.1.20 Safety Certifications

- UL/CSA 60950-1 Recognition
- IEC 60950 - CB certification
- China CNCA CCC Certification
- Taiwan BSMI Certification

9.2 DC/DC Specification

9.2.1 VRM / Embedded Regulator

Output voltages of AC/DC unit are 12 V and 5 Vsb. Both outputs are provided by non-isolated DC/DC converters mounted on the main board. The “Delta Electronics, P12T100-1 (Intel enabled parts)” is validated as the voltage regulator (VR) for Intel® Server System SR9000MK4U.

9.2.2 Standby Output/Standby Mode

Standby output voltages are 5 Vsb, 3.3 Vsb, and 1.5 Vsb. 5 Vsb is provided by AC/DC unit. 3.3 Vsb and 1.5 Vsb are made from 5 Vsb by non-isolated DC/DC converters mounted on the main board.

9.2.3 Power-On/Off Sequence

- Main voltages: Main voltages on main board should be sequentially powered.
- Standby voltages:
  - Power-on sequence:
    3.3 Vsb and 1.5 Vsb are automatically powered on after 5 Vsb is applied. Power on sequence does not have any restriction. BMC power-on reset signal should be made with proper delay after 3.3 Vsb and 1.5 Vsb are established.
  - Power-off sequence:
    N/A. (Standby voltages are not powered off unless AC input is unplugged.)

- MMR:
  - Power-on sequence: Power-on signal makes hot-swap circuit active. 12 V and 3.3 V are supplied to the MMR board.
    - 1.5 V DC/DC is automatically activated after hot-swap circuit is active.
    - 1.8 V DC/DC is automatically activated after 1.5 V is active.
  - Power-off sequence: There is no sequence for power-off.

9.2.4 Programmable Voltage Margin Check Function

Voltages can be set to +/-5% or nominal by I^2C signal.

10. Cooling

The server system inlets have 5+1 redundant fans for cooling. The power supplies have non-redundant fans that provide airflow through the rear of the chassis.

10.1 Cooling Structure

Six 120 mm x 38 mm fans provide redundant airflow to cool the system components, processor, memory and chipset. The fans are placed across the front of the chassis, directly in front of the processors. The hard drives and DVD drive are cooled by intake airflow. Components on the main board, including the processors and the chipset are cooled by airflow through the air duct. The cooling fans are Sanyo* 9G1212P1G04 (120 mm x 120 mm x 38 mm).

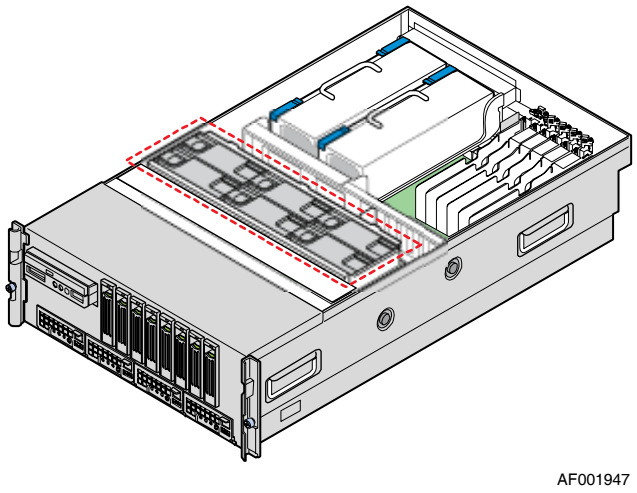


Figure 31. System Fan Location

10.1.1 Fan Failure Control

Each of the six hot swap fans has a green LED that is lit when the fan is operating normally. The green LED turns off if a fan failure is detected or if the hot swap fan is removed. If a fan fails or is removed, then the remaining fans boost to full speed after a short period of time.

10.2 Processor Cooling

The processors are cooled by passive heatsinks and airflow provided by the six front fans. The processor heatsink model is Fujikura Ltd.* FHP-5133 or FHP-7446. An airflow guide provides optimal cooling over the processors.

Figure 32. Air Flow Guide

11. Firmware

The firmware is based around three components.

- System Abstraction Layer (SAL)
  - Initializes system hardware
  - Provides services and functions to OS and EFI
- Extensible Firmware Interface (EFI)
  - Provides and environment for booting an OS and running pre-boot applications
  - Based on Intel EFI Sample Implementation 1.10.14.62
  - Incorporates drivers provided by I/O vendors
- Baseboard Management Controller (BMC)
  - Initiate power on sequence
  - Monitors system status and logs information
  - Provides interfaces and commands based on IPMI 2.0 specification

Code is executed by a H8S/2166 16-bit microcomputer.

11.1 System Abstraction Layer (SAL)

The SAL oversees the system initialization after the BMC has started. If an error occurs during system initialization the SAL can perform a firmware recovery and read the backup ROM image from flash memory. The SAL is based on Phoenix* BIOS and compliant with the SAL Specification, Revision 3.2. The SAL does not support a graphical splash screen feature.

The SAL supports the following boot devices

- On-board SAS
- Network boot
  - GbE ports
  - 100 Mb ports
- IDE DVD-ROM drive
- USB ports
- PCI add-in cards

The SAL has a dedicated connection to the BMC capable of interfacing with IPMI commands. The dedicated KCS interface is used for management LAN configuration, serial port operations, progress code display, SEL log, and clock synchronization. The SAL can also interface with the operating system through ACPI 3.0 tables and SMBIOS tables.

11.2 Extensible Firmware Interface (EFI)

The EFI boot manager enables the user to control the booting environment of the server. After the system power is on, the boot manager activates the system using the boot option settings. For example, the user can boot to the EFI shell, to an operating system on the network or on media in the server, or to the boot maintenance menu. The EFI shell is compliant with the EFI Specification 1.1.

The following drivers are integrated into system firmware image.

- FPSWA (floating-point exception handler)
- EFI driver for ESB2 LAN (Intel® PRO/1000)
- EFI driver for onboard SAS (LSI* SAS1068)
- EFI driver for Management LAN (Intel PRO/100)
- Legacy OPROM for onboard VGA (ATI* ES1000)

11.2.1 EFI Console

EFI uses VGA as a standard console of EFI boot manager and EFI shell. In an EFI environment, the EFI VGA driver directory controls the VGA.

The figure below shows the outline of console control by EFI. EFI can redirect the standard input/output and error output to VGA, keyboard, or serial console.

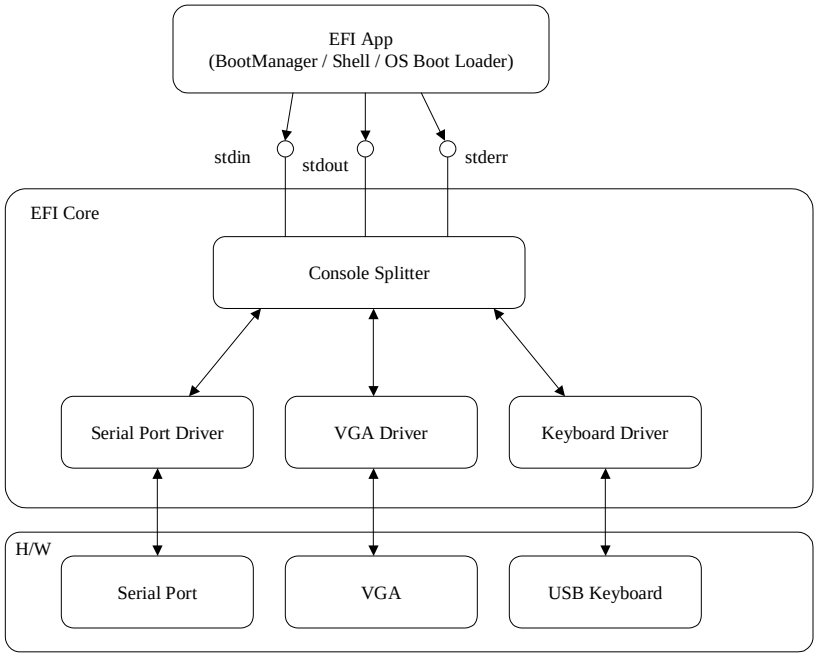


Figure 33. Console Control by EFI

11.2.2 EFI System Setup

The System Setup utility provides a way for users to modify the default server settings. Users can execute this utility regardless of whether an operating system is installed.

The System Setup utility stores most of the setting values in the battery-backed CMOS. The rest of the values are stored in flash memory. Changes to values take effects when the server is booted.

The power-on self test (POST) uses these values when it sets up the hardware. If the values and the hardware do not match, then POST generates an error message and the user must use the System Setup utility to specify the correct settings.

Run the System Setup utility to view or modify the following server board functions:

- Processor configuration
- Memory configuration
- Onboard VGA setting
- Serial port configuration
- Default CMOS settings

Figure 34. System Setup Utility

11.2.2.1 Starting the System Setup Utility

1. Press the power button on the front control panel.
2. When the EFI Boot Manager starts, select [Boot Maintenance Menu] and press <Enter>.
3. Select [System Setup] in the [Boot Maintenance Menu] and press <Enter>. The main System Setup Utility screen is displayed.

11.2.2.2 Recording Your Setup Settings

Before changing any settings, record the current values and the new values. If you need to restore the default values later, such as with a CMOS clear, you may need to enter the System Setup utility to change values. By referring to the stored original settings, the restore operation may become easier.

11.2.2.3 Navigating Setup Utility Screens

The System Setup utility consists of ten primary menus. Each menu occupies one screen and displays a list of menu items. Some menu items have sub-menus. The user can modify the settings of some menu items on the screen. The table below describes how to navigate through the screens and menus.

Table 28. Using Setup Screens

Press	To
Enter	Select a sub-menu item or changes to next value of a selected item.
↑	Move up through menu items.
↓	Move down through menu items.

11.2.2.4 Primary Screens

The System Setup utility uses the following primary screens

Table 29. Primary Setup Screens

Screen	Description
Main	Configure system's attribute as operation at AC power recovery.
Processor	Configures the processors. For details, see section 11.2.2.4.1
Memory	Configures memory. For details, see section 11.2.2.4.3
Devices	Configures VGA. For details, see section 11.2.2.4.4
Server Management	Configures server management. For details, see section 11.2.2.4.5
System Information	Display firmware version, and board, chassis, product information
Save changes and Exit	Stores the changed values in CMOS, and exits setup. Clicking on the menu item causes the system to prompt the user for a Yes or No response. Yes: Saves the changes and reboots the system. No: Aborts the action.

Screen	Description
Discard changes and Exit	Does not store the changed values in CMOS, and exits setup. Clicking on the menu item causes the system to prompt the user for a Yes or No response. Yes: Saves the changes and exits the utility. No: Aborts the action.
Restore Defaults	Restores the setting values to default. Clicking on the menu item causes the system to prompt the user for a Yes or No response. Yes: Loads the system setup defaults. No: Aborts the action.
Exit	Exits setup. If there are any changes, the user is prompted for a Yes or No response. Yes: Saves the changes and reboots the system. No: Aborts the action.

In the tables below, default values are in brackets.

11.2.2.4.1 Main

Table 30. Main Screen

Primary Menu Item	Sub Menu Item	Options	Description
Power On Option	After Power Failure	[Return] On Off	Determines whether the system should boot once power returns after a power loss. Return: Return to previous state at power loss occurs. If power loss occurs at system on state, the system returns to the power-on state at power recovery. If it occurs at system off state, the system remains off. On: Power on after power recovery. Off: Not goes to power on state (Power off) after power recovery.

When the power button is pressed and released while the main power is on, the power turns off or the operating system begins a shut down process. If the power button is held down, a forced power off is executed. If the power is forced off, then the server is not powered on after AC power recovery even if on is selected as the Power On Option. To rectify this situation, use the power button to power on the system, and then press and release the power button to shut down the server without forcing it into the power off state.

When the system is configured with AfterPowerFailure = On, the power turns on automatically in the following situations:

- When a power loss occurs while the equipment main power is on.
- When the operating system is shut down normally, the main power turns off, and then a power loss occurs.

11.2.2.4.2 Processor Screen

Table 31. Processor Screen

Menu Item	Options	Description
Hyper Threading	[Disable] Enable	Enables or disables multi-threading.
Failed Processor Deconfiguration	[Enable] Disable	Enable: Deconfigures the failure-detected processor and boots. Disable: Cancels boot and turns off the power.

11.2.2.4.3 Memory Screen

Table 32. Memory Screen

Menu Item	Options	Description
Memory Mirroring	[Disable] Enable	Enables or disables memory mirroring.
Failed Memory Deconfiguration	[Enable] Disable	Enable: Deconfigures the failure-detected memory and boots. Disable: Cancels boot and turns off the power.
NUMA	[Enable] Disable	Enables or disables NUMA memory configuration.

11.2.2.4.4 Devices Screen

Table 33. Devices Screen

Primary Menu Item	Sub Menu Item	Options	Description
VGA	Onboard VGA	[Enable] Disable	Enables or disables on-board VGA.

11.2.2.4.5 Server Management

Table 34. Server Management Screen

Primary Menu Item	Sub Menu Item	Options	Description
Console Redirection	COM1 Console Redirection	Press <Enter>	Pressing <Enter> invokes the submenu to configure COM1 console redirection. See Table 35.
Management LAN	DHCP	[Enable] Disable	Enable: Acquires IP address of LAN port by DHCP. Disable: Requires the manual settings.
	IP Address	[255.255.255.255]	IP address of management LAN port. Available when DHCP is disabled.
	Subnet Mask	[255.255.255.255]	Subnet mask of management LAN port. Available when DHCP is disabled.
	Default Gateway	[255.255.255.255]	Default gateway address of management LAN port. Available when DHCP is disabled.
SEL Clear	-	Press <Enter>	Pressing <Enter> key prompts the user to respond with Yes or No. Yes: Clears the SEL. No: Aborts the action.

Table 35. COM1 Console Redirection Screen

Menu Item	Options	Description
Headless Support	[Enable] Disable	Enable: Outputs firmware or EFI console input/output to COM1. Provides SPCR or HCDP to OS. Disable: Does not output firmware or EFI console input/output to COM1. Does not provide SPCR or HCDP to the OS. When the valid VGA is not mounted, Enable is set.
COM1 Speed	9600 bps [19200bps]	Uses the communication speed specified when console redirection is valid.

11.2.2.4.6 System Information

System information, such as firmware version, board information, chassis information, and product information, is displayed.

```
System Information

     SAL Revision              :xx-xx
     BMC Firmware Revision     :xx-xx
     Board Part Number         :xxxxxxxx
     Board Serial Number       :xxxxxxxx
     Product Part Number       :xxxxxxxx
     Product Serial Number     :xxxxxxxx
     Chassis Part Number       :xxxxxxxx
     Chassis Serial Number     :xxxxxxxx

     Exit
```

11.3 Baseboard Management Controller (BMC)

The BMC provides an interface for out-of-band (OOB) management of the system. The BMC supports IPMI 2.0 commands such as powering the system up or down the system. System logs are accessed through the BMC as well as front panel mechanisms.

To prevent system failures the BMC duplicates the firmware to the H8S internal ROM and an external flash ROM. If the internal ROM fails, then the BMC copies the contents of the external ROM and continues to start.

The BMC provides the following features:

- **Hardware monitoring**
  The BMC monitors the voltage, fan speed and temperature, and detects abnormalities in these values by using the National Semiconductor* LM93 as a sensor.
- **Power failure**
  The BMC monitors the *Power Good* signal of the power subsystem, and detects failures of the power subsystem.
- **Battery monitoring**
  The BMC detects the battery drain. This function is available by monitoring the GPIO of H8 microcomputer or by referring to the ESB2 register.
- **Core ratio programming**
  The BMC is responsible for setting the processor and bus speed. The processor information ROM (PIROM) data is available through I^2C, even when the system is powered off. The BMC gathers the bus speed, sets information from the PIROMs, and then configures the processors to the optimal core ratio.

- **System reset**
  The BMC controls the system reset for the system. When the reset button on the front panel is pressed, reset signals to the chipset are routed to the BMC, which allows the BMC to monitor and control the reset.
- **Access to the PIROM registers**
  The BMC is responsible for setting the registers in the NDC for the system. The BMC can access to the registers in the NDC through a special side band bus, called the parallel scan (PSC) bus. The PSC bus is connected to the BMC via the flip-chip pin grid array (FPGA).
- **CMOS clearing**
  The BMC controls clearing the CMOS (back-up SRAM in the ESB2).
- **Management LAN control**
  The BMC communicates with the Intel® 82551QM LAN controller through a special side band bus, called the TCO-port. The TCO-port adopts the standard SMBus block read and write commands to send and receive information to and from the BMC.
- **Shared memory**
  The BMC shares the memory with the software abstraction layer (SAL).

12. Design and Environmental Specifications

The operation of the server boards at conditions beyond those shown in the following table may cause permanent damage to the system. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Operational Environment	Altitude	Operational: -30 to 1524 meters (-100 to 5000 feet)
	Temperature (Operating)	Operational: ▪ 5 to 35°C (-100 to 2000 feet) ▪ 5 to 34°C (2000 to 3000 feet) ▪ 5 to 33°C (3000 to 4000 feet) ▪ 5 to 32°C (4000 to 5000 feet) (max rate change: 10°C /h) Non-operational: -10 to 43°C (max rate change: 10°C /h)
	Relative Humidity	Operational: 20 to 80% Non-Operational: less than 95%, non-condensing at 25 to 30°C
	ROHS	Compliance with ROHS. Parts that are used for this server system are in compliance with ROHS. Lead-free assembly process should be employed in the PCB assembly. The exemption of leads in solders for server, storage and storage array systems is applied to this server system.
Shock and Vibration	Vibration	Sine sweep 3 Hz to 200 Hz 0.3 G (packed) Random Vibration 0.8G (packed)
	Shock	450 mm (palletized) x 1 drop 300 mm (palletized) x 4 drops
Acoustic	Sound Pressure	<55 dBA / 60 dBA at ambient temperature 25°C Measured at a bystander position.

***Disclaimer Note**: Intel Corporation server boards contain high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system meets the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible, if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.*

13. Reliability, Serviceability, and Availability

The mean time between failures (MTBF) estimates are derived from a historical failure rate and multiplied by factors for application, electrical and/or thermal stress and age.

Table 36. MTBF Estimates

FRU	MTBF (hours)	Notes
Main Board	160,000	
Memory Box	790,000	
Z-Box	110,000	Configuration; Power Supply x1, MMR x1 Fans and DIMMs have redundancy and are considered.
Full Configuration	74,000	Configuration; four MVRs four processor, four memory boxes Fan, DIMM and MVR have redundancy and are considered..

14. Product Regulations

The system is subject to the following safety compliance and electromagnetic compatibility.

Table 37. Safety Compliance and Electromagentic Compatibility

Category	Region	Compliance Name
Safety / EMC	Canada	CSA.60950-1 ICES-003
	China	CCC GB4943
	Europe	EN60950-1 EMC Directive 89/336/EEC (CE Mark) EN55022 – Class A Limit (Radiated & Conducted Emissions) EN55024 (Immunity) EN61000-3-2 / EN610003-3, Harmonic Currents/Voltage Flicker NEMKO GS (Germany)
	International	IEC60950-1 (CB Report) CISPR 22 – Class A Limit (Radiated & Conducted Emissions) CISPR 24 (Immunity)
	United States	UL60950-1 FCC Class A (Radiated & Conducted Emissions)
	Australia / New Zealand	AS/NZS CISPR22
	Belarus	Belarus Certification
	Ukraine	Ukraine Certification
	Argentina	IRAM Certification
	Japan	VCCI (Class A Limit)
	Korea	RRL, MIC Notices No. 1997-41 & 1997- 42 – Class A Limit (Radiated & Conducted Emissions)
	Russia	GOST certificate issued for compliance with EN55022, EN55024
	Taiwan	BSMI, CNS13438 – Class A Limit (Radiated & Conducted Emissions)
Product Ecology	Intel Requirements	All materials, parts and subassemblies must not contain restricted materials as defined in Intel's Environmental Product Content Specification of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm
	Europe	Europe - European Directive 2002/95/EC Restriction of Hazardous Substances (RoHS) Threshold limits and banned substances are noted below. Quantity limit of 0.1% by mass (1000 PPM) for Lead, Mercury, Hexavalent Chromium, Polybrominated Biphenyls Diphenyl Ethers (PBB/PBDE) Quantity limit of 0.01% by mass (100 PPM) for: Cadmium
	Europe	WEEE Directive

Appendix A: Integration and Usage Tips

- Update systems to the latest firmware release. The firmware is http://support.intel.com/support/motherboards/server/SR9000MK4U
- There is no power redundancy or hot swap power supply support when the system is operated in a 110V -120V operating environment. Both of these features are supported when the system is operated in a 220V-240V environment
- A minimum of four DIMMs must be installed in each installed memory box (MMR) for the system to operate. The system will not operate if any of the installed memory boxes is populated with less than four DIMMs.
- When installing a DIMM into a memory box, verify that the DIMM is properly aligned with the notch on the DIMM connector. DIMM banks within the memory box are oriented differently.
- Prior to OS boot, only the front USB ports are enabled. Therefore, if an adapter requires configuration via an option ROM configuration utility, a USB keyboard must be attached to one of the front USB ports before power on.

Appendix B: POST Code Tables

Table 38. POST Code Generated by BMC and Logged at Seven-Segment LED

No.	Code	Description	Classification	Operation to Recover
0	0	(reserved)		
0	1	SRAM Check Started	Progress	
0	2	SRAM Check Completed	Progress	
0	3	Active side BMC F/W binary file checking	Progress	
0	4	Spool side BMC F/W binary file checking	Progress	
0	5	File check completed	Progress	
0	6	File update process started (normal process)	Progress	
0	7	File update process completed (normal process)	Progress	
0	8	File update process started (recovery process)	Progress	
0	9	File update process completed (recovery process)	Progress	
0	A	FWM Boot Block procedure completed	Progress	
0	B	Request to start F/W in Non Boot Block	Progress	
0	C	(reserved)		
0	D	(reserved)		
0	E	(reserved)		
0	F	(reserved)		
1	0	(reserved)		
1	1	(reserved)		
1	2	(reserved)		
1	3	(reserved)		
1	4	(reserved)		
1	5	(reserved)		
1	6	(reserved)		
1	7	(reserved)		
1	8	WDT overflow occurred	Error	BMC Error
1	9	Active side file recovery error	Error	Replace MB
1	A	Active side file update error	Error	
1	B	Check sum error detected in active side	Error	
1	C	SRAM check error (SRAM testing)	Error	
1	D	SRAM check error (Hardware detects error in SRAM testing)	Error	
1	E	Check sum error detected in both banks	Error	
1	F	SRAM Parity error detected	Error	
2	0	F/W in Non Boot Block started	Progress	
2	1	Initialization process of OS started	Progress	
2	2	AMI initialization started	Progress	
2	3	First process of task initialization started	Progress	
2	4	AMI task initialization, generation started	Progress	

No.	Code	Description	Classification	Operation to Recover
2	5	Second process of task initialization started	Progress	
2	6	AMI initialization completed	Progress	
2	7	OS booting process started	Progress	
2	8	Task booting process started	Progress	
2	9	(reserved)		
2	A	(reserved)		
2	B	(reserved)		
2	C	(reserved)		
2	D	(reserved)		
2	E	(reserved)		
2	F	(reserved)		
3	0	Message handler started	Progress	
3	1	PDK initialization process started	Progress	
3	2	Task generation process started	Progress	
3	3	BMC initialization completed	Progress	
3	4	(reserved)		
3	5	(reserved)		
3	6	(reserved)		
3	7	(reserved)		
3	8	(reserved)		
3	9	(reserved)		
3	A	(reserved)		
3	B	(reserved)		
3	C	Detailed log collection started by WDT overflow	Error	BMC Error
3	D	BMC restarted by WDT overflow	Error	
3	E	Failed in task generation	Error	
3	F	Illegal or mismatch format of GUID	Error	
4	0	CPU0 Thermal Trip	Error, event logged to SEL	Check SEL list
4	1	CPU0 Configuration Error (Absent)	Error, event logged to SEL	Check SEL list
4	2	CPU0 Configuration Error (Disabled)	Error, event logged to SEL	
4	3	CPU0 Configuration Error (Illegal Type)	Error, event logged to SEL	
4	4	CPU0 I2C Access Error (PIROM)	Error, event logged to SEL	
4	5	CPU0 I2C Access Error (Temperature Monitor)	Error, event logged to SEL	
4	6	CPU1 Thermal Trip	Error, event logged to SEL	
4	7	CPU1 Configuration Error (Disabled)	Error, event logged to SEL	
4	8	CPU1 Configuration Error (Illegal Type)	Error, event logged to SEL	
4	9	CPU1 Configuration Error (Different Type)	Error, event logged to SEL	
4	A	CPU1 I2C Access Error (PIROM)	Error, event logged to SEL	
4	B	CPU1 I2C Access Error (Temperature Monitor)	Error, event logged to SEL	
4	C	CPU2 Thermal Trip	Error, event logged to SEL	
4	D	CPU2 Configuration Error (Disabled)	Error, event logged to SEL	
4	E	CPU2 Configuration Error (Illegal Type)	Error, event logged to SEL	

No.	Code	Description	Classification	Operation to Recover
4	F	CPU2 Configuration Error (Different Type)	Error, event logged to SEL	
5	0	CPU2 I2C Access Error (PIROM)	Error, event logged to SEL	Check SEL list
5	1	CPU2 I2C Access Error (Temperature Monitor)	Error, event logged to SEL	Check SEL list
5	2	CPU3 Thermal Trip	Error, event logged to SEL	
5	3	CPU3 Configuration Error (Disabled)	Error, event logged to SEL	
5	4	CPU3 Configuration Error (Illegal Type)	Error, event logged to SEL	
5	5	CPU3 Configuration Error (Different Type)	Error, event logged to SEL	
5	6	CPU3 I2C Access Error (PIROM)	Error, event logged to SEL	
5	7	CPU3 I2C Access Error (Temperature Monitor)	Error, event logged to SEL	
5	8	MB Power Failure (Main 5.0V)	Error, event logged to SEL	
5	9	MB Power Failure (Main 3.3V)	Error, event logged to SEL	
5	A	MB Power Failure (Main 2.5V)	Error, event logged to SEL	
5	B	MB Power Failure (Main 1.8V)	Error, event logged to SEL	
5	C	MB Power Failure (Main 1.5V)	Error, event logged to SEL	
5	D	MB Power Failure (Main 1.2V0)	Error, event logged to SEL	
5	E	MB Power Failure (Main 1.2V1)	Error, event logged to SEL	
5	F	MB Power Failure (Main 1.2V2)	Error, event logged to SEL	
6	0	MB Power Failure (Voltage Type Unknown)	Error, event logged to SEL	Check SEL list
6	1	MVR0 Power Failure	Error, event logged to SEL	Check SEL list
6	2	MVR1 Power Failure	Error, event logged to SEL	
6	3	MVR2 Power Failure	Error, event logged to SEL	
6	4	MVR3 Power Failure	Error, event logged to SEL	
6	5	PS0 Configuration Error (Absent)	Error, event logged to SEL	
6	6	PS0 Configuration Error (Illegal Type)	Error, event logged to SEL	
6	7	PS0 Configuration Error (Insufficient Resources)	Error, event logged to SEL	
6	8	PS1 Configuration Error (Insufficient Resources)	Error, event logged to SEL	
6	9	PS1 Configuration Error (Different Type)	Error, event logged to SEL	
6	A	PS0 Power Failure (Insufficient Resources)	Error, event logged to SEL	
6	B	PS1 Power Failure (Insufficient Resources)	Error, event logged to SEL	
6	C	CPU / MMR Overinstall (PS Insufficient Resources)	Error, event logged to SEL	
6	D	MB I2C Access Error (Sensor0)	Error, event logged to SEL	
6	E	MB I2C Access Error (Sensor1)	Error, event logged to SEL	
6	F	MB I2C Access Error (Voltage Margin0)	Error, event logged to SEL	
7	0	MB I2C Access Error (Voltage Margin1)	Error, event logged to SEL	Check SEL list
7	1	MB I2C Access Error (Clock Generator)	Error, event logged to SEL	Check SEL list
7	2	MB PLL Lock Error (NDC30)	Error, event logged to SEL	
7	3	MB PLL Lock Error (NDC31)	Error, event logged to SEL	
7	4	MMR0 Power Failure	Error, event logged to SEL	
7	5	MMR1 Power Failure	Error, event logged to SEL	
7	6	MMR2 Power Failure	Error, event logged to SEL	
7	7	MMR3 Power Failure	Error, event logged to SEL	
7	8	MMR0 Removed (Wrong Operation)	Error, event logged to SEL	

No.	Code	Description	Classification	Operation to Recover
7	9	MMR1 Removed (Wrong Operation)	Error, event logged to SEL	
7	A	MMR2 Removed (Wrong Operation)	Error, event logged to SEL	
7	B	MMR3 Removed (Wrong Operation)	Error, event logged to SEL	
7	C	CPU0 Configuration Error (Installation Rule)	Error, event logged to SEL	
7	D	CPU1 Configuration Error (Installation Rule)	Error, event logged to SEL	
7	E	CPU2 Configuration Error (Installation Rule)	Error, event logged to SEL	
7	F	Chassis Intrusion detected	Error, event logged to SEL	
8	X	(reserved)		
9	0	Multiple Machine Check Interrupt	Error, event logged to SEL	Check SEL list
9	1	MB Config Access Error (NDC30)	Error, event logged to SEL	Check SEL list
9	2	MB Config Access Error (NDC31)	Error, event logged to SEL	
9	3	MB Config Access Error (ESB2)	Error, event logged to SEL	
9	4	MB Config Access Error (PXH)	Error, event logged to SEL	
9	5	MB HSCP Link Error (NDC30 / Port1)	Error, event logged to SEL	
9	6	MB HSCP Link Error (NDC31 / Port1)	Error, event logged to SEL	
9	7	MB Bit Deskew Latency Error (NDC30 / Port0)	Error, event logged to SEL	
9	8	MB Bit Deskew Latency Error (NDC30 / Port1)	Error, event logged to SEL	
9	9	MB Bit Deskew Latency Error (NDC30 / Port2)	Error, event logged to SEL	
9	A	MB Bit Deskew Latency Error (NDC31 / Port0)	Error, event logged to SEL	
9	B	MB Bit Deskew Latency Error (NDC31 / Port1)	Error, event logged to SEL	
9	C	MB Bit Deskew Latency Error (NDC31 / Port2)	Error, event logged to SEL	
9	D	MB PCI Express Link Error	Error, event logged to SEL	
9	E	MB Illegal Machine Check Interrupt	Error, event logged to SEL	
9	F	(reserved)		
A	0	HDDPL I2C Access Error (SEEPROM)	Error, event logged to SEL	
A	2	(reserved)		
A	3	(reserved)		
A	4	(reserved)		
A	5	(reserved)		
A	6	(reserved)		
A	7	(reserved)		
A	8	(reserved)		
A	9	(reserved)		
A	A	(reserved)		
A	B	(reserved)		
A	C	(reserved)		
A	D	(reserved)		
A	E	(reserved)		
A	F	(reserved)		
B	7	(reserved)		
B	8	(reserved)		
B	9	(reserved)		

No.	Code	Description	Classification	Operation to Recover
B	A	(reserved)		
B	B	(reserved)		
B	C	(reserved)		
B	D	(reserved)		
B	E	(reserved)		
B	F	(reserved)		
C	X	(reserved)		
D	X	(reserved)		
E	X	(reserved)		
F	X	(reserved)		

Table 39. POST Code Generated by SAL and Logged at Seven-Segment LED

No	Code	Description	Classification	Operation to Recover
1	100	BSP selection HW Mutex service initialization Non-Volatile memory service initialization AP synchronization control Chipset low level initialization PAL status check	Progress	Check previous SEL
2	1EB	RTC initialization	Progress	
3	1E3	Super IO initialization	Progress	
4	1EA	Console initialization	Progress	
5	1F5	Chipset initialization Memory initialization	Progress	
6	1F4	Recovery SAL Data Area initialization	Progress	
7	1EC	SAL_A shadowing Both BSP and AP jump to the shadowing code.	Progress	
8	1E2	Decides whether recovery is necessary or not.	Progress	
9	1E4	Decides whether recovery is necessary or not.	Progress	
10	1E6	FIT checksums	Progress	
11	1E7	Recovery POST termination	Progress	
12	006	Finalize memory layout Memory Attribute Register initialization	Progress	
13	016	SAL Data Area initialization	Progress	
14	014	SAL shadowing	Progress	
15	0F2	FREQ_BASE acquisition	Progress	
16	013	PAL shadowing	Progress	
17	012	IA32BIOS shadowing	Progress	

No	Code	Description	Classification	Operation to Recover
18	029	Wakes up an AP. Executes and guards AP self test. This code itself directly calls and initializes the POST task for AP self test. Reboots the memory or processor that has errored.	Progress	
19	0F1	Memory-based Mutex* service initialization	Progress	Check previous SEL
20	0F0	Runtime memory allocator initialization	Progress	
21	0D1	Error Record Buffer initialization	Progress	
22	0D2	MCA handler initialization	Progress	
23	033	Initialize interrupt vector table (IVT).	Progress	
24	0CB	Multiple Host Bus Bridge initialization	Progress	
25	0D6	PCI initialization	Progress	
26	001	Transfer to the virtual mode	Progress	
27	015	IA32BIOS execution	Progress	
28	004	Transfer to the physical mode	Progress	
29	0F8	Initialize IDE controller	Progress	
30	0F4	PCI initialization after returning from IA32 BIOS	Progress	
31	0F3	RAS late initialization	Progress	
32	0F5	clear error flags in chipset	Progress	
33	0D0	EFI code shadowing EFI execution	Progress	
34	AF~15	EFI POST task execution	Progress	

Table 40. Error POST Code Generated by SAL

No	Code	Description	Classification	Operation to Recover
1	0xC000～0xC003	CPU0 failure	Error	Check SEL list
2	0xC004～0xC007	CPU1 failure	Error	
3	0xC008～0xC00B	CPU2 failure	Error	
4	0xC00C～0xC00F	CPU3 failure	Error	
5	0xC020～0xC021	Chipset(NDC3) failure	Error	
6	0xC030	FWH failure	Error	
7	0xC037	Unsupported processor loads in board	Error	
8	0xC03F	FWH failure	Error	
9	0xC081	Detected illegal DIMM loading pattern or unsupported DIMM.	Error	
10	0xC082	No usable memory	Error	
11	0xC08B	Memory Controller failure	Error	
12	0xC0D0	Some trouble module were detected.	Error	
13	0x8002	Unexpected failure	Error	Check previous SEL

No	Code	Description	Classification	Operation to Recover
14	0x8003	Unexpected failure	Error	
15	0x8004	Chipset (NDC3) failure	Error	
16	0x8005	Processor failure	Error	
17	0x8006	Processor failure	Error	
18	0x8008	Unexpected failure	Error	
19	0x800A	Unexpected failure	Error	
20	0x800B	Unexpected failure	Error	
21	0x800C	Unexpected failure	Error	
22	0x8014	Unexpected failure	Error	
23	0x8015	Unexpected failure	Error	
24	0x8016	Unexpected failure	Error	
25	0x8017	Unexpected failure	Error	
26	0x8018	Unexpected failure	Error	
27	0x8019	Unexpected failure	Error	
28	0x8020	Unexpected failure	Error	
29	0xC086	Unexpected failure detected while initializing memory.	Error	
30	0xC090～C092	OS machine check handler is not registered or not valid	Error	Please check previous SEL
31	0xC0E0	Unexpected failure	Error	
32	0xC0E1	Unexpected failure in the SAL machine check handler.	Error	
33	0xC0E2	Unexpected failure in the SAL machine check handler.	Error	
34	0xC0E3	Unexpected failure in the SAL machine check handler.	Error	
35	0xC0E4	Unexpected failure in the SAL machine check handler.	Error	
36	0xC0E6	Unexpected failure	Error	
37	0xA108	Unexpected failure in the machine check handler.	Error	

Appendix C: Sensor Tables

Table 41. BMC Sensor Table

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0001	MB Temp0, 30	Assert	Upper Critical going-high	20 00	01	01	59 - XX - XX		Warning message. MB Temperature0 Upper Critical. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation.
0002	MB Temp0, 30	Assert	Upper Non-recoverable going-high	20 00	01	01	5B - XX - XX		Error message. MB Temperature0 Upper Non-recoverable. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation. Replace MB.
0003	MB Temp0, 30	Deassert	Upper Critical going-high	20 00	01	81	59 - XX - XX		Informational message. MB Temperature0 Upper Critical Deassert. No action necessary.
0004	MB Temp0	Deassert	Upper Non-recoverable going-high	20 00	01	81	5B - XX - XX		Informational message. MB Temperature0 Upper Non-recoverable Deassert. No action necessary.
0005	MB Temp1, 31	Assert	Upper Critical going-high	20 00	01	01	59 - XX - XX		Warning message. MB Temperature1 Upper Critical. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation.
0006	MB Temp1, 31	Assert	Upper Non-recoverable going-high	20 00	01	01	5B - XX - XX		Error message. MB Temperature1 Upper Non-recoverable. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation. Replace MB.
0007	MB Temp1, 31	Deassert	Upper Critical going-high	20 00	01	81	59 - XX - XX		Informational message. MB Temperature1 Upper Critical Deassert. ; No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0008	MB Temp1, 31	Deassert	Upper Non-recoverable going-high	20 00	01	81	5B - XX - XX		Informational message. MB Temperature1 Upper Non-recoverable Deassert. No action necessary.
0009	Environment Temp, 32	Assert	Lower Critical going-low	20 00	01	01	52 - XX - XX		Warning message. Environment Temperature Lower Critical. Check room temperature.
0010	Environment Temp, 32	Assert	Upper Critical going-high	20 00	01	01	59 - XX - XX		Warning message. Environment Temperature Upper Critical. Check room temperature.
0011	Environment Temp, 32	Assert	Upper Non-recoverable going-high	20 00	01	01	5B - XX - XX		Error message. Environment Temperature Upper Non-recoverable. Check room temperature.
0012	Environment Temp, 32	Deassert	Lower Critical going-low	20 00	01	81	52 - XX - XX		Informational message. Environment Temperature Lower Critical Deassert. No action necessary.
0013	Environment Temp, 32	Deassert	Upper Critical going-high	20 00	01	81	59 - XX - XX		Informational message. Environment Temperature Upper Critical Deassert. No action necessary.
0014	Environment Temp, 32	Deassert	Upper Non-recoverable going-high	20 00	01	81	5B - XX - XX		Informational message. Environment Temperature Upper Non-recoverable Deassert. No action necessary.
0015	CPU0 Temp, 43	Assert	Upper Critical going-high	20 00	01	01	59 - XX - XX		Warming message. CPU0 Temperature Upper Critical. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation.
0016	CPU0 Temp, 43	Assert	Upper Non-recoverable going-high	20 00	01	01	5B - XX - XX		Error message. CPU0 Temperature Upper Non-recoverable. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation. Replace CPU0
0017	CPU0 Temp, 43	Deassert	Upper Critical going-high	20 00	01	81	59 - XX - XX		Informational message. CPU0 Temperature Upper Critical Deassert. No action necessary.
0018	CPU0 Temp, 43	Deassert	Upper Non-recoverable going-high	20 00	01	81	5B - XX - XX		Informational message. CPU0 Temperature Upper Non-recoverable Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0019	CPU1 Temp, 53	Assert	Upper Critical going-high	20 00	01	01	59 - XX - XX		Warning message. CPU1 Temperature Upper Critical. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation.
0020	CPU1 Temp, 53	Assert	Upper Non-recoverable going-high	20 00	01	01	5B - XX - XX		Error message. CPU1 Temperature Upper Non-recoverable. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation. Replace CPU1.
0021	CPU1 Temp, 53	Deassert	Upper Critical going-high	20 00	01	81	59 - XX - XX		Informational message. CPU1 Temperature Upper Critical Deassert. No action necessary.
0022	CPU1 Temp, 53	Deassert	Upper Non-recoverable going-high	20 00	01	81	5B - XX - XX		Informational message. CPU1 Temperature Upper Non-recoverable Deassert. No action necessary.
0023	CPU2 Temp, 63	Assert	Upper Critical going-high	20 00	01	01	59 - XX - XX		Warning message. CPU2 Temperature Upper Critical. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation.
0024	CPU2 Temp, 63	Assert	Upper Non-recoverable going-high	20 00	01	01	5B - XX - XX		Error message. CPU2 Temperature Upper Non-recoverable. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation. Replace CPU2.
0025	CPU2 Temp, 63	Deassert	Upper Critical going-high	20 00	01	81	59 - XX - XX		Informational message. CPU2 Temperature Upper Critical Deassert. No action necessary.
0026	CPU2 Temp, 63	Deassert	Upper Non-recoverable going-high	20 00	01	81	5B - XX - XX		Informational message. CPU2 Temperature Upper Non-recoverable Deassert. No action necessary.
0027	CPU3 Temp, 73	Assert	Upper Critical going-high	20 00	01	01	59 - XX - XX		Warning message. CPU3 Temperature Upper Critical. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0028	CPU3 Temp, 73	Assert	Upper Non-recoverable going-high	20 00	01	01	5B - XX - XX		Error message. CPU3 Temperature Upper Non-recoverable. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation. Replace CPU3.
0029	CPU3 Temp, 73	Deassert	Upper Critical going-high	20 00	01	81	59 - XX - XX		Informational message. CPU3 Temperature Upper Critical Deassert. No action necessary.
0030	CPU3 Temp, 73	Deassert	Upper Non-recoverable going-high	20 00	01	81	5B - XX - XX		Informational message. CPU3 Temperature Upper Non-recoverable Deassert. No action necessary.
0031	MB M12V, 23	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MB Main 12V Lower Critical. If PS0-1 Power Failure SEL is generated, give priority to it. Replace PS0, PS1. Replace MB.
0032	MB M12V, 23	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MB Main 12V Lower Non-recoverable. If PS0-1 Power Failure SEL is generated, give priority to it. Replace PS0, PS1. Replace MB.
0033	MB M12V, 23	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MB Main 12V Upper Critical. If PS0-1 Power Failure SEL is generated, give priority to it. Replace PS0, PS1. Replace MB
0034	MB M12V, 23	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MB Main 12V Upper Non-recoverable. If PS0-1 Power Failure SEL is generated, give priority to it. Replace PS0, PS1. Replace MB.
0035	MB M12V, 23	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MB Main 12V Lower Critical Deassert. No action necessary.
0036	MB M12V, 23	Deassert	Lower Non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MB Main 12V Lower Non-recoverable Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0037	MB M12V, 23	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MB Main 12V Upper Critical Deassert. No action necessary.
0038	MB M12V, 23	Deassert	Upper Non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MB Main 12V Upper Non-recoverable Deassert. No action necessary.
0039	MB M5.0V, 24	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MB Main 5.0V Lower Critical. Replace MB.
0040	MB M5.0V, 24	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MB Main 5.0V Lower Non-recoverable. Replace MB.
0041	MB M5.0V, 24	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MB Main 5.0V Upper Critical. Replace MB.
0042	MB M5.0V, 24	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MB Main 5.0V Upper Non-recoverable. Replace MB.
0043	MB M5.0V, 24	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MB Main 5.0V Lower Critical Deassert. No action necessary.
0044	MB M5.0V, 24	Deassert	Lower Non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MB Main 5.0V Lower Non-recoverable Deassert. No action necessary.
0045	MB M5.0V, 24	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MB Main 5.0V Upper Critical Deassert. No action necessary.
0046	MB M5.0V, 24	Deassert	Upper Non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MB Main 5.0V Upper Non-recoverable Deassert. No action necessary.
0047	MB M3.3V, 25	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MB Main 3.3V Lower Critical. Replace MB.
0048	MB M3.3V, 25	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MB Main 3.3V Lower Non-recoverable. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0049	MB M3.3V, 25	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MB Main 3.3V Upper Critical. Replace MB.
0050	MB M3.3V, 25	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MB Main 3.3V Upper Non-recoverable. Replace MB.
0051	MB M3.3V, 25	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MB Main 3.3V Lower Critical Deassert. No action necessary.
0052	MB M3.3V, 25	Deassert	Lower Non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MB Main 3.3V Lower Non-recoverable Deassert. No action necessary.
0053	MB M3.3V, 25	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MB Main 3.3V Upper Critical Deassert. No action necessary.
0054	MB M3.3V, 25	Deassert	Upper Non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MB Main 3.3V Upper Non-recoverable Deassert. No action necessary.
0055	MB M2.5V, 26	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Error message. MB Main 2.5V Lower Critical. Replace MB.
0056	MB M2.5V, 26	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MB Main 2.5V Lower Non-recoverable. Replace MB.
0057	MB M2.5V, 26	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MB Main 2.5V Upper Critical. Replace MB.
0058	MB M2.5V, 26	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MB Main 2.5V Upper Non-recoverable. Replace MB.
0059	MB M2.5V, 26	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MB Main 2.5V Lower Critical Deassert. No action necessary.
0060	MB M2.5V, 26	Deassert	Lower Non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MB Main 2.5V Lower Non-recoverable Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0061	MB M2.5V, 26	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MB Main 2.5V Upper Critical Deassert. No action necessary.
0062	MB M2.5V, 26	Deassert	Upper Non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MB Main 2.5V Upper Non-recoverable Deassert. No action necessary.
0063	MB M1.8V, 27	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MB Main 1.8V Lower Critical. Replace MB.
0064	MB M1.8V, 27	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MB Main 1.8V Lower Non-recoverable. Replace MB.
0065	MB M1.8V, 27	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MB Main 1.8V Upper Critical. Replace MB.
0066	MB M1.8V, 27	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MB Main 1.8V Upper Non-recoverable. Replace MB.
0067	MB M1.8V, 27	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MB Main 1.8V Lower Critical Deassert. No action necessary.
0068	MB M1.8V, 27	Deassert	Lower Non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MB Main 1.8V Lower Non-recoverable Deassert. No action necessary.
0069	MB M1.8V, 27	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MB Main 1.8V Upper Critical Deassert. No action necessary.
0070	MB M1.8V, 27	Deassert	Upper Non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MB Main 1.8V Upper Non-recoverable Deassert. No action necessary.
0071	MB M1.5V, 28	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MB Main 1.5V Lower Critical. Replace MB.
0072	MB M1.5V, 28	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MB Main 1.5V Lower Non-recoverable. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0073	MB M1.5V, 28	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MB Main 1.5V Upper Critical. Replace MB.
0074	MB M1.5V, 28	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		MB Main 1.5V Upper Non-recoverable. Replace MB.
0075	MB M1.5V, 28	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MB Main 1.5V Lower Critical Deassert. No action necessary.
0076	MB M1.5V, 28	Deassert	Lower Non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MB Main 1.5V Lower Non-recoverable Deassert. No action necessary.
0077	MB M1.5V, 28	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MB Main 1.5V Upper Critical Deassert. No action necessary.
0078	MB M1.5V, 28	Deassert	Upper Non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MB Main 1.5V Upper Non-recoverable Deassert. No action necessary.
0079	MB M1.2V0, 29	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MB Main 1.2V0 Lower Critical. Replace CPU0, CPU1. Replace MB.
0080	MB M1.2V0, 29	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MB Main 1.2V0 Lower Non-recoverable. Replace CPU0, CPU1. Replace MB.
0081	MB M1.2V0, 29	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MB Main 1.2V0 Upper Critical. Replace CPU0, CPU1. Replace MB.
0082	MB M1.2V0, 29	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MB Main 1.2V0 Upper Non-recoverable. Replace CPU0, CPU1. Replace MB.
0083	MB M1.2V0, 29	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MB Main 1.2V0 Lower Critical Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0084	MB M1.2V0, 29	Deassert	Lower Non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MB Main 1.2V0 Lower Non-recoverable Deassert. No action necessary.
0085	MB M1.2V0, 29	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MB Main 1.2V0 Upper Critical Deassert. No action necessary.
0086	MB M1.2V0, 29	Deassert	Upper Non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MB Main 1.2V0 Upper Non-recoverable Deassert. No action necessary.
0087	MB M1.2V1, 2A	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MB Main 1.2V1 Lower Critical. Replace CPU2, CPU3. Replace MB.
0088	MB M1.2V1, 2A	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MB Main 1.2V1 Lower Non-recoverable. Replace CPU2, CPU3. Replace MB.
0089	MB M1.2V1, 2A	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MB Main 1.2V1 Upper Critical. Replace CPU2, CPU3. Replace MB.
0090	MB M1.2V1, 2A	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MB Main 1.2V1 Upper Non-recoverable. Replace CPU2, CPU3. Replace MB.
0091	MB M1.2V1, 2A	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MB Main 1.2V1 Lower Critical Deassert. No action necessary.
0092	MB M1.2V1, 2A	Deassert	Lower Non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MB Main 1.2V1 Lower Non-recoverable Deassert. No action necessary.
0093	MB M1.2V1, 2A	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MB Main 1.2V1 Upper Critical Deassert. No action necessary.
0094	MB M1.2V1, 2A	Deassert	Upper Non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MB Main 1.2V1 Upper Non-recoverable Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0095	MB M1.2V2, 2B	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MB Main 1.2V2 Lower Critical. Replace MB.
0096	MB M1.2V2, 2B	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MB Main 1.2V2 Lower Non-recoverable. Replace MB.
0097	MB M1.2V2, 2B	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MB Main 1.2V2 Upper Critical. Replace MB.
0098	MB M1.2V2, 2B	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MB Main 1.2V2 Upper Non-recoverable. Replace MB.
0099	MB M1.2V2, 2B	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MB Main 1.2V2 Lower Critical Deassert. No action necessary.
0100	MB M1.2V2, 2B	Deassert	Lower Non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MB Main 1.2V2 Lower Non-recoverable Deassert. No action necessary.
0101	MB M1.2V2, 2B	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MB Main 1.2V2 Upper Critical Deassert. No action necessary.
0102	MB M1.2V2, 2B	Deassert	Upper Non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MB Main 1.2V2 Upper Non-recoverable Deassert. No action necessary.
0103	MB M-12V, 2C	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MB Main -12V Lower Critical. If SLOT1-6 Fault Status Asserted SEL is generated, give priority to it. Replace MB.
0104	MB M-12V, 2C	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MB Main -12V Lower Non-recoverable. If SLOT1-6 Fault Status Asserted SEL is generated, give priority to it. Replace MB.
0105	MB M-12V, 2C	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MB Main -12V Upper Critical. If SLOT1-6 Fault Status Asserted SEL is generated, give priority to it. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0106	MB M-12V, 2C	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MB Main -12V Upper Non-recoverable. If SLOT1-6 Fault Status Asserted SEL is generated, give priority to it. Replace MB.
0107	MB M-12V, 2C	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MB Main -12V Lower Critical Deassert. No action necessary.
0108	MB M-12V, 2C	Deassert	Lower Non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MB Main -12V Lower Non-recoverable Deassert. No action necessary.
0109	MB M-12V, 2C	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MB Main -12V Upper Critical Deassert. No action necessary.
0110	MB M-12V, 2C	Deassert	Upper Non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MB Main -12V Upper Non-recoverable Deassert. No action necessary.
0111	HDDPL M12V0, 2D	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. HDDPL Main 12V0 Lower Critical. Replace MB, HDDPL.
0112	HDDPL M12V0, 2D	Assert	Lower Non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. HDDPL Main 12V0 Lower Non-recoverable. Replace MB, HDDPL.
0113	HDDPL M12V0, 2D	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. HDDPL Main 12V0 Upper Critical. Replace MB, HDDPL.
0114	HDDPL M12V0, 2D	Assert	Upper Non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. HDDPL Main 12V0 Upper Non-recoverable. Replace MB, HDDPL.
0115	HDDPL M12V0, 2D	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. HDDPL Main 12V0 Lower Critical Deassert. No action necessary.
0116	HDDPL M12V0, 2D	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. HDDPL Main 12V0 Lower Non-recoverable Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0117	HDDPL M12V0, 2D	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. HDDPL Main 12V0 Upper Critical Deassert. No action necessary.
0118	HDDPL M12V0, 2D	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. HDDPL Main 12V0 Upper Non-recoverable Deassert. No action necessary.
0119	HDDPL M12V1, 2E	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. HDDPL Main 12V1 Lower Critical. Replace MB, HDDPL.
0120	HDDPL M12V1, 2E	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. HDDPL Main 12V1 Lower Non-recoverable. Replace MB, HDDPL.
0121	HDDPL M12V1, 2E	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. HDDPL Main 12V1 Upper Critical. Replace MB, HDDPL.
0122	HDDPL M12V1, 2E	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. HDDPL Main 12V1 Upper Non-recoverable. Replace MB, HDDPL.
0123	HDDPL M12V1, 2E	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. HDDPL Main 12V1 Lower Critical Deassert. No action necessary.
0124	HDDPL M12V1, 2E	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. HDDPL Main 12V1 Lower Non-recoverable Deassert. No action necessary.
0125	HDDPL M12V1, 2E	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. HDDPL Main 12V1 Upper Critical Deassert. No action necessary.
0126	HDDPL M12V1, 2E	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. HDDPL Main 12V1 Upper Non-recoverable Deassert. No action necessary.
0126A	HDDPL S3.3V, 2F	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. HDDPL Sub 3.3V Lower Critical. Replace MB, HDDPL.
0126B	HDDPL S3.3V, 2F	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. HDDPL Sub 3.3V Lower Non-recoverable. Replace MB, HDDPL.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0126C	HDDPL S3.3V, 2F	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. HDDPL Sub 3.3V Upper Critical. Replace MB, HDDPL.
0126D	HDDPL S3.3V, 2F	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. HDDPL Sub 3.3V Upper Non-recoverable. Replace MB, HDDPL.
0126E	HDDPL S3.3V, 2F	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. HDDPL Sub 3.3V Lower Critical Deassert. No action necessary.
0126F	HDDPL S3.3V, 2F	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. HDDPL Sub 3.3V Lower Non-recoverable Deassert. No action necessary.
0126G	HDDPL S3.3V, 2F	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. HDDPL Sub 3.3V Upper Critical Deassert. No action necessary.
0126H	HDDPL S3.3V, 2F	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. HDDPL Sub 3.3V Upper Non-recoverable Deassert. No action necessary.
0127	MMR0 M3.3V, 83	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR0 Main 3.3V Lower Critical. Replace MMR0. Replace MB.
0128	MMR0 M3.3V, 83	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR0 Main 3.3V Lower Non-recoverable. Replace MMR0. Replace MB.
0129	MMR0 M3.3V, 83	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR0 Main 3.3V Upper Critical. Replace MMR0. Replace MB.
0130	MMR0 M3.3V, 83	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR0 Main 3.3V Upper Non-recoverable. Replace MMR0. Replace MB.
0131	MMR0 M3.3V, 83	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR0 Main 3.3V Lower Critical Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0132	MMR0 M3.3V, 83	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR0 Main 3.3V Lower Non-recoverable Deassert. No action necessary.
0133	MMR0 M3.3V, 83	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR0 Main 3.3V Upper Critical Deassert. No action necessary.
0134	MMR0 M3.3V, 83	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR0 Main 3.3V Upper Non-recoverable Deassert. No action necessary.
0135	MMR0 M1.8V, 84	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR0 Main 1.8V Lower Critical. Replace MMR0. Replace MB.
0136	MMR0 M1.8V, 84	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR0 Main 1.8V Lower Non-recoverable. Replace MMR0. Replace MB.
0137	MMR0 M1.8V, 84	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR0 Main 1.8V Upper Critical. Replace MMR0. Replace MB.
0138	MMR0 M1.8V, 84	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR0 Main 1.8V Upper Non-recoverable. Replace MMR0. Replace MB.
0139	MMR0 M1.8V, 84	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR0 Main 1.8V Lower Critical Deassert. No action necessary.
0140	MMR0 M1.8V, 84	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR0 Main 1.8V Lower Non-recoverable Deassert. No action necessary.
0141	MMR0 M1.8V, 84	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR0 Main 1.8V Upper Critical Deassert. No action necessary.
0142	MMR0 M1.8V, 84	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR0 Main 1.8V Upper Non-recoverable Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0143	MMR0 M1.5V, 85	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR0 Main 1.5V Lower Critical. Replace MMR0. Replace MB.
0144	MMR0 M1.5V, 85	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR0 Main 1.5V Lower Non-recoverable. Replace MMR0. Replace MB.
0145	MMR0 M1.5V, 85	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR0 Main 1.5V Upper Critical. Replace MMR0. Replace MB.
0146	MMR0 M1.5V, 85	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR0 Main 1.5V Upper Non-recoverable. Replace MMR0. Replace MB.
0147	MMR0 M1.5V, 85	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR0 Main 1.5V Lower Critical Deassert. No action necessary.
0148	MMR0 M1.5V, 85	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR0 Main 1.5V Lower Non-recoverable Deassert. No action necessary.
0149	MMR0 M1.5V, 85	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR0 Main 1.5V Upper Critical Deassert. No action necessary.
0150	MMR0 M1.5V, 85	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR0 Main 1.5V Upper Non-recoverable Deassert. No action necessary.
0151	MMR1 M3.3V, 93	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR1 Main 3.3V Lower Critical. Replace MMR1. Replace MB.
0152	MMR1 M3.3V, 93	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR1 Main 3.3V Lower Non-recoverable. Replace MMR1. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0153	MMR1 M3.3V, 93	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR1 Main 3.3V Upper Critical. Replace MMR1.; Replace MB.
0154	MMR1 M3.3V, 93	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR1 Main 3.3V Upper Non-recoverable. Replace MMR1. Replace MB.
0155	MMR1 M3.3V, 93	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR1 Main 3.3V Lower Critical Deassert. No action necessary.
0156	MMR1 M3.3V, 93	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR1 Main 3.3V Lower Non-recoverable Deassert. No action necessary.
0157	MMR1 M3.3V, 93	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR1 Main 3.3V Upper Critical Deassert. No action necessary.
0158	MMR1 M3.3V, 93	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR1 Main 3.3V Upper Non-recoverable Deassert. No action necessary.
0159	MMR1 M1.8V, 94	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR1 Main 1.8V Lower Critical. Replace MMR1. Replace MB.
0160	MMR1 M1.8V, 94	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR1 Main 1.8V Lower Non-recoverable. Replace MMR1.; Replace MB.
0161	MMR1 M1.8V, 94	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR1 Main 1.8V Upper Critical. Replace MMR1. Replace MB.
0162	MMR1 M1.8V, 94	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR1 Main 1.8V Upper Non-recoverable. Replace MMR1. Replace MB.
0163	MMR1 M1.8V, 94	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR1 Main 1.8V Lower Critical Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0164	MMR1 M1.8V, 94	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR1 Main 1.8V Lower Non-recoverable Deassert. No action necessary.
0165	MMR1 M1.8V, 94	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR1 Main 1.8V Upper Critical Deassert. No action necessary.
0166	MMR1 M1.8V, 94	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR1 Main 1.8V Upper Non-recoverable Deassert. No action necessary.
0167	MMR1 M1.5V, 95	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR1 Main 1.5V Lower Critical. Replace MMR1. Replace MB.
0168	MMR1 M1.5V, 95	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR1 Main 1.5V Lower Non-recoverable. Replace MMR1. Replace MB.
0169	MMR1 M1.5V, 95	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR1 Main 1.5V Upper Critical. Replace MMR1. Replace MB.
0170	MMR1 M1.5V, 95	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR1 Main 1.5V Upper Non-recoverable. Replace MMR1. Replace MB.
0171	MMR1 M1.5V, 95	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR1 Main 1.5V Lower Critical Deassert. No action necessary.
0172	MMR1 M1.5V, 95	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR1 Main 1.5V Lower Non-recoverable Deassert. No action necessary.
0173	MMR1 M1.5V, 95	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR1 Main 1.5V Upper Critical Deassert. No action necessary.
0174	MMR1 M1.5V, 95	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR1 Main 1.5V Upper Non-recoverable Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0175	MMR2 M3.3V, A3	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR2 Main 3.3V Lower Critical. Replace MMR2 Replace MB.
0176	MMR2 M3.3V, A3	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR2 Main 3.3V Lower Non-recoverable. Replace MMR2. Replace MB.
0177	MMR2 M3.3V, A3	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR2 Main 3.3V Upper Critical. Replace MMR2. Replace MB.
0178	MMR2 M3.3V, A3	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR2 Main 3.3V Upper Non-recoverable. Replace MMR2. Replace MB.
0179	MMR2 M3.3V, A3	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR2 Main 3.3V Lower Critical Deassert. No action necessary.
0180	MMR2 M3.3V, A3	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR2 Main 3.3V Lower Non-recoverable Deassert. No action necessary.
0181	MMR2 M3.3V, A3	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR2 Main 3.3V Upper Critical Deassert. No action necessary.
0182	MMR2 M3.3V, A3	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR2 Main 3.3V Upper Non-recoverable Deassert. No action necessary.
0183	MMR2 M1.8V, A4	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR2 Main 1.8V Lower Critical. Replace MMR2. Replace MB.
0184	MMR2 M1.8V, A4	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR2 Main 1.8V Lower Non-recoverable. Replace MMR2. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0185	MMR2 M1.8V, A4	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR2 Main 1.8V Upper Critical. Replace MMR2.; Replace MB.
0186	MMR2 M1.8V, A4	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR2 Main 1.8V Upper Non-recoverable. Replace MMR2. Replace MB.
0187	MMR2 M1.8V, A4	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR2 Main 1.8V Lower Critical Deassert. No action necessary.
0188	MMR2 M1.8V, A4	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR2 Main 1.8V Lower Non-recoverable Deassert. No action necessary.
0189	MMR2 M1.8V, A4	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR2 Main 1.8V Upper Critical Deassert. No action necessary.
0190	MMR2 M1.8V, A4	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR2 Main 1.8V Upper Non-recoverable Deassert. No action necessary.
0191	MMR2 M1.5V, A5	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR2 Main 1.5V Lower Critical. Replace MMR2. Replace MB.
0192	MMR2 M1.5V, A5	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR2 Main 1.5V Lower Non-recoverable. ; Replace MMR2. Replace MB.
0193	MMR2 M1.5V, A5	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR2 Main 1.5V Upper Critical. Replace MMR2. Replace MB.
0194	MMR2 M1.5V, A5	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR2 Main 1.5V Upper Non-recoverable. Replace MMR2. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0195	MMR2 M1.5V, A5	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR2 Main 1.5V Lower Critical Deassert. No action necessary.
0196	MMR2 M1.5V, A5	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR2 Main 1.5V Lower Non-recoverable Deassert. No action necessary.
0197	MMR2 M1.5V, A5	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR2 Main 1.5V Upper Critical Deassert. No action necessary.
0198	MMR2 M1.5V, A5	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR2 Main 1.5V Upper Non-recoverable Deassert. No action necessary.
0199	MMR3 M3.3V, B3	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR3 Main 3.3V Lower Critical. Replace MMR3. Replace MB.
0200	MMR3 M3.3V, B3	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR3 Main 3.3V Lower Non-recoverable. Replace MMR3. Replace MB.
0201	MMR3 M3.3V, B3	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR3 Main 3.3V Upper Critical. Replace MMR3. Replace MB.
0202	MMR3 M3.3V, B3	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR3 Main 3.3V Upper Non-recoverable. Replace MMR3. Replace MB.
0203	MMR3 M3.3V, B3	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR3 Main 3.3V Lower Critical Deassert. No action necessary.
0204	MMR3 M3.3V, B3	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR3 Main 3.3V Lower Non-recoverable Deassert. No action necessary.
0205	MMR3 M3.3V, B3	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR3 Main 3.3V Upper Critical Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0206	MMR3 M3.3V, B3	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR3 Main 3.3V Upper Non-recoverable Deassert. No action necessary.
0207	MMR3 M1.8V, B4	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR3 Main 1.8V Lower Critical. Replace MMR3. Replace MB.
0208	MMR3 M1.8V, B4	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR3 Main 1.8V Lower Non-recoverable. Replace MMR3. Replace MB.
0209	MMR3 M1.8V, B4	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR3 Main 1.8V Upper Critical. Replace MMR3. Replace MB.
0210	MMR3 M1.8V, B4	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR3 Main 1.8V Upper Non-recoverable. Replace MMR3. Replace MB.
0211	MMR3 M1.8V, B4	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR3 Main 1.8V Lower Critical Deassert. No action necessary.
0212	MMR3 M1.8V, B4	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR3 Main 1.8V Lower Non-recoverable Deassert. No action necessary.
0213	MMR3 M1.8V, B4	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR3 Main 1.8V Upper Critical Deassert. No action necessary.
0214	MMR3 M1.8V, B4	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR3 Main 1.8V Upper Non-recoverable Deassert. No action necessary.
0215	MMR3 M1.5V, B5	Assert	Lower Critical going-low	20 00	02	01	52 - XX - XX		Warning message. MMR3 Main 1.5V Lower Critical. Replace MMR3. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0216	MMR3 M1.5V, B5	Assert	Lower non-recoverable going-low	20 00	02	01	54 - XX - XX		Error message. MMR3 Main 1.5V Lower Non-recoverable. Replace MMR3. Replace MB.
0217	MMR3 M1.5V, B5	Assert	Upper Critical going-high	20 00	02	01	59 - XX - XX		Warning message. MMR3 Main 1.5V Upper Critical. Replace MMR3. Replace MB.
0218	MMR3 M1.5V, B5	Assert	Upper non-recoverable going-high	20 00	02	01	5B - XX - XX		Error message. MMR3 Main 1.5V Upper Non-recoverable. Replace MMR3. Replace MB.
0219	MMR3 M1.5V, B5	Deassert	Lower Critical going-low	20 00	02	81	52 - XX - XX		Informational message. MMR3 Main 1.5V Lower Critical Deassert. No action necessary.
0220	MMR3 M1.5V, B5	Deassert	Lower non-recoverable going-low	20 00	02	81	54 - XX - XX		Informational message. MMR3 Main 1.5V Lower Non-recoverable Deassert. No action necessary.
0221	MMR3 M1.5V, B5	Deassert	Upper Critical going-high	20 00	02	81	59 - XX - XX		Informational message. MMR3 Main 1.5V Upper Critical Deassert. No action necessary.
0222	MMR3 M1.5V, B5	Deassert	Upper non-recoverable going-high	20 00	02	81	5B - XX - XX		Informational message. MMR3 Main 1.5V Upper Non-recoverable Deassert. No action necessary.
0223	FAN0 Tach, E0	Assert	Lower Critical going-low	20 00	04	01	52 - XX - XX		Error message. FAN0 Tach Lower Critical. Replace FAN0. Replace MB.
0224	FAN0 Tach, E0	Deassert	Lower Critical going-low	20 00	04	81	52 - XX - XX		Informational message. FAN0 Tach Lower Critical Deassert. No action necessary.
0225	FAN1 Tach, E1	Assert	Lower Critical going-low	20 00	04	01	52 - XX - XX		Error message. FAN1 Tach Lower Critical. Replace FAN1. Replace MB.
0226	FAN1 Tach, E1	Deassert	Lower Critical going-low	20 00	04	81	52 - XX - XX		Informational message. FAN1 Tach Lower Critical Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0227	FAN2 Tach, E2	Assert	Lower Critical going-low	20 00	04	01	52 - XX - XX		Error message. FAN2 Tach Lower Critical. Replace FAN2. Replace MB.
0228	FAN2 Tach, E2	Deassert	Lower Critical going-low	20 00	04	81	52 - XX - XX		Informational message. FAN2 Tach Lower Critical Deassert. No action necessary.
0229	FAN3 Tach, E3	Assert	Lower Critical going-low	20 00	04	01	52 - XX - XX		Error message. FAN3 Tach Lower Critical. Replace FAN3. Replace MB.
0230	FAN3 Tach, E3	Deassert	Lower Critical going-low	20 00	04	81	52 - XX - XX		Informational message. FAN3 Tach Lower Critical Deassert. No action necessary.
0231	FAN4 Tach, E4	Assert	Lower Critical going-low	20 00	04	01	52 - XX - XX		Error message. FAN4 Tach Lower Critical. Replace FAN4 Replace MB.
0232	FAN4 Tach, E4	Deassert	Lower Critical going-low	20 00	04	81	52 - XX - XX		Informational message. FAN4 Tach Lower Critical Deassert. No action necessary.
0233	FAN5 Tach, E5	Assert	Lower Critical going-low	20 00	04	01	52 - XX - XX		Error message. FAN5 Tach Lower Critical. Replace FAN5. Replace MB.
0234	FAN5 Tach, E5	Deassert	Lower Critical going-low	20 00	04	81	52 - XX - XX		Informational message.FAN5 Tach Lower Critical Deassert. No action necessary.
0235	CPU0, 40	Assert	Thermal Trip	20 00	07	6F	01 - FF - FF	40	Error message. CPU0 Thermal Trip. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation. Replace CPU0.
0236	CPU0, 40	Assert	Processor Disabled	20 00	07	6F	08 - FF - FF		Error message. CPU0 Disabled. Replace CPU0.
0237	CPU0, 40	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 00	41	Error message. CPU0 Configuration Error (Absent). All CPU slots are empty. Replace CPU0.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0238	CPU0, 40	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 02	42	Error message. CPU0 Configuration Error (Disabled). All CPUs are disabled. Replace CPU0.
0239	CPU0, 40	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 03	43	Error message. CPU0 Configuration Error (Illegal Type). CPU0 is WB unsupported type. Replace CPU0 with WB supported type.
0239A	CPU0, 40	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 03	7C	Error message. CPU0 Configuration Error (Installation Rule). CPU0 slot is empty. Install supported processor.
0240	CPU0 Init Error, 41	Assert	Transition to non-recoverable from less serve	20 00	07	07	A3 - 03 - 40	44	Error message. CPU0 I2C Access Error (PIROM). Replace CPU0. Replace MB.
0241	CPU0 Init Error, 41	Assert	Transition to non-recoverable from less serve	20 00	07	07	A3 - 03 - 41	45	Error message. CPU0 I2C Access Error (Temperature Monitor). Replace CPU0. Replace MB.
0242	CPU1, 50	Assert	Thermal Trip	20 00	07	6F	01 - FF - FF	46	Error message. CPU1 Thermal Trip. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation. Replace CPU1.
0243	CPU1, 50	Assert	Processor Disabled	20 00	07	6F	08 - FF - FF		Error message. CPU1 Disabled. Replace CPU1.
0244	CPU1, 50	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 11	47	Error message. CPU1 Configuration Error (Disabled). All CPUs are disabled. (Include CPU1). Replace CPU1.
0245	CPU1, 50	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 12	48	Error message. CPU1 Configuration Error (Illegal Type). CPU1 is WB unsupported type. Replace CPU1 with WB supported type.
0246	CPU1, 50	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 13	49	Error message. CPU1 Configuration Error (Different Type). CPU1 is different type from CPU0. Replace CPU1 with same type as CPU0.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0246A	CPU1, 50	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 14	7D	Error message. CPU1 Configuration Error (Installation Rule). CPU1 socket is empty. Install supported processor in CPU1 socket.
0247	CPU1 Init Error, 51	Assert	Transition to non-recoverable from less serve	20 00	07	07	A3 - 03 - 50	4A	Error message. CPU1 I2C Access Error (PIROM). Replace CPU1. Replace MB.
0248	CPU1 Init Error, 51	Assert	Transition to non-recoverable from less serve	20 00	07	07	A3 - 03 - 51	4B	Error message. CPU1 I2C Access Error (Temperature Monitor). Replace CPU1. Replace MB.
0249	CPU2, 60	Assert	Thermal Trip	20 00	07	6F	01 - FF - FF	4C	Error message. CPU2 Thermal Trip. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation. Replace CPU2.
0250	CPU2, 60	Assert	Processor Disabled	20 00	07	6F	08 - FF - FF		Error message. CPU2 Disabled. Replace CPU2.
0251	CPU2, 60	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 21	4D	Error message. CPU2 Configuration Error (Disabled). All CPUs are disabled. (Include CPU2).; Replace CPU2.
0252	CPU2, 60	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 22	4E	Error message. CPU2 Configuration Error (Illegal Type). CPU2 is WB unsupported type. Replace CPU2 with WB supported type.
0253	CPU2, 60	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 23	4F	Error message. CPU2 Configuration Error (Different Type). Replace CPU2 with same type as CPU0-1.
0253A	CPU2, 60	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 24	7E	Error message. CPU2 Configuration Error (Installation Rule). CPU2 socket is empty. Install supported processor in CPU2 socket.
0254	CPU2 Init Error, 61	Assert	Transition to non-recoverable from less serve	20 00	07	07	A3 - 03 - 60	50	Error message. CPU2 I2C Access Error (PIROM). Replace CPU2. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0255	CPU2 Init Error, 61	Assert	Transition to non-recoverable from less serve	20 00	07	07	A3 - 03 - 61	51	Error message. CPU2 I2C Access Error (Temperature Monitor). Replace CPU2. Replace MB.
0256	CPU3, 70	Assert	Thermal Trip	20 00	07	6F	01 - FF - FF	52	Error message. CPU3 Thermal Trip. If FAN0-5 Tach Lower Critical SEL is generated, give priority to it. Check chassis ventilation. Replace CPU3.
0257	CPU3, 70	Assert	Processor Disabled	20 00	07	6F	08 - FF - FF		Error message. CPU3 Disabled. Replace CPU3.
0258	CPU3, 70	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 31	53	Error message. CPU3 Configuration Error (Disabled). All CPUs are disabled. (Include CPU3). Replace CPU3.
0259	CPU3, 70	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 32	54	Error message. CPU3 Configuration Error (Illegal Type). CPU3 is WB unsupported type. Replace CPU3 with WB supported type.
0260	CPU3, 70	Assert	Configuration Error	20 00	07	6F	A5 - 0C - 33	55	Error message. CPU3 Configuration Error (Different Type). CPU3 is different type from CPU0-2. Replace CPU3 with same type as CPU0-2.
0261	CPU3 Init Error, 71	Assert	Transition to non-recoverable from less serve	20 00	07	07	A3 - 03 - 70	56	Error message. CPU3 I2C Access Error (PIROM). Replace CPU3. Replace MB.
0262	CPU3 Init Error, 71	Assert	Transition to non-recoverable from less serve	20 00	07	07	A3 - 03 - 71	57	Error message. CPU3 I2C Access Error (Temperature Monitor). Replace CPU3. Replace MB.
0263	MB Power Fail, 22	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 00	58	Error message. MB Power Failure (Main 5.0V). Replace MB.
0264	MB Power Fail, 22	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 01	59	Error message. MB Power Failure (Main 3.3V). Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0265	MB Power Fail, 22	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 02	5A	Error message. MB Power Failure (Main 2.5V). Replace MB.
0266	MB Power Fail, 22	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 03	5B	Error message. MB Power Failure (Main 1.8V). Replace MB.
0267	MB Power Fail, 22	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 04	5C	Error message. MB Power Failure (Main 1.5V). Replace MB.
0268	MB Power Fail, 22	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 05	5D	Error message. MB Power Failure (Main 1.2V0). Replace MB.
0269	MB Power Fail, 22	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 06	5E	Error message. MB Power Failure (Main 1.2V1). Replace MB.
0270	MB Power Fail, 22	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 07	5F	Error message. MB Power Failure (Main 1.2V2). Replace MB.
0271	MB Power Fail, 22	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 08	60	Error message. MB Power Failure (Voltage Type Unknown). Replace MB.
0272	MVR0 Power Fail, 42	Assert	Power Supply Failure Detected	20 00	08	6F	01 - FF - FF	61	Error message. MVR0 Power Failure. Check MVRCBL0 connection, CPU0 and MVR0 Installation. Replace MVRCBL0, MVR0. Replace MB.
0273	MVR1 Power Fail, 52	Assert	Power Supply Failure Detected	20 00	08	6F	01 - FF - FF	62	Error message. MVR1 Power Failure. Check MVRCBL0 connection, CPU1 and MVR1 Installation. Replace MVRCBL0, MVR1. Replace MB.
0274	MVR2 Power Fail, 62	Assert	Power Supply Failure Detected	20 00	08	6F	01 - FF - FF	63	Error message. MVR2 Power Failure. Check MVRCBL1 connection, CPU2 and MVR2 Installation. Replace MVRCBL1, MVR2. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0275	MVR3 Power Fail, 72	Assert	Power Supply Failure Detected	20 00	08	6F	01 - FF - FF	64	Error message. MVR3 Power Failure. Check MVRCBL1 connection, CPU3 and MVR3 Installation. Replace MVRCBL1, MVR3. Replace MB.
0276	MMR0 Power Fail, 82	Assert	Power Supply Failure Detected	20 00	08	6F	01 - FF - FF	74	Error message. MMR0 Power Failure. Replace MMR0. Replace MB.
0277	MMR1 Power Fail, 92	Assert	Power Supply Failure Detected	20 00	08	6F	01 - FF - FF	75	Error message. MMR1 Power Failure. Replace MMR1. Replace MB.
0278	MMR2 Power Fail, A2	Assert	Power Supply Failure Detected	20 00	08	6F	01 - FF - FF	76	Error message. MMR2 Power Failure. Replace MMR2. Replace MB.
0279	MMR3 Power Fail, B2	Assert	Power Supply Failure Detected	20 00	08	6F	01 - FF - FF	78	Error message. MMR3 Power Failure. Replace MMR3. Replace MB.
0280	PS0, C0	Assert	Configuration Error	20 00	08	6F	A6 - 0D - 00	65	Error message. PS0 Configuration Error (Absent). BMC did not find PS presence. Replace PS0.
0281	PS0, C0	Assert	Configuration Error	20 00	08	6F	A6 - 0D - 01	66	Error message. PS0 Configuration Error (Illegal Type). Replace PS0.
0282	PS0, C1	Assert	Configuration Error	20 00	08	6F	A6 - 0D - 02	67	Error message. PS0 Configuration Error (Insufficient Resources). Replace PS0.
0283	PS1, C1	Assert	Configuration Error	20 00	08	6F	A6 - 0D - 12	68	Error message. PS1 Configuration Error (Insufficient Resources). PS1 slot is empty. Replace PS1.
0284	PS1, C1	Assert	Configuration Error	20 00	08	6F	A6 - 0D - 13	69	Error message. PS1 Configuration Error (Different Type). PS1 is different type from PS0. Replace PS1 with same type as PS0.
0285	PS0 Hot Plug, C2	Assert	Device Removed	20 00	08	08	00 - FF - FF		Informational message. PS0 Removed. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0286	PS0 Hot Plug, C2	Assert	Device Inserted	20 00	08	08	01 - FF - FF		Informational message.PS0 Inserted. No action necessary.
0287	PS1 Hot Plug, C3	Assert	Device Removed	20 00	08	08	00 - FF - FF		Informational message. PS1 Removed. No action necessary.
0288	PS1 Hot Plug, C3	Assert	Device Inserted	20 00	08	08	01 - FF - FF		Informational message. PS1 Inserted. No action necessary.
0289	PS0 Power Fail, C4	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 20		Error message. PS0 Power Failure (Redundancy Lost). Check PSCBL0 connection. Replace PS0.
0290	PS0 Power Fail, C4	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 21	6A	Error message. PS0 Power Failure (Insufficient Resources). Check PSCBL0 connection. Replace PS0.
0291	PS0 Power Fail, C4	Deassert	Power Supply Failure Detected	20 00	08	EF	A1 - 01 - 22		Informational message. PS0 Power Failure Deassert. No action necessary.
0292	PS1 Power Fail, C5	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 30		Error message. PS1 Power Failure (Redundancy Lost). Check PSCBL1 connection. Replace PS1.
0293	PS1 Power Fail, C5	Assert	Power Supply Failure Detected	20 00	08	6F	A1 - 01 - 31	6B	Error message. PS1 Power Failure (Insufficient Resources). Check PSCBL1 connection. Replace PS1.
0294	PS1 Power Fail, C5	Deassert	Power Supply Failure Detected	20 00	08	EF	A1 - 01 - 32		Informational message. PS1 Power Failure Deassert. No action necessary.
0295	Cold Start, 00	Assert	AC Lost	20 00	09	6F	04 - FF - FF		Informational message. Cold Start (AC Lost). No action necessary.
0297	FAN Redundancy, E8	Assert	Redundancy Lost	20 00	0A	0B	01 - FF - FF		Informational message. FAN Redundancy Lost. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0298	FAN Redundancy, E8	Assert	Insufficient Resources	20 00	0A	0B	05 - FF - FF		Informational message. FAN Insufficient Resources. No action necessary.
0299	FAN Redundancy, E8	Deassert	Redundancy Lost	20 00	0A	8B	01 - FF - FF		Informational message. FAN Redundancy Lost Deassert. No action necessary.
0300	FAN Redundancy, E8	Deassert	Insufficient Resources	20 00	0A	8B	05 - FF - FF		Informational message. FAN Insufficient Resources Deassert. No action necessary.
0301	Boot Timeout, 06	Assert	System Firmware Hang	20 00	0F	6F	A1 - XX - XX		Error message. Boot Timeout (System Firmware Hang). Event Data 2-3: POST Code Check POST code (Maintenance action depends on POST code).
0302	OEM Event, 01	Assert	Transition to non-recoverable from less serve	20 00	12	07	A3 - 0A - 00	90	Error message. Multiple Machine Check Interrupt. Replace MB.
0303	OEM Event, 01	Assert	Transition to non-recoverable from less serve	20 00	12	07	A3 - 0B - 00		Error message. Machine Check Timeout. Replace MB.
0304	OEM Event, 01	Assert	Informational	20 00	12	07	A8 - 00 - 00		Informational message. BMC Restart (IPMI command). No action necessary.
0305	OEM Event, 01	Assert	Informational	20 00	12	07	A8 - 00 - 01		Informational message. BMC Restart (BMC Firmware Update). No action necessary.
0306	OEM Event, 01	Assert	Informational	20 00	12	07	A8 - 00 - 02		Informational message. BMC Restart (BMC Memory Re-initialize). No action necessary.
0307	OEM Event, 01	Assert	Informational	20 00	12	07	A8 - 00 - 10		Informational message. BMC Firmware Update. No action necessary.
0308	OEM Event, 01	Assert	Informational	20 00	12	07	A8 - 00 - 20		Informational message. SDINT Button Pressed. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0309	OEM Event, 01	Assert	Informational	20 00	12	07	A8 - 00 - 30		Informational message. CMOS Clear Mode Enter. No action necessary.
0310	OEM Event, 01	Assert	Informational	20 00	12	07	A8 - 00 - 31		Informational message. CMOS Clear Mode Exit. No action necessary.
0311	OEM Event, 01	Assert	Informational	20 00	12	07	A8 - 00 - 40		Informational message. FWH Emergency Recovery Mode Enter. No action necessary.
0312	OEM Event, 01	Assert	Informational	20 00	12	07	A8 - 00 - 41		Informational message. FWH Emergency Recovery Mode Exit. No action necessary.
0312A	OEM Event, 01	Assert	Informational	20 00	12	07	A8 - 00 - 50		Informational message. ACPI Power Button Event Emulation (Initiate Soft-shutdown). No action necessary.
0313	Hard Reset, 03	Assert	OEM System Boot Event	20 00	12	6F	01 - FF - FF		Informational message. Hard Reset (OEM System Boot Event). No action necessary.
0314	Soft Reset Critical Interrupt, 04	Assert	Front Panel NMI / Diagnostic Interrupt	20 00	13	6F	00 - FF - FF		Informational message. Dump Interrupt (Diagnostic Interrupt). No action necessary.
0315	Soft Reset Critical Interrupt, 04	Assert	Fatal NMI	20 00	13	6F	09 - FF - FF		Informational message. Machine Check Interrupt (Fatal NMI). No action necessary.
0316	Reset Button, 05	Assert	Reset Button Pressed	20 00	14	6F	02 - FF - FF		Informational message. Reset Button Pressed. No action necessary.
0317	BMC Board / Module Error, 20	Assert	Transition to non-critical from OK	20 00	15	07	A1 - 02 - 00		Warning message. BMC Error (BMC ROM Checksum Error). Update BMC firmware. Replace MB.
0318	BMC Board / Module Error, 20	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 02 - 20		Error message. BMC Error (BMC SRAM Parity Error). Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0319	BMC Board / Module Error, 20	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 02 - 30		Error message. BMC Error (BMC Watchdog Timer Expired). Replace MB.
0319A	BMC Board / Module Error, 20	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 0F - 00		Error message. Environment Temperature Sensor Disabled (Unsettled Value). Replace HDDPL, HDDCBL0.
0319B	BMC Board / Module Error, 20	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 0F - 01		Error message. Environment Temperature Sensor Disabled (Error Margin). Replace HDDPL, HDDCBL0.
0320	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 03 - 00		Error message. MB I2C Access Error (Fan Boost Control). Replace MB.
0321	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 03 - 20	6D	Error message. MB I2C Access Error (Sensor0). Replace MB.
0322	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 03 - 21	6E	Error message. MB I2C Access Error (Sensor1). Replace MB.
0323	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 03 - 22	6F	Error message. MB I2C Access Error (Voltage Margin0). Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0324	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 03 - 23	70	Error message. MB I2C Access Error (Voltage Margin1). Replace MB.
0325	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 03 - 24	71	Error message. MB I2C Access Error (Clock Generator). Replace MB.
0325A	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 03 - 30	71	Error message. HDDPL I2C Access Error (SEEPROM). Replace MB, HDDPL.
0325B	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 03 - 31	71	Error message. HDDPL I2C Access Error (Sensor). Replace MB, HDDPL.
0326	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 04 - 00	91	Error message. MB Config Access Error (NDC30). Replace MB.
0327	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 04 - 10	92	Error message. MB Config Access Error (NDC31). Replace MB.
0328	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 04 - 20	93	Error message. MB Config Access Error (ESB2). Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0329	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 04 - 30	94	Error message. MB Config Access Error (PXH). Replace MB.
0330	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 05 - 00	72	Error message. MB PLL Lock Error (NDC30). Replace MB.
0331	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 05 - 10	73	Error message. MB PLL Lock Error (NDC31). Replace MB.
0332	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 06 - 01	95	Error message. MB HSCP Link Error (NDC30 / Port1). Replace MB.
0333	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 06 - 11	96	Error message. MB HSCP Link Error (NDC31 / Port1). Replace MB.
0334	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 07 - 00	97	Error message. MB Bit Deskew Latency Error (NDC30 / Port0). Replace MB.
0335	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 07 - 01	98	Error message. MB Bit Deskew Latency Error (NDC30 / Port1). Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0336	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 07 - 02	99	Error message. MB Bit Deskew Latency Error (NDC30 / Port2). Replace MB.
0337	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 07 - 10	9A	Error message. MB Bit Deskew Latency Error (NDC31 / Port0). Replace MB.
0338	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 07 - 11	9B	Error message. MB Bit Deskew Latency Error (NDC31 / Port1). Replace MB.
0339	MB Init Error, 21	Assert	Transition to Non-recoverable from less serve	20 00	15	07	A3 - 07 - 12	9C	Error message. MB Bit Deskew Latency Error (NDC31 / Port2). Replace MB.
0340	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 08 - 00	9D	Error message. MB PCI Express Link Error. Replace MB.
0341	MB Init Error, 21	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 09 - 00	9E	Error message. MB Illegal Machine Check Interrupt. Replace MB.
0342	MMR0 Init Error, 81	Assert	Transition to non-recoverable from less severe error	20 00	15	07	A3 - 03 - 80		Error message. MMR0 I2C Access Error (Voltage Monitor). Replace MMR0. Replace MB.
0343	MMR0 Hot Plug, 86	Assert	Device Removed	20 00	15	08	A0 - 0E - 00		Informational message. MMR0 Removed (Correct Operation). No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0344	MMR0 Hot Plug, 86	Assert	Device Removed	20 00	15	08	A0 - 0E - 01	78	Informational message. MMR0 Removed (Wrong Operation). No action necessary.
0345	MMR0 Hot Plug, 86	Assert	Device Inserted	20 00	15	08	A1 - 0E - 02		Informational message. MMR0 Inserted. No action necessary.
0346	MMR1 Init Error, 91	Assert	Transition to non-recoverable from less serve	20 00	15	07	A3 - 03 - 90		Replace MMR1. MMR1 I2C Access Error (Voltage Monitor). Replace MB.
0347	MMR1 Hot Plug, 96	Assert	Device Removed	20 00	15	08	A0 - 0E - 10		Informational message. MMR1 Removed (Correct Operation). No action necessary.
0348	MMR1 Hot Plug, 96	Assert	Device Removed	20 00	15	08	A0 - 0E - 11	79	Informational message. MMR1 Removed (Wrong Operation). No action necessary.
0349	MMR1 Hot Plug, 96	Assert	Device Inserted	20 00	15	08	A0 - 0E - 12		Informational message. MMR1 Inserted. No action necessary.
0350	MMR2 Init Error, A1	Assert	Transition to non-recoverable from less serve	20 00	15	07	A3 - 03 - A0		Error message. MMR2 I2C Access Error (Voltage Monitor). Replace MMR2. Replace MB.
0351	MMR2 Hot Plug, A6	Assert	Device Removed	20 00	15	08	A0 - 0E - 20		Informational message. MMR2 Removed (Correct Operation). No action necessary.
0352	MMR2 Hot Plug, A6	Assert	Device Removed	20 00	15	08	A0 - 0E - 21	7A	Informational message. MMR2 Removed (Wrong Operation). No action necessary.
0353	MMR2 Hot Plug, A6	Assert	Device Inserted	20 00	15	08	A0 - 0E - 22		Informational message. MMR2 Inserted. No action necessary.
0354	MMR3 Init Error, B1	Assert	Transition to non-recoverable from less serve	20 00	15	07	A3 - 03 - B0		Error message. MMR3 I2C Access Error (Voltage Monitor). Replace MMR3. Replace MB.
0355	MMR3 Hot Plug, B6	Assert	Device Removed	20 00	15	08	A0 - 0E - 30		Informational message. MMR3 Removed (Correct Operation). No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0356	MMR3 Hot Plug, B6	Assert	Device Removed	20 00	15	08	A0 - 0E - 31	7B	Informational message. MMR3 Removed (Wrong Operation). No action necessary.
0357	MMR3 Hot Plug, B6	Assert	Device Inserted	20 00	15	08	A0 - 0E - 32		Informational message. MMR3 Inserted. No action necessary.
0358	SLOT1, D1	Assert	Fault Status Asserted	20 00	21	6F	00 - FF - FF		Error message. SLOT1 Fault. Replace SLOT1. Replace MB.
0359	SLOT1, D1	Deassert	Fault Status Asserted	20 00	21	EF	00 - FF - FF		Informational message. SLOT1 Fault Deassert. No action necessary.
0360	SLOT2, D2	Assert	Fault Status Asserted	20 00	21	6F	00 - FF - FF		Error message. SLOT2 Fault. Replace SLOT2. Replace MB.
0361	SLOT2, D2	Deassert	Fault Status Asserted	20 00	21	EF	00 - FF - FF		Informational message. SLOT2 Fault Deassert. No action necessary.
0362	SLOT3, D3	Assert	Fault Status Asserted	20 00	21	6F	00 - FF - FF		Error message. SLOT3 Fault. Replace SLOT3. Replace MB.
0363	SLOT3, D3	Deassert	Fault Status Asserted	20 00	21	EF	00 - FF - FF		Informational message. SLOT3 Fault Deassert. No action necessary.
0364	SLOT4, D4	Assert	Fault Status Asserted	20 00	21	6F	00 - FF - FF		Error message. SLOT4 Fault. Replace SLOT4. Replace MB.
0365	SLOT4, D4	Deassert	Fault Status Asserted	20 00	21	EF	00 - FF - FF		Informational message. SLOT4 Fault Deassert. No action necessary.
0366	SLOT5, D5	Assert	Fault Status Asserted	20 00	21	6F	00 - FF - FF		Error message. SLOT5 Fault. Replace SLOT5. Replace MB.
0367	SLOT5, D5	Deassert	Fault Status Asserted	20 00	21	EF	00 - FF - FF		Informational message. SLOT5 Fault Deassert. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Seg Code	Message Type, Description, Recovery Information
0368	SLOT6, D6	Assert	Fault Status Asserted	20 00	21	6F	00 - FF - FF		Error message. SLOT6 Fault. Replace SLOT6. Replace MB.
0369	SLOT6, D6	Deassert	Fault Status Asserted	20 00	21	EF	00 - FF - FF		Informational message. SLOT6 Fault Deassert. No action necessary.
0370	Power Up/Down, 02	Assert	S0 / G0 working	20 00	22	6F	00 - FF - FF		Informational message. Power Up (S0 / G0 "working"). No action necessary.
0371	Power Up/Down, 02	Assert	S5 / G2 soft-off	20 00	22	6F	05 - FF - FF		Informational message. Power Down (S5 / G2 soft-off). No action necessary.
0372	Watchdog Timer, 0D	Assert	Timer Expired	20 00	23	6F	XX - XX - XX		Informational message. Watchdog Timer Expired. No action necessary.
0373	BAT, 33	Assert	Battery Failed	20 00	29	6F	01 - FF - FF		Warning message. Battery Failed. Replace the battery.
0374	BAT, 33	Deassert	Battery Failed	20 00	29	EF	01 - FF - FF		Informational message. Battery Failed Deassert. No action necessary.

Table 42. IPMI SEL

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1001	Processor, 03	Assert	to Non-Critical from OK	01 00	07	07	A1 - CPU Socket ID - XX	Processor correctable error limit reached. CPU Socket ID: x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Warning message. This SEL message is logged when the error checker lights at the location other than the external bus. Replace CPUx.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1002	Processor, 03	Assert	Critical	01 00	07	07	A2 - CPU Socket ID - XX	Processor recoverable error. CPU Socket ID: x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Error message. This SEL message is logged when the error checker lights at the location other than external bus. Replace CPUx.
1003	Processor, 03	Assert	Non-recoverable	01 00	07	07	A3 - CPU Socket ID - XX	Processor fatal error. CPU Socket ID: x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Error message. This SEL message is logged when the error checker lights at the location other than external bus. Replace CPUx
1004	Processor, 03	Assert	Informational	01 00	07	07	A8 - CPU Socket ID - XX	Processor correctable error. CPU Socket ID x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Information This SEL message is logged when the error checker lights at the location other than external bus
1005	Processor, 04	Assert	FRB1/BIST Failure	01 00	07	6F	A2 - CPU Socket ID - XX	Processor Early/Late Self-test failure. CPU Socket ID: x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Error message. Replace CPUx
1006	Processor, 04	Assert	FRB2/Hang in POST failure	01 00	07	6F	A3 - CPU Socket ID - XX	Processor Hang in POST. CPU Socket ID: x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Error message. Replace CPUx
1006A1	Processor,	Assert	Processor Automatically Throttled	01 00	07	6F	AA - CPU Socket ID - XX	Processor Automatically Throttled. CPU Socket ID: x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Informational message. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1006A2	Processor, 04	Deassert	Processor Automatically Throttled	01 00	07	6F	AA - CPU Socket ID - XX	Processor Automatically Throttled Recovered. CPU Socket ID: x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Informational message. No action necessary.
1007	Processor, 04	Assert	FRB3/Processor Startup/Initialization failure (CPU Didn't start)	01 00	07	6F	A4 - CPU Socket ID - XX	Processor not hand-off to SAL. CPU Socket ID: x0 : CPU0 X1 : CPU1 x2 : CPU2 x3 : CPU3	Error message. Replace CPUx
1009	Memory, 02	Assert	Correctable ECC	01 00	0C	6F	B1 - XX - MMR ID	Memory correctable ECC error: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : D2A1 6 : JD2B0 7 : JD2B1	Information Indicates one DIMM at CPE. (The system will log one SEL.)

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1010A0	Memory, 02	Assert	Uncorrectable ECC	01 00	0C	6F	B2 - 0X - MMR ID	Memory uncorrectable ECC error: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Error message. Four DIMMs should be replaced (Single Mode). The system will log four messages in the SEL. Replace MMRx-DIMMx
1010A1	Memory, 02	Assert	Uncorrectable ECC	01 00	0C	6F	B2 - 1X - MMR ID	Memory uncorrectable ECC error: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Error message. Four DIMMs should be replaced (Double Mode). The system will log four messages in the SEL. DIMMs to be replaced exist in multiple MMRs. Replace MMRx-DIMMx
1010A2	Memory, 02	Assert	Uncorrectable ECC	01 00	0C	6F	B2 - 2X - MMR ID	Memory uncorrectable ECC error: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Error message. Eight DIMMs should be replaced (Mirror Mode). The system will log eight messages in the SEL. DIMMs to be replaced exist in multiple MMRs. Replace MMRx-DIMMx

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1010A3	Memory, 02	Assert	Uncorrectable ECC	01 00	0C	6F	B2 - 3X - MMR ID	Memory uncorrectable ECC error: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Error message. Outputs by Uncorrectable Error at initialization. The system will log the same number of messages in the SEL with the number of replacement. DIMMs to be replaced exist in multiple MMRs. Replace MMRx-DIMMx
1011	Memory, 02	Assert	Memory Scrub Failed (Stack bit)	01 00	0C	6F	B3 - XX - MMR ID	Memory chip replace didn't start: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Informational message. No action necessary.; Outputs at the memory replacement when the memory was already replaced in the past and there is no redundant DRAM.
1012	Memory, 02	Assert	Memory Device Disabled	01 00	0C	6F	B4 - XX - XF where Event Data3 is X[MMR ID]	MMR disabled: bit[7:4] MMR ID (0-3)	Error message. Replace MMRx.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1013	Memory, 02	Assert	Memory Device Disabled	01 00	0C	6F	B4 - XX - MMR ID, unless XF	DIMM disabled: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Error message. DIMM degradation will be performed in the unit of four. (The system will log four messages in the SEL.). Replace MMRx-DIMMx.
1014	Memory, 02	Assert	Correctable ECC limit reached	01 00	0C	6F	B5 - XX - MMR ID	Memory correctable ECC error limit reached: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Warning message. DIMM degradation will be performed in the unit of four. (The system will log four messages in the SEL.). Replace MMRx-DIMMx.
1015A0	Memory, 02	Assert	Presence Detected	01 00	0C	6F	B6 - X0 - XF, where Event Data3 is X[MMR ID]	MMR added: bit[7:4] MMR ID (0-3)	Informational message. No action necessary.
1015A1	Memory, 02	Assert	Presence Detected	01 00	0C	6F	B6 - X1 - XF, where Event Data3 is X[MMR ID]	MMR added: bit[7:4] MMR ID (0-3)	Informational message. No action necessary.
1015A2	Memory, 02	Assert	Presence Detected	01 00	0C	6F	B6 - X2 - XF, where Event Data3 is X[MMR ID]	MMR added: bit[7:4] MMR ID (0-3)	Informational message. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1016	Memory, 02	Assert	Configuration Error	01 00	0C	6F	B7 - XX - MMR ID	Memory configuration failure: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Error message. Indicates in the unit of four. Replace MMRx-DIMMx.
1017	Memory, 02	Assert	Spare	01 00	0C	6F	B8 - XX - MMR ID	Memory chip replace started: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Informational message. Replace MMRx-DIMMx.
1018A0	Memory, 02	Deassert	Presence Detected	01 00	0C	EF	B6 - X0 - Xf where Event Data3 is X[MMR ID]	MMR removed successfully: bit[7:4] MMR ID (0-3)	Informational message. No action necessary.
1018A1	Memory, 02	Deassert	Presence Detected	01 00	0C	EF	B6 - X1 - XF, where Event Data3 is X[MMR ID]	MMR removal started: bit[7:4] MMR ID (0-3)	Informational message. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1019A0	Memory, 02	Deassert	Spare	01 00	0C	EF	B8 - 3X - MMR ID	Memory chip replacement finished: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Informational message. No action necessary.
1019A1	Memory, 02	Deassert	Spare	01 00	0C	EF	B8 - 3X - MMR ID	Memory chip replacement finished: bit[7:4] MMR ID (0-3) bit[3:0] DIMM ID 0 : JD0A0 1 : JD0A1 2 : JD0B0 3 : JD0B1 4 : JD2A0 5 : JD2A1 6 : JD2B0 7 : JD2B1	Informational message. No action necessary.
1020	System Firmware Progress, 12	Assert	System Firmware Error (POST Error)	01 00	0F	6F	A0 - POST error code - POST error code	POST Critical Error. POST Error Code	Error message. Check POST code. The maintenance action depends on the POST code.
1020A0	System Firmware Progress, 12	Assert	System Firmware Error (POST Error)	01 00	0F	6F	C0 - 02 - 00	No usable system memory	Error message. Check if MMRs installed correctly. Check DIMM configuration on each MMR. Check earlier logged messages in the SEL with memory sensor type.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1021	BIOS Critical Interrupt, 10	Assert	Front Panel NMI/Diagnostic Interrupt	01 00	13	6F	A0 - XX - XX	Front Panel NMI / Diagnostic Interrupt	Informational message. No action necessary.
1021A0	BIOS Critical Interrupt, 10	Assert	Bus Uncorrectable Error	01 00	13	6F	A8 - XX - XX	MCA raised	Informational message. No action necessary.
1022	Board, 00	Assert	to Non-Critical from OK	01 00	15	07	A1 - MMR ID - 0X	FSB correctable error limit reached. CPU Socket ID: 00 : CPU0 01 : CPU1 10 : CPU2 11 : CPU3	Warning message. Replace CPUx (pointed out by Event Data 2). Replace the other CPU on the same FSB. Replace MB.
1024	Board, 00	Assert	to Non-Critical from OK	01 00	15	07	A1 - 00 - 51	PCI Express* correctable error limit reached (ESI I/f, NDC detected)	Warning message. Error has been detected at ESI I/F in NDC. Replace MB.
1025	Board, 00	Assert	to Non-Critical from OK	01 00	15	07	A1 - 01 - 51	PCI Express correctable error limit reached (ESI I/f, ESB2 detected)	Warning message. Error has been detected at ESI I/F in ESB2. Replace MB.
1026	Board, 00	Assert	to Non-Critical from OK	01 00	15	07	A1 - 02 - 51	PCI Express correctable error limit reached (NDC-ESB2 PCI-E I/f, NDC detected)	Warning message. Error has been detected at NDC-ESB2 PCI-E I/F in NDC. Replace MB.
1027	Board, 00	Assert	to Non-Critical from OK	01 00	15	07	A1 - 03 - 51	PCI Express correctable error limit reached (NDC-ESB2 PCI-E I/f, ESB2 detected)	Warning message. Error has been detected at NDC-ESB2 PCI-E I/F in ESB2. Replace MB.
1027A0	Board, 00	Assert	to Non-Critical from OK	01 00	15	07	A1 - 04 - 51	PCI Express correctable error limit reached (ESB2-PXH I/f, ESB2 detected)	Warning message. Replace MB.
1027A1	Board, 00	Assert	to Non-Critical from OK	01 00	15	07	A1 - 05 - 51	PCI Express correctable error limit reached (ESB2-PXH I/f, PXH detected)	Warning message. Replace MB.
1028	Board, 00	Assert	to Non-Critical from OK	01 00	15	07	A1 - XX - 1X	Node Link correctable error limit reached	Warning message. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1029	Board, 00	Assert	to Non-Critical from OK	01 00	15	07	A1 - XX - 2X A1 - MMR ID - 2X	NDC-MC Interface correctable error limit reached. MMR ID: 00 : MMR0 01 : MMR1 02 : MMR0 03 : MMR1 10 : MMR2 11 : MMR3 12 : MMR2 13 : MMR3	Warning message. Replace MMRx. Replace MB.
1030	Board, 00	Assert	to Non-Critical from OK	01 00	15	07	A1 - XX - 3X	HSCP correctable error limit reached	Warning message. Replace MB.
1031	Board, 00	Assert	Critical	01 00	15	07	A2 - CPU Socket ID - 0X	FSB fatal error. CPU Socket ID: x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Error message. Replace CPUx (pointed out by Event Data 2). Replace the other CPU on the same FSB. Replace MB.
1032	Board, 00	Assert	Critical	01 00	15	07	A2 - 00 - 4X	PCI recoverable error (ESB2 detected)	Error message. Replace MB.
1033	Board, 00	Assert	Critical	01 00	15	07	A2 - 00 - 51	PCI Express recoverable error (ESI I/f, NDC detected)	Error message. Error has been detected at ESI I/F in NDC.; Replace MB.
1034	Board, 00	Assert	Critical	01 00	15	07	A2 - 01 - 51	PCI Express recoverable error (ESI I/f, ESB2 detected)	Error message. Error has been detected at ESI I/F in ESB2. Replace MB.
1035	Board, 00	Assert	Critical	01 00	15	07	A2 - 02 - 51	PCI Express recoverable error (NDC-ESB2 PCI-E I/f, NDC detected)	Error message. Error has been detected at NDC-ESB2PCI-E I/F in NDC. Replace MB.
1036	Board, 00	Assert	Critical	01 00	15	07	A2 - 03 - 51	PCI Express recoverable error (NDC-ESB2 PCI-E I/f, NDC detected)	Error message. Error has been detected at NDC-ESB2 PCI-E I/F in ESB2. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1036A0	Board, 00	Assert	Critical	01 00	15	07	A2 - 04 - 51	PCI Express recoverable error (ESB2-PXH I/f, ESB2 detected)	Error message. Replace MB.
1036A1	Board, 00	Assert	Critical	01 00	15	07	A2 - 05 - 51	PCI Express recoverable error (ESB2-PXH I/f, PXH detected)	Error message. #1: replace MB
1037	Board, 00	Assert	Critical	01 00	15	07	A2 - XX - 1X	Node Link recoverable error	Error message. Replace MB.
1037A1	Board, 00	Assert	Critical	01 00	15	07	A2 - 00 - 86	Unexpected Clock Frequency	Warning message. Reboot system (This works in case that clock frequency has been altered by OEM -defined IPMI command). Replace MB.
1038	Board, 00	Assert	Non-recoverable	01 00	15	07	A3 - CPU Socket ID - 0X	FSB fatal error. CPU Socket ID: x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Error message. Replace CPUx (pointed out by Event Data 2) Replace the other CPU on the same FSB. Replace MB.
1039	Board, 00	Assert	Non-recoverable	01 00	15	07	A3 - 00 - 4X	PCI fatal error (ESB2 detected)	Error message. Replace MB.
1040	Board, 00	Assert	Non-recoverable	01 00	15	07	A3 - 00 - 51	PCI Express fatal error (ESI I/f, NDC detected)	Error message. Error has been detected at ESI I/F in NDC. Replace MB.
1041	Board, 00	Assert	Non-recoverable	01 00	15	07	A3 - 01 - 51	PCI Express fatal error (ESI I/f, ESB2 detected)	Error message. Error has been detected at ESI I/F in ESB2. Replace MB.
1042	Board, 00	Assert	Non-recoverable	01 00	15	07	A3 - 02 - 51	PCI Express fatal error (NDC-ESB2 PCI-E I/f, NDC detected)	Error message Error has been detected at NDC-ESB2 PCI-E I/F in NDC. Replace MB.
1043	Board, 00	Assert	Non-recoverable	01 00	15	07	A3 - 03 - 51	PCI Express fatal error (NDC-ESB2 PCI-E I/f, ESB2 detected)	Error message Error has been detected at NDC-ESB2 PCI-E I/F in ESB2. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1043A0	Board, 00	Assert	Non-recoverable	01 00	15	07	A3 - 04 - 51	PCI Express fatal error (ESB2-PXH I/f, ESB2 detected)	Error message Replace MB.
1043A1	Board, 00	Assert	Non-recoverable	01 00	15	07	A3 - 05 - 51	PCI Express fatal error (ESB2-PXH I/f, PXH detected)	Error message Replace MB.
1044	Board, 00	Assert	Non-recoverable	01 00	15	07	A3 - XX - 1X	Node Link fatal error	Error message Replace MB.
1045	Board, 00	Assert	Non-recoverable	01 00	15	07	A3 - XX - 21	NDC-MC Interface fatal error. MMR ID: 00 : MMR0 01 : MMR1 02 : MMR0 03 : MMR1 10 : MMR2 11 : MMR3 12 : MMR2 13 : MMR3	Error message Replace MMRx. Replace MB.
1046	Board, 00	Assert	Informational	01 00	15	07	A8 - CPU Socket ID - 0X	FSB correctable error. CPU Socket ID: x0 : CPU0 x1 : CPU1 x2 : CPU2 x3 : CPU3	Informational message. No action necessary.
1048	Board, 00	Assert	Informational	01 00	15	07	A8 - 00 - 51	PCI Express correctable error (ESI I/f, NDC detected)	Informational message. No action necessary. Error has been detected at ESI I/F in NDC.
1049	Board, 00	Assert	Informational	01 00	15	07	A8 - 01 - 51	PCI Express correctable error (ESI I/f, ESB2 detected)	Informational message. No action necessary. Error has been detected at ESI I/F in ESB2.
1050	Board, 00	Assert	Informational	01 00	15	07	A8 - 02 - 51	PCI Express correctable error (NDC-ESB2 PCI-E I/f, NDC detected)	Informational message. No action necessary. Error has been detected at NDC-ESB2 PCI-E I/F in NDC.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1051	Board, 00	Assert	Informational	01 00	15	07	A8 - 03 - 51	PCI Express correctable error (NDC-ESB2 PCI-E I/f, ESB2 detected)	Informational message. No action necessary. Error has been detected at NDC-ESB2 PCI-E I/F in ESB2.
1051A0	Board, 00	Assert	Informational	01 00	15	07	A8 - 04 - 51	PCI Express correctable error (ESB2-PXH I/f, ESB2 detected)	Informational message. No action necessary.
1051A1	Board, 00	Assert	Informational	01 00	15	07	A8 - 05 - 51	PCI Express correctable error (ESB2-PXH I/f, PXH detected)	Informational message. No action necessary.
1052	Board, 00	Assert	Informational	01 00	15	07	A8 - XX - 1X	Node Link correctable error	Informational message. No action necessary.
1053	Board, 00	Assert	Informational	01 00	15	07	A8 - MMR ID - 2X	NDC-MC Interface correctable error. MMR ID: 00 : MMR0 01 : MMR1 02 : MMR0 03 : MMR1 10 : MMR2 11 : MMR3 12 : MMR2 13 : MMR3	Informational message. No action necessary.
1054	Board, 00	Assert	Informational	01 00	15	07	A8 - XX - 3X	HSCP correctable error	Informational message. No action necessary.
1055	Chipset, 01	Assert	to Non-Critical from OK	01 00	19	07	A1 - X0 - X6	Chipset correctable error limit reached	Warning message. Other than Event Data3 = 46. Replace MB.
1056	Chipset, 01	Assert	to Non-Critical from OK	01 00	19	07	A1 - X0 - 65	LCM counter sync error	Warning message. Replace MB.
1057	Chipset, 01	Assert	to Non-Critical from OK	01 00	19	07	A1 - X0 - 7X	L3 Cache Tag (SRAM) correctable error limit reached	Warning message. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1058	Chipset, 01	Assert	to Non-Critical from OK	01 00	19	07	A1 - MMR ID - 46	Memory controller correctable error limit reached. MMR ID: 00 : MMR0 01 : MMR1 02 : MMR0 03 : MMR1 10 : MMR2 11 : MMR3 12 : MMR2 13 : MMR3	Warning message. Replace MMRx.
1059	Chipset, 01	Assert	Critical	01 00	19	07	A2 - X0 - X6	Chipset recoverable error	Error message. Replace MB.
1059A0	Chipset, 01	Assert	Critical	01 00	19	07	A2 - X0 - 7X	L3 Cache Tag (SRAM) uncorrectable error	Error message. Replace MB.
1059A1	Chipset, 01	Assert	Critical	01 00	19	07	A2 - MMR ID - 46	Memory controller recoverable error. MMR ID: 00 : MMR0 01 : MMR1 02 : MMR0 03 : MMR1 10 : MMR2 11 : MMR3 12 : MMR2 13 : MMR3	Error message. Replace MMRx.
1060	Chipset, 01	Assert	Critical	01 00	19	07	A2 - X0 - X3	Bad chipset data received	Error message. Review SEL.
1060A0	Chipset, 01	Assert	Critical	01 00	19	07	A2 - XX - XF	Recoverable error (Unknown)	Error message Unable to identify the cause. Replace MB.
1061	Chipset, 01	Assert	Non-Recoverable	01 00	19	07	A3 - X0 - X6	Chipset fatal error	Error message Other than Event Data3 = 46. Replace MB.
1062	Chipset, 01	Assert	Non-Recoverable	01 00	19	07	A3 - XX - X6	Chipset timeout	Error message. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1063	Chipset, 01	Assert	Non-recoverable	01 00	19	07	A3 - X0 - 7X	L3 Cache Tag (SRAM) fatal error on POST	Error message Other than Event Data3 = 70. Replace MB.
1064	Chipset, 01	Assert	Non-recoverable	01 00	19	07	A3 - MMR ID - 46	Memory controller fatal error. MMR ID: 00 : MMR0 01 : MMR1 02 : MMR0 03 : MMR1 10 : MMR2 11 : MMR3 12 : MMR2 13 : MMR3	Error message. Replace MMRx.
1065	Chipset, 01	Assert	Non-recoverable	01 00	19	07	A3 - 00 - 41	Memory controller illegal data detected	Error message Two MMRs (or four of MC chipset) are candidates of failure unit, but no detection ability to indicate which MMR is failed. Replace MMR0. Replace MMR1. Replace MB.
1065A0	Chipset, 01	Assert	Non-recoverable	01 00	19	07	A3 - 10 - 41	Memory controller illegal data detected	Error message Two MMRs (or four of MC chipset) are candidates of failure unit, but no detection ability to indicate which MMR is failed. Replace MMR2. Replace MMR3. Replace MB.
1066A0	Chipset, 01	Assert	Non-recoverable	01 00	19	07	A3 - XX - XF	Fatal error (Unknown)	Error message Unable to identify the cause. Replace MB.
1067	Chipset, 01	Assert	Informational	01 00	19	07	A8 - X0 - X6	Chipset correctable error	Informational message. No action necessary. Other than Event Data3 = 46
1068	Chipset, 01	Assert	Informational	01 00	19	07	A8 - X0 - 65	LCM counter sync error	Informational message. No action necessary.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1069	Chipset, 01	Assert	Informational	01 00	19	07	A8 - X0 - 7F	L3 Cache Tag (SRAM) correctable error	Informational message. No action necessary.
1070	Chipset, 01	Assert	Informational	01 00	19	07	A8 - MMR ID - 46	Memory controller correctable error. MMR ID: 00 : MMR0 01 : MMR1 02 : MMR0 03 : MMR1 10 : MMR2 11 : MMR3 12 : MMR2 13 : MMR3	Informational message. No action necessary.
1071	OS Boot	Assert	Boot completed - boot device not specified	01 00	1F	6F	06 - XX - XX	OS boot complete	
1072	Slot	Assert	to Non-Critical from OK	01 00	21	07	A1 - 0X - 0X	SLOTx correctable error limit reached. Slot ID(x): 01 : SLOT1 02 : SLOT2 03 : SLOT3 04 : SLOT4 05 : SLOT5 06 : SLOT6	Replace SLOTx. Replace MB.
1073	Slot	Assert	to Non-Critical from OK	01 00	21	07	A1 - 0X - 81	ESB2 correctable error limit reached	Replace MB.
1077	Slot, 05	Assert	to Non-Critical from OK	01 00	21	07	A1 - 0X - 85	PXH correctable error limit reached	Warning message. Replace MB.
1078	Slot, 05	Assert	Critical	01 00	21	07	A2 - 0X - Slot ID	SLOTx recoverable error. Slot ID(x): 01 : SLOT1 02 : SLOT2 03 : SLOT3 04 : SLOT4 05 : SLOT5 06 : SLOT6	Error message. Replace SLOTx. Replace MB.

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1079	Slot, 05	Assert	Critical	01 00	21	07	A2 - 0X - 81	ESB2 recoverable error	Error message. Replace MB
1080	Slot, 05	Assert	Critical	01 00	21	07	A2 - 0X - 81	SAS controller recoverable error	Error message. Replace MB.
1081	Slot, 05	Assert	Critical	01 00	21	07	A2 - 0X - 83	Management LAN Controller recoverable error	Error message. Replace MB.
1082	Slot, 05	Assert	Critical	01 00	21	07	A2 - 0X - 84	VGA Controller recoverable error	Error message. Replace MB.
1083	Slot, 05	Assert	Critical	01 00	21	07	A2 - 0X - 85	PXH recoverable error	Error message. Replace MB.
1084	Slot, 05	Assert	Non-recoverable	01 00	21	07	A3 - 0X - Slot ID	SLOTx fatal error. Slot ID(x): 01 : SLOT1 02 : SLOT2 03 : SLOT3 04 : SLOT4 05 : SLOT5 06 : SLOT6	Error message. Replace SLOTx. Replace MB.
1085	Slot, 05	Assert	Non-recoverable	01 00	21	07	A3 - 0X - 81	ESB2 fatal error	Error message. Replace MB.
1086	Slot, 05	Assert	Non-recoverable	01 00	21	07	A3 - 0X - 82	SAS controller fatal error	Error message. Replace MB.
1087	Slot, 05	Assert	Non-recoverable	01 00	21	07	A3 - 0X - 83	Management LAN Controller fatal error	Error message. Replace MB
1088	Slot, 05	Assert	Non-recoverable	01 00	21	07	A3 - 0X - 84	VGA Controller fatal error	Error message. Replace MB.
1089	Slot, 05	Assert	Non-recoverable	01 00	21	07	A3 - 0X - 85	PXH fatal error	Replace MB.
1090	Slot, 05	Assert	Informational	01 00	21	07	A8 - 0X - 0X	SLOTx correctable error. Slot ID(x): 01 : SLOT1 02 : SLOT2 03 : SLOT3 04 : SLOT4 05 : SLOT5 06 : SLOT6	
1091	Slot, 05	Assert	Informational	01 00	21	07	A8 - 0X - 81	ESB2 correctable error	

#	Sensor Name and Number	Event		Generator ID	Sensor Type	Event Trigger	Event Data1 - Event Data2 - Event Data3	Description	Message Type / Recovery Information
1095	Slot, 05	Assert	Informational	01 00	21	07	A8 - 0X - 85	PXH correctable error	Informational message. No action necessary.
1096	Version Change, 11	Assert	Firmware or software change detected	01 00	2B	6F	01 - XX - XX	Firmware Recovery Start	Informational message. No action necessary.
1097	Version Change, 11	Assert	Invalid or unsupported firmware version	01 00	2B	6F	E5 - 00 - XX	Firmware Version Unmatch (No valid backup image)	Error message. Replace MB.
1097A0	Version Change, 11	Assert	Invalid or unsupported firmware version	01 00	2B	6F	E5 - 01 - FWH ID	Firmware Version Unmatch (FWH #xx write failure). FWH ID (0-3)	Error message. Replace MB.
1098	Version Change, 11	Assert	Software or F/W Change was successful	01 00	2B	6F	07 - XX - XX	Firmware Update Succeeded	Informational message. No action necessary.

Appendix D: Power Cord Recommendations

This section assists customers with the procurement of power cords for the Intel® Server System SR9000MK4U. Information provided by geographical region includes:

- A general description of the component and its function
- Current part numbers and revision levels
- Vendor contact information

Power Cord Specifications

The Intel® Server System SR9000MK4U does not include power cord sets for the two 1390-watt power supplies because of the unique requirements and the differing AC services in the regions where the system may be shipped.

The maximum input/output power of the Intel® Server System SR9000MK4U are:

- System power input: 80% minimum efficiency at >90 VAC
- System power output: 2780 watts at 200-240 VAC

The 1390-watt power supply has an IEC 320 C-14 AC input connector that mates with C13 cord plug.

1390 Watt Power Supply Specifications

The maximum input/output power expectations of the 1390 watt power supply are:

Nominal Input Voltage	200-240 VAC	100-127 VAC
Minimal Input Voltage	180 VAC	90 VAC
Maximum Input Voltage	264 VAC	140 VAC
Maximum Input Current (At Nominal VAC)	9A (50-60Hz)	12A (50-60Hz)
AC Inlet connector	IEC 320 C-14	IEC 320 C-14

Cord and Service

The following criteria should be used for the wire cord and AC service selection for installation of the server system. The selections should be verified by a certified safety and regulatory professional for the safety requirements of each application.

- In North America, the cord must be UL Listed/CSA Certified, 14/3, type SJT/SO/STO, with NEMA 5-15P or equivalent attachment plug for 100-127 VAC, or UL Listed/CSA Certified, 16/3, type SJT/SO, with NEMA 6-15 or equivalent attachment plug for 200-240 VAC and IEC 320 C19 plug outlet.
- Outside of North America, the cord must be flexible VDE certified or HAR rated 250V, 3 x 1mm minimum conductor size with IEC 320 C13 outlet, and rated for no less than the product ratings. The AC wall attachment plug shall be a three conductor grounding type, rated at 125% of the total input current rating and must be for the configuration of the specific region or country. The AC wall attachment plug must bear at least an accepted safety agency certification mark for the specific region or country.
- The cord must be no longer than 4.5 meters (14.76 feet).

Warning: *Do not attempt to modify or use an AC power cord that is not the exact type required.*

How to Purchase 1390 Watt Power Supply Cord Sets

See the vendor information below to source a power cord set. These selections are assembled cord sets, not raw parts. Check the power source outlets to determine if the selection is suitable. All selections should be further verified by a certified safety and regulatory professional for the safety requirements of each application.

North American Power Supply Cordsets

Table 43. Interpower* Corporation North American Cordset 125 VAC

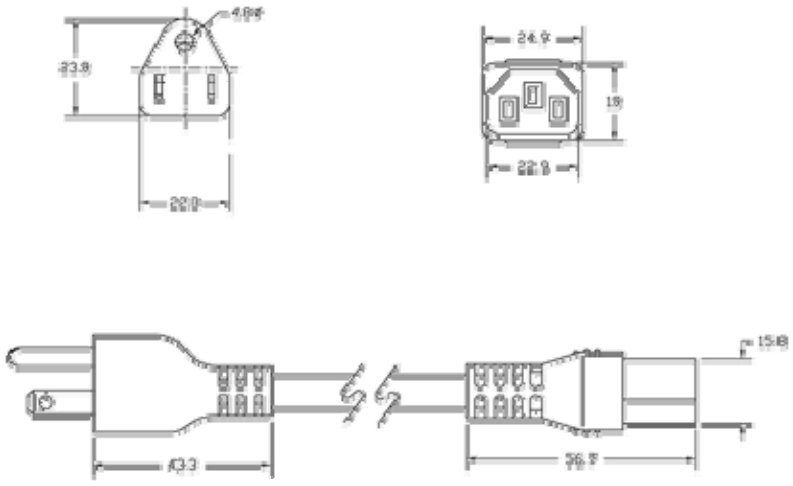
Part Number	86221590
Contact Telephone Number	1-800-662-2290
Vendor Website	http://www.interpower.com/
Equipment End	IEC 60320 C13
Supply End	NEMA 5-15P
Current Rating	15A
Voltage Rating	125VAC
Length	2.5 meters
	
	

Table 44. Quail Electronics* North American Cordset 125 VAC

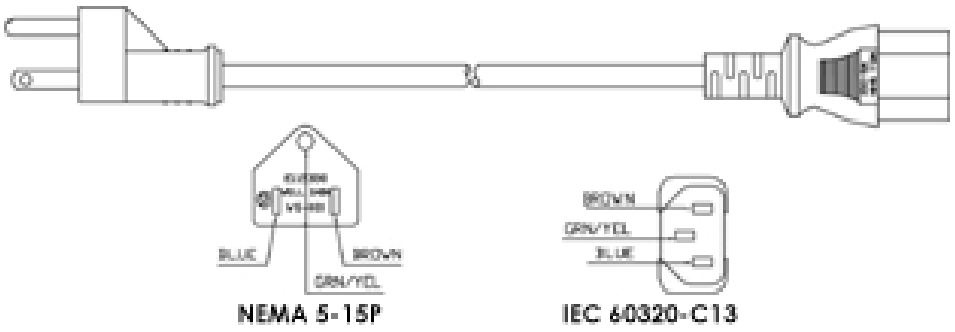
Part Number	5041.072, 5041.096, 5041.120
Contact Telephone Number	1-925-373-6700
Vendor Website	http://www.quail.com/
Equipment End	IEC 60320 C13
Supply End	NEMA 5-15P
Current Rating	15A
Voltage Rating	125VAC
Length	6, 8, and 10 feet
	
	

Table 45. Interpower Corporation* North American Cordset 250 VAC

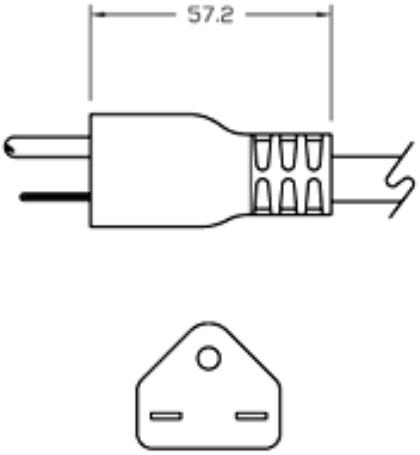
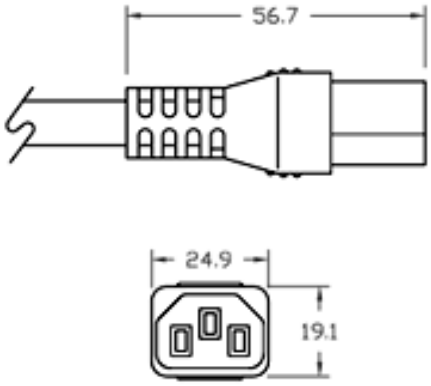
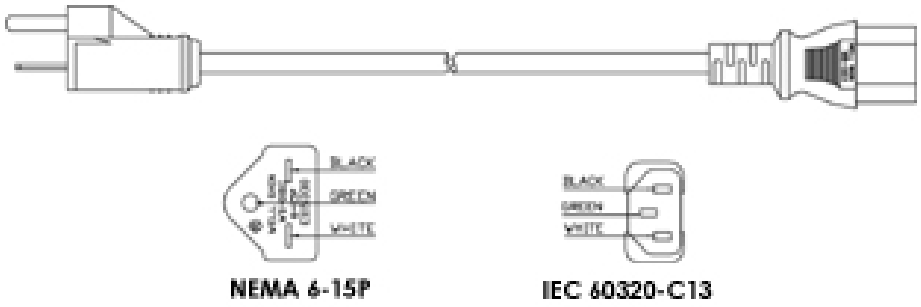
Part Number	86610100
Contact Telephone Number	1-800-662-2290
Vendor Website	http://www.interpower.com/
Equipment End	IEC 60320 C13
Supply End	NEMA6-15P
Current Rating	10A
Voltage Rating	250VAC
Length	2.4 meters
	
	

Table 46. Quail Electronics* North American Cordset 250 VAC

Part Number	1691.072, 1591.096, 1691.120
Contact Telephone Number	1-925-373-6700
Vendor Website	http://www.quail.com/
Equipment End	IEC 60320 C13
Supply End	NEMA6-15P
Current Rating	15A
Voltage Rating	250VAC
Length	6, 8, and 10 feet



European Power Supply Cordsets

Table 47. Interpower Corporation* Continental Europe Cordset

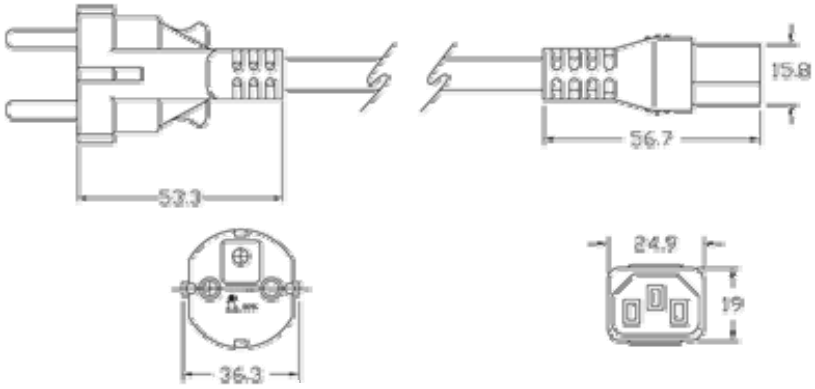
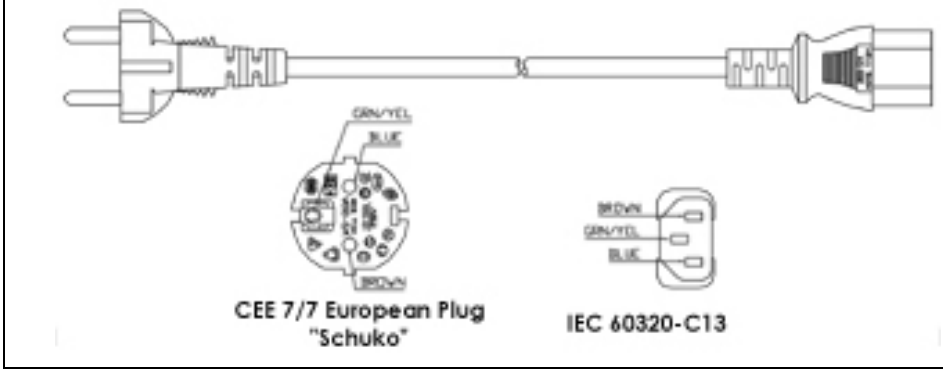
Part Number	86231530
Contact Telephone Number	44 (0) 1908 327700
Vendor Website	http://www.interpower.com/
Equipment End	IEC 60320 C13
Supply End	CEE 7/7
Current Rating	10A
Voltage Rating	250VAC
Length	3.5 meters
	
	

Table 48. Quail Electronics* Continental Europe Cordset

Part Number	8500.098
Contact Telephone Number	011-1-800-669-8090
Vendor Website	http://www.quail.com/
Equipment End	IEC 60320 C13
Supply End	CEE 7/7 (Schuko)
Current Rating	10A
Voltage Rating	250VAC
Length	2.5 meters
	

Chinese Power Supply Cordsets

Table 49. Interpower Corporation* Chinese Cordset

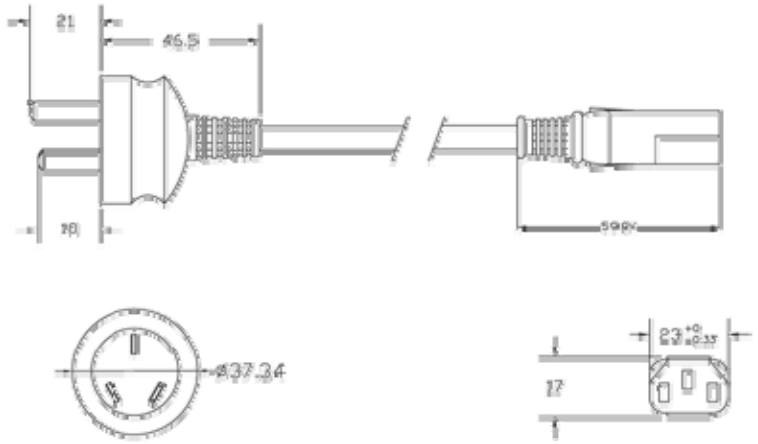
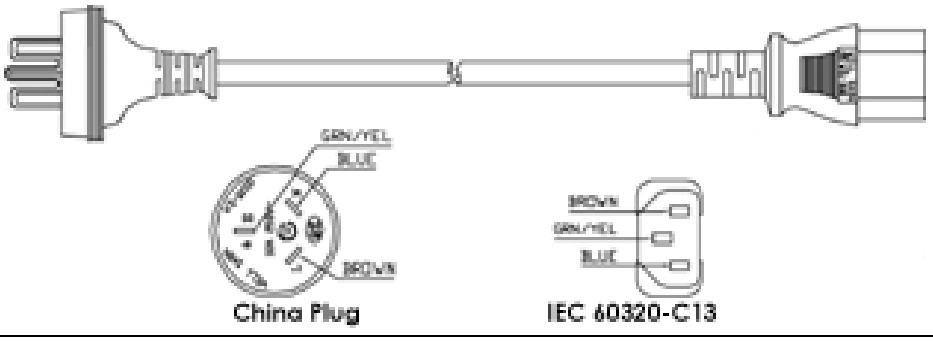
Part Number	86517040
Contact Telephone Number	44 (0) 1908 327700
Vendor Website	http://www.interpower.com/
Equipment End	IEC 60320 C13
Supply End	GB 2099-1-1996
Current Rating	10A
Voltage Rating	250VAC
Length	2.5 meters
	
	

Table 50. Quail Electronics* Chinese Cordset

Part Number	8590.098
Contact Telephone Number	011-1-800-669-8090
Vendor Website	http://www.quail.com/
Equipment End	IEC 60320 C13
Supply End	GB 2099-1-1996
Current Rating	10A
Voltage Rating	250VAC
Length	2.5 meters
	

United Kingdom Power Supply Cordsets

Table 51. Interpower Corporation* United Kingdom Cordset

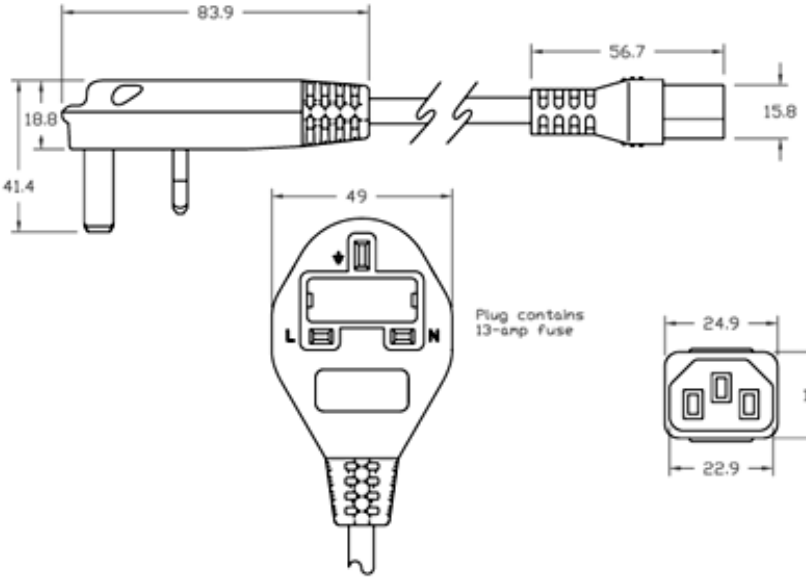
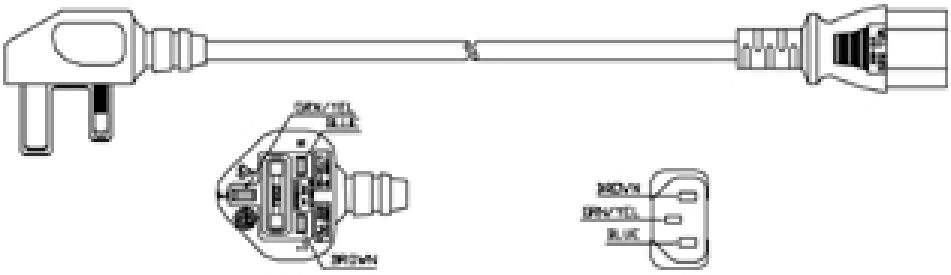
Part Number	86240080
Contact Telephone Number	44 (0) 1908 327700
Vendor Website	http://www.interpower.com/
Equipment End	IEC 60320 C13
Supply End	U.K. Plug BS 1363
Current Rating	10A
Voltage Rating	250 VAC
Length	3.5 meters
	
	

Table 52. Quail Electronics* United Kingdom Cordset

Part Number	9650.098
Contact Telephone Number	011-1-800-669-8090
Vendor Website	http://www.quail.com/
Equipment End	IEC 60320 C13
Supply End	U.K. Plug BS 1363
Current Rating	10A
Voltage Rating	250VAC
Length	2.5 meters



Reference Documents

- *Intel® Server System SR9000MK4U Product Guide*
- *Intel® Server System SR9000MK4U Tested Hardware and OS List*
- *Intel® Server System SR9000MK4U Memory Tested List*

Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ASIC	Application Specific Integrated Circuit
ASMI	Advanced Server Management Interface
BIOS	Basic Input / Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
byte	8-bit quantity.
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMP	Emergency Management Port
EPS	External Product Specification
ESB2	Enterprise South Bridge 2
FBD	Fully Buffered DIMM
F MB	Flexible Mother Board
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GB	1024 MB
GPIO	General Purpose I/O
GTL	Gunning Transceiver Logic
HSC	Hot-Swap Controller
Hz	Hertz (1 cycle / second)
I2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture
IBF	Input Buffer
ICH	I/O Controller Hub
IC MB	Intelligent Chassis Management Bus
IERR	Internal Error
IFB	I/O and Firmware Bridge
INTR	Interrupt
IP	Internet Protocol

Term	Definition
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
ITP	In-Target Probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB	1024KB
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
MMR	Memory Box
ms	milliseconds
MTTR	Memory Type Range Register
Mux	Multiplexor
MVR	Modular Voltage Regulator
NDC	Node Controller
NIC	Network Interface Controller
NMI	Nonmaskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm	Unit of electrical resistance
PEF	Platform Event Filtering
PEP	Platform Event Paging
PIA	Platform Information Area (This feature configures the firmware for the platform hardware)
PLD	Programmable Logic Device
PMI	Platform Management Interrupt
POST	Power-On Self Test
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board)
SDINT	System Diagnostic Interrupt
SDR	Sensor Data Record
SECC	Single Edge Connector Cartridge
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory

Term	Definition
SEL	System Event Log
SIO	Server Input / Output
SMI	Server Management Interrupt (SMI is the highest priority nonmaskable interrupt)
SMM	Server Management Mode
SMS	Server Management Software
SNMP	Simple Network Management Protocol
TBD	To Be Determined
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver / Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
UTC	Universal time coordinare
VID	Voltage Identification
VRD	Voltage Regulator Down
Word	16-bit quantity
ZIF	Zero Insertion Force