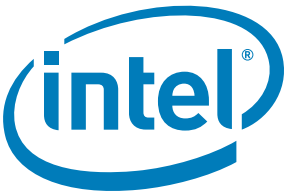

# Intel® Celeron® M Processor 500Δ Series

## Datasheet

***For Mobile Intel® 945 Express Chipset Family***

***September 2007***

Document Number: 316205-003

# Contents

## Figures



## Tables

# Revision History

| Revision Number | Description | Date |
|---|---|---|
| -001 | Initial Release | January 2007 |
| -002 | • Added Intel® Celeron M 520 and Celeron M 530 Thermal and Electrical Information<br>• Updated Table 6 Electrical Specifications<br>• Updated Table 16 Thermal Specifications<br>• Added Package information for A-1 stepping | July 2007 |
| -003 | • Added Celeron M 523 Ultra Low Voltage processor<br>• Updated Electrical Specifications with ULV Celeron data<br>• Updated Thermal Specifications with ULV Celeron data | September 2007 |

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# 1 Introduction

The Intel® Celeron® M processor 500[Δ] series for Mobile Intel® 945 Express Chipset family-based systems is the first Celeron M processor to feature 64-bit support. Built on 65-nanometer process technology, it is based on the new Intel® Core™ micro-architecture.

***Note:*** All references to the word “processor” in this document are references to the Celeron M processor 500 series with a 533-MHz front side bus (FSB) unless specified otherwise.

The following list provides some of the key features of this processor:

- Single Core
- On-die, primary 32-kB instruction cache and 32-kB write-back data cache
- On-die, 1-MB second level shared cache with Advanced Transfer Cache Architecture
- 533-MHz Source-Synchronous Front Side Bus (FSB)
- Supports Intel Architecture with Dynamic Execution
- Data Prefetch Logic
- Micro-FCPGA packaging technology
- MMX, Streaming SIMD Extensions (SSE), Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3), and Supplemental Streaming SIMD Extensions 3 (SSSE3)
- Digital Thermal Sensor (DTS)
- Execute Disable Bit support for enhanced security
- Intel® 64 architecture (formerly Intel® EM64T)[Φ]
- Architectural and performance enhancements of the Core micro-architecture.

***Note:*** [Φ] Intel® 64 architecture requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel 64. The processor will not operate (including 32-bit operation) without an Intel 64-enabled BIOS. Performance will vary depending on your hardware and software configurations. See http://developer.intel.com/technology/intel64/index.htm for more information including details on which processors support Intel 64 or consult with your system vendor for more information.

## 1.1 Terminology

| Term | Definition |
|---|---|
| # | A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level). XXXX means that the specification or value is yet to be determined. |
| Front Side Bus (FSB) | Refers to the interface between the processor and system core logic (also known as the chipset components). |
| AGTL+ | Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors. |
| Storage Conditions | Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor lands should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material. |
| Processor Core | Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core. |
| Intel® 64 architecture | 64-bit memory extensions to the IA-32 architecture. |
| $V_{CC}$ | The processor core power supply |
| $V_{SS}$ | The processor ground |

## 1.2 References

Material and concepts in the following documents may be beneficial when reading this document. Please note that “platform design guide” refers to the following document: *Intel® Centrino® Duo Mobile Technology Design Guide.* Note that the Celeron M processor is supported by Mobile Intel® 945 Express Family Chipsets, and Intel® 82801GBM (code named ICH7M).

| Document | Document Number[1] |
|---|---|
| *Intel® Celeron® M Processor Specification Update* | 300302 |
| *Mobile Intel® 945 Express Chipset Family Datasheet* | 309219 |
| *Mobile Intel® 945 Express Chipset Family Specification Update* | 309220 |
| *Intel® I/O Controller Hub 7 (ICH7) Family Datasheet* | 307013 |
| *Intel® I/O Controller Hub 7 (ICH7) Family Specification Update* | 307014 |
| *Intel® 64 and IA-32 Intel® Architectures Software Developer's Manual* | |
| *Volume 1: Basic Architecture* | 253665 |
| *Volume 2A: Instruction Set Reference, A-M* | 253666 |
| *Volume 2B: Instruction Set Reference, N-Z* | 253667 |
| *Volume 3A: System Programming Guide, Part 1* | 253668 |
| *Volume 3B: System Programming Guide, Part 2* | 253669 |
| *Intel® 64 and IA-32 Intel® Architectures Software Developer's Manual Documentation Changes* | 252046 |
| *AP-485 Intel® Processor Identification and the CPUID Instruction* | 241618 |

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# 2 Low Power Features

## 2.1 Clock Control and Low Power States

The Celeron M processor supports the C1/AutoHALT, C1/MWAIT, C2, and C3 core low power states, along with their corresponding package level states for power management. These package states include Normal, Stop Grant, Stop Grant Snoop, Sleep, and Deep Sleep. The processor's central power management logic enters a package low power state by initiating a P_LVLx (P_LVL2, P_LVL3) I/O read to the Intel 945 Express Chipset family. Figure 1 shows the package level low-power states and Figure 2 shows the core low-power states. Refer to Table 1 for a mapping of core low power states to package low power states.

The Celeron M processor implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor and do not directly result in I/O reads on the processor FSB. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured through the IA32_MISC_ENABLES Model Specific Register (MSR).

If the processor encounters a chipset break event while STPCLK# is asserted, it asserts the PBE# output signal. Assertion of PBE# when STPCLK# is asserted indicates to system logic that the processor should return to the Normal state.

**Table 1. Core Low Power States at the Package Level**

| Core States | Package States |
|---|---|
| C0 | Normal |
| C1(1) | Normal |
| C2 | Stop Grant |
| C3 | Deep Sleep |

**NOTE:** (1) AutoHALT or MWAIT/C1

**Figure 1. Package Low Power States**

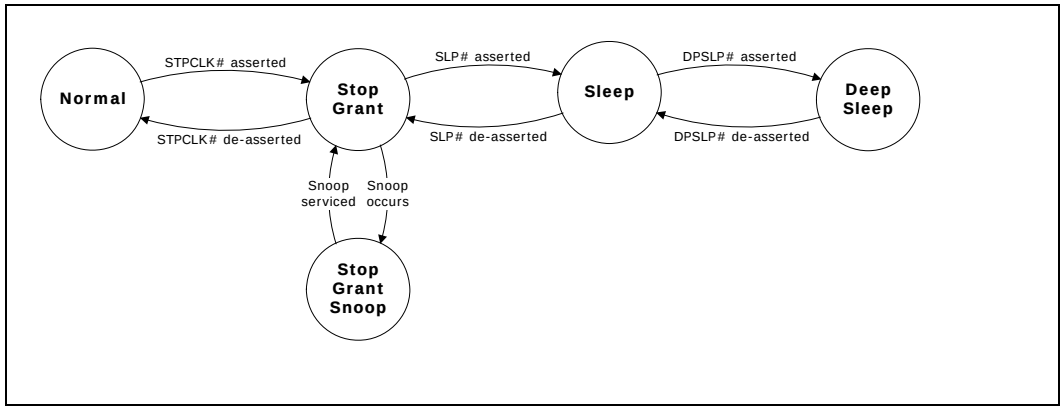
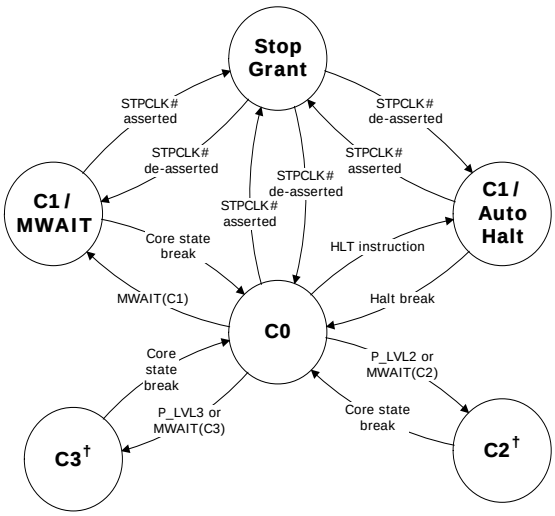


**Figure 2. Core Low Power States**




halt break = A20M# transition, INIT#, INTR, NMI, PREQ#, RESET#, SMI#, or APIC interrupt
core state break = (halt break OR Monitor event) AND STPCLK# high (not asserted)
† — STPCLK# assertion and de-assertion have no affect if a core is in C2, or C3.

## 2.1.1 Core Low-Power State Descriptions

### 2.1.1.1 C0 State

This is the normal operating state of the Celeron M processor.

### 2.1.1.2 C1 / AutoHALT Powerdown State

C1/AutoHALT is a low power state entered when the processor core executes the HALT instruction. The processor core will transition to the C0 state upon the occurrence of SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt message. RESET# will cause the processor to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT Powerdown state. See the *Intel 64 and IA-32 Intel® Architectures Software Developer's Manual, Volume 3A/3B: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Powerdown state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT powerdown state the Celeron M processor will process only the bus snoops. The processor core will enter a snoopable sub-state (not shown in Figure 2) to process the snoop and then return to the AutoHALT Powerdown state.

#### 2.1.1.3 C1/MWAIT Powerdown State

MWAIT is a low power state entered when the processor core executes the MWAIT instruction. Processor behavior in the MWAIT state is identical to the AutoHALT state except that there is an additional event that can cause the processor core to return to the C0 state: the Monitor event. See the *Intel 64 and IA-32 Intel® Architectures Software Developer's Manual, Volume 2A/2B: Instruction Set Reference* for more information.

#### 2.1.1.4 Core C2 State

The core of the Celeron M processor can enter the C2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C2) instruction, but the processor will not issue a Stop Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted.

While in C2 state, the Celeron M processor will process only the bus snoops. The processor core will enter a snoopable sub-state (not shown in Figure 2) to process the snoop and then return to the C2 state.

#### 2.1.1.5 Core C3 State

Core C3 state is a very low power state the processor core can enter while maintaining context. The core of the Celeron M processor can enter the C3 state by initiating a P_LVL3 I/O read to the P_BLK or an MWAIT(C3) instruction. Before entering the C3 state, the processor core flushes the contents of its L1 cache into the processor's L2 cache. Except for the caches, the processor core maintains all its architectural state in the C3 state. The Monitor remains armed if it is configured. All of the clocks in the processor core are stopped in the C3 state.

Because the core's caches are flushed, the processor keeps the core in the C3 state when the processor detects a snoop on the FSB. The processor core will transition to the C0 state upon the occurrence of a Monitor event, SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt message. RESET# will cause the processor core to immediately initialize itself.

### 2.1.2 Package Low Power State Descriptions

#### 2.1.2.1 Normal State

This is the normal operating state for the processor. The Celeron M processor enters the Normal state when the core is in the C0, C1/AutoHALT, or C1/MWAIT state.

#### 2.1.2.2 Stop-Grant State

When the STPCLK# pin is asserted the core of the Celeron M processor enters the Stop-Grant state within 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle. When the STPCLK# pin is deasserted the core returns to the previous core low-power state.

***Note:*** Since the AGTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to $V_{CCP}$) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. When RESET# is asserted by the system the STPCLK#, SLP#, and DPSLP# pins must be deasserted more than 480 µs prior to RESET# deassertion

(AC Specification T45). When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be deasserted ten or more bus clocks after the deassertion of SLP# (AC Specification T75).

While in the Stop-Grant State, the processor will service snoops and latch interrupts delivered on the FSB. The processor will latch SMI#, INIT#, LINT[1:0] interrupts and will serviced only upon return to the Normal state.

The PBE# signal may be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt or monitor event latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that the processor should return to the Normal state.

A transition to the Stop Grant Snoop state will occur when the processor detects a snoop on the FSB (see Section 2.1.2.3). A transition to the Sleep state (see Section 2.1.2.4) will occur with the assertion of the SLP# signal.

### 2.1.2.3 Stop Grant Snoop State

The processor will respond to snoop or interrupt transactions on the FSB while in Stop-Grant state by entering the Stop-Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. The processor will return to the Stop-Grant state once the snoop has been serviced or the interrupt has been latched.

### 2.1.2.4 Sleep State

The Sleep state is a low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and stops all internal clocks. The Sleep state is entered through assertion of the SLP# signal while in the Stop-Grant state. The SLP# pin should only be asserted when the processor is in the Stop-Grant state. SLP# assertions while the processor is not in the Stop-Grant state is out of specification and may result in unapproved operation.

***Note:*** In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP# or RESET#) are allowed on the FSB while the processor is in Sleep state. Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior. Any transition on an input signal before the processor has returned to the Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state, by asserting the DPSLP# pin. (See Section 2.1.2.5.) While the processor is in the Sleep state, the SLP# pin must be deasserted if another asynchronous FSB event needs to occur.

#### 2.1.2.5 Deep Sleep State

The Deep Sleep state is a very low power state the processor can enter while maintaining context. Deep Sleep state is entered by asserting the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform level power savings. BCLK stop/restart timings on appropriate chipset-based platforms with the CK410M clock chip are as follows:

- Deep Sleep entry: the system clock chip may stop/tristate BCLK within 2 BCLKs of DPSLP# assertion. It is permissible to leave BCLK running during Deep Sleep.
- Deep Sleep exit: the system clock chip must drive BCLK to differential DC levels within 2-3 ns of DPSLP# deassertion and start toggling BCLK within 10 BCLK periods.

To re-enter the Sleep state, the DPSLP# pin must be deasserted. BCLK can be re-started after DPSLP# deassertion as described above. A period of 15 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin must be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the FSB while the processor is in Deep Sleep state. When the processor is in Deep Sleep state, it will not respond to interrupts or snoop transactions. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

## 2.2 Low Power FSB Features

The Celeron M processor incorporates FSB low power enhancements:

- Dynamic On-die Termination disabling
- Low $V_{CCP}$ (I/O termination voltage)

The On-die Termination on the processor FSB buffers is disabled when the signals are driven low, resulting in power savings. The low I/O termination voltage is on a dedicated voltage plane independent of the core voltage, enabling low I/O switching power at all times.

## 2.3 Processor Power Status Indicator (PSI#) Signal

The processor incorporates the PSI# signal that is asserted when the processor is in a reduced power consumption state. PSI# can be used to improve light load efficiency of the voltage regulator, resulting in platform power savings and extended battery life. The algorithm that the Celeron M processor uses for determining when to assert PSI# is different from the algorithm used in previous Intel Celeron M processors.

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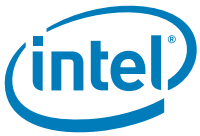


# 3 Electrical Specifications

## 3.1 Power and Ground Pins

For clean, on-chip power distribution, the Celeron M processor has many $V_{CC}$ (power) and $V_{SS}$ (ground) inputs. All power pins must be connected to $V_{CC}$ power planes while all $V_{SS}$ pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. Please contact your Intel representative for more details. The processor $V_{CC}$ pins must be supplied the voltage determined by the VID (Voltage ID) pins.

## 3.2 FSB Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous generation processors, the Celeron M processor uses a differential clocking implementation and the core frequency is a multiple of the BCLK[1:0] frequency.

## 3.3 Voltage Identification

The processor uses seven voltage identification pins, VID[6:0], to support automatic selection of power supply voltages. The VID pins for the Celeron M processor are CMOS outputs driven by the processor VID circuitry. Table 2 specifies the voltage level corresponding to the state of VID[6:0]. A 1 in this refers to a high-voltage level and a 0 refers to low-voltage level.

**Table 2. Voltage Identification Definition (Sheet 1 of 4)**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Vcc (V) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.5000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.4875 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.4750 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.4625 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.4500 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.4375 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.4250 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.4125 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.4000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.3875 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.3750 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.3625 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.3500 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.3375 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1.3250 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.3125 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1.3000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.2875 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1.2750 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1.2625 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1.2500 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1.2375 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1.2250 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1.2125 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1.2000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1.1875 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1.1750 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1.1625 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1.1500 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1.1375 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1.1250 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1.1125 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1.1000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1.0875 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1.0750 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1.0625 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1.0500 |

**Table 2. Voltage Identification Definition (Sheet 2 of 4)**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Vcc (V) |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1.0375 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1.0250 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.0125 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1.0000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.9875 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0.9750 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0.9625 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0.9500 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0.9375 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0.9250 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0.9125 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0.9000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0.8875 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0.8750 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0.8625 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0.8500 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0.8375 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0.8250 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0.8125 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0.8000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0.7875 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0.7750 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0.7625 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0.7500 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0.7375 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0.7250 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0.7125 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0.7000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0.6875 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0.6750 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0.6625 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0.6500 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0.6375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0.6250 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0.6125 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0.6000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0.5875 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0.5750 |

**Table 2. Voltage Identification Definition (Sheet 3 of 4)**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Vcc (V) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0.5625 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0.5500 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0.5375 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0.5250 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0.5125 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0.5000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0.4875 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0.4750 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0.4625 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0.4500 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0.4375 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0.4250 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0.4125 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0.4000 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0.3875 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0.3750 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0.3625 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0.3500 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0.3375 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0.3250 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0.3125 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0.3000 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0.2875 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0.2750 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.2625 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0.2500 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0.2375 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0.2250 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0.2125 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0.2000 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0.1875 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0.1750 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0.1625 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0.1500 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0.1375 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0.1250 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0.1125 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0.1000 |

**Table 2. Voltage Identification Definition (Sheet 4 of 4)**

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Vcc (V) |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0.0875 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0.0750 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0.0625 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0.0500 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0.0375 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0.0250 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0.0125 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.0000 |

## 3.4 Catastrophic Thermal Protection

The Celeron M processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125°C (maximum), or if the THERMTRIP# signal is asserted, the $V_{CC}$ supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP# functionality is not guaranteed if the PWRGOOD signal is not asserted.

## 3.5 Reserved and Unused Pins

All RESERVED (RSVD) pins must remain unconnected. Connection of these pins to $V_{CC}$, $V_{SS}$, or to any other signal (including each other) can result in component malfunction or incompatibility with future Celeron M processors. See Table 14 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground ($V_{SS}$). Unused outputs can be left unconnected.

The TEST1 pin must have a stuffing option connection to $V_{SS}$ separately via 1-kΩ, pull-down resistors. The TEST2 pin must have a 51-Ω ±5%, pull-down resistor to $V_{SS}$.

For testing purposes it is recommended, but not required, to route the TEST3 and TEST4 pins through a ground referenced 55-Ω trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

## 3.6 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). These signals should be connected to the clock chip and the chipset system on the platform. The BSEL encoding for BCLK[1:0] is shown in Table 3.

**Table 3. BSEL[2:0] Encoding for BCLK Frequency**

| BSEL[2] | BSEL[1] | BSEL[0] | BCLK Frequency |
|---|---|---|---|
| L | L | L | RESERVED |
| L | L | H | 133 MHz |

## 3.7 FSB Signal Groups

In order to simplify the following discussion, the FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals that are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals that are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 4 identifies which signals are common clock, source synchronous, and asynchronous.

**Table 4. FSB Pin Groups (Sheet 1 of 2)**

| Signal Group | Type | Signals[1] |
|---|---|---|
| AGTL+ Common Clock Input | Synchronous to BCLK[1:0] | BPRI#, DEFER#, PREQ#[5], RESET#, RS[2:0]#, DPWR#, TRDY# |
| AGTL+ Common Clock I/O | Synchronous to BCLK[1:0] | ADS#, BNR#, BPM[3:0]#[3], BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#[3] |
| AGTL+ Source Synchronous I/O | Synchronous to assoc. strobe | |

| Signals | Associated Strobe |
|---|---|
| REQ[4:0]#, A[16:3]# | ADSTB[0]# |
| A[35:17]#[6] | ADSTB[1]# |
| D[15:0]#, DINV0# | DSTBP0#, DSTBN0# |
| D[31:16]#, DINV1# | DSTBP1#, DSTBN1# |
| D[47:32]#, DINV2# | DSTBP2#, DSTBN2# |
| D[63:48]#, DINV3# | DSTBP3#, DSTBN3# |

**Table 4. FSB Pin Groups (Sheet 2 of 2)**

| Signal Group | Type | Signals[1] |
|---|---|---|
| AGTL+ Strobes | Synchronous to BCLK[1:0] | ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]# |
| CMOS Input | Asynchronous | A20M#, DPRSTP#, DPSLP#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK# |
| Open Drain Output | Asynchronous | FERR#, IERR#, THERMTRIP# |
| Open Drain I/O | Asynchronous | PROCHOT#[4] |
| CMOS Output | Asynchronous | PSI#, VID[6:0], BSEL[2:0] |
| CMOS Input | Synchronous to TCK | TCK, TDI, TMS, TRST# |
| Open Drain Output | Synchronous to TCK | TDO |
| FSB Clock | Clock | BCLK[1:0] |
| Power/Other | | COMP[3:0], DBR#[2], GTLREF, RSVD, TEST2, TEST1, THERMDA, THERMDC, $V_{CC}$, $V_{CCA}$, $V_{CCP}$, $V_{CC\_SENSE}$, $V_{SS}$, $V_{SS\_SENSE}$ |

**NOTES:**
1. Refer to Chapter 4, "Package Mechanical Specifications and Pin Information" for signal descriptions and termination requirements.
2. **In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.**
3. BPM[2:1]# and PRDY# are AGTL+ output only signals.
4. PROCHOT# signal type is open drain output and CMOS input.
5. On-die termination differs from other AGTL+ signals, please contact your Intel Representative for more details.
6. When paired with a chipset limited to 32-bit addressing, A[35:32] should remain unconnected.

## 3.8 CMOS Signals

CMOS input signals are shown in Table 4. Legacy output FERR#, IERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the CMOS signals are required to be asserted for at least three BCLKs in order for the processor to recognize them. See Section 3.10 for the DC specifications for the CMOS signal groups.

## 3.9 Maximum Ratings

Table 5 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute

maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

**Table 5. Processor Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Unit | Notes[1] |
|---|---|---|---|---|---|
| $T_{STORAGE}$ | Processor storage temperature | -40 | 85 | °C | 2,3,4 |
| $V_{CC}$ | Any processor supply voltage with respect to $V_{SS}$ | -0.3 | 1.55 | V | |
| $V_{inAGTL+}$ | AGTL+ buffer DC input voltage with respect to $V_{SS}$ | -0.1 | 1.55 | V | |
| $V_{inAsynch\_CMOS}$ | CMOS buffer DC input voltage with respect to $V_{SS}$ | -0.1 | 1.55 | V | |

**NOTES:**
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
3. This rating applies to the processor and does not include any tray or packaging.
4. Failure to adhere to this specification can affect the long term reliability of the processor.

## 3.10 Processor DC Specifications

**The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise**. See Table 4 for the pin signal definitions and signal pin assignments. Most of the signals on the FSB are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 9. DC specifications for the CMOS group are listed in Table 10.

Table 6 through Table 11 list the DC specifications and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Active mode loadline specifications apply in all states except in the Deep Sleep state. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications are at Tjunction = 100°C. Care should be taken to read all notes associated with each parameter.

## Table 6. DC Voltage and Current Specifications

| Symbol | Parameter | | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ of the Processor Core | | 0.95 | 1.15 | 1.30 | V | 1, 2 |
| $V_{CC,BOOT}$ | Default $V_{CC}$ Voltage for Initial Power Up | | | 1.20 | | V | 2 |
| $V_{CCP}$ | AGTL+ Termination Voltage | | 1.00 | 1.05 | 1.10 | V | |
| $V_{CCA}$ | PLL Supply Voltage | | 1.425 | 1.5 | 1.575 | V | |
| $I_{CCDES}$ | $I_{CC}$ for Celeron® M processors Recommended Design Targets: | | | | 36 | A | 5 |
| $I_{CC}$ | $I_{CC}$ for Celeron M Processors | | | | | A | |
| | Processor Number | Frequency | | | | | |
| | 520-fused | 1.60 GHz | | | 34.5 | A | 3,11 |
| | 530-fused | 1.73 GHz | | | 34.5 | A | 3,11 |
| | 520 | 1.60 GHz | | | 34.5 | A | 3 |
| | 530 | 1.73 GHz | | | 34.5 | A | 3 |
| $I_{AH}$, $I_{SGNT}$ | $I_{CC}$ Auto-Halt & Stop-Grant | | | | 21 | A | 3,4 |
| $I_{SLP}$ | $I_{CC}$ Sleep | | | | 20.5 | A | 3,4 |
| $I_{DSLP}$ | $I_{CC}$ Deep Sleep | | | | 18.6 | A | 3,4 |
| $dI_{CC/DT}$ | $V_{CC}$ Power Supply Current Slew Rate at CPU Package Pin | | | | 600 | A/µs | 6, 7 |
| $I_{CCA}$ | $I_{CC}$ for $V_{CCA}$ Supply | | | | 130 | mA | |
| $I_{CCP}$ | $I_{CC}$ for $V_{CCP}$ Supply before $V_{CC}$ Stable<br>$I_{CC}$ for $V_{CCP}$ Supply after $V_{CC}$ Stable | | | | 4.5<br>2.5 | A<br>A | 9<br>10 |

**NOTES:**

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range.
2. The voltage specifications are assumed to be measured across $V_{CC\_SENSE}$ and $V_{SS\_SENSE}$ pins at the socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100°C Tj.
4. Specified at the VID voltage.
5. The $I_{CCDES}$(max) specification of 36 A comprehends only the Celeron M processor 500 series.
6. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal $V_{CC}$. Not 100% tested.
7. Measured at the bulk capacitors on the motherboard.
8. $V_{CC,BOOT}$ tolerance shown in Figure 3
9. This is a steady-state Iccp current specification, which is applicable when both $V_{CCP}$ and $V_{CC\_CORE}$ are high.
10. This is a power-up peak current specification, which is applicable when $V_{CCP}$ is high and $V_{CC\_CORE}$ is low.
11. These units will display processor family ID 06F6h.

## Table 7. DC Voltage and Current Specifications ULV

| Symbol | Parameter | | | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ of the Processor Core | | | 0.8 | | 0.975 | V | 1, 2 |
| $V_{CC,BOOT}$ | Default $V_{CC}$ Voltage for Initial Power Up | | | | 1.20 | | V | 2, 7, 9 |
| $V_{CCP}$ | AGTL+ Termination Voltage | | | 1.00 | 1.05 | 1.10 | V | |
| $V_{CCA}$ | PLL Supply Voltage | | | 1.425 | 1.5 | 1.575 | V | |
| $I_{CCDES}$ | $I_{CC}$ for Processor Recommended Design Targets: | | | | | 17 | A | 5 |
| $I_{CC}$ | $I_{CC}$ for Processor | | | | | | A | |
| | Processor Number | Frequency | Die Variant | | | | | |
| | 523 | 933 MHz | 1 M | | | 8 | A | 3,4 |
| $I_{AH}$, $I_{SGNT}$ | $I_{CC}$ Auto-Halt & Stop-Grant | | | | | 7.4 | A | 3,4 |
| $I_{SLP}$ | $I_{CC}$ Sleep | | | | | 7.3 | A | 3,4 |
| $I_{DSLP}$ | $I_{CC}$ Deep Sleep | | | | | 6.2 | A | 3,4 |
| $dI_{CC/DT}$ | $V_{CC}$ Power Supply Current Slew Rate at CPU Package Pin | | | | | 600 | A/µs | 6, 8 |
| $I_{CCA}$ | $I_{CC}$ for $V_{CCA}$ Supply | | | | | 130 | mA | |
| $I_{CCP}$ | $I_{CC}$ for $V_{CCP}$ Supply before $V_{CC}$ stable<br>$I_{CC}$ for $V_{CCP}$Supply after $V_{CC}$ stable | | | | | 4.5<br>2.5 | A<br>A | 10<br>11 |

**NOTES:**

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range.
2. The voltage specifications are assumed to be measured across $V_{CC\_SENSE}$ and $V_{SS\_SENSE}$ pins at the socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100°C Tj.
4. Specified at the VID voltage.
5. The $I_{CCDES}$(max) specification of 36 A comprehends only the Celeron M processor 500 series.
6. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal $V_{CC}$. Not 100% tested.
7. Measured at the bulk capacitors on the motherboard.
8. $V_{CC,BOOT}$ tolerance shown in Figure 3
9. This is a steady-state Iccp current specification, which is applicable when both $V_{CCP}$ and $V_{CC\_CORE}$ are high.
10. This is a power-up peak current specification, which is applicable when $V_{CCP}$ is high and $V_{CC\_CORE}$ is low.
11. These units will display processor family ID 06F6h.

**Figure 3. Active $V_{CC}$ and $I_{CC}$ Loadline Standard Voltage**

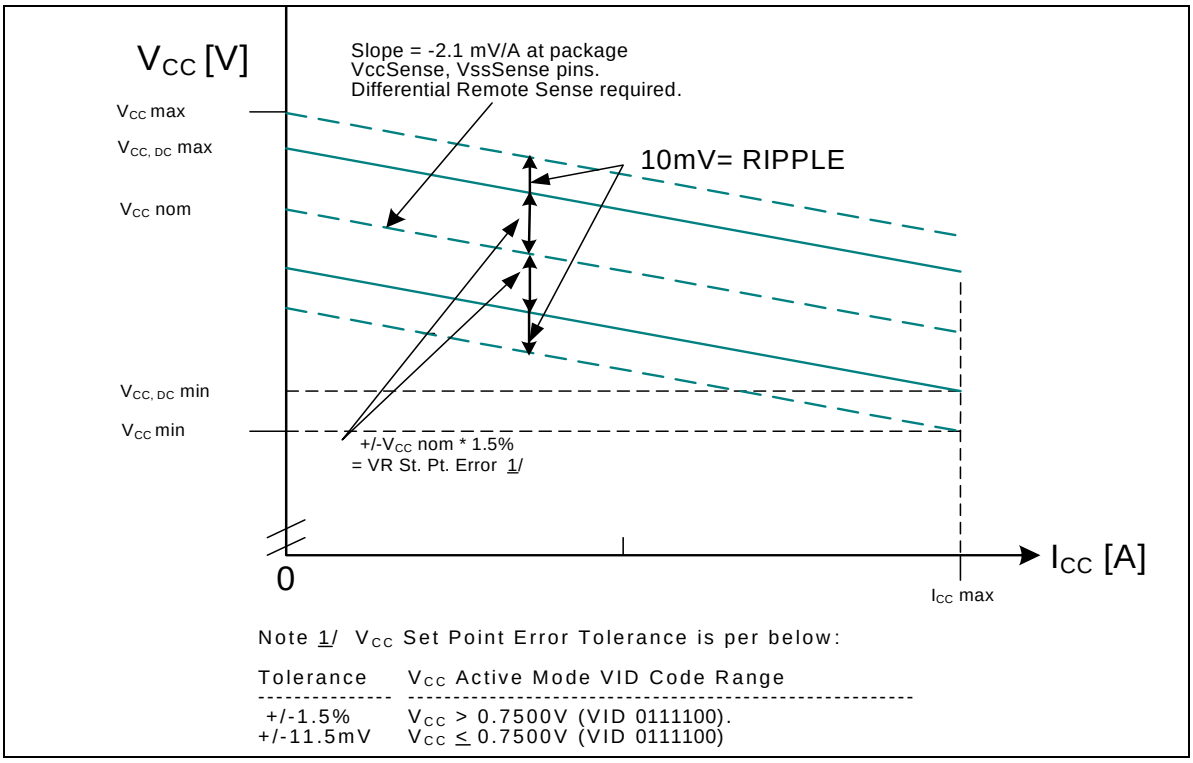
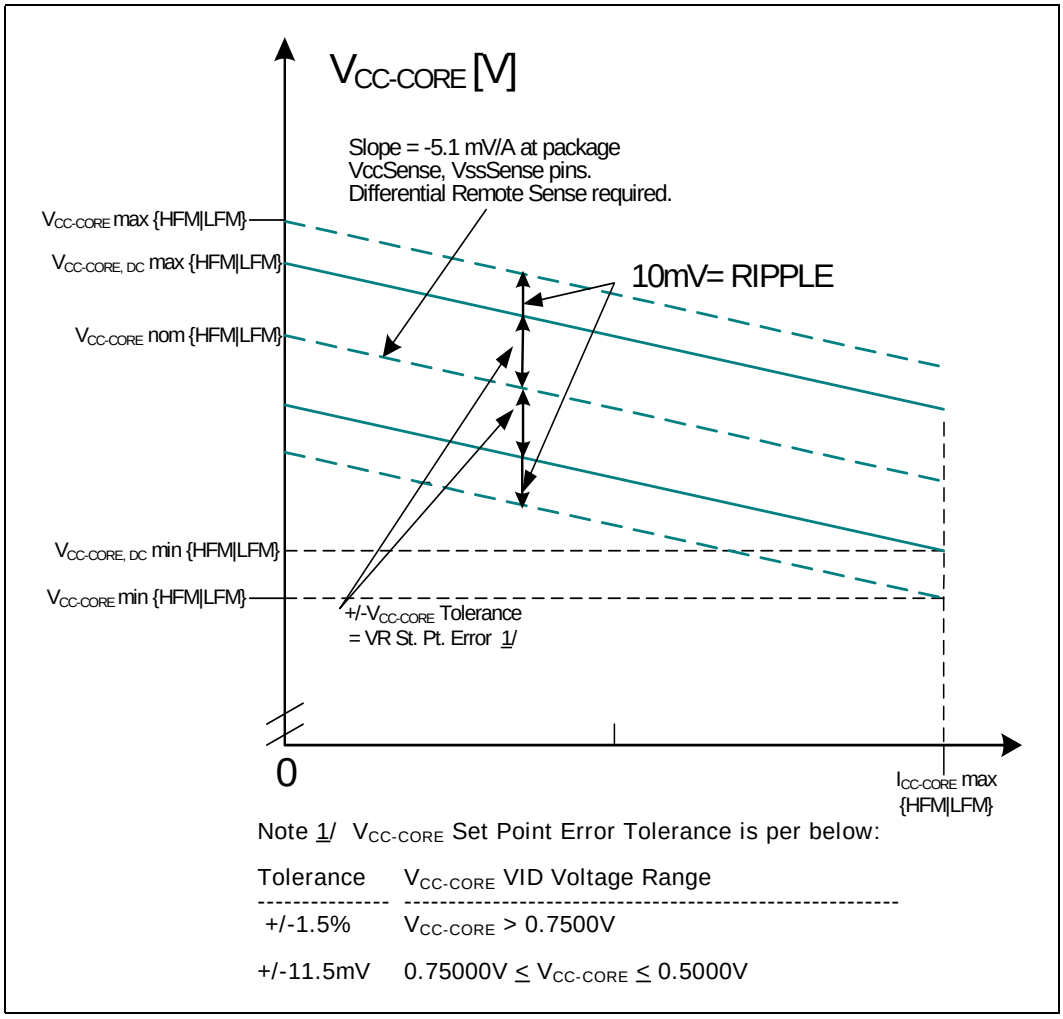



**Table 8. FSB Differential BCLK Specifications**

| Symbol | Parameter | Min | Typ | Max | Unit | Notes[1] |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 0.660 | 0.710 | 0.85 | V | |
| $V_{IL}$ | Input Low Voltage | | 0 | | V | |
| $V_{CROSS}$ | Crossing Voltage | 0.25 | 0.35 | 0.55 | V | 2 |
| $\Delta V_{CROSS}$ | Range of Crossing Points | | | 0.14 | V | 6 |
| $V_{TH}$ | Threshold Region | $V_{CROSS}$ -0.100 | | $V_{CROSS}$+0.100 | V | 3 |
| $I_{LI}$ | Input Leakage Current | | | ±100 | µA | 4 |
| Cpad | Pad Capacitance | 0.95 | 1.2 | 1.45 | pF | 5 |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. Threshold Region is defined as a region entered about the crossing voltage in which the differential receiver switches. It includes input threshold hysteresis.
4. For Vin between 0 V and $V_{IH}$.
5. Cpad includes die capacitance only. No package parasitics are included.
6. $\Delta V_{CROSS}$ is defined as the total variation of all crossing voltages as defined in note 2.

**Figure 4. Active $V_{CC}$ and $I_{CC}$ Loadline Single-core Ultra Low Voltage**




Note 1/ $V_{CC-CORE}$ Set Point Error Tolerance is per below:

| Tolerance | $V_{CC-CORE}$ VID Voltage Range |
|---|---|
| +/-1.5% | $V_{CC-CORE} > 0.7500V$ |
| +/-11.5mV | $0.75000V \leq V_{CC-CORE} \leq 0.5000V$ |

## Table 9. AGTL+ Signal Group DC Specifications

| Symbol | Parameter | Min | Typ | Max | Unit | Notes[1] |
|---|---|---|---|---|---|---|
| $V_{CCP}$ | I/O Voltage | 1.00 | 1.05 | 1.10 | V | |
| GTLREF | Reference Voltage | | 2/3 $V_{CCP}$ | | V | 6 |
| $R_{COMP}$ | Compensation Resistor | 27.23 | 27.5 | 27.78 | Ω | 10 |
| $R_{ODT}$ | Termination Resistor | | 55 | | Ω | 11 |
| $V_{IH}$ | Input High Voltage | GTLREF+0.10 | $V_{CCP}$ | $V_{CCP}$ +0.10 | V | 3,6 |
| $V_{IL}$ | Input Low Voltage | -0.10 | 0 | GTLREF-0.10 | V | 2,4 |
| $V_{OH}$ | Output High Voltage | $V_{CCP}$ -0.10 | $V_{CCP}$ | $V_{CCP}$ | | 6 |
| $R_{TT}$ | Termination Resistance | 50 | 55 | 61 | Ω | 7 |
| $R_{ON}$ | Buffer On Resistance | 22 | 25 | 28 | Ω | 5 |
| $I_{LI}$ | Input Leakage Current | | | ±100 | µA | 8 |
| Cpad | Pad Capacitance | 1.6 | 2.1 | 2.55 | pF | 9 |

**NOTES:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. $V_{IL}$ is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. $V_{IH}$ is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. $V_{IH}$ and $V_{OH}$ may experience excursions above $V_{CCP}$. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull-down driver resistance. Refer to processor I/O Buffer Models for I/V characteristics. Measured at $0.31*V_{CCP}$. $R_{ON}$ (min) = $0.38*R_{TT}$. $R_{ON}$ (typ) = $0.45*R_{TT}$. $R_{ON}$ (max) = $0.52*R_{TT}$.
6. GTLREF should be generated from $V_{CCP}$ with a 1% tolerance resistor divider. The $V_{CCP}$ referred to in these specifications is the instantaneous $V_{CCP}$.
7. $R_{TT}$ is the on-die termination resistance measured at $V_{OL}$ of the AGTL+ output driver. Measured at $0.31*V_{CCP}$. $R_{TT}$ is connected to $V_{CCP}$ on-die. Refer to processor I/O buffer models for I/V characteristics.
8. Specified with on-die $R_{TT}$ and $R_{ON}$ are turned off. Vin between 0 and $V_{CCP}$.
9. Cpad includes die capacitance only. No package parasitics are included.
10. This is the external resistor on the comp pins.
11. On-die termination resistance, measured at $0.33*V_{CCP}$.

## Table 10. CMOS Signal Group DC Specifications

| Symbol | Parameter | Min | Typ | Max | Unit | Notes[1] |
|---|---|---|---|---|---|---|
| $V_{CCP}$ | I/O Voltage | 1.00 | 1.05 | 1.10 | V | |
| $V_{IH}$ | Input High Voltage | 0.7*$V_{CCP}$ | $V_{CCP}$ | $V_{CCP}$+0.1 | V | 2 |
| $V_{IL}$ | Input Low Voltage CMOS | -0.10 | 0.00 | 0.3*$V_{CCP}$ | V | 2, 3 |
| $V_{OH}$ | Output High Voltage | 0.9*$V_{CCP}$ | $V_{CCP}$ | $V_{CCP}$+0.1 | V | 2 |
| $V_{OL}$ | Output Low Voltage | -0.10 | 0 | 0.1*$V_{CCP}$ | V | 2 |
| $I_{OH}$ | Output High Current | 1.5 | | 4.1 | mA | 5 |
| $I_{OL}$ | Output Low Current | 1.5 | | 4.1 | mA | 4 |
| $I_{LI}$ | Input Leakage Current | | | ±100 | µA | 6 |
| Cpad1 | Pad Capacitance | 1.6 | 2.1 | 2.55 | pF | 7 |
| Cpad2 | Pad Capacitance for CMOS Input | 0.95 | 1.2 | 1.45 | | 8 |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The $V_{CCP}$ referred to in these specifications refers to instantaneous $V_{CCP}$.
3. Refer to the processor I/O Buffer Models for I/V characteristics.
4. Measured at 0.1*$V_{CCP}$.
5. Measured at 0.9*$V_{CCP}$.
6. For Vin between 0 V and $V_{CCP}$. Measured when the driver is tristated.
7. Cpad1 includes die capacitance only for DPRSTP#, DPSLP#, PWRGOOD. No package parasitics are included.
8. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.

## Table 11. Open Drain Signal Group DC Specifications

| Symbol | Parameter | Min | Typ | Max | Unit | Notes[1] |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $V_{CCP}$ -5% | $V_{CCP}$ | $V_{CCP}$ +5% | V | 3 |
| $V_{OL}$ | Output Low Voltage | 0 | | 0.20 | V | |
| $I_{OL}$ | Output Low Current | 16 | | 50 | mA | 2 |
| $I_{LO}$ | Output Leakage Current | | | ±200 | µA | 4 |
| Cpad | Pad Capacitance | 1.9 | 2.2 | 2.45 | pF | 5 |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2 V.
3. $V_{OH}$ is determined by value of the external pull-up resistor to $V_{CCP}$. Please refer to platform design guide for details.
4. For Vin between 0 V and $V_{OH}$.
5. Cpad includes die capacitance only. No package parasitics are included.

§ §

# 4 Package Mechanical Specifications and Pin Information

## 4.1 Package Mechanical Specifications

The Celeron M processor 500 series is available in a 478-pin Micro-FCPGA package and Micro-FCBGA package for Ultra Low Voltage parts. Package mechanical dimensions are shown in Figure 5.

### 4.1.1 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted in the keep-out areas. The location and quantity of the capacitors may change but will remain within the component keep-in. See Figure 6 for keep-out zones.

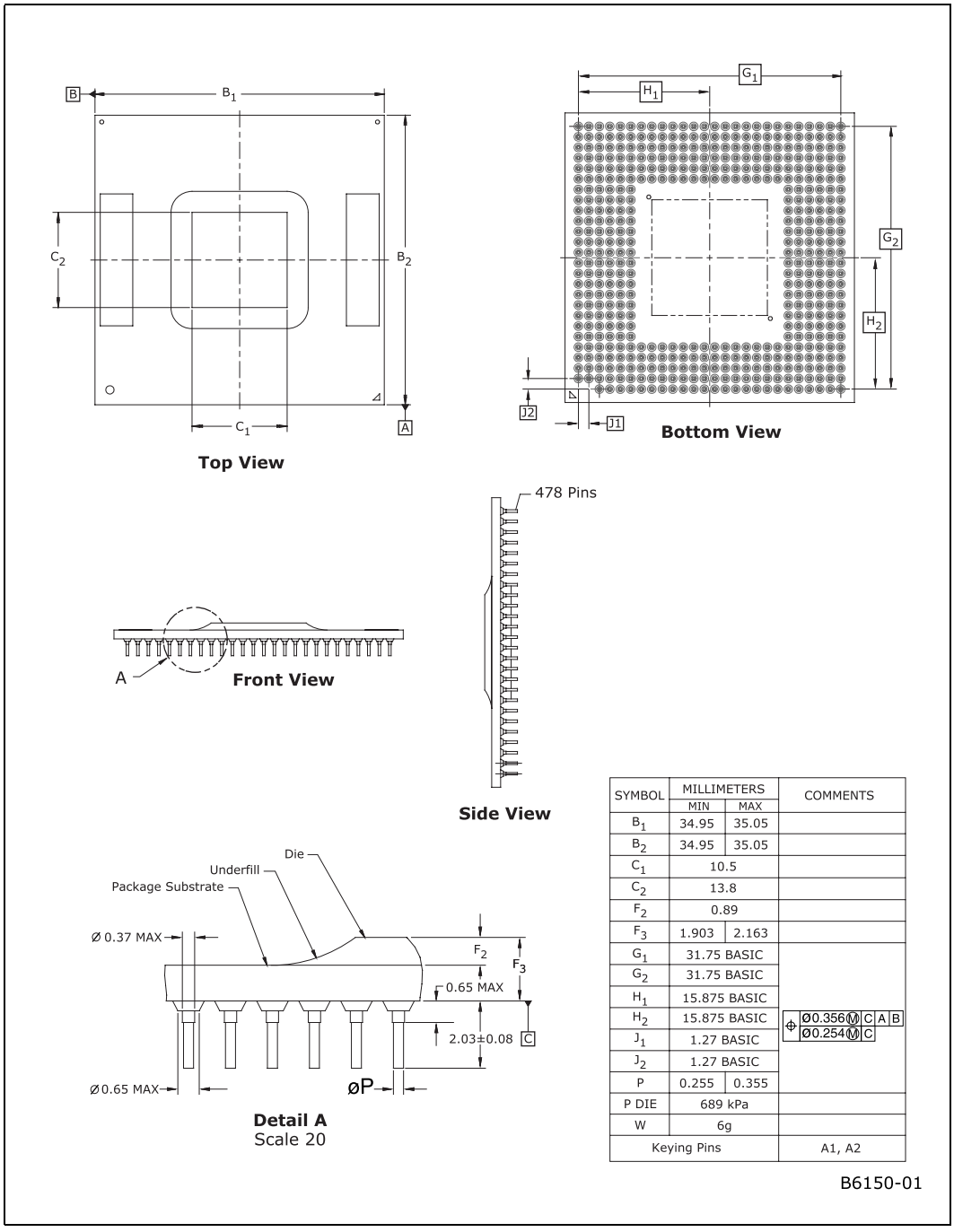
### 4.1.2 Package Loading Specifications

Maximum mechanical package loading specifications are given in Figure 5. These specifications are static compressive loading in the direction normal to the processor. This maximum load limit should not be exceeded during shipping conditions, standard use condition, or by the thermal solution. In addition, there are additional load limitations against transient bend, shock, and tensile loading. These limitations are more platform specific and should be obtained by contacting your field support. Moreover, the processor package substrate should not be used as a mechanical reference or load-bearing surface for the thermal or mechanical solution.

### 4.1.3 Processor Mass Specifications

The typical mass of the processor is given in Figure 5. This mass includes all the components that are included in the package.

## Figure 5. 1-MB Fused Micro-FCPGA Processor Package Drawing (1 of 2)




| SYMBOL | MILLIMETERS | | COMMENTS |
|---|---|---|---|
| | MIN | MAX | |
| $B_1$ | 34.95 | 35.05 | |
| $B_2$ | 34.95 | 35.05 | |
| $C_1$ | 10.5 | | |
| $C_2$ | 13.8 | | |
| $F_2$ | 0.89 | | |
| $F_3$ | 1.903 | 2.163 | |
| $G_1$ | 31.75 BASIC | | |
| $G_2$ | 31.75 BASIC | | |
| $H_1$ | 15.875 BASIC | | |
| $H_2$ | 15.875 BASIC | | ⌖ Ø0.356Ⓜ C A B<br>Ø0.254Ⓜ C |
| $J_1$ | 1.27 BASIC | | |
| $J_2$ | 1.27 BASIC | | |
| P | 0.255 | 0.355 | |
| P DIE | 689 kPa | | |
| W | 6g | | |
| Keying Pins | | | A1, A2 |

B6150-01

## Figure 6. 1-MB Fused Micro-FCPGA Processor Package Drawing (2 of 2)

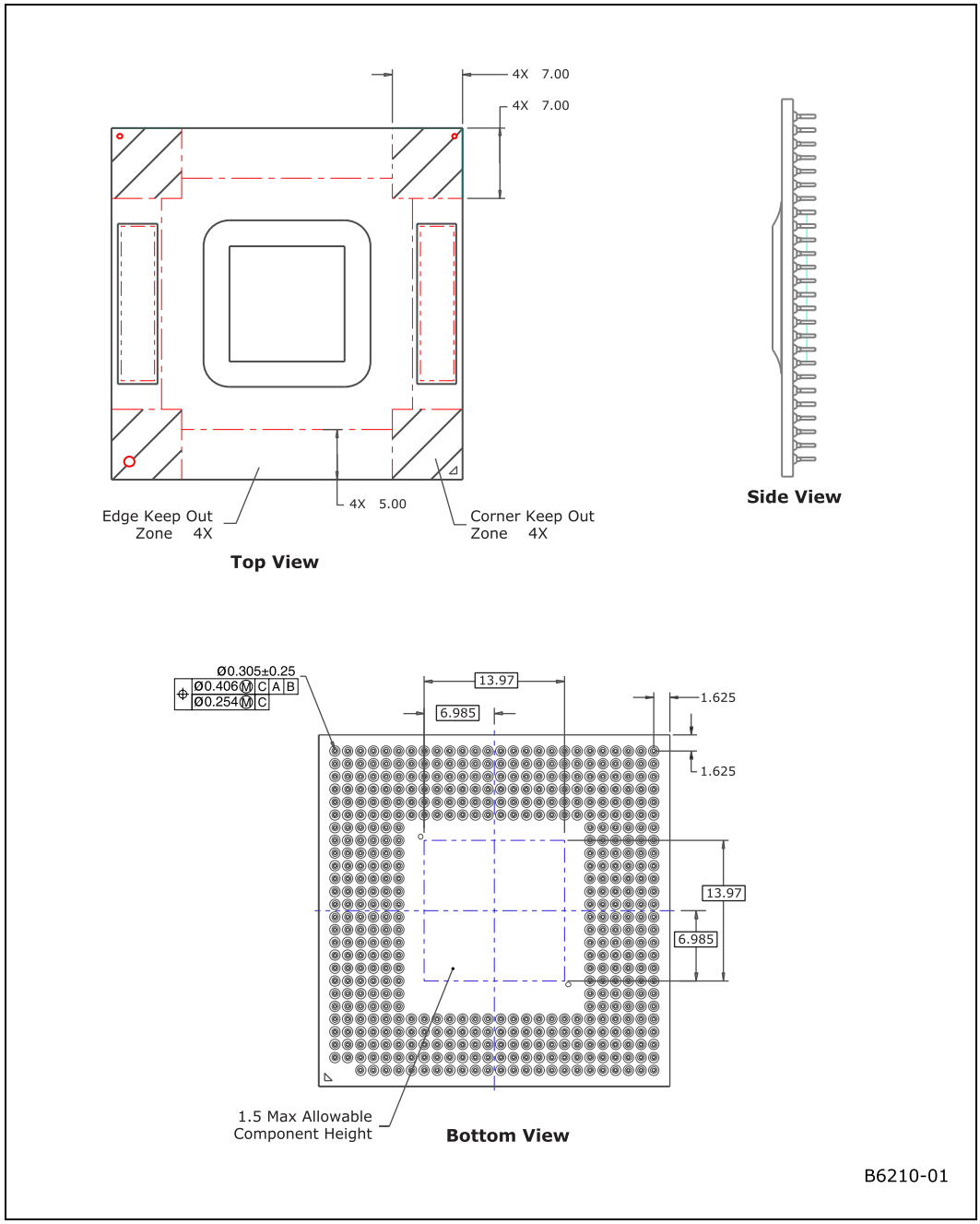
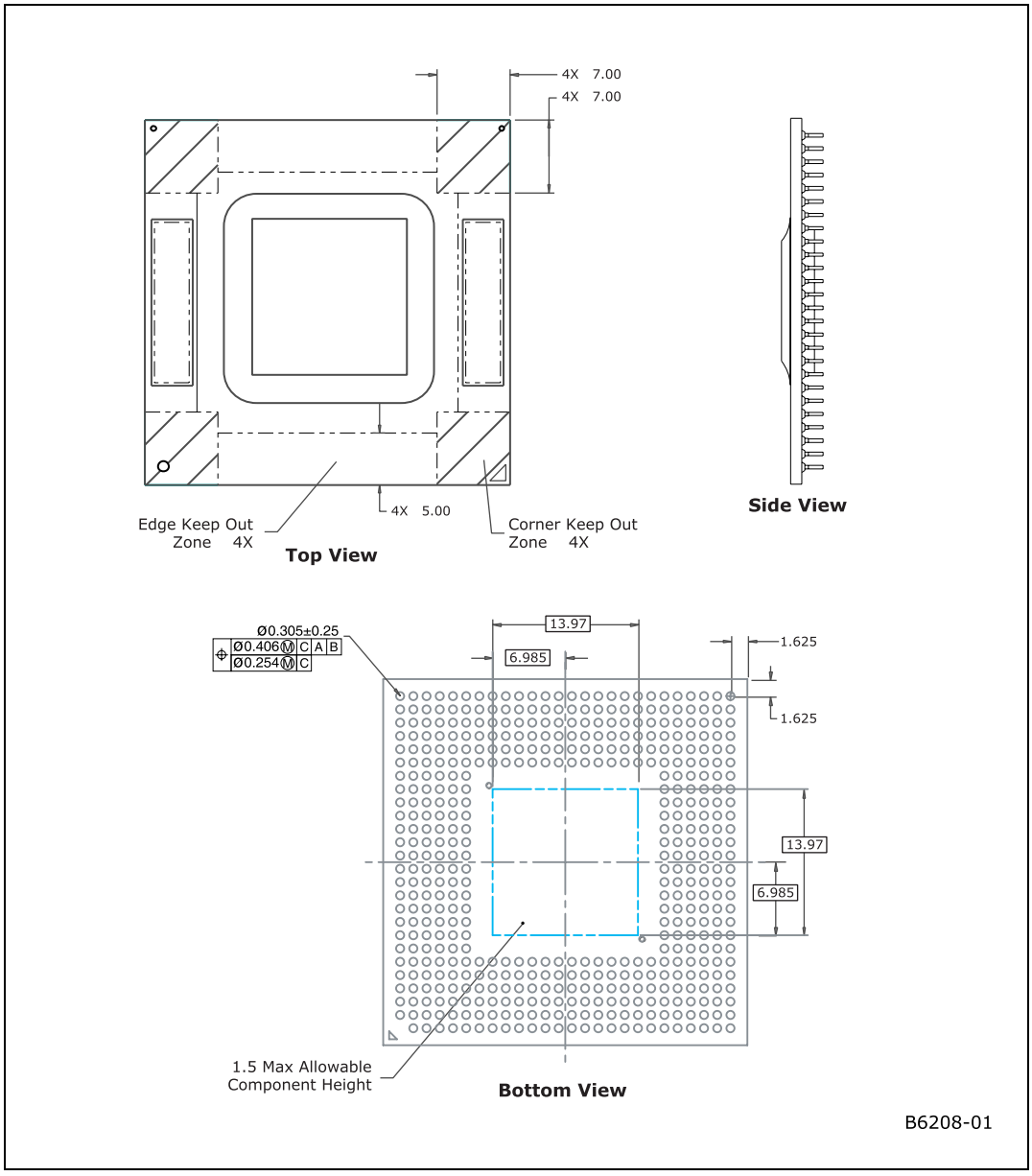
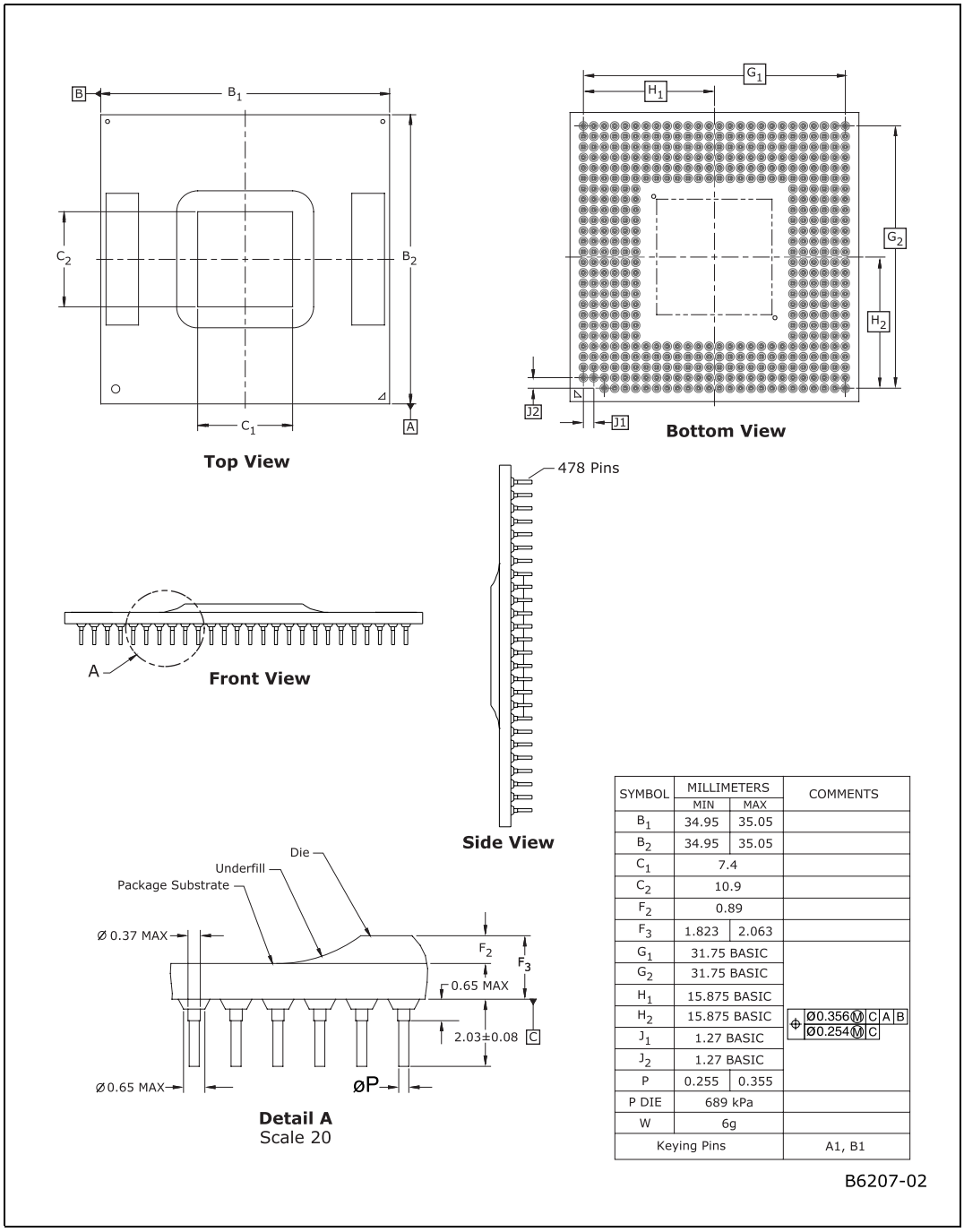


**Figure 7. 1-MB Micro-FCPGA Processor Package Drawing (1 of 2)**



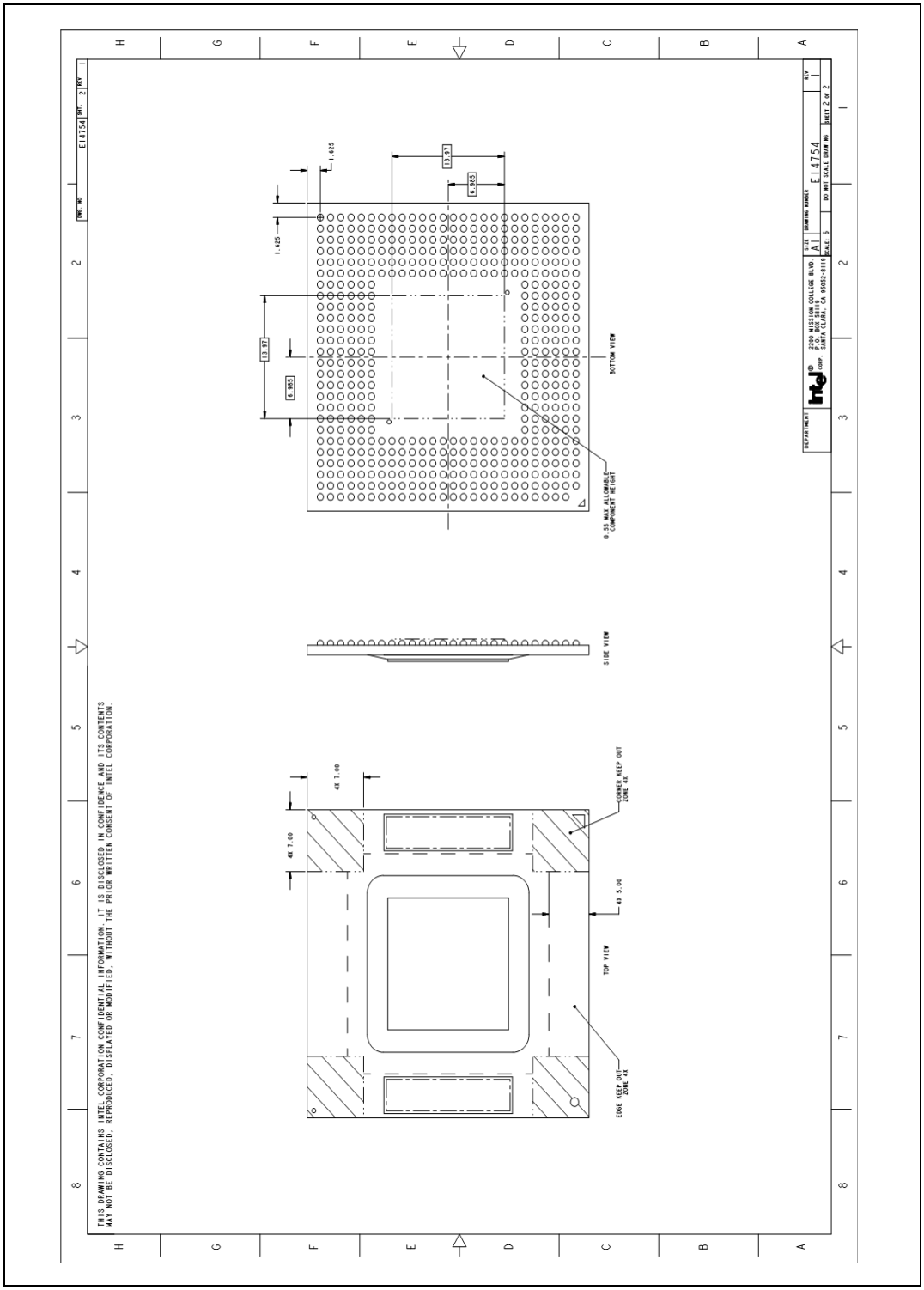
## Figure 8. 1-MB Micro-FCPGA Processor Package Drawing (2 of 2)



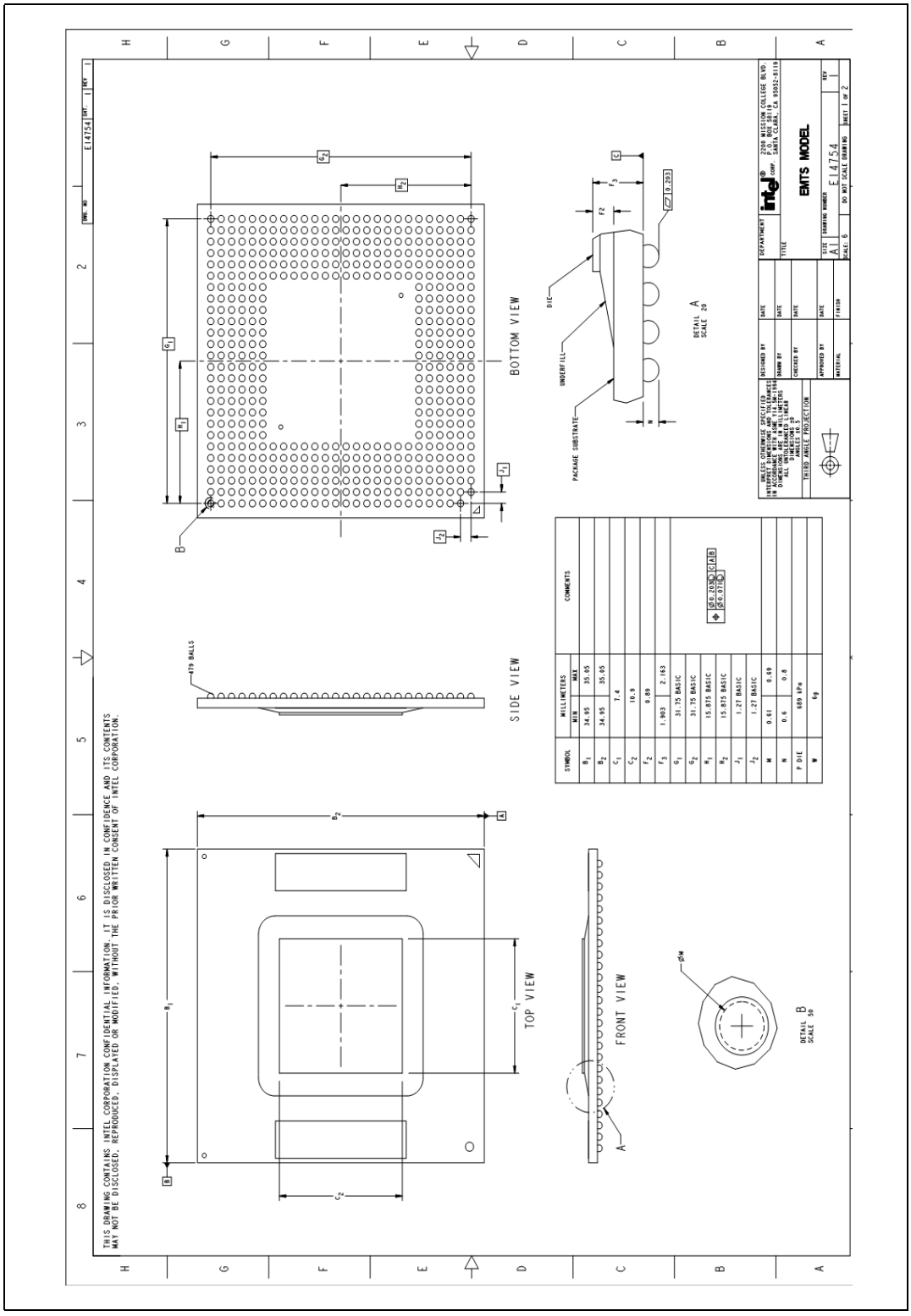

| SYMBOL | MILLIMETERS | | COMMENTS |
|---|---|---|---|
| | MIN | MAX | |
| $B_1$ | 34.95 | 35.05 | |
| $B_2$ | 34.95 | 35.05 | |
| $C_1$ | 7.4 | | |
| $C_2$ | 10.9 | | |
| $F_2$ | 0.89 | | |
| $F_3$ | 1.823 | 2.063 | |
| $G_1$ | 31.75 BASIC | | |
| $G_2$ | 31.75 BASIC | | |
| $H_1$ | 15.875 BASIC | | |
| $H_2$ | 15.875 BASIC | | ⌖ Ø0.356Ⓜ C A B<br>Ø0.254Ⓜ C |
| $J_1$ | 1.27 BASIC | | |
| $J_2$ | 1.27 BASIC | | |
| P | 0.255 | 0.355 | |
| P DIE | 689 kPa | | |
| W | 6g | | |
| Keying Pins | | | A1, B1 |

B6207-02

**Figure 9. 1-MB Micro-FCBGA Processor Package Drawing (1 of 2)**



## Figure 10. 1-MB Micro-FCBGA Processor Package Drawing (2 of 2)



## 4.2 Processor Pinout and Pin List

Table 12 shows the top view pinout of the Celeron M processor.

**Table 12. The Coordinates of the Processor Pins as Viewed from the Top of the Package (Sheet 1 of 2)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | | SMI# | VSS | FERR# | A20M# | VCC | VSS | VCC | VCC | VSS | VCC | VCC | A |
| B | RESET# | RSVD | INIT# | LINT1 | DPSLP# | VSS | VCC | VSS | VCC | VCC | VSS | VCC | VSS | B |
| C | RSVD] | VSS | RSVD | IGNNE # | VSS | LINT0 | THERM TRIP# | VSS | VCC | VCC | VSS | VCC | VCC | C |
| D | VSS | RSVD | RSVD | VSS | STPCLK # | PWRGO OD | SLP# | VSS | VCC | VCC | VSS | VCC | VSS | D |
| E | DBSY# | BNR# | VSS | HITM# | DPRSTP # | VSS | VCC | VSS | VCC | VCC | VSS | VCC | VCC | E |
| F | BR0# | VSS | RS[0]# | RS[1]# | VSS | RSVD | VCC | VSS | VCC | VCC | VSS | VCC | VSS | F |
| G | VSS | TRDY# | RS[2]# | VSS | BPRI# | HIT# | | | | | | | | G |
| H | ADS# | REQ[1] # | VSS | LOCK# | DEFER# | VSS | | | | | | | | H |
| J | A[9]# | VSS | REQ[3] # | A[3]# | VSS | VCCP | | | | | | | | J |
| K | VSS | REQ[2] # | REQ[0] # | VSS | A[6]# | VCCP | | | | | | | | K |
| L | A[13]# | ADSTB[ 0]# | VSS | A[4]# | REQ[4] # | VSS | | | | | | | | L |
| M | A[7]# | VSS | A[5]# | RSVD | VSS | VCCP | | | | | | | | M |
| N | VSS | A[8]# | A[10]# | VSS | RSVD | VCCP | | | | | | | | N |
| P | A[15]# | A[12]# | VSS | A[14]# | A[11]# | VSS | | | | | | | | P |
| R | A[16]# | VSS | A[19]# | A[24]# | VSS | VCCP | | | | | | | | R |
| T | VSS | RSVD | A[26]# | VSS | A[25]# | VCCP | | | | | | | | T |
| U | COMP[2] | A[23]# | VSS | A[21]# | A[18]# | VSS | | | | | | | | U |
| V | COMP[3] | VSS | RSVD | ADSTB[ 1]# | VSS | VCCP | | | | | | | | V |
| W | VSS | A[30]# | A[27]# | VSS | A[28]# | A[20]# | | | | | | | | W |
| Y | A[31]# | A[17]# | VSS | A[29]# | A[22]# | VSS | | | | | | | | Y |
| AA | A[32]# | VSS | A[35]# | A[33]# | VSS | TDI | VCC | VSS | VCC | VCC | VSS | VCC | VCC | AA |
| AB | VSS | A[34]# | TDO | VSS | TMS | TRST# | VCC | VSS | VCC | VCC | VSS | VCC | VSS | AB |
| AC | PREQ# | PRDY# | VSS | BPM[3] # | TCK | VSS | VCC | VSS | VCC | VCC | VSS | VCC | VCC | AC |
| AD | BPM[2]# | VSS | BPM[1] # | BPM[0] # | VSS | VID[0] | VCC | VSS | VCC | VCC | VSS | VCC | VSS | AD |
| AE | VSS | VID[6] | VID[4] | VSS | VID[2] | PSI# | VSS SENSE | VSS | VCC | VCC | VSS | VCC | VCC | AE |
| AF | TEST3 | VID[5] | VSS | VID[3] | VID[1] | VSS | VCC SENSE | VSS | VCC | VCC | VSS | VCC | VSS | AF |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |

## Table 13. The Coordinates of the Processor Pins as Viewed from the Top of the Package (Sheet 2 of 2)

| | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | VCC | VSS | VCC | VCC | VSS | VCC | BCLK[1] | BCLK[0] | VSS | THRMDA | THRMDC | VSS | A |
| B | VCC | VCC | VSS | VCC | VCC | VSS | VCC | VSS | BSEL[0] | BSEL[1] | VSS | TEST4 | VCCA | B |
| C | VSS | VCC | VSS | VCC | VCC | VSS | DBR# | BSEL[2] | VSS | RSVD | RSVD | VSS | TEST1 | C |
| D | VCC | VCC | VSS | VCC | VCC | VSS | IERR# | PROCHOT# | RSVD | VSS | DPWR# | TEST2 | VSS | D |
| E | VSS | VCC | VSS | VCC | VCC | VSS | VCC | VSS | D[0]# | D[7]# | VSS | D[6]# | D[2]# | E |
| F | VCC | VCC | VSS | VCC | VCC | VSS | VCC | DRDY# | VSS | D[4]# | D[1]# | VSS | D[13]# | F |
| G | | | | | | | | VCCP | DSTBP[0]# | VSS | D[9]# | D[5]# | VSS | G |
| H | | | | | | | | VSS | D[3]# | DSTBN[0]# | VSS | D[15]# | D[12]# | H |
| J | | | | | | | | VCCP | VSS | D[11]# | D[10]# | VSS | DINV[0]# | J |
| K | | | | | | | | VCCP | D[14]# | VSS | D[8]# | D[17]# | VSS | K |
| L | | | | | | | | VSS | D[21]# | D[22]# | VSS | D[20]# | D[29]# | L |
| M | | | | | | | | VCCP | VSS | D[23]# | DSTBN[1]# | VSS | DINV[1]# | M |
| N | | | | | | | | VCCP | D[16]# | VSS | D[31]# | DSTBP[1]# | VSS | N |
| P | | | | | | | | VSS | D[25]# | D[26]# | VSS | D[24]# | D[18]# | P |
| R | | | | | | | | VCCP | VSS | D[19]# | D[28]# | VSS | COMP[0] | R |
| T | | | | | | | | VCCP | RSVD | VSS | D[27]# | D[30]# | VSS | T |
| U | | | | | | | | VSS | D[39]# | D[37]# | VSS | D[38]# | COMP[1] | U |
| V | | | | | | | | VCCP | VSS | DINV[2]# | D[34]# | VSS | D[35]# | V |
| W | | | | | | | | VCCP | D[41]# | VSS | DSTBN[2]# | D[36]# | VSS | W |
| Y | | | | | | | | VSS | D[45]# | D[42]# | VSS | DSTBP[2]# | D[44]# | Y |
| AA | VSS | VCC | VSS | VCC | VCC | VSS | VCC | D[51]# | VSS | D[32]# | D[47]# | VSS | D[43]# | AA |
| AB | VCC | VCC | VSS | VCC | VCC | VSS | VCC | D[52]# | D[50]# | VSS | D[33]# | D[40]# | VSS | AB |
| AC | VSS | VCC | VSS | VCC | VCC | VSS | DINV[3]# | VSS | D[48]# | D[49]# | VSS | D[53]# | D[46]# | AC |
| AD | VCC | VCC | VSS | VCC | VCC | VSS | D[54]# | D[59]# | VSS | DSTBN[3]# | D[57]# | VSS | GTLREF | AD |
| AE | VSS | VCC | VSS | VCC | VCC | VSS | VCC | D[58]# | D[55]# | VSS | DSTBP[3]# | D[60]# | VSS | AE |
| AF | VCC | VCC | VSS | VCC | VCC | VSS | VCC | VSS | D[62]# | D[56]# | VSS | D[61]# | D[63]# | AF |
| | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |



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**Table 14. Pin Listing by Pin Name (Sheet 1 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| A[3]# | J4 | Source Synch | Input/ Output |
| A[4]# | L4 | Source Synch | Input/ Output |
| A[5]# | M3 | Source Synch | Input/ Output |
| A[6]# | K5 | Source Synch | Input/ Output |
| A[7]# | M1 | Source Synch | Input/ Output |
| A[8]# | N2 | Source Synch | Input/ Output |
| A[9]# | J1 | Source Synch | Input/ Output |
| A[10]# | N3 | Source Synch | Input/ Output |
| A[11]# | P5 | Source Synch | Input/ Output |
| A[12]# | P2 | Source Synch | Input/ Output |
| A[13]# | L1 | Source Synch | Input/ Output |
| A[14]# | P4 | Source Synch | Input/ Output |
| A[15]# | P1 | Source Synch | Input/ Output |
| A[16]# | R1 | Source Synch | Input/ Output |
| A[17]# | Y2 | Source Synch | Input/ Output |
| A[18]# | U5 | Source Synch | Input/ Output |
| A[19]# | R3 | Source Synch | Input/ Output |
| A[20]# | W6 | Source Synch | Input/ Output |
| A[21]# | U4 | Source Synch | Input/ Output |
| A[22]# | Y5 | Source Synch | Input/ Output |
| A[23]# | U2 | Source Synch | Input/ Output |

**Table 14. Pin Listing by Pin Name (Sheet 2 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| A[24]# | R4 | Source Synch | Input/ Output |
| A[25]# | T5 | Source Synch | Input/ Output |
| A[26]# | T3 | Source Synch | Input/ Output |
| A[27]# | W3 | Source Synch | Input/ Output |
| A[28]# | W5 | Source Synch | Input/ Output |
| A[29]# | Y4 | Source Synch | Input/ Output |
| A[30]# | W2 | Source Synch | Input/ Output |
| A[31]# | Y1 | Source Synch | Input/ Output |
| A[32]# | AA1 | Source Synch | Input/ Output |
| A[33]# | AA4 | Source Synch | Input/ Output |
| A[34]# | AB2 | Source Synch | Input/ Output |
| A[35]# | AA3 | Source Synch | Input/ Output |
| A20M# | A6 | CMOS | Input |
| ADS# | H1 | Common Clock | Input/ Output |
| ADSTB[0]# | L2 | Source Synch | Input/ Output |
| ADSTB[1]# | V4 | Source Synch | Input/ Output |
| BCLK[0] | A22 | Bus Clock | Input |
| BCLK[1] | A21 | Bus Clock | Input |
| BNR# | E2 | Common Clock | Input/ Output |
| BPM[0]# | AD4 | Common Clock | Input/ Output |
| BPM[1]# | AD3 | Common Clock | Output |
| BPM[2]# | AD1 | Common Clock | Output |
| BPM[3]# | AC4 | Common Clock | Input/ Output |

**Table 14. Pin Listing by Pin Name (Sheet 3 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| BPRI# | G5 | Common Clock | Input |
| BR0# | F1 | Common Clock | Input/ Output |
| BSEL[0] | B22 | CMOS | Output |
| BSEL[1] | B23 | CMOS | Output |
| BSEL[2] | C21 | CMOS | Output |
| COMP[0] | R26 | Power/Other | Input/ Output |
| COMP[1] | U26 | Power/Other | Input/ Output |
| COMP[2] | U1 | Power/Other | Input/ Output |
| COMP[3] | V1 | Power/Other | Input/ Output |
| D[0]# | E22 | Source Synch | Input/ Output |
| D[1]# | F24 | Source Synch | Input/ Output |
| D[2]# | E26 | Source Synch | Input/ Output |
| D[3]# | H22 | Source Synch | Input/ Output |
| D[4]# | F23 | Source Synch | Input/ Output |
| D[5]# | G25 | Source Synch | Input/ Output |
| D[6]# | E25 | Source Synch | Input/ Output |
| D[7]# | E23 | Source Synch | Input/ Output |
| D[8]# | K24 | Source Synch | Input/ Output |
| D[9]# | G24 | Source Synch | Input/ Output |
| D[10]# | J24 | Source Synch | Input/ Output |
| D[11]# | J23 | Source Synch | Input/ Output |
| D[12]# | H26 | Source Synch | Input/ Output |
| D[13]# | F26 | Source Synch | Input/ Output |

**Table 14. Pin Listing by Pin Name (Sheet 4 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| D[14]# | K22 | Source Synch | Input/ Output |
| D[15]# | H25 | Source Synch | Input/ Output |
| D[16]# | N22 | Source Synch | Input/ Output |
| D[17]# | K25 | Source Synch | Input/ Output |
| D[18]# | P26 | Source Synch | Input/ Output |
| D[19]# | R23 | Source Synch | Input/ Output |
| D[20]# | L25 | Source Synch | Input/ Output |
| D[21]# | L22 | Source Synch | Input/ Output |
| D[22]# | L23 | Source Synch | Input/ Output |
| D[23]# | M23 | Source Synch | Input/ Output |
| D[24]# | P25 | Source Synch | Input/ Output |
| D[25]# | P22 | Source Synch | Input/ Output |
| D[26]# | P23 | Source Synch | Input/ Output |
| D[27]# | T24 | Source Synch | Input/ Output |
| D[28]# | R24 | Source Synch | Input/ Output |
| D[29]# | L26 | Source Synch | Input/ Output |
| D[30]# | T25 | Source Synch | Input/ Output |
| D[31]# | N24 | Source Synch | Input/ Output |
| D[32]# | AA23 | Source Synch | Input/ Output |
| D[33]# | AB24 | Source Synch | Input/ Output |
| D[34]# | V24 | Source Synch | Input/ Output |
| D[35]# | V26 | Source Synch | Input/ Output |

**Table 14. Pin Listing by Pin Name (Sheet 5 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| D[36]# | W25 | Source Synch | Input/ Output |
| D[37]# | U23 | Source Synch | Input/ Output |
| D[38]# | U25 | Source Synch | Input/ Output |
| D[39]# | U22 | Source Synch | Input/ Output |
| D[40]# | AB25 | Source Synch | Input/ Output |
| D[41]# | W22 | Source Synch | Input/ Output |
| D[42]# | Y23 | Source Synch | Input/ Output |
| D[43]# | AA26 | Source Synch | Input/ Output |
| D[44]# | Y26 | Source Synch | Input/ Output |
| D[45]# | Y22 | Source Synch | Input/ Output |
| D[46]# | AC26 | Source Synch | Input/ Output |
| D[47]# | AA24 | Source Synch | Input/ Output |
| D[48]# | AC22 | Source Synch | Input/ Output |
| D[49]# | AC23 | Source Synch | Input/ Output |
| D[50]# | AB22 | Source Synch | Input/ Output |
| D[51]# | AA21 | Source Synch | Input/ Output |
| D[52]# | AB21 | Source Synch | Input/ Output |
| D[53]# | AC25 | Source Synch | Input/ Output |
| D[54]# | AD20 | Source Synch | Input/ Output |
| D[55]# | AE22 | Source Synch | Input/ Output |
| D[56]# | AF23 | Source Synch | Input/ Output |
| D[57]# | AD24 | Source Synch | Input/ Output |

**Table 14. Pin Listing by Pin Name (Sheet 6 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| D[58]# | AE21 | Source Synch | Input/ Output |
| D[59]# | AD21 | Source Synch | Input/ Output |
| D[60]# | AE25 | Source Synch | Input/ Output |
| D[61]# | AF25 | Source Synch | Input/ Output |
| D[62]# | AF22 | Source Synch | Input/ Output |
| D[63]# | AF26 | Source Synch | Input/ Output |
| DBR# | C20 | CMOS | Output |
| DBSY# | E1 | Common Clock | Input/ Output |
| DEFER# | H5 | Common Clock | Input |
| DINV[0]# | J26 | Source Synch | Input/ Output |
| DINV[1]# | M26 | Source Synch | Input/ Output |
| DINV[2]# | V23 | Source Synch | Input/ Output |
| DINV[3]# | AC20 | Source Synch | Input/ Output |
| DPRSTP# | E5 | CMOS | Input |
| DPSLP# | B5 | CMOS | Input |
| DPWR# | D24 | Common Clock | Input |
| DRDY# | F21 | Common Clock | Input/ Output |
| DSTBN[0]# | H23 | Source Synch | Input/ Output |
| DSTBN[1]# | M24 | Source Synch | Input/ Output |
| DSTBN[2]# | W24 | Source Synch | Input/ Output |
| DSTBN[3]# | AD23 | Source Synch | Input/ Output |
| DSTBP[0]# | G22 | Source Synch | Input/ Output |
| DSTBP[1]# | N25 | Source Synch | Input/ Output |

**Table 14. Pin Listing by Pin Name (Sheet 7 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| DSTBP[2]# | Y25 | Source Synch | Input/ Output |
| DSTBP[3]# | AE24 | Source Synch | Input/ Output |
| FERR# | A5 | Open Drain | Output |
| GTLREF | AD26 | Power/Other | Input |
| HIT# | G6 | Common Clock | Input/ Output |
| HITM# | E4 | Common Clock | Input/ Output |
| IERR# | D20 | Open Drain | Output |
| IGNNE# | C4 | CMOS | Input |
| INIT# | B3 | CMOS | Input |
| LINT0 | C6 | CMOS | Input |
| LINT1 | B4 | CMOS | Input |
| LOCK# | H4 | Common Clock | Input/ Output |
| PRDY# | AC2 | Common Clock | Output |
| PREQ# | AC1 | Common Clock | Input |
| PROCHOT# | D21 | Open Drain | Input/ Output |
| PSI# | AE6 | CMOS | Output |
| PWRGOOD | D6 | CMOS | Input |
| REQ[0]# | K3 | Source Synch | Input/ Output |
| REQ[1]# | H2 | Source Synch | Input/ Output |
| REQ[2]# | K2 | Source Synch | Input/ Output |
| REQ[3]# | J3 | Source Synch | Input/ Output |
| REQ[4]# | L5 | Source Synch | Input/ Output |
| RESET# | B1 | Common Clock | Input |
| RS[0]# | F3 | Common Clock | Input |
| RS[1]# | F4 | Common Clock | Input |

**Table 14. Pin Listing by Pin Name (Sheet 8 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| RS[2]# | G3 | Common Clock | Input |
| RSVD | B2 | Reserved | |
| RSVD | C1 | Reserved | |
| RSVD | C23 | Reserved | |
| RSVD | C24 | Reserved | |
| RSVD | C3 | Reserved | |
| RSVD | D2 | Reserved | |
| RSVD | D22 | Reserved | |
| RSVD | D3 | Reserved | |
| RSVD | F6 | Reserved | |
| RSVD | M4 | Reserved | |
| RSVD | N5 | Reserved | |
| RSVD | T2 | Reserved | |
| RSVD | T22 | Reserved | |
| RSVD | V3 | Reserved | |
| SLP# | D7 | CMOS | Input |
| SMI# | A3 | CMOS | Input |
| STPCLK# | D5 | CMOS | Input |
| TCK | AC5 | CMOS | Input |
| TDI | AA6 | CMOS | Input |
| TDO | AB3 | Open Drain | Output |
| TEST1 | C26 | Test | |
| TEST2 | D25 | Test | |
| TEST3 | AF1 | Test | |
| TEST4 | B25 | Test | |
| THERMDA | A24 | Power/Other | |
| THERMDC | A25 | Power/Other | |
| THERMTRIP# | C7 | Open Drain | Output |
| TMS | AB5 | CMOS | Input |
| TRDY# | G2 | Common Clock | Input |
| TRST# | AB6 | CMOS | Input |
| VCC | A10 | Power/Other | |
| VCC | A12 | Power/Other | |
| VCC | A13 | Power/Other | |

**Table 14. Pin Listing by Pin Name (Sheet 9 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | A15 | Power/Other | |
| VCC | A17 | Power/Other | |
| VCC | A18 | Power/Other | |
| VCC | A20 | Power/Other | |
| VCC | A7 | Power/Other | |
| VCC | A9 | Power/Other | |
| VCC | AA10 | Power/Other | |
| VCC | AA12 | Power/Other | |
| VCC | AA13 | Power/Other | |
| VCC | AA15 | Power/Other | |
| VCC | AA17 | Power/Other | |
| VCC | AA18 | Power/Other | |
| VCC | AA20 | Power/Other | |
| VCC | AA7 | Power/Other | |
| VCC | AA9 | Power/Other | |
| VCC | AB10 | Power/Other | |
| VCC | AB12 | Power/Other | |
| VCC | AB14 | Power/Other | |
| VCC | AB15 | Power/Other | |
| VCC | AB17 | Power/Other | |
| VCC | AB18 | Power/Other | |
| VCC | AB20 | Power/Other | |
| VCC | AB7 | Power/Other | |
| VCC | AB9 | Power/Other | |
| VCC | AC10 | Power/Other | |
| VCC | AC12 | Power/Other | |
| VCC | AC13 | Power/Other | |
| VCC | AC15 | Power/Other | |
| VCC | AC17 | Power/Other | |
| VCC | AC18 | Power/Other | |
| VCC | AC7 | Power/Other | |
| VCC | AC9 | Power/Other | |
| VCC | AD10 | Power/Other | |
| VCC | AD12 | Power/Other | |
| VCC | AD14 | Power/Other | |
| VCC | AD15 | Power/Other | |

**Table 14. Pin Listing by Pin Name (Sheet 10 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | AD17 | Power/Other | |
| VCC | AD18 | Power/Other | |
| VCC | AD7 | Power/Other | |
| VCC | AD9 | Power/Other | |
| VCC | AE10 | Power/Other | |
| VCC | AE12 | Power/Other | |
| VCC | AE13 | Power/Other | |
| VCC | AE15 | Power/Other | |
| VCC | AE17 | Power/Other | |
| VCC | AE18 | Power/Other | |
| VCC | AE20 | Power/Other | |
| VCC | AE9 | Power/Other | |
| VCC | AF10 | Power/Other | |
| VCC | AF12 | Power/Other | |
| VCC | AF14 | Power/Other | |
| VCC | AF15 | Power/Other | |
| VCC | AF17 | Power/Other | |
| VCC | AF18 | Power/Other | |
| VCC | AF20 | Power/Other | |
| VCC | AF9 | Power/Other | |
| VCC | B10 | Power/Other | |
| VCC | B12 | Power/Other | |
| VCC | B14 | Power/Other | |
| VCC | B15 | Power/Other | |
| VCC | B17 | Power/Other | |
| VCC | B18 | Power/Other | |
| VCC | B20 | Power/Other | |
| VCC | B7 | Power/Other | |
| VCC | B9 | Power/Other | |
| VCC | C10 | Power/Other | |
| VCC | C12 | Power/Other | |
| VCC | C13 | Power/Other | |
| VCC | C15 | Power/Other | |
| VCC | C17 | Power/Other | |
| VCC | C18 | Power/Other | |
| VCC | C9 | Power/Other | |

**Table 14. Pin Listing by Pin Name (Sheet 11 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | D10 | Power/Other | |
| VCC | D12 | Power/Other | |
| VCC | D14 | Power/Other | |
| VCC | D15 | Power/Other | |
| VCC | D17 | Power/Other | |
| VCC | D18 | Power/Other | |
| VCC | D9 | Power/Other | |
| VCC | E10 | Power/Other | |
| VCC | E12 | Power/Other | |
| VCC | E13 | Power/Other | |
| VCC | E15 | Power/Other | |
| VCC | E17 | Power/Other | |
| VCC | E18 | Power/Other | |
| VCC | E20 | Power/Other | |
| VCC | E7 | Power/Other | |
| VCC | E9 | Power/Other | |
| VCC | F10 | Power/Other | |
| VCC | F12 | Power/Other | |
| VCC | F14 | Power/Other | |
| VCC | F15 | Power/Other | |
| VCC | F17 | Power/Other | |
| VCC | F18 | Power/Other | |
| VCC | F20 | Power/Other | |
| VCC | F7 | Power/Other | |
| VCC | F9 | Power/Other | |
| VCCA | B26 | Power/Other | |
| VCCP | G21 | Power/Other | |
| VCCP | J21 | Power/Other | |
| VCCP | J6 | Power/Other | |
| VCCP | K21 | Power/Other | |
| VCCP | K6 | Power/Other | |
| VCCP | M21 | Power/Other | |
| VCCP | M6 | Power/Other | |
| VCCP | N21 | Power/Other | |
| VCCP | N6 | Power/Other | |
| VCCP | R21 | Power/Other | |

**Table 14. Pin Listing by Pin Name (Sheet 12 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VCCP | R6 | Power/Other | |
| VCCP | T21 | Power/Other | |
| VCCP | T6 | Power/Other | |
| VCCP | V21 | Power/Other | |
| VCCP | V6 | Power/Other | |
| VCCP | W21 | Power/Other | |
| VCCSENSE | AF7 | Power/Other | |
| VID[0] | AD6 | CMOS | Output |
| VID[1] | AF5 | CMOS | Output |
| VID[2] | AE5 | CMOS | Output |
| VID[3] | AF4 | CMOS | Output |
| VID[4] | AE3 | CMOS | Output |
| VID[5] | AF2 | CMOS | Output |
| VID[6] | AE2 | CMOS | Output |
| VSS | A11 | Power/Other | |
| VSS | A14 | Power/Other | |
| VSS | A16 | Power/Other | |
| VSS | A19 | Power/Other | |
| VSS | A23 | Power/Other | |
| VSS | A26 | Power/Other | |
| VSS | A4 | Power/Other | |
| VSS | A8 | Power/Other | |
| VSS | AA11 | Power/Other | |
| VSS | AA14 | Power/Other | |
| VSS | AA16 | Power/Other | |
| VSS | AA19 | Power/Other | |
| VSS | AA2 | Power/Other | |
| VSS | AA22 | Power/Other | |
| VSS | AA25 | Power/Other | |
| VSS | AA5 | Power/Other | |
| VSS | AA8 | Power/Other | |
| VSS | AB1 | Power/Other | |
| VSS | AB11 | Power/Other | |
| VSS | AB13 | Power/Other | |
| VSS | AB16 | Power/Other | |
| VSS | AB19 | Power/Other | |

**Table 14. Pin Listing by Pin Name (Sheet 13 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | AB23 | Power/Other | |
| VSS | AB26 | Power/Other | |
| VSS | AB4 | Power/Other | |
| VSS | AB8 | Power/Other | |
| VSS | AC11 | Power/Other | |
| VSS | AC14 | Power/Other | |
| VSS | AC16 | Power/Other | |
| VSS | AC19 | Power/Other | |
| VSS | AC21 | Power/Other | |
| VSS | AC24 | Power/Other | |
| VSS | AC3 | Power/Other | |
| VSS | AC6 | Power/Other | |
| VSS | AC8 | Power/Other | |
| VSS | AD11 | Power/Other | |
| VSS | AD13 | Power/Other | |
| VSS | AD16 | Power/Other | |
| VSS | AD19 | Power/Other | |
| VSS | AD2 | Power/Other | |
| VSS | AD22 | Power/Other | |
| VSS | AD25 | Power/Other | |
| VSS | AD5 | Power/Other | |
| VSS | AD8 | Power/Other | |
| VSS | AE1 | Power/Other | |
| VSS | AE11 | Power/Other | |
| VSS | AE14 | Power/Other | |
| VSS | AE16 | Power/Other | |
| VSS | AE19 | Power/Other | |
| VSS | AE23 | Power/Other | |
| VSS | AE26 | Power/Other | |
| VSS | AE4 | Power/Other | |
| VSS | AE8 | Power/Other | |
| VSS | AF11 | Power/Other | |
| VSS | AF13 | Power/Other | |
| VSS | AF16 | Power/Other | |
| VSS | AF19 | Power/Other | |
| VSS | AF21 | Power/Other | |

**Table 14. Pin Listing by Pin Name (Sheet 14 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | AF24 | Power/Other | |
| VSS | AF3 | Power/Other | |
| VSS | AF6 | Power/Other | |
| VSS | AF8 | Power/Other | |
| VSS | B11 | Power/Other | |
| VSS | B13 | Power/Other | |
| VSS | B16 | Power/Other | |
| VSS | B19 | Power/Other | |
| VSS | B21 | Power/Other | |
| VSS | B24 | Power/Other | |
| VSS | B6 | Power/Other | |
| VSS | B8 | Power/Other | |
| VSS | C11 | Power/Other | |
| VSS | C14 | Power/Other | |
| VSS | C16 | Power/Other | |
| VSS | C19 | Power/Other | |
| VSS | C2 | Power/Other | |
| VSS | C22 | Power/Other | |
| VSS | C25 | Power/Other | |
| VSS | C5 | Power/Other | |
| VSS | C8 | Power/Other | |
| VSS | D1 | Power/Other | |
| VSS | D11 | Power/Other | |
| VSS | D13 | Power/Other | |
| VSS | D16 | Power/Other | |
| VSS | D19 | Power/Other | |
| VSS | D23 | Power/Other | |
| VSS | D26 | Power/Other | |
| VSS | D4 | Power/Other | |
| VSS | D8 | Power/Other | |
| VSS | E11 | Power/Other | |
| VSS | E14 | Power/Other | |
| VSS | E16 | Power/Other | |
| VSS | E19 | Power/Other | |
| VSS | E21 | Power/Other | |
| VSS | E24 | Power/Other | |

**Table 14. Pin Listing by Pin Name (Sheet 15 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | E3 | Power/Other | |
| VSS | E6 | Power/Other | |
| VSS | E8 | Power/Other | |
| VSS | F11 | Power/Other | |
| VSS | F13 | Power/Other | |
| VSS | F16 | Power/Other | |
| VSS | F19 | Power/Other | |
| VSS | F2 | Power/Other | |
| VSS | F22 | Power/Other | |
| VSS | F25 | Power/Other | |
| VSS | F5 | Power/Other | |
| VSS | F8 | Power/Other | |
| VSS | G1 | Power/Other | |
| VSS | G23 | Power/Other | |
| VSS | G26 | Power/Other | |
| VSS | G4 | Power/Other | |
| VSS | H21 | Power/Other | |
| VSS | H24 | Power/Other | |
| VSS | H3 | Power/Other | |
| VSS | H6 | Power/Other | |
| VSS | J2 | Power/Other | |
| VSS | J22 | Power/Other | |
| VSS | J25 | Power/Other | |
| VSS | J5 | Power/Other | |
| VSS | K1 | Power/Other | |
| VSS | K23 | Power/Other | |
| VSS | K26 | Power/Other | |
| VSS | K4 | Power/Other | |
| VSS | L21 | Power/Other | |
| VSS | L24 | Power/Other | |
| VSS | L3 | Power/Other | |
| VSS | L6 | Power/Other | |
| VSS | M2 | Power/Other | |
| VSS | M22 | Power/Other | |
| VSS | M25 | Power/Other | |
| VSS | M5 | Power/Other | |

**Table 14. Pin Listing by Pin Name (Sheet 16 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | N1 | Power/Other | |
| VSS | N23 | Power/Other | |
| VSS | N26 | Power/Other | |
| VSS | N4 | Power/Other | |
| VSS | P21 | Power/Other | |
| VSS | P24 | Power/Other | |
| VSS | P3 | Power/Other | |
| VSS | P6 | Power/Other | |
| VSS | R2 | Power/Other | |
| VSS | R22 | Power/Other | |
| VSS | R25 | Power/Other | |
| VSS | R5 | Power/Other | |
| VSS | T1 | Power/Other | |
| VSS | T23 | Power/Other | |
| VSS | T26 | Power/Other | |
| VSS | T4 | Power/Other | |
| VSS | U21 | Power/Other | |
| VSS | U24 | Power/Other | |
| VSS | U3 | Power/Other | |
| VSS | U6 | Power/Other | |
| VSS | V2 | Power/Other | |
| VSS | V22 | Power/Other | |
| VSS | V25 | Power/Other | |
| VSS | V5 | Power/Other | |
| VSS | W1 | Power/Other | |
| VSS | W23 | Power/Other | |
| VSS | W26 | Power/Other | |
| VSS | W4 | Power/Other | |
| VSS | Y21 | Power/Other | |
| VSS | Y24 | Power/Other | |
| VSS | Y3 | Power/Other | |
| VSS | Y6 | Power/Other | |
| VSSSENSE | AE7 | Power/Other | Output |

**Table 15. Pin Listing by Pin Number (Sheet 1 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| SMI# | A03 | CMOS | Input |
| VSS | A04 | Power/Other | |
| FERR# | A05 | Open Drain | Output |
| A20M# | A06 | CMOS | Input |
| VCC | A07 | Power/Other | |
| VSS | A08 | Power/Other | |
| VCC | A09 | Power/Other | |
| VCC | A10 | Power/Other | |
| VSS | A11 | Power/Other | |
| VCC | A12 | Power/Other | |
| VCC | A13 | Power/Other | |
| VSS | A14 | Power/Other | |
| VCC | A15 | Power/Other | |
| VSS | A16 | Power/Other | |
| VCC | A17 | Power/Other | |
| VCC | A18 | Power/Other | |
| VSS | A19 | Power/Other | |
| VCC | A20 | Power/Other | |
| BCLK[1] | A21 | Bus Clock | Input |
| BCLK[0] | A22 | Bus Clock | Input |
| VSS | A23 | Power/Other | |
| THERMDA | A24 | Power/Other | |
| THERMDC | A25 | Power/Other | |
| VSS | A26 | Power/Other | |
| A[32]# | AA01 | Source Synch | Input/ Output |
| VSS | AA02 | Power/Other | |
| A[35]# | AA03 | Source Synch | Input/ Output |
| A[33]# | AA04 | Source Synch | Input/ Output |
| VSS | AA05 | Power/Other | |
| TDI | AA06 | CMOS | Input |
| VCC | AA07 | Power/Other | |
| VSS | AA08 | Power/other | |
| VCC | AA09 | Power/Other | |

**Table 15. Pin Listing by Pin Number (Sheet 2 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | AA10 | Power/Other | |
| VSS | AA11 | Power/Other | |
| VCC | AA12 | Power/Other | |
| VCC | AA13 | Power/Other | |
| VSS | AA14 | Power/Other | |
| VCC | AA15 | Power/Other | |
| VSS | AA16 | Power/Other | |
| VCC | AA17 | Power/Other | |
| VCC | AA18 | Power/Other | |
| VSS | AA19 | Power/Other | |
| VCC | AA20 | Power/Other | |
| D[51]# | AA21 | Source Synch | Input/ Output |
| VSS | AA22 | Power/Other | |
| D[32]# | AA23 | Source Synch | Input/ Output |
| D[47]# | AA24 | Source Synch | Input/ Output |
| VSS | AA25 | Power/Other | |
| D[43]# | AA26 | Source Synch | Input/ Output |
| VSS | AB01 | Power/Other | |
| A[34]# | AB02 | Source Synch | Input/ Output |
| TDO | AB03 | Open Drain | Output |
| VSS | AB04 | Power/Other | |
| TMS | AB05 | CMOS | Input |
| TRST# | AB06 | CMOS | Input |
| VCC | AB07 | Power/Other | |
| VSS | AB08 | Power/Other | |
| VCC | AB09 | Power/Other | |
| VCC | AB10 | Power/Other | |
| VSS | AB11 | Power/Other | |
| VCC | AB12 | Power/Other | |
| VSS | AB13 | Power/Other | |
| VCC | AB14 | Power/Other | |
| VCC | AB15 | Power/Other | |
| VSS | AB16 | Power/Other | |

**Table 15. Pin Listing by Pin Number (Sheet 3 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | AB17 | Power/Other | |
| VCC | AB18 | Power/Other | |
| VSS | AB19 | Power/Other | |
| VCC | AB20 | Power/Other | |
| D[52]# | AB21 | Source Synch | Input/ Output |
| D[50]# | AB22 | Source Synch | Input/ Output |
| VSS | AB23 | Power/Other | |
| D[33]# | AB24 | Source Synch | Input/ Output |
| D[40]# | AB25 | Source Synch | Input/ Output |
| VSS | AB26 | Power/Other | |
| PREQ# | AC01 | Common Clock | Input |
| PRDY# | AC02 | Common Clock | Output |
| VSS | AC03 | Power/Other | |
| BPM[3]# | AC04 | Common Clock | Input/ Output |
| TCK | AC05 | CMOS | Input |
| VSS | AC06 | Power/Other | |
| VCC | AC07 | Power/Other | |
| VSS | AC08 | Power/Other | |
| VCC | AC09 | Power/Other | |
| VCC | AC10 | Power/Other | |
| VSS | AC11 | Power/Other | |
| VCC | AC12 | Power/Other | |
| VCC | AC13 | Power/Other | |
| VSS | AC14 | Power/Other | |
| VCC | AC15 | Power/Other | |
| VSS | AC16 | Power/Other | |
| VCC | AC17 | Power/Other | |
| VCC | AC18 | Power/Other | |
| VSS | AC19 | Power/Other | |
| DINV[3]# | AC20 | Source Synch | Input/ Output |
| VSS | AC21 | Power/Other | |

**Table 15. Pin Listing by Pin Number (Sheet 4 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| D[48]# | AC22 | Source Synch | Input/ Output |
| D[49]# | AC23 | Source Synch | Input/ Output |
| VSS | AC24 | Power/Other | |
| D[53]# | AC25 | Source Synch | Input/ Output |
| D[46]# | AC26 | Source Synch | Input/ Output |
| BPM[2]# | AD01 | Common Clock | Output |
| VSS | AD02 | Power/Other | |
| BPM[1]# | AD03 | Common Clock | Output |
| BPM[0]# | AD04 | Common Clock | Input/ Output |
| VSS | AD05 | Power/Other | |
| VID[0] | AD06 | CMOS | Output |
| VCC | AD07 | Power/Other | |
| VSS | AD08 | Power/Other | |
| VCC | AD09 | Power/Other | |
| VCC | AD10 | Power/Other | |
| VSS | AD11 | Power/Other | |
| VCC | AD12 | Power/Other | |
| VSS | AD13 | Power/Other | |
| VCC | AD14 | Power/Other | |
| VCC | AD15 | Power/Other | |
| VSS | AD16 | Power/Other | |
| VCC | AD17 | Power/Other | |
| VCC | AD18 | Power/Other | |
| VSS | AD19 | Power/Other | |
| D[54]# | AD20 | Source Synch | Input/ Output |
| D[59]# | AD21 | Source Synch | Input/ Output |
| VSS | AD22 | Power/Other | |
| DSTBN[3]# | AD23 | Source Synch | Input/ Output |
| D[57]# | AD24 | Source Synch | Input/ Output |

**Table 15. Pin Listing by Pin Number (Sheet 5 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | AD25 | Power/Other | |
| GTLREF | AD26 | Power/Other | Input |
| VSS | AE01 | Power/Other | |
| VID[6] | AE02 | CMOS | Output |
| VID[4] | AE03 | CMOS | Output |
| VSS | AE04 | Power/Other | |
| VID[2] | AE05 | CMOS | Output |
| PSI# | AE06 | CMOS | Output |
| VSSSENSE | AE07 | Power/Other | Output |
| VSS | AE08 | Power/Other | |
| VCC | AE09 | Power/Other | |
| VCC | AE10 | Power/Other | |
| VSS | AE11 | Power/Other | |
| VCC | AE12 | Power/Other | |
| VCC | AE13 | Power/Other | |
| VSS | AE14 | Power/Other | |
| VCC | AE15 | Power/Other | |
| VSS | AE16 | Power/Other | |
| VCC | AE17 | Power/Other | |
| VCC | AE18 | Power/Other | |
| VSS | AE19 | Power/Other | |
| VCC | AE20 | Power/Other | |
| D[58]# | AE21 | Source Synch | Input/ Output |
| D[55]# | AE22 | Source Synch | Input/ Output |
| VSS | AE23 | Power/Other | |
| DSTBP[3]# | AE24 | Source Synch | Input/ Output |
| D[60]# | AE25 | Source Synch | Input/ Output |
| VSS | AE26 | Power/Other | |
| TEST3 | AF01 | Test | |
| VID[5] | AF02 | CMOS | Output |
| VSS | AF03 | Power/Other | |
| VID[3] | AF04 | CMOS | Output |
| VID[1] | AF05 | CMOS | Output |
| VSS | AF06 | Power/Other | |

**Table 15. Pin Listing by Pin Number (Sheet 6 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VCCSENSE | AF07 | Power/Other | |
| VSS | AF08 | Power/Other | |
| VCC | AF09 | Power/Other | |
| VCC | AF10 | Power/Other | |
| VSS | AF11 | Power/Other | |
| VCC | AF12 | Power/Other | |
| VSS | AF13 | Power/Other | |
| VCC | AF14 | Power/Other | |
| VCC | AF15 | Power/Other | |
| VSS | AF16 | Power/Other | |
| VCC | AF17 | Power/Other | |
| VCC | AF18 | Power/Other | |
| VSS | AF19 | Power/Other | |
| VCC | AF20 | Power/Other | |
| VSS | AF21 | Power/Other | |
| D[62]# | AF22 | Source Synch | Input/ Output |
| D[56]# | AF23 | Source Synch | Input/ Output |
| VSS | AF24 | Power/Other | |
| D[61]# | AF25 | Source Synch | Input/ Output |
| D[63]# | AF26 | Source Synch | Input/ Output |
| RESET# | B01 | Common Clock | Input |
| RSVD | B02 | Reserved | |
| INIT# | B03 | CMOS | Input |
| LINT1 | B04 | CMOS | Input |
| DPSLP# | B05 | CMOS | Input |
| VSS | B06 | Power/Other | |
| VCC | B07 | Power/Other | |
| VSS | B08 | Power/Other | |
| VCC | B09 | Power/Other | |
| VCC | B10 | Power/Other | |
| VSS | B11 | Power/Other | |
| VCC | B12 | Power/Other | |
| VSS | B13 | Power/Other | |

**Table 15. Pin Listing by Pin Number (Sheet 7 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | B14 | Power/Other | |
| VCC | B15 | Power/Other | |
| VSS | B16 | Power/Other | |
| VCC | B17 | Power/Other | |
| VCC | B18 | Power/Other | |
| VSS | B19 | Power/Other | |
| VCC | B20 | Power/Other | |
| VSS | B21 | Power/Other | |
| BSEL[0] | B22 | CMOS | Output |
| BSEL[1] | B23 | CMOS | Output |
| VSS | B24 | Power/Other | |
| TEST4 | B25 | Test | |
| VCCA | B26 | Power/Other | |
| RSVD | C01 | Reserved | |
| VSS | C02 | Power/Other | |
| RSVD | C03 | Reserved | |
| IGNNE# | C04 | CMOS | Input |
| VSS | C05 | Power/Other | |
| LINT0 | C06 | CMOS | Input |
| THERMTRIP # | C07 | Open Drain | Output |
| VSS | C08 | Power/Other | |
| VCC | C09 | Power/Other | |
| VCC | C10 | Power/Other | |
| VSS | C11 | Power/Other | |
| VCC | C12 | Power/Other | |
| VCC | C13 | Power/Other | |
| VSS | C14 | Power/Other | |
| VCC | C15 | Power/Other | |
| VSS | C16 | Power/Other | |
| VCC | C17 | Power/Other | |
| VCC | C18 | Power/Other | |
| VSS | C19 | Power/Other | |
| DBR# | C20 | CMOS | Output |
| BSEL[2] | C21 | CMOS | Output |
| VSS | C22 | Power/Other | |
| RSVD | C23 | Reserved | |

**Table 15. Pin Listing by Pin Number (Sheet 8 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| RSVD | C24 | Reserved | |
| VSS | C25 | Power/Other | |
| TEST1 | C26 | Test | |
| VSS | D01 | Power/Other | |
| RSVD | D02 | Reserved | |
| RSVD | D03 | Reserved | |
| VSS | D04 | Power/Other | |
| STPCLK# | D05 | CMOS | Input |
| PWRGOOD | D06 | CMOS | Input |
| SLP# | D07 | CMOS | Input |
| VSS | D08 | Power/Other | |
| VCC | D09 | Power/Other | |
| VCC | D10 | Power/Other | |
| VSS | D11 | Power/Other | |
| VCC | D12 | Power/Other | |
| VSS | D13 | Power/Other | |
| VCC | D14 | Power/Other | |
| VCC | D15 | Power/Other | |
| VSS | D16 | Power/Other | |
| VCC | D17 | Power/Other | |
| VCC | D18 | Power/Other | |
| VSS | D19 | Power/Other | |
| IERR# | D20 | Open Drain | Output |
| PROCHOT# | D21 | Open Drain | Input/ Output |
| RSVD | D22 | Reserved | |
| VSS | D23 | Power/Other | |
| DPWR# | D24 | Common Clock | Input |
| TEST2 | D25 | Test | |
| VSS | D26 | Power/Other | |
| DBSY# | E01 | Common Clock | Input/ Output |
| BNR# | E02 | Common Clock | Input/ Output |
| VSS | E03 | Power/Other | |
| HITM# | E04 | Common Clock | Input/ Output |

**Table 15. Pin Listing by Pin Number (Sheet 9 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| DPRSTP# | E05 | CMOS | Input |
| VSS | E06 | Power/Other | |
| VCC | E07 | Power/Other | |
| VSS | E08 | Power/Other | |
| VCC | E09 | Power/Other | |
| VCC | E10 | Power/Other | |
| VSS | E11 | Power/Other | |
| VCC | E12 | Power/Other | |
| VCC | E13 | Power/Other | |
| VSS | E14 | Power/Other | |
| VCC | E15 | Power/Other | |
| VSS | E16 | Power/Other | |
| VCC | E17 | Power/Other | |
| VCC | E18 | Power/Other | |
| VSS | E19 | Power/Other | |
| VCC | E20 | Power/Other | |
| VSS | E21 | Power/Other | |
| D[0]# | E22 | Source Synch | Input/ Output |
| D[7]# | E23 | Source Synch | Input/ Output |
| VSS | E24 | Power/Other | |
| D[6]# | E25 | Source Synch | Input/ Output |
| D[2]# | E26 | Source Synch | Input/ Output |
| BR0# | F01 | Common Clock | Input/ Output |
| VSS | F02 | Power/Other | |
| RS[0]# | F03 | Common Clock | Input |
| RS[1]# | F04 | Common Clock | Input |
| VSS | F05 | Power/Other | |
| RSVD | F06 | Reserved | |
| VCC | F07 | Power/Other | |
| VSS | F08 | Power/Other | |
| VCC | F09 | Power/Other | |
| VCC | F10 | Power/Other | |

**Table 15. Pin Listing by Pin Number (Sheet 10 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | F11 | Power/Other | |
| VCC | F12 | Power/Other | |
| VSS | F13 | Power/Other | |
| VCC | F14 | Power/Other | |
| VCC | F15 | Power/Other | |
| VSS | F16 | Power/Other | |
| VCC | F17 | Power/Other | |
| VCC | F18 | Power/Other | |
| VSS | F19 | Power/Other | |
| VCC | F20 | Power/Other | |
| DRDY# | F21 | Common Clock | Input/ Output |
| VSS | F22 | Power/Other | |
| D[4]# | F23 | Source Synch | Input/ Output |
| D[1]# | F24 | Source Synch | Input/ Output |
| VSS | F25 | Power/Other | |
| D[13]# | F26 | Source Synch | Input/ Output |
| VSS | G01 | Power/Other | |
| TRDY# | G02 | Common Clock | Input |
| RS[2]# | G03 | Common Clock | Input |
| VSS | G04 | Power/Other | |
| BPRI# | G05 | Common Clock | Input |
| HIT# | G06 | Common Clock | Input/ Output |
| VCCP | G21 | Power/Other | |
| DSTBP[0]# | G22 | Source Synch | Input/ Output |
| VSS | G23 | Power/Other | |
| D[9]# | G24 | Source Synch | Input/ Output |
| D[5]# | G25 | Source Synch | Input/ Output |
| VSS | G26 | Power/Other | |

**Table 15. Pin Listing by Pin Number (Sheet 11 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| ADS# | H01 | Common Clock | Input/ Output |
| REQ[1]# | H02 | Source Synch | Input/ Output |
| VSS | H03 | Power/Other | |
| LOCK# | H04 | Common Clock | Input/ Output |
| DEFER# | H05 | Common Clock | Input |
| VSS | H06 | Power/Other | |
| VSS | H21 | Power/Other | |
| D[3]# | H22 | Source Synch | Input/ Output |
| DSTBN[0]# | H23 | Source Synch | Input/ Output |
| VSS | H24 | Power/Other | |
| D[15]# | H25 | Source Synch | Input/ Output |
| D[12]# | H26 | Source Synch | Input/ Output |
| A[9]# | J01 | Source Synch | Input/ Output |
| VSS | J02 | Power/Other | |
| REQ[3]# | J03 | Source Synch | Input/ Output |
| A[3]# | J04 | Source Synch | Input/ Output |
| VSS | J05 | Power/Other | |
| VCCP | J06 | Power/Other | |
| VCCP | J21 | Power/Other | |
| VSS | J22 | Power/Other | |
| D[11]# | J23 | Source Synch | Input/ Output |
| D[10]# | J24 | Source Synch | Input/ Output |
| VSS | J25 | Power/Other | |
| DINV[0]# | J26 | Source Synch | Input/ Output |
| VSS | K01 | Power/Other | |
| REQ[2]# | K02 | Source Synch | Input/ Output |

**Table 15. Pin Listing by Pin Number (Sheet 12 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| REQ[0]# | K03 | Source Synch | Input/ Output |
| VSS | K04 | Power/Other | |
| A[6]# | K05 | Source Synch | Input/ Output |
| VCCP | K06 | Power/Other | |
| VCCP | K21 | Power/Other | |
| D[14]# | K22 | Source Synch | Input/ Output |
| VSS | K23 | Power/Other | |
| D[8]# | K24 | Source Synch | Input/ Output |
| D[17]# | K25 | Source Synch | Input/ Output |
| VSS | K26 | Power/Other | |
| A[13]# | L01 | Source Synch | Input/ Output |
| ADSTB[0]# | L02 | Source Synch | Input/ Output |
| VSS | L03 | Power/Other | |
| A[4]# | L04 | Source Synch | Input/ Output |
| REQ[4]# | L05 | Source Synch | Input/ Output |
| VSS | L06 | Power/Other | |
| VSS | L21 | Power/Other | |
| D[21]# | L22 | Source Synch | Input/ Output |
| D[22]# | L23 | Source Synch | Input/ Output |
| VSS | L24 | Power/Other | |
| D[20]# | L25 | Source Synch | Input/ Output |
| D[29]# | L26 | Source Synch | Input/ Output |
| A[7]# | M01 | Source Synch | Input/ Output |
| VSS | M02 | Power/Other | |
| A[5]# | M03 | Source Synch | Input/ Output |
| RSVD | M04 | Reserved | |

**Table 15. Pin Listing by Pin Number (Sheet 13 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | M05 | Power/Other | |
| VCCP | M06 | Power/Other | |
| VCCP | M21 | Power/Other | |
| VSS | M22 | Power/Other | |
| D[23]# | M23 | Source Synch | Input/ Output |
| DSTBN[1]# | M24 | Source Synch | Input/ Output |
| VSS | M25 | Power/Other | |
| DINV[1]# | M26 | Source Synch | Input/ Output |
| VSS | N01 | Power/Other | |
| A[8]# | N02 | Source Synch | Input/ Output |
| A[10]# | N03 | Source Synch | Input/ Output |
| VSS | N04 | Power/Other | |
| RSVD | N05 | Reserved | |
| VCCP | N06 | Power/Other | |
| VCCP | N21 | Power/Other | |
| D[16]# | N22 | Source Synch | Input/ Output |
| VSS | N23 | Power/Other | |
| D[31]# | N24 | Source Synch | Input/ Output |
| DSTBP[1]# | N25 | Source Synch | Input/ Output |
| VSS | N26 | Power/Other | |
| A[15]# | P01 | Source Synch | Input/ Output |
| A[12]# | P02 | Source Synch | Input/ Output |
| VSS | P03 | Power/Other | |
| A[14]# | P04 | Source Synch | Input/ Output |
| A[11]# | P05 | Source Synch | Input/ Output |
| VSS | P06 | Power/Other | |
| VSS | P21 | Power/Other | |
| D[25]# | P22 | Source Synch | Input/ Output |

**Table 15. Pin Listing by Pin Number (Sheet 14 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| D[26]# | P23 | Source Synch | Input/ Output |
| VSS | P24 | Power/Other | |
| D[24]# | P25 | Source Synch | Input/ Output |
| D[18]# | P26 | Source Synch | Input/ Output |
| A[16]# | R01 | Source Synch | Input/ Output |
| VSS | R02 | Power/Other | |
| A[19]# | R03 | Source Synch | Input/ Output |
| A[24]# | R04 | Source Synch | Input/ Output |
| VSS | R05 | Power/Other | |
| VCCP | R06 | Power/Other | |
| VCCP | R21 | Power/Other | |
| VSS | R22 | Power/Other | |
| D[19]# | R23 | Source Synch | Input/ Output |
| D[28]# | R24 | Source Synch | Input/ Output |
| VSS | R25 | Power/Other | |
| COMP[0] | R26 | Power/Other | Input/ Output |
| VSS | T01 | Power/Other | |
| RSVD | T02 | Reserved | |
| A[26]# | T03 | Source Synch | Input/ Output |
| VSS | T04 | Power/Other | |
| A[25]# | T05 | Source Synch | Input/ Output |
| VCCP | T06 | Power/Other | |
| VCCP | T21 | Power/Other | |
| RSVD | T22 | Reserved | |
| VSS | T23 | Power/Other | |
| D[27]# | T24 | Source Synch | Input/ Output |
| D[30]# | T25 | Source Synch | Input/ Output |
| VSS | T26 | Power/Other | |

**Table 15. Pin Listing by Pin Number (Sheet 15 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| COMP[2] | U01 | Power/Other | Input/ Output |
| A[23]# | U02 | Source Synch | Input/ Output |
| VSS | U03 | Power/Other | |
| A[21]# | U04 | Source Synch | Input/ Output |
| A[18]# | U05 | Source Synch | Input/ Output |
| VSS | U06 | Power/Other | |
| VSS | U21 | Power/Other | |
| D[39]# | U22 | Source Synch | Input/ Output |
| D[37]# | U23 | Source Synch | Input/ Output |
| VSS | U24 | Power/Other | |
| D[38]# | U25 | Source Synch | Input/ Output |
| COMP[1] | U26 | Power/Other | Input/ Output |
| COMP[3] | V01 | Power/Other | Input/ Output |
| VSS | V02 | Power/Other | |
| RSVD | V03 | Reserved | |
| ADSTB[1]# | V04 | Source Synch | Input/ Output |
| VSS | V05 | Power/Other | |
| VCCP | V06 | Power/Other | |
| VCCP | V21 | Power/Other | |
| VSS | V22 | Power/Other | |
| DINV[2]# | V23 | Source Synch | Input/ Output |
| D[34]# | V24 | Source Synch | Input/ Output |
| VSS | V25 | Power/Other | |
| D[35]# | V26 | Source Synch | Input/ Output |
| VSS | W01 | Power/Other | |
| A[30]# | W02 | Source Synch | Input/ Output |

**Table 15. Pin Listing by Pin Number (Sheet 16 of 16)**

| Pin Name | Pin Number | Signal Buffer Type | Direction |
|---|---|---|---|
| A[27]# | W03 | Source Synch | Input/ Output |
| VSS | W04 | Power/Other | |
| A[28]# | W05 | Source Synch | Input/ Output |
| A[20]# | W06 | Source Synch | Input/ Output |
| VCCP | W21 | Power/Other | |
| D[41]# | W22 | Source Synch | Input/ Output |
| VSS | W23 | Power/Other | |
| DSTBN[2]# | W24 | Source Synch | Input/ Output |
| D[36]# | W25 | Source Synch | Input/ Output |
| VSS | W26 | Power/Other | |
| A[31]# | Y01 | Source Synch | Input/ Output |
| A[17]# | Y02 | Source Synch | Input/ Output |
| VSS | Y03 | Power/Other | |
| A[29]# | Y04 | Source Synch | Input/ Output |
| A[22]# | Y05 | Source Synch | Input/ Output |
| VSS | Y06 | Power/Other | |
| VSS | Y21 | Power/Other | |
| D[45]# | Y22 | Source Synch | Input/ Output |
| D[42]# | Y23 | Source Synch | Input/ Output |
| VSS | Y24 | Power/Other | |
| DSTBP[2]# | Y25 | Source Synch | Input/ Output |
| D[44]# | Y26 | Source Synch | Input/ Output |

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## 4.3 Alphabetical Signals Reference

**Table 16. Signal Description (Sheet 1 of 9)**

| Name | Type | Description |
|---|---|---|
| A[35:3]# | Input/ Output | A[35:3]# (Address) define a $2^{36}$-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Celeron® M processor FSB. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.<br>**NOTE: When paired with a chipset limited to 32-bit addressing, A[35:32] should remain unconnected** |
| A20M# | Input | If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.<br>A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/ Output Write bus transaction. |
| ADS# | Input/ Output | ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. |
| ADSTB[1:0]# | Input/ Output | Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.<br>**Signals** / **Associated Strobe**<br>REQ[4:0]#, A[16:3]# / ADSTB[0]#<br>A[35:17]# / ADSTB[1]# |
| BCLK[1:0] | Input | The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs.<br>All external timing parameters are specified with respect to the rising edge of BCLK0 crossing $V_{CROSS}$. |
| BNR# | Input/ Output | BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. |

**Table 16. Signal Description (Sheet 2 of 9)**

| Name | Type | Description |
|---|---|---|
| BPM[2:1]#<br><br>BPM[3,0]# | Output<br><br>Input/ Output | BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Celeron M processor FSB agents. This includes debug or performance monitoring tools.<br>Please refer to the platform design guide for more detailed information. |
| BPRI# | Input | BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#. |
| BR0# | Input/ Output | BR0# is used by the processor to request the bus. The arbitration is done between the Celeron M processor (Symmetric Agent) and GMCH-M (High Priority Agent). |
| BSEL[2:0] | Output | BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. Table 3 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The Celeron M processor 500 series operates at a 533-MHz system bus frequency (133-MHz BCLK[1:0] frequency). |
| COMP[3:0] | Analog | COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the appropriate platform design guide for more details on implementation. |

## Table 16. Signal Description (Sheet 3 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>D[63:0]#</td><td>Input/ Output</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.<br>D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#.<br>Quad-Pumped Signal Groups
<table>
<tr><th>Data Group</th><th>DSTBN# / DSTBP#</th><th>DINV#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBR#</td><td>Output</td><td>DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.</td></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both FSB agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both FSB agents.</td></tr>
</table>

**Table 16. Signal Description (Sheet 4 of 9)**

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DINV[3:0]#</td><td>Input/ Output</td><td>DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.<br>DINV[3:0]# Assignment to Data Bus
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DINV[3]#</td><td>D[63:48]#</td></tr>
<tr><td>DINV[2]#</td><td>D[47:32]#</td></tr>
<tr><td>DINV[1]#</td><td>D[31:16]#</td></tr>
<tr><td>DINV[0]#</td><td>D[15:0]#</td></tr>
</table></td></tr>
<tr><td>DPRSTP#</td><td>Input</td><td>DPRSTP# is not used by the Celeron M processor. For termination requirements please refer to the platform design guide.</td></tr>
<tr><td>DPSLP#</td><td>Input</td><td>DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. In order to return to the Sleep State, DPSLP# must be deasserted. DPSLP# is driven by the ICH7M chipset.</td></tr>
<tr><td>DPWR#</td><td>Input</td><td>DPWR# is a control signal from the Mobile Intel® 945 Express Chipset family used to reduce power on the CPU data bus input buffers. This is not utilized by the Celeron M Processor 500 Series.</td></tr>
<tr><td>DRDY#</td><td>Input/ Output</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr>
<tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr>
<tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr>
<tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr>
</table></td></tr>
<tr><td>DSTBP[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DINV[0]#</td><td>DSTBP[0]#</td></tr>
<tr><td>D[31:16]#, DINV[1]#</td><td>DSTBP[1]#</td></tr>
<tr><td>D[47:32]#, DINV[2]#</td><td>DSTBP[2]#</td></tr>
<tr><td>D[63:48]#, DINV[3]#</td><td>DSTBP[3]#</td></tr>
</table></td></tr>
</table>

## Table 16. Signal Description (Sheet 5 of 9)

| Name | Type | Description |
|---|---|---|
| FERR#/PBE# | Output | FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# assertion indicates that an unmasked floating point error has been detected. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. In both cases, assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.<br>For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the *Intel® 64 and IA-32 Intel® Architectures Software Developer's Manual* and *AP-485 Intel® Processor Identification and the CPUID Instruction application note.*<br>For termination requirements please refer to the appropriate platform design guide. |
| GTLREF | Input | GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 $V_{CCP}$. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Please refer to the appropriate platform design guide for details on GTLREF implementation. |
| HIT#<br>HITM# | Input/ Output<br>Input/ Output | HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together. |
| IERR# | Output | IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.<br>For termination requirements please refer to the appropriate platform design guide. |
| IGNNE# | Input | IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set.<br>IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/ Output Write bus transaction. |

**Table 16. Signal Description (Sheet 6 of 9)**

| Name | Type | Description |
|---|---|---|
| INIT# | Input | INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both FSB agents.<br>If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)<br>For termination requirements please refer to the appropriate platform design guide. |
| LINT[1:0] | Input | LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous.<br>Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/ INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration. |
| LOCK# | Input/ Output | LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction.<br>When the priority agent asserts BPRI# to arbitrate for ownership of the FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the FSB throughout the bus locked operation and ensure the atomicity of lock. |
| PRDY# | Output | Probe Ready signal used by debug tools to determine processor debug readiness. |
| PREQ# | Input | Probe Request signal used by debug tools to request debug operation of the processor. |
| PROCHOT# | Input/ Output | As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system deasserts PROCHOT#.<br>This signal may require voltage translation on the motherboard. |
| PSI# | Output | Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep). |

## Table 16. Signal Description (Sheet 7 of 9)

| Name | Type | Description |
|---|---|---|
| PWRGOOD | Input | PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. “Clean” implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state.<br>The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. |
| REQ[4:0]# | Input/ Output | REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#. |
| RESET# | Input | Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after $V_{CC}$ and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.<br>Please refer to the appropriate platform design guide for termination requirements and implementation details. There is a 55 Ω (nominal) on-die pull-up resistor on this signal. |
| RS[2:0]# | Input | RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents. |
| RSVD | Reserved /No Connect | These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. |
| SLP# | Input | SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state. |
| SMI# | Input | SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.<br>If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs. |

**Table 16. Signal Description (Sheet 8 of 9)**

| Name | Type | Description |
|---|---|---|
| STPCLK# | Input | STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input. |
| TCK | Input | TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).<br>Please refer to the platform design guide for termination requirements and implementation details. |
| TDI | Input | TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.<br>Please refer to the appropriate platform design guide for termination requirements and implementation details. |
| TDO | Output | TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.<br>Please refer to the appropriate platform design guide for termination requirements and implementation details. |
| TEST1, TEST2, TEST3, TEST4 | Input | TEST1 and TEST2 must have a stuffing option of separate pull down resistors to $V_{SS}$.<br>For testing purposes it is recommended, but not required, to route the TEST3 and TEST4 pins through a ground referenced 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.<br>Please refer to the appropriate platform design guide for more details. |
| THERMDA | Other | Thermal Diode Anode. |
| THERMDC | Other | Thermal Diode Cathode. |
| THERMTRIP# | Output | The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin. |
| TMS | Input | TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.<br>Please contact you Intel representative for more details |
| TRDY# | Input | TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents. |
| TRST# | Input | TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. |
| $V_{CC}$ | Input | Processor core power supply. |
| $V_{CCA}$ | Input | $V_{CCA}$ provides isolated power for the internal processor core PLL's. |
| $V_{CCP}$ | Input | Processor I/O Power Supply. |

## Table 16. Signal Description (Sheet 9 of 9)

| Name | Type | Description |
|---|---|---|
| $V_{CC\_SENSE}$ | Output | $V_{CC\_SENSE}$ together with $V_{SS\_SENSE}$ are voltage feedback signals to Intel® MVP 6 that control the 2.1-mΩ loadline at the processor die. It should be used to sense or measure power near the silicon with little noise. |
| VID[6:0] | Output | VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages ($V_{CC}$). Unlike some previous generations of processors, these are CMOS signals that are driven by the Celeron M processor. The voltage supply for these pins must be valid before the VR can supply $V_{CC}$ to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 2 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself. |
| $V_{SS\_SENSE}$ | Output | $V_{SS\_SENSE}$ together with $V_{CC\_SENSE}$ are voltage feedback signals to Intel MVP 6 that control the 2.1-mΩ loadline at the processor die. It should be used to sense or measure ground near the silicon with little noise. |

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# 5 Thermal Specifications

A complete thermal solution includes both component and system level thermal management features. The Celeron M processor requires a thermal solution to maintain temperatures within operating limits.

***Caution:*** Any attempt to operate the processor outside operating limits may result in permanent damage to the processor and potentially other components in the system.

The system/processor thermal solution should remain within the minimum and maximum junction temperature (Tj) specifications at the corresponding thermal design power (TDP) value listed below.

Contact your Intel representative for more details on processor and system level cooling approaches.

**Table 17. Power Specifications for the Celeron M Processor 500 Series**

| Symbol | Processor Number | Core Frequency and Voltage | Thermal Design Power | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| TDP | 520-fused | 1.60 GHz | 30 | | | W | 1,4,5 |
| TDP | 530-fused | 1.73 GHz | 30 | | | W | 1,4,5 |
| TDP | 520 | 1.60 GHz | 26 | | | W | 1,4,5,8 |
| TDP | 530 | 1.73 GHz | 26 | | | W | 1,4,5,8 |
| **Symbol** | **Parameter** | | **Min** | **Typ** | **Max** | **Unit** | |
| $P_{AH}$, $P_{SGNT}$ | Auto Halt, Stop Grant Power at $V_{CC}$ | | | | 10.9 | W | 2,6 |
| $P_{SLP}$ | Sleep Power at $V_{CC}$ | | | | 10.1 | W | 2,6 |
| $P_{DSLP}$ | Deep Sleep Power at $V_{CC}$ | | | | 5.6 | W | 2,7 |
| $T_J$ | Junction Temperature | | 0 | | 100 | °C | 3,4 |

**NOTES:**
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum $T_J$ has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. At Tj of 100°C.
6. At 50°C.
7. At 35°C.
8. The units will display processor family ID 06F6h.

**Table 18. Ultra Low Voltage Power Specifications**

| Symbol | Processor Number | Core Frequency & Voltage | Die Variant | Thermal Design Power | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| TDP | 523 | 0.933 GHz | 1 M | 5.5 | | | W | 1,4,5 |
| **Symbol** | **Parameter** | | | **Min** | **Typ** | **Max** | **Unit** | |
| $P_{AH}$, $P_{SGNT}$ | Auto Halt, Stop Grant Power at $V_{CC}$ | | | | | 1.7 | W | 2,6 |
| $P_{SLP}$ | Sleep Power at Vcc | | | | | 1.6 | W | 2,6 |
| $P_{DSLP}$ | Deep Sleep Power at $V_{CC}$ | | | | | 0.8 | W | 2,7 |
| $T_J$ | Junction Temperature | | | 0 | | 100 | °C | 3,4 |

**NOTES:**
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum $T_J$ has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. At Tj of 100°C.
6. At 50°C.
7. At 35°C.

The Celeron M processor incorporates three methods of monitoring die temperature:

- Thermal diode
- Intel Thermal Monitor
- Digital Thermal Sensor

***Note:*** The Intel Thermal Monitor (detailed in Section 5.2) must be used to determine when the maximum specified processor junction temperature has been reached.

## 5.1 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal "diode," with its collector shorted to Ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor Model Specific Register (MSR) and applied. See Section 5.1.1 for more details. Please see Section 5.2 for thermal diode usage recommendation when the PROCHOT# signal is not asserted.

***Note:*** The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals will not necessarily reflect the temperature of the

hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the $T_J$ temperature can change.

Offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events. This offset is different than the diode Toffset value programmed into the Celeron M processor MSR.

Table 19 to Table 22 provides the diode interface and specifications. Two different sets of diode parameters are listed in Table 21 and Table 22. The Diode model parameters apply to the traditional thermal sensors that use the Diode equation to determine the processor temperature. Transistor model parameters have been added to support thermal sensors that use the transistor equation method. The transistor model may provide more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Please contact your external sensor supplier for their recommendation. The thermal diode is separate from the Intel Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Intel Thermal Monitor.

### 5.1.1 Thermal Diode Offset

In order to improve the accuracy of the diode based temperature measurements, a temperature offset value (specified as Toffset) will be programmed in the Celeron M processor Model Specific Register (MSR) which will contain thermal diode characterization data. During manufacturing each processor thermal diode will be evaluated for its behavior relative to the theoretical diode. Using the equation above, the temperature error created by the difference $n_{trim}$ and the actual ideality of the particular processor will be calculated.

If the $n_{trim}$ value used to calculate the Toffset differs from the $n_{trim}$ value used to in a temperature sensing device, the $T_{error(nf)}$ may not be accurate. If desired, the Toffset can be adjusted by calculating $n_{actual}$ and then recalculating the offset using the $n_{trim}$ as defined in the temperature sensor manufacturer's data sheet.

The $n_{trim}$ used to calculate the Diode Correction Toffset are listed in Table 19.

**Table 19. Thermal Diode $n_{trim}$ and Diode Correction Toffset**

| Symbol | Parameter | | Unit |
|---|---|---|---|
| $n_{trim}$ | Diode Ideality used to calculate Toffset | 1.01 | |

Please contact your Intel representative for more details on the temperature offset MSR definition and recommended offset implementation.

**Table 20. Thermal Diode Interface**

| Signal Name | Pin/Ball Number | Signal Description |
|---|---|---|
| THERMDA | A24 | Thermal diode anode |
| THERMDC | A25 | Thermal diode cathode |

## Table 21. Thermal Diode Parameters using Diode Mode

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{FW}$ | Forward Bias Current | 5 | | 200 | µA | 1 |
| n | Diode Ideality Factor | 1.000 | 1.009 | 1.050 | | 2, 3, 4 |
| $R_{TT}$ | Series Resistance | 2.79 | 4.52 | 6.24 | W | 2, 3, 5 |

**NOTES:**

1. Intel does not support or recommend operation of the thermal diode under reverse bias. Intel does not support or recommend operation of the thermal diode when the processor power supplies are not within their specified tolerance range.
2. Characterized across a temperature range of 50–100°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:
   $I_{FW}=I_s *(e^{(qV_D/nkT)} -1)$,
   where $I_S$ = saturation current, q = electronic charge, $V_D$ = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, $R_{TT}$, is provided to allow for a more accurate measurement of the diode junction temperature. $R_{TT}$ as defined includes the pins of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. $R_{TT}$ can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:
   $T_{error} = [R_{TT}*(N-1)*I_{FWmin}]/[(no/q)*\ln N]$
   where $T_{error}$ = sensor temperature error, N = sensor current ratio, k = Boltzmann Constant, and q = electronic charge.

**Table 22. Thermal Diode Parameters using Transistor Model**

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{FW}$ | Forward Bias Current | 5 | | 200 | µA | 1,2 |
| $I_E$ | Emitter Current | 5 | | 200 | µA | 1 |
| $n_Q$ | Transistor Ideality | 0.997 | 1.001 | 1.005 | | 3,4,5 |
| Beta | | 0.3 | | 0.760 | | 3,4 |
| $R_{TT}$ | Series Resistance | 2.79 | 4.52 | 6.24 | Ω | 3,6 |

**NOTES:**
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Same as $I_{FW}$ in Table 21.
3. Characterized across a temperature range of 50-100°C.
4. Not 100% tested. Specified by design characterization.
5. The ideality factor, $n_Q$, represents the deviation from ideal diode behavior as exemplified by the equation for the collector current:
   $I_C = I_s * (e^{(qV_{BE}/n_Q kT)} - 1)$
   where $I_S$ = saturation current, q = electronic charge, $V_{BE}$ = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).
6. The series resistance, $R_{TT}$, provided in the Diode Model Table (Table 21) can be used for more accurate readings as needed.

When calculating a temperature based on the thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equations listed under Table 21. In most sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode, the ideality value (also called $n_{trim}$)will be 1.000. Given that most diodes are not perfect, the designers usually select an $n_{trim}$ value that more closely matches the behavior of the diodes in the processor. If the processor diode ideality deviates from that of the $n_{trim}$, each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

$$T_{error(nf)} = T_{measured} * (1 - n_{actual}/n_{trim})$$

Where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, $n_{actual}$ is the measured ideality of the diode, and $n_{trim}$ is the diode ideality assumed by the temperature sensing device.

## 5.2 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable.

***Caution:*** An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: Automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

***Note:*** The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications.

The processor supports an automatic mode called Intel Thermal Monitor 1. This mode is enabled by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

During high temperature situations, Intel Thermal Monitor 1 will modulate the clocks by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/ inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

***Note:*** PROCHOT# will not be asserted when the processor is in the Stop Grant, Sleep, and Deep Sleep low power states (internal clocks stopped.). As a result, the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low power states with PROCHOT# already asserted, PROCHOT# will remain

asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

## 5.3 Digital Thermal Sensor

The Celeron M processor also contains an on-die Digital Thermal Sensor (DTS) that can be read via a MSR (no I/O interface). The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation via the Intel Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (C0 state).

Unlike traditional thermal devices, the DTS will output a temperature relative to the maximum supported operating temperature of the processor ($T_{J,max}$). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the digital thermal sensor will always be at or below $T_{J,max}$. Over temperature conditions are detectable via an Out Of Spec status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not guaranteed once the activation of the Out of Spec status bit is set.

The DTS relative temperature readout corresponds to an Intel Thermal Monitor trigger point. When the DTS indicates maximum processor core temperature has been reached the Intel Thermal Monitor 1 hardware thermal control mechanism will activate. The DTS and Intel Thermal Monitor 1 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach and software application. The system designer is required to use the DTS to guarantee proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's APIC. Refer to the *Intel® 64 and IA-32 Intel® Architectures Software Developer's Manual* for specific register and programming details

## 5.4 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor's Intel Thermal Monitor 1 is triggered and the temperature remains high, an "Out Of Spec" status and sticky bit are latched in the status MSR register and generates thermal interrupt.

## 5.5 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If the Intel Thermal Monitor 1 is enabled (note that the Intel Thermal Monitor 1 must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

The Celeron M processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from over-heating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

One application for the PROCHOT# signal is the thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR can cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

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