Addendum— Intel Architecture Software Developer's Manual

Volume 1: Basic Architecture

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NOTE: The *Intel Architecture Software Developer's Manual* consists of the following volumes: *Basic Architecture*, Order Number 243190; *Instruction Set Reference*, Order Number 243191; Addendum to the *Instruction Set Reference*, Order Number 243689; *System Programming Guide*, Order Number 243192; and the Addendum to the *System Programming Guide*, Order Number 243690. Please refer to all of these volumes when evaluating your design needs.

TABLE OF CONTENTS

CHAPTER 10
PROCESSOR IDENTIFICATION AND FEATURE DETERMINATION

When writing software intended to run on several different types of Intel Architecture processors, it is generally necessary to identify the type of processor present in a system and the processor features that are available to an application. This chapter describes how to identify the processor that is executing the code and determine the features the processor supports. It also shows how to determine if an FPU or NPX is present. For more information about processor identification and supported features, refer to the following documents:

- AP-485, *Intel Processor Identification and the CPUID Instruction*
- For a complete list of the features that are available for the different Intel Architecture processors, refer to Chapter 17 of the *Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide.*

10.1. CPUID INSTRUCTION EXTENSIONS

The CPUID instruction of all P6 family processors behave identically. The CPUID instruction is described in detail in the application note, AP-485, *Intel Processor Identification and the CPUID Instruction*. This section describes processor-specific information returned by the CPUID instruction.

The CPUID instruction's behavior varies depending upon the contents of the EAX register when the instruction is executed. Table 10-1 shows the interaction between the value in EAX before the call to CPUID and the value that CPUID returns.

Table 10-1. EAX Input Value and CPUID Return Values

EAX	CPUID Return Values	
0	EAX	Maximum CPUID input value
	EBX	756E6547H 'uneG' (G in BL)
	EDX	49656E69H 'Ieni' (i in DL)
	ECX	6C65746EH 'letn' (n in CL)
1	EAX	Version information (Type, Family, Model, Stepping)
	EBX	Reserved
	EDX	Reserved
	ECX	Feature information
2	EAX	Cache Information
	EBX	Cache Information
	EDX	Cache Information
	ECX	Cache Information

Refer to the CPUID application note, AP-485, for details on cache information. AP-485 is available from the following web site: http://developer.intel.com/design/pro/applnots/ap485.htm.

In addition, the following two new cache descriptors are defined for P6 family processors with Model > 3:

1M L2 Cache	4-way set associative	32-byte line size	44h
2M L2 Cache	4-way set associative	32-byte line size	45h

10.1.1. Version Information

When the CPUID instruction is executed with a 1 in EAX, it returns version and feature information. Figure 10-1 shows the version information bit fields returned by CPUID in EAX. The 233, 266, and 300 MHz Pentium® II processors are indicated by a '6' in the Family ID and a '3' in the Model ID field. Future P6 family processors are indicated by a '6' in the Family ID and a value greater than '3' in the Model ID field.

31 12	11 08	07 04	03 00
Reserved (0)	Family ID	Model ID	Stepping ID

Figure 10-1. Processor Version Information Returned by CPUID in EAX

Figure 10-2 shows the feature information bit fields returned by CPUID in EDX.

31 25	24	23	22-18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved (0)	FXSR	MMX	*rsvd*	PSE-36	PAT	CMOV	MCA	PGE	MTRR	SEP	*rsvd*	APIC	CX8	MCE	PAE	MSR	TSC	PSE	DE	VME	FPU

Figure 10-2. Feature Information Returned by CPUID in EDX

Table 10-2 describes the bit representations for the new P6 family processor features.

Table 10-2. New P6 Family Processor Feature Information Returned by CPUID in EDX

Bit	Feature	Value	Description	Notes
11	SEP	1	Fast System Call	Indicates whether the processor supports the Fast System Call instructions, SYSENTER and SYSEXIT..
23	MMX	1	MMX™ technology	Indicates whether the processor supports the MMX™ technology instruction set and architecture..

Table 10-3 describes the bit representations for new P6 family processor features.

Table 10-3. New P6 Family Processor Feature Information Returned by CPUID in EDX

Bit	Feature	Value	Description	Notes
16	PAT	1	Page Attribute Table	Indicates whether the processor supports the Page Attribute Table. This feature augments the Memory Type Range Registers (MTRRs), allowing an operating system to specify attributes of memory on a page granularity through a linear address.
17	PSE-36	1	36-bit Page Size Extension	Indicates whether the processor supports 4 MB pages that are capable of addressing physical memory beyond 4 GB. This feature indicates that the upper four bits of the physical address of the 4-MB page is encoded by bits 13-16 of the page directory entry.
18-22	rsvd	0	Reserved	These bits are reserved for future use. The contents of these fields are not defined and should not be relied upon or altered.
24	FXSR	1	Fast floating point save and restore	Indicates whether the processor supports the FXSAVE and FXRSTOR instructions for fast save and restore of the floating point context. Presence of this bit also indicates that CR4.OSFXSR is available, allowing an operating system to indicate that it uses the fast save/restore instructions.

10.1.2. Control Register Extensions

The control registers (CR0, CR1, CR2, CR3 and CR4) determine the operating mode of the processor and the characteristics of the currently executing task. A new field has been added to CR4, which contains a group of flags used to enable several architectural extensions as depicted in Figure 10-3.

31 10	09	08	07	06	05	04	03	02	01	00
Reserved (set to 0)	OSFXSR	PCE	PGE	MCE	PAE	PSE	DE	TSD	PVI	VME

Figure 10-3. CR4 Register Extensions

The new field at bit 9 (OSFXSR) is set by the operating system to indicate that it uses the FXSAVE/FXRSTOR instructions for saving/restoring FP/MMX state during context switches. This bit defaults to clear (zero) at processor initialization.

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