Intel® Xeon™ Processor and Intel® E7500 / E7501 Chipset Compatible Platform

Design Guide

For Use with Intel® Xeon™ Processors with 512-KB L2 Cache and Intel® Xeon™ Processors with 533 MHz System Bus

For designing a single platform compatible with both the Intel® E7500 and E7501 chipsets

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Revision History

Revision	Description	Date
-001	Initial Release	December 2002

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Introduction 1

This design guide documents Intel's design recommendations for systems based on the Intel® Xeon™ processor with 512-KB L2 cache / Intel® Xeon™ processor with 533 MHz system bus and the Intel® E7500/E7501 chipset. This guide is intended for E7500/E7501 chipset compatible platforms. All new E7500 chipet platforms should use this document. Existing E7500 chipset-only designs may still conform to the *Intel® Xeon™ Processor with 512 KB L2 Cache and Intel® E7500 Chipset Platform Design Guide.* In addition to providing motherboard design recommendations (e.g., layout and routing guidelines), this document addresses system design issues (e.g., power delivery).

Carefully follow the design information, board schematics, debug recommendations, and system checklists provided in this document. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues.

Note that the guidelines recommended in this document are based on experience and simulation work completed at Intel while developing Intel Xeon processor / E7500/E7501 chipset-based systems.

Board designers may use the associated Intel schematics as a reference. While the schematics cover a specific design implementation, the core schematics remain the same for most E7500/E7501 chipset-based platforms. The schematic set provides a reference schematic for each E7500/E7501 chipset component as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components.

1.1 Terminology

This section defines terminology used throughout the design guide.

Terminology	Description
Aggressor	A network that transmits a coupled signal to another network.
AGTL+	The processor system bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain, and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.
Asynchronous GTL+	Legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output signals (FERR# and IERR#) and non-AGTL+ signals (THERMTRIP# and PROCHOT#) also utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0], and are therefore referred to as "Asynchronous GTL+ Signals". All of the Asynchronous GTL+ signals must be asserted for at least two BCLKs for the processor to recognize them.
Bus Agent	A component or group of components that, when combined, represent a single load on the system bus.

Terminology	Description
Core Power	Core power refers to a power rail that is on only during full-power operation. These power rails are on when the active-low PSON signal is asserted to the power supply. The core power rails that are distributed directly from the power supply are: +12 V, +5 V, and +3.3 V.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk – Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. • Forward Crosstalk – Coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal. • Even Mode Crosstalk – Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk – Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Derived power	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, +2.5 V is derived from a +5 V power rail using a voltage regulator.
Dual Processor (DP)	Used to specify a system configuration using two processors.
Electromagnetic Compatibility (EMC)	The successful operation of electronic equipment in its intended electromagnetic environment.
Electromagnetic Interference (EMI)	Electromagnetic radiation from an electrical source that exceeds the federally regulated limits.
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the Tco of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, flight time is defined as: • The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications, i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when only the driver can drive a test load used to specify the driver's AC timings. • Maximum and Minimum Flight Time – Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance, and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. • Maximum flight time is the largest acceptable flight time that a network experiences under all conditions. • Minimum flight time is the smallest acceptable flight time that a network experiences under all conditions.
Full-power	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state, and the S1 (processor stop-grant) state.
GTLREF	Reference voltage for AGTL+ input pins.
Inter-Symbol Interference (ISI)	The effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line, and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Overshoot	The maximum voltage observed for a signal at the device pad, measured with respect to VCC.

Terminology	Description
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
Pin	The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings can be measured at the pin.
Power-Good	“Power-Good,” “PWRGOOD,” or “CPUPWRGOOD” (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.
Power Rails	A power supply has five power rails: +12 V, –12 V, +5 V, +3.3 V, and +5 VSB. In addition to these power rails from the power supply, several other power rails are derived on the motherboard by on-board regulators.
Ringback	The voltage to which a signal changes after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.
System Bus	The System Bus is the bus which connects the processor to the platform.
Setup Window	The time between the beginning of Setup to Clock (TSU_MIN) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
Simultaneous Switching Output (SSO)	Effects which are differences in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (“push-out”) or a decrease in propagation delay (“pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Standby Power Rail	Standby power is supplied by the power supply during times when the system is powered down. The purpose is to maintain functions that always need to be enabled, such as the date and time-of-day within the BIOS. The power supply provides a +5 VSB power rail.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	The minimum voltage extending below VSS observed for a signal at the device pad.
VCC_CPU	VCC_CPU is the core power for the processor. The system bus is terminated to VCC_CPU.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
Voltage Regulator Down (VRD)	A VRD refers to a processor voltage regulator which is placed directly onto the system motherboard.
Voltage Regulator Module (VRM)	A VRM refers to a processor voltage regulator which is designed on an add-in card that interfaces with the system design through a connector on the platform.
Intel® x4 Single Device Data Correction (x4 SDDC)	In a x4 DDR memory device, provides error detection and correction for 1, 2, 3 or 4 data bits within that single device and in two x4 DDR memory devices, provides error detection in up to 8 data bits within those two devices.

1.2 Reference Documentation

Table 1-1. Reference Documents (Sheet 1 of 2)

Document	Document Number/Source
603-Pin Socket Design Guidelines	http://developer.intel.com/design/Xeon/guides/249672.htm
ITP700 Debug Port Design Guide	http://developer.intel.com/design/Xeon/guides/
Intel® Xeon™ Processor with 512-KB L2 Cache Signal Integrity Models	http://developer.intel.com/design/Xeon/devtools
Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet	http://developer.intel.com/design/chipsets/e7500/datashts/290733.htm
Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Thermal Design Guide	http://developer.intel.com/design/chipsets/e7500/guides/252175.htm
Intel®E7500/E7501/E7505 Chipset Thermal Design Guide	http://developer.intel.com/design/chipsets/e7500/guides/298647
Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet	http://developer.intel.com/design/chipsets/e7500/datashts/290732.htm
Intel® E7500 Chipset: Intel® E7500 Chipset Memory Controller Hub (MCH) Datasheet	http://developer.intel.com/design/chipsets/e7500/datashts/290730.htm
PCI Bus Power Management Interface Specification, Revision 1.1	http://www.pcisig.com/specifications/pci_bus_power_management_interface
PCI Hot-Plug Specification, Revision 1.1	http://www.pcisig.com/specifications/pci_hot_plug
PCI Local Bus Specification, Revision 2.2	http://www.pcisig.com/specifications/conventional_pci
PCI-PCI Bridge Architecture Specification, Revision 1.1	http://www.pcisig.com/specifications/pci_to_pci_bridge_architecture
PCI Standard Hot-Plug Controller and Subsystem Specification, Revision 1.0	http://www.pcisig.com/specifications/pci_hot_plug
PCI-X Specification, Revision 1.0a	http://www.pcisig.com/specifications/pci_x
System Management Bus Specification (SMBus), Revision 1.1	http://www.smbus.org/specs/
Universal Serial Bus Specification, Revision 1.1	http://www.usb.org/developers/docs.html
VRM 9.1 DC-DC Converter Design Guidelines	http://developer.intel.com/design/Xeon/guides/
Intel® Xeon™ Processor with 512-KB L2 Cache at 1.80 GHz to 2.80 GHz Datasheet	http://developer.intel.com/design/xeon/datashts/298642.htm
Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines	http://developer.intel.com/design/Xeon/guides/
Intel® Xeon™ Processor with 512-KB L2 Cache System Compatibility Guidelines	http://developer.intel.com/design/Xeon/guides/
Intel® Xeon™ Processor Thermal Design Guidelines	http://developer.intel.com/design/Xeon/guides/298348.htm
Intel® Xeon™ Processor Thermal Solution Functional Specifications	http://developer.intel.com/design/Xeon/applnots/249673.htm

Table 1-1. Reference Documents (Sheet 2 of 2)

Document	Document Number/Source
Intel® Xeon™ Processor with 512-KB L2 Cache Thermal Models	http://developer.intel.com/design/Xeon/devtools/
Intel® Xeon™ Processor with 512-KB L2 Cache Mechanical Model in IGES Format	http://developer.intel.com/design/Xeon/devtools/
Intel® Xeon™ Processor with 512-KB L2 Cache Mechanical Model in ProE Format*	http://developer.intel.com/design/Xeon/devtools/
AP-485 Intel® Processor Identification and CPUID Instruction	http://developer.intel.com/design/Xeon/applnots/241618.htm
AP-728 Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions	http://developer.intel.com/design/chipsets/applnots/292276.htm
Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet	http://developer.intel.com/design/chipsets/e7501/datashts/251927
Server System Infrastructure (SSI) Specifications	http://www.ssiforum.org/

NOTES:
1. Contact your Intel Field Representative for additional reference documentation.

1.3 System Overview

The E7500 and E7501 chipsets are Intel's server chipsets designed for use with the Intel Xeon processor. The architecture of the chipset provides the performance and feature-set required for dual-processor based severs in the entry-level and mid-range, front-end and general-purpose server market segments. A chipset component interconnect, the Hub Interface 2.0 (HI2.0), is designed into the E7500/E7501 chipset to provide more efficient communication between chipset components for high-speed I/O. Each HI2.0 provides 1.066 GB/s I/O peak bandwidth. The E7500/E7501 chipset MCH has three HI2.0 connections, delivering 3.2 GB/s peak bandwidth for high-speed I/O, which can be used for PCI/PCI-X bridges. The system bus is used to connect the processor with the E7500/E7501 chipset.

The Intel® Xeon™ processor with 512-KB L2 cache system bus uses a 400 MHz transfer rate for data transfers, delivering 3.2 GB/s. The E7500/E7501 chipset architecture supports a 144-bit wide, 200 MHz DDR memory interface also capable of transferring data at 3.2 GB/s. When the E7501 chipset is used with the Intel® Xeon™ processor with 533 MHz system bus and DDR266 DIMMs, the processor uses a 533 MHz transfer rate for data transfers, delivering 4.27 GB/s.

Table 1-2. DDR and Processor Bus Supported Speeds

Feature	Intel® E7500 Chipset	Intel® E7501 Chipset
Processor Data Bus Speed	400 MHz Only	400 and 533 MHz
DDR Support	DDR200 Only	DDR200 and DDR266

The chipset only supports one clock ratio between the memory bus and processor bus. The MCH will either run in DDR200/400 MHz, or in DDR266/533 MHz.

Table 1-3. Intel® E7500 and E7501 Chipset Lock Step Requirements

Memory Installed	Processor Installed	
	Intel® Xeon™ Processor with 512-KB L2 Cache (INT-mPGA Package)	Intel® Xeon™ Processor with 533 MHz System Bus (FC-mPGAs Package)
DDR200 DIMM	DDR200 / 400 MHz	Not Supported
DDR266 DIMM	DDR200 / 400 MHz	DDR266 / 533 MHz

Unless otherwise noted, the term MCH refers to the E7500 chipset MCH and E7501 chipset MCH. Supported system bus speeds are indicated as 400/533 MHz as applying to both chipsets, though 533 MHz can only be attained using the E7501 chipset with the Intel Xeon processor with 533 MHz system bus. Supported DDR speeds are indicated as DDR200 / DDR266 as applying to both chipsets, though DDR266 is only for the E7501 chipset with the Intel Xeon processor with 533 MHz system bus.

In addition to these performance features, E7500/E7501 chipset-based platforms also provide the RASUM (Reliability, Availability, Serviceability, Usability, and Manageability) features required for entry-level and mid-range servers. These features include: x4 SDDC technology ECC for memory, ECC for all high-performance I/O, out-of-band manageability through SMBus target interfaces on all chipset components, memory scrubbing and auto-initialization, processor thermal monitoring, and Hot-Plug PCI. For a complete list of the features on this platform, refer to the component datasheets listed in Section 1.2.

1.3.1 Intel® Xeon™ Processors

The Intel Xeon processor with 512-KB L2 cache and the Intel Xeon processor with 533 MHz system bus are targeted for servers using Intel® NetBurst™ microarchitecture in a dual-processor (DP) configuration. The processor delivers performance levels that are significantly higher than previous generations of IA-32 processors. The E7500/E7501 chipset compatible platform supports all versions of the Intel Xeon processor with 512-KB L2 cache and Intel Xeon processor with 533 MHz system bus.

The Intel Xeon processor with 512-KB L2 cache is available in the Interposer Micro-Pin Grid Array (INT-mPGA) package and only supports 400 MHz system bus configurations. The Intel Xeon processor with 533 MHz system bus is available in the Flip Chip Micro-Pin Grid Array 2 (FC-mPGA2) package and only supports 533 MHz system bus configurations.

Other differences between these two processors are that the Intel Xeon processor with 533 MHz system bus lacks the PIROM, Scratch EEPROM, thermal sensor, and SMBus that are all available on the Intel Xeon processor with 512-KB L2 cache. The Intel Xeon processor with 533 MHz system bus still contains the thermal diode, but will provide direct access to the diode output pins. These output pins can interface with a thermal sensor device placed on the motherboard. Another difference is that the Intel Xeon processor with 533 MHz system bus requires a new socket termed “mPGA604 socket.” Table 1-4 summarizes the main features offered in the different versions of the Intel Xeon processors. Refer to the *Intel® Xeon™ Processor Datasheet* for complete details about the processor.

Table 1-4. Processor Feature Set Overview

Feature	Intel® Xeon™ Processor with 512-KB L2 Cache (INT-mPGA Package)	Intel® Xeon™ Processor with 533 MHz System Bus (FC-mPGAs Package)
Processor System Bus (PSB)	400 MHz	533 MHz
Data Bus Transfer Rate	3.2 GB/s	4.27 GB/s
Manageability Features	PIROM, Scratch EEPROMs and Thermal Sensor on Package	Direct Thermal Diode Access
Operating Voltage	1.500 V	
Socket	603-Pin Socket and mPGA604 Socket	mPGA604 Socket Only
Package Dimensions[1]	X-Y: 53.5 mm Z: 5.0 mm	X-Y: 42.5 mm Z: 3.6 mm

NOTES:
1. This data is provided for comparison only; refer to the *Intel® Xeon™ Processor Datasheet* for actual specifications

The Intel Xeon processor with 512-KB L2 cache and Intel Xeon processor with 533 MHz system bus include the following advanced microarchitecture features:

- Hyper-Pipelined Technology
- Advanced Dynamic Execution
- Execution Trace Cache
- Streaming SIMD (Single Instruction, Multiple Data) Extensions 2
- Advanced Transfer Cache
- Enhanced Floating Point and Multimedia Engine

The system bus uses a source-synchronous transfer of address and data to improve performance and enables addressing at 2X the system bus frequency and data transfers at 4X the system bus frequency of 100 MHz or 133 MHz. This allows the 400 MHz system bus support to transfer data at 3.2 GB/s for the Intel Xeon processor with 512-KB L2 cache, and the 533 MHz system bus support to transfer data at 4.27 GB/s for the Intel Xeon processor with 533 MHz system bus.

1.3.2 Intel® E7500/E7501 Chipset

The E7500/E7501 chipset consists of three major components: the Intel® E7500/E7501 chipset Memory Controller Hub (referred to throughout this document as the MCH), the Intel® 82801CA I/O Controller Hub 3 (hereafter referred to as ICH3-S), and the Intel® 82870P2 PCI/ PCI-X 64-bit Hub 2 (abbreviated to P64H2). The chipset components communicate via hub interfaces (HIs). The MCH provides four hub interface connections: one for the ICH3-S and three for high-speed I/O using 82870P2 P64H2 components. The hub interfaces are point-to-point and therefore only support two components (the MCH plus one I/O device). Therefore, the system supports a maximum of three P64H2 devices.

1.3.2.1 Intel® E7500/E7501 Memory Controller Hub (MCH)

The MCH is a 1005-ball FC-BGA package and contains the following functionality:

- System Bus
  - — Supports dual processors at 100 MHz or 133 MHz (x4 transfers).
  - — System bus peak bandwidth of 3.2 GB/s (400 MHz) or 4.27 GB/s (533 MHz).
  - — Supports 36-bit system bus addressing model.
  - — 12 deep in-order queue, 2 deep defer queue.
- Memory Bus
  - — 144-bit wide, DDR200 / DDR266 memory interface with memory peak bandwidth of 3.2 GB/s or 4.27 GB/s.
  - — Supports x72, ECC, registered DDR200 / DDR266 DIMMs using 128-Mb, 256-Mb and 512-Mb DRAMs.
  - — Supports a maximum of 16 GB of memory.
  - — Supports Single 4-bit Error Correct, Double 4-bit Error Detect (S4EC/D4ED) using Intel® x4 Single Device Data Correction (x4 SDDC).
  - — Supports up to 32 simultaneous open pages.
- I/O
  - — Provides Hub Interface 1.5 connection for ICH3-S (Hub Interface_A):
    - 266 MB/s point-to-point connection for ICH3-S with parity protection.
    - 8-bit wide, 66 MHz base clock, 4X data transfer.
    - Parallel termination mode for longer trace lengths.
    - 64-bit inbound addressing, 32-bit outbound addressing.
  - — Provides 3 Hub Interface 2.0 Connections for P64H2 devices (Hub Interfaces_B, C and D):
    - 1.066 GB/s point-to-point connection per connection for I/O bridges with ECC protection for up to 3.2 GB/s bandwidth when 3 devices are used.
    - 16-bit wide, 66 MHz base clock, 8X data transfer.
    - Parallel termination mode for longer trace lengths.
    - 64-bit inbound addressing, 32-bit outbound addressing.
- Power Management
  - — Supports C0, C1, C2, S0, S1, and S5 power states. **(Does not support C3, C4, S2, S3, and S4).**

1.3.2.2 I/O Controller Hub 3 (Intel® ICH3-S)

The I/O Controller Hub 3 (ICH3-S) provides the legacy I/O subsystem for E7500 chipset-based platforms. Additionally, it integrates many advanced I/O functions. The ICH3-S includes the following features:

- Provides Hub Interface 1.5 Connection to MCH
  - 266 MB/s point-to-point connection for ICH3-S with parity protection
  - 8-bit wide, 66 MHz base clock, 4X data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing
- 2 channel Ultra ATA/100 bus master IDE controller
- 3 Universal Host Controller Interface (UHCI) USB 1.1 compliant host controllers (capabilities for six ports)
- I/O APIC
- *System Management Bus (SMBus) Specification, Version 2.0* compliant controller
- Low Pin Count (LPC) interface
- *AC '97 Component Specification, Revision 2.2* compliant interface
- *PCI Local Bus Specification, Revision 2.2* compliant interface
- Integrated LAN controller

1.3.2.3 PCI/PCI-X 64-bit Hub 2 (Intel® 82870P2 P64H2)

The P64H2 provides PCI/PCI-X, high-performance I/O capability including:

- 16-bit, Hub Interface 2.0 Connection to MCH
  - 1.066 GB/s point-to-point connection for I/O bridges with ECC protection
  - 16-bit wide, 66 MHz base clock, 8X data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing
- Two Independent, 64-bit PCI/PCI-X Interfaces
  - *PCI-X Specification, Revision 1.0a* compliant
  - *PCI Local Bus Specification, Revision 2.2* compliant
  - *PCI-PCI Bridge Architecture Specification, Revision 1.1* compliant
  - *PCI Hot-Plug Specification, Revision 1.1* compliant
  - One PCI Hot-Plug Controller (PHPC) per PCI/PCI-X interface
  - One IOxAPIC per PCI/PCI-X Interface (16 external, 8 internal interrupts)
  - SMBus target for access to all internal PCI registers

1.3.3 Peak Bandwidth Summary

Table 1-5 describes the clock maximum speed, sample rate, and peak bandwidth for each of the interfaces in the E7500/E7501 chipset based platform.

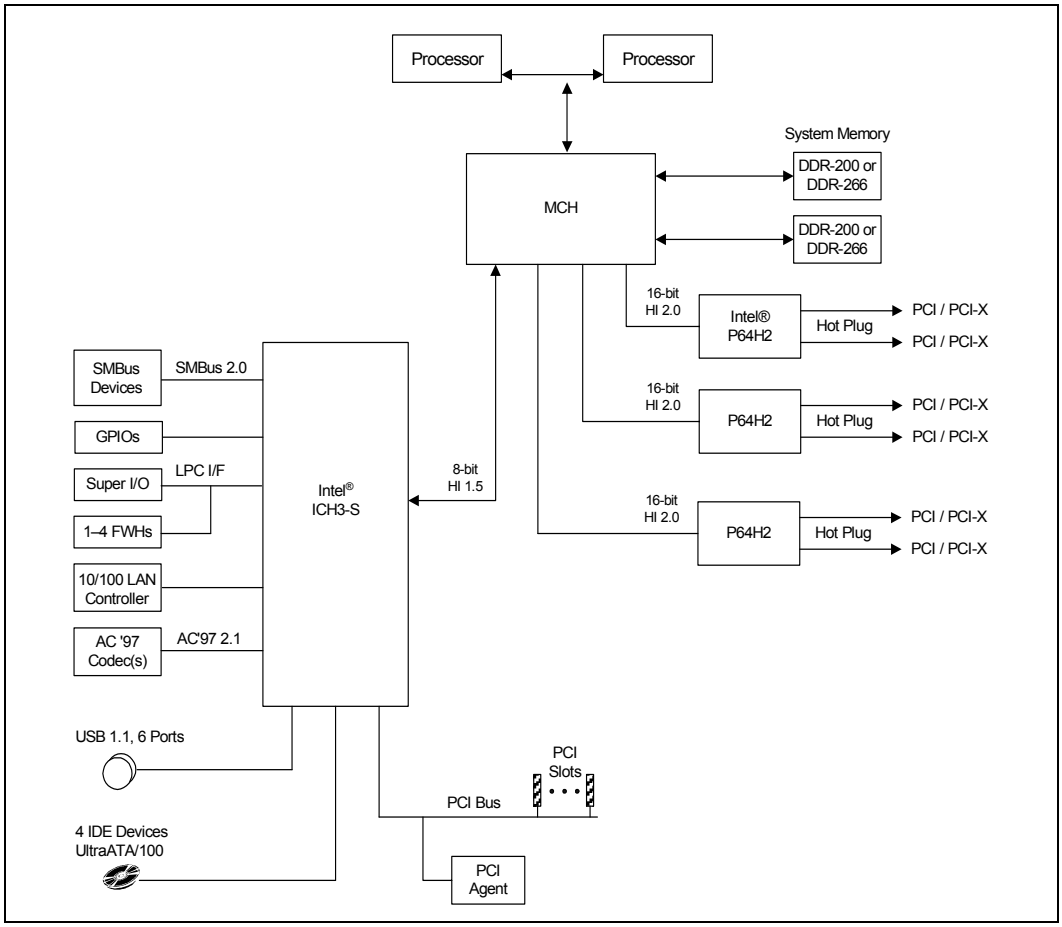
Table 1-5. Platform Peak Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Peak Bandwidth (MB/s)
System Bus (Data)	100 / 133	4	8	3200 / 4270
DDR Interface	100 / 133	2	16	3200 / 4270
Hub Interface_A	66	4	1	266
Hub Interface_B,C,D	66	8	2	1066
PCI-X	133	1	8	1066

1.3.4 System Configurations

Figure 1-1 illustrates an example E7500/E7501 chipset-based system configuration for server platforms using Intel Xeon processors.

Figure 1-1. Example Intel® E7500/E7501 Chipset-Based System Configuration



Component Quadrant Layout 2

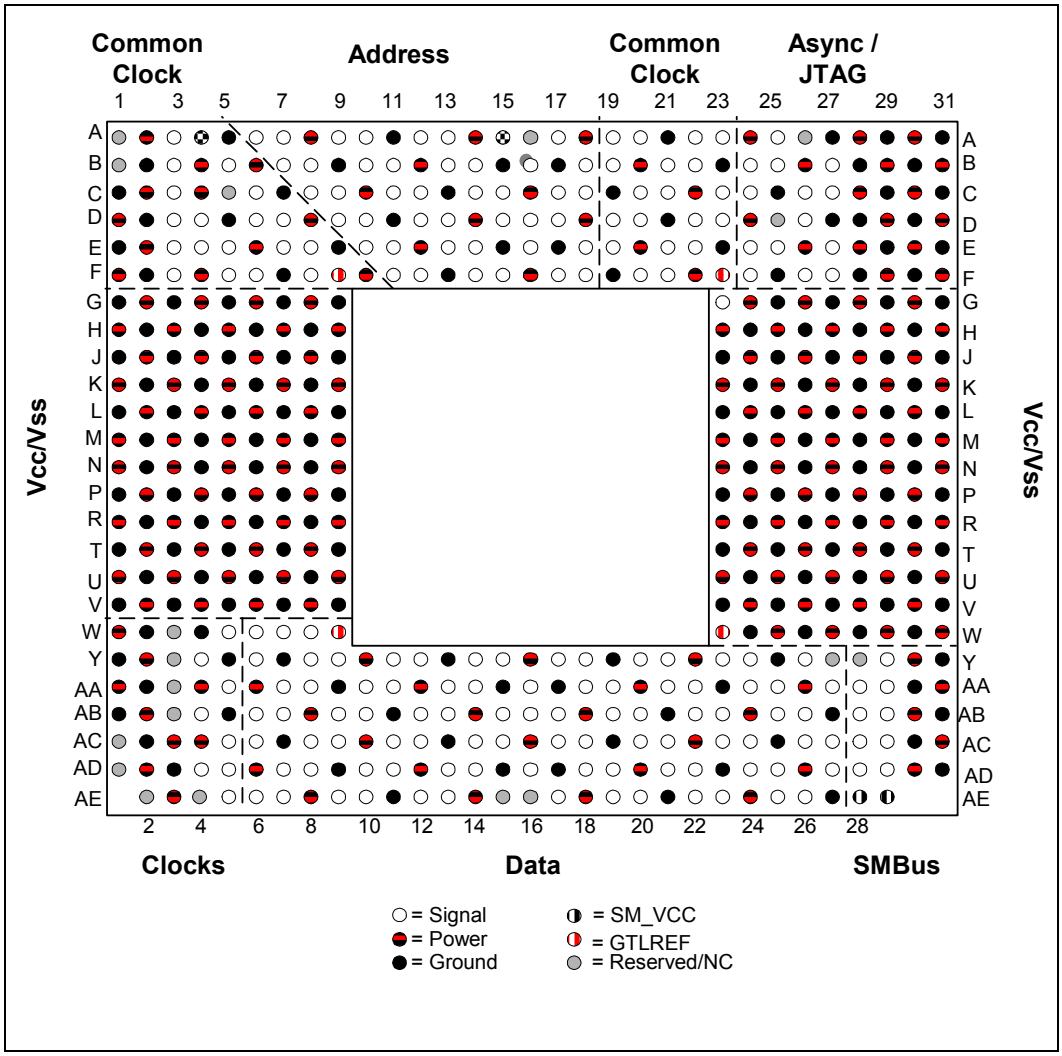
The following figures show only general quadrant information, not exact component ball count. Designers should use only the exact ball assignment to conduct routing analyses. Reference the following documents for exact ball assignment information.

- *Intel® Xeon™ Processor Datasheet*
- *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet*
- *Intel® PCI-64 Hub 2 (P64H2) Datasheet*
- *Intel® E7500 Chipset Memory Controller Hub (MCH) Datasheet*
- *Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet*

2.1 Intel® Xeon™ Processor Quadrant Layout

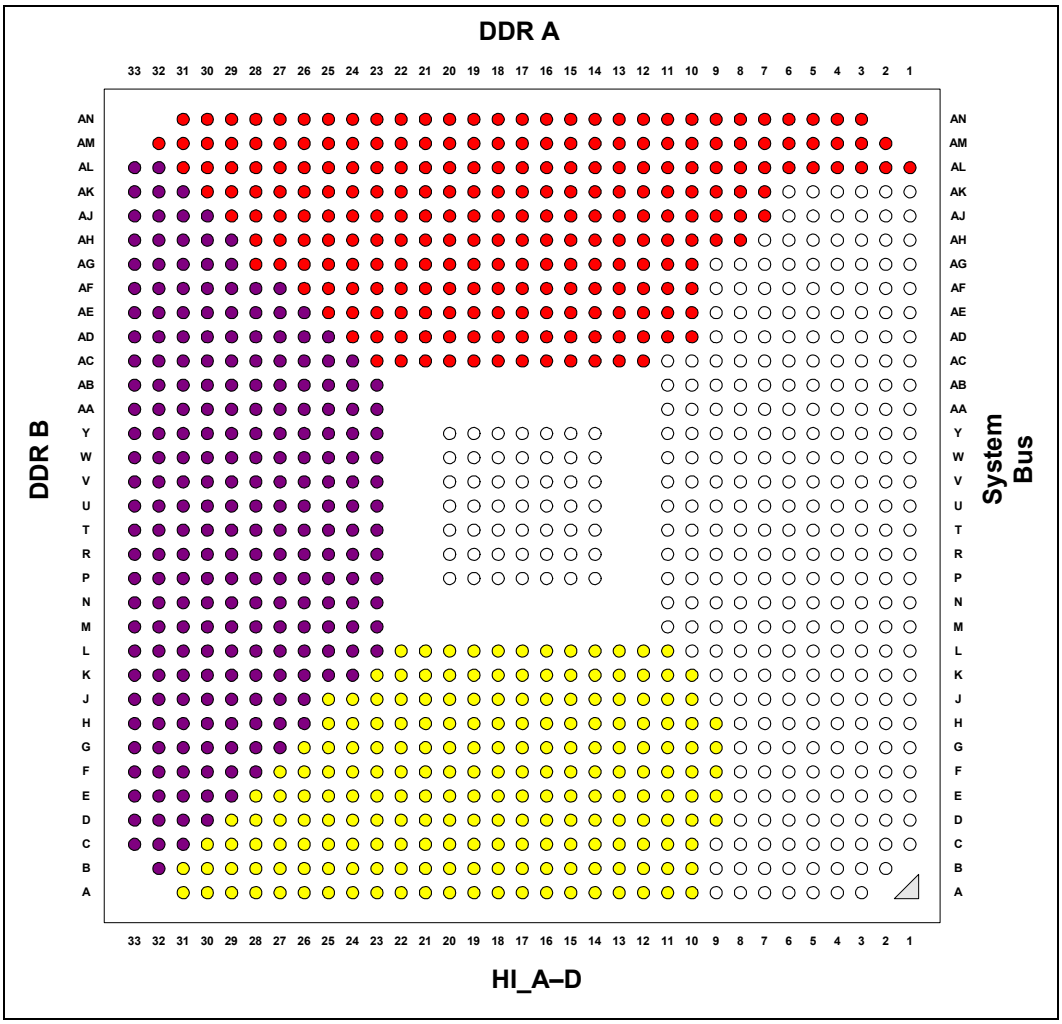
Figure 2-1 shows the quadrant layout for the Intel Xeon processor with 512-KB L2 cache and Intel Xeon processor with 533 MHz system bus.

Figure 2-1. Intel® Xeon™ Processor Quadrant Layout (Top View)



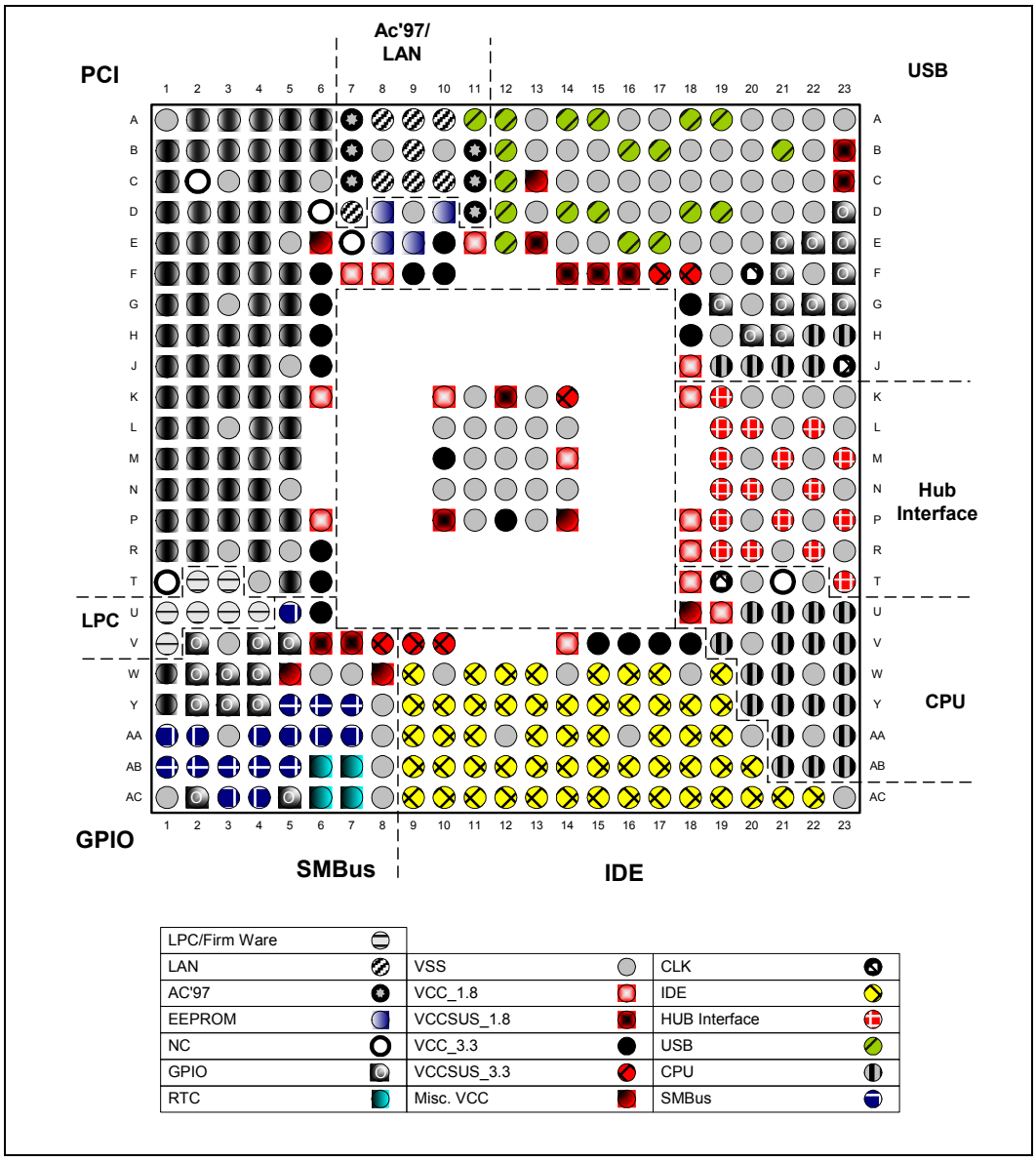
2.2 Intel® E7500/E7501 Chipset MCH Quadrant Layout

Figure 2-2. Intel® E7500/E7501 Chipset MCH Quadrant Layout (Top View)



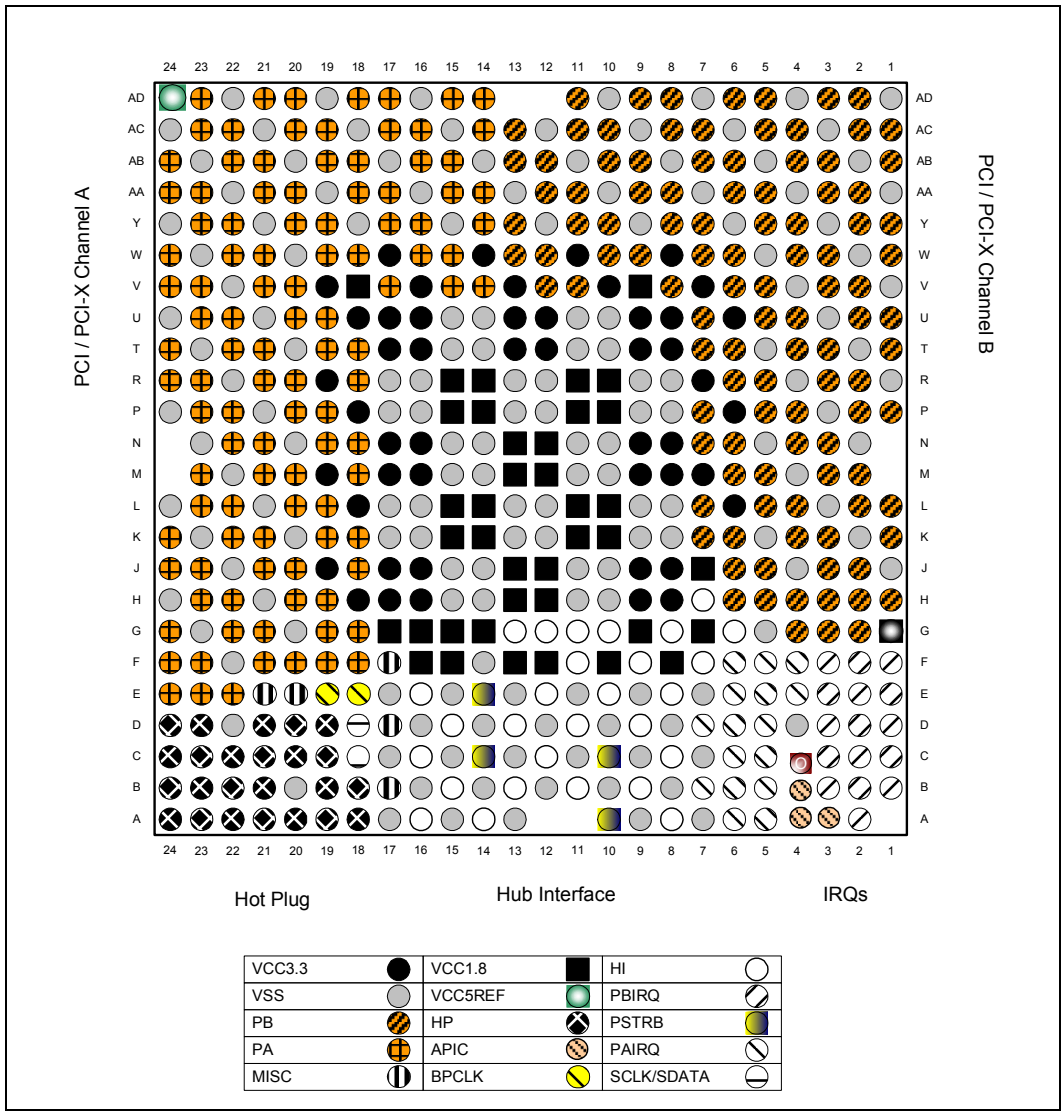
2.3 Intel® ICH3-S Quadrant Layout

Figure 2-3. Intel® ICH3-S Quadrant Layout (Top View)



2.4 Intel® 82870P2 P64H2 Quadrant Layout

Figure 2-4. Intel® P64H2 Quadrant Layout (Top View)



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Baseboard Requirements 3

This chapter summarizes the stack-up used for all platform simulations, the placement of components on the motherboard, and required features to be SSI compliant.

3.1 Platform Stack-Up

Figure 3-1 shows the recommended platform stack-up. All layers are 1 oz copper. The processor requires 2 oz of copper to deliver power and 2 oz of copper to deliver ground.

Route signal layers as asymmetric stripline on layers 2, 4, 5, and 7. The signal layers must reference ground on layer 3 or layer 6 only. Route signals on layers 4 and 5 orthogonally with respect to routes on signal layers to reduce crosstalk between the layers.

Intel strongly recommends that system designers use the stack-up shown in Figure 3-1 and recommendations in Table 3-1 when designing their boards. Intel realizes numerous ways exist to achieve these targeted impedance tolerances; contact your board vendor for these specifics. Intel encourages platform designers to perform comprehensive simulation analysis to ensure all timing specifications are met. This is particularly important if a design deviates from the design guidelines provided.

Figure 3-1. 8 Layer, 50 Ω Board with 5-Mil Traces

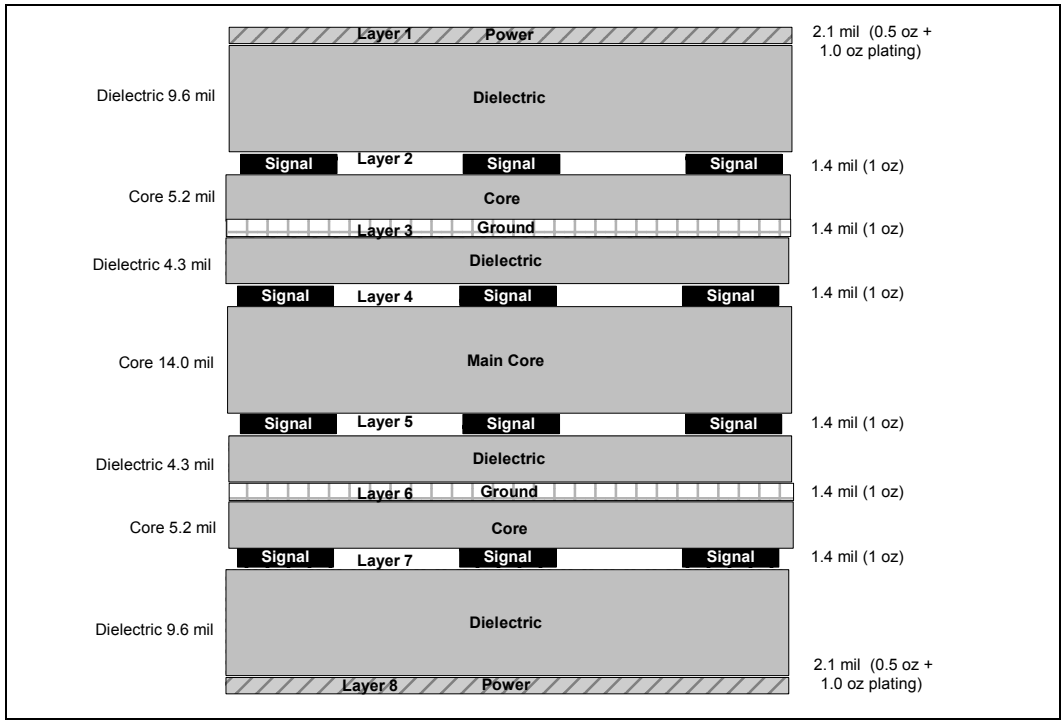


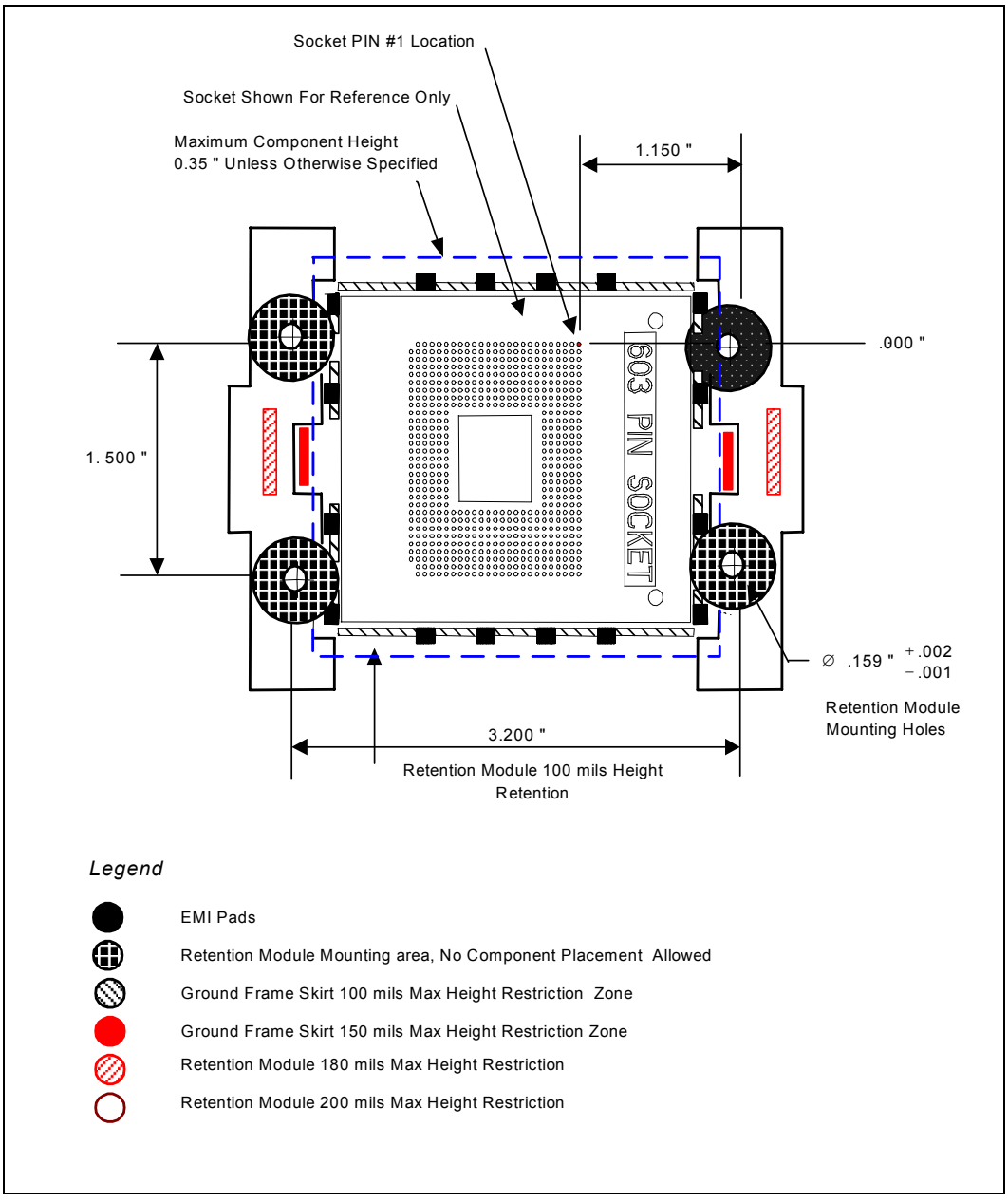
Table 3-1. Board Requirements

Board Factor	Recommendation
Material	• Standard FR4 Tg 170 Epoxy.
Impedance Requirements	• 50 Ω impedance ± 10% Layers 2,4,5,7 (except lower left corner SCSI interface). • SCSI interface 83 Ω single-ended, 122 Ω differential pair ± 10% (layers 1 and 8 lower-left corner using the reference stack-up).
Etch	• 5-mil trace width and space minimum inner/outer. • SCSI interface: 6-mil separation within a pair, 20-mil space between adjacent pairs.
Finished Via Size	• Minimum via size is 0.014 mil, finished in a 0.026-mil land with 0.040-mil antipad. • Approximately 15,000 plated through holes total.
Finish	• Solder Mask On Bare Copper (SMOBC)
Soldermask Type	• SM-840 minimum web 0.004 mils.
Fabrication	• Edge Routed.
Component Technology	• Through hole / SMT. • QFP, BGA, front side. • Discrete 0603, 0805 back side.

3.2 Processor Retention Mechanism Placement and Keep-Outs

The Retention Mechanism (RM) for the Intel Xeon processor requires two keep-out zones: one for the EMI ground pads, and another for a limited component height area under the RM. This is specified in the *Intel® Xeon™ Processor Datasheet*. Figure 3-2 shows the relationship between the RM mounting holes and pin one of the sockets; it also documents the ground pads and keep-outs.

Figure 3-2. Retention Mechanism Placement and Keep-Out Overview

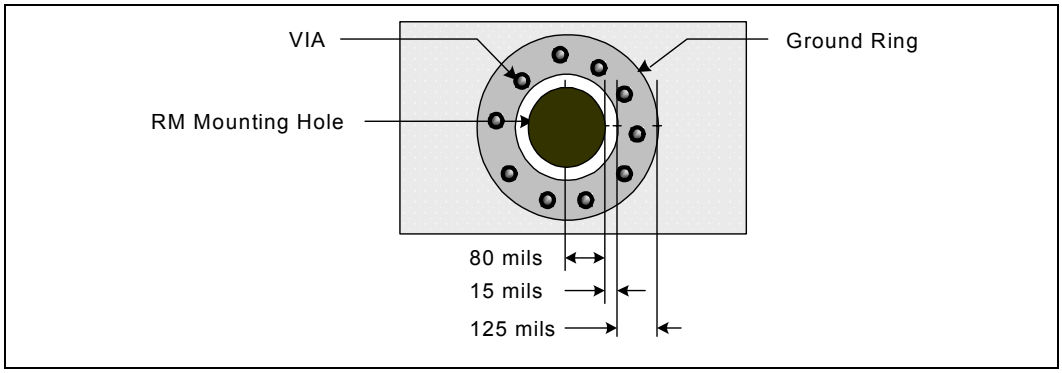


Utilization of the DC grounding strips requires ground pads around the mounting holes for the retention mechanism. Metal inserts will be pre-assembled to the retention modules to establish DC contact between heatsink base plate and the motherboard ground. The inserts will be grounded to the baseboard at mounting hole ground pads. Fingers on top of the insert will connect to the base of the heatsink. The requirements for the DC grounding insert are as follows:

- All four RM mounting holes must have ground pad rings.
- Ground pad annular ring should be no less than 125-mils wide. Try to cover the entire keep-out zone, if possible. See Figure 3-3 for better dimensions.
- Place 8–12 vias in the annular ring, which connects the pad to internal ground planes.
- Anodizing or any form of insulated coating of the heatsink is strongly discouraged.

Refer to Figure 3-3 for specific details regarding the required ground pads.

Figure 3-3. Retention Mechanism Ground Ring



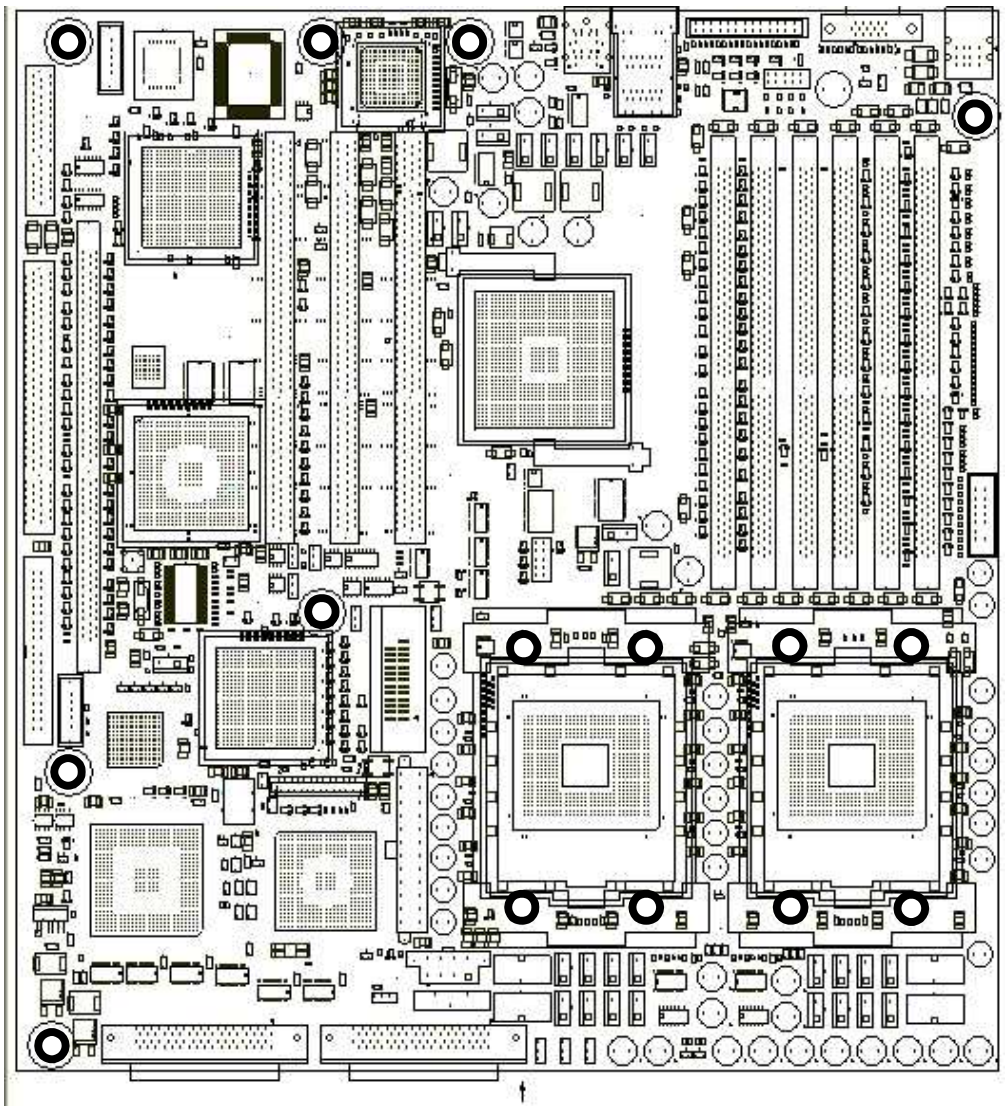
3.3 Platform Component Placement

Figure 3-4 illustrates the component placement for a typical tower optimized board. Table 3-2 lists the assumptions used for the component placement. Refer to www.ssiforum.org for detailed information on the SSI (Server System Infrastructure) specification.

Table 3-2. Assumptions for System Placement Example

System Configuration	Assumptions		
	Form Factor (SSI Specification)	Number of PCB Layers	Assembly
DP Server	SSI Entry (12”x13”)	8 Layers	Double Sided

Figure 3-4. Typical 2U Rack Optimized Board System Placement Example



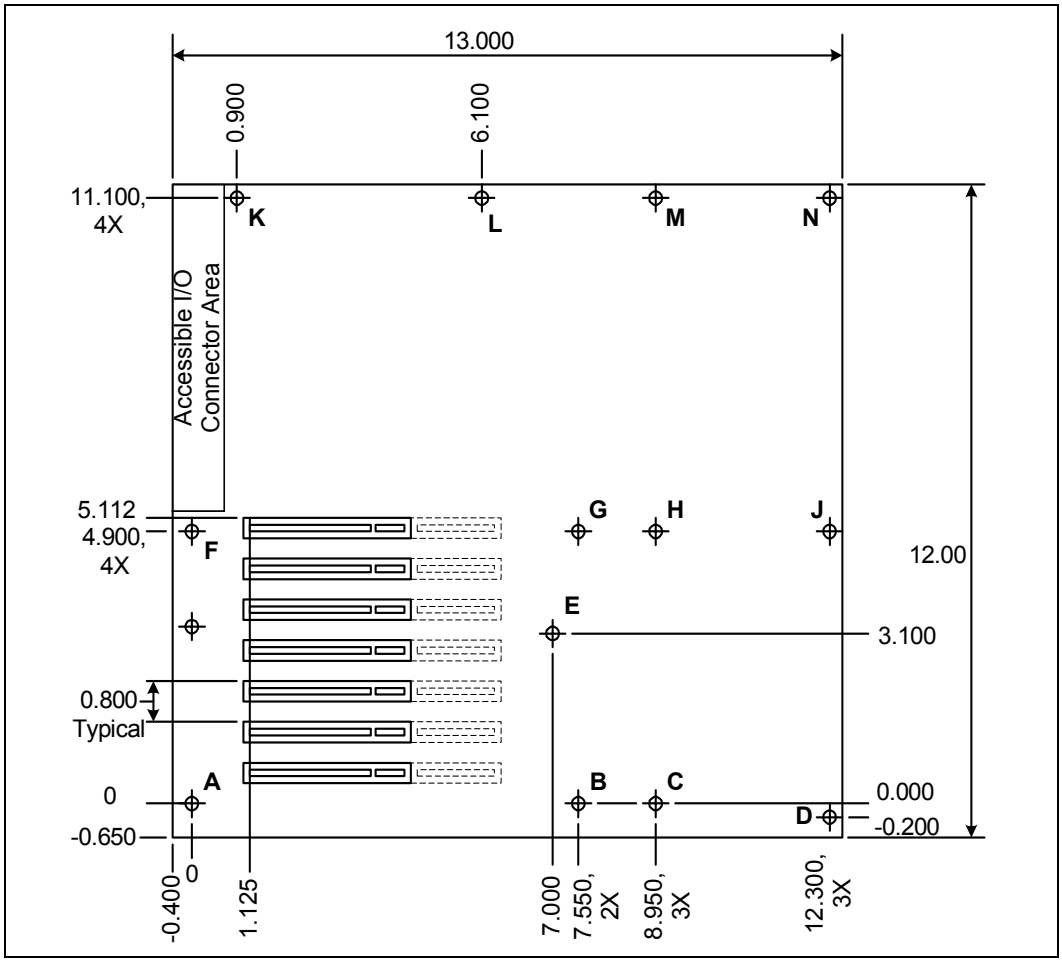
3.4 SSI Compliance

If your motherboard is intended to meet Server System Infrastructure (SSI) Specifications, it must meet a minimum set of requirements. All requirements from the *Entry-level Electronics-Bay Specification: A Server System Infrastructure (SSI) Specification for Entry Server Version 3.0* (SSI EEB) are highlighted here. Where anything conflicts with the SSI specification, the SSI specification supersedes this document.

3.4.1 Mounting Hole Placement

The SSI Specification requires that every SSI compliant chassis provides a mounting hole at each of the locations enumerated in Figure 3-5. Pedestal Server chassis typically provide stand-offs for each of these mounting holes. The baseboard manufacturer can choose to use any of the mounting holes by simply removing the un-needed stand-offs. However, in a 2U rack mount chassis, there is not enough vertical room for removable standoffs. A system integrator must work with the chassis manufacturer to ensure that mounting holes are provided for only those chosen by the baseboard.

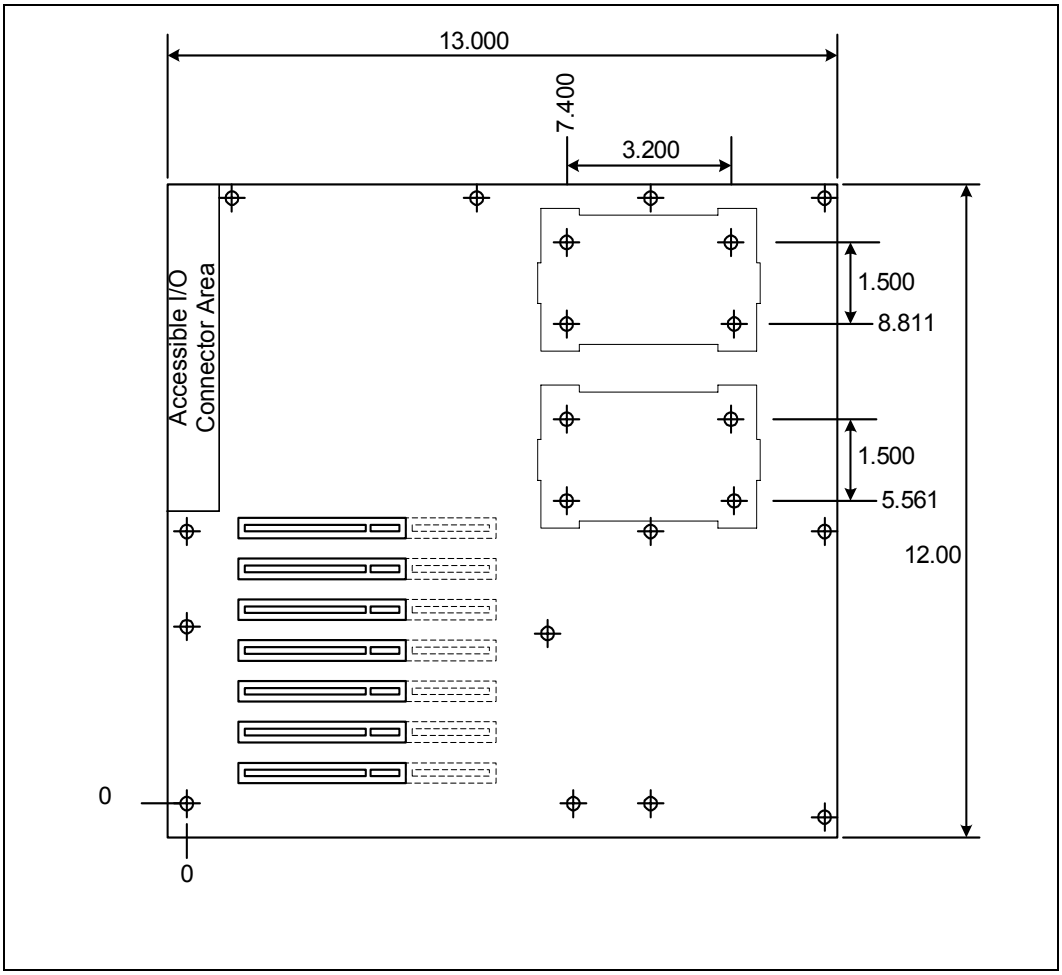
Figure 3-5. Available Baseboard Mounting Holes Supported by the Chassis



NOTE: This figure is a copy of the SSI EEB Specification version 3.0 Figure 1: Available Baseboard Mounting Holes Supported by the Chassis. All dimensions are in inches.

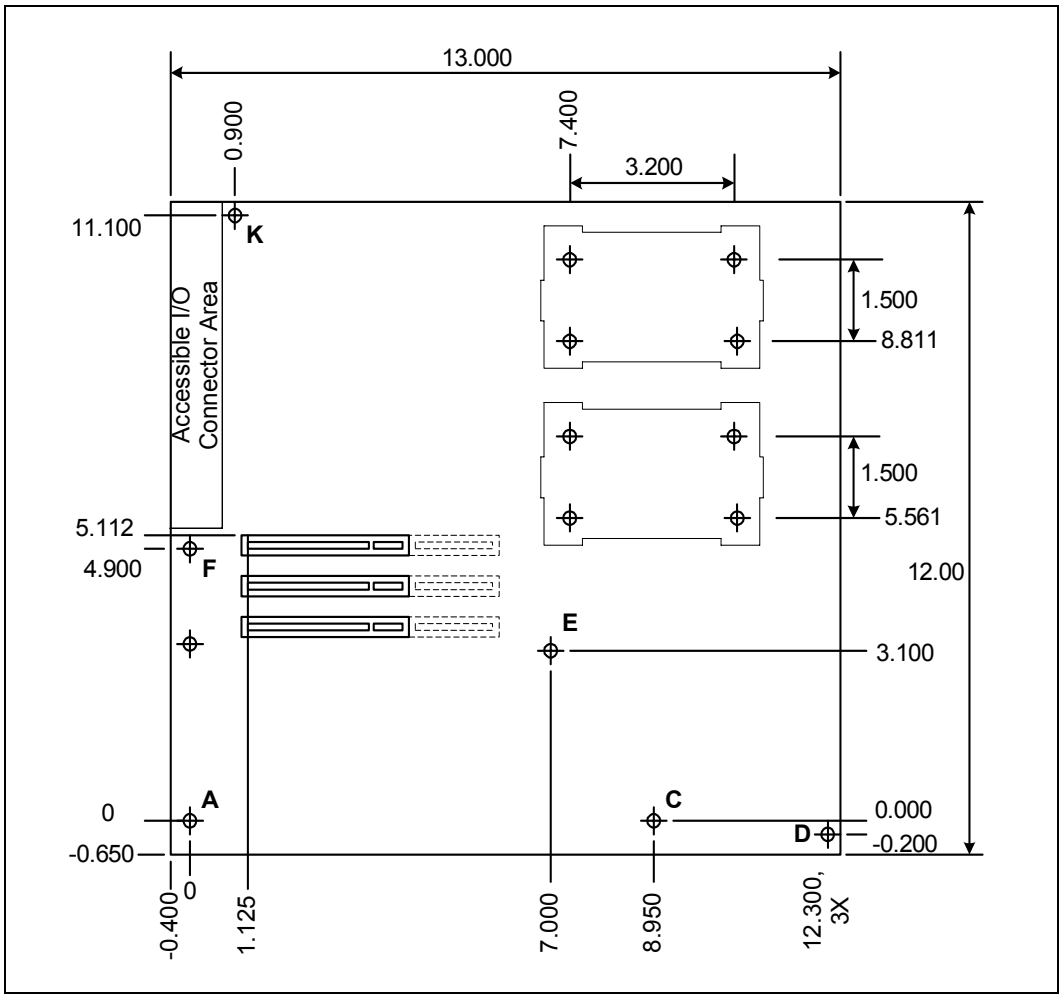
The SSI EEB specification enumerates various processor mounting locations. A board based on the Intel Xeon processor with E7501 chipset must use the hole locations as specified in Figure 3-6 (SSI EEB, Section 7.1, Figure 18). The baseboard manufacturer must work closely with the chassis manufacturer to ensure these holes are available. Figure 3-7 enumerates all holes used by the reference design.

Figure 3-6. Available Baseboard Mounting Holes Supported by the Chassis for the Processor



NOTE: This figure is a copy of the SSI EEB Specification, Version 3.0, Figure 18: Mounting Hole Option for Next Generation Intel® Xeon™ Processor Baseboards. All dimensions are in inches.

Figure 3-7. Baseboard Mounting Holes Used by Intel® E7501 Reference Board



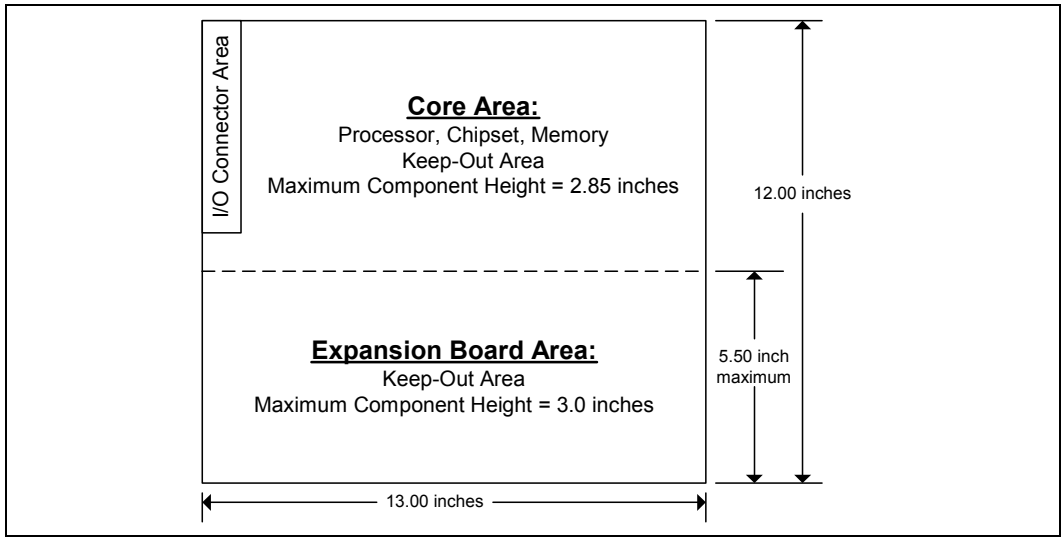
NOTE: All dimensions are in inches.

3.4.2 Volume Constraints for Typical General Purpose Baseboards

Figure 3-8 and Figure 3-9 show the minimum outer dimensions of the Electronics Bay and the height above the baseboard that must remain clear of chassis features. The keep-out height of the core area (processor, chipset, memory) is defined for high-density servers, such as, but not limited to 2U and 3U servers. These are the volumetric constraints to which the reference board is designed. To ensure the motherboard will fit within your chassis, the baseboard must fall within these constraints.

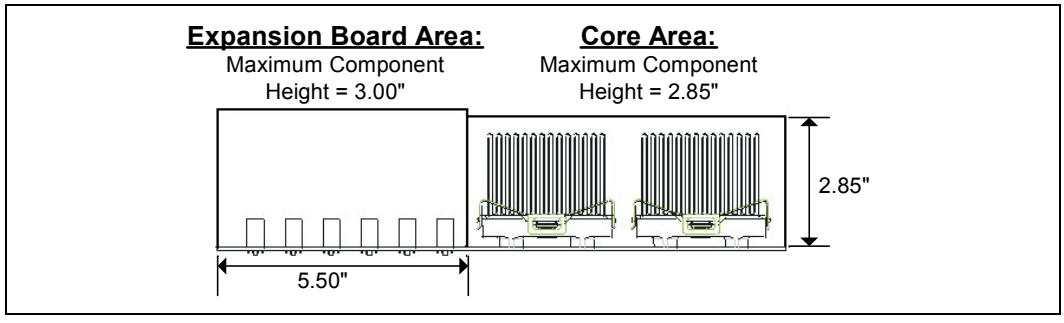
This core area keep-out zone differs from the ATX specification. Overhanging peripherals (e.g., CD-ROM drives, floppy disk drives, and hard disk drives) and chassis features must not intrude into any portion of the keep out area.

Figure 3-8. Typical Baseboard Maximum Height Restrictions



NOTE: This figure is a copy of the SSI EEB Specification version 3.0 Figure 2: Typical Baseboard Maximum Height Restrictions.

Figure 3-9. EEB Case-2: 2-Dimensional End View of a Low Profile / High-Density Server Application

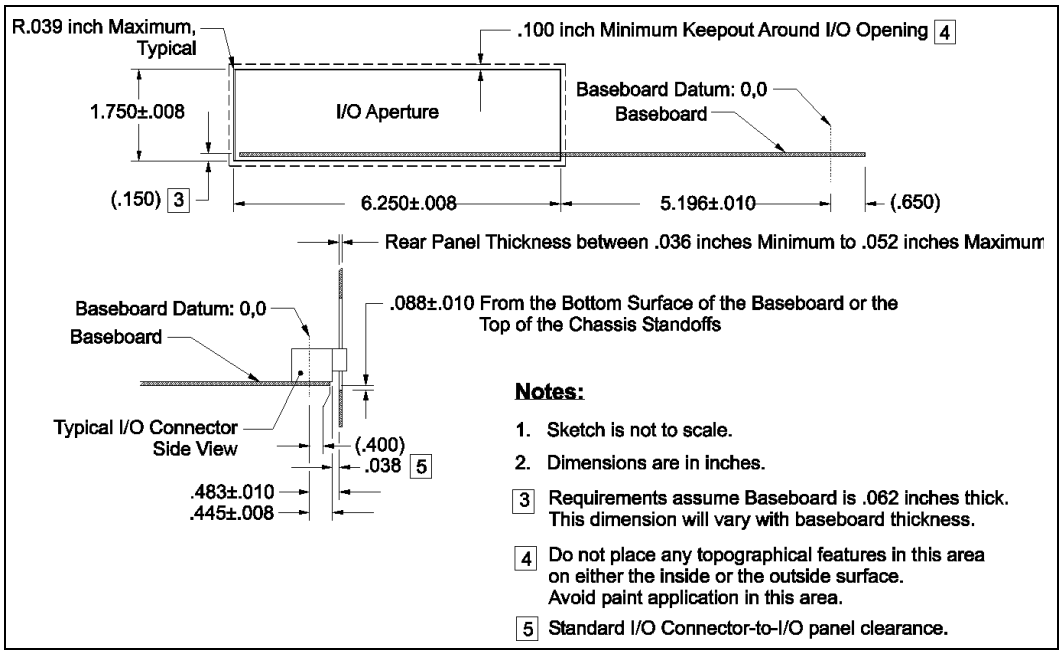


NOTE: This figure is a copy of the SSI EEB Specification, Version 3.0, Figure 6: EEB Case-2: 2-Dimensional End View of a Low Profile / High-Density Server Application.

3.4.3 Standard Cutout for Onboard I/O Ports

The Entry Electronics-Bay Specification includes the I/O aperture of the ATX 2.03 specification and uses the same dimensions. Because the same dimensions are used, a baseboard manufacturer can create just one thin metal shield for the rear I/O connectors, a shield that works in any chassis that meets this specification. This chassis-independent shield closes the Electronics-Bay, except for small openings that allow access to board-mounted connectors such as, but not limited to, network, serial, parallel, video, and mouse/keyboard. The shield provides the chassis shielding and connector grounding that a system requires to meet emissions and susceptibility regulations. Figure 3-10 shows the Electronics-Bay aperture.

Figure 3-10. Standard I/O Cutout



NOTE: This figure is a copy of the SSI EEB Specification, Version 3.0, Figure 6: Standard I/O Cutout.

3.4.4 Connectors

The SSI Spec requires that your baseboard have the following connectors: Main Power Connector, +12 Volt Power Connector, Auxiliary Signal Connector, and cooling fan connectors. All of this information is in the SSI Specification, but is presented here for convenience. This information also meets the *EPS12V Power Supply Design Guide Version 1.6*. The Power Supply Design Guide supercedes all documentation here.

3.4.4.1 Entry SSI Main Power Connector

The baseboard must have a 24-pin Molex 44472 family connector or equivalent. The header must have the pinout as enumerated in Table 3-3. The PWR OK signal has strict electrical requirements, as documented in the SSI EEB Specification, Version 3.0, Section 5.3.1.5 (Power OK).

Table 3-3. Entry SSI Main Power Connector Pinout

Pin	Signal	Pin	Signal
1	+3.3 VDC	13	+3.3 VDC
2	+3.3 VDC	14	-12 VDC
3	COM	15	COM
4	+5 VDC	16	PS ON
5	COM	17	COM
6	+5 VDC	18	COM
7	COM	19	COM
8	PWR OK	20	Rsvd
9	5 VSB	21	+5 VDC
10	+12V2 VDC	22	+5 VDC
11	+12V2 VDC	23	+5 VDC
12	+3.3 VDC	24	COM

NOTE: This table is a copy of the SSI EEB Specification, Version 3.0, Table 3: Entry SSI Main Power Connector Layout.

3.4.4.2 +12 Volt Power Connector

The baseboard must have an 8-pin Molex 44472 family connector or equivalent. The header must have the pinout as enumerated in Table 3-4. The SSI Specification dictates that the +12V3 rail on the motherboard must be separate from the +12V2 rail.

Table 3-4. Entry SSI +12 Volt Power Connector Pinout

Pin	Signal	Pin	Signal
1	COM	5	+12V1 VDC
2	COM	6	+12V1 VDC
3	COM	7	+12V1 VDC
4	COM	8	+12V1 VDC

NOTE: This table is a copy of the SSI EEB Specification, Version 3.0, Table 4: Electronics-Bay +12 Volt Power Connector Layout.

3.4.4.3 Auxiliary Signal Connector

The baseboard must have a 5-pin Molex 70545 family connector or equivalent. The header must have the pinout as enumerated in Table 3-5. The PS Alert signal has strict electrical requirements, as documented in the SSI EEB Specification, Version 3.0, Section 5.3.1.6 (PS Alert).

Table 3-5. Entry Auxiliary Signal Connector Pinout

Pin	Signal
1	SMBus Clock
2	SMBus Data
3	PS Alert
4	ReturnS
5	3.3 RS

NOTE: This table is a copy of the SSI EEB Specification, Version 3.0, Table 5: Electronics-Bay Server Signal Connector.

3.4.4.4 Cooling Fan Connector

The baseboard must have a 3-pin AMP 644953-3 connector or equivalent. The header must have the pinout as enumerated in Table 3-6.

Table 3-6. Cooling Fan Pinout

Pin	Wire Color	Signal
1	Black	COM
2	Red	Fan-V
3	Yellow	TACH

NOTE: This table is a copy of the SSI EEB Specification, Version 3.0, Table 11: Cooling Fan Pinout.

Platform Clock Routing Guidelines 4

To minimize jitter, improve routing, and reduce cost, E7500/E7501 chipset-based systems should use a single chip clock solution, the CK408B. In this configuration, the CK408B provides four, 100 MHz or 133 MHz differential outputs pairs for all of the bus agents, including the ITP connector, and five, 66 MHz speed clocks that drive all I/O buses. Figure 4-1 illustrates the clock architecture for the platform. For more information on CK408B compliance, contact your Intel representative.

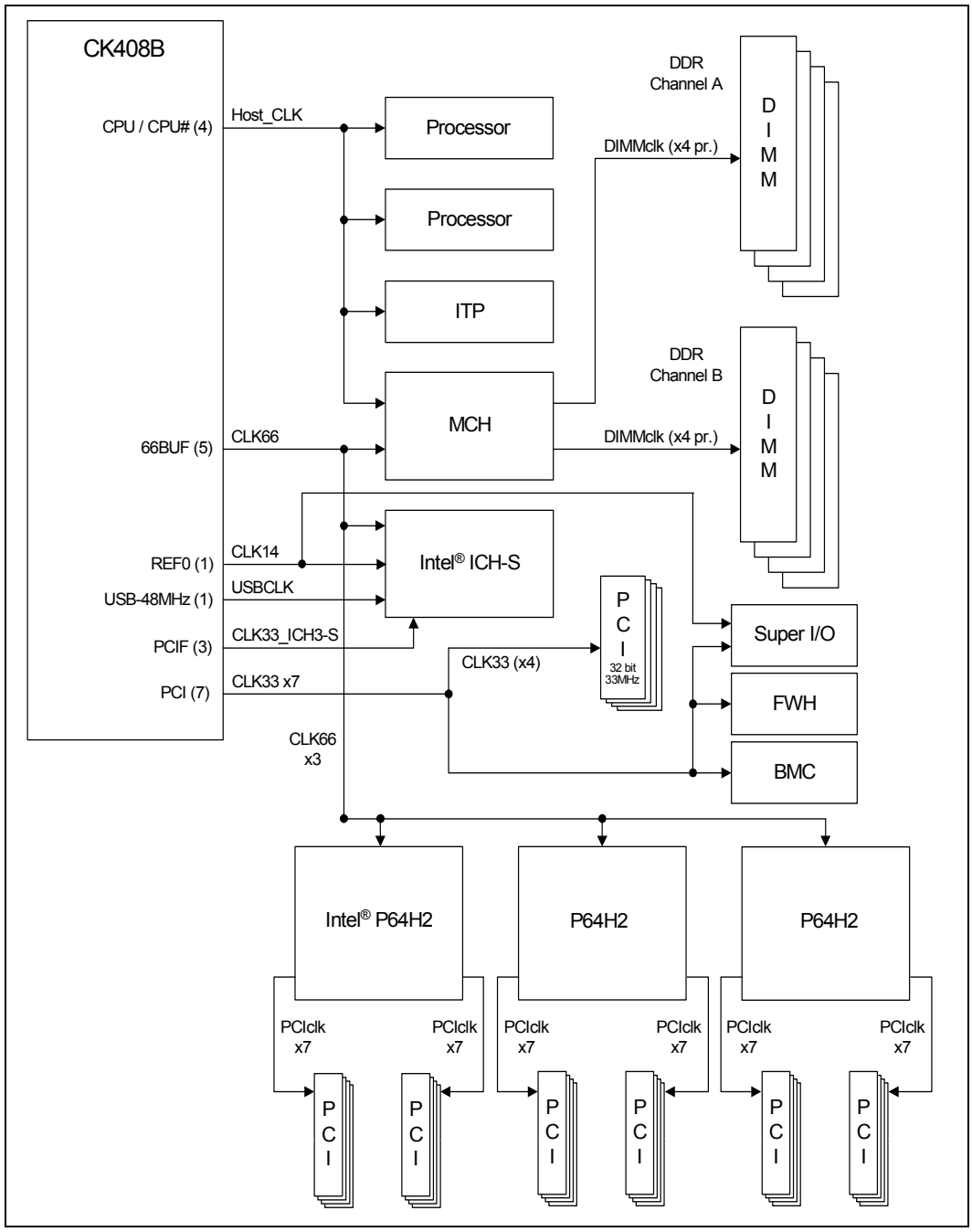
Table 4-1. CK408B Clock Groups

Clock Group Name	Frequency (MHz)	Receiver
Host_CLK	100 / 133	Processor 0, Processor 1, Debug Port, and MCH
CLK66	66	MCH, Intel® ICH3-S, and Intel® P64H2
CLK33_ICH3-S	33	ICH3-S
CLK14	14.318	ICH3-S and SIO
CLK33	33	PCI Connector, SIO, BMC, and FWH
USBCLK	48	ICH3-S

Table 4-2. Platform System Clock-Reference

Clock Group	CK-408B Pin	Component	Component Pin Name
Host_CLK	CPU#	Debug Port	BCLK[0]
	CPU	Debug Port	BCLK[1]
	CPU#	Processor 0	BCLK[0]
	CPU	Processor 0	BCLK[1]
	CPU#	Processor 1	BCLK[0]
	CPU	Processor 1	BCLK[1]
	CPU#	MCH	HCLKINP
	CPU	MCH	HCLKINN
CLK66	66BUF	MCH	66IN
		Intel® ICH3-S	CLK66
		Intel® P64H2	CLK66
CLK33_ICH3-S	PCIF	ICH3-S	PCICLK
CLK14	REF0	ICH3-S	CLK14
		SIO	CLOCKI
CLK33	PCI	PCI Connector #1	CLK
		PCI Connector #2	CLK
		PCI Connector #3	CLK
		PCI Connector #4	CLK
		PCI Connector #5	CLK
		FWH	CLK
		SIO	PCI_CLK
	PCIF	BMC	LCLK
USBCLK	USB-48MHZ	ICH3-S	CLK48

Figure 4-1. System Clocking Diagram



4.1 HOST_CLK Clock Group

The clock synthesizer provides four sets of 100/133 MHz differential clock outputs. The 100/133 MHz differential clocks are driven to the processors, the MCH, and the processors' debug port as shown in Figure 4-1.

The clock driver differential bus output structure is a "Current Mode Current Steering" output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors "Rt." The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of "R"' to match impedances or to accommodate future load requirements.

4.1.1 HOST_CLK Clock Topology

The recommended termination for the differential bus clock is a "Shunt Source Termination." Refer to Figure 4-2 for an illustration of this termination scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors "Rs" provide isolation from the clock driver's output parasitics that would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the motherboard, and Rs should be between 20 Ω and 33 Ω. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

- Mult0 pin (pin #43) is pulled high – making the multiplication factor 6.
- IREF pin (pin # 42) is connected to ground through a 475 Ω ± 1% resistor – making the IREF 2.32 mA.

Figure 4-2. Source Shunt Termination

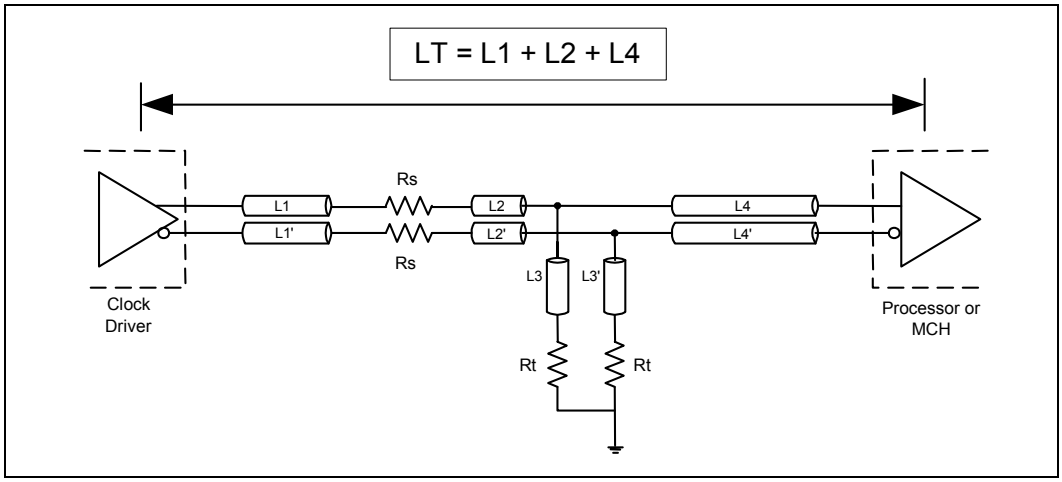


Table 4-3. HOST_CLK[1:0]# Routing Guidelines

Layout Guideline	Value	Reference	Notes
HOST_CLK Skew between Agents	300 ps total budget: 150 ps for clock driver 150 ps for interconnect	Figure 4-3	1,2,3,4
Trace Width	5 mils	Figure 4-4	7
Differential Pair Spacing	20 – 25 mils	Figure 4-4	5,6
Spacing to Other Traces	25 mils	Figure 4-4	
Serpentine Spacing	Maintain a minimum S1/h ratio of > 26/5	Section 12.3	
Motherboard Impedance – Differential	100 Ω typical		8
Motherboard Impedance – Single Ended	50 Ω ± 10%		9
Processor, ITP and MCH Routing Length – L1, L1': Clock Driver to Rs	0 – 0.5"	Figure 4-2	11
Processor, ITP and MCH Routing Length – L2, L2': Rs to Rs-Rt Node	0 – 0.2"	Figure 4-2	11
Processor, ITP and MCH Routing Length – L3, L3': Rs-Rt Node to Rt	0 – 0.2"	Figure 4-2	11
Processor, ITP and MCH Routing Length – L4, L4': Rs-Rt Node to Load	0 – 20"	Figure 4-2	12
Processor to MCH Length Matching (LT)	0.044" ± 0.025" MCH LT must be 0.044" shorter than processor LT.	Figure 4-2	10
Processor to Processor Length Matching (LT)	± 25 mils	Figure 4-2	13
Processor to ITP Length Matching (LT)	See ITP700 Port Design Guide	Figure 4-2	14
HOST_CLKn – HOST_CLKn# Differential Pair Length Matching	± 25 mils		
Rs Series Termination Value	20 – 33 Ω ± 5%	Figure 4-2	
Rt Shunt Termination Value	49.9 Ω ± 1% (for 50 Ω board impedance)	Figure 4-2	

NOTES:
1. The skew budget includes clock driver output pair to output pair jitter (differential jitter) and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on a single layer and routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two-bus agents. Measured at the crossing point.
5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing because this degrades the noise rejection of the network.
7. Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack-up.
8. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1-2*Kb) where Kb is the backwards cross-talk coefficient. For the recommended trace spacing, Kb is very small, and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the HOST_CLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.

10. Length compensation for the processor socket and package delay is included in chipset routing to match electrical lengths between the chipset and the processor from the die pad of each.
11. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ringback.
12. Do not change routed layers. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er and the impedance variations due to physical tolerances of circuit board material.
13. Length of LT for one processor must match the LT of all other HOST_CLK traces to other processor with specified tolerance.
14. If ITP is implemented, ITP HOST_CLK lengths need to be length matched to the processor HOST_CLK lengths as specified in the *ITP700 Debug Port Design Guide*.

Figure 4-3. Clock Skew As Measured from Agent to Agent

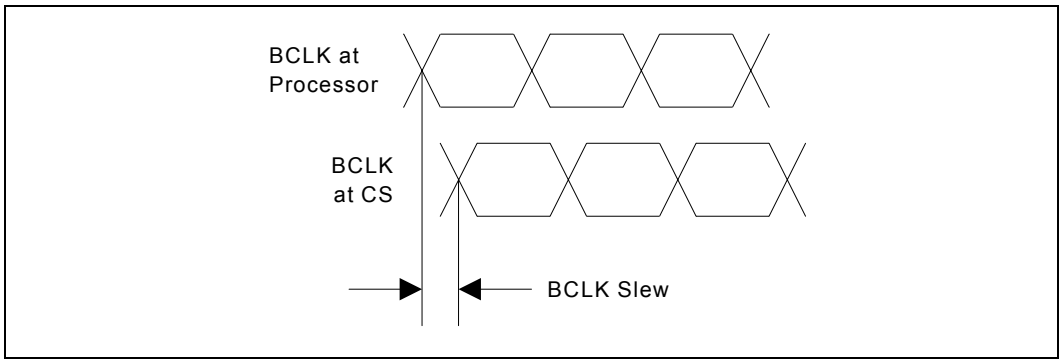
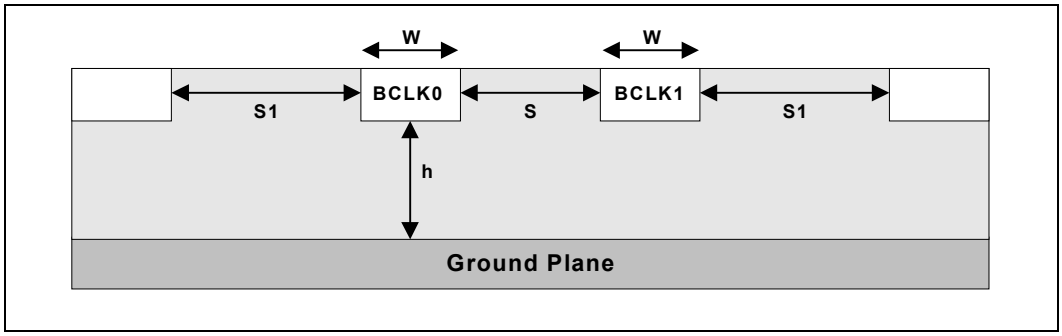


Figure 4-4. Trace Spacing for HOST_CLK Clocks



4.1.2 HOST_CLK General Routing Guidelines

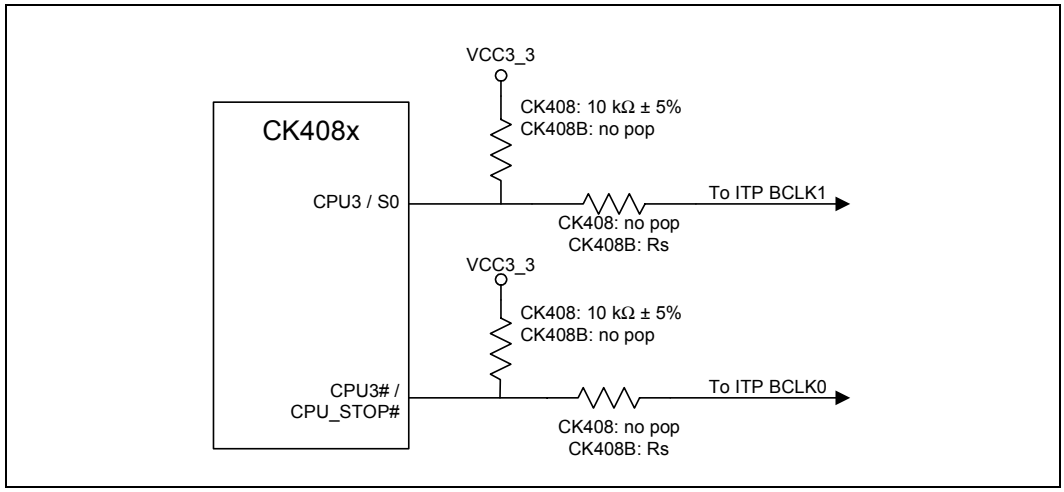
- When routing the differential clocks, do not split up the two halves of a differential clock pair between layers. Route to all agents on the same physical routing layer referenced to ground.
- Do not change routed layers. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er and the impedance variations due to physical tolerances of circuit board material.
- Do not place vias between adjacent complementary clock traces, and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

4.1.3 CK408 vs. CK408B Requirement

The CK408 and CK408B are pin compatible. The only difference between the two chips is the CK408B replaces two signals on the CK408 with a fourth HOST_CLK pair for the In Target Probe (ITP) and is preferred by board designers for preliminary testing and validation. The CK408 requires pull-up resistors on the additional clock pair while the CK408B pins need to be connected to the ITP.

- Add one 10 kΩ ± 5% pull-up resistor close to the clock driver before the 33 Ω ± 5% (Rs) (see Figure 4-5) series resistor on each ITP signal trace (CPU3, CPU3#). This would give the option to use the CK408 instead of the CK408B.
- When using only a CK408, the 10 kΩ ± 5% pull-up resistor is the only necessary part.

Figure 4-5. Stuffing Options for CK408 and CK408B



4.2 CLK66 Clock Group

In the CLK66 clock group, the driver is the clock synthesizer 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the MCH, ICH3-S, and P64H2.

Figure 4-6. Topology for CLK66

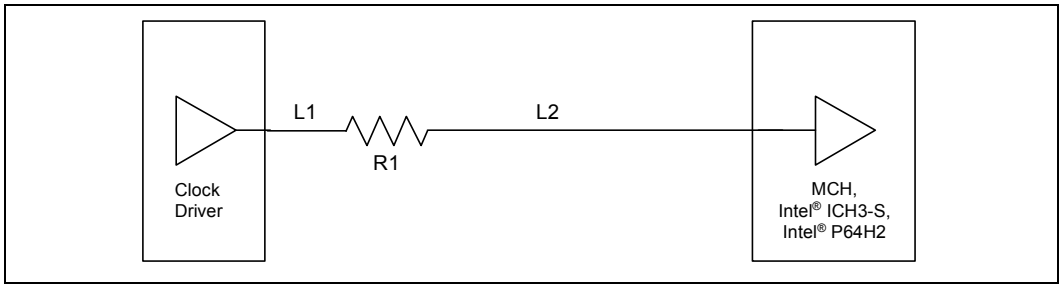


Table 4-4. CLK66 Routing Guidelines

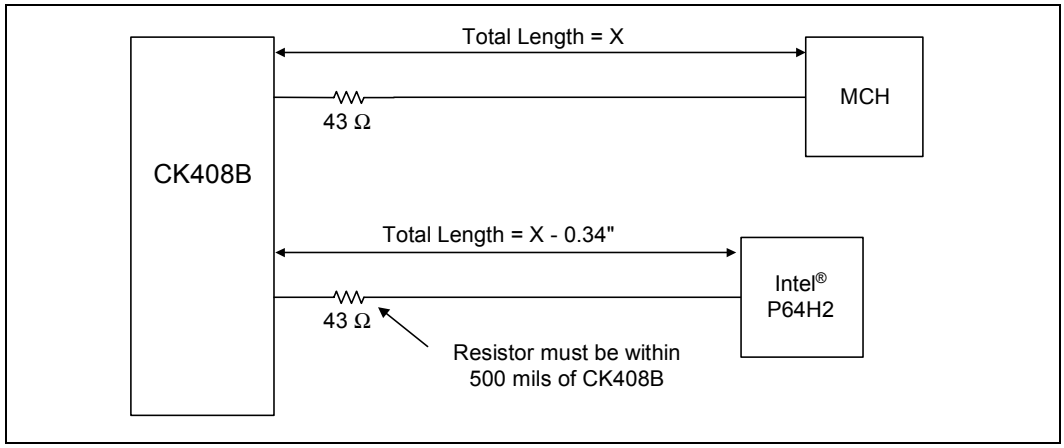
Parameters	Routing Guidelines
Clock Group	CLK66
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	5 mils
Trace Spacing	25 mils
Trace Length – L1	0.00” – 0.50”
Trace Length – L2	3.00” – 9.0”
Resistor	R1 = 43 Ω ± 5%
Skew Requirements	All the clocks in the CLK66 group must have < 100-mil skew between each other.
Clock Driver to MCH	X = (3” – 9.5”)[1], where X = L1 + L2
Clock Driver to ICH3-S	X = (3” – 9.5”)[1], where X = L1 + L2
Clock Driver to P64H2	X – 0.34” [2], where X = L1 + L2

NOTES:
1. For better understanding of the concept, refer to Section 4.2.1, Figure 4-7, and Figure 4-8.
2. Assuming no connector.

4.2.1 CLK66 Skew Requirements

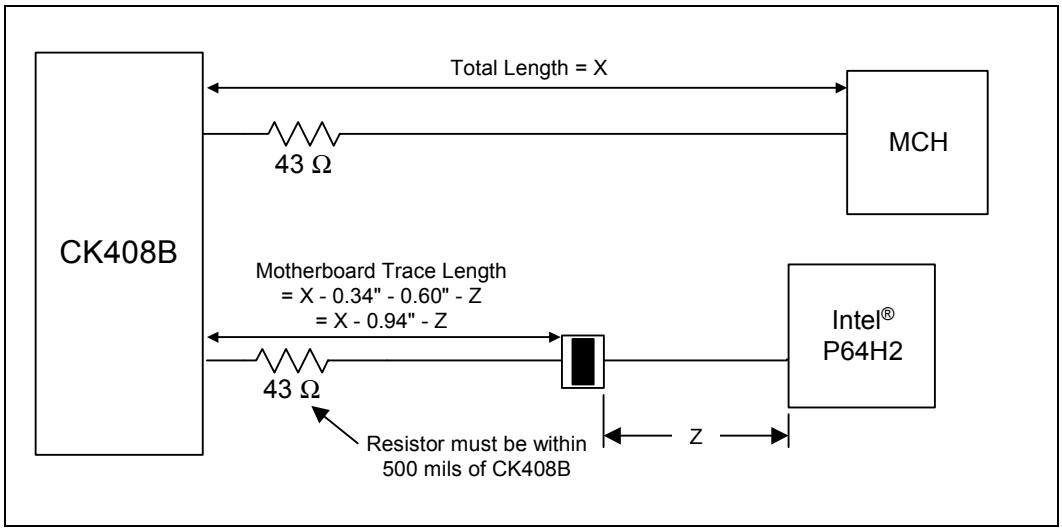
Traces going to the P64H2 could have up to **two** connectors. Designers should keep in mind that all Total Lengths are referenced to the MCH length ("X") and assume no connector. Each connector is equivalent to 0.60 inch of trace. Adding a single connector on the P64H2 trace would reduce the motherboard trace length by the card length **"Z"** to **X – 0.34" – 0.60" – Z = X – 0.94" – Z** (refer to Figure 4-8). In addition, some OEMs might consider having the components on a riser, in which case the riser card trace length designator "**Y"** should also be accounted for as yet another factor. In this case the last equation would become **X – 0.34" – 0.60"– Z – 0.60"– Y = X – 1.54"–Y – Z** (refer to Figure 4-9). Note that if a riser is used, the motherboard clock trace must be designed for the specific riser card trace length and connector.

Figure 4-7. Clock Skew Requirements



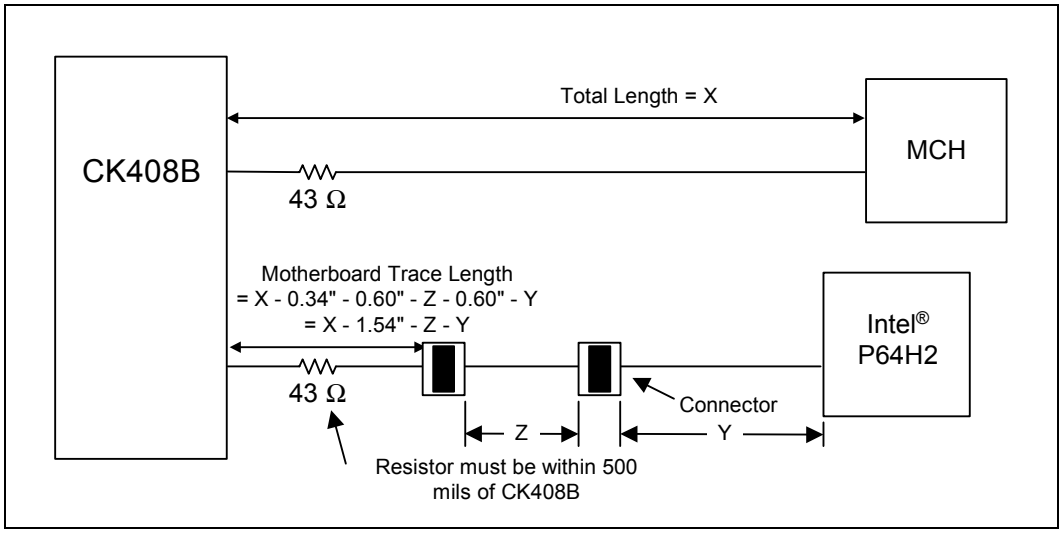
NOTES:
1. All lengths must be matched within 100 mils of target length.
2. 66 MHz clock lines routed with 25-mils isolation from any other signal.
3. Length from CK408B to MCH must be between 3 inches and 9.5 inches.

Figure 4-8. Example of Adding a Single Connector



NOTES:
1. All lengths must be matched within 100 mils of target length.
2. 66 MHz clock lines routed with 25-mils isolation from any other signal.
3. Length from CK408B to MCH must be between 3 inches and 9.5 inches.
4. Each connector is equivalent to ~ 0.60 inch of trace.
5. Z is the card trace length.

Figure 4-9. Example of Adding Two Connectors and/or a Riser



NOTES:
1. All lengths must be matched within 100 mils of target length.
2. 66 MHz clock lines routed with 25-mils isolation from any other signal.
3. Length from CK408B to MCH must be between 3 inches and 9.5 inches.
4. Each connector is equivalent to ~ 0.60 inch of trace.
5. Z is the card trace length.
6. Each riser is equivalent to ~0.60 + Y where Y is the riser card trace length.
7. The riser must be built with the CLK66 trace length matched to the motherboard routed length.

4.3 CLK33_ICH3-S Clock

In the CLK33_ICH3-S case, the driver is the clock synthesizer PCIF 33 MHz clock output buffer, and the receiver is the PCICLK 33 MHz clock input buffer at the ICH3-S. Care must be taken to length match this 33 MHz clock with the ICH3-S 66 MHz clock.

Figure 4-10. Topology for CLK33_ICH3-S

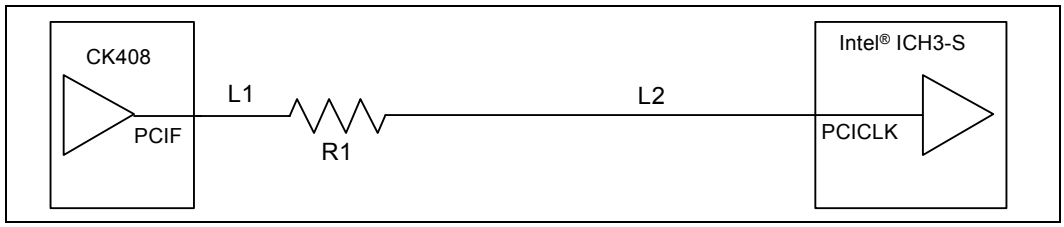


Table 4-5. CLK33_ICH3-S Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK33_ICH3-S
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	5 mils
Trace Spacing	25 mils
Trace Length – L1	0.00” – 0.50”
Trace Length – L2	3.00” – 9.0”
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	Must be matched to ± 100 mils of CLK66

4.4 CLK33 Clock Group

For the CLK33 clock group, the driver is the clock synthesizer 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer at the PCI devices on the PCI cards.

Figure 4-11. Topology for CLK33 to PCI Device Down

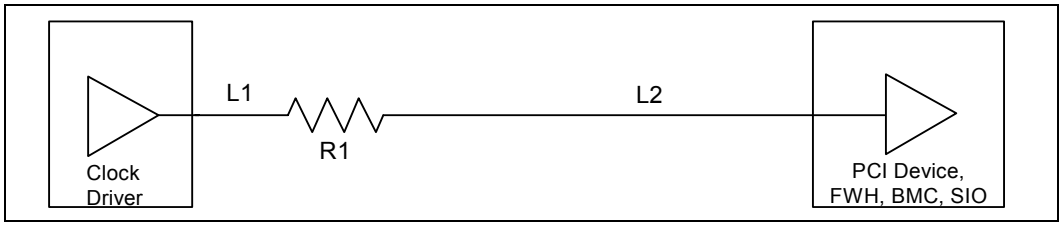


Table 4-6. CLK33 Routing Guidelines for PCI Device Down

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	5 mils
Trace Spacing	25 mils
Trace Length – L1	0.00” – 0.50”
Trace Length – L2	3.00” – 9.0”
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	PCI device – PCI device skew max allowed by *PCI Local Bus Specification, Rev 2.2* is 2 ns. Therefore, length match with other CLK33 signals within ± 1 ns.

Figure 4-12. Topology for CLK33 to PCI Slot

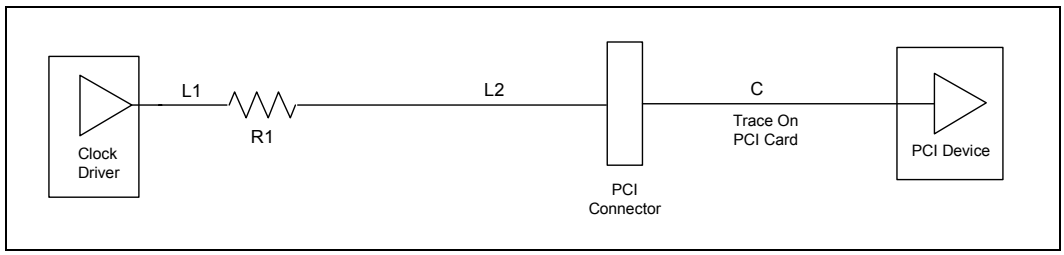


Table 4-7. CLK33 Routing Guidelines for PCI Slot

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length – L1	0.00” – 0.50”
Trace Length – L2	3.00” – 9.0”
Trace Length – C	Routed 2.50” per *PCI Local Bus Specification, Rev 2.2*
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	PCI device – PCI device skew max allowed by *PCI Local Bus Specification, Rev 2.2* is 2 ns. Therefore, length match with other CLK33 signals within ± 1 ns.
Maximum Via Count Per Signal	1

4.5 CLK14 Clock Group

The driver in the CLK14 clock group is the clock synthesizer 14.318 MHz clock output buffer (pin REF0), and the receiver is the 14.318 MHz clock input buffer at the ICH3-S, SIO, and LPC.

Figure 4-13. Topology for CLK14

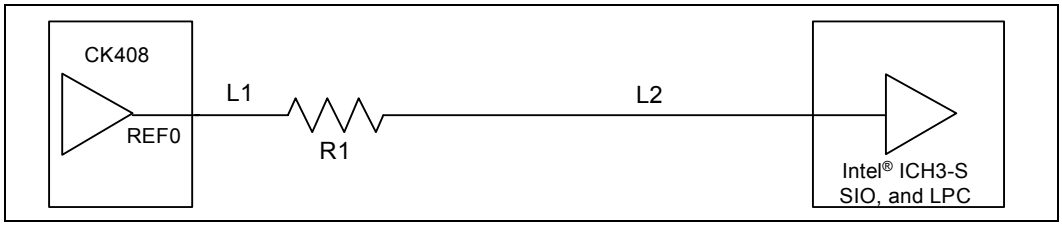


Table 4-8. CLK14 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	5 mils
Trace Spacing	10 mils
Trace Length – L1	0.00” – 0.50”
Trace Length – L2	3.00” – 9.0”
Resistor	R1 = 22 Ω ± 5%
Skew Requirements	None

4.6 USBCLK Clock Group

For the USBCLK clock group, the driver is the clock synthesizer USB clock output buffer (pin USB-48MHz), and the receiver is the USB clock input buffer at the ICH3-S (pin CLK48). Note that this clock is asynchronous to any other clock on the board.

Figure 4-14. Topology for USB_CLK

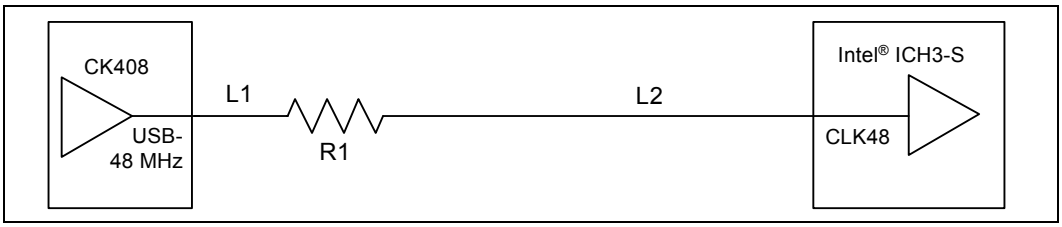


Table 4-9. USBCLK Routing Guidelines

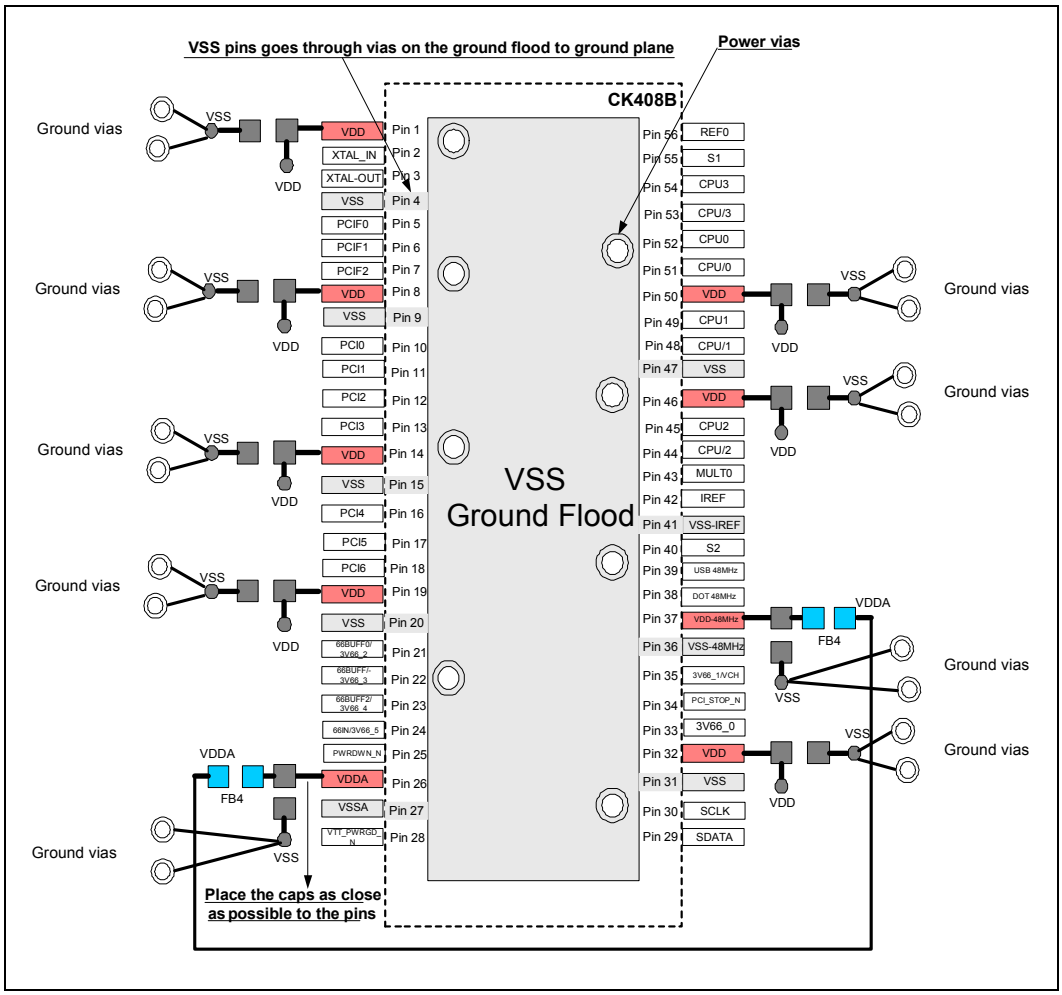
Parameter	Routing Guideline
Clock Group	USBCLK
Topology	Point-to-Point
Reference Plane	Ground referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	5 mils
Trace Spacing	25 mils
Trace Length – L1	0.00” – 0.50”
Trace Length – L2	3.00” – 12.00”
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	None – USBCLK is asynchronous to any other clock on the board
Maximum Via Count	2

4.7 Clock Driver Decoupling

The decoupling requirements for a CK408B compliant clock synthesizer are as follows:

- One, 22 µF polarized (decoupling) capacitor placed close to the VDD generation circuitry.
- Eleven, 0.1 µF high-frequency decoupling capacitors placed close to the VDD pins on the clock driver.
- Three, 0.1 µF high-frequency decoupling capacitors placed close to the VDDA pins on the clock driver.
- One, 10 µF polarized (decoupling) capacitor placed close to the VDDA pins on the clock driver.
- One, 0.1 µF high-frequency decoupling capacitor placed close to the VDDA generation circuitry.
- All decoupling capacitors should be placed close to the clock driver pins. Refer to Figure 4-15.

Figure 4-15. Decoupling Capacitors Placement and Connectivity



4.8 Clock Driver Power Delivery

Designers must take special care to provide a quiet VDDA supply to the Ref VDD, VDDA and the 48 MHz VDD. These VDDA signals are especially sensitive to switching noise induced by the other VDDs on the clock chip. They are also sensitive to switching noise generated elsewhere in the system such as the processor voltage regulator. It is recommended that a ground flood be placed directly under the clock chip to provide a low impedance connection for the VSS pins. In addition, power vias should be distributed evenly throughout the ground flood.

Note: For all power connections to planes, decoupling capacitors, and vias, the maximum trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.

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System Bus Routing Guidelines 5

This chapter covers the system bus source synchronous (data, address, and associated strobes) and common clock signal routing. Table 5-1 lists the signals and their corresponding signal types.

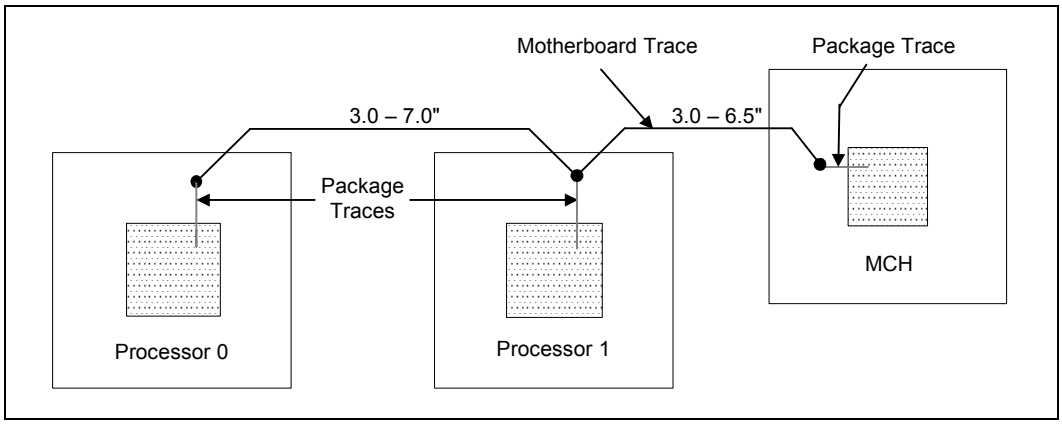
Table 5-1. System Bus Signal Groups

Signal Group	Type	Signals
AGTL+ Common Clock Input	Synchronous to BCLK	BPRI#, BR[3:1]#[1,2], DEFER#, RESET#[1,6], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK	ADS#, AP[1:0]#, BINIT#[3], BNR#[3], BPM[5:0]#[1,6], BR0#[1], DBSY#, DP[3:0]#, DRDY#, HIT#[3], HITM#[3], LOCK#, MCERR#[3]
AGTL+ Source Synchronous I/O: 4X Group	Synchronous to assoc. strobe	D[63:0]#, DBI[3:0]#
AGTL+ Source Synchronous I/O: 2X Group	Synchronous to assoc. strobe	A[35:3]#[4], REQ[4:0]#
AGTL+ Strobes	Synchronous to BCLK [1:0]	ADSTB[1:0]#, DSTBN[3:0]#, DSTBP[3:0]#
Asynchronous GTL+ Input[1]	Asynchronous	A20M#, IGNNE#, INIT#[4], LINT0/INTR, LINT1/NMI, SMI#[4], CPUSLP#, STPCLK#
Asynchronous GTL+ Output[1]	Asynchronous	FERR#/PBE#, IERR#, PROCHOT#, THERMTRIP#
System Bus Clock	Clock	BCLK0, BCLK1
TAP Input[6]	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output[6]	Synchronous to TCK	TDO
SMBus Interface[1,7]	Synchronous to SM_CLK	SM_EP_A[2:0], SM_TS_A[1:0], SM_DAT, SM_CLK, SM_ALERT#, SM_WP
Power/Other	Power/Other	BSEL[1:0], GTLREF[3:0], COMP[1:0], ODTEN, PWRGOOD, RESERVED, SKTOCC#, SMB_PRT[7], TESTHI[6:0], THERMDA[7], THERMDC[7], VID[4:0], VID_VCC[5,7], VCC_CPU, SM_VCC[5], VCCA, VSSA, VCCIOPLL, VSS, VCCSENSE, VSSSENSE

NOTES:
1. These signals do not have on-die termination on the processor. They must be terminated properly on the motherboard. If the signal is not connected, it must be pulled to the appropriate voltage level through a 1 kΩ ± 5% resistor.
2. Intel Xeon processors use only BR0# and BR1#.
3. The processor uses these signals as 'wired-OR'. They may be driven simultaneously by multiple agents.
4. The value of these pins during the active edge of RESET# determine processor configuration options.
5. SM_VCC/VID_VCC has critical power sequencing requirements documented in Section 11.2.6.
6. Critical terminations and routing for RESET#, BPM[5:0]#, TAP signals and all debug port signals are found in the *ITP700 Debug Port Design Guide*.
7. These signals are only defined and driven by the Intel Xeon processor with 533 MHz system bus.

The dual-processor topology requires that the MCH be at one end of the bus, Processor 0 be at the other end of the bus, and Processor 1 be in the middle of the bus (Figure 5-1). The motherboard routing to Processor 1 must not create a stub on the system bus signals at the socket. This requires routing into the socket and back out of the socket. For Uni-Processor (UP) operation, the single processor must be installed in the Processor 0 socket, at the end of the bus. Figure 5-1 shows the recommended dual processor topology used for system bus routing.

Figure 5-1. Dual Processor System Bus Topology



Refer to Table 5-2 for a summary of the dual-processor system bus routing recommendations. Use this as a quick reference only. The following sections provide more detailed information for each parameter. Intel strongly recommends simulation of all signals to ensure the design meets setup and hold times.

Table 5-2. System Bus Routing Summary

Parameter	Platform Routing Guidelines
Trace Width/Spacing	• 5/15 mils. • Serpentine ratio of 5:1. See Section 12.3.
2X and 4X Signal Group	• MCH-to-Processor: 3.0 inches– 6.5 inches pin-to-pin. • Processor-to-Processor: 3.0 inches– 7.0 inches pin-to-pin. • Total bus length must not exceed 13.5 inches. • Balance trace lengths ± 25 mils with respect to the associated strobes (see Table 5-4) between agents to compensate for the stub created by the processor package. Use a Signal Integrity Adjustment Factor of 0.78. See Section 12.6 for a detailed description of processor bus tuning. • Route all signals within the same strobe group on the same layer for the entire length of the bus. • Never change layers on 2X and 4X signals. • Never route over a plane split.
DSTBN[3:0]# / DSTBP[3:0]# and ADSTB[1:0]#	• Follow the same routing rules as the 2X and 4X Signal Group. • Maintain a 25-mil spacing around each strobe signal. • Do not route differentially.
Common Clock Signal	• Follow the same routing rules as the 2X and 4X Signal Group; however, no length compensation is necessary. • If a layer change must occur, use vias connecting the two reference planes to provide a low impedance path for the return current. Vias should be as close as possible to the signal via.
Topology	• Daisy chain with the chipset at one end of the system bus and Processor 0 at the other. • End processor must have on-die termination enabled.
Routing Requirements	• No motherboard contribution to stub length of middle processor (35-mil max trace via to pad). • Stripline, ground referenced only.
Motherboard Impedance	• 50 Ω ± 10%

5.1 Routing Guidelines for the AGTL+ Source Synchronous 2X and 4X Groups

The 4X group of signals uses four times the frequency of the base clock: 400 MHz or 533 MHz. The 2X group uses twice the frequency of the base clock: 200 MHz or 266 MHz. The 2X and 4X signals are listed in Table 5-3. Table 5-4 defines the 2X and 4X signals with their associated strobes.

Table 5-3. 2X and 4X Signal Groups

2X Group	4X Group
A[35:3]# REQ[4:0]#	HD[63:0]# DBI[3:0]#

Table 5-4. Source Synchronous Signals with the Associated Strobes

Signals	Associated Strobe
REQ[4:0]#, HA[16:3]#	ADSTB0#
A[35:17]#	ADSTB1#
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#

Routing guidelines for the 2X and 4X signal groups are given in Table 5-2. All 2X and 4X signals of the same group (refer to Table 5-4) must be routed within ± 25 mils of the same length between agents and within ± 50 mils of the entire length of the bus on the same layer.

Warning: *AGTL+ Source Synchronous 2X and 4X signals must never change layer: always route the signal on the same layer for the entire length of the bus.*

5.2 Routing Guidelines for Common Clock Signals

Table 5-5 lists the common clock signals.

Table 5-5. AGTL+ Common Clock I/O Signals

Signal Types	Signals
Input	BPRI#, BR[3:1]#, DEFER#, RESET#[1], RS[2:0]#, RSP#, TRDY#
I/O	ADS#, AP[1:0]#, BINIT#, BNR#, BR0#, DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#

NOTES:
1. RESET# has additional requirements in the *ITP700 Debug Port Design Guide*.

Route the common clock signals according to the processor system bus topology shown in Figure 5-1. Routing guidelines for the common clock signal group are in Table 5-2. Route the traces with at least 50% of the trace width directly over a reference plane. Common clock signals may change layers.

5.2.1 Wired-OR Signals

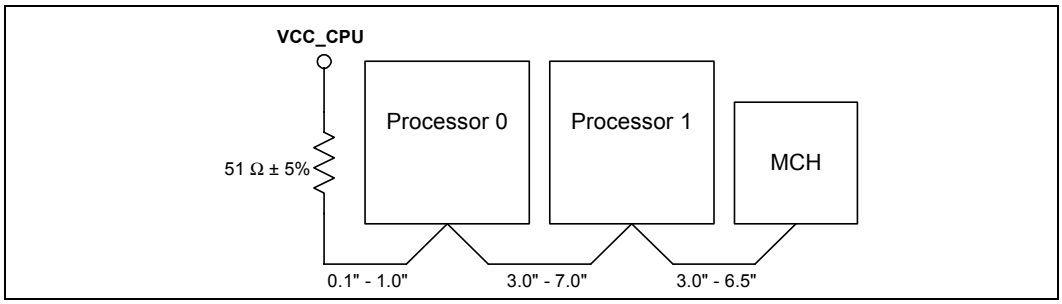
The "wired-OR" signals are HIT#, HITM#, MCERR#, BINIT#, and BNR#. These signals differ from the other system bus signals in that more than one agent can be driving the signal at the same time. Intel recommends that special attention be given to the routing of these signals in adherence to the layout guidelines presented in Table 5-2. Timing and signal integrity must be met for the cases where one agent is driving, all agents are driving, and any combination of agents are driving.

The wired-OR signals should follow the same routing rules as the common clock signals. Intel recommends that simulations for these signals be performed for each system.

5.2.2 RESET# Topology

Since the processor does not contain on-die termination for the RESET# input signal, these additional layout guidelines for the RESET# signal are required. The baseboard trace length from Processor 0's pin to the termination resistor should be 0 to 1 inch. Follow the same routing guidelines given for common clock signals listed above in this same section.

Figure 5-2. RESET# Topology



NOTES:
1. Trace Z_0 = 50 Ω
2. Trace spacing = 10 mil

If ITP is implemented, see the *ITP700 Debug Port Design Guide* for the correct implementation.

5.2.3 BR[3:0]# Routing Guidelines

Connect BR[3:0]# as shown in Figure 5-3. The total bus length must be less than 20.2 inches. BR3# and BR2# are not used and are pulled to VCC_CPU. The designer may pull-up BR[3:2] independantly instead of tying the lines between the processors.

Figure 5-3. BR[3:0]# Connection for DP Configuration

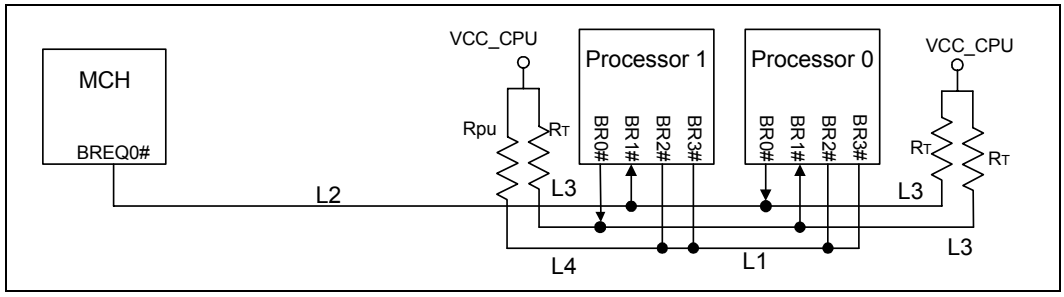


Table 5-6. BR[3:0]# Connection

Trace Impedance	L1 Processor-to-Processor	L2 Processor1 BR1# to MCH	L3 Processor-to-R_T Stub	L4 Processor-to-R_{PU} Stub	R_T	R_{PU}
50 Ω	3.0 – 10.0”	15.7” max	1” max	3” max	50 Ω ± 5%	50 Ω ± 5%

5.3 Routing Guidelines for Asynchronous GTL+ and Miscellaneous Signals

Table 5-7 enumerates the remainder of the processor signals discussed in this document.

Table 5-7. Asynchronous GTL+ and Miscellaneous Signals

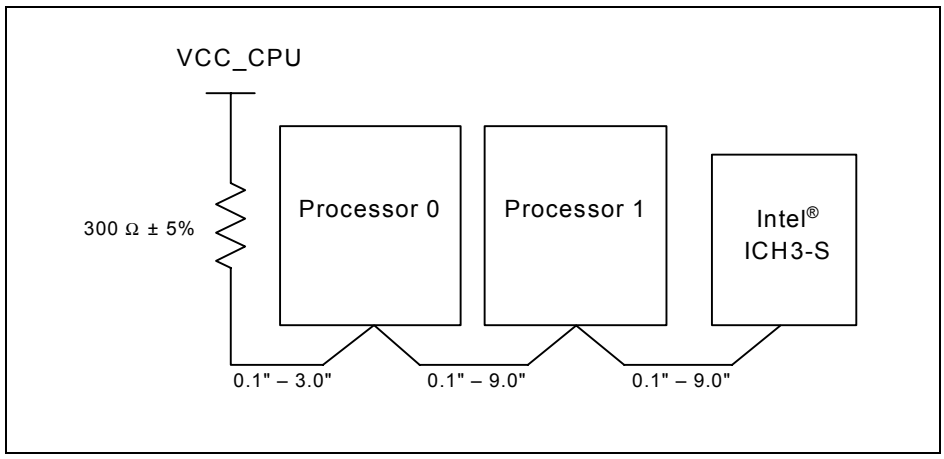
Signal Name	Type	Processor I/O Type	Driven By	Received By
A20M#	Async GTL+	I	Intel® ICH3-S	Processor
BSEL[1:0]	Other	O	Processor	External Logic
COMP[1:0]	Analog	I	Pull-down	Processor
FERR#/PBE#	Async GTL+	O	Processor	ICH3-S
IERR#	Async GTL+	O	Processor	External Logic (such as Baseboard Management Controller)
IGNNE#	Async GTL+	I	ICH3-S	Processor
INIT#	Async GTL+	I	ICH3-S	Processor
LINT[1:0]	Async GTL+	I	ICH3-S	Processor
ODTEN	Other	I	Pull-up / Pull-down	Processor
PROCHOT#	Async GTL+	O	Processor	External Logic
PWRGOOD	Other	I	External Logic	Processor
SLP#	Async GTL+	I	ICH3-S	Processor
SM_ALERT#[1]	SMBUS (3.3 V)	O	Processor/Controller	Controller
SM_CLK[1]	SMBUS (3.3 V)	I/O	Processor/Controller	Processor/Controller
SM_DAT[1]	SMBUS (3.3 V)	I/O	Processor/Controller	Processor/Controller
SM_EP_A[2:0][1]	SMBUS (3.3 V)	I	Pull-up / Pull-down	Processor
SM_TS_A[1:0][1]	SMBUS (3.3 V)	I	Pull-up / Pull-down	Processor
SM_WP[1]	SMBUS (3.3 V)	I	External Logic	Processor
SMI#	Async GTL+	I	ICH3-S	Processor
STPCLK#	Async GTL+	I	ICH3-S	Processor
THERMDA	Other	O	Processor	Thermal Sensor
THERMDC	Other	O	Processor	Thermal Sensor
THERMTRIP#	Async GTL+	O	Processor	External Logic
VCCA	Power	I	RLC Filter Circuit	Processor
VCCIOPLL	Power	I	RLC Filter Circuit	Processor
VCCSENSE	Other	O	Processor	Test Point
VID[4:0]	Other	O	Processor	Voltage Regulator
GTLREF	Power	I	Pull-up / Pull-down	Processor/MCH
VSSA	Power	I	RLC Filter Circuit	Processor
VSSSENSE	Other	O	Processor	Test Point

NOTES:
1. These signals only exist on the Intel Xeon processor with 512-KB L2 cache (INT-mPGA package).

5.3.1 Power Good

Follow the topology shown in Figure 5-4 when routing power good. Connect the processor PWRGOOD pin to the ICH3-S CPUPWRGD pin. You may choose to isolate power good for each voltage regulator and processor pair to recognize individual voltage regulator failures.

Figure 5-4. Topology for PWRGOOD (CPUPWRGOOD)

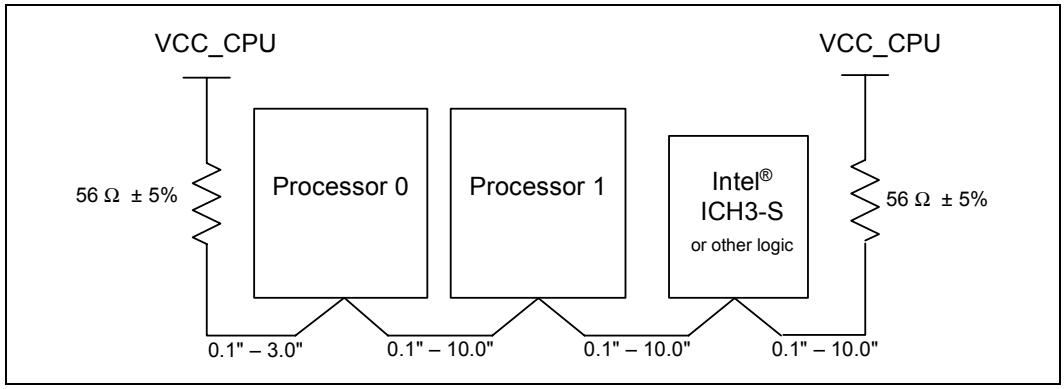


NOTES:
1. Trace Z_0 = 50 Ω
2. Trace spacing = 10 mil

5.3.2 Asynchronous GTL+ Signals Driven by the Processor

Follow the topology shown in Figure 5-5 when routing FERR#/PBE#, IERR#, PROCHOT# and THERMTRIP#. This topology shows these signals connected in a "wired-OR" configuration, however, special routing consideration is not required if the layout guidelines in this section are followed. Note that FERR#/PBE# is the only signal in this group that connects the processors to the ICH3-S. IERR#, PROCHOT# and THERMTRIP# connect to other motherboard logic (e.g., the Baseboard Management Controller) and may need voltage translation logic, depending on the motherboard receiver logic devices used. Do not route a stub when routing to the processors.

Figure 5-5. Topology for Asynchronous GTL+ Signals Driven by the Processor

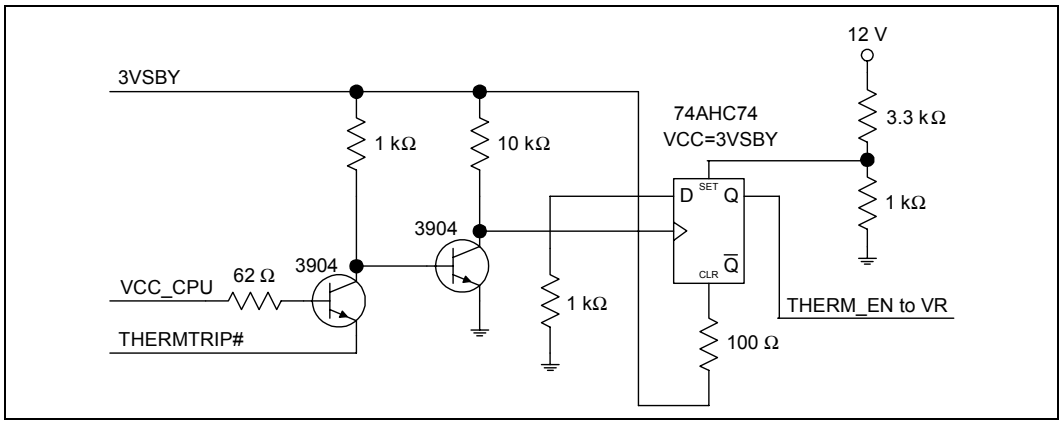


NOTES:
1. Trace Z_0 = 50 Ω
2. Trace spacing = 10 mil

5.3.2.1 Proper THERMTRIP# Usage

To protect the processors from damage in over-temperature situations, power to the processor core must be removed within 0.5 seconds of the assertion of THERMTRIP#. If power is applied to a processor when no thermal solution is attached, normal leakage currents causes the die temperature to rapidly rise to levels at which permanent silicon damage is possible. This high temperature causes THERMTRIP# to go active. Use dual termination on the THERMTRIP# signal. Each processor's THERMTRIP# can be routed to its own receiver, or they can be wire-OR'd together. If routed separately, each signal must be terminated at the receiver end only. All power supply sources to all processors must be disabled when any installed processor signals THERMTRIP#. In the reference schematic, the 74AHC74 flip-flop latches the THERMTRIP# signal HIGH after a PWRGOOD assertion, and LOW after a THERMTRIP# assertion.

Figure 5-6. Recommended THERMTRIP# Circuit



5.3.3 System Bus COMP Routing Guidelines

Terminate the processor COMP[1:0] pins to ground through 49.9 Ω ± 1% resistors. Do not wire the COMP pins together—connect each pin to its own termination resistor.

Terminate the MCH HXRCOMP and HYRCOMP with a 25 Ω ± 1% resistor pull-down to ground. Terminate the MCH HXSWING and HYSWING using a 150 Ω ± 1% resistor pull-down to ground, and a 301 Ω ± 1% pull-up to VCC_CPU, respectively. Use two 0.01 µF decoupling capacitors.

5.3.4 ODTEN Signal Routing Guidelines

Processor 0, the end processor in a dual-processor system, must have its on-die termination enabled. To enable the on-die termination, pull the ODTEN pin to a high state by pulling it up to VCC_CPU through a 50 Ω ± 20% resistor. The resistor value must be within 20% of the trace impedance (50 Ω ± 20%). Processor 1, the middle agent, must have its on-die termination disabled. To disable on-die termination, pull the ODTEN pin to a low state by terminating it to ground through a 50 Ω ± 20% resistor.

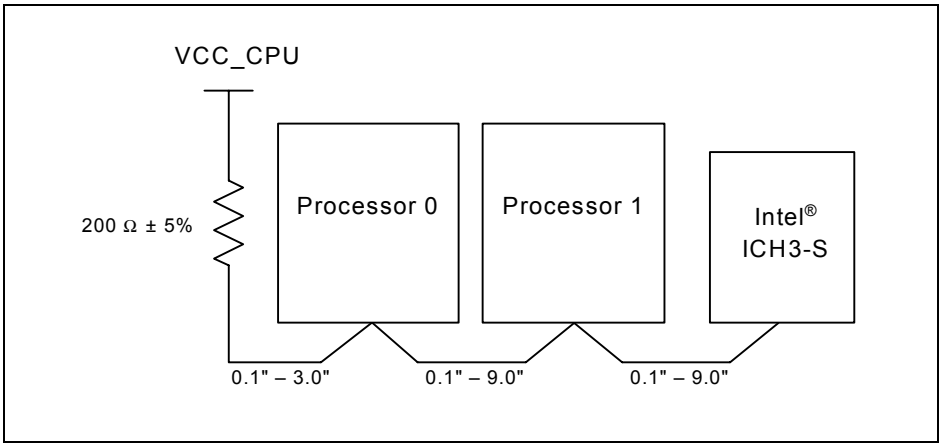
5.3.5 TESTHI[6:0] Routing Guidelines

All TESTHI[6:0] pins must be connected to VCC_CPU via pull-up resistors with a pull-up value within 20% of the signal impedance (50 Ω ± 20%). TESTHI[3:0] may all be tied together and pulled up to VCC_CPU with a single, 50 Ω ± 20% resistor if desired. TESTHI[6:5] may also be tied together and pulled up to VCC_CPU with a single 50 Ω ± 20% resistor. However, boundary scan testing will not be functional if any TESTHI pins are pulled up together. TESTHI4 must always be pulled up independently from the other TESTHI pins regardless of the usage of boundary scan.

5.3.6 Asynchronous GTL+ Signals Driven by the Chipset

Follow the topology shown in Figure 5-7 when routing A20M#, IGNNE#, INIT#, LINT[1:0], CPUSLP#, SMI# and STPCLK#. Do not route a stub when routing to the processors.

Figure 5-7. Topology for Asynchronous GTL+ Signals Driven by the Chipset

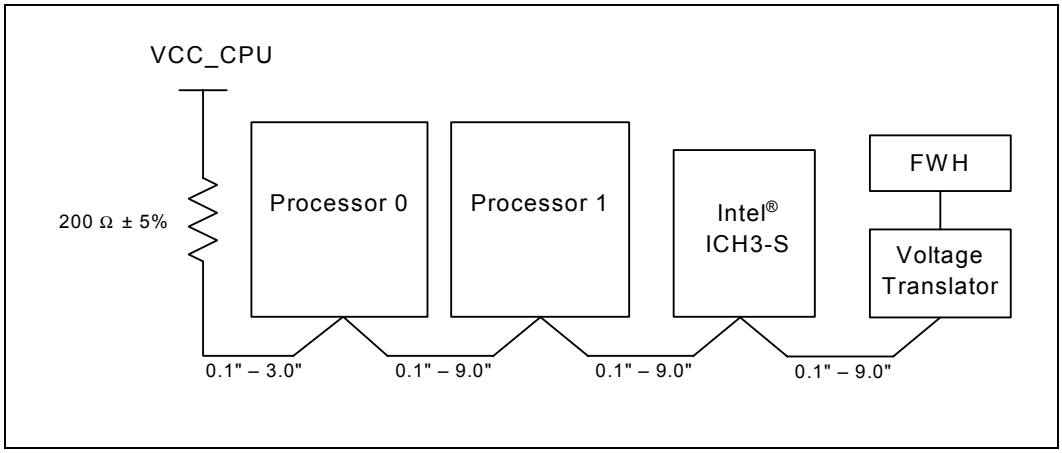


NOTES:
1. Trace Z_0 = 50 Ω
2. Trace spacing = 10 mil

5.3.6.1 Voltage Translation for INIT#

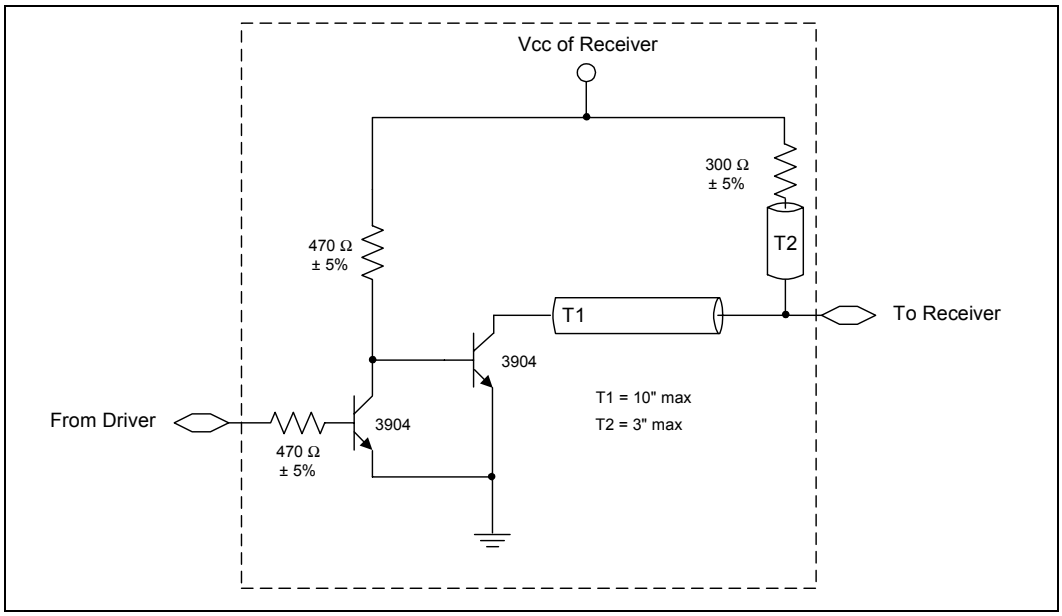
A voltage translator circuit is required for the INIT# signal for all platforms that use the FWH. The required routing topology for INIT# is given in Figure 5-8. Do not route a stub when routing to the processors. Figure 5-9 shows the voltage translator circuit.

Figure 5-8. INIT# Routing Topology



NOTE: The total trace length between the ICH3-S pin and the Processor 0 pin must be less than 15 inches.

Figure 5-9. Voltage Translator Circuit



NOTE: T1 and T2 must be referenced to ground.

5.4 Intel® Xeon™ Processor with 533 MHz System Bus and Intel® Xeon™ Processor with 512-KB L2 Cache

The following sections describe the differences between the Intel Xeon processor with 512-KB L2 cache (INT-mPGA package) and Intel Xeon processor with 533 MHz system bus (FC-mPGA2 package) that require special platform design consideration. Each section also provides design guidelines addressing how to support both processor packages.

5.4.1 Intel® Xeon™ Processor with 533 MHz System Bus Identification

The Intel Xeon processor with 533 MHz system bus provides both an electrical and mechanical method for the motherboard to identify this processor. The Intel Xeon processor with 533 MHz system bus contains an extra pin (location AE30) compared to the Intel Xeon processor with 512-KB L2 cache. This additional pin serves as a mechanical keying mechanism to prevent the Intel Xeon processor with 533 MHz system bus from being installed in the 603-pin socket. The Intel Xeon processors with 533 MHz system bus are only supported in the mPGA604 socket. Section 5.4.2 contains more details about the mPGA604 socket.

The Intel Xeon processor with 533 MHz system bus uses a signal at pin AE4 named “SMB_PRT” that is defined as a Reserved signal on the Intel Xeon processor with 512-KB L2 cache. This signal can be used by the motherboard logic to detect the processor type. For example, platforms with the mPGA604 socket may implement logic that determines proper support for the different manageability features found on the Intel Xeon processor with 512-KB L2 cache and Intel Xeon processor with 533 MHz system bus as recommended in Section 5.5. Table 5-8 summarizes the behavior of pin AE4 on both processors.

Table 5-8. Pin AE4 Signal Values Seen at mPGA604 Socket

Processor (Package Type)	Pin AE4 Definition	Output
Intel® Xeon™ processor with 512-KB L2 cache (INT-mPGA package)	Reserved	Z (High impedance)
Intel® Xeon™ processor with 533 MHz system bus (FC-mPGA2 package)	SMB_PRT	L (Grounded on package)

5.4.2 mPGA604 Socket

The mPGA604 socket contains an additional contact to accept the new keying pin on the Intel Xeon processor with 533 MHz system bus package at pin location AE30 (described in Section 5.4.1). The mPGA604 socket will also accept Intel Xeon processors with 512-KB L2 cache. Since the additional contact for pin AE30 is electrically inert, the mPGA604 socket will not have a solder ball at this location. Therefore, the additional keying pin will not require a motherboard via nor a surface-mount pad.

5.5 SMBus Implementation

Intel Xeon processors with 512-KB L2 cache contain SMBus devices (i.e., PIROM, Scratch EEPROMs, and thermal sensor). Intel Xeon processors with 533 MHz system bus do not contain these SMBus devices. The following sections provide guidelines for designing a system to operate with both processors with respect to these SMBus features.

5.5.1 Intel® Xeon™ Processor with 512-KB L2 Cache SMBus Signals

The Intel Xeon processor with 512-KB L2 cache (INT-mPGA package) contains SMBus devices (i.e., PIROM, Scratch EEPROMs, and thermal sensor). The SMBus signals provide access to the thermal sensor and memory device on the processor. The signaling protocol used adheres to the specification of the System Management Bus. Refer to *Intel® Xeon™ Processor Datasheet* for details on the Intel Xeon processor implementation and addressing scheme.

Connect the SM_ALERT#, SM_CLK, and SM_DAT signals to the SMBus controller in adherence to the *System Management Bus (SMBus) Specification, Version 1.1*. These signals can be connected to other processors on the same SMBus.

The SM_EP_A[2:0] signals set the SMBus address for the memory device on the processor. These signals must be set at power up with a unique address per bus. They have an internal 10 kΩ ± 5% pull-down. To pull the SM_EP_A[2:0] signals to a logic high level, connect each signal to a 100 Ω ± 5% resistor tied to SM_VCC. Refer to the section on SMBus Device Addressing in the processor datasheet for addressing details.

The SM_TS_A[1:0] signals set the SMBus address for the thermal device on the processor. These signals must be set at power up with a unique address per bus. The SM_TS_A[1:0] can be set to logic high, logic low, or a high impedance state giving nine possible combinations of addresses. Refer to the section on SMBus Device Addressing in the processor datasheet for addressing details. The SM_TS_A[1:0] signals do not have an internal pull-down and thus must be pulled to VSS or SM_VCC with a 1 kΩ ± 5% or smaller resistor. Leaving the pins floating achieves a high-Z state.

The SM_WP signal is a write protect signal for the memory device. Pulling this signal to SM_VCC with a 100 Ω ± 5% resistor enables write protection. SM_WP has an internal 10 kΩ pull-down.

5.5.2 Thermal Diode and SMBus Interface

Intel Xeon processors with 533 MHz system bus provide voltage readings directly from the processor core's thermal diode via the THERMDA1 (pin Y27) and THERMDC1 (pin Y28) signals. Note that these signals are not used on the Intel Xeon processors with 512-KB L2 cache since thermal data is obtained via the SMBus from the thermal sensor. Table 5-9 summarizes the functionality of the thermal diode and applicable SMBus pins on both processor package types.

Table 5-9. Functionality for SMBus and Thermal Diode Pins

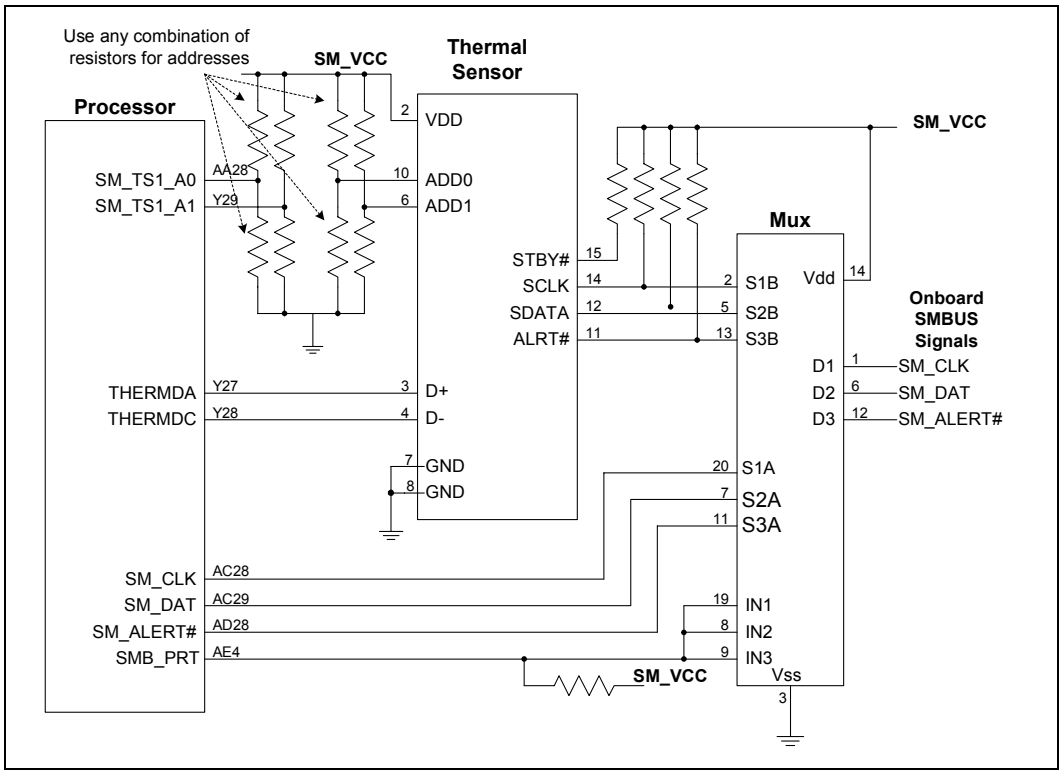
Signal (Pin)	Intel® Xeon™ Processor with 512-KB L2 Cache (INT-mPGA)	Intel® Xeon™ Processor with 533 MHz System Bus (FC-mPGA2)
THERMDA1 (Pin Y27)	N/C: Not used by processor	Output: Provides access to anode of thermal diode.
THERMDC1 (Pin Y28)	N/C: Not used by processor	Output: Provides access to cathode of thermal diode.
SM_CLK (Pin AC28)	Input: SMBus clock	N/C: Not used by processor
SM_DAT (Pin AC29)	I/O: SMBus data signal	N/C: Not used by processor
SM_ALERT# (Pin AD28)	Output: Asserted by thermal sensor device	N/C: Not used by processor
SM_TS1_A[1:0] (Pin AA28, Y29)	Input: Thermal Sensor Select Address	N/C: Not used by processor
SM_EP_A[2:0] (Pin AB28, AB29, AA29)	Input: EEPROM Select Address	N/C: Not used by process
SMB_PRT (Pin AE4)	Reserved: Hi-Z	Output: Grounded on package
SM_WP (Pin AD29)	Input: EEPROM Write Protect	N/C: Not used by process

A system intending to support both packaged versions of the processor needs to include a method for selecting which method (SMBus versus direct diode) from which to obtain thermal data and properly interface with all signals listed in Table 5-9. The following sections describe a hardware and firmware method for supporting both package types.

5.5.2.1 Hardware Selection of SMBus Thermal Devices

Figure 5-10 illustrates a hardware method for selecting the correct thermal sensor device when either an Intel Xeon processor with 512-KB L2 cache or Intel Xeon processor with 533 MHz system bus is installed. This reference circuit needs to be applied to both processor sockets.

Figure 5-10. Circuit Implementation for Hardware-Based SMBus Selection Using Mux



The reference circuit contains a multiplexer device that uses the System Management Bus Present (SM_PRT) signal to select between the system SMBus interfacing with the SMBus from the motherboard's thermal sensor versus the processor SMBus. The multiplexer will only select the processor's SMBus interface when an Intel Xeon processor with 512-KB L2 cache (Hi-Z SM_PRT signal that goes high with the pull-up) is present, resulting in the IN[3:1] inputs driven high. Installation of an Intel Xeon processor with 533 MHz system bus (Grounded SM_PRT signal) results in the multiplexer selecting the motherboard thermal sensor to interface with the system SMBus, resulting in the IN[3:1] inputs driven low.

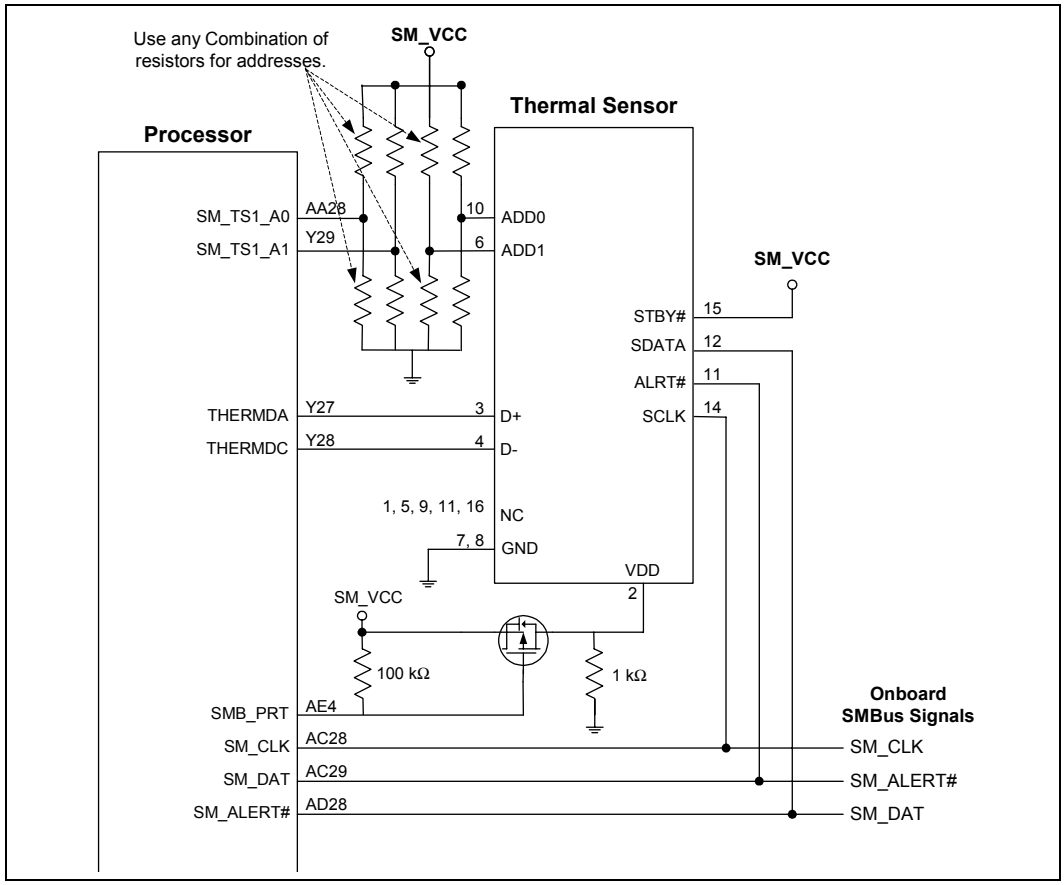
Note that the SMBus address of the motherboard thermal sensor and processor thermal sensor are configured identically to each other, transparent to Server Management software/firmware regardless of which processor package type is installed. Both the processor and thermal sensor inject current onto their three state address pins to determine their address. The thermal sensor does this every time it does an A/D conversion. As a result, both devices should not share the same address resistors.

Figure 5-11 shows a reference circuit similar to Figure 5-10. This circuit requires all of the following thermal sensor properties be properly electrically isolated from the SMBus when the sensor is disabled by the P-channel FET circuit. Refer to our thermal sensor datasheet documentation to confirm these requirements:

The SCLK, SDATA, and ALRT# signals must exhibit a High-Z state. For example, high input current due to backpowering of the device or unpredictable I/O logic behavior as a result of a grounded VDD may prevent correct SMBus operation by pulling any of these signals to an electrically low state.

The SCLK, SDATA, and ALRT# must not exhibit increased leakage current when the VDD supply is grounded. If this is the case, then the motherboard pull-up resistance needs to be evaluated for acceptable VIHMIN levels due to the increased leakage current.

Figure 5-11. Circuit Implementation for Hardware-Based SMBus Selection Using FET



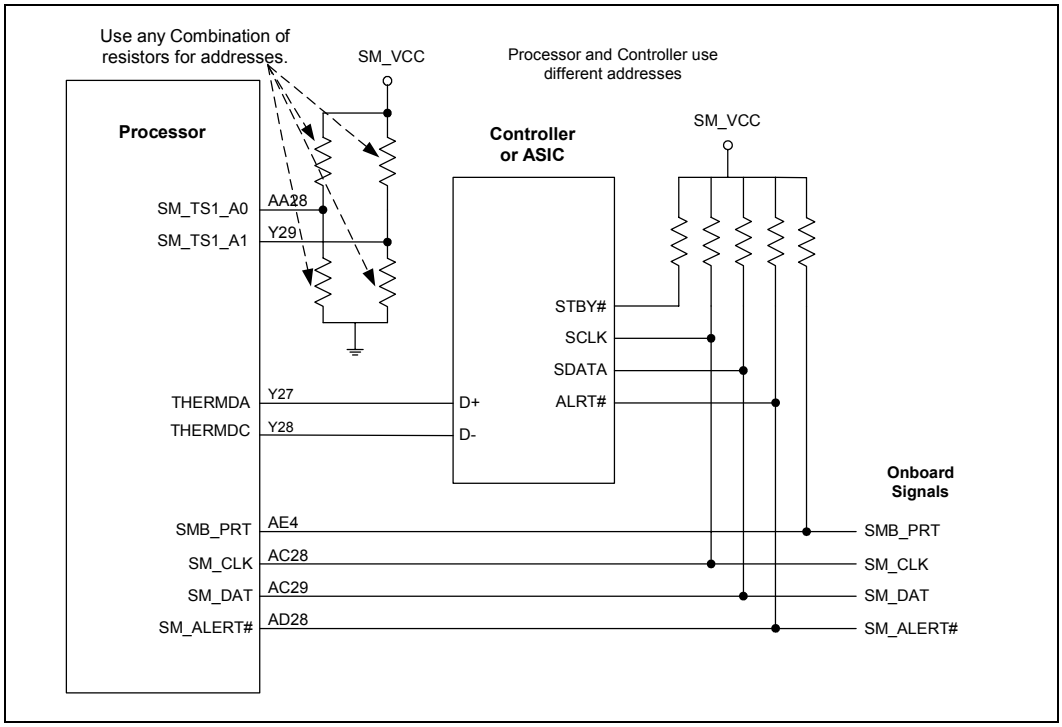
The reference circuit shown in Figure 5-11 assumes the Field Effect Transistor (FET) is a P-channel logic type with low source-to-drain on-resistance and source-to-drain current capacity to supply power to the thermal sensor. Based on the thermal sensor components listed in Figure 5-10, the FET should be capable of handling a minimum of 180 µA source-drain current and have less than 1 Ω source-drain resistance. The FET also needs specific gate electrical specifications to support the two logic levels presented by a processor-driven grounded or open SMB_PRT signal (state depends on processor type), and the associated pull-up resistor\voltage used in the reference circuit. The FET should have a maximum gate input leakage current of 1 µA when the FET is in the OFF state.

The FET should have a minimum\maximum VGS-Thresh (Gate-Source Threshold Voltage) of approximately -0.4 V\-1.0 V. The “minimum” value of -0.4 V will prevent leakage current pulling an open SMB_PRT signal to an electrically low state. And the “maximum” -1.0 V value will still allow a grounded SMB_PRT signal to switch the FET's gate to an ON state.

5.5.2.2 Firmware Selection of SMBus Thermal Devices

This section describes a firmware method for supporting either the Intel Xeon processor with 512-KB L2 cache or the Intel Xeon processor with 533 MHz system bus. This method is based on the thermal sensor implementation illustrated in Figure 5-12. The board designer can route each processor's SMB_PRT to an ICH3-S GPIO pin, Baseboard Management Controller GPIO pin, or any other ASIC or microcontroller. Likewise, any Baseboard Management Controller, microcontroller, or ASIC can also be used as a thermal sensor. Firmware can detect whether the signal is low or high to determine which device to address the processor temperature. If the signal is high, then an Intel Xeon processor with 512-KB L2 cache is installed and the SMBus controller can access the processor SMBus target. If an Intel Xeon processor with 533 MHz system bus is installed, SMB_PRT is low and the SMBus controller knows to access the other device which contains a thermal sensor. Both the processor and the controller or ASIC must have different addresses so that they can be differentiated on the SMBus. The advantage of this method over the hardware option discussed in the previous section is that no mux device is required.

Figure 5-12. Circuit Implementation for Firmware-Based SMBus Selection



5.5.3 Thermal Sensor Selection

Figure 5-10 illustrates an example implementation where the same thermal sensor device used on the Intel Xeon processor with 512-KB L2 cache (See Table 5-10 for details) is also placed on the motherboard to provide equivalent thermal sensor operation between Intel Xeon processor with 512-KB L2 cache and Intel Xeon processor with 533 MHz system bus. Use of either of the thermal sensor devices listed in Table 5-10 is not required as device selection should be based on the features, operating requirements, or other factors defined by the platform.

Table 5-10. Thermal Sensor Devices

Vendor	Part Number
Philips Semiconductors	NE1617A
Analog Devices, Inc.	ADM1021A

NOTE: This list is provided for reference purposes only. It is not intended to be a complete list of available components that can provide this function.

5.5.4 Thermal Sensor Layout and Routing Considerations

Because the motherboard thermal sensor device is measuring very small voltages from the processor (Intel Xeon processor with 533 MHz system bus only) thermal diode, extreme care must be taken to minimize the noise induced on the thermal sensor input pins. The following are guidelines a motherboard designer can use to help ensure a clean thermal sensor implementation:

- Place the thermal sensor device as close to the processor socket as possible. Ideally, the placement should be as close as possible to the THERMDA and THERMDC thermal diode output pins to reduce the length of the processor thermal diode output signals to the thermal sensor.
- Route the processor thermal diode output signals close together and in parallel. Intel strongly recommends surrounding the signal pair with ground guard traces and adding component pad sites close to the thermal sensor input to support a shunt capacitor between the THERMDA and THERMDC signal traces.
- Use wide traces and spacing to route the processor thermal diode output signals. This will minimize induction and reduce the noise on these signals.
- Keep noisy sources such as clock generators and high-speed data and address buses away from the thermal sensor and the processor thermal diode output signals to help minimize noise.

For more in-depth layout and routing considerations, please refer to documentation provided by your thermal sensor device vendor.

5.5.5 Alternative Method to Obtain PIROM Data

Since the Intel Xeon processor with 533 MHz system bus does not contain a PIROM device, systems must not rely on these data contents. However, some of the PIROM data field contents may be obtained by alternative methods using either the CPUID instruction or by reading certain processor mode-specific registers. Table 5-11 summarizes the information available and the method for obtaining the data. Contact your Intel representative for more information Refer to the *AP-485 Intel® Processor Identification and CPUID Instruction* and your Intel representative for complete details.

Table 5-11. Alternative Method to Obtain Processor Information

PIROM Data Field	Alternative Method for Obtaining Information
Processor Core Data	
Processor Core Type	CPUID with input 1
Processor Core Model	CPUID with input 1
Processor Core Family	CPUID with input 1
Processor Core Stepping	CPUID with input 1
System Bus Speed	MSR_EBC_FREQUENCY_ID
Maximum Core Frequency	MSR_EBC_FREQUENCY_ID[1]
Cache Size	
L2 Cache Size	CPUID with input 2

NOTE: This register provides the core frequency-to-system bus ratio. Processor core frequency may be obtained by multiplying the ratio times the system bus frequency.

5.6 Boot Critical Signals

Processors can only run in certain dual-processor configurations. The following section discusses which signals dictate certain processor signals, which dictate processor settings, and a sample circuit.

5.6.1 VID[4:0]

Route the VID[4:0] signals of the processor to the VID[4:0] inputs of the voltage regulator controller. The voltage regulator controller should provide internal pull-up resistors for these signals. Refer to the *VRM 9.1 DC-DC Converter Design Guidelines* and the specification of the voltage controller specific to your design for further details.

Since both processors must operate at the same voltage, the designer should provide a way to check the VID[4:0] signals to ensure a processor does not operate out of specification. Refer to Figure 11-4 for more information.

5.6.2 SKTOCC# Signal Routing Guidelines

The SKTOCC# signal is an output from the processor used as an indication of whether a processor is installed or not. It is asserted low when a processor is installed in the socket, and floats when no processor is present. If this signal is used on the board, the designer can use a pull-up to prevent floating. SKTOCC# can be used to disable the VRM or VRD output for unpopulated processor sockets or the power supply output when no processors are installed and other features.

5.6.3 BSEL[1:0] Implementation

The processor provides two output signals named BSEL[1:0] that the motherboard uses to identify the system bus frequency supported by the installed processor. The BSEL[1:0] output values are shown in Table 5-12. The recommended pull-up value for BSEL with the comparator in Section 11.2.6 is a 1 kΩ, though the designer should ensure that the proper VIH and VIL is maintained for the receiver. These outputs may be used by motherboard logic to:

- Automatically select the proper system bus clock frequency driven by the CK408B.
- Verify both processors support the same system bus frequency. If processor system bus frequencies do not match, then disable the voltage regulator output which supplies power to the processors.

Table 5-12. BSEL[1:0] Output

System Bus Speed	BSEL1	BSEL0
400 MHz	L	L
533 MHz	L	H

BSEL[1:0] have a power sequencing requirement discussed in Section 11.2.6.

5.6.4 Sample Implementation Circuit

Figure 5-13 shows an example BSEL[1:0] motherboard implementation that is incorporated into the E7501 MCH Customer Reference Board. This circuit performs those functions mentioned previously and leverages the existing VID comparator logic used on the E7500 Chipset Customer Reference Board. The major addition is that BSEL[1:0] outputs from both processor sockets are routed to the P6/P5 and Q6/Q5 inputs of the VID comparator. The comparator will check that all VID[4:0] and BSEL[1:0] signal values match on both processors. The SKTOCC# signal is also utilized, to determine when Socket 1 is not populated (i.e., only one processor is present).

The first condition of this circuit that enables the voltage regulator is when the VIDs and BSELs match. If both processors are installed and running with the same VID and BSEL values, a low goes to the input of the NAND from the comparator, enabling the voltage regulator.

The second condition of this circuit which enables the voltage regulator is when Socket 1 is not populated. If a processor is only present in Socket 0, an erroneous mismatch signal is ignored, and the low asserted from the inverter ensures the NAND outputs a high, enabling the voltage regulator.

The condition that disables the voltage regulator is when both inputs to the NAND are high. In this case, there is both a mismatch (comparator outputs a high) and a populated Socket 1 (the SKT_OCC# inverter outputs a high). In this instance, the NAND outputs a low, disabling the voltage regulator. If both processors are present, the VIDs and BSELs do not match. If Socket 1 is populated and Socket 0 is not, a mismatch occurs, disabling the voltage regulator.

The BSEL0 output from the processor 0 socket is also connected to the CK408B and GPI to program both devices to operate at either 100 MHz or 133 MHz based on the processor installed. Table 5-13 summarizes the operation of the reference circuit.

Figure 5-13. BSEL[1:0] Reference Circuit

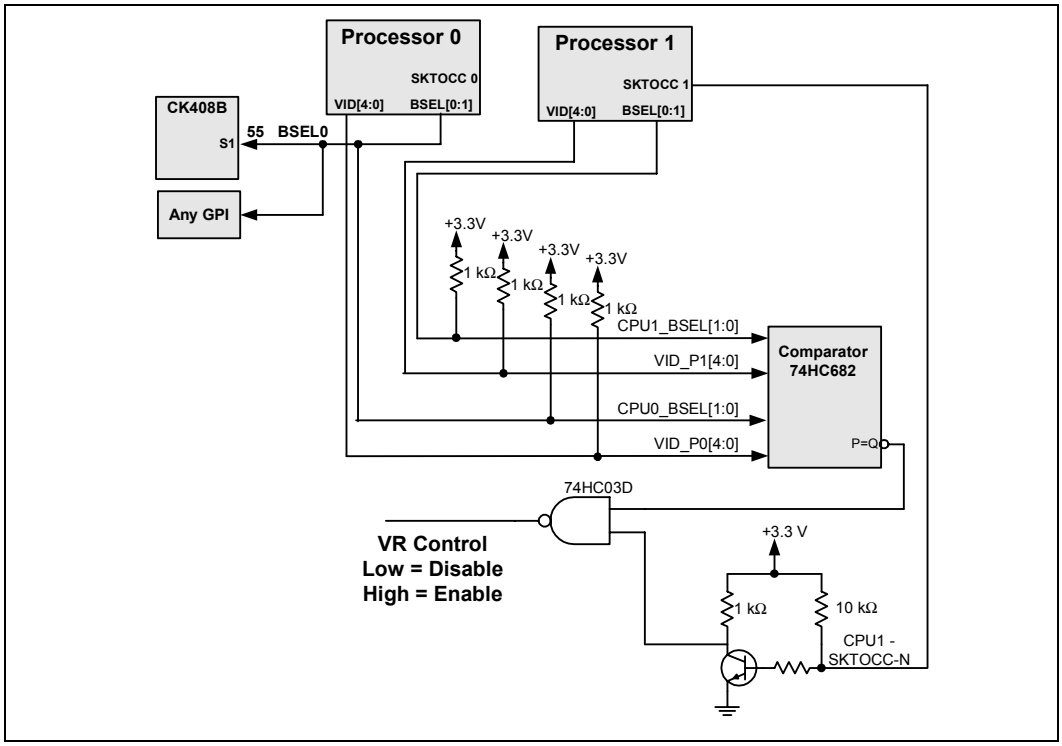


Table 5-13. Functionality of SKTOCC# and VR Output

Processor 0 Socket	Processor 1 Socket	SKTOCC#	VR Output Low = Disable High = Enable	Functionality
533 MHz System Bus Processor	533 MHz System Bus Processor	L	H	Operates system in DP mode with 133 MHz system bus clock.
400 MHz System Bus Processor	533 MHz System Bus Processor	L	L	Disables voltage regulator to prevent processor operation.
533 MHz System Bus Processor	400 MHz System Bus Processor	L	L	Disables voltage regulator to prevent processor operation.
400 MHz System Bus Processor	400 MHz System Bus Processor	L	H	Operates system in DP mode with 100 MHz system bus clock.
533 MHz System Bus Processor	None	H	H	Operates system in UP mode with 133 MHz system bus clock.
None	533 MHz System Bus Processor	L	L	Disables voltage regulator to prevent processor operation.
400 MHz System Bus Processor	None	H	H	Operates system in UP mode with 100 MHz system bus clock.
None	400 MHz System Bus Processor	L	L	Disables voltage regulator to prevent processor operation.

NOTE: VID[4:0] have been omitted from this table to simplify the description. Described functionality assumes that VID values match when both processors are installed. In the event where VID values do not match, the circuit will disable the voltage regulator to prevent unsupported processor operation.

Memory Interface Routing Guidelines 6

The E7500 chipset MCH and E7501 chipset MCH memory interface consist of two DDR memory channels that operate in "lock-step." Each channel consists of 64 data and eight ECC bits. Logically, this is one, 144-bit wide memory bus; electrically, each channel is separate.

The E7501 chipset MCH supports an additional feature to the E7500 chipset MCH: DDR266. The E7500 chipset MCH only supports DDR200 while the E7501 chipset MCH supports both DDR200 and DDR266. This chapter only documents the configurations Intel simulated to support these features. The customer should simulate any deviations from these recommendations. A 2-DIMM per-channel configuration may be used with the "3-DIMM Solution" recommendations.

This chapter covers routing guidelines for the DDR interfaces. Note that these guidelines apply to both channel A and channel B. Each DDR interface has six signal types: Command Clocks, Source Clocked Signals, Source Synchronous Signals, Chip Selects, Clock Enable, and DC Biasing. Refer to the *Intel® E7500 Chipset Memory Controller Hub (MCH) Datasheet* and *Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet* for details on the signals.

Table 6-1. DDR Channel Signal Groups

Group	Signal
Source Synchronous Signals	DQS_x[17:0] DQ_x[63:0] CB_x[7:0]
Command Clocks	CMDCLK_x[3:0] CMDCLK_x[3:0]#
Source Clocked Signals	MA_x[12:0] RAS_x# CAS_x# WE_x# BA_x[1:0]
Chip Selects	CS_x[7:0]#
Clock Enable	CKE_x
DC Biasing	See Table 6-9

6.1 DDR Overview

Figure 6-1 and Figure 6-2 show both channels being routed to a single "bank" of eight DIMMs. The DIMMs are physically interleaved. Intel recommends using this interleaving, starting with Channel B closest to the MCH, for optimal routing.

The platform requires DDR DIMMs to be populated in-order, starting with the DIMMs furthest from the MCH in a "fill-farthest" approach (see Figure 6-1 and Figure 6-2). In addition, single rank DIMMs should be populated furthest when a combination of single ranked and double ranked DIMMs are used. This recommendation is based on the signal integrity requirements of the DDR interface. Intel's recommendation is to check for correct DIMM placement during BIOS initialization. Additionally, it is strongly recommended that all designs follow the DIMM ordering, SMBus Addressing, Command Clock routing and Chip Select routing documented in Figure 6-1 and Figure 6-2. This addressing must be maintained to be compliant with the reference BIOS code supplied by Intel. For a 2-DIMM board, follow the same methodology.

Figure 6-1. 3-DIMM per-Channel Implementation

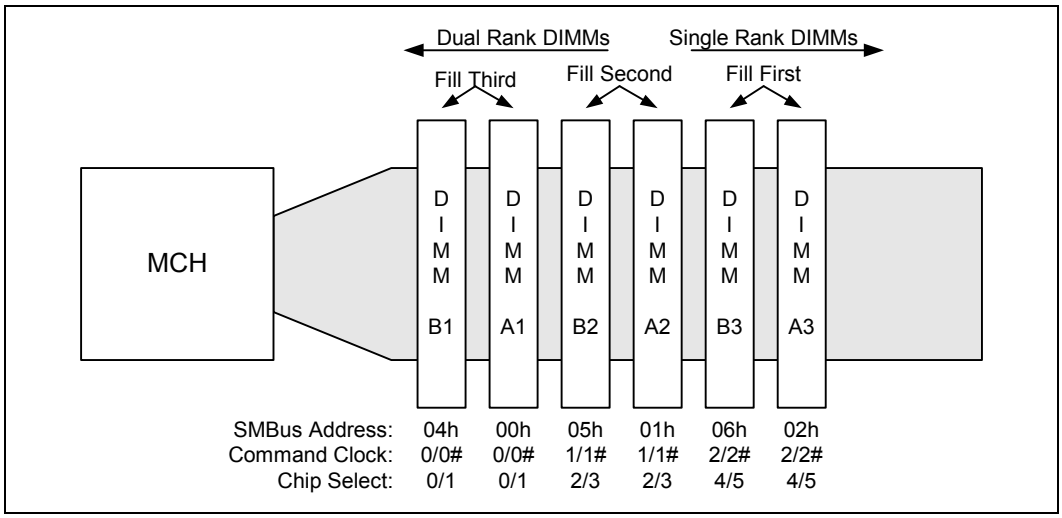
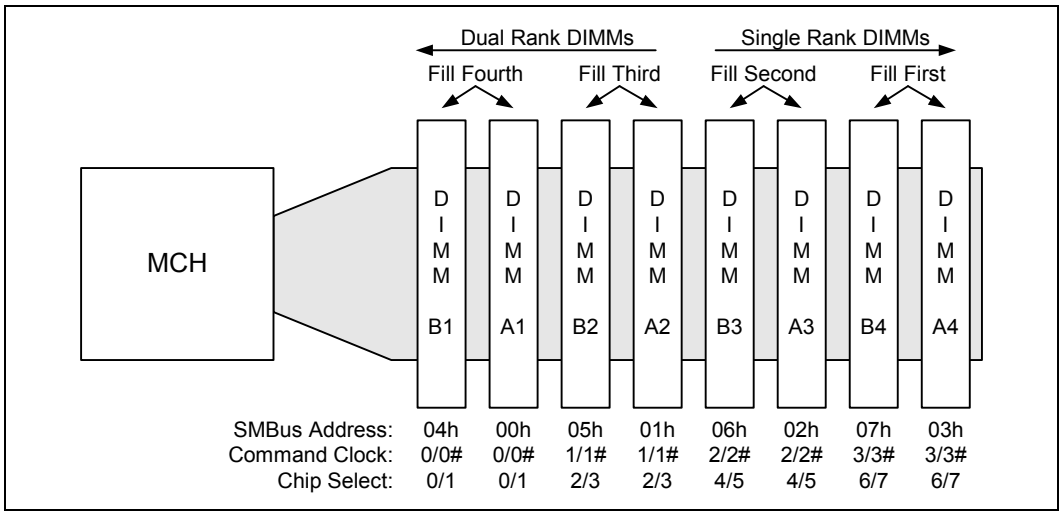


Figure 6-2. 4-DIMM per-Channel Implementation



Certain combinations of DIMM types in 3-DIMM and 4-DIMM per channel systems have been found to violate the JEDEC write ring back measurement specification. 1-DIMM and 2-DIMM per channel systems do not violate the JEDEC write ring back specification. When combining double-rank DIMMs (x4 or x8) with single-rank DIMMs (x4 or x8), if the first populated slot (closest to the MCH) contains a single-ranked DIMM, the write ringback at that DIMM violates the JEDEC DRAM specification. To reduce write ring back, populate single-ranked DIMMs furthest from the MCH when a combination of single-ranked and double-ranked DIMMs is used.

To determine if a registered DDR DIMM is a single-bank DIMM or a double-bank DIMM, refer to your Intel representative for more information.

Figure 6-3. Example of Proper Single and Dual Rank Mixing

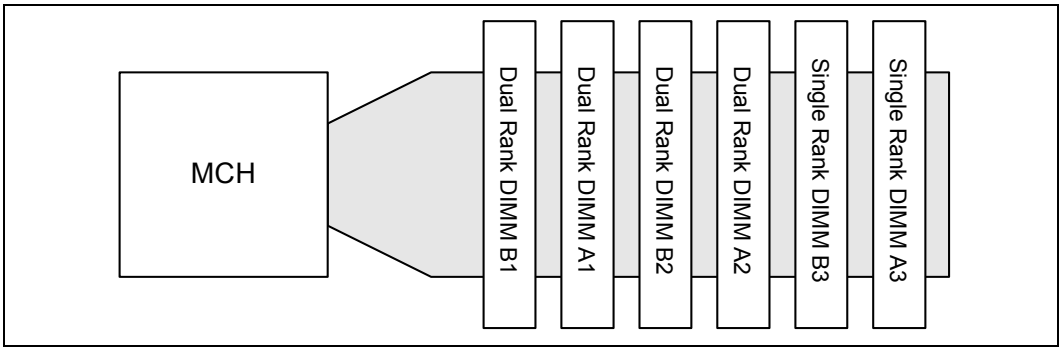
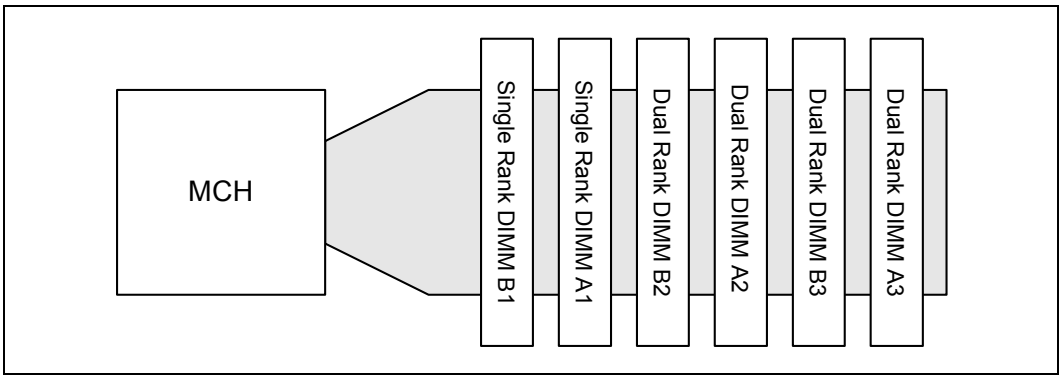


Figure 6-4. Example of Incorrect Single and Dual Rank Mixing



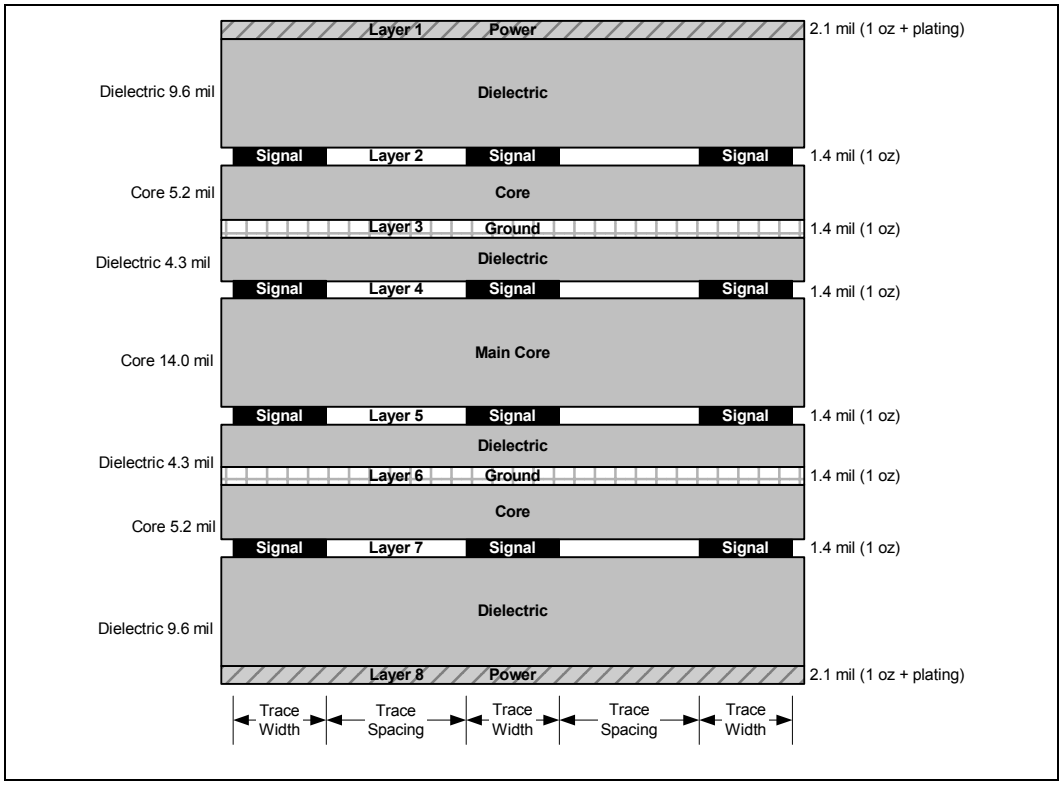
6.1.1 DDR Channel Impedance Requirements

The DDR channel requires different widths for different signals depending on the configuration used. Table 6-2 indicates the impedances for the trace widths used for routing the data bus.

Table 6-2. Trace Width to impedance Requirements

Trace Width	Nominal Trace Impedance (Z_0)
4 mil	55 Ω ± 10%
5 mil	50 Ω ± 10%
6 mil	45 Ω ± 10%
7.5 mil	40 Ω ± 10%

Figure 6-5. Trace Width and Spacing for All DDR Signals Except CMDCLK_x[3:0]/ CMDCLK_x[3:0]#



NOTE: Traces on layers 4 and 5 must be routed orthogonally to each other to minimize the effects of crosstalk.

6.2 Source Synchronous Signal Group Routing

The MCH source synchronous signals are divided into groups consisting of data bits (DQ) and check bits (CB). An associated strobe (DQS) exists for each DQ and CB group, as shown in Table 6-3. The MCH supports both x4 and x8 devices, and the number of signals in each data group depends on the type of devices that are populated. For example, if x4 devices are populated, the 72-bit channel is divided into 18 data groups (16 groups consisting of four data bits each, and two groups consisting of four check bits each). One DQS is associated with each of these groups (18 total). Likewise, if x8 devices are populated, the 72-bit channel is divided into a total of nine data groups. In this case, only 9 of the 18 strobes are used.

Table 6-3. DQ/CB to DQS Mapping

Data Group	Associated Strobe(1)
DQ_x[7:0]	DQS_x0, DQS_x9
DQ_x[15:8]	DQS_x1, DQS_x10
DQ_x[23:16]	DQS_x2, DQS_x11
DQ_x[31:24]	DQS_x3, DQS_x12
DQ_x[39:32]	DQS_x4, DQS_x13
DQ_x[47:40]	DQS_x5, DQS_x14
DQ_x[55:48]	DQS_x6, DQS_x15
DQ_x[63:56]	DQS_x7, DQS_x16
CB_x[7:0]	DQS_x8, DQS_x17

NOTE:
1. In x4 configurations, the high DQS is associated with the high nibble and the low DQS is associated with the low nibble. In x8 configurations, only the low DQS is used.

Table 6-4 states the trace length requirements for the DQ, DQS, and CB signals. All signals in a data group must be length matched to the associated DQSs, as described in Section 12.5. Length matching past the last DIMM connector is not critical. Route all data signals and their associated strobes on the same layer. Try to maintain routing the signals on the same layer. If a layer transition must occur, minimize the discontinuity in the ground reference plane. The source synchronous signals require series termination resistors (Rs) placed close to the first DIMM connector, and parallel termination resistors (Rtt) placed after the last DIMM connector. These solutions do not require DQS to CMDCLK pair length matching. If you use resistor packs for the termination resistors, it is suggested that data group signals not be mixed with Source Clocked, Chip Select, or Clock Enable signals within the same resistor pack for validation purposes.

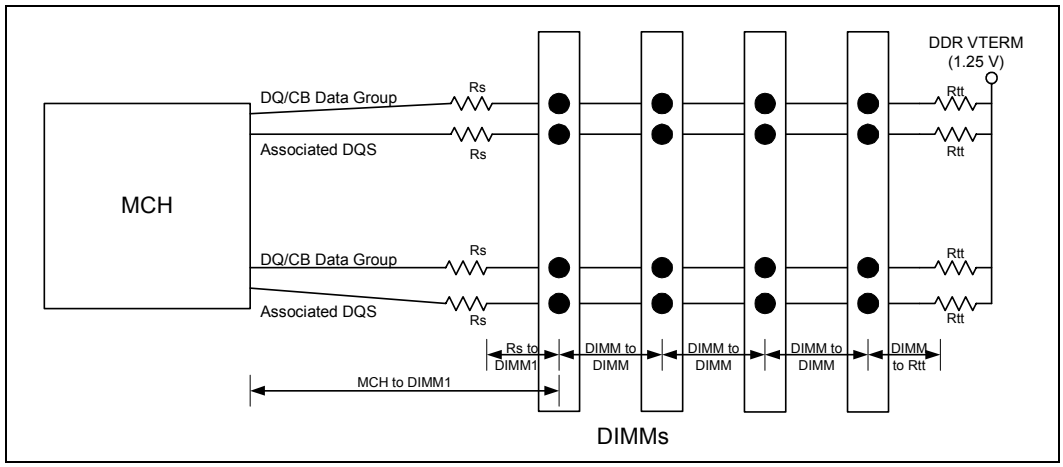
Table 6-4. Source Synchronous Signal Group Routing Guidelines

Parameter	3-DIMM Solution	4-DIMM Solution	Reference
Signal Group	DQ[63:0], CB[7:0], DQS[17:0]		
Topology	Daisy Chain		Figure 6-6
Reference Plane	Ground		Figure 6-5
MCH to Rs Trace Impedance (Z_0)	50 Ω ± 10%	45 Ω ± 10%	Table 6-2
Rs to Rtt Trace Impedance (Z_0)	50 Ω ± 10%	55 Ω ± 10%	Table 6-2
MCH to Rs Trace Width	5 mil	6 mil	Figure 6-5
Rs to Rtt Trace Width	5 mil	4 mil	Figure 6-5
Nominal Trace Spacing	15 ± 1 mil	15 ± 1 mil	Figure 6-5
MCH to DIMM1 Trace Length[4]	3.5" to 6.3"	6.1" to 6.3"	Figure 6-6
Rs to DIMM1 Trace Length	0.1" to 0.8"	0.1" to 0.8"	Figure 6-6
DIMM to DIMM Trace Length	1.0" to 1.2" ± 50 mil[5]	1.0" to 1.2" ± 50 mil [5]	Figure 6-6
DIMM to Rtt Trace Length	< 0.8"	0.3" to 1.3"	Figure 6-6
Series Resistor (Rs)	10 Ω ± 2%	0 Ω /6.2 Ω ± 5%[1]	Figure 6-6
Termination Resistor (Rtt)	39.2 Ω ± 1% / 33.2 Ω ± 1%[2]	34.8 Ω ± 1%	Figure 6-6
MCH Breakout Guidelines	5/5, < 500 mil	5/5, < 500 mil	
Length Tuning Requirements	DQ to DQS: ± 25 mil[3]	DQ to DQS: ± 25 mil[3]	Section 12.5

NOTES:

1. On a compatible motherboard, use a 6.2 Ω for an E7500 chipset MCH and a 0 Ω for an E7501 chipset MCH. On a motherboard which only supports an E7501 chipset MCH, no Rs is required. Instead, change the impedance at the first DIMM pin.
2. On a compatible motherboard, use a 33.2 Ω for an E7500 chipset MCH and a 39.2 Ω for an E7501 chipset MCH.
3. The DQS pair in the group must also be tuned to each other with this parameter. The DQ and DQS lines in the same group must be length tuned to all DIMMs. Tune all lengths to the E7501 chipset MCH package trace lengths.
4. The MCH to DIMM1 trace length is defined as E7501 chipset MCH die pad (PCB trace velocity equivalent, see Section 12.5) to DIMM1 pin.
5. Within the same group, this length range should not vary by more than 50 mils. However, the length can be anywhere from 1.0" to 1.2".

Figure 6-6. Source Synchronous Topology



NOTE: Indicated lengths measure from the MCH die pad (PCB trace velocity equivalent, see Section 12.5) to the DIMM connector pin (including the series resistor).

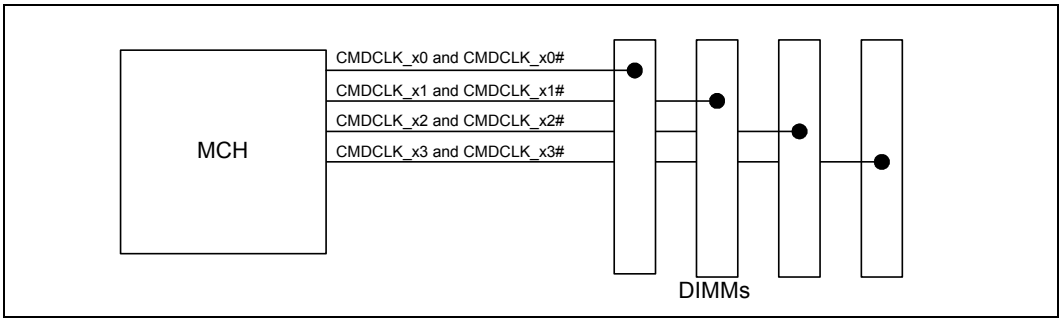
6.3 Command Clock Routing

Only one differential clock pair is routed to each DIMM connector because the MCH only supports registered DDR DIMMs. All CMDCLK/CMDCLK# termination is on the DIMM modules. Route each clock and its compliment adjacent to each other. The two complimentary signals (e.g., CMDCLK_x0 and CMDCLK_x0#) must be length matched to each other within ± 2 mils and must be routed on the same layer. If a layer transition must occur, minimize the discontinuity in the ground reference plane.

Table 6-5. Command Clock Pair Routing Guidelines

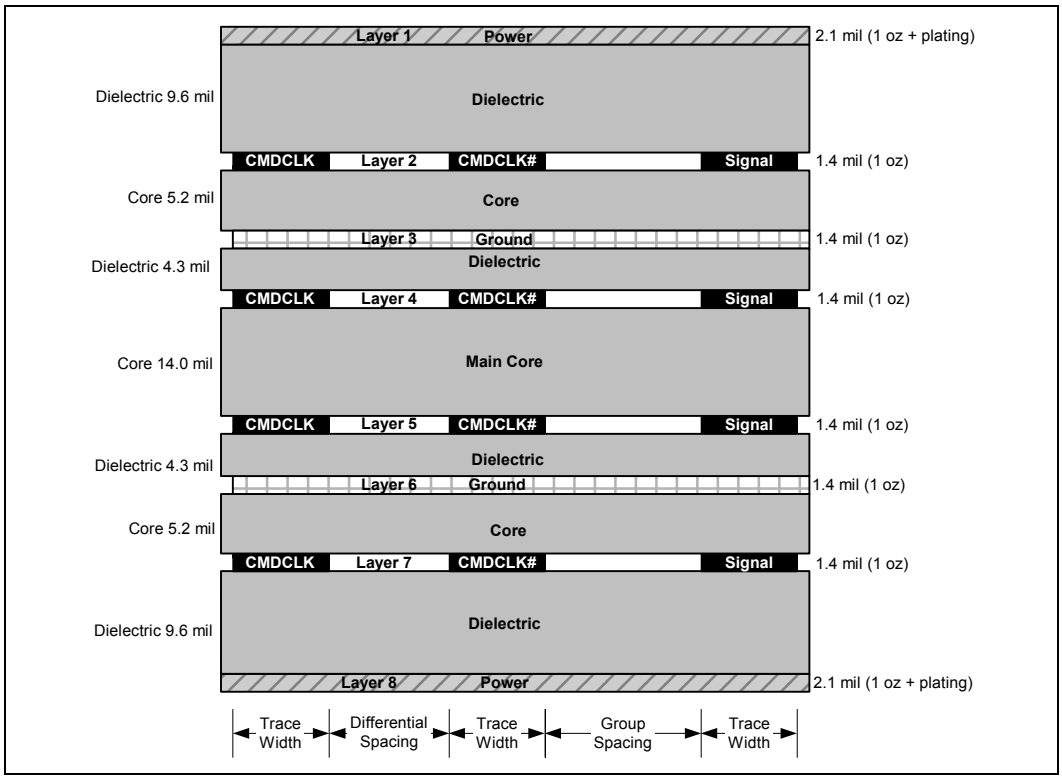
Parameter	3-DIMM Solution	4-DIMM Solution	Reference
Signal Group	CMDCLK, CMDCLK#		
Topology	Point-to-point		Figure 6-7
Reference Plane	Ground		Figure 6-8
Differential Trace Impedance (Z_0)	100 Ω ± 10%	100 Ω ± 10%	Figure 6-8
Nominal Trace Width	5 mil	5 mil	Figure 6-8
Differential Trace Spacing	7.5 mil	7.5 mil	Figure 6-8
Group Trace Spacing	20 mil	20 mil	Figure 6-8
MCH to DIMM1 Trace Length	4.0" ± 250 mil	7.50" ± 100 mil	Figure 6-7
MCH to DIMM2 Trace Length	6.0" ± 250 mil	8.00" ± 100 mil	Figure 6-7
MCH to DIMM3 Trace Length	8.0” ± 250 mil	8.75" ± 100 mil	Figure 6-7
MCH to DIMM4 Trace Length	Not Supported	10.75" ± 100 mil	Figure 6-7
MCH Breakout Guidelines	5/5, < 500 mil	5/5, < 500 mil	
Length Tuning Requirements	CMDCLK to CMDCLK#: ± 2 mil	CMDCLK to CMDCLK#: ± 2 mil	Figure 6-7

Figure 6-7. Command Clock Topology



NOTES:
1. CMDCLK/CMDCLK# must be matched to within ± 2 mils using package trace length compensation.
2. 3-DIMM solution: Treat the CMDCLK_x3/CMDCLK_x3# pair as a no connect.
3. Indicated lengths measured from the MCH component pin to the DIMM connector pin.

Figure 6-8. Trace Width/Spacing for CMDCLK/CMDCLK# Routing



6.4 Source Clocked Signal Group Routing

The MCH drives the command clock signals and the source-clocked signals together. That is, the MCH drives the command clock in the center of the valid window, and the source-clocked signals propagate with the command clock signal. Therefore, the critical timing is the difference between the command clock flight time and the source clocked signal flight time. The absolute flight time is not as critical.

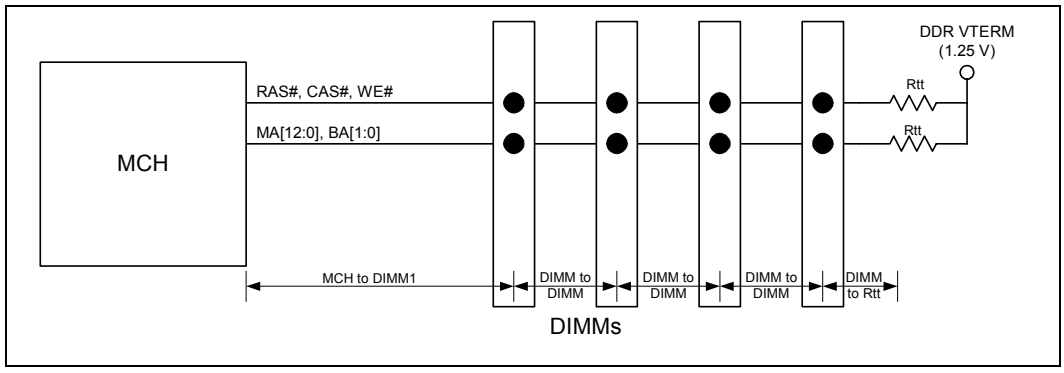
If you use resistor packs for the termination resistors, it is suggested that data group signals not be mixed with Source Clocked, Chip Select, or Clock Enable signals within the same resistor pack for validation purposes.

Table 6-6. Source Clocked Signal Group Routing Guidelines

Parameter	3-DIMM Solution	4-DIMM Solution	Reference
Signal Group	RAS#, CAS#, WE#, MA[12:0], BA[1:0]		
Topology	Daisy Chain		Figure 6-9
Reference Plane	Ground		Figure 6-5
Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%	Table 6-2
Nominal Trace Width	5 mil	5 mil	Figure 6-5
Nominal Trace Spacing	15 mil	15 mil	Figure 6-5
MCH to DIMM1 Trace Length	2.0” to 6.0”	2.0” to 6.0”	Figure 6-9
DIMM to DIMM Trace Length	1.0” to 1.2”	1.0” to 1.2”	Figure 6-9
DIMM to Rtt Trace Length	< 0.8”	0.3” to 1.3”	Figure 6-9
Termination Resistor (Rtt)	39.2 Ω ± 1% / 33.2 Ω ± 1% [1]	34.8 Ω ± 1%	Figure 6-9
MCH Breakout Guidelines	5/5, < 500 mil	5/5, < 500 mil	

NOTES:
1. On a compatible motherboard, use a 33.2 Ω for an E7500 chipset MCH and a 39.2 Ω for an E7501 chipset MCH.

Figure 6-9. Source Clocked Signal Topology



NOTES:
1. Indicated lengths measure from the MCH component pin to the DIMM connector pin.

6.5 Chip Select Routing

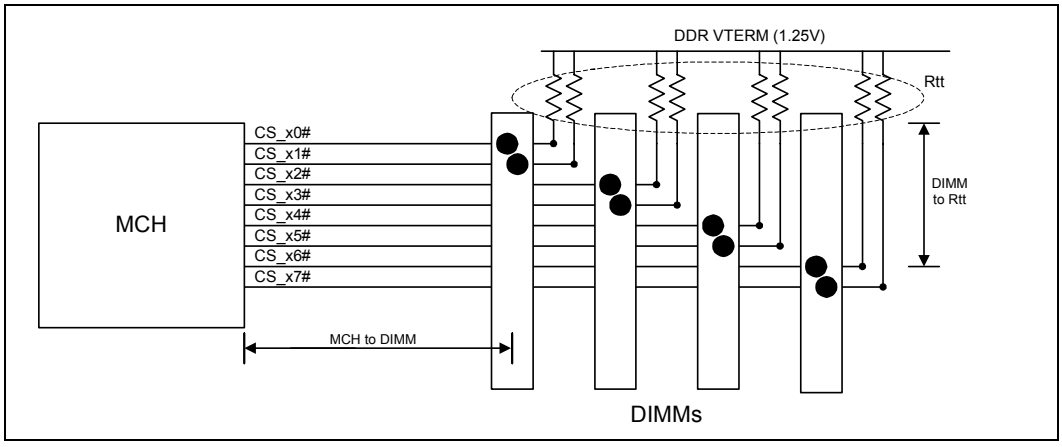
The MCH provides eight chip select signals. Two chip selects must be routed to each DIMM (one for each side). Chip selects for each DIMM must be length matched to the corresponding clock within ± 875 mils and require parallel termination resistors (Rtt) to DDR VTERM.

Table 6-7. Chip Select Routing Guidelines

Parameter	3-DIMM Solution	4-DIMM Solution	Reference
Signal Group	CS[7:0]#		
Topology	Point to Point		Figure 6-10
Reference Plane	Ground		Figure 6-5
Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%	Table 6-2
Nominal Trace Width	5 mil	5 mil	Figure 6-5
Nominal Trace Spacing	15 mil	15 mil	Figure 6-5
MCH to DIMM1 Trace Length	4.0" ± 875 mil	7.50" ± 875 mil	Figure 6-10
MCH to DIMM2 Trace Length	6.0" ± 875 mil	8.00" ± 875 mil	Figure 6-10
MCH to DIMM3 Trace Length	8.0" ± 875 mil	8.75" ± 875 mil	Figure 6-10
MCH to DIMM4 Trace Length	Not Applicable	10.75" ± 875 mil	Figure 6-10
Trace Length - DIMM to Rtt	0.3" to 1.5”	0.1" to 1.5”	Figure 6-10
Termination Resistor (Rtt)	39.2 Ω ± 1% / 33.2 Ω ± 1%[1]	34.8 Ω ± 1%	Figure 6-10
MCH Breakout Guidelines	5/5, < 500 mil	5/5, < 500 mil	

NOTES:
1. On a compatible motherboard, use a 33.2 Ω for an E7500 chipset MCH and a 39.2 Ω for an E7501 chipset MCH.

Figure 6-10. Chip Select Topology



NOTES:
1. 3-DIMM solution: Treat CS_x6# and CS_x7# as a no connect.
2. Indicated lengths measured from the MCH component pin to the DIMM connector pin.

6.6 Clock Enable Routing

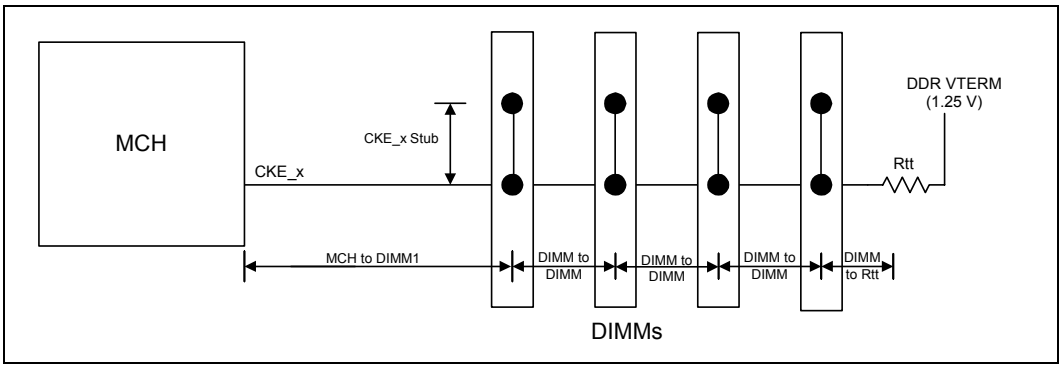
The MCH provides a single clock enable (CKE) signal. This signal is used during initialization to indicate that valid power and clocks are being applied to the DIMMs. Because the CKE signal has higher loading, it requires a lower impedance. The recommended impedance for the CKE signal is 40 Ω. This can be achieved using a 7.5-mil wide trace on the recommended stack-up (refer to Figure 6-5). It is acceptable to route the CKE signal 5-mils wide and 5-mils spacing when breaking out of the MCH. However, the trace must be widened to 7.5 mils before widening the spacing to 15 mil. The CKE signal requires a parallel termination resistor (Rtt) to DDR VTERM placed as close to the last DIMM connector as possible.

Table 6-8. Clock Enable Routing Guidelines

Parameter	3-DIMM Solution	4-DIMM Solution	Reference
Signal Group	CKE		
Topology	Daisy Chain with Stubs		Figure 6-11
Reference Plane	Ground		Figure 6-5
Trace Impedance (Z_0)	40 Ω ± 10%	40 Ω ± 10%	Table 6-2
Nominal Trace Width	7.5 mil	7.5 mil	Figure 6-5
Nominal Trace Spacing	15 mil	15 mil	Figure 6-5
MCH to DIMM1 Trace Length	1.8” to 6.0”	1.8” to 6.0”	Figure 6-11
DIMM to DIMM Trace Length	0.8” to 1.2”	0.8” to 1.2”	Figure 6-11
CKE_x Stub Trace Length	< 300 mil	< 300 mil	Figure 6-11
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	Figure 6-11
Termination Resistor (Rtt)	39.2 Ω ± 1% / 33.2 Ω ± 1%[1]	34.8 Ω ± 1%	Figure 6-11
MCH Breakout Guidelines	5/5, < 500 mil	5/5, < 500 mil	

NOTES:
1. On a compatible motherboard, use a 33.2 Ω for an E7500 chipset MCH and a 39.2 Ω for an E7501 chipset MCH.

Figure 6-11. CKE Topology



NOTE: Indicated lengths measure from the MCH component pin to the DIMM connector pin.

6.7 DC Biasing Signals

The DC Biasing signals are DDR signals which are not channel configuration specific. Table 6-9 documents all of these signals, indicating the new names for many of these signals. Many of the E7501 chipset MCH usages have been changed from the original E7500 chipset MCH recommendation. This section documents a compatibility layout for both E7500 chipset MCH and E7501 chipset MCH with stuffing options, dependant on which MCH is used.

Table 6-9. DC Biasing Ball Differences Between Intel® E7500 Chipset MCH and Intel® E7501 Chipset MCH

Ball	Intel® E7500 Chipset MCH	Intel® E7501 Chipset MCH
AM22	RCVENIN_A#	No Connect
N30	RCVENIN_B#	No Connect
AG20	RCVENOUT_A#	RCVEN_A
R25	RCVENOUT_B#	RCVEN_B
AK17	DDRCVOH_A	DDRCVO_A
W32	DDRCVOH_B	DDRCVO_B
AN16	DDRCVOL_A	No Connect
V29	DDRCVOL_B	No Connect
AH17	DDRCOMP_A	DDRCOMP_A
W30	DDRCOMP_B	DDRCOMP_B
AK21,AM16, AL9,AJ7	DDRVREF_A[3:0]	DDRVREF_A[3:0]
AK27	DDRVREF_A4	Reserved
AJ28	DDRVREF_A5	ODTCOMP
N33,U26, AG32,AC25	DDRVREF_B[3:0]	DDRVREF_B[3:0]
E30,M25	DDRVREF_B[5:4]	Reserved

6.7.1 Receive Enable Signal

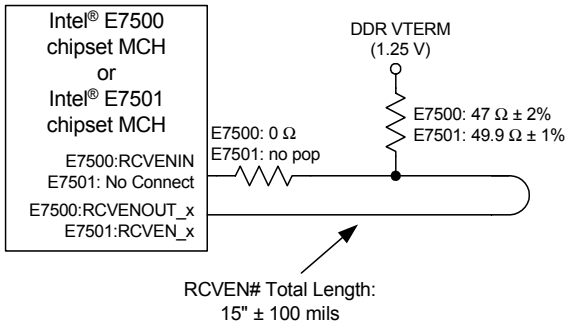
The E7500 chipset MCH uses the “receive enable” signal to determine the approximate round-trip flight time (command flight + data flight) to the DIMMs. Two pins exist on the MCH to facilitate the use of receive enable. RCVENOUT# is an output of the MCH and RCVENIN# is an input to the MCH. The board designer must connect RCVENOUT# to RCVENIN#. The length of the RCVEN# signal trace must be 15 inches ± 100 mils. Figure 6-12 illustrates the routing recommendations of the RCVEN# signal.

While the E7500 chipset MCH designs require this signal trace and a pull-up, the E7501 chipset MCH only requires a pull-up resistor (Rtt) to DDR VTERM on RCVEN. If your board will only use the E7501 chipset MCH, you do not need to route a 15-inch trace. Also, you do not need the isolation resistor nor the trace between the isolation resistor and the No Connect. Figure 6-12 summarizes these options.

Table 6-10. Receive Enable Routing Guidelines

Parameter	Intel® E7500 Chipset MCH	Intel® E7501 Chipset MCH
Signal Group	Receive Enable	
Topology	Feedback Loop	Pull-up
Trace Impedance (Z_0)	50 Ω ± 10%	50 Ω ± 10%
Nominal Trace Width	5 mil	5 mil
Nominal Trace Spacing	15 mil	15 mil
Trace Length - MCH RCVENIN to Rtt	< 1.0”	N/A
Termination Resistor (Rtt)	47 Ω ± 2%	49.9 Ω ± 1%
Total Length	15" ± 100 mils	No Requirement

Figure 6-12. Receive Enable Signal Routing Guidelines



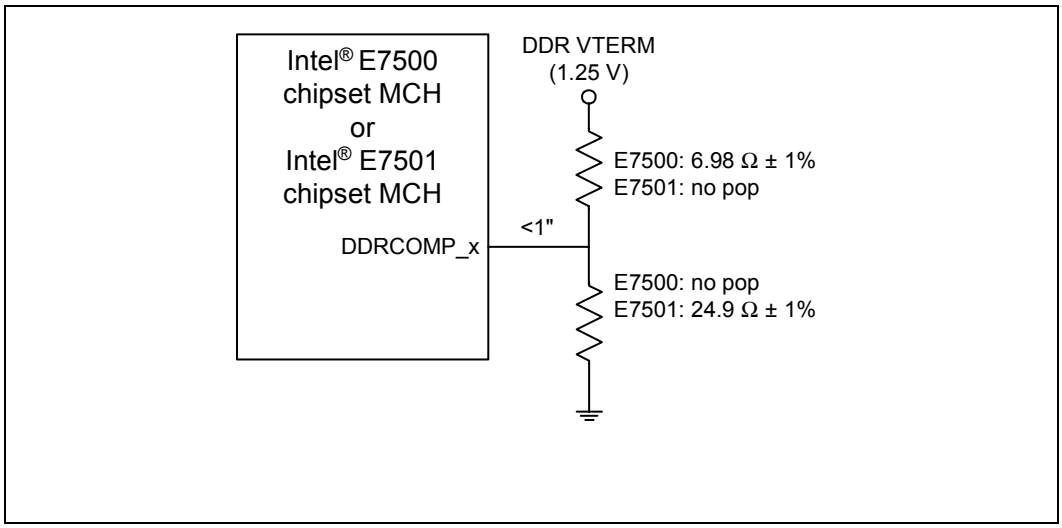
6.7.2 DDR Comp

The MCH uses DDRCOMP_x to calibrate the DDR channel buffers. This is periodically done by sampling the DDRCOMP pin on the MCH. The E7500 chipset MCH calibrates using a 6.98 Ω ± 1% pull-up to VTERM. The E7501 chipset MCH calibrates using a 24.9 Ω ± 1% pull-down to ground. This can be implemented by routing a 15-mil wide trace to a resistive network where the correct pull-up or pull-down is stuffed and the other is not populated, as depicted in Figure 6-13. Place a decoupling capacitor between the VTERM pull-up and any other terminations.

Table 6-11. DDRCOMP Routing Guidelines

Parameter	Intel® E7500 Chipset MCH	Intel® E7501 Chipset MCH
Topology	pull-up	pull-down
Nominal Trace Width	15 mil	15 mil
Nominal Trace Spacing	20 mil	20 mil
Trace Length - MCH to Rtt	< 1.0”	< 1.0”
Termination Resistor (Rtt)	6.98 Ω ± 1%	24.9 Ω ± 1%
Termination Voltage	DDR VTERM	Ground

Figure 6-13. DDRCOMP Resistive Compensation



NOTE: ‘x’ indicates channel A or B.

6.7.3 DDRVREF and ODTCOMP

The DDR system memory reference voltage (VREF) is used by the DRAM devices and the MCH to determine the logic level being driven on the data, command, and control signals. VREF of the receiving device must track changes in VTERM to maximize DDR interface margin. However, VTERM and VREF **cannot** be the same power plane due to the sensitivity of the DRAM VREF buffers to the termination plane noise. If a voltage regulator is used, it must reference VTERM (See Figure 6-14). If a local resistor divider is used, VREF and VTERM must have a common source voltage between them (i.e., both VREF and VTT are derived from the same voltage plane), and 1% resistors should be used (See Figure 6-15). Decouple VREF locally at the divider and DIMMs/MCH using one 0.1 uF capacitor per VREF pin.

On E7500 chipset platforms that implement a resistor divider network to obtain DDRVREF, the recommended resistor values for the MCH divider are 35.7 Ω pull-up to DDR VDD and a 37.4 Ω pull-down to ground. These values are chosen to assure ½ VDD at DDRVREF at the MCH. This change is to compensate for an electrical loading of the Intel E7500 chipset MCH. Failure to assure the accurate reference voltage can cause erratic behavior on the memory bus. For boards that are already in production, ensure that the values of DDRVREF at the DIMMs and at the MCH are within 1% of each other. This does not apply to the E7501 chipset MCH. Continue to use equal resistor values to derive DDRVREF at the DIMMs and for the E7501 chipset MCH.

Figure 6-14. DDRVREF Voltage Regulator

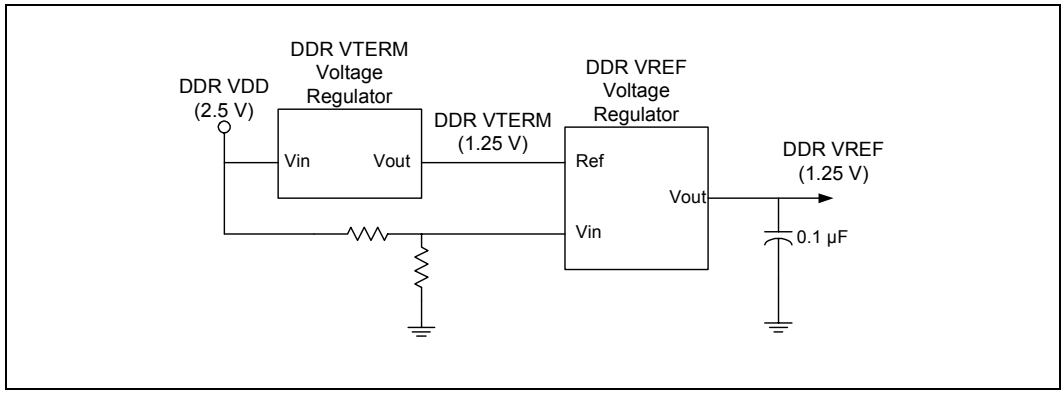
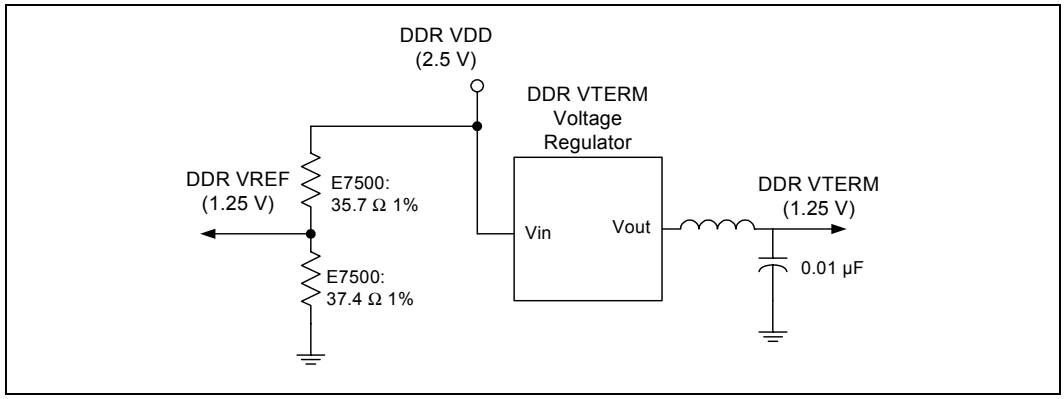


Figure 6-15. DDRVREF Voltage Divider

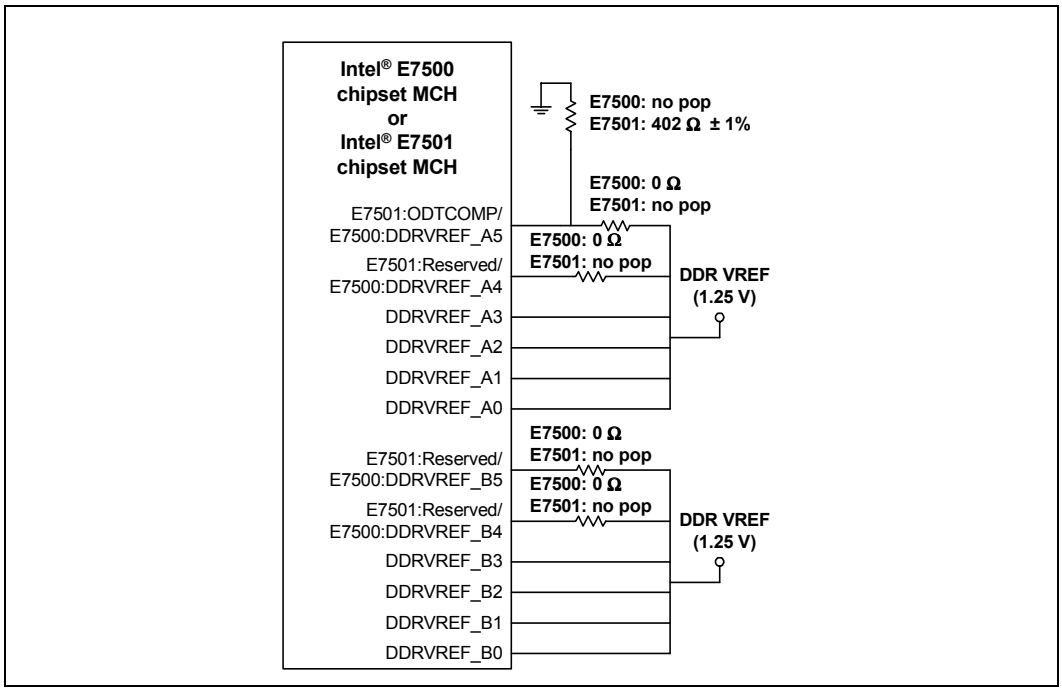


NOTE: The resistor values only apply to supply VREF to the MCH when an E7500 chipset MCH is populated. Use equal resistor values at the DIMMs and for the E7501 chipset MCH.

ODTCOMP, a redefined pin on the E7501 chipset MCH, is connected to the E7500 chipset MCH DVREF_A5 pin. The E7501 chipset MCH includes active read-cycle termination for all source synchronous signals (DQ and DQS signals). This On-Die-Termination (ODT) serves to control signal swing at the MCH receiver during read cycles. It does not function during write cycles. The ODT circuit has the effect of a weak pull-up of 200 Ω ± 15% to VTT. The value of termination is not adjustable. The ODT reduces ringbacks and overshoots, and in some cases can help reduce the need for series termination.

The E7500 chipset MCH has six VREFs per channel (12 total) while the E7501 chipset MCH only has four VREFs per channel (eight total). The remaining four pins on the E7501 chipset MCH must be separated from the DDRVREF plane. This can be done using 0 Ω isolation resistors between the pins and the plane. Route DDRVREF and ODTCOMP traces 5-mil wide. When the E7500 chipset MCH is used, the isolation resistors should be stuffed. When the E7501 chipset MCH is used, the isolation resistors should **not** be stuffed. When the E7500 chipset MCH is used, do not stuff the ODTCOMP pull-down. When the E7501 chipset MCH is used, stuff the 402 Ω pull-down.

Figure 6-16. Routing DDRVREF and ODTCOMP



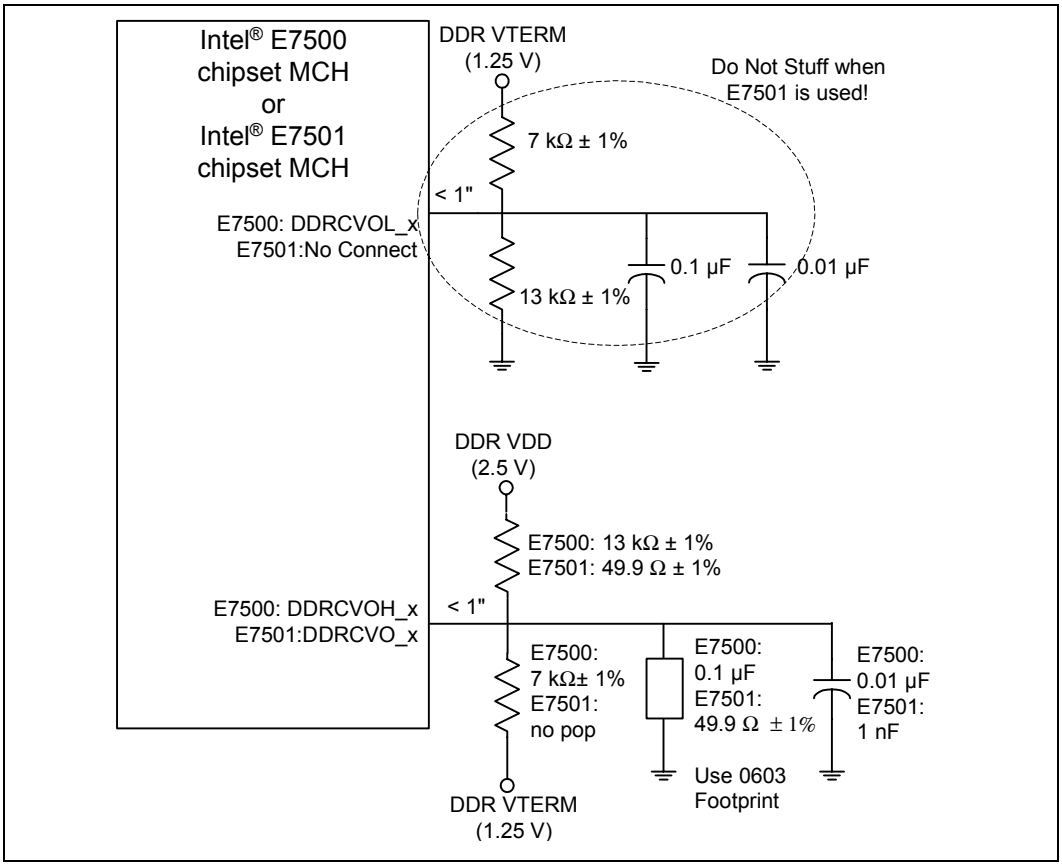
6.7.4 DDRCVO

The MCH uses a compensation signal to adjust buffer characteristics and output voltage swing over temperature, process, and voltage skew. Calibration is done periodically by sampling the DDRCVO_x pins on the MCH. Place the voltage divider network (Figure 6-17) within 1 inch of the MCH. When an E7501 chipset MCH is used on a compatible board, all of the components on the DDRCVOL circuit do not need to be stuffed, as shown in Figure 6-17. Also, a compatible footprint should be used between the resistor and the capacitor stuffing options. A 0603 resistor is sufficient for power dissipation. For an E7501 chipset MCH only design, omit the entire upper circuit in Figure 6-17 from the board. Also, on E7501 chipset MCH only designs, the empty pull-down stuffing option to DDR VTERM is not needed.

Table 6-12. DDRCVOL and DDRCVOH Routing Guidelines

Parameter	Intel® E7500 Chipset MCH	Intel® E7501 Chipset MCH
Topology	Resistor Divider	Resistor Divider
Nominal Trace Width	15 mil	15 mil
Nominal Trace Spacing	20 mil	20 mil
Trace Length - MCH to Divider	< 1.0”	< 1.0”

Figure 6-17. DDRCVOL, DDRCVOH, and DDRCVO Network

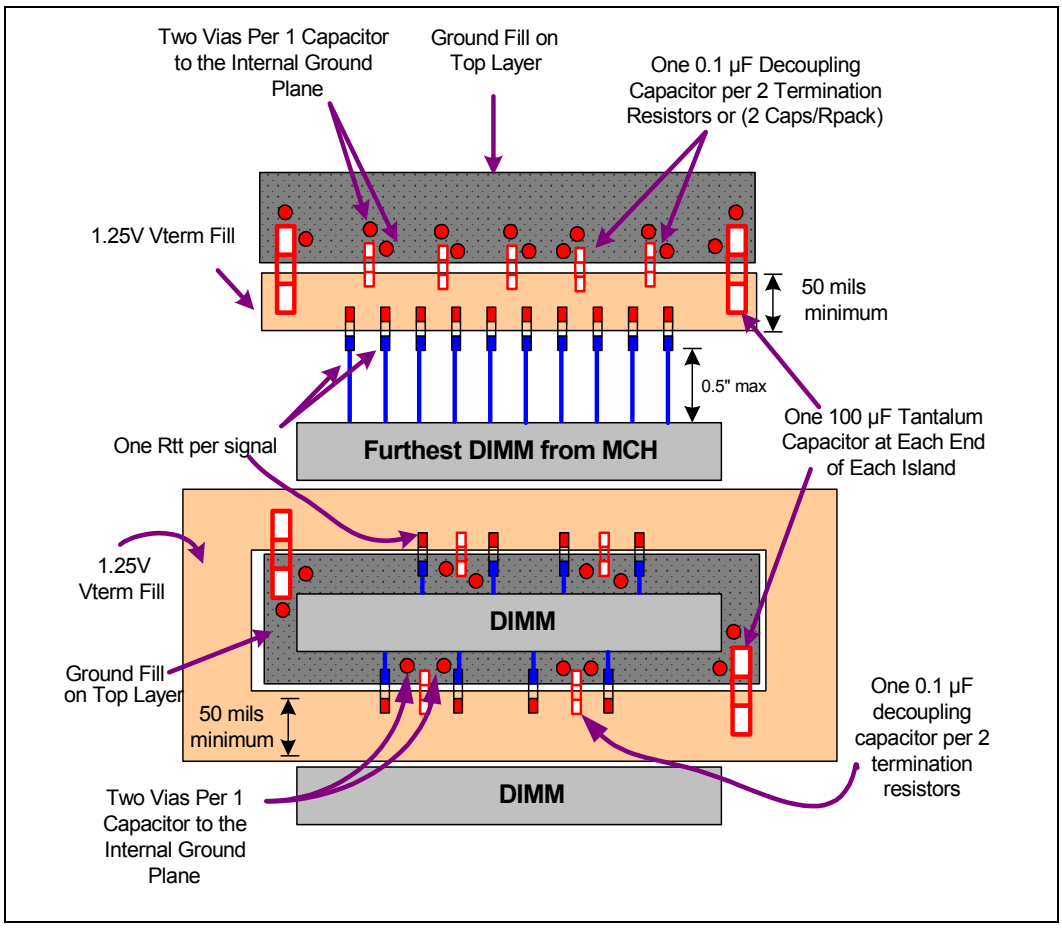


NOTE: ‘x’ indicates channel A or B.

6.8 DDR Signal Termination and Decoupling

Place a 1.25 V termination plane on the top layer, just beyond (within 0.5 inch) the DIMM connector furthest from the MCH on each channel, as shown in Figure 6-18. The VTERM island must be at least 50-mils wide. Use this termination plane to terminate all DIMM signals, using one Rtt resistor per signal. Decouple the VTERM plane using one 0.1 µF decoupling capacitor per two termination resistors. Each decoupling capacitor must have at least two vias between the top layer ground fill and the internal ground plane. In addition place one 100 µF Tantalum capacitor on each end of the termination island for bulk decoupling. Refer to Figure 6-18.

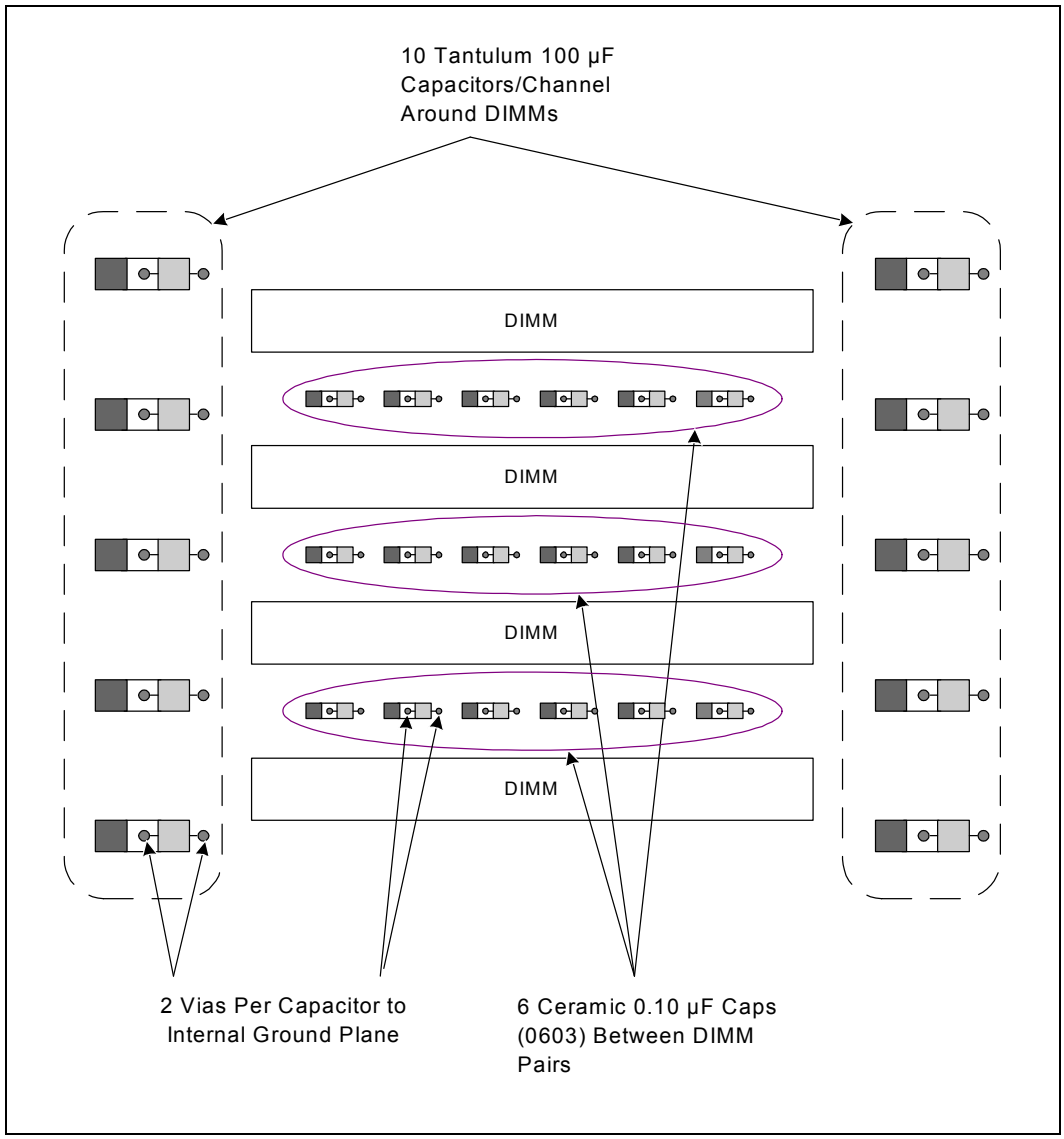
Figure 6-18. DDR VTerm Plane



6.9 2.5 V Decoupling Requirements

Decouple the DIMM connectors as shown in Figure 6-19. Place six ceramic 0.1 µF (0603) capacitors between each pair of DIMM connectors. Place ten Tantalum 100 µF capacitors around the DIMM connectors per channel, keeping them within 0.5 inch of the DIMM connectors.

Figure 6-19. DIMM Decoupling



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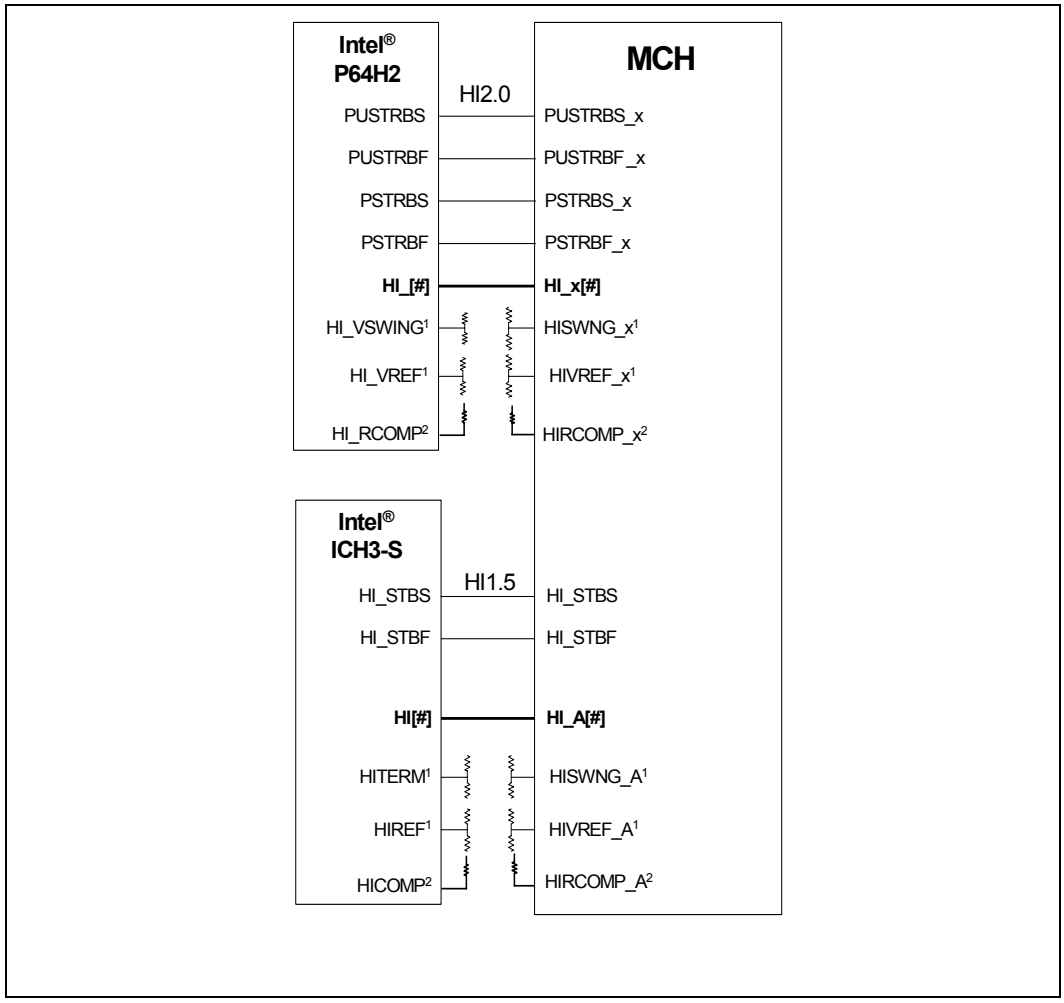
Hub Interface 7

7.1 Signal Naming Convention

Figure 7-1 has the Hub Interface 2.0 and Hub Interface 1.5 signal naming convention for each component. This figure is intended to give a quick naming cross reference to designers. The specific guidelines and implementation on these signals are given in the following sections. Note that throughout the document, the "x" part of the MCH signal has been dropped for simplicity.

Figure 7-1. Signal Naming Convention on Both Sides of the Hub Interfaces



NOTES:
1. These signals have individual resistor dividers. For specific values, refer to Figure 7-5 and Figure 7-8.
2. These signals have individual pull-up resistors. For specific values, refer to Figure 7-6 and Figure 7-9.
3. Signal names for HI2.0 on the MCH: x = B, C, or D.

7.2 Hub Interface 2.0 Implementation

The MCH and P64H2 ballout assignments are optimized to simplify the hub interface routing between these devices. To allow for greater flexibility in design, a connector can be placed on the interface to access a HI2.0 agent that resides on an adapter card. The typical card implementation uses an extension to the 3.3 V PCI-64 connector that provides an additional 70 pins for HI2.0. Power, JTAG and SMBus signals are taken from the PCI portion of the connector. The remaining PCI signals are unused. This approach provides the flexibility to allow either a PCI/PCI-X card or a HI2.0 card to be populated in the slot.

For the 16-bit hub interface, HI[7:0] and HI[20] are associated with PSTRBF and PSTRBS, and HI[15:8] and HI[21] are associated with PUSTRBF and PUSTRBS. HI[18:16] are common clock signals; they are sampled using CLK66. The three hub interfaces on the MCH are functionally and electrically identical. Therefore, these guidelines apply to all three hub interfaces.

Table 7-1. Hub Interface 2.0 Signal/Strobe Association

Data Group	Associated Strobes
HI[7:0] HI[20]	PSTRBF PSTRBS
HI[15:8] HI[21]	PUSTRBF PUSTRBS

7.2.1 Hub Interface 2.0 High-Speed Routing Guidelines

This section documents the routing guidelines for the Hub Interface 2.0. The Hub Interface 2.0 signal groups are listed in Table 7-2. The general routing guidelines for the Hub Interface 2.0 signals are given in Table 7-3.

Table 7-2. Hub Interface 2.0 Signal Groups

Group	Signal	
	MCH	Intel® P64H2
Common Clock Signals	HI[18:16]_x	HI[18:16]
Source Synchronous Signals	HI[21:20]_x, HI[15:0]_x, PSTRBF, PSTRBS, PUSTRBF, PUSTRBS	HI[21:20],HI[15:0], PSTRBF, PSTRBS, PUSTRBF, PUSTRBS
Miscellaneous Signals	HIRCOMP_x, HISWNG_x, HIVREF_x	HI_RCOMP, HI_VSWING, HI_VREF

NOTE: x = B, C, or D

Table 7-3. Hub Interface 2.0 Routing Parameters

System Type	Trace Length Min-Max (For HI2.0 Device Down)	Trace Length Min-Max (For HI2.0 Card Solution)	Trace Z_0	Trace Width/Spacing	Breakout Width/Spacing
533 MHz	3” – 20”	3” – 14”	50 Ω ± 10%	5/15 mils	5/5 mils (max dist = 0.5”)

The hub interface signals must be routed directly from the MCH to P64H2 with all signals referenced to ground. Maintain a consistent ground reference plane at all times. In addition, route all signals within a data group (consisting of nine bits of data and a pair of strobes) on the same layer and reference them to the same ground plane. Keep layer transitions to a minimum. If a layer change is required, use only two vias per net and keep all signals within a data group on the same layer.

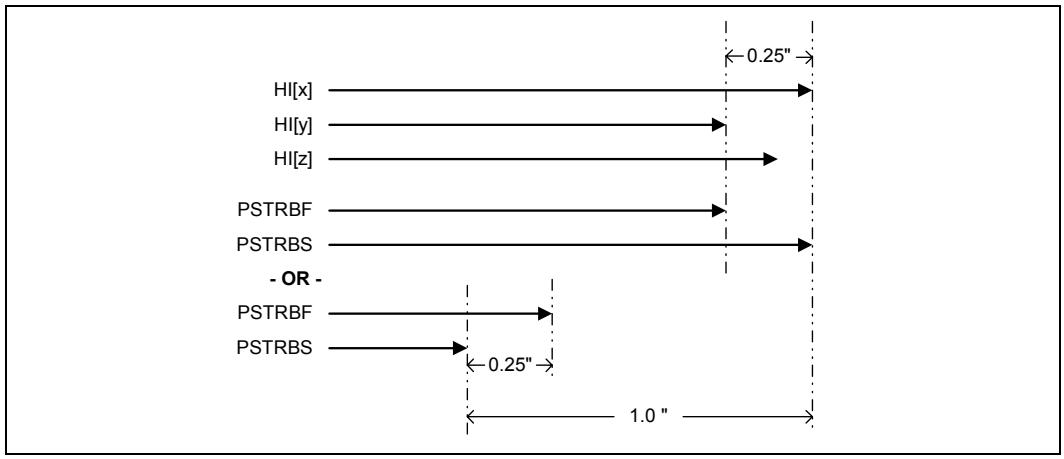
Route the Hub Interface 2.0 data signal traces 5-mils wide using the recommended stack-up. There must be 15-mils spacing between data signal traces (5/15). Each strobe signal must have a minimum of 35 mils of spacing from any adjacent signals to minimize effects that cause signal degradation. To break out of the MCH and P64H2 package, the hub interface data signals can be routed 5/5. The signals must separate to 5/15 (or strobes to 5/35) within 0.5 inch of the package.

Hub Interface 2.0 requires package length compensation, which is similar to the system bus package length compensation. For E7500/E7501 chipset component package lengths, refer to the component datasheets.

For Hub Interface 2.0 devices on the motherboard, trace length matching of ± 0.25 inch (including package length compensation) is required among all signals within a data group. If the hub device is on an adapter, length matching of ± 0.125 inch (including package length compensation) is required among all signals within a data group. The hub interface strobe trace lengths must be 0 to 1 inch shorter than the longest hub interface data trace.

Figure 7-2 depicts the length matching rules for a hub device on the motherboard. All of the hub interface data signals must be length matched within 0.25 inch. The figure shows HI[x] and HI[y] with the maximum allowed difference in length, while HI[z] is somewhere in the middle. The strobes in each strobe pair (PSTRBF and PSTRBS; PUSTRBF and PUSTRBS) are also matched within 0.25 inch. However, the absolute length of the strobe pair is adjusted according to the **longest hub interface data line**. The upper pair shows the case where one of the strobes is the same **exact** length as the longest hub interface data line (which is the longest possible length one of the strobes can be). In this case, the other strobe **must** be equal to or shorter than it, but by no more than 0.25 inch. The lower strobe pair shows the case where one of the strobes is **exactly** 1 inch shorter than the longest hub interface data line (which is the shortest possible length one of the strobes can be). In this case, the other strobe **must** be equal to or longer than it, but by no more than 0.25 inch.

Figure 7-2. Hub Interface 2.0 Length Matching



NOTES:
1. All signal lines with arrows depict the total length of the signal including the mother board trace length, MCH package trace length, and P64H2 device trace length.
2. PUSTRBF and PUSTRBS length matching is the same as for PSTRBF and PSTRBS.
3. This figure is only an example for an implementation with the device on the motherboard. For an implementation with the hub interface device on a riser card, simply replace both instances of 0.25 inch with 0.125 inch.
4. In the example above, HI[x], HI[y], and HI[z] represent Hub Interface data signals. The other six data signals in the group must also be matched within 0.25 inch. The associated strobe pair must be within 1.0 inch of the longest data signal.

Hub Interface 2.0 has a minimum trace length requirement of 3 inches, and a maximum trace length requirement of 20 inches for a device on the motherboard implementation for all hub interface signals (using an internal routing layer on the recommended stack-up). However, for a device on an adapter card plugged in a Hub Interface 2.0 connector, the maximum motherboard trace length is 14 inches. (3 inches for card routing and 3 inches for connector skew.) For a riser card topology, the maximum trace length would reduce by 3 inches to (11-Y) inches, where Y is the riser card trace length. The riser must be built to not exceed the maximum trace length with the motherboard routed length.

Figure 7-3. Hub Interface 2.0 Routing Guidelines for Device Down Solutions

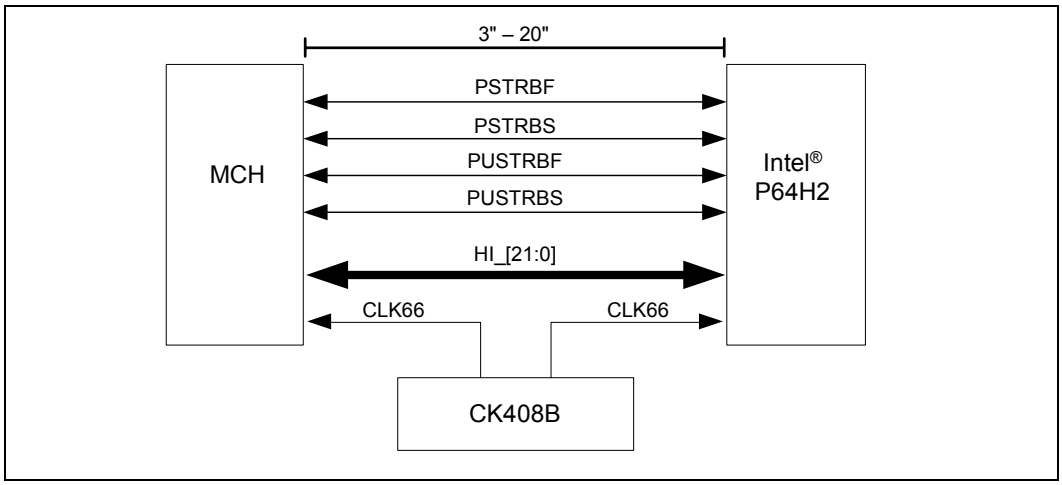
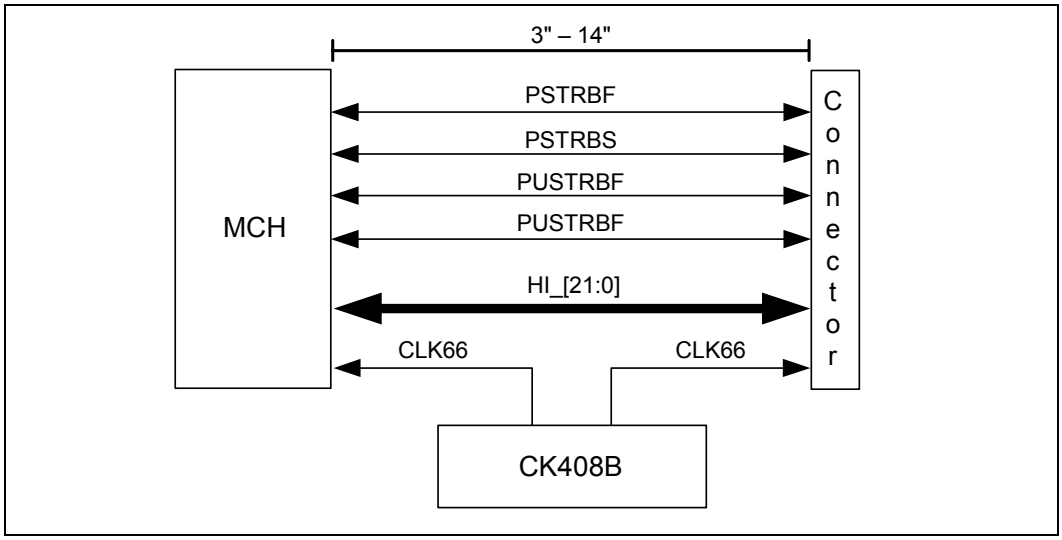


Figure 7-4. Hub Interface 2.0 Routing Guidelines for Hub Interface Connector Solutions



NOTE: The 14-inch maximum length allows for a single connector and 3-inch adaptor card trace length. The PCI connector is an equivalent 3-inch electrical length. The maximum motherboard trace length must be shortened if additional trace is allocated for the trace of a riser card, making sure to also subtract the additional equivalent trace of a second connector.

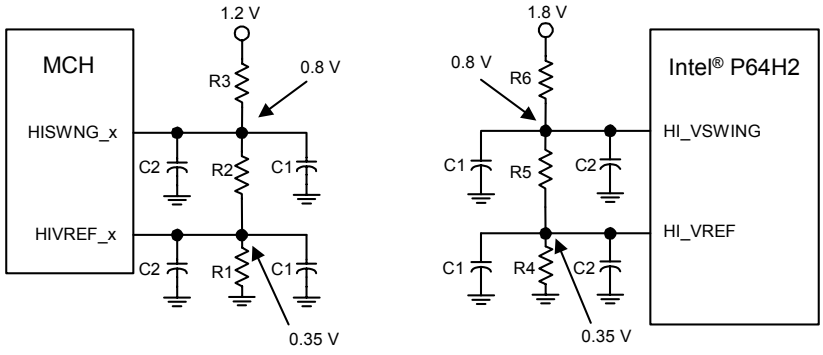
7.2.2 Hub Interface 2.0 Generation/Distribution of Reference Voltages

The nominal Hub Interface 2.0 reference voltage is 0.350 V ± 5%. Each Hub Interface 2.0 on the MCH has a dedicated HIVREF pin to sample this reference voltage. Similarly, the P64H2 has a dedicated reference voltage pin. In addition to the reference voltage, a reference swing voltage must be supplied to control buffer voltage swing characteristics. The nominal Hub Interface 2.0 reference swing voltage should be 0.8 V ± 5% for the MCH and P64H2. Each Hub Interface 2.0 on the MCH has a dedicated HISWNG pin to sample this reference swing voltage. The P64H2 has a dedicated reference swing voltage pin as well. Both of these reference voltages can be generated locally with a single voltage divider circuit. Figure 7-5 shows an example voltage divider circuit.

Table 7-4. Hub Interface 2.0 Reference Circuit Specifications

Reference Voltage Specification (V)	Reference Swing Voltage Specification (V)	1.2 V Voltage DIvider Circuit Recommended Resistor Values (Ω)	1.8 V Voltage DIvider Circuit Recommended Resistor Values (Ω)	Decoupling Requirements (µF)
0.350 ± 5%	For Intel® P64H2 = 0.8 ± 5% For MCH = 0.8 ± 5%	R1 = 392 ± 1% R2 = 499 ± 1% R3 = 453 ± 1%	R4 = 261 ± 1% R5 = 332 ± 1% R6 = 750 ± 1%	C1 = 0.1 C2 = 0.01

Figure 7-5. Hub Interface 2.0 with Locally Generated Voltage Divider Circuit



The resistor values R1, R2, R3, R4, R5, and R6 must be rated at ± 1% tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A 0.1 µF capacitor (C1 in the above circuits) should be placed close to each resistor divider, and a 0.01 µF bypass capacitor (C2 in the above circuits) should be placed near each reference voltage pin. If the length of the trace from the voltage divider to the pin is greater than 1 inch, place more than one 0.01 µF capacitor near the reference voltage pin. The trace length from the voltage divider circuit to the corresponding pin must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed 20 mils to 25 mils from all other signals.

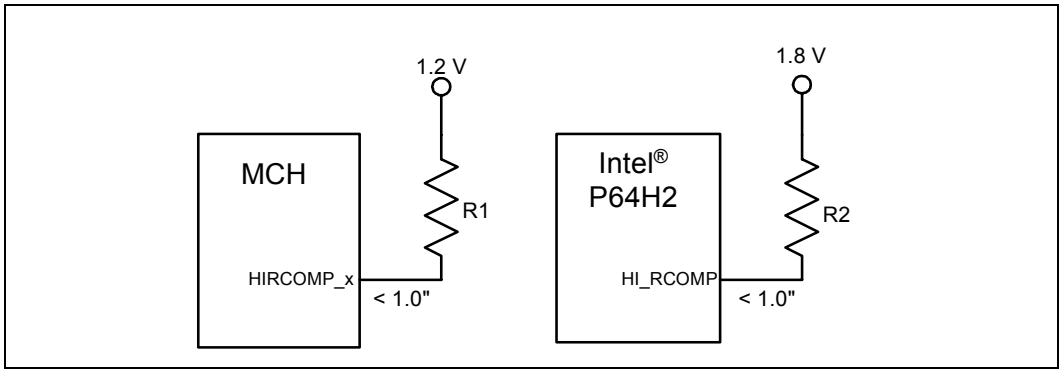
7.2.3 Hub Interface 2.0 Resistive Compensation

The hub interface uses a resistive compensation signal (HIRCOMP_x) to compensate buffer characteristics across temperature, voltage, and process. The HIRCOMP_x resistor values are given in Table 7-5. Figure 7-6 shows the RCOMP_x circuits. The length of the trace from the component to the pull-up must be less than 1 inch and have a trace impedance of 50 Ω ± 10%.

Table 7-5. Hub Interface 2.0 RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	50 Ω ± 10%	R1 = 24.9 Ω ± 1%	VCC1_2
Intel® P64H2	50 Ω ± 10%	R2 = 61.9 Ω ± 1%	VCC1_8

Figure 7-6. Hub Interface 2.0 RCOMP Circuits



7.2.4 Hub Interface 2.0 Decoupling Guidelines

To improve I/O power delivery, use two, 0.1 µF capacitors per component (i.e., MCH, P64H2). These capacitors should be placed within 150 mils of each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_8/VCC1_2 side of the capacitors to the VCC1_8/VCC1_2 power pins. Similarly, if layout allows, metal fingers running on the VCC1_8/VCC1_2 side of the board should connect the ground side of the capacitors to the VSS power pins.

7.2.5 Unused Hub Interface 2.0 Interfaces

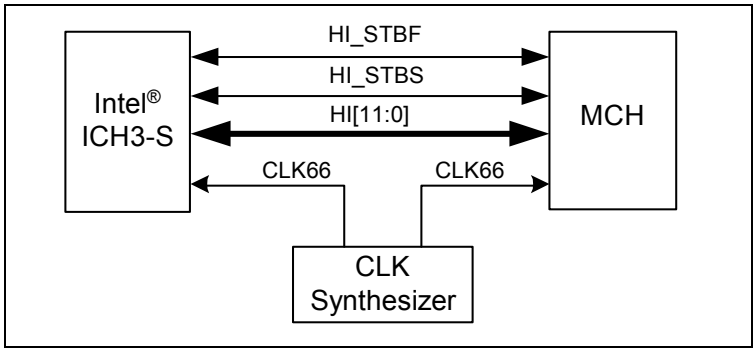
Terminate unused Hub Interface 2.0 interfaces as described below:

- All hub interface data and strobe, HIRCOMP_x, and HISWNG_x signals can be left as no connects.
- HIVREF must be tied low to ground.

7.3 Hub Interface 1.5 Implementation

The Hub Interface 1.5 signals HI[7:0] are associated with HI_STBS/HI_STBF. For those familiar with Hub Interface 1.0, HI_STBF and HI_STBS are called HI_STB# and HI_STB, respectively.

Figure 7-7. 8-Bit Hub Interface 1.5 Routing



This section documents the routing guidelines for the Hub Interface 1.5 that is responsible for connecting the MCH to the ICH3-S. Hub Interface 1.5 supports parallel termination mode only; therefore, the DPRSLPVR pin on the ICH3-S must be left as No Connect (NC); this signal has an internal pull-down.

7.3.1 Hub Interface 1.5 High-Speed Routing Guidelines

The Hub Interface signals must be routed directly from the MCH to ICH3-S with all signals referenced to ground. Maintain a consistent ground reference plane at all times. In addition, route all signals within a data group (consisting of nine bits of data and a pair of strobes) on the same layer and reference them to the same ground plane. Keep layer transitions to a minimum. If a layer change is required, use only two vias per net and keep all signals within a data group on the same layer.

The Hub Interface 1.5 signal groups are listed in Table 7-6. The general routing guidelines for the Hub Interface 1.5 signals are given in Table 7-7.

Table 7-6. Hub Interface 1.5 Signal Groups

Group	Signals	
	MCH	Intel® ICH3-S
Common Clock Signals	HI_A[11:8]	HI[11:8]
Source Synchronous Signals	HI_A[7:0], HI_STBF, HI_STBS	HI[7:0], HI_STBF, HI_STBS
Miscellaneous Signals	HIRCOMP_A, HISWNG_A, HIVREF_A	HICOMP, HITERM, HIREF

Table 7-7. Hub Interface 1.5 Routing Parameters

System Type	Trace Length Min-Max	Trace Z_0	Trace Width/Spacing	Breakout Width/Spacing
266 MHz	3” – 20”	50 Ω ± 10%	5/15 mils	5/5 mils (max dist = 0.5”)

Route the Hub Interface 1.5 data signal traces 5 mils wide using the recommended stack-up. There must be 15 mils spacing between data signal traces (5/15). Each strobe signal must have a minimum of 35 mils of spacing from any adjacent signals to minimize effects that cause signal degradation. To break out of the MCH and ICH3-S package, the hub interface data signals can be routed 5/5. The signals must separate to 5/15 (or strobes to 5/35) within 0.5 inch of the package.

For Hub Interface 1.5 devices on the motherboard, each strobe signal trace must be the same length, and each data signal trace must be matched with respect to the strobes within ± 0.1 inch.

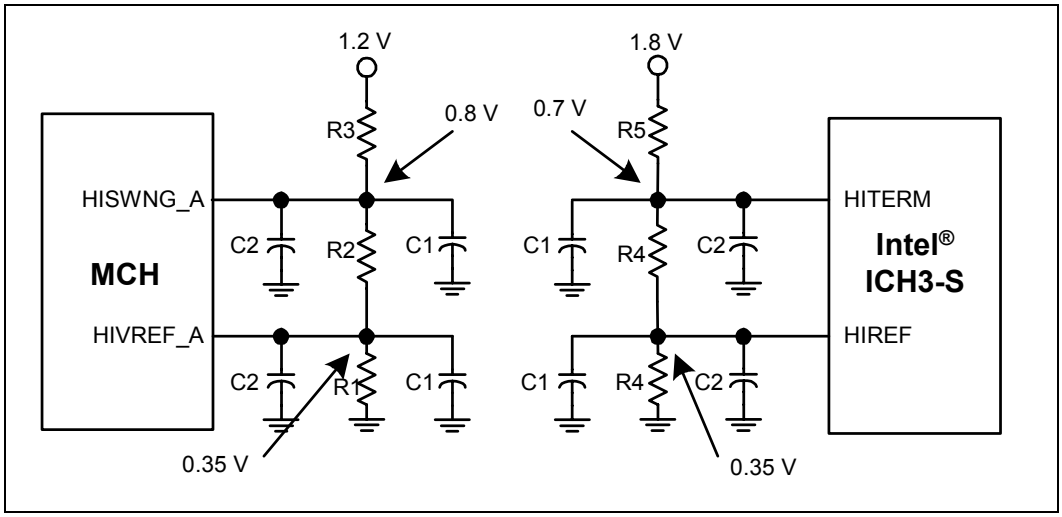
7.3.2 Hub Interface 1.5 Generation/Distribution of Reference Voltages

The nominal Hub Interface 1.5 reference voltage is 0.35 V ± 5%. The 8-bit Hub Interface on the MCH has a dedicated HIVREF pin to sample this reference voltage. In addition to the reference voltage, a reference swing voltage must be supplied to control buffer voltage swing characteristics. The nominal Hub Interface 1.5 reference voltage swing must be 0.8 V ± 5% for the MCH and 0.7 V ± 5% for the ICH3-S. This voltage is sampled by the MCH using HISWNG, and is sampled by the ICH3-S using HITERM (see Table 7-8). Both HISWNG and HITERM can be generated locally with a single voltage divider circuit as shown in Figure 7-8.

Table 7-8. Hub Interface 1.5 Reference Circuit Specifications

Reference Voltage Specification (V)	Reference Swing Voltage Specification (V)	1.2 V Voltage Divider Circuit Recommended Resistor Values (Ω)	1.8 V Voltage Divider Circuit Recommended Resistor Values (Ω)	Decoupling Requirements (µF)
0.35 ± 5%	For Intel® ICH3-S = 0.7 ± 5% For MCH = 0.8 ± 5%	R1 = 392 ± 1% R2 = 499 ± 1% R3 = 453 ± 1%	R4 = 261 ± 1% R5 = 825 ± 1%	C1 = 0.1 C2 = 0.01

Figure 7-8. Hub Interface 1.5 Locally Generated Reference Divider Circuits



The values of R1, R2, R3, R4 and R5 must be rated at ± 1% tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A 0.1 µF capacitor (C1 in Figure 7-8) should be placed within 0.5 inch of each resistor divider, and a 0.01 µF bypass capacitor (C2 in Figure 7-8) should be placed within 0.25 inch of reference voltage pins. If the length of the trace from the voltage divider to the pin is greater than 1 inch, place more than one 0.01 µF capacitor near the reference voltage pin. The trace length from the voltage divider circuit to the HIREF and HUBREF pins must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed at least 20 mils to 25 mils from all other signals.

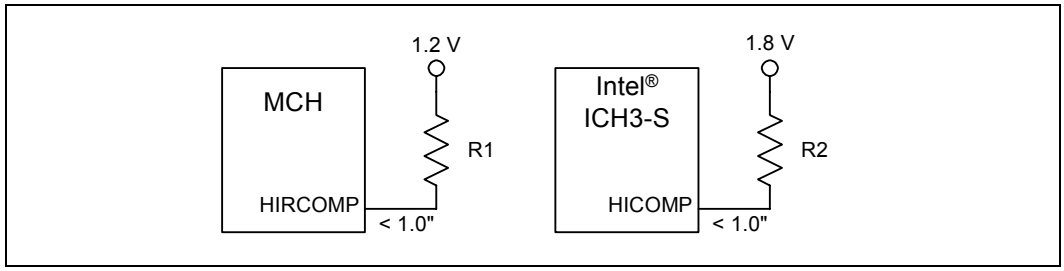
7.3.3 Hub Interface 1.5 Resistive Compensation

The hub interface uses a resistive compensation signal (RCOMP) to compensate buffer characteristics for temperature, voltage, and process. The HIRCOMP resistor values are given in Table 7-9. Figure 7-7 shows the RCOMP_x circuits. The length of the trace from the component to the pull-up must be less than 1 inch and have a trace impedance of 50 Ω ± 10%.

Table 7-9. Hub Interface 1.5 RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	50 Ω ± 10%	R1 = 24.9 Ω ± 1%	VCC1_2
Intel® ICH3-S	50 Ω ± 10%	R2 = 78.7 Ω ± 1%	VCC1_8

Figure 7-9. Hub Interface 1.5 RCOMP Circuits



7.3.4 Hub Interface 1.5 Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors per each component (i.e., the ICH3-S and MCH). These capacitors should be placed within 150 mils of each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_8/VCC1_2 side of the capacitors to the VCC1_8/ VCC1_2 power pins. Similarly, if layout allows, metal fingers running on the VCC1_8/VCC1_2 side of the board should connect the ground side of the capacitors to the VSS power pins.

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Intel® 82870P2 (P64H2) 8

The 82870P2 (P64H2) is a peripheral chip that performs PCI/PCI-X bridging functions between the Hub Interface 2.0 and the PCI bus. The P64H2 is an integral part of the E7500/E7501 chipset, bridging the MCH and the PCI/PCI-X bus. On the primary bus, the P64H2 uses a 16-bit data bus to interface with the Hub Interface 2.0, and on the secondary bus, it supports two, 64-bit PCI/PCI-X bus segments. Either of the secondary PCI/PCI-X bus interfaces can be configured to operate in PCI or PCI-X mode. Each PCI/PCI-X interface contains an I/OxAPIC with 24 interrupts and a Hot-Plug controller that supports each PCI/PCI-X bus segment.

8.1 PCI/PCI-X Design Guidelines

The P64H2 contains two PCI/PCI-X Interfaces. The PCI Interface has a 33-/66-MHz bus speed, and the PCI-X interface has a 66-/100-/133-MHz bus speed (see Table 8-1).

Table 8-1. PCI/PCI-X Frequencies

PCI		
Frequency	**Maximum Slots**	**Voltage**
33 MHz	6	3.3 V, 5 V
66 MHz	2	3.3 V

PCI-X		
Frequency	**Maximum Slots**	**Voltage**
66 MHz	4	3.3 V
100 MHz	2	3.3 V
133 MHz	1	3.3 V

NOTE: Frequencies specified are not the only ones supported, rather the maximum allowed in the configuration.

Intel simulated the PCI/PCI-X bus topologies shown in Section 8.1.2 and Section 8.1.3. If a platform implements a PCI/PCI-X topology not found in the following sections, it is the responsibility of the system designer to ensure the system meets the specified timings. The recommended lengths specified are not intended to replace thorough system simulations and validation.

8.1.1 General PCI-X Routing Guidelines

Most PCI-X signals are timing critical. The timing critical signals have length restrictions for propagation, setup, and hold requirements. Table 8-2 itemizes all timing critical and some of the non-critical signals. All of the topologies in the following sections itemize the lengths for the timing critical signals in configurations which Intel simulated.

Table 8-2. Simulated Timing Critical Signals

PxAD[63:0], PxC/BE[7:0]#, PxDEVSEL#, PxFRAME#, PxIRDY#, PxTRDY#, PxSTOP#, PxPERR#, PxSERR#, PxREQ[5:0]#, PxPLOCK#, PxPAR64, PxGNT[5:0]#, PCIXCAP, PxM66EN, Px_133EN, PxREQ64#, PxACK64#, PxIRQ[15:0]

The configurations enumerated in the following sections were simulated on a 50 Ω ± 10% board impedance. Route the signals stripline with 5-mil wide traces with 10-mil wide spacing (5/10).

PCI control signals always require pull-up resistors on the motherboard to ensure that they contain stable values when no agent is actively driving the bus. This includes FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, INTA#, INTB#, INTC#, INTD#. In addition the 64-bit extension signals REQ64#, ACK64#, AD[63:32], C/BE[7:4]#, and PAR64 require pull-ups.

In the special case of a 64-bit bus that only contains 64-bit devices down, the pull-ups for AD[63:32], C/BE[7:4]# and PAR64 may not be needed. If the device down drives AD[63:32], C/BE[7:4]# and PAR64 during a 32-bit transaction then pull-ups are not necessary. If the device down leaves AD[63:32], C/BE[7:4]#, and PAR64 floating during a 32-bit transaction, then pull-ups will be required. Refer to the datasheet or specification for the 64-bit device down to determine if pull-ups are necessary.

A PCI/PCI-X bus has a maximum rating. PCI buses may be down shifted to a lower rating depending on the devices plugged into the bus. PCI/PCI-X buses may not be upshifted. Table 8-3 lists the ordering of PCI/PCI-X mode and frequencies. This means that when PCI-X 133 MHz is specified, the configuration can run at any mode or frequency below it (see Table 8-3). Topologies specified at PCI-X 100 MHz configurations can run at any speed below it, but not PCI-X 133 MHz. PCI 66 MHz configurations can be run at PCI 66 MHz, PCI-X 66 MHz, or below. PCI-X 66 MHz configurations **may not** run at PCI 66 MHz.

Table 8-3. PCI/PCI-X Mode and Frequency Ordering

Bus Mode and Frequency Ordering
PCI-X 133 MHz
PCI-X 100 MHz
PCI 66 MHz
PCI-X 66 MHz
PCI 33 MHz

Note: All topologies documented are stated at the highest rated bus mode and frequency for the motherboard topology.

8.1.2 PCI/PCI-X Routing Requirements (No Hot-Plug Switch)

The P64H2 supports a large number of PCI/PCI-X configurations. The basic topology of the bus is shown in Figure 8-1. Multiple slots are connected in a daisy chain topology with the device(s) down on the motherboard at the end of the daisy chain. Table 8-4 documents the lengths for the configurations Intel simulated. These topologies can also be used for Hot-Plug parallel mode configurations where a Hot-Plug switch is not used.

Figure 8-1. Typical PCI/PCI-X Topology

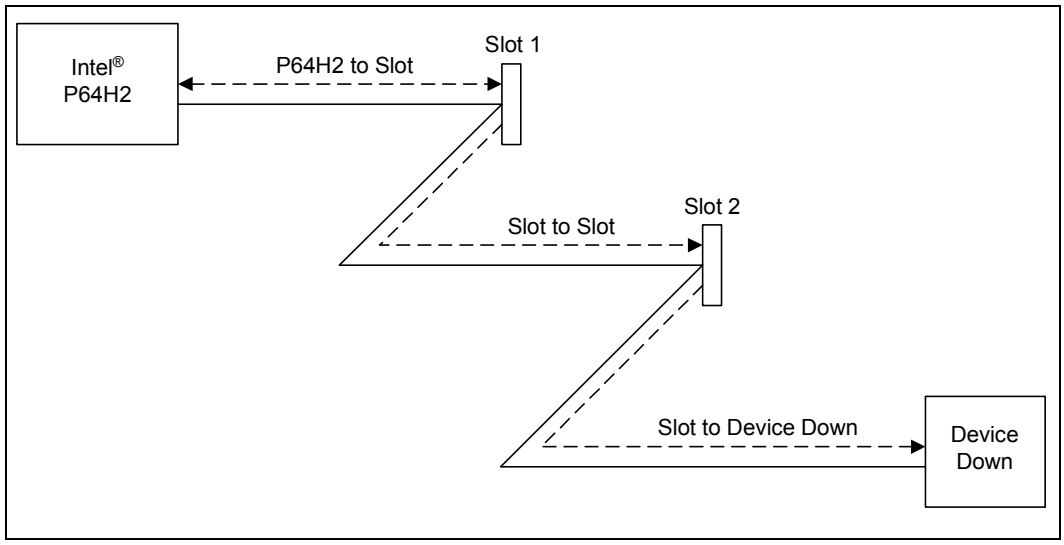


Table 8-4. Intel® P64H2 PCI/PCI-X Length Requirements

Configuration	Intel® P64H2 to Slot	Slot to Slot	Slot to Device Down
33 MHz, 5 slots / 1 device down	2.0” – 7.0”	1.0”	3.0” – 6.0”
66 MHz, 4 slots / 0 devices down	6.0” – 8.0”	1.5”	N/A
100 MHz, 2 slots / 0 devices down	5.0” – 8.0”	1.0” – 1.75”	N/A
100 MHz, 2 slots / 1 device down	3.0” – 3.5”	0.75”	2.5” – 3.0”
100 MHz, 1 slot / 2 devices down	2.0” – 4.0”	(device to device) 5.0”	2.0”
133 MHz, 1 slot / 0 devices down	1.0” – 8.25”[2]	N/A	N/A
133 MHz, 0 slots / 1 device down	1.25” – 10.0” (P64H2 to device)	N/A	N/A

NOTE:
1. During simulation, slot to slot lengths were held constant for some configurations. Therefore, no range can be given for these length requirements.
2. The 8.25 inches maximum only applies to the signals in the original 32-bit space. The 64-bit extension has a maximum length of 7.0 inches.

8.1.3 PCI/PCI-X Hot-Plug Switch Routing Requirements

The P64H2 supports a large number of PCI/PCI-X Hot-Plug serial mode configurations. These configurations require the usage of a Hot-Plug switch. The Hot-Plug topology of the bus is shown in Figure 8-2. Hot-Plug switches are connected in a daisy chain topology with the device(s) down on the motherboard at the end of the daisy chain. Table 8-5 documents the lengths for the configurations that Intel simulated.

Figure 8-2. Typical Hot-Plug Topology

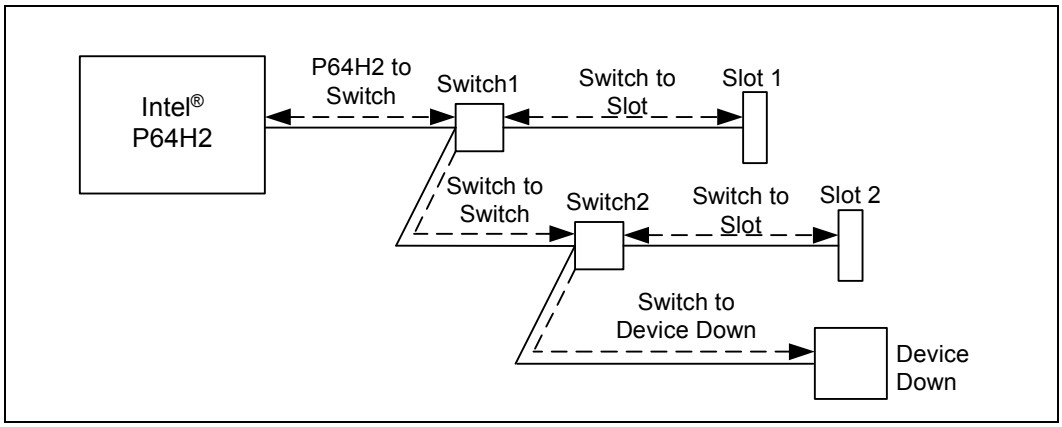


Table 8-5. Intel® P64H2 Hot-Plug Length Requirements

Configuration	Intel® P64H2 to Switch	Switch to Slot	Switch to Switch	Switch to Device Down
66 MHz, 4 Slots / 0 Device	2.0” – 6.0”	0.5” – 3.0”	0.5”	N/A
100 MHz, 2 Slots / 1 Device	2.5” – 3.5”	0.5” – 0.75”	0.75”	1.5” – 2.5”
100 MHz, 2 Slots / 0 Device	3.5” – 4.5”	1.0” – 1.75”	1.0” – 1.75”	N/A
100 MHz, 1 Slot / 1 Device	4.0” – 5.0”	1.75” – 2.25”	N/A	3.5” – 4.5”
133 MHz, 1 Slot / 0 Devices	1.5” – 3.5”	0.5” – 3.0”	N/A	N/A

NOTE: During simulation, slot to slot lengths were held constant for some configurations. Therefore, no range can be given for these length requirements.

8.1.4 Riser Card Topologies

The following guidelines are for systems that use a PCI-X riser card. A PCI-X riser card is a card containing PCI-X slots that is plugged into a PCI-X connector. These guidelines assume a PCI/PCI-X riser card with a 0.7 – 1.0 inch long trace length between slots. These simulations require the clocks for each device and riser card slot to be tuned within 500 ps, or 2.85 in, of each other. For the riser slot to also support a standard PCI/PCI-X adapter card, the tuning must also include the adapter card length.

The following topologies denote an upper and lower portion to the length requirements. The PCI specification requires the original 32-bit signals to have a card length of 0.75 to 1.5 inches. The 64-bit extension specifies the additional signals in the extension to have a length of 1.75 inches to 2.75 inches. Upper indicates the signals on the extension while Lower indicates signals lying in the original 32-bit space.

In some of the riser card topologies, series resistors are required. These series resistors must be placed on all signals listed in Table 8-2.

Figure 8-3 shows a PCI-X channel with a single connector used for a riser. If a 1 slot riser is used, the channel can be run up to PCI-X 133 MHz. If a three slot riser is used, the channel can be run up to PCI 66 MHz.

Figure 8-3. PCI-X Riser Card Topology

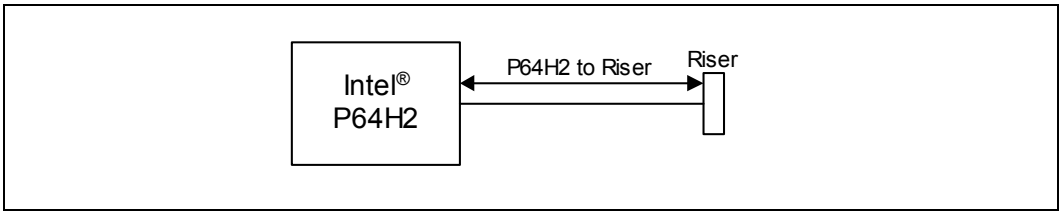


Table 8-6. PCI-X Riser Card Length Requirements

Configuration	Intel® P64H2 to Riser	
	Lower	Upper
PCI-X 133 MHz, 1 slot riser	1.0” – 7.25”	1.0” – 6.5”
PCI-X 66 MHz, 3 slot riser	1.0” – 8.25”	1.0” – 3.8”

Figure 8-4 shows a PCI-X channel with a device down before a riser card connector. If a one-slot riser is used, the channel can be run up to PCI-X 100 MHz. If a three-slot riser is used, the channel can be run up to PCI-X 66 MHz.

Figure 8-4. Device Down before PCI-X Riser Card Topology

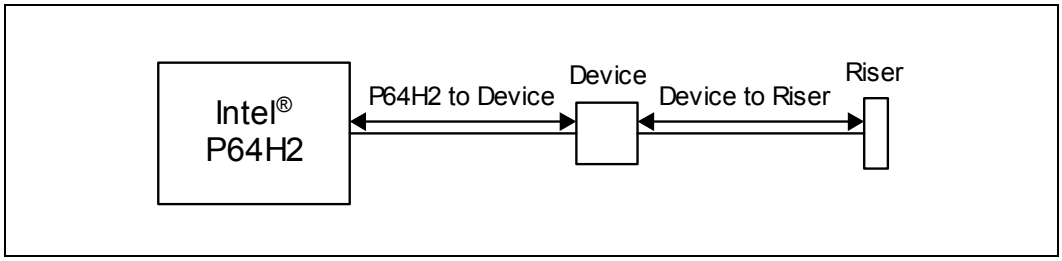


Table 8-7. Device Down before PCI-X Riser Card Length Requirements

Configuration	Intel® P64H2 to Device		Device to Riser	
	Lower	Upper	Lower	Upper
PCI-X 100 MHz, 1 slot riser	0.0” – 6.0”	0.0” – 5.0”	0.0” – 6.0”	0.0” – 5.0
PCI-X 66 MHz, 3 slot riser	1.0” – 6.0”	1.0” – 4.0”	1.0” – 4.0”	1.0” – 4.0”

Figure 8-5 shows a riser card topology with a device down after the riser card connector. The one-slot riser requires a 10 Ω series resistor on the riser between the riser fingers and the connector. The three-slot riser configuration cannot be run at PCI 66 MHz. It requires a 15 Ω series resistor on the baseboard between the P64H2 and the Riser connector closer to the riser. A second 15 Ω resistor is also need on the riser itself between the riser card fingers and the first connector.

Figure 8-5. Device Down after PCI-X Riser Card Topology

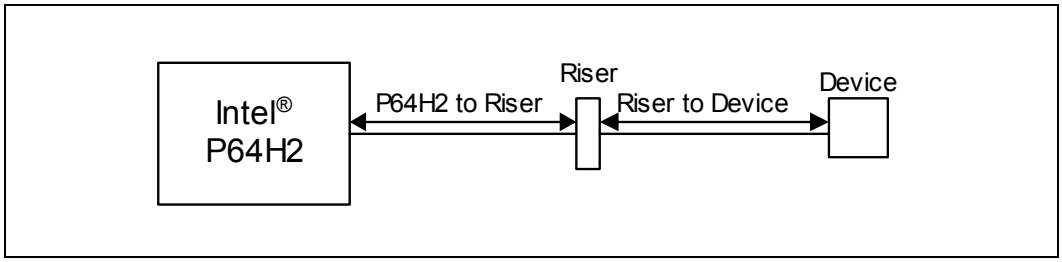


Table 8-8. Device Down after PCI-X Riser Card Length Requirements

Configuration	Intel® P64H2 to Riser		Riser to Device	
	Lower	Upper	Lower	Upper
PCI-X 100 MHz, 1 slot riser	0.0” – 8.0”	0.0” – 8.0”	0.0” – 8.0”	0.0” – 8.0”
PCI-X 66 MHz, 3 slot riser	1.0” – 6.0”	1.0”– 4.0”	1.0” – 4.0”	1.0” – 2.25”

Figure 8-6 shows a device down before a PCI-X riser card. Place a 22 Ω series resistor on the stub to riser leg, close to the riser itself. This topology can only be run at PCI 66 MHz or below.

Figure 8-6. Device Down with Stub before PCI-X Riser Card Topology

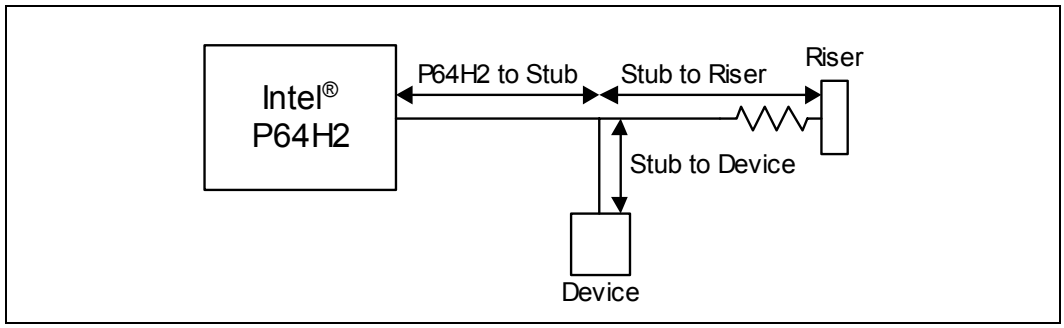


Table 8-9. Device Down with Stub before PCI-X Riser Card Length Requirements

Configuration	Intel® P64H2 to Stub		Stub to Riser		Stub to Device	
	Lower	Upper	Lower	Upper	Lower	Upper
PCI-X 66 MHz, 3 slot riser	3.3" – 5.6"	3.3" – 4.6"	0.2" – 2.3"	0.2" – 1.3"	1.9" – 6.5"	1.9" – 5.5"

8.1.5 PCI-X Two Devices Down Routing Requirements

The following guideline is for a system that uses two devices down on a singe PCI-X channel. A good example of usage for this configuration is an I/O Processor or RAID device and a SCSI controller. This channel can be run at PCI-X 100 MHz.

Figure 8-7. Two Devices Down Card Topology

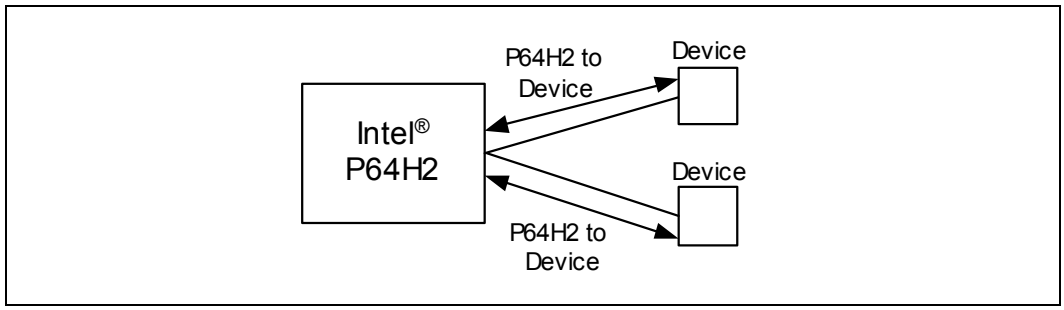


Table 8-10. Two Devices Down Length Requirements

Configuration	Intel® P64H2 to Device	
	Lower	Upper
100 MHz PCI-X	3.5" – 7.0"	3.5" – 7.0"

8.1.6 Clock Configuration

All PCI clocks must be disabled in the BIOS for any unused/unpopulated PCI/PCI-X slots. The PxPCLKO[5:0] pins can each be disabled by writing to the Disable PCLKOUT 5 – 0 bits (DPCLK, bits 15:10, configuration register offset 40h in each bridge). These clocks function the same in serial and dual-slot parallel modes. In serial mode, the PxPCLKO[5:0] signals are all driven low when the clock to the slot is disabled by the Hot-Plug controller, regardless of the DPCLK bits. Once the Hot-Plug controller connects the clock to the slot, these clocks are enabled again—which clocks are enabled does depend on DPCLK at this point. It is expected that PxPCLK0 will be connected to the PCI slot in single-slot parallel mode.

Figure 8-8. Hot-Plug Clock Topology

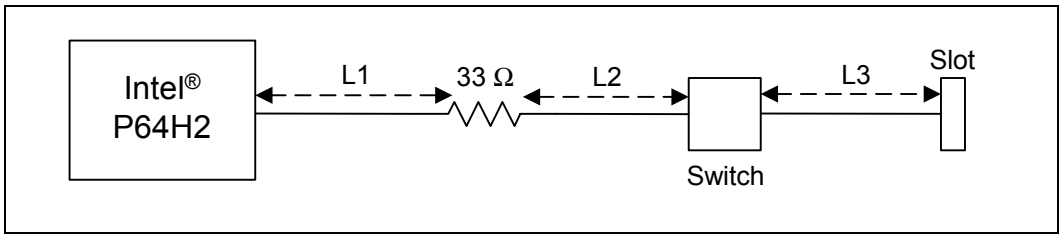


Table 8-11. Hot-Plug Clock Routing Length Parameters

Clock Speed	L1 (inches)	L2 (inches)	L3 (inches)
66 MHz	0.25 – 1.0	(L_{fbi} – L3) – 2.523	0.75 – 1.25
100 MHz	3.5 – 4.5	0.25 – 0.5 = L3	0.25 – 0.5 = L2
133 MHz	1.5 – 2.5	0.5 – 1.0 = L3	0.5 – 1.0 = L2

Figure 8-9. No Hot-Plug Clock Topology

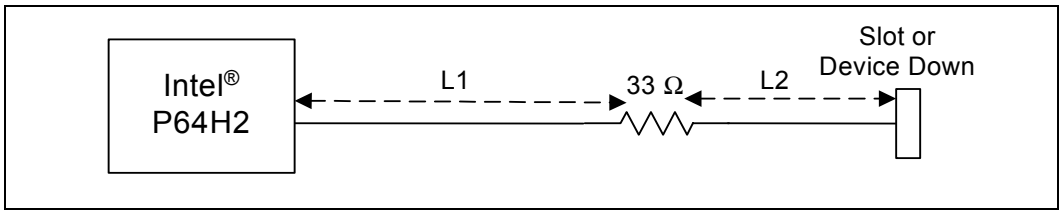


Table 8-12. No Hot-Plug Clock Routing Length Parameters

Clock Speed	L1 (inches)	L2 (inches) Slot	L2 (inches) Device Down
33 MHz Slot	3.5 – 5.5	0.5 – 5.0	2.9 – 7.9
66 MHz	3.5 – 4.5	0.5 – 1.0	3.0 – 3.5
100 MHz	≤ 1.0	L_{fbi} – 2.5[1]	L_{fbi}[1]
133 MHz	≤ 1.0	L_{fbi} – 2.5[1]	L_{fbi}[1]

NOTES:
1. The clock signal and feedback loops are closely related. L2 and L_{fbi} can be any length, but need to be tuned to each other ± 25 mils. Refer to Figure 8-9 for L2, and Figure 8-10 for L_{fbi}.

8.1.7 Loop Clock Configuration

You must tie PxPCLKO6 to PxPCLKI because this clock always runs and is needed by the internal PCI PLLs to properly align output signals with the external clocks by removing clock insertion delay. The PxPCLKO6 signal does not have to be routed through a bus switch before returning to PxPCLKI.

Figure 8-10. Loop Clock Topology

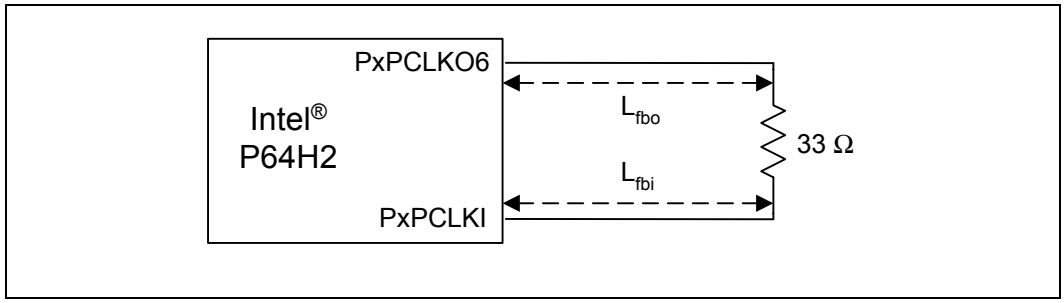


Table 8-13. Loop Clock Configuration Routing Length Parameters

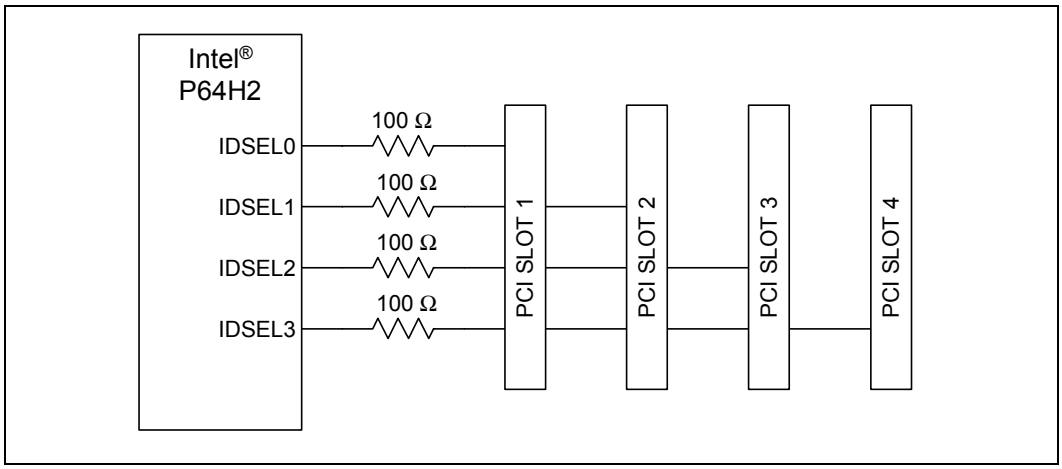
Clock Speed / Configuration	L_{fbo} (inches)	L_{fbi} (inches)
33 MHz / No HP	3.5 – 5.5	2.9 – 7.9
66 MHz / No HP	4.5 – 5.5	3.9 – 4.9
66 MHz / With HP	0.25 – 1.0	7.0 – 12.0
100 MHz / No HP	≤ 1.0	See Note
100 MHz / With HP	4.5 – 5.5	3.9 – 4.9
133 MHz / No HP	0.25 – 1.0	See Note
133 MHz / With HP	3.5 – 4.0	5.5 – 5.7

NOTE: L_{fbi} must be the same length (± 25 mils) as any device clock length on the same bus. If a device is down on the motherboard, L_{fbi} = L2. If a devices is on an expansion card, L_{fbi} = L2 + 2.5 inches. Refer to Figure 8-9 for L2 and Figure 8-10 for L_{fbi}.

8.1.8 IDSEL Implementation

Designers should use a 100 Ω series coupling resistor on the IDSEL signal when implementing PCI-X. Though the *PCI-X Addendum PCI Local Bus Specification, Revision 1.0* calls for a 2 kΩ resistor, the current specification, *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a* allows for other resistor values. See Figure 8-11 for an example of how to implement the coupling resistor. IDSEL mapping per P64H2 pin is arbitrary. However, AD16 is reserved.

Figure 8-11. IDSEL Sample Implementation Circuit



8.1.9 SMBus Address

The SMBus interface does not have configuration registers. The SMBus address is set by the states of pins PAGNT[5:4] and PBGNT[5:4] when PWROK is asserted as described in Table 8-14. Refer to the *Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet* for a more detailed description of P64H2 strap latching.

Table 8-14. SMBus Address Configuration

Bit	Value
7	1
6	1
5	PAGNT5
4	0
3	PAGNT4
2	PBGNT5
1	PBGNT4

NOTE: There is no bit 0 because it is the read/write direction indicator.

8.2 Hot-Plug Implementation

The P64H2 contains two integrated Hot-Plug controllers (one per PCI/PCI-X interface) that operate independently. These integrated controllers can be individually disabled or configured to operate in one of the three defined modes of operation: single-slot parallel mode, dual-slot parallel mode, and serial mode. This section describes each of these three modes of operation, as well as switch and button implementation and the Hot-Plug Standard Usage Model.

8.2.1 Standard Usage Model

To define a programming model for the Hot-Plug controllers (HPC), it is necessary to make some assumptions about the interface between a user and a Hot-Plug system that must be incorporated into the hardware solution. The programming model includes two LED indicators, one optional push button, and a sensor on the manually-operated retention latch (MRL) for each supported slot. See Section 8.2.2 for MRL and attention button implementation. Section 8.2.3 describes the LED indicators. For more information on the Hot-Plug Standard Usage Model, see the *PCI Standard Hot-Plug Controller and Subsystem Specification, Revision 1.0.*

Caution: Users must always notify the operating system via a software user interface or Attention Button (if present) before opening an MRL. This allows the operating system to isolate the slot from the PCI bus and unload the device driver gracefully. The unexpected opening of an MRL leads to unpredictable results, including data corruption, abnormal termination of the operating system, or damage to card or platform hardware.

8.2.1.1 Hot-Removals

1. User selects a slot holding an enabled add-in card and requests that slot be disabled.
   a. User interacts with a software user interface to request that slot be disabled.
   b. User confirms request. System software validates request and initiates slot power down sequence. Power Indicator LED blinks.

   – OR –

   a. User presses momentary Attention Button at that slot.
   b. Software interprets change on HxPRSNT# pin as a push button event. (Software ignores second interrupt on HxPRSNT# caused by button release.) Power Indicator LED blinks.
   c. User is permitted to cancel request within 5 seconds by pressing Attention Button again.
   d. System software validates request and initiates slot power down sequence.
2. System software waits for card activity on the PCI bus to end.
3. Hot-Plug controller asserts RST#, bus signals and clock lines are disconnected from the slot, and power is removed.
4. Power Indicator LED is turned off. User may open MRL, disconnect cables, and remove card.

8.2.1.2 Hot-Insertions

1. User selects an empty, disabled slot and opens MRL.
2. User inserts add-in card, closes MRL, and attaches cables to card.
3. User requests that slot be enabled.
   a. User requests that slot be enabled via a software user interface.
   b. Power Indicator LED next to slot blinks while system software validates request.

   – OR –

   a. User presses momentary Attention Button at that slot.
   b. Software interprets change on HxPRSNT# pin as a push button event. (Software ignores second interrupt on HxPRSNT# caused by button release.)
   c. User is permitted to cancel request within 5 seconds by pressing Attention Button again.
   d. Power Indicator LED next to slot blinks while system software validates request.
4. Hot-Plug controller asserts RST# to the slot; main supply voltages are present at the slot.
5. Clock and bus signals are connected to the slot; RST# is deasserted.
6. Power Indicator LED is turned on. The slot is ready for operation.

8.2.2 Hot-Plug Switch Implementation

The mechanical design for the chassis should include a manually-operated retention latch (MRL) that holds an add-in card in the slot. Each MRL should have an associated switch, optical device, or other type of sensor to indicate whether a slot is “opened” or “closed.” (Note that the terms opened and closed do not necessarily indicate the electrical state of the switches used, but should be thought of as a mechanical door that enables or disables cards to be installed or removed.) A slot can be auto-powered down should someone attempt to remove a card without first notifying the operating system. The mechanical design should be such that it is impossible for an expansion card to be removed without the switch indicating that the slot is open. The mechanical design should also prevent inadvertent switch “openings.”

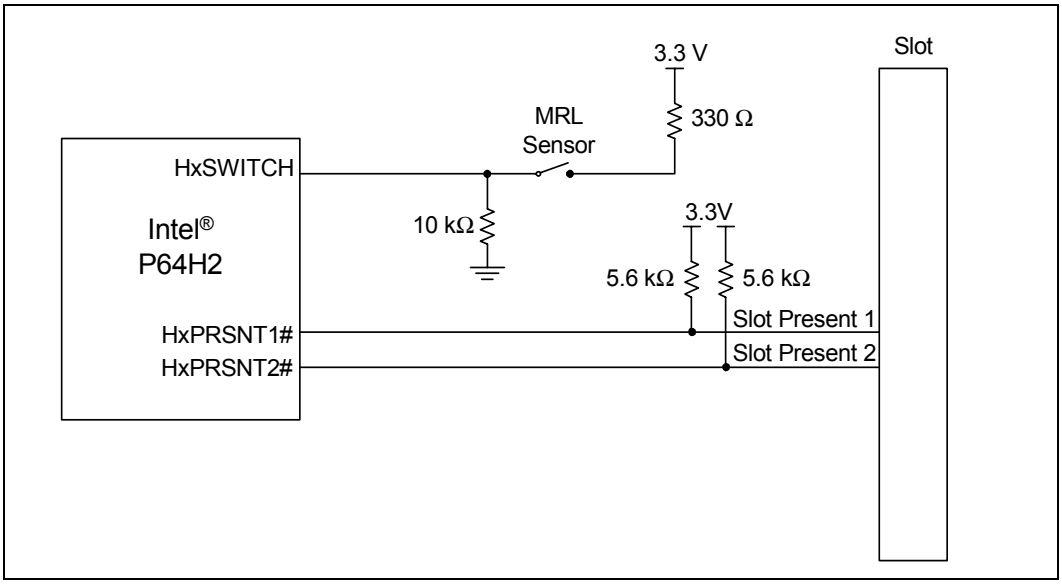
An “attention button” is a momentary-contact push-button. This button serves to invoke the Hot-Plug service so that an adapter can be added or removed without the use of a software interface. Support for the attention button is optional.

8.2.2.1 Manually-Operated Retention Latch Sensor

The HxSWITCH signal is monitored by the Hot-Plug controller to determine whether or not a slot should be powered. The MRL sensor, or slot switch, should be connected to the HxSWITCH pin such that it drives this pin low to indicate that the slot is closed and can be powered on. When the signal is driven high, it indicates that the slot should immediately be powered off. The MRL Sensor in represented schematically as a switch in Figure 8-12.

The Slot Present pins on each Hot-Plug slot are connected directly to the HxPRSNT2# and HxPRSNT1# pins on the P64H2.

Figure 8-12. Manually-Operated Retention Latch Sensor

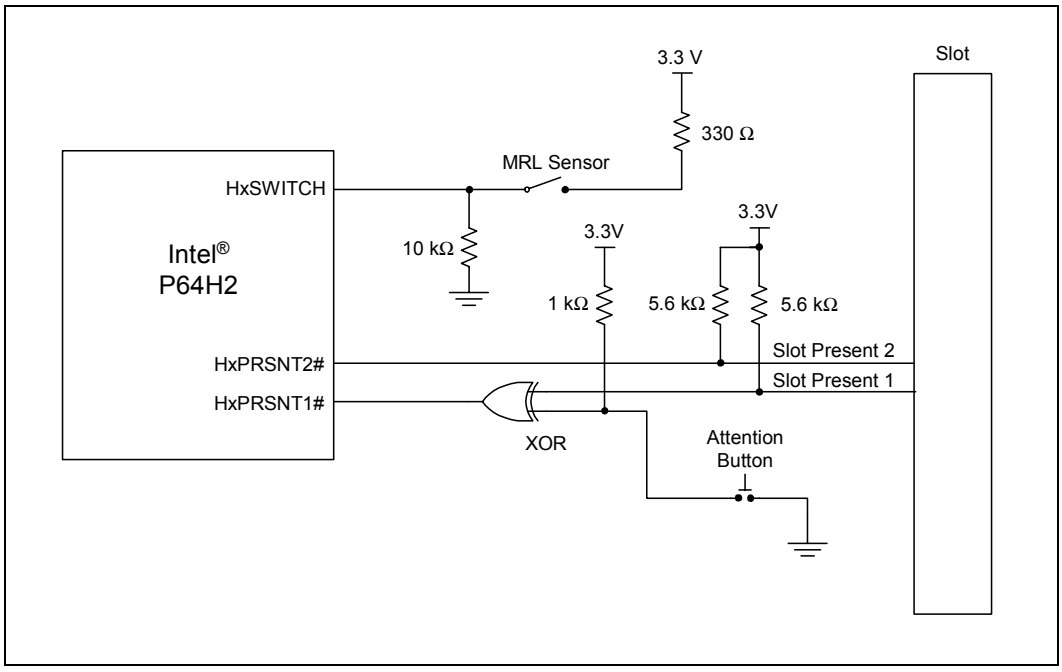


NOTE: The pin names shown in the Intel P64H2 block are hot-plug slot signal names. For single-slot parallel mode, refer to Table 8-17 for the corresponding P64H2 pin name. For dual-slot parallel mode, refer to Table 8-19 for the corresponding P64H2 pin name.

8.2.2.2 Optional Attention Button

The Attention Button state is observed on the slot-specific HxPRSNT1# pin. An exclusive-OR (XOR) gate is inserted between the Slot Present signal and the Hot-Plug controller as shown in Figure 8-13. A momentary contact button is connected to the other input of the XOR gate. When the button is in the released state, the Slot Present signal is unaffected. When the button is actively being pressed/asserted, the Slot Present signal is inverted, signaling the Hot-Plug controller to commence slot power up/down sequence.

Figure 8-13. Attention Button Implementation



NOTE: The pin names shown in the Intel P64H2 block are hot-plug slot signal names. For single-slot parallel mode, refer to Table 8-17 for the corresponding P64H2 pin name. For dual-slot parallel mode, refer to Table 8-19 for the corresponding P64H2 pin name.

8.2.3 LED Indicator Outputs

The PCI Hot-Plug Standard Usage Model assumes that the platform provides two indicators per slot. Indicators must be placed in close proximity to their associated slot so that the association between the indicators and the Hot-Plug slot is clear.

The LED output signals for all modes of P64H2 Hot-Plug controller operation are active high. In all cases, the green LED is the power indicator, and the amber LED is the attention indicator.

8.2.4 Hot Plug Interrupt Routing Requirements

The recommended method to support hot plug is to route the SCI interrupt output signal on the P64H2 (pin PAIRQ7) to an available GPIO pin on the ICH3. A System Controlled Interrupt (SCI) is a system interrupt used by hardware to notify the operating system of ACPI events. SCI is an active-low, shareable, level-triggered interrupt.

8.2.5 Disabling/Enabling an Intel® P64H2 Hot-Plug Controller

8.2.5.1 Hot-Plug Strapping Options

The HPx_SLOT [2:0] strapping pins are used to enable and disable the Hot-Plug controller. Table 8-15 lists the strapping options associated with these pins, and the modes of operation they enable.

Table 8-15. Hot-Plug Mode

HPx_SLOT 2:0]	Hot-Plug Mode	Notes
000	Hot-Plug Disabled	
001	1-Slot (Parallel Mode)	1
010	2-Slot (Parallel Mode)	2
011	3-Slot (Serial Mode)	3
100	4-Slot (Serial Mode)	3
101	5-Slot (Serial Mode)	3
110	6-Slot (Serial Mode)	3
111	Reserved	

NOTES:
1. Refer to Section 8.2.6 for single-slot parallel mode operation.
2. Refer to Section 8.2.7 for dual-slot parallel mode operation.
3. Refer to Section 8.2.7.9 for serial mode operation.

8.2.5.2 Hot-Plug Registers' Visibility

The Hot-Plug controller function is completely hidden when the controller is disabled by the slot strapping pins HPx_SLOT[2:0], and the registers are not available or accessible.

8.2.6 Single-Slot Parallel Mode

Single-slot parallel mode allows for only one card to be connected to the PCI/PCI-X Bus. This mode should be used only to implement a one-slot Hot-Plug solution because of the behavior of the PCI bus when in this mode. No serialization/deserialization logic is required for this mode of operation.

8.2.6.1 Required Additional Logic

Single-slot parallel mode requires a power switch to be used to turn the slot power on and off. Single-slot parallel mode does not require the use of a bus and clock switch. In this mode, all PCI signals are driven to ground whenever a PCI card is to be disconnected.

If the platform supports PME# or SMBus connections to the slot, isolation logic is required to disconnect these signals prior to inserting or removing a card. See the *PCI Hot-Plug Specification, Revision 1.1* for implementation details. The HxSWITCH signal can be used to control the isolation switches.

8.2.6.2 PCI Clock

In single-slot parallel mode, it is expected that PxPCLK0 is used.

8.2.6.3 Debounced Hot-Plug Switch Input

The switch inputs (PxIRQ15 in this case—see Table 8-17) to the Hot-Plug controller do not require any debouncing logic in this mode. This logic is contained within the P64H2. The POWERON value for this input is determined by BIOS. However, it is recommended that BIOS define a logic 0 to represent that the slot can be powered on.

8.2.6.4 Comparator Circuit for PCIXCAP1/PCIXCAP2 Pins

A comparator circuit is required for properly decoding the PCI/PCI-X capability of the slot. Refer to the *PCI Local Bus Specification, Revision 2.2* for this circuit. For more information on the reference circuit, refer to Section 8.2.7.9. The board designers could also use Table 8-16 as a reference.

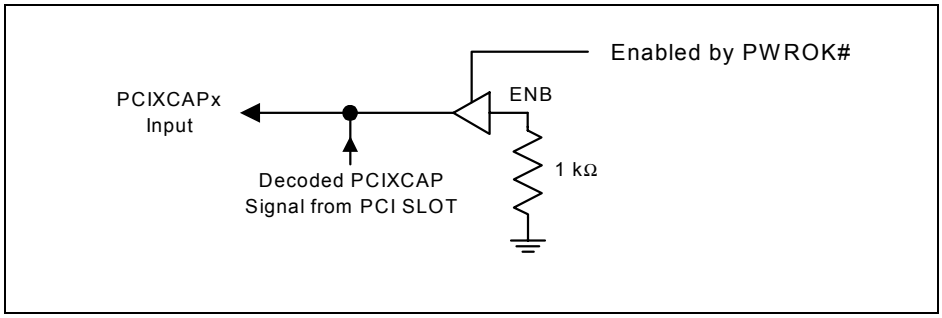
Table 8-16. Frequency Matrix

Frequency	M66EN	PCIXCAP1	PCIXCAP2	133EN
PCI 33	0	X	X	X
PCI 66	1	0	0	X
PCI-X 66	X	1	0	X
PCI-X 100	X	1	1	0
PCI-X 133	X	1	1	1

8.2.6.5 Tri-State Buffer or 2:1 Multiplexer for HPx_SLOT[2:0]

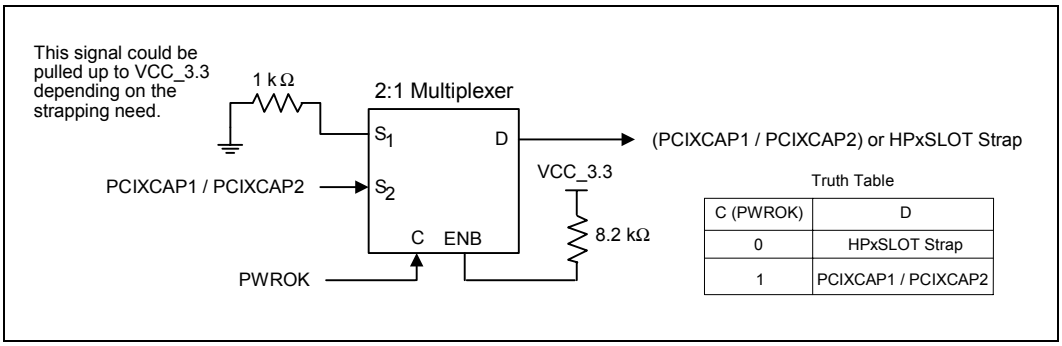
The HPx_SLOT [2:0] pins are pull-ups/pull-downs for determining the slot count and mode of operation for the P64H2 Hot-Plug controller. The strapping value on these pins is latched on the rising edge of PWROK. In single-slot parallel mode, these pins also function as the PCIXCAP1A, PCIXCAP2A, and PCIXCAP1B inputs to the controller. Logic must exist to preserve the slot count value when the system is in reset (PWROK signal is low).

Figure 8-14. Tri-State Buffer Circuit Example



It is also possible to accomplish this strapping requirement using a 2:1 multiplexer. The PWROK signal can be used to enable the tri-state buffer. The decision is left up to the individual designer on which method to use. See Figure 8-15 for an example of the optional multiplexer circuit.

Figure 8-15. Multiplexer Circuit Example



8.2.6.6 Hot-Plug Multiplexed Signals in Single-Slot Parallel Mode

The Hot-Plug signals that connect to the controller are shown in Table 8-17. In Table 8-17 the "Signal" column refers to the name of the slot pin when in single-slot mode. The "Bus A" and "Bus B" columns represent the corresponding P64H2 pins.

Table 8-17. Single-Slot Parallel Mode Hot-Plug Signal Table

Signal	Type	Multiplexed With				Note
		Bus A	Ball #	Bus B	Ball #	
HxSWITCHA	I	PAIRQ15	F4	PBIRQ15	F1	
HxFAULTA#	I	PAIRQ14	E4	PBIRQ14	E1	
HxPRSNT2A#	I	PAIRQ13	F5	PBIRQ13	D1	
HxPRSNT1A#	I	PAIRQ12	E5	PBIRQ12	C1	
HxM66ENA	I/O	PAIRQ11	D5	PBIRQ11	B1	
HxPCIXCAP1A	I	HPA_SLOT2	D20	HPB_SLOT2	D23	1
HxPCIXCAP2A	I	HPA_SLOT1	C20	HPB_SLOT1	C23	1
HxRESETA#	O	PAGNT5	E22	PBGNT5	G4	2
HxGNLEDA	O	HPA_SOC	A19	HPB_SOC	A24	2
HxAMLEDA	O	HPA_SOL	D19	HPB_SOL	C22	2
HxBUSENA#	O	HPA_SORR#	A18	HPB_SORR#	A22	2, 3
HxCLKENA#	O	HPA_SIL#	D24	HPB_SIL#	D24	2, 3
HxPWRENA	O	HPA_SOD	B19	HPB_SOD	C24	2

NOTES:
1. HPx_SLOT[N] are pull-ups/pull-downs. When in dual-slot parallel mode, the external logic that decodes the three-state value of PCIXCAP from the card must actively drive these signals to either logic 1 or logic 0 to overcome the value of the pull-up/pull-down, and must be tri-stated during reset and while the card is not connected to avoid damaging the slot count value.
2. The P64H2 must drive this signal to its corresponding state shown in Table 8-18 in case the system is set up for single-slot parallel mode so that LEDs are in the appropriate state (off), and the Q-switches remain disconnected. Note that the placement of the signals should be such that the value driven by the P64H2 in dual-slot parallel mode is the same value it would have driven if in serial mode.
3. In both parallel modes, the BUSEN# and CLKEN# signals become active low instead of active high as they are during serial mode.

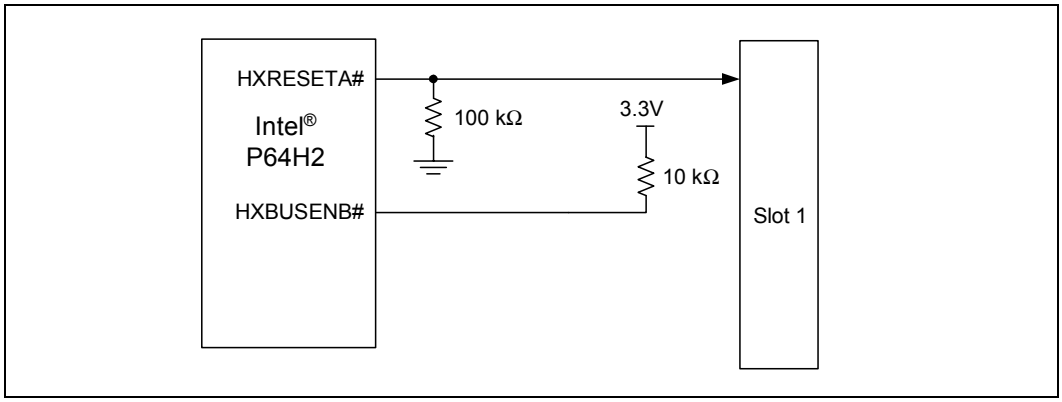
Table 8-18. Hot-Plug Controller Output Signal Reset Values

Signals	Reset Value
PxGNT[5:3]	011
HPx_SOC	0
HPx_SIC	0
HPx_SOL	0
HPx_SOLR	0
HPx_SOD	0
HPx_SORR#	1
HPx_SOR#	0
HPx_SIL#	1

8.2.6.7 SMBus Address Considerations

In single-slot parallel mode, the SMBus address strap pins listed in Table 8-14 are multiplexed with Hot-Plug control signal HxRESETA#. Therefore, it is recommended that the following technique be used for determining an SMBus address. Pull the PAGNT5 (RESETA#) signal to ground through a 100 kΩ ± 5% resistor. This will keep the reset signal active until the P64H2 is ready for it to become deasserted. Pull the PAGNT4 (HxBUSENB#) signal to 3.3 V through a 10 kΩ ± 5% resistor. The P64H2 will be able to drive this signal to ground when the signal must be asserted.

Figure 8-16. Single-Slot Parallel SMBus Circuit



NOTE: The pin names shown in the Intel P64H2 block are hot-plug slot signal names. For single-slot parallel mode, refer to Table 8-17 for the corresponding P64H2 pin name.

8.2.6.8 Pull-Ups/Pull-Downs in Single-Slot Parallel Mode

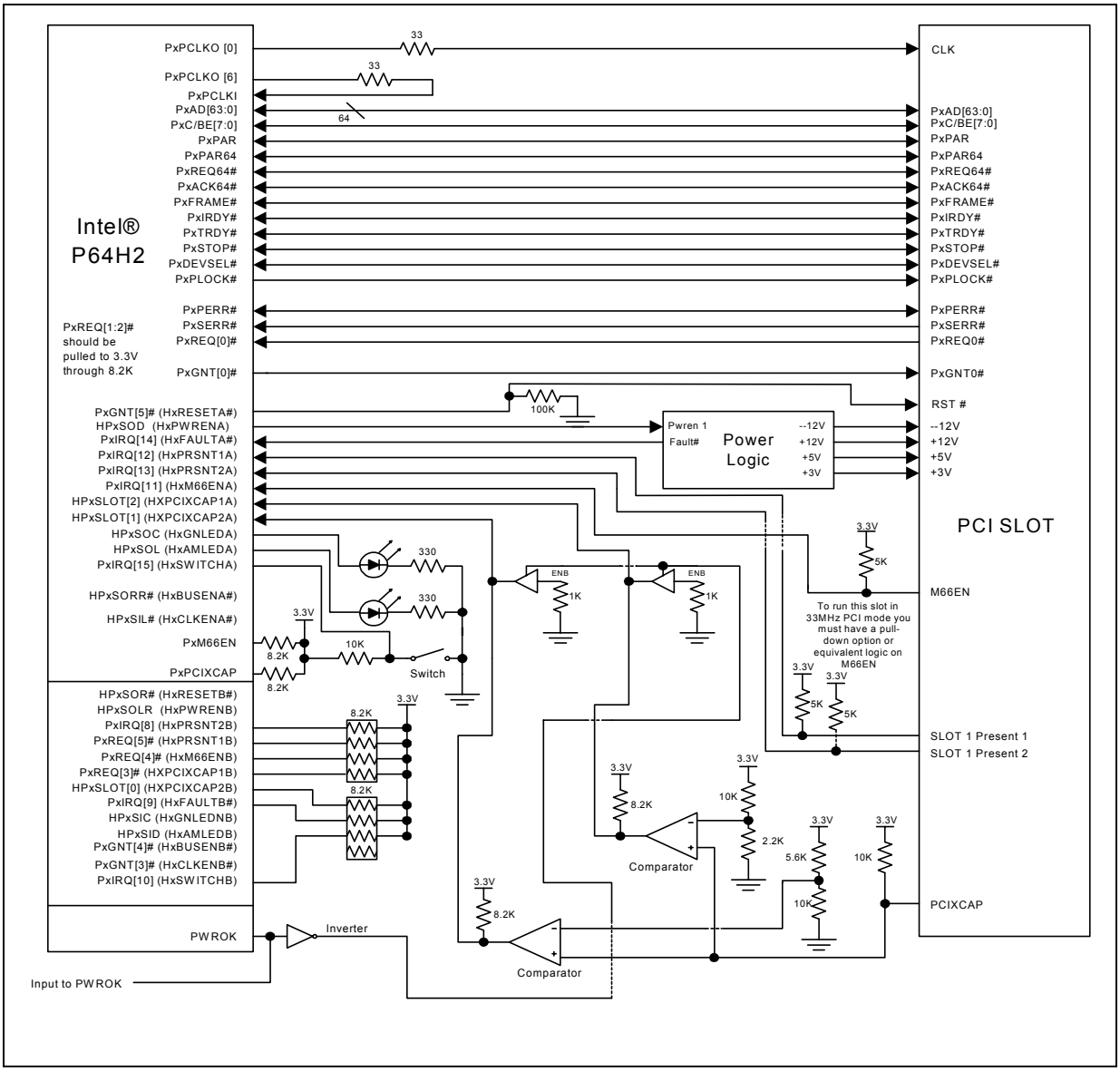
All PCI signals should follow the *PCI Local Bus Specification, Revision 2.2* pull-up requirements whether they are multiplexed or not. All unused input signals should be pulled to 3.3 V through an 8.2 kΩ ± 5% resistor to keep them from floating.

Table 8-17 defines which multiplexed signals are to be used with single-slot parallel mode. Note that whether in single- or dual-slot parallel mode, all signals from Table 8-17 are actually multiplexed even though only the signals listed in Table 8-18 are used. As a result, all unused input signals listed in Table 8-17 must be pulled to 3.3 V through an 8.2 kΩ ± 5% resistor to keep them from toggling.

8.2.6.9 Reference Schematic for Single-Slot Parallel Mode

Note that the following schematic is based on definition and simulation of the P64H2. This schematic has not been fully validated.

Figure 8-17. Reference Schematic for Single-Slot Parallel Mode



8.2.7 Dual-Slot Parallel Mode

Dual-slot parallel mode is used when it is desirable to have two slots that are Hot-Pluggable. No serialization/deserialization logic is required for this mode of operation.

8.2.7.1 Required Additional Logic

Dual-slot parallel mode requires a power switch to be used to turn the slot power on and off. Dual-slot parallel mode also requires the use of a bus and clock switch. Unlike single-slot parallel mode, the PCI signals are not driven to ground when a PCI card is to be disconnected. In addition, dual-slot parallel mode requires auto bus and clock disable logic to immediately disable the PCI bus and clock when the power fault signal (from the power switch) goes active.

If the platform supports PME# or SMBus connections to the slots, isolation logic is required to disconnect these signals before inserting or removing a card. See *PCI Hot-Plug Specification, Revision 1.1* for implementation details.

8.2.7.2 Debounced Hot-Plug Switch Input

The switch inputs (PAIRQ15 and PAIRQ10 in this case—see Table 8-19) to the Hot-Plug controller do not require debouncing logic in this mode. This logic is contained within the P64H2.

8.2.7.3 Comparator Circuit for PCIXCAP1/PCIXCAP2 Pins

A comparator circuit is required for properly decoding the PCI/PCI-X capability of the slot. Refer to the *PCI Local Bus Specification, Revision 2.2* for this circuit. An example of this circuit is also contained in the reference schematics. For a frequency reference matrix, see Table 8-16.

8.2.7.4 Tri-State Buffer or 2:1 Multiplexer for HPx_SLOT [2:0]

As with single-slot parallel mode, the HPx_SLOT [2:0] pins are pull-ups/pull downs for determining the slot count and mode of operation for the P64H2 Hot-Plug controller in dual-slot parallel mode. The strapping value on these pins is latched on the rising edge of PWROK. In dual-slot parallel mode these pins also function as the PCIXCAP1A, PCIXCAP2A, and PCIXCAP1B inputs to the controller. Logic must exist to preserve the slot count value when the system is in reset (PWROK signal is low). Connecting a tri-state buffer or a 2:1 multiplexer to these pins to pull the line high or low accordingly can do this. The PWROK signal can be used to enable the tri-state buffer to drive the line high or low or select the multiplexed signal. See Figure 8-14 for a tri-state buffer example circuit, and Figure 8-15 for a 2:1 multiplexer circuit example.

8.2.7.5 HPx_SID Output Signal

In dual-slot parallel mode, this signal is connected to the Amber LED slot status indicator. During a reset operation, this signal goes high which could flicker the LED on and confuse the user. To avoid having this LED turn on during a reset operation (PWROK logic zero), it is possible to use a buffer to electrically isolate this LED from the HPx_SID signal. The PWROK input signal to the P64H2 should be used to enable this buffer. See the dual-slot parallel mode reference schematic in Section 8.2.7.9 for an example of this circuit.

8.2.7.6 Pull-Ups/Pull-Downs in Dual-Slot Parallel Mode

All PCI signals should follow the *PCI Local Bus Specification, Revision 2.2* pull-up requirements whether they are multiplexed or not. Any unused input signals should be pulled to 3.3 V through an 8.2 kΩ ± 5% resistor to keep them from floating.

8.2.7.7 Hot-Plug Multiplexed Signals in Dual-Slot Parallel Mode

The Hot-Plug signals that connect to the controller are listed in Table 8-19. In Table 8-19 the "Signal" column refers to the name of the slot pin when in dual-slot mode. The "Bus A" and "Bus B" columns represent the corresponding P64H2 pins.

Table 8-19. Dual-Slot Parallel Mode Hot-Plug Signals Table

Signal	Type	Multiplexed Intel® P64H2 Pin				Note
		Bus A	Ball #	Bus B	Ball #	
HxSWITCHA	I	PAIRQ15	F4	PBIRQ15	F1	
HxFAULTA#	I	PAIRQ14	E4	PBIRQ14	E1	
HxPRSNT2A#	I	PAIRQ13	F5	PBIRQ13	D1	
HxPRSNT1A#	I	PAIRQ12	E5	PBIRQ12	C1	
HxM66ENA	I/O	PAIRQ11	D5	PBIRQ11	B1	
HxPCIXCAP1A	I	HPA_SLOT2	D20	HPB_SLOT2	D22	1
HxPCIXCAP2A	I	HPA_SLOT1	C20	HPB_SLOT1	C23	1
HxRESETA#	O	PAGNT5	E22	PBGNT5	G4	3
HxGNLEDA	O	HPA_SOC	A19	HPB_SOC	A24	3
HxAMLEDA	O	HPA_SOL	D19	HPB_SOL	C22	3
HxBUSENA#	O	HPA_SORR#	A18	HPB_SORR#	A22	3, 4
HxCLKENA#	O	HPA_SIL#	C21	HPB_SIL#	D24	3, 4
HxPWRENA	O	HPA_SOD	B19	HPB_SOD	C24	3
HxSWITCHB	I	PAIRQ10	C5	PBIRQ10	F2	
HxFAULTB#	I	PAIRQ9	B5	PBIRQ9	E2	
HxPRSNT2B#	I	PAIRQ8	A5	PBIRQ8	D2	
HxPRSNT1B#	I	PAREQ5	F24	PBREQ5	G3	
HxM66ENB	I/O	PAREQ4	F21	PBREQ4	H4	
HxPCIXCAP1B	I	PAREQ3	F19	PBREQ3	H2	
HxPCIXCAP2B	I	HPA_SLOT0	A20	HPB_SLOT0	B2	1
HxRESETB#	O	HPA_SOR#	B18	HPB_SOR#	A21	3
HxGNLEDB	O	HPA_SIC	A23	HPB_SIC	A23	3
HxAMLEDB	O	HPA_SID	B24	HPB_SID	B24	2
HxBUSENB#	O	PAGNT4	F23	PBGNT4	H5	3, 4
HxCLKENB#	O	PAGNT3	F20	PBGNT3	H3	3, 4
HxPWRENB	O	HPA_SOLR	C19	HPB_SOLR	B22	3

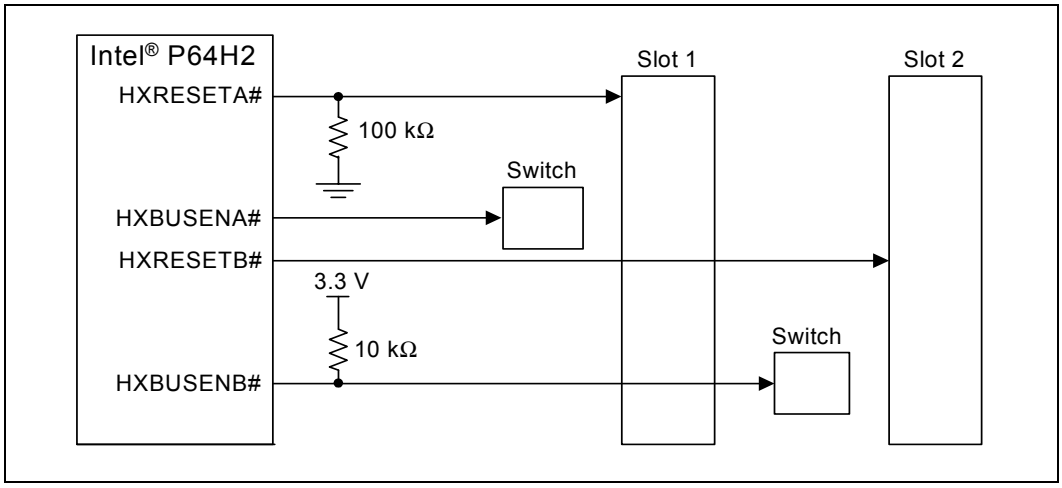
NOTES:
1. HPx_SLOT[N] are pull-ups/pull-downs. When in dual-slot parallel mode, the external logic that decodes the three-state value of PCIXCAP from the card must actively drive these signals to either logic 1 or logic 0 to overcome the value of the pull-up/pull-down, and must be tri-stated during reset and while the card is not connected to avoid damaging the slot count value.
2. HPx_SID must be pulled down on the system board when configuring the P64H2 for dual-slot parallel mode so that the LED for slot B on busses A and B remain off during reset.
3. The P64H2 must drive this signal to the corresponding state shown in Table 8-18 in case the system is set up for dual-slot parallel mode so that LEDs are in the appropriate state (off), and the Q-switches remain disconnected. Note that the placement of the signals should be such that the value driven by the P64H2 in dual-slot parallel mode is the same value it would have driven if in serial mode.
4. In both parallel modes, the BUSEN# and CLKEN# signals become active low instead of active high, as they are during serial mode.

8.2.7.8 SMBus Address Considerations

In dual-slot parallel mode, the SMBus address strap pins in Table 8-14 are multiplexed as Hot-Plug control signals HxRESETA# and HxBUSENB#. Therefore, it is recommended that the following technique be used for determining an SMBus address. Pull the PAGNT5 (RESETA#) signals to ground through a 100 kΩ ± 5% resistor. This keeps the reset signal active until the P64H2 is ready for it to become deasserted. Pull the PAGNT4 (BUSENB#) signals to 3.3 V through a 10 kΩ ± 5% resistor. The P64H2 will be able to drive this signal to ground when the signal must be asserted.

Keep in mind that this limits the range of addresses you can achieve. Using this technique, the address is fixed if operating in dual-slot parallel mode on both controllers.

Figure 8-18. Dual-Slot Parallel SMBus Circuit

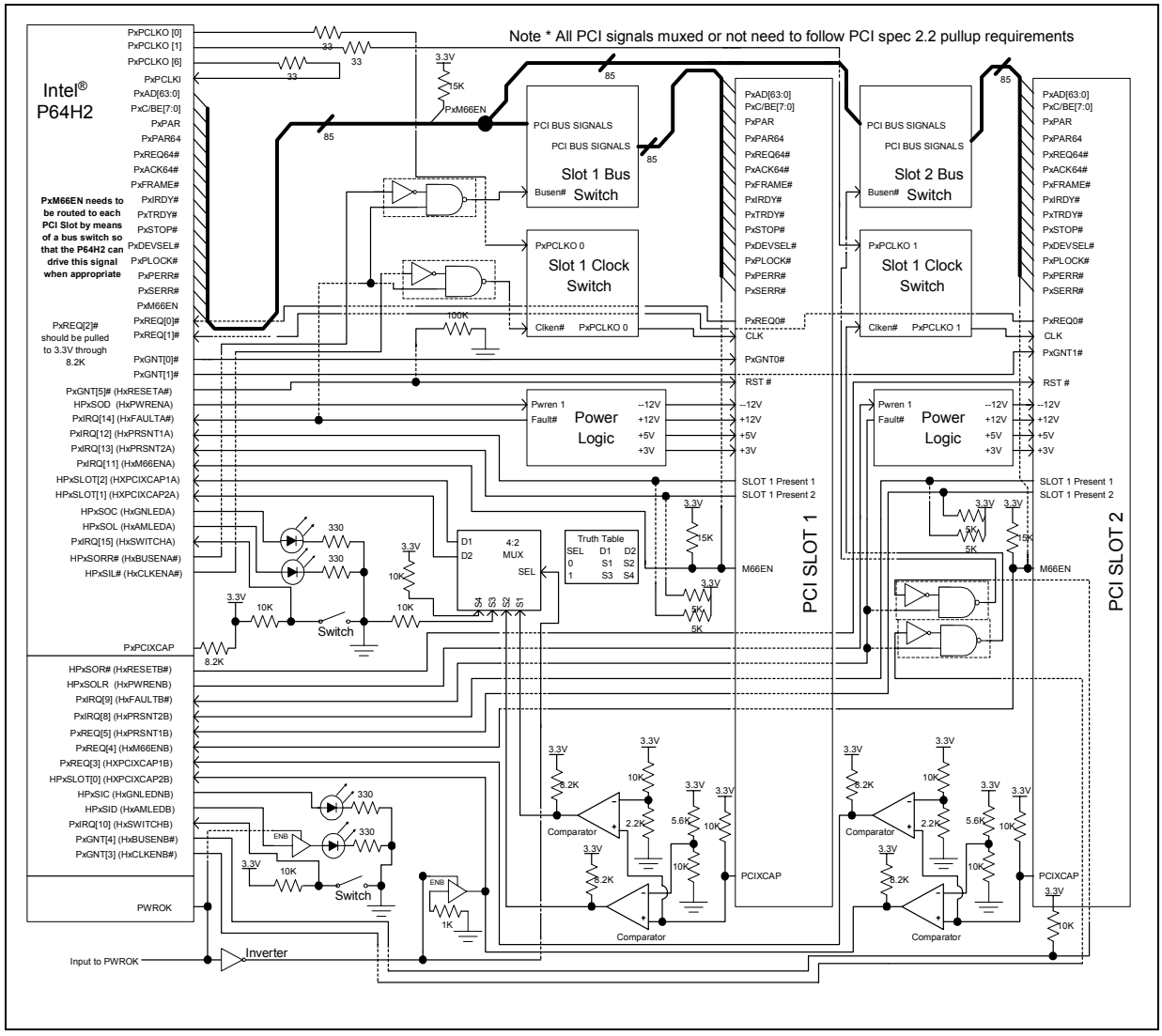


NOTE: The pin names shown in the Intel P64H2 block are slot pin names. For dual-slot parallel mode, refer to Table 8-19 for the corresponding P64H2 pin name.

8.2.7.9 Reference Schematic for Dual-Slot Parallel Mode

Note that the following schematic is based on definition and simulation of the P64H2. This schematic has not been fully validated.

Figure 8-19. Reference Schematic for Dual-Slot Parallel Mode



8.2.8 Three or More Slot Serial Mode

Serial mode allows for three to six slots to be Hot-Pluggable. This mode can also be used to enable slots that are Hot-Pluggable, and others that are not on the same PCI/PCI-X bus.

8.2.8.1 Hot-Plug and Non-Hot-Plug Combinations

To accomplish Hot-Plug and non-Hot-Plug combinations, put the non-Hot-Pluggable devices on their own Hot-Plug serialization logic (for M66EN and PCIXCAP), and scan them in for software to view. Do not electrically isolate those devices—allow software to see their capabilities to choose bus frequency properly.

8.2.8.2 Required Additional Logic

Serial mode requires a power switch to be used to turn the slot power on and off on all Hot-Pluggable slots. Serial mode also requires the use of a bus and clock switch. In addition, serial mode requires auto bus and clock disable logic to immediately disable the PCI bus and clock when the power fault signal (from the power switch) goes active.

If the platform supports PME# or SMBus connections to the slots, isolation logic is required to disconnect these signals before inserting or removing a card. See the *PCI Hot-Plug Specification, Revision 1.1* for implementation details.

8.2.8.3 Debounced Hot-Plug Switch Input

The switch inputs to the serialization/deserialization logic may require debouncing logic. This depends on the logic used for serialization, and is left up to the individual designer.

8.2.8.4 Comparator Circuit for PCIXCAP1/PCIXCAP2 Pins

A comparator circuit is required for properly decoding the PCI/PCI-X capability of the slot. Refer to the *PCI Local Bus Specification, Revision 2.2* for this circuit. An example of this circuit is also contained in the reference schematics.

8.2.8.5 HPx_SLOT [2:0]

The HPx_SLOT [2:0] pins are pull-ups/pull-downs that are used to determine the slot count and mode of operation for the P64H2 Hot-Plug controller. These pins should be strapped to the proper slot count value. See Table 8-15.

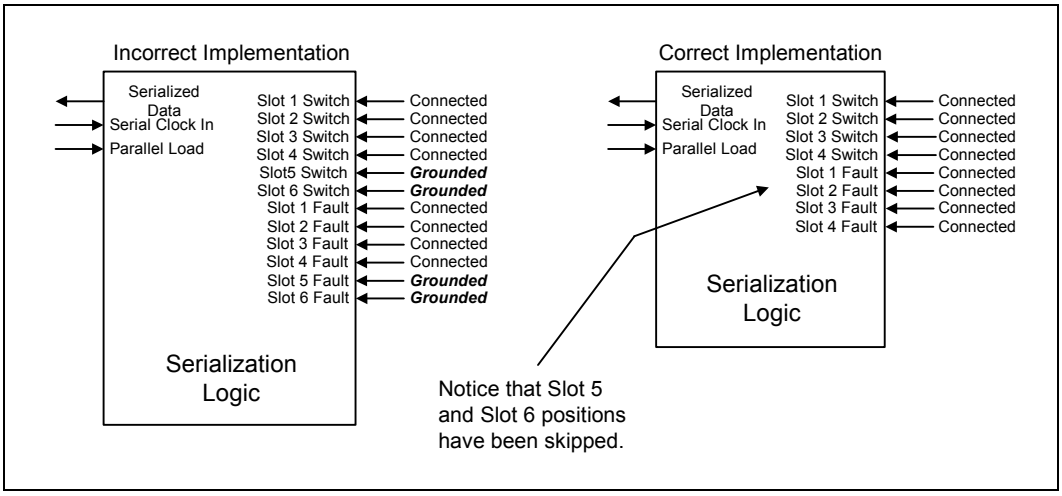
8.2.8.6 Stutter Logic for Implementing Fewer Than Six Slots

The serialized input/output data stream effectively stutters around the unused bit positions corresponding with the number of Hot-Plug slots determined by HPx_SLOT[2:0]. This reduces the amount of logic required to implement fewer than six slots. If HPx_SLOT[2:0] is strapped to enable four Hot-Pluggable slots, bit positions 4 and 5 would be skipped. Refer to Figure 8-20 for an example of this. Note that this concept also applies to the output data stream as well.

Table 8-20. Shift Register Input Data

Bit	Byte 0	Byte 1	Byte 2	Byte 3
0	Slot 1 switch (0 = closed)	Slot 1 fault# (0 = fault)	Slot 1 present bit 2	Slot 1 present bit 1
1	Slot 2 switch	Slot 2 fault#	Slot 2 present bit 2	Slot 2 present bit 1
2	Slot 3 switch	Slot 3 fault#	Slot 3 present bit 2	Slot 3 present bit 1
3	Slot 4 switch	Slot 4 fault#	Slot 4 present bit 2	Slot 4 present bit 1
4	Slot 5 switch	Slot 5 fault#	Slot 5 present bit 2	Slot 5 present bit 1
5	Slot 6 switch	Slot 6 fault#	Slot 6 present bit 2	Slot 6 present bit 1
6	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)
7	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)
Bit	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**
0	Slot 1 M66EN	Slot 1 PCIXCAP1	Slot 1 PCIXCAP2	User Defined
1	Slot 2 M66EN	Slot 2 PCIXCAP1	Slot 2 PCIXCAP2	User Defined
2	Slot 3 M66EN	Slot 3 PCIXCAP1	Slot 3 PCIXCAP2	User Defined
3	Slot 4 M66EN	Slot 4 PCIXCAP1	Slot 4 PCIXCAP2	User Defined
4	Slot 5 M66EN	Slot 5 PCIXCAP1	Slot 5 PCIXCAP2	User Defined
5	Slot 6 M66EN	Slot 6 PCIXCAP1	Slot 6 PCIXCAP2	User Defined
6	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)
7	Stutter (not used)	Stutter (not used)	Stutter (not used)	Stutter (not used)

Figure 8-20. Four Slot Stutter Logic Implementation Example



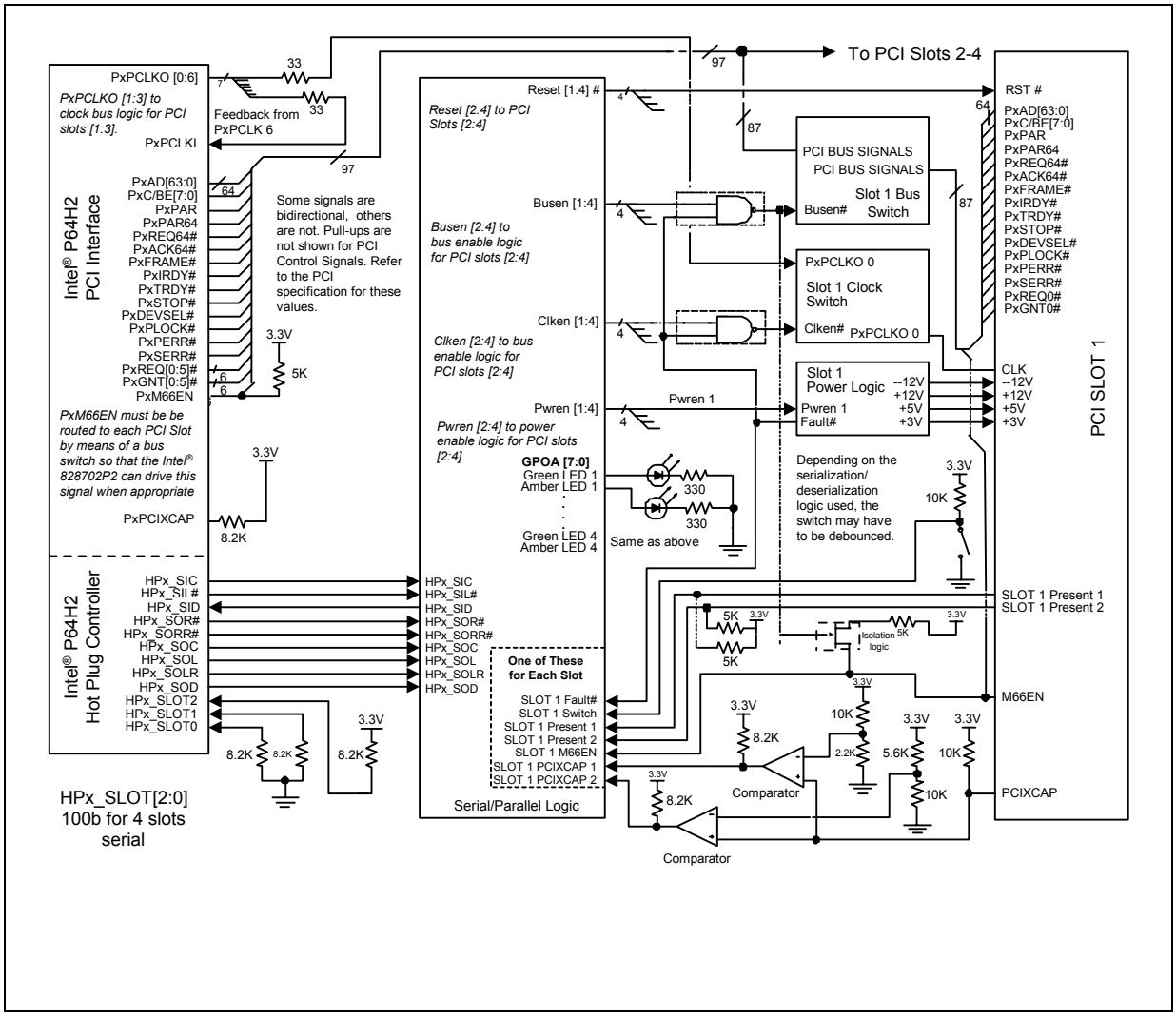
8.2.8.7 Pull-Ups/Pull-Downs in Three or More Slot Serial Mode

All PCI signals should follow the *PCI Local Bus Specification, Revision 2.2* pull-up requirements whether they are multiplexed or not. Any unused input signals should be pulled to 3.3 V through an 8.2 kΩ ± 5% resistor to keep them from floating.

8.2.8.8 Reference Schematic for Serial Mode

The following schematic is based on definition and simulation of the P64H2. This schematic has not been fully validated.

Figure 8-21. Reference Schematic for Serial Mode



8.2.9 Intel® P64H2 PCI Interface PCIXCAP and M66EN Pins

8.2.9.1 PCIXCAP Pin Requirements

During all modes of the P64H2 Hot-Plug controller operation, the P64H2 PCI/PCI-X interface pin PxPCIXCAP is not used. This pin should be tied to VCC3_3 through an 8.2 kΩ resistor to avoid having this line float.

The slot-specific HxPCIXCAP1 and HxPCIXCAP2 pins should be connected to their associated slot. See Section 8.2.6, Section 8.2.7, and Section 8.2.7.9 for more information on properly decoding PCI/PCI-X capability.

8.2.9.2 M66EN Pin Requirements

When operating in single-slot parallel mode, the P64H2 never drives PxM66EN. This pin should be tied to either VCC3_3 or ground through an 8.2 kΩ ± 5% resistor to avoid having this line float. M66EN on the slot must be connected to the associated HxM66EN pin with a pull-up/pull-down on the motherboard. If the slot is to be a 33 MHz slot, then M66EN must be pulled to ground on the motherboard. This will make the slot a 33 MHz PCI slot always. If the M66EN pin is pulled high, then the slot cannot be run at 33 MHz PCI. This means that after a card is powered up at 33 MHz (Hot-Plug default), software must reset the bus to at least 66 MHz PCI mode (or a PCI-X mode) before any software attempts accesses to the PCI card. Otherwise, the card could experience operational problems if it requires M66EN for setting up PLLs, etc.

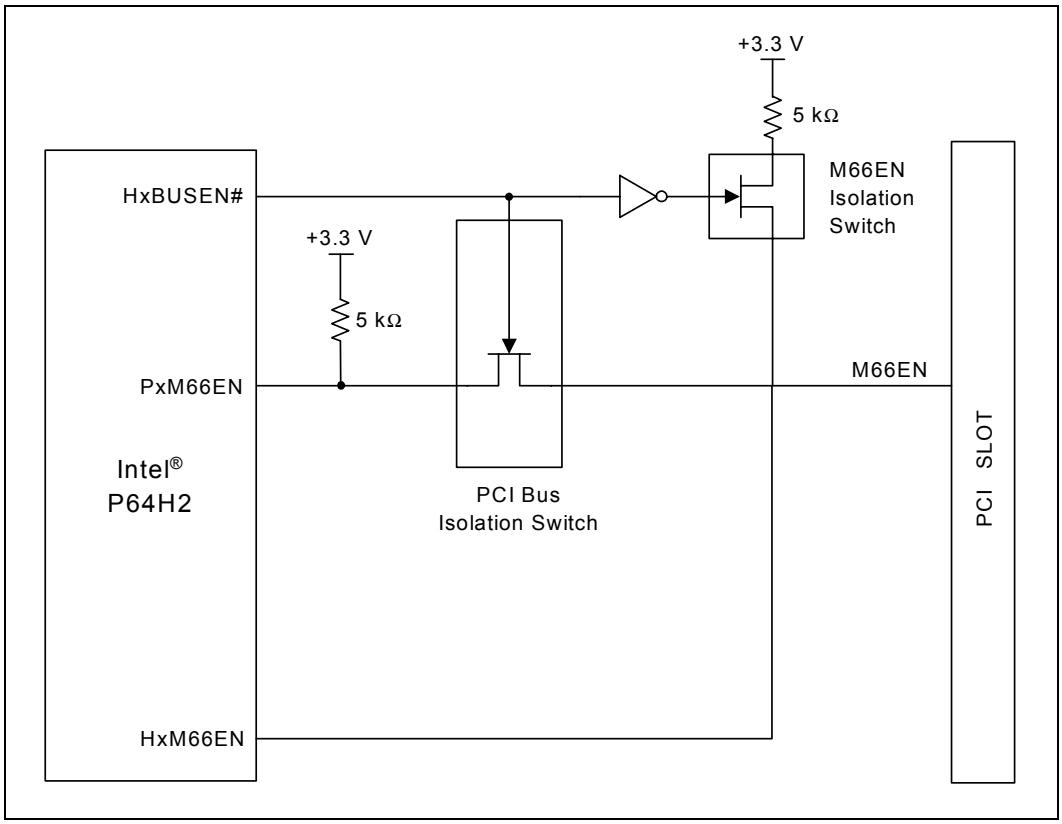
In Dual Slot Parallel and Serial Modes, the PxM66EN pin (on the P64H2 PCI/PCI-X interface) is a switched PCI bus signal that must be tied to all the slots through isolation logic. All cards must be able to see the value of PxM66EN being driven by the P64H2 when coming out of reset. The HxM66EN pins (on the P64H2 Hot-Plug Interface) should be connected to their associated slots.

The PxM66EN and HxM66EN pins each require 5 kΩ ± 5% pull-up resistors as specified in *PCI Local Bus Specification, Revision 2.2*. When the slot is connected to the bus, the P64H2 will be sinking through both resistors, which is a violation of the specification. The following sections describe two possible M66EN design solutions.

M66EN Isolation Switch Solution

One possible solution to the issue described in the previous paragraphs is to place a single 5 kΩ ± 5% pull-up on the P64H2 side of the isolation logic and a 5 kΩ ± 5% pull-up on the slot side after the isolation logic, but with its own isolation switch, which uses an inverted version of the bus enable control signal. This way, when the isolation logic has the bus disconnected, the slot side will be pulled up with a 5 kΩ ± 5% resistor. When the isolation logic has the bus connected, the slot side resistor will be isolated, and the M66EN line will be pulled up by the 5 kΩ ± 5% pull-up on the P64H2 side of the isolation logic. Using this method, the P64H2 would only be sinking through a single 5 kΩ resistor at any time and would always be meeting the *PCI Local Bus Specification, Revision 2.2* on the M66EN pull-up (*PCI Local Bus Specification, Revision 2.2, Section 7.7.7*). See Figure 8-22.

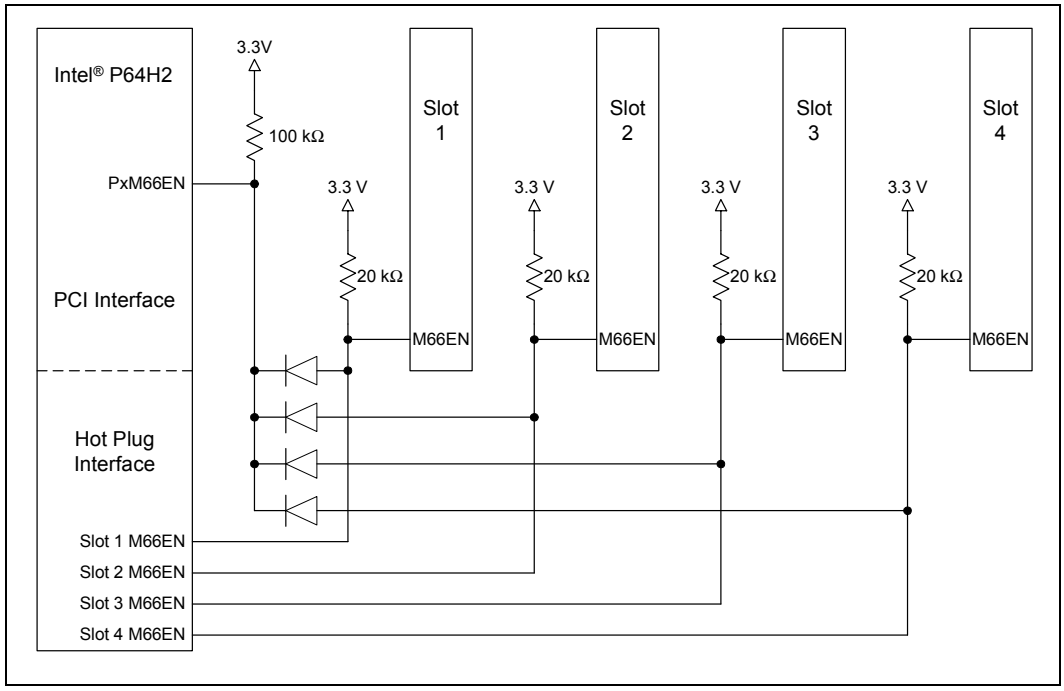
Figure 8-22. M66EN Isolation Switch Solution



M66EN Diode Solution

Another possible solution to the issue described in the previous paragraphs is to use diodes to isolate the individual slots from one another while still allowing the P64H2 to drive the M66EN signals to ground. The P64H2 PCI interface PxM66EN signal should be pulled to 3.3 V through a 100 kΩ ± 5% resistor. This signal would then be connected to the individual slots through a reverse biased diode (one diode per slot). The PCI slots should also be pulled up individually to 3.3 V through a resistor of value such that the equivalent of all the resistances on the M66EN bus is approximately 5 kΩ (the PCI recommended value). This circuit allows the P64H2 to pull the slots' M66EN to ground during initial power-up. During normal operation, each of the slots' M66EN signals will be isolated from one another allowing for polling of the Hot-Plug HxM66EN input for slot capability. Figure 8-23 shows the diode solution implemented in serial mode, where "Slot x M66EN" is a serialized input to the Hot-Plug controller.

Figure 8-23. M66EN Diode Solution



NOTE: All PCI signals, multiplexed or not, must follow PCI Specification 2.2 pull-up requirements.

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I/O Controller Hub 3 (Intel® ICH3-S) 9

9.1 IDE Interface

This section contains guidelines for connecting and routing the ICH3-S IDE interface. The ICH3-S has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH3-S has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5-mil traces on 7-mil spaces, and must be less than 8 inches long (from ICH3-S to IDE connector). Additionally, maximum length difference between the longest and shortest trace lengths of a channel is 0.5 inch.

9.1.1 Cabling

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
- **Capacitance:** The capacitance of each IDE cable must be less than 35 pF.
- **Placement:** A maximum of 6 inches is allowed between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (no more than 6 inches away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- **ICH3-S Placement:** The ICH3-S must be placed equal to or less than 8 inches from the ATA connector(s).

9.1.2 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH3-S IDE controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5. The ICH3-S must determine the type of cable that is present to configure itself for the fastest possible transfer mode the hardware can support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than 2 (Ultra ATA/33). This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, and so on. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the *Small Form Factor Specification SFF-8049*. This specification can be obtained from the Small Form Factor Committee.

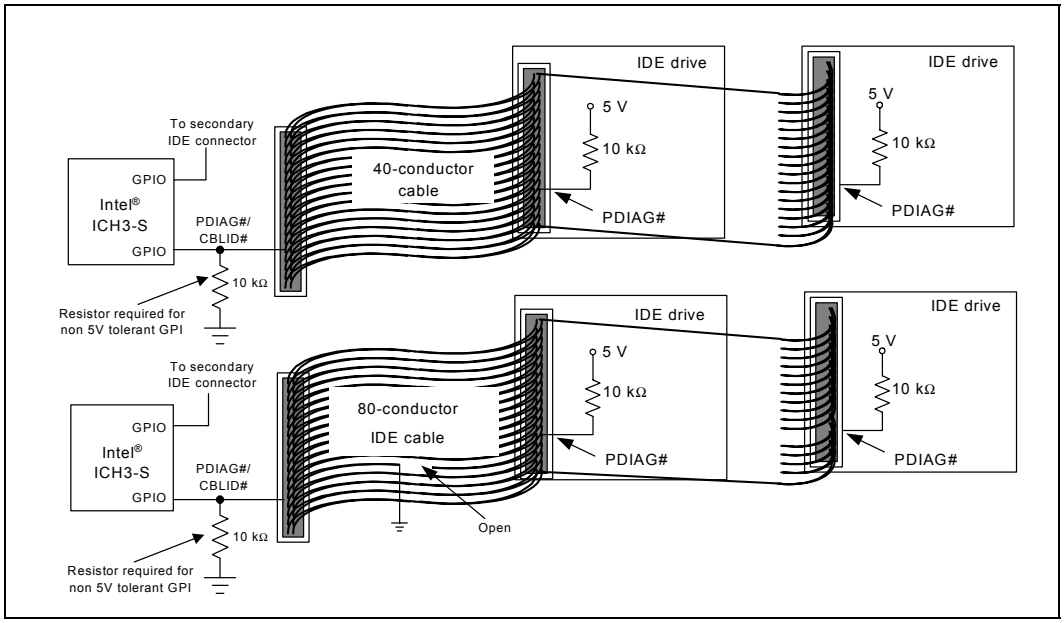
To determine if Ultra DMA modes greater than 2 (Ultra ATA/33) can be enabled, the ICH3-S requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination Host-Side/Device-Side detection mechanism.

9.1.2.1 Combination Host-Side/Device-Side Cable Detection

Host-side detection (described in the *ATA/ATAPI-4 Standard*, Section 5.2.11) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 9-1. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. Not all of the GPI and GPIO pins on the ICH3-S are 5 V tolerant. A 10 kΩ ± 5% pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present. The pull-down resistor also allows for the use of a non-5 V tolerant GPIO.

Figure 9-1. Combination Host-Side/Device-Side IDE Cable Detection



This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high, then a 40-conductor cable is present in the system and Ultra DMA modes greater than Mode 2 (Ultra ATA/33) must not be enabled.

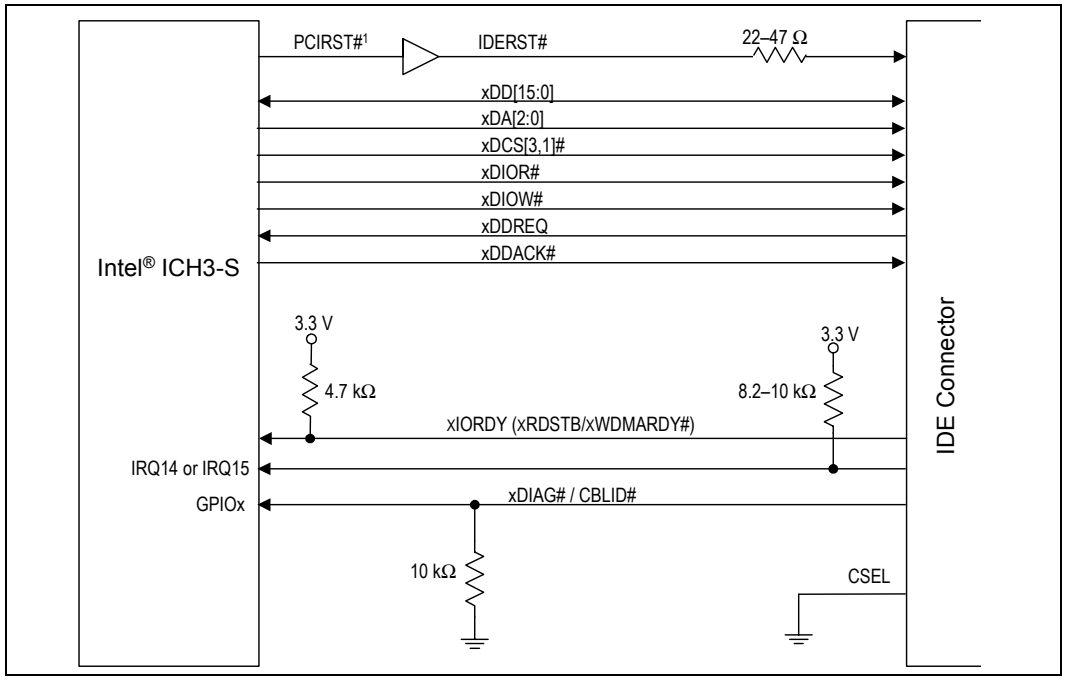
If PDIAG#/CBLID# is detected low, then an 80-conductor cable may be in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is 1, an 80-conductor cable is present. If this bit is 0, a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present and notify the user of the problem.

9.1.3 IDE Connector Requirements

The requirements for the primary and secondary IDE connector are shown in Figure 9-2.

- A 22 Ω to 47 Ω series resistor is required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3_3.
- A 4.7 kΩ ± 5% pull-up resistor to VCC3_3 is required on PIORDY.
- Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10 kΩ ± 5% resistor to ground on the PDIAG#/CBLID# signal is required on the connector. This change is to prevent the GPIOx pin from floating if a device is not present on the IDE interface.

Figure 9-2. Connection Requirements for IDE Connector

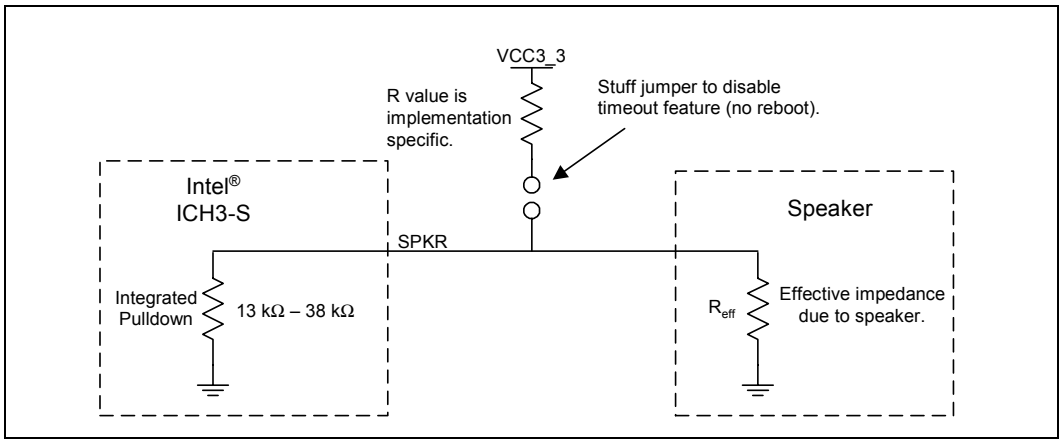


NOTES:
1. Because of ringing, PCIRST# must be buffered.
2. 'x' indicates Primary or Secondary channel.

9.2 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH3-S sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable TCO timer reboot, a jumper can be populated to pull the signal line high (see Figure 9-3). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (REFF), and the ICH3-S's integrated pull-down resistor will be read as logic high (0.5 VCC3_3 to VCC3_3 + 0.5 V).

Figure 9-3. Example Speaker Circuit

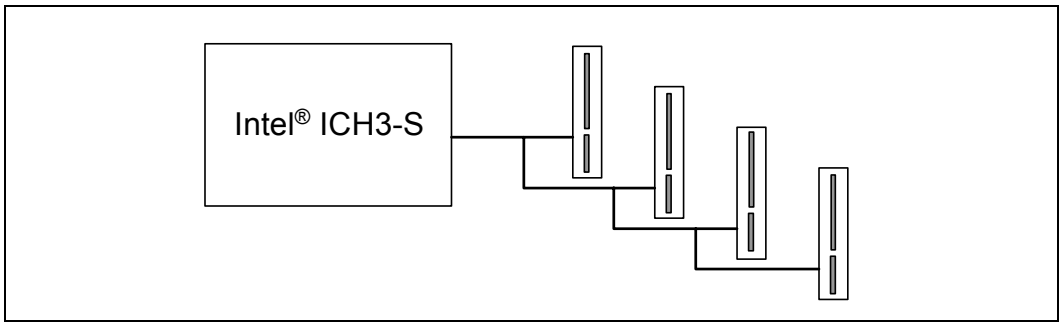


9.3 PCI

The ICH3-S provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2.* The implementation is optimized for high-performance data streaming when the ICH3-S is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2.*

The ICH3-S supports six PCI Bus masters (excluding the ICH3-S), by providing six REQ# / GNT# pairs. In addition, the ICH3-S supports two PC/PCI REQ# / GNT# pairs, one of which is multiplexed with a PCI REQ# / GNT# pair.

Figure 9-4. PCI Bus Layout Example



9.4 USB

The ICH3-S contains three UHCI Host controllers. Each UHCI controller includes a root hub with two separate USB ports, for a total of six USB ports. This section provides guidelines for routing USB.

9.4.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines help minimize signal quality and EMI problems. USB validation efforts have focused on a ground referenced design.

1. Place the ICH3-S and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
2. USB signals should be ground referenced (on layers 3 and 6).
3. Route USB signals using a minimum of vias and corners. This reduces reflections and impedance changes.
4. When it becomes necessary to turn 90 degrees, use two 45-degree turns or an arc instead of a single 90 degree turn. This reduces reflections on the signal by minimizing impedance discontinuities.
5. Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on USB signals should be avoided because stubs have an effect on signal quality. If stubs are necessary, none should be greater than 200 mils.
7. Route all traces over continuous ground planes with no interruptions. Avoid crossing over anti-etch if possible; this increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces.
8. Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, and can be very difficult to filter out.
9. Keep traces at least 50 mils away from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires, and helps prevent free radiation of the signal from the edge of the PCB.

9.4.2 USB Routing Parameters

Use the following separation guidelines.

- Recommended trace width and separation is 5-mil trace width with 6-mil spacing (90 Ω differential impedance).
- Maintain parallelism between USB differential signals, with the trace spacing needed to achieve 90 Ω differential impedance.
- Use at a minimum 20-mil spacing between USB signal pair and other traces on the PCB. This helps to prevent crosstalk. If possible, keep clock and PCI traces at least 50 mils from the USB differential pairs.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk.
- Trace length match USB signal pair traces. The maximum trace length mismatch between USB signal pair should be no greater than 150 mils.

9.4.3 EMI Considerations

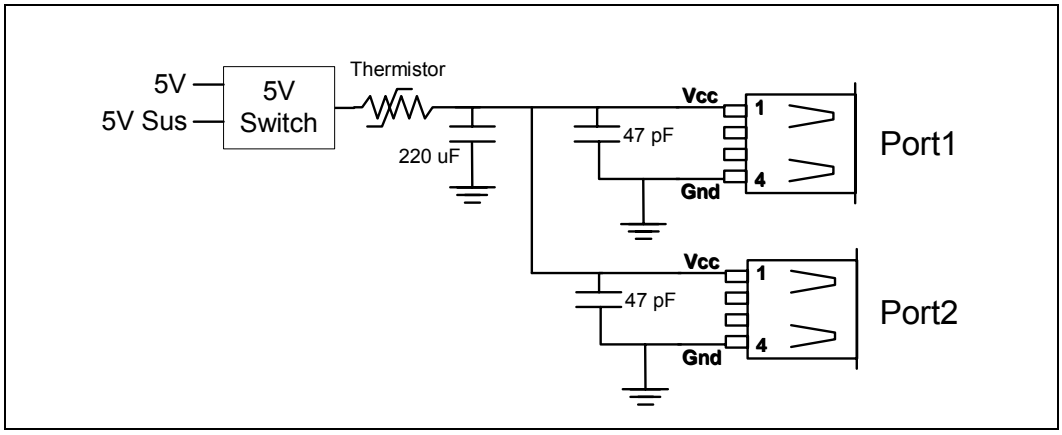
An optional 47 pF capacitor may be placed as close to the USB connector as possible on the USB data lines. This capacitor can be used for improved signal quality (rise/fall time), and to help minimize EMI radiation.

Note: Any EMI or ESD solution should be placed as close to the port as possible. For example, if using a front-panel daughtercard, the EMI/ESD solution should be placed on the daughtercard.

9.4.4 USB Power Line Layout Topologies

The following is a suggested topology for power distribution of VBUS to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop), and dynamic detach flyback protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port, and the power-carrying traces should be as wide as possible, preferably a plane.

Figure 9-5. Suggested USB Downstream Power Connection



9.5 Intel® ICH3-S SMBus/SMLink Interface

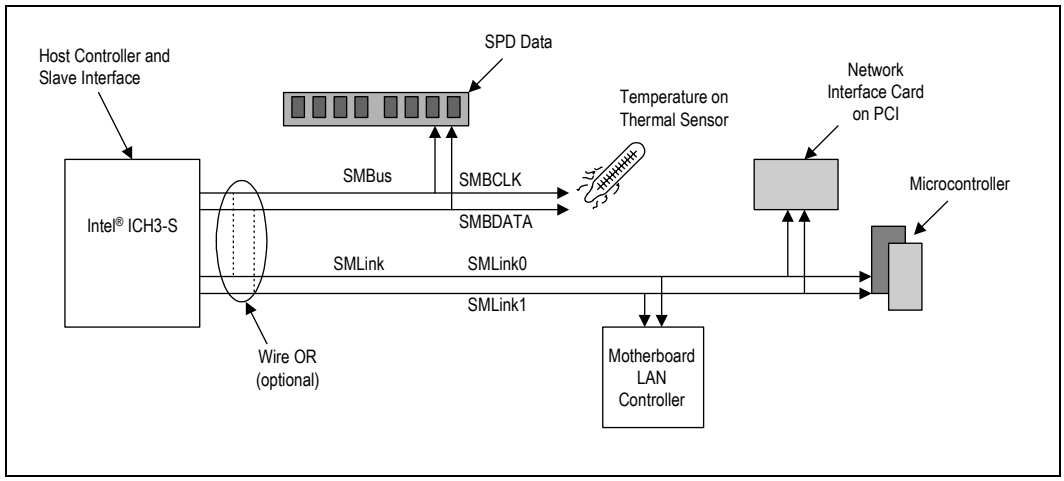
The SMBus interface on the ICH3-S uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus host controller. The SMBus host controller resides inside the ICH3-S. If the SMBus is used only for the SPD EEPROMs (one on each DIMM), both signals should be pulled up with a 4.7 kΩ ± 5% resistor to VCC3_3.

The ICH3-S incorporates an SMLink interface supporting Alert on LAN*, Alert on LAN2*, and a slave functionality. This interface uses two signals, SMLINK[1:0]. SMLINK0 corresponds to an SMBus clock signal, and SMLINK1 corresponds to an SMBus data signal. These signals are part of the SMBus Slave Interface.

For Alert on LAN* functionality, the ICH3-S transmits heartbeat and event messages over the interface. When using the 82562EM Platform LAN Connect Component, the ICH3-S's integrated LAN controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2-enabled LAN controller (i.e., Intel® 82550) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH3-S SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus host controller and the SMBus Slave Interface obey the SMBus 2.0 protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (e.g., 82550) to access targets on the SMBus as well as the ICH3-S Slave interface. Additionally, the ICH3-S supports slave functionality, including the Host Notify protocol, on the SMLink pins. This is done by connecting SMLink0 to SMBCLK and SMLink1 to SMBDATA.

Figure 9-6. Intel® ICH3-S SMBus / SMLink Interface



Note: Intel does not support external access of the ICH3-S's Integrated LAN controller via the SMLink interface. In addition, Intel does not support access of the ICH3-S's SMBus Slave Interface by the ICH3-S's SMBus host controller. Refer to the *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

9.5.1 SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Regardless of the architecture used, there are some general design considerations.

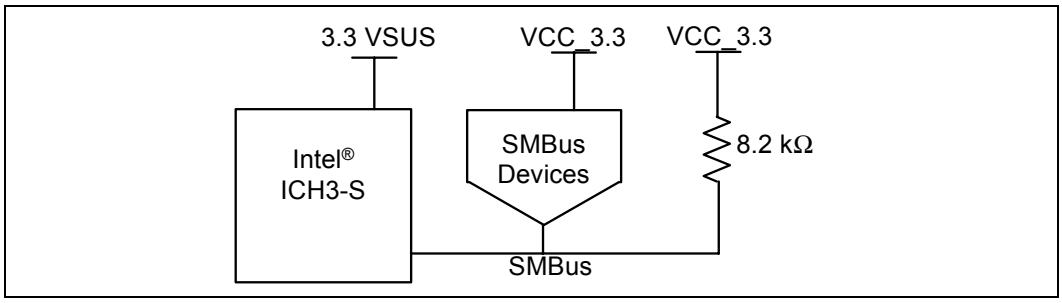
- Device class (High/Low power). Most designs use primarily High Power Devices.
- Amount of VCC_SUSPEND current available (i.e., minimizing load of VCC_SUSPEND).
- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor can not be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and time specification.
- The maximum bus capacitance that a physical segment can reach is 400 pF.
- The ICH3-S does not run SMBus cycles while in S5.
- SMBus devices that can operate in S5 must be powered by the VCC_SUSPEND supply.
- If SMBus is connected to PCI it must be connected to all PCI slots.
- It is recommended that I^2C devices be powered by the 1.8 V supply. During an SMBus transaction in which the device is sending information to the ICH3-S, the device may not release the SMBus if the ICH3-S receives an asynchronous reset. 1.8 V is used to allow BIOS to reset the device if necessary. SMBus 2.0-compliant devices have a timeout capability which makes them insusceptible to this I^2C issue, allowing flexibility in choosing a voltage supply.

9.5.2 The Unified VCC_CORE Architecture

Designing an SMBus using the ICH3-S is based on the power supply source for the SMBus microcontrollers. For the platform, all devices are powered by VCC3_3; therefore, the preferred design choice is the unified VCC3_3 architecture.

In the unified VCC_CORE architecture, all SMBus devices are powered by the VCC3_3 supply. This architecture in Figure 9-7 allows none of the devices to operate in S5, minimizing the load on 3.3 V SUSPEND.

Figure 9-7. Unified VCC3_3 Architecture

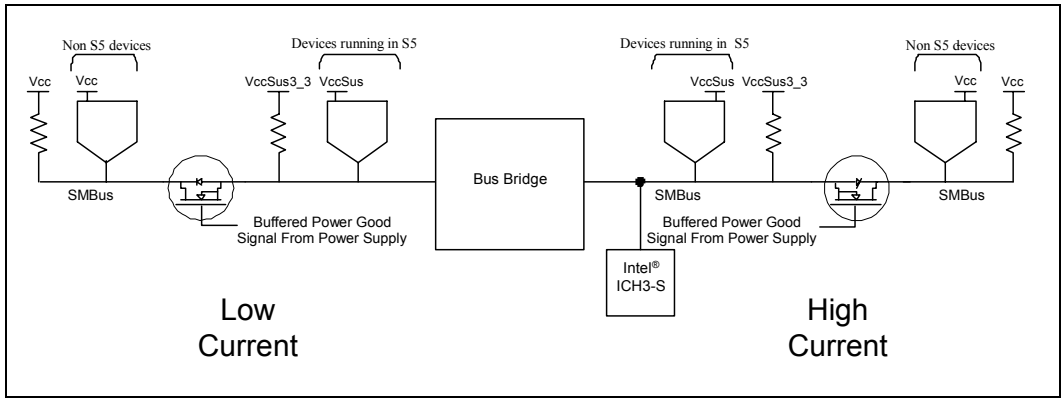


NOTES:
1. The SMBus device must be back-drive safe while its supply (VCC3_3) is off and 3.3 V SUS is still powered.
2. In suspended modes where VCC3_3 is OFF and 3.3 V SUS is on, the VCC3_3 node will be very near ground. In this case, the input leakage of the ICH3-S will be approximately 10 µA.

9.5.3 High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate while in S5. VCC_SUSPEND leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of a “FET” to isolate the devices powered by the core and suspend supplies. See Figure 9-8.

Figure 9-8. High Power/Low Power Mixed VCC_SUSPEND/ VCC_CORE Architecture



Added Considerations for Mixed Architecture:

- The bus switch must be powered by VCC_SUSPEND.
- Devices that are powered by the VCC_SUSPEND well must not drive into other devices that are powered off. This is accomplished with the “bus switch”.
- The bus bridge can be a device like the Phillips PCA9515.

9.5.4 Calculating The Physical Segment Pull-Up Resistor

The following tables are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, then a bus bridge device like the Phillips PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 9-1. Bus Capacitance Reference Chart

Device	No. of Devices/ Trace Length	Capacitance Includes	Cap (pF)
Intel® ICH3-S	1	Pin Capacitance	12
CK408	1	Pin Capacitance	10
DIMMS	2	Pin Capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per DIMM and 2 pF connector capacitance per DIMM	28
	3		42
PCI Slots	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector	86
	3		129
	4		172
	5		215
	6		258
SMBus Trace Length in inches	≥ 24”	2 pF per inch of trace length	48
	≥ 36”		72
	≥ 48”		96

Table 9-2. Bus Capacitance/Pull-Up Resistor Relationship

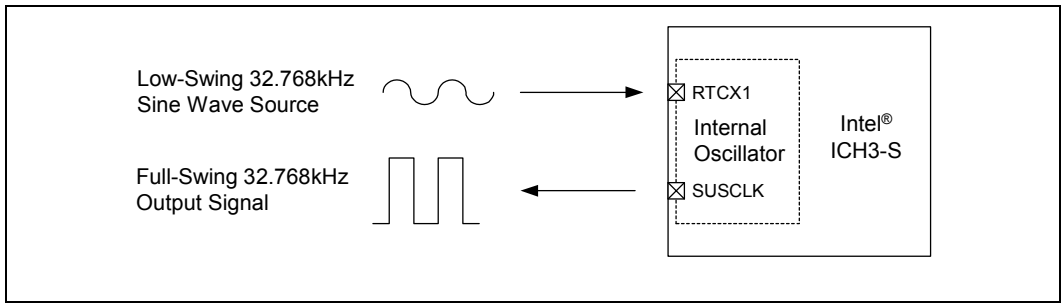
Physical Bus Segment Capacitance	Pull-Up Range (For Vcc = 3.3 V)
0 to 100 pF	8.2 kΩ to 1.2 kΩ
100 to 200 pF	4.7 kΩ to 1.2 kΩ
200 to 300 pF	3.3 kΩ to 1.2 kΩ
300 to 400 pF	2.2 kΩ to 1.2 kΩ

9.6 Real Time Clock (RTC)

The ICH3-S contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time, and storing system data in its RAM when the system is powered down.

The ICH3-S uses a crystal circuit that generates a low-swing 32 kHz input sine wave. The RTCX1 input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH3-S, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use illustrated in Figure 9-9. This ICH-S output ball is called SUSCLK.

Figure 9-9. RTCX1 and SUSCLK Relationship

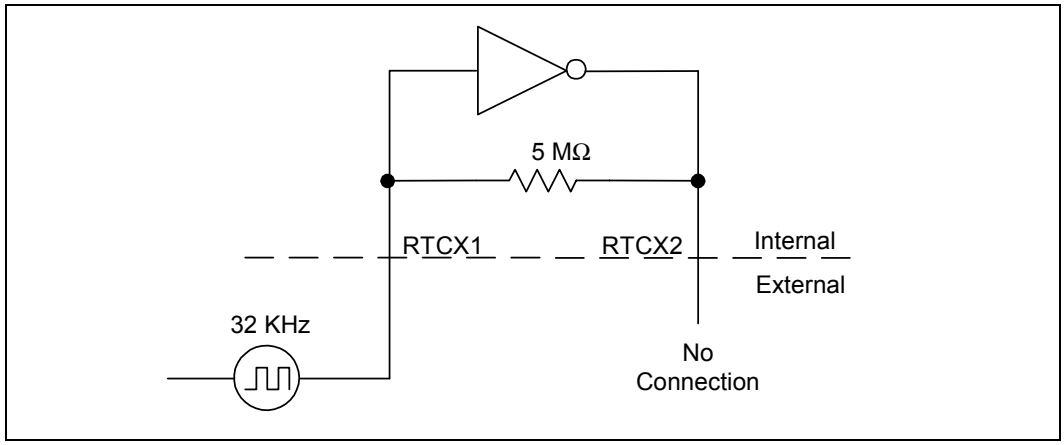


For further information on the RTC, consult Intel application note *AP-728 Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions* (http://developer.intel.com/design/chipsets/applnots/292276.htm).

This section presents the recommended hookup for the RTC circuit for the ICH3-S.

Even if the ICH3-S internal RTC is not used, it is still necessary to supply clock inputs to RTCX1 and RTCX2 pins of the ICH3-S because other signals are gated with that clock in suspend modes. However, in this case the frequency (32.768 kHz) of the clock inputs is not critical. A lower-cost crystal can be used, or a single clock input can be driven into the RTCX1 pin with the RTCX2 pin left as no connect; Figure 9-10 illustrates this. This is not a validated configuration with ICH3-S.

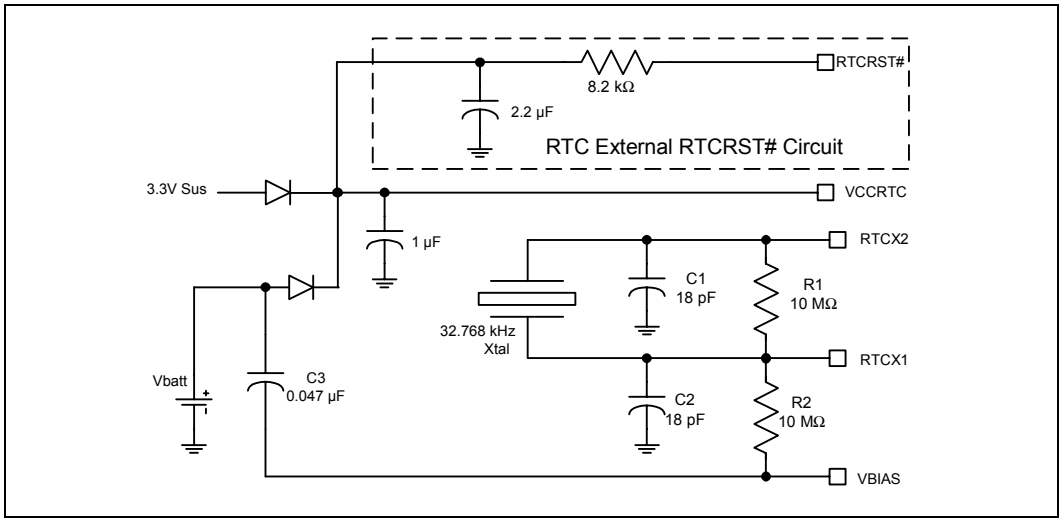
Figure 9-10. RTC Connection When Not Using Internal RTC



9.6.1 RTC External Circuit

The ICH3-S RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 9-11 documents the external circuitry that comprises the oscillator of the ICH3-S RTC.

Figure 9-11. Example RTC External Circuitry



NOTES:
1. The exact capacitor values must be based on the crystal maker recommendation. (Typical values for C1 and C2 are 18 pF for a crystal load of 12 pF.)
2. VCCRTC: Power for RTC Well
3. RTCX2: Feedback for the external crystal
4. RTCX1: Input to the internal oscillator
5. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.

9.6.2 RTC External RTCRST# Circuit

The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10 ms – 20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1 and remains set until software clears it. Because of this, when the system boots, the BIOS knows that the RTC battery has been removed. Figure 9-11 is an example of RTCRST# circuitry that is used in conjunction with the external diode circuit.

9.6.3 External Capacitors

To maintain the RTC accuracy, the external capacitor C3 must be 0.047 µF, and capacitor values C1 and C2 should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

Cload = [(C1 + Cin1 + Ctrace1)*(C2 + Cin2 + Ctrace2)]/[(C1 + Cin1 + Ctrace1 + C2 + Cin2 + Ctrace2)] + Cparasitic

Where:

Cload = Crystal's load capacitance. This value can be obtained from crystal's specification.

Cin1, Cin2 = input capacitances at RTCX1, RTCX2 balls of the ICH3-S. These values can be obtained in the *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet*.

Ctrace1, Ctrace2 = Trace length capacitances measured from crystal terminals to the RTCX1 and RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces, and the length of the traces. Typical value is approximately:

Ctrace = trace length * 2 pF / inch (dependent upon board characteristics)

Cparasitic = Crystal's parasitic capacitance. This capacitance is created by the existence of two electrode plates, and the dielectric constant of the crystal blank inside the crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C1 and C2 can be selected such that C1 = C2. Using the equation of Cload above, the value of C1 and C2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C2 can be chosen such that C2 > C1. Then C1 can be trimmed to obtain 32.768 kHz.

In certain conditions, both C1 and C2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C1 and C2 values are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example illustrates the use of the practical values C1 and C2 in the case that theoretical values can not guarantee the accuracy of the RTC in a low temperature condition.

Example

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH3-S, the calculated values of C1 = C2 are 10 pF at room temperature (25 °C) to yield a 32.768 kHz oscillation.

At 0 °C, the frequency stability of the crystal gives -23 ppm (assumed that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C1 and C2 are chosen to be 6.8 pF instead of 10 pF. This will make the RTC oscillate at a higher frequency at room temperature (+23 ppm), but this configuration of C1 and C2 makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C1 and C2 is the **practical value.**

Note that the temperature dependency of crystal frequency is a parabolic relationship (ppm / degree squared). The effect of the changing crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature).

9.6.4 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires high accurate oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. ICH3-S requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Route the RTC circuit short to simplify the trace length measurement and increase accuracy when calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
- Reduce trace signal coupling by avoiding routing of adjacent PCI signals close to RTCX1, RTCX2, and VBIAS.
- A ground guard plane is highly recommended.

9.6.5 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH3-S is not powered by the system.

Example batteries are: Duracell 2032, 2025, or 2016 (or equivalent), which can give many years of operation.

Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable), and the average current required is 3 µA, the battery life will be at least:

170,000 µAh / 3 µA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. The battery voltage of the RTC must be greater than 2 V at all times to ensure the accuracy of the RTC clock.

Connect the battery to the ICH3-S via an isolation diode circuit. The diode circuit allows the ICH3-S RTC-well to be powered by the battery when the system power is not available, and by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 9-11 is an example of a diode circuit. As noted, a standby power supply should be used in a server system to provide continuous power to the RTC when available to significantly increase the RTC battery life.

9.6.6 VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 9-11); therefore, it is a self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 filters out most of the AC signals that exist on this ball. However, the noise on this ball should be kept to a minimum to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX1 and RTCX2 signals (using Op-Amp). See application note *AP-728, Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions,* for further details on measuring techniques.

Note: VBIAS is also very sensitive to environmental conditions.

9.6.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30% and 70%.

If the SUSCLK duty cycle is beyond the 30%–70% range, there is a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using a normal probe (50 Ω input impedance probe), and it is an appropriate signal to check the RTC frequency to determine the accuracy of the ICH3-S RTC clock.

9.6.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in the G3 state. RTCRST#, when configured as shown in Figure 9-11, meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

9.7 Internal LAN Layout Guidelines

The ICH3-S provides various options for integrated LAN capability. The platform supports several components depending on the target market. The guidelines use the term 82562ET to refer to both the Intel® 82562ET, and the Intel® 82562EM. The 82562EM is specified in those cases where a difference exists.

Platform LAN Connect Component	Connection	Features
Intel® 82562EM	Advanced 10/100 Ethernet	Alert on LAN* & Ethernet 10/100 Connection
Intel® 82562ET	10/100 Ethernet	Ethernet 10/100 Connection

Design guidelines are provided for each required interface and connection. Refer to Figure 9-12 and Table 9-3 for the corresponding section of the design guide.

Figure 9-12. Platform LAN Connect

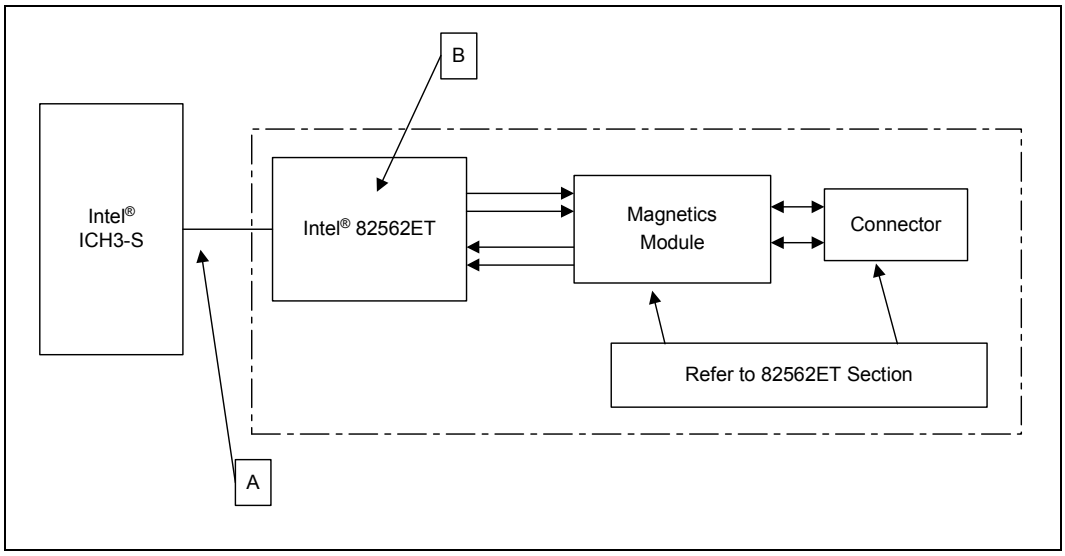


Table 9-3. LAN Design Guide Section Reference

Layout Section	Figure 9-12 Reference	Design Guide Section
Intel® ICH3-S – LAN Connect Interface	A	Section 9.7.1, Intel® ICH3-S – LCI (LAN Connect Interface) Guidelines
General Routing Guidelines	B	Section 9.7.2, General LAN Routing Guidelines and Consideration
Intel® 82562ET / 82562EM	B	Section 9.7.3, Intel® 82562ET/EM Guidelines

9.7.1 LCI (LAN Connect Interface) Guidelines

This section contains guidelines on how to implement a PLC (Platform LAN Connect) device on a system motherboard using LCI. It should not be treated as a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH3-S to LAN component interface. The following signal lines are used on this interface:

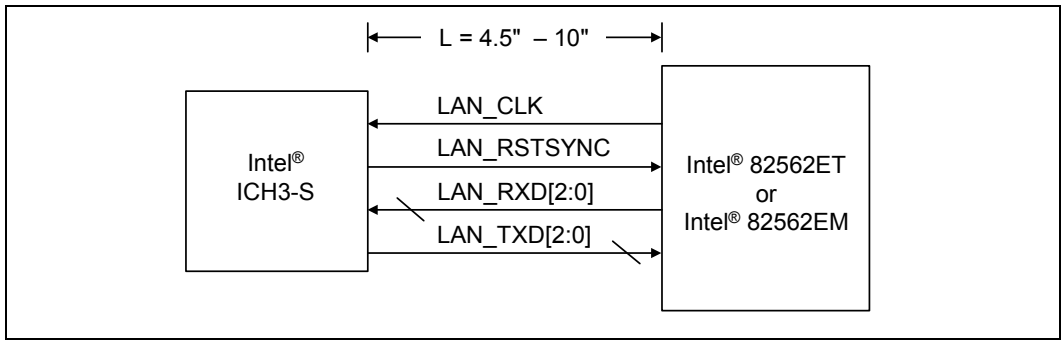
- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports 82562ET/82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD0, and LAN_TXD0 are shared by all components.

9.7.1.1 Bus Topology

The LAN Connect Interface must be configured in direct point-to-point connection between the ICH3-S and the LAN component topology. (Refer to Figure 9-13.)

Figure 9-13. Point-to-Point Interconnect Guideline



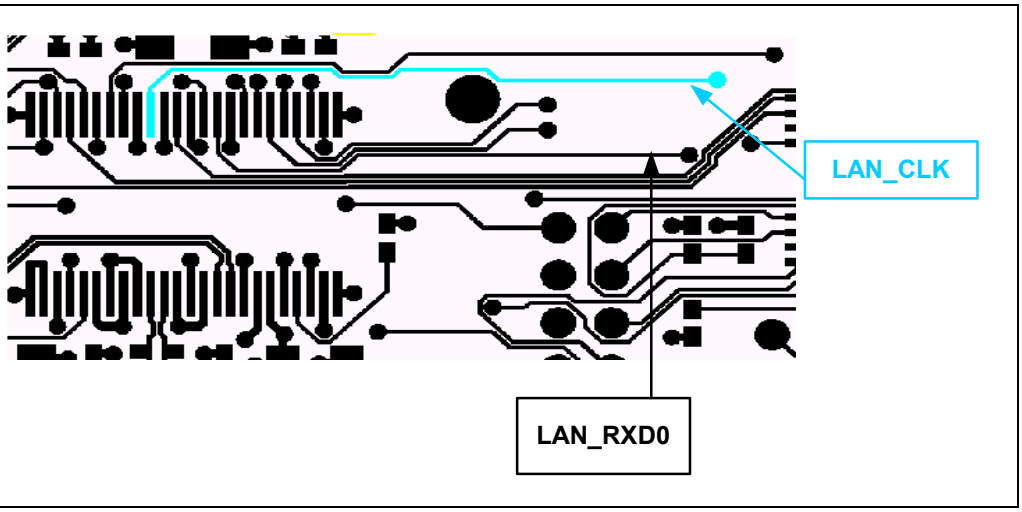
9.7.1.2 LCI Routing Parameters

Route the LCI signals carefully on the motherboard to meet the timing and signal quality requirements of this interface specification. The board designer should simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk.

Table 9-4. LCI Routing Parameter Summary

Parameter	Requirements
Trace Impedance (Z_0)	60 Ω ± 15% due to signal integrity requirements.
Trace Spacing	Minimum of 100 mils from non-LCI signals
Termination	33 Ω series resistor can be installed at the driver side of the interface.
Length Tuning	On the motherboard, the length of each data trace should be either equal in length to the LAN_CLK trace, or up to 0.5 inch shorter than the LAN_CLK trace. LAN_CLK should always be the longest motherboard trace in each group.

Figure 9-14. LAN_CLK Routing Example



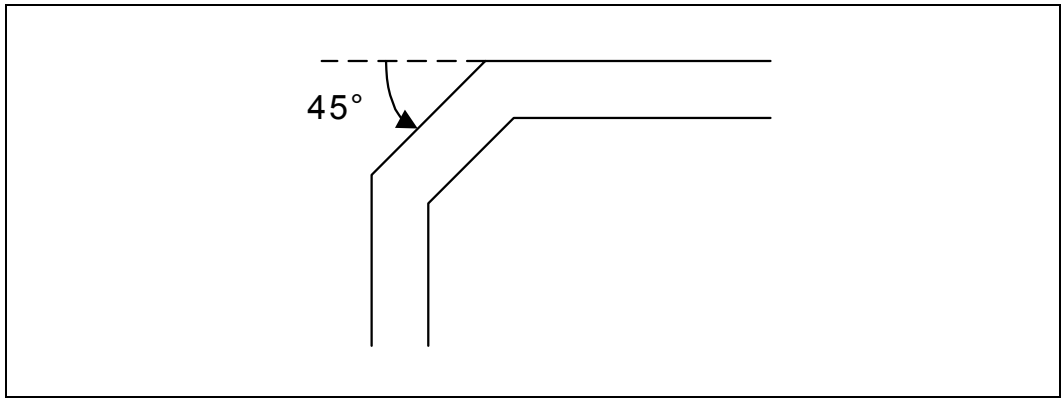
9.7.2 General LAN Routing Guidelines and Considerations

9.7.2.1 General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance:

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. (Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER [Bit Error Rate].)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces parallel to the differential traces, or closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90 degree bend is required, it is recommended to use two 45-degree bends instead. Refer to Figure 9-15.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 9-15. Routing a 90-Degree Bend



9.7.2.2 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length, and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge-to-edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also, for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than 1 inch to the connector/magnetic edge of the board.

9.7.2.3 Signal Isolation

Follow these rules for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Over the length of the trace run, each differential pair should be at least 0.3 inch away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

9.7.2.4 Power and Ground Connections

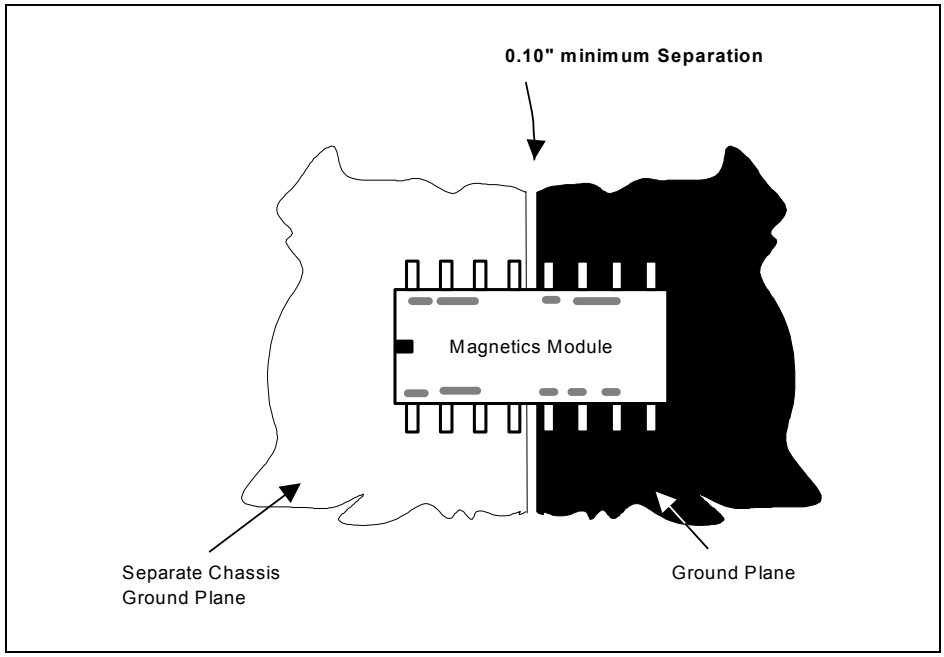
Follow these rules for power and ground connections:

- All VCC balls should be connected to the same power supply.
- All VSS balls should be connected to the same ground plane.
- Four to six decoupling capacitors, including two 4.7 µF capacitors, are recommended.
- Place decoupling as close as possible to power balls.

9.7.2.5 General Power and Ground Plane Consideration

To properly implement the common mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 9-16. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return. These will significantly reduce EMI radiation.

The following are guidelines that help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions (don't route over a plane split). If vacant areas exist on a ground or power plane, avoid routing signals over the vacant area. Routing over a vacant area will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics, which can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

9.7.2.6 Board Design

The following recommendations are based on a ground referenced design.

- Top Layer Routing

  Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity, and removes any impedance inconsistencies due to layer changes.

- Ground Plane

  A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended. It is also recommended to minimize the digital noise injected into the 82562 common ground plane. Suggestions include optimizing decoupling on neighboring noisy digital components, isolating the 82562 digital ground using a ground cutout, etc.

- Power Plane

  Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply plane's VDD_A. Analog power may be a metal fill "island," separated and RC filtered from digital power.

- Signal Layer Routing

  The digital high-speed signals, which include all of the LAN interconnect interface signals, must be routed on an internal signal layer away from the analog signals.

9.7.2.7 Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs:

- Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
- Lack of symmetry between the two traces within a differential pair. (For each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
- Excessive distance between the PLC and the magnetics or between the magnetics and the RJ45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are long. The magnetics should be as close to the connector as possible (≤ 1 inch).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC), and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inch from the differential traces.
- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inch or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ45/11, and the PLC.

- Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
- Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or application note.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The application notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
- Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5 Ω–20 Ω. A 10 Ω–15 Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.
- Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a capacitor is put in either of these locations. If a capacitor is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These capacitors are not necessary, unless there is some overshoot in 100 Mbps mode.

Note: It is important to keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.

Note: Close should be considered to be less than 0.03 inch between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

9.7.3 Intel® 82562ET/EM Guidelines

For documentation on LAN, refer to Section 1.2. For correct LAN performance, designers must follow the general guidelines outlined in Section 9.7.2. Additional guidelines for implementing an 82562ET or 82562EM platform LAN connect component are provided in the following sections.

9.7.3.1 Guidelines for Intel® 82562ET/EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which can cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation affects the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.7.3.2 Crystals and Oscillators

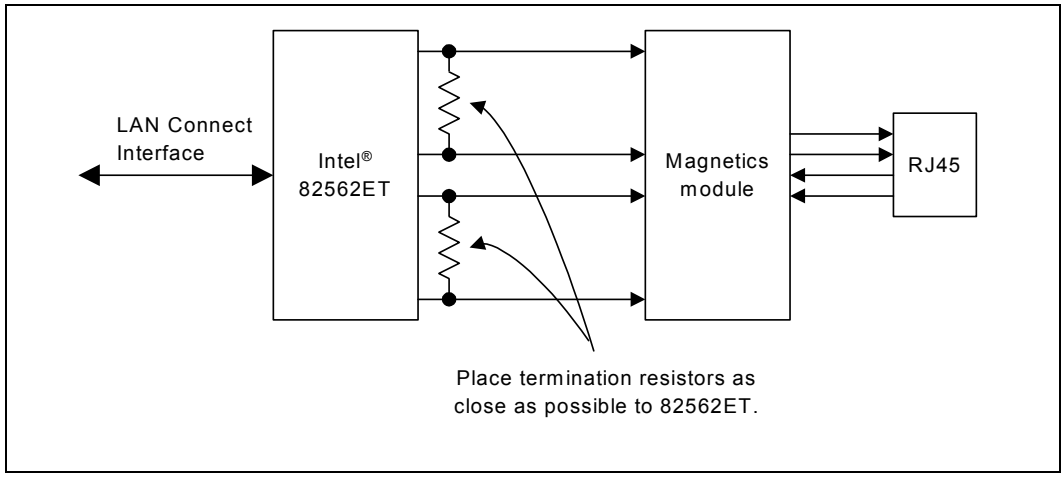
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility of radiation from the crystal case, and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562ET or 82562EM, keeping the trace length as short as possible. Do not route any noisy signals in this area.

9.7.3.3 Intel® 82562ET/EM Termination Resistors

The 100 Ω ± 1% resistor used to terminate the differential transmit pairs (TDP/TDN), and the 121 Ω ± 1% resistor used to terminate the differential receive pairs (RDP/RDN) should be placed as close to the Platform LAN connect component (82562ET or 82562EM) as possible. This is due to the fact that these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

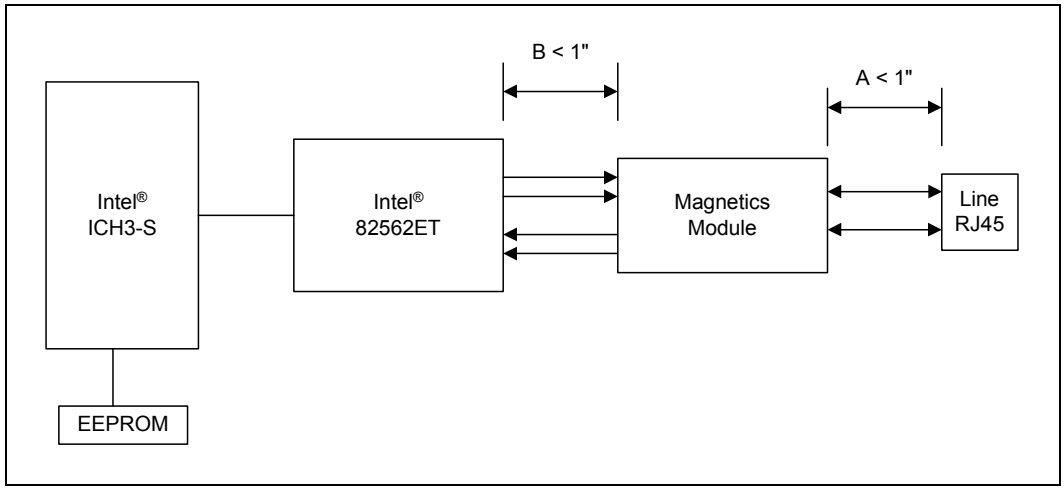
Figure 9-17. Intel® 82562ET/EM Termination



9.7.4 Critical Dimensions

There are two dimensions to consider during layout. Distance 'A' from the line RJ45 connector to the magnetics module, and distance 'B' from the 82562ET or 82562EM to the magnetics module. The combined total distances A and B must not exceed 2 inches. (See Figure 9-18.)

Figure 9-18. Critical Dimensions for Component Placement



Distance from Magnetics Module to RJ45 (Distance A)

The distance A in Figure 9-18 should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than 1 inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation, and with exactly the same lengths and physical dimensions (for example, width).

Warning: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562ET must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562ET and RJ45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often results in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω –110 Ω should compensate for second order effects.

Distance from Intel® 82562ET to Magnetics Module (Distance B)

Distance B should also be designed to be less than 1 inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and equal length within each differential pair.

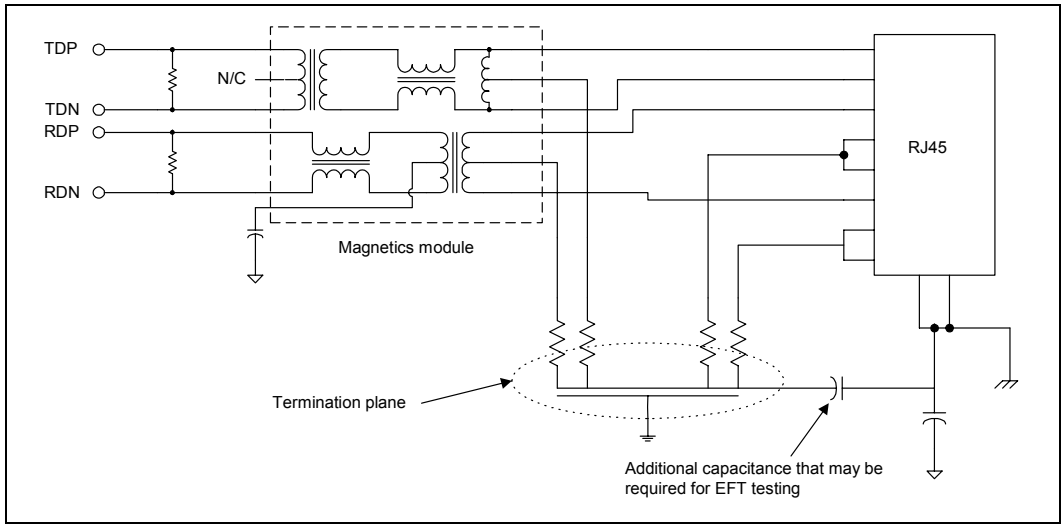
9.7.5 Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the "Bob Smith" Termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane, and couples capacitively to the ground plane creating the required 1500 pF of capacitance. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used to meet the EFT requirements, it should be rated for at least 1000 Vac.

Figure 9-19. Termination Plane



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Debug Tools 10

The debug port design information can be found in a separate document. The routing of the signals, the signal levels, and all other information required to develop a debug port on this platform can be found in the *ITP700 Debug Port Design Guide*.

10.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the system bus of Intel Xeon processors. Contact Tektronix, Inc. and Agilent Technologies to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of these systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a system that can make use of an LAI: mechanical and electrical.

10.2 Mechanical Considerations

The LAI is installed between the processor socket and the microprocessor. The LAI pins plug into the socket, and the microprocessor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the microprocessor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keep-out volume remains unobstructed inside the system.

10.3 Electrical Considerations

The LAI also affects the electrical performance of the system bus. Therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that the tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution it provides.

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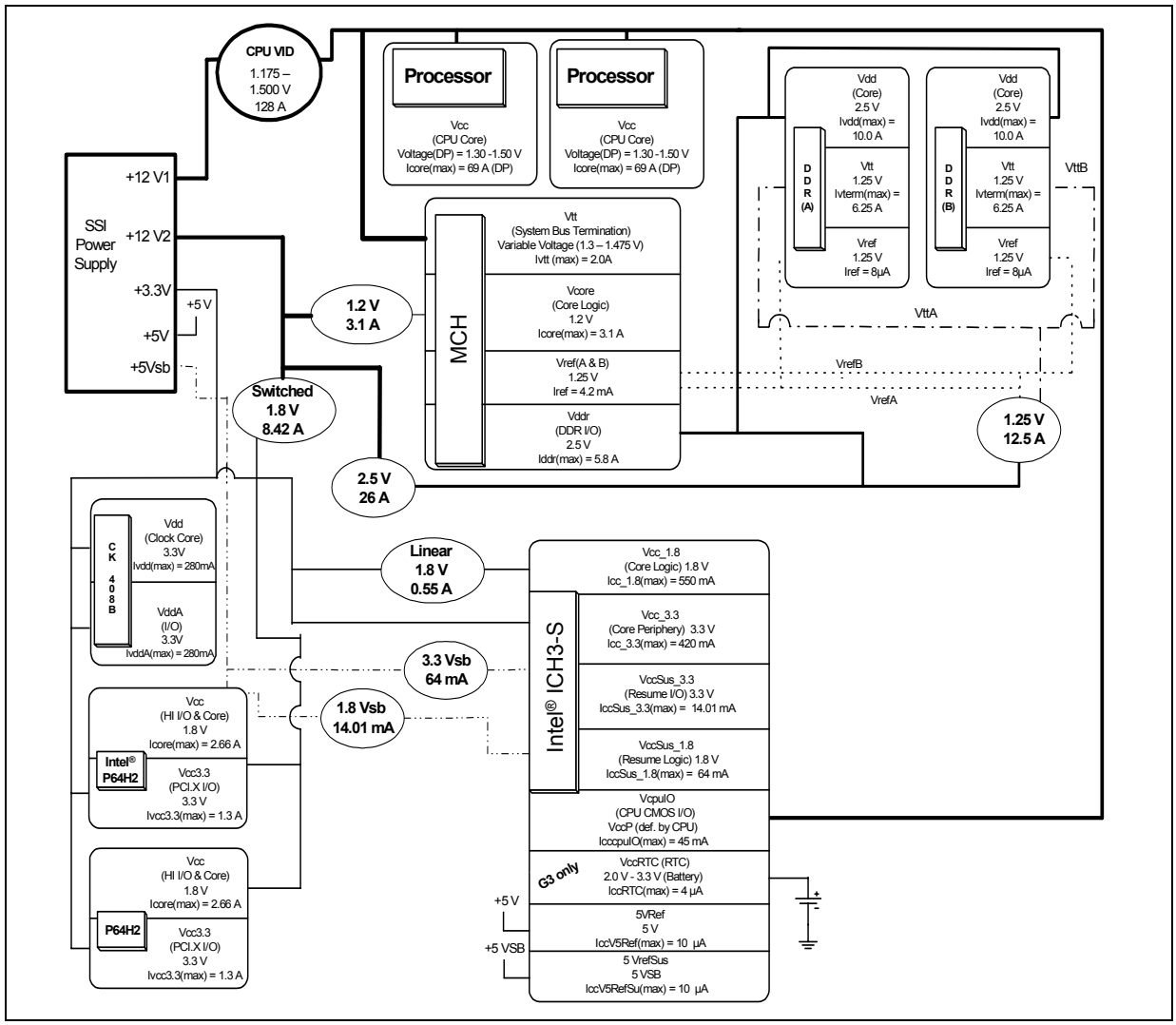
Platform Power Delivery Guidelines 11

This chapter provides an example for board power delivery and the power requirements for some board components.

11.1 Customer Reference Board Power Delivery

Figure 11-1 shows the power delivery architecture for the E7501 Chipset Customer Reference Board.

Figure 11-1. Power Delivery Example



NOTE: The examples given in this Design Guide are only examples. Many power distribution methods achieve similar results. It is critical, when deviating from these examples in any way, to consider the effects of the change.

11.1.1 12 V

System designs may require user access to energized areas of the system. In these cases the power supply may be required to meet regulatory 240 VA limits for any power rail. Since the +12 V rail combined power exceeds 240 VA it must be divided into separate channels to meet this requirement. Each separate rail needs to be limited to less than 20 A for each +12V rail. +12V1 is dedicated for providing power to the input of the processor voltage regulator. The +12V2 rail is used to power the rest of the board +12 V power needs and peripherals devices, such as the 1.2 V, 1.8 V, and 2.5 V regulators.

11.1.2 Processor Core Voltage

The processor core voltage power plane is used to power the processors. The processor core voltage operates between 1.30 V and 1.50 V. A VRM 9.1 compatible design is required for all Intel Xeon processor based platforms. The Voltage Regulator solution can be either a VRM 9.1 or a VRD design. The voltage regulator solution can be either a Voltage Regulator Module (VRM) 9.1 or Voltage Regulator Down (VRD)-based design that meets the *Voltage Regulator Module (VRM) 9.1 DC-DC Converter Design Guidelines* or *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines* respectively. The processor core voltage plane also provides power to the MCH system bus signal I/O buffers and termination.

11.1.3 2.5 V

The 2.5 V power plane is used to provide power to the DDR DRAM core, the MCH DDR IO ring, and reference voltage to the 1.25 V switching regulator. The 2.5 V power plane is created using a switching regulator, which should be able to support up to 26 A of current. This switching regulator receives its input directly from the 5 V power rail of the power supply. The DDR DRAM core requires at most 20.0 A of current. This value is a worst-case current, and is based on DRAM vendor specific specification for maximum current. Power levels will vary. In some cases, current requirements may be less than half of this maximum value, but a maximum current level of 20.0 A should be used to allow interoperability among DRAM devices. The current dedicated for VDD in the MCH is 6.8 A. This regulator is required in all designs.

11.1.4 1.25 V

A voltage regulator derived off 2.5 V produces two 1.25 V rails. One is for the MCH reference voltage (VREF); the other is for DDR termination voltage (VTERM). The switching regulator divides the 2.5 V power rail by 2 to drive 1.25 V reference voltage. This provides some common-mode noise rejection between the DDR termination and I/O voltages. The entire power plane requires about 12 A of maximum current, and can be achieved by using either one or two regulators (one for both channels or one for each channel).

11.1.5 1.8 V

There are two 1.8 V power planes on the reference design. One is created using a switching regulator sourcing from the 5 V power rail on the power supply delivering a bulk of the platform 1.8 V current. This powers the 1.2 V regulator and the hub interface I/O rings of the P64H2s, totaling approximately 8.42 A. A secondary linear voltage regulator is used to supply the 1.8 V rail for the ICH3-S to ensure that the ICH3-S 1.8 V rail is never more than 2 V less than the 3.3 V rail. The hub interface on each P64H2 device consumes about 2.66 A. The hub interface on the ICH3-S device consumes about 550 mA of current.

11.1.6 1.2 V

The 1.2 V power plane powers the MCH core logic requiring 4.5 A. A switching regulator using either the 3.3 V or the 5 V power rail is the regulator's input to power the 1.2V plane.

11.1.7 5 VSB

The 5 VSB power plane comes directly off the 5 VSB power rail and has two functions, to provide power to resume functions via a 3.3 VSB regulator in I/O devices off of the ICH3-S, and to provide 1.8 VSB power through a linear regulator. The resume I/O segment of the ICH3-S requires 64 mA of current, while the 5 VSB-to-1.8 VSB regulator requires 14.01 mA.

11.1.8 3.3 VSB

The 3.3 VSB power plane is the output of a 5 VSB-to-3.3 VSB voltage regulator. The power plane is used solely for the resume I/O features of the ICH3-S. This segment is given only about 64 mA. This regulator is required in all designs.

11.1.9 1.8 VSB

As stated before, the 1.8 VSB provides power to the resume logic within the ICH3-S. This logic uses about 14 mA. This regulator is required in all designs.

11.1.10 Power Summary

Table 11-1 summarizes the platform power. For current, up to date values, refer to each component's datasheet.

Table 11-1. Power Summary

Power Rail	Source	Destination	Max Current
Processor	VRM 9.1 / VRD	2 Processors, MCH, Intel® ICH3-S	140 A
2.5 V	12 V switching regulator	MCH DDR	27 A
1.25 V	5 V to 2.5 V switching regulator	MCH DDR	12.5 A
1.8 V	12 V switching regulator	Intel® P64H2, 1.2 V switching regulator	8.42 A
1.8 V	3.3 V linear regulator	ICH3-S	550 mA
1.2 V	12 V switching regulator	MCH	4.5 A
5 VSB	Power Supply	3.3 VSB, 1.8 VSB	78 mA
3.3 VSB	5 VSB voltage regulator	ICH3-S	64 mA
1.8 VSB	5 VSB voltage regulator	ICH3-S	14 mA

11.2 Processor Power Distribution Guidelines

11.2.1 Processor Power Requirements

This section describes the requirements for supplying power to an Intel Xeon processor. For detailed electrical specifications, refer to the *Intel® Xeon™ Processor Datasheet*. The processor allows the use of Auto HALT, Stop-Grant, and Sleep states to reduce power consumption by stopping the clock to specific internal sections of the processor and the BCLK depending on each particular state. This can create load-change transients as high as 450 A/µs on VCC_CPU at the socket pins. Note that the processor can also cause load changes of this magnitude while executing regular code. In this document, a load-change transient is a change from one current requirement (averaged over many clocks) to another. In the future, the processor may require higher currents and different voltages.

11.2.1.1 Multiple Voltages

"VCC_CPU" in this section refers to the processor core VCC, cache supply voltage, and Assisted Gunning Transceiver Logic + (AGTL+) supply voltage. In the processor, the core and cache are on the same silicon and are powered from the same power plane.

For the processor, VCCMAX = 1.500 V and SM_VCC_CPU = 3.3 V. The VCCA supplies power to the processor core and on-die termination used for the AGTL+ bus.

VCCIOPLL, VCCA, and VSSA are the power supplies to the internal PLL. VCCIOPLL,VCCA and VSSA must be connected to VCC_CPU through a discrete RLC filter as described in Section 11.2.7. Refer to the *Intel® Xeon™ Processor Datasheet* for the pin locations of these voltages.

11.2.1.2 Voltage Tolerance

Refer to the *Intel® Xeon™ Processor Datasheet* for voltage tolerance specifications. Failure to meet these specifications on the low-end tolerance results in transistors slowing down and not meeting timing specifications. Not meeting the specifications on the high-end tolerance can cause damage or reduce the life of the processor.

The Intel Xeon processor specifications for VCC_CPU and ICC are not independent. The VID definition is changed to absolute maximum VCC_CPU allowed. ICC_MAX is measured at VCC_MAX.

11.2.2 Power Delivery Layout Requirements

This section provides processor power delivery layout requirements that are common to both VR Module (VRM) and VR Down (VRD) based designs. Designing a dual-processor system which shares the same power plane requires careful consideration of how the VRM or VRD delivers power to two processors that can vary their DC and AC loading requirements. Specific placement recommendations for the VRM and VRD are detailed in Section 11.2.4 and Section 11.2.5 respectively. Note that the Voltage Regulator must be placed as close as possible to its processor, on one of the two sides of the socket that has the greatest density of power and ground pins.

The maximum distance between each processor and its voltage regulator module or the output inductors of an embedded Voltage Regulator should not be greater than 1.5 inches. To be more specific, the distance between the facing edges of the Voltage Regulator connector and the socket should be no more than 0.5 inch.

Processor VCC_CPU static and transient tolerances and the corresponding Voltage Regulator tolerances assume power distribution paths with resistances no greater than 0.4 mΩ and inductances no greater than 0.1 nH. Meeting these limits can be a challenge because of system layout constraints.

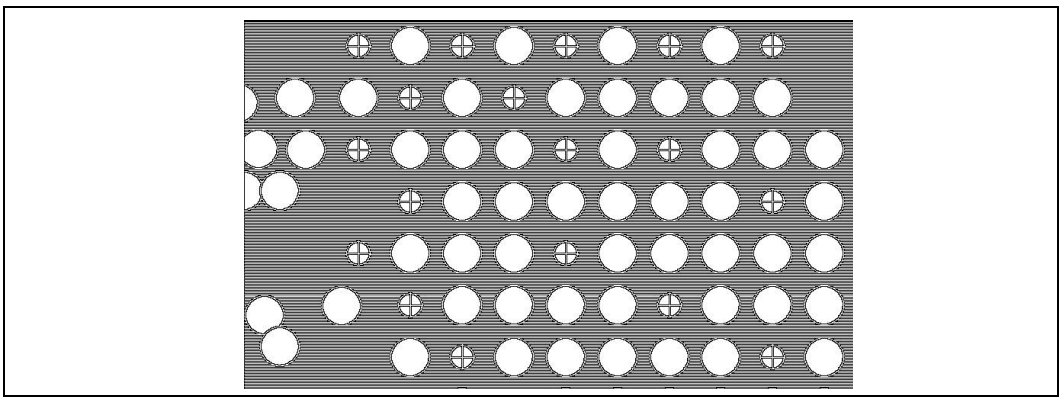
Refer to Figure 3-1 for the recommended stack-up showing power and ground layer implementation. Power must be distributed as a plane. This plane can be constructed as an island on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. Processor power should never be distributed by traces alone.

Because processor voltage is unique to most system designs, a voltage island is probably the most cost-effective means of distributing power to the processors. This island should not have any breaks from the source of power to the load to minimize inductance in the plane. It should completely surround all of the pins of the source and all of the pins of the load.

Use a 2 oz. copper power plane for VCC_CPU and a 2 oz. copper power plane for ground. Using the recommended power and ground plane copper weight and geometries minimizes resistance and inductance in the planes that affects the ability of the voltage regulator and decoupling to meet the DC and AC power requirements of the processors. This can be implemented on two 1 oz. copper layers or four 1/2 oz. copper layers. The bulk capacitors can be placed close to the processors, and the high-frequency capacitors should be placed next to the processors. Distribute the bulk and high-frequency capacitors equally on both sides of the socket where the power/ground pins are located.

The Intel Xeon processor socket has 603 or 604 pins (depending on processor package: refer to Table 1-4) with a 50-mil pitch. The routing of the signals, power, and ground pins require creation of may vias. These vias cause a “swiss cheese” effect in the power and ground planes beneath the processor, resulting in increased inductance of these planes. To minimize this swiss cheese effect, the power / ground planes should completely surround all of the pins of the VRM or VRD and processor socket. Also minimize the size of the processor socket vias’ anti-pads where possible. Anti-pads should be no larger than 35 mils. Figure 11-2 shows an example of good socket power/ground plane routing for an inner layer. Note the absence of plane cuts or other plane discontinuities that inhibit the current flow to these power pins. Bad power/ground routing to the processor socket pin vias and large anti-pads reduce the amount of effective copper, which may result in highly inductive current paths in the socket breakout region. Locations of the capacitor pads on the outer power layer should not hinder power distribution by creating a “slot”-shaped geometry in the plane. This can limit the ability of the decoupling capacitors and/or voltage regulator to supply the necessary current response to processor transients. It is recommended that you place as many high-frequency capacitors as possible inside the cutout of the processor socket. The remaining high-frequency capacitors should be placed next to the processor, specifically near the power/ground pins.

Figure 11-2. Example of Good Plane Distribution to Power or Grounds of the Processor Socket



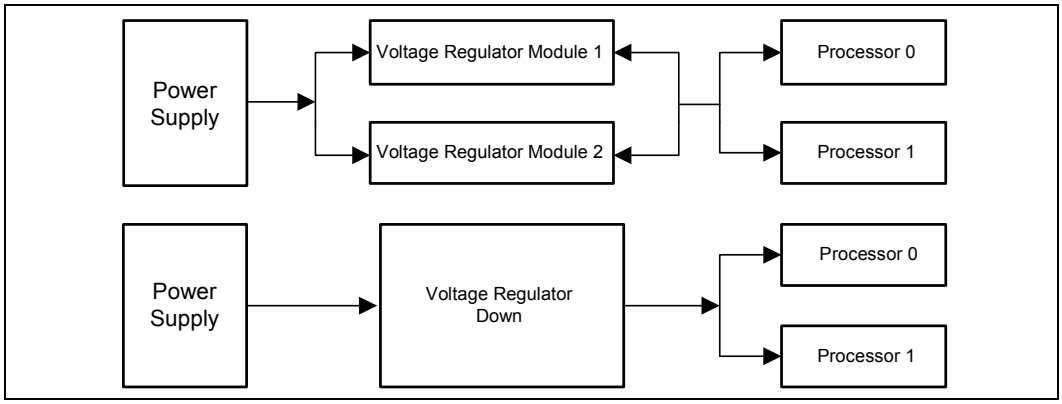
The data bus must route over a uniform power plane because of signal quality constraints. Consequently, in a multiprocessor system design, a single power plane should be used for power delivery to all processors. Multiple processors operating at different voltages are not supported, and will not be validated by Intel.

The processor VCCSENSE and VSSSENSE pins must be routed to vias. The vias should be as close to the socket pins as possible and should be connected with low impedance traces. Because these signals provide measurement points to verify adherence to the processor's VCC_CPU specifications, the vias need to be accessible to measurement equipment. These pins must not be used as SENSE lines to the VRs.

11.2.3 Voltage Regulator Requirements

Intel requires a local VRM 9.1-compliant Voltage Regulator for VCC_CPU. As shown in Figure 11-3, it can be either one Voltage Regulator Module (VRM 9.1) DC-to-DC converter for each processor, or one Voltage Regulator-Down (VRD) solution for both processors in a DP system. Refer to either *VRM 9.1 DC-DC Converter Design Guidelines* or *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines* for Voltage Regulator tolerance specifications (regulation requirements at the voltage regulator remote sense point located at the geometric center of the processors). These two documents are referred to as the voltage regulator guidelines.

Figure 11-3. Power Distribution Block Diagrams for DP System Motherboard



The voltage regulator should be capable of accepting a 5-bit VID code, which is used to indicate the maximum voltage allowed by the individual processor unit. The VID values are documented in the *Intel® Xeon™ Processor Datasheet*.

11.2.3.1 Input Voltages and Currents

To minimize power distribution losses, the recommended main power source for the VR is 12 V +5%, – 8%. This voltage is supplied by a conventional server power supply such as the SSI EPS-12 V. The system designer should ensure that the input circuit of the VR incorporates the necessary local bulk bypassing on the 12 V rail.

11.2.3.2 Power Good Output (PWRGD)

The VR should provide an open collector or equivalent Power Good signal consistent with TTL DC levels. This signal should transition to the open (>100 kΩ) state within 10 ms of the output voltage stabilizing within the specified processor operating voltage range. The signal should be in the low impedance (to ground) state when VCC_CPU is outside of the required range, and should

be in the open state whenever VCC_CPU is within its specified range. At power up, the PWRGD signal must remain in the low-impedance state until the output voltage has stabilized within the required tolerance.

The minimum voltage at which PWRGD is asserted should be the minimum VCC_CPU specified in the *Intel® Xeon™ Processor Datasheet*, minus margin to prevent false deassertion, but at least 95% of (VID minus 125 mV). The maximum voltage at which PWRGD is asserted should be the VID set-point voltage, plus margin to prevent false deassertion, but must be no greater than (VID plus 250 mV).

This PWRGD should be capable of sinking up to 4 mA while maintaining a voltage of 0.4 V or lower. When the output is in the open state, it should be capable of withstanding up to 5.5 V. Latch-up or damage cannot occur if the pull-up voltage on the system board is present with no +12 V input present. VR Power Good should remain low if the VR is disabled by the Output Enable (OUTEN) pin.

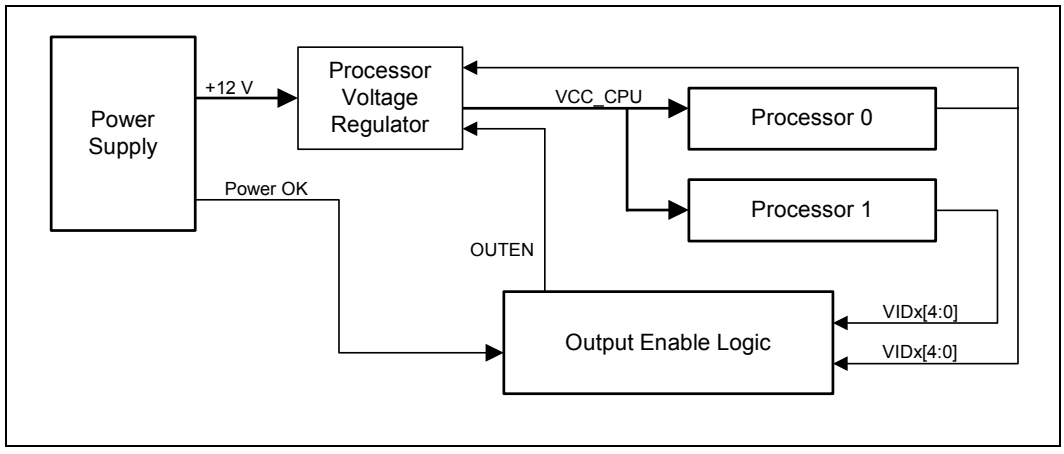
11.2.3.3 Fault Protection

When looking for a VR solution, you can look for some fault protection features. The features help the VR to prevent damage to itself and the circuits it powers. The VR should provide over-voltage protection (OVP) by including a circuit, separate from the voltage sense path, capable of shutting off the output drive when the output voltage rises beyond Vtrip. The power input (12 V) should be protected with a fuse rated not greater than 30 A that sustains all operating and inrush conditions, and that "blows" only for catastrophic failure of the VR. The VR should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the unit. If the VR goes into a shutdown state due to a fault condition on its output (not an internal failure), it should return to normal operation after the fault has been removed, or after the fault has been removed and power has been cycled off and on.

11.2.3.4 VID Routing and Enable Logic

Figure 11-4 shows the recommended implementation of logic for monitoring the VID pins of all processors. This logic will determine that all of the installed processors are requesting the same VCC. If mixed voltage processors are detected, the output enable signal (OUTEN) of all VRs must be disabled. Note that if the middle processor is not installed, the VID[4:0] of that processor are all high, and this should not cause disabling of the output of other VRs. The VID lines must be pulled up internally in the VR.

Figure 11-4. VRM VID Routing



11.2.4 VR Module 9.1 Recommendations

Intel has defined VRM 9.1 for supplying VCC_CPU power to Intel Xeon processor based systems. The VRM 9.1 definition includes Remote-Sense, Current Share, and Output Enable features. VRM 9.1 suppliers must provide these features and must meet voltage and current requirements set forth in the *VRM 9.1 DC-DC Converter Design Guidelines*.

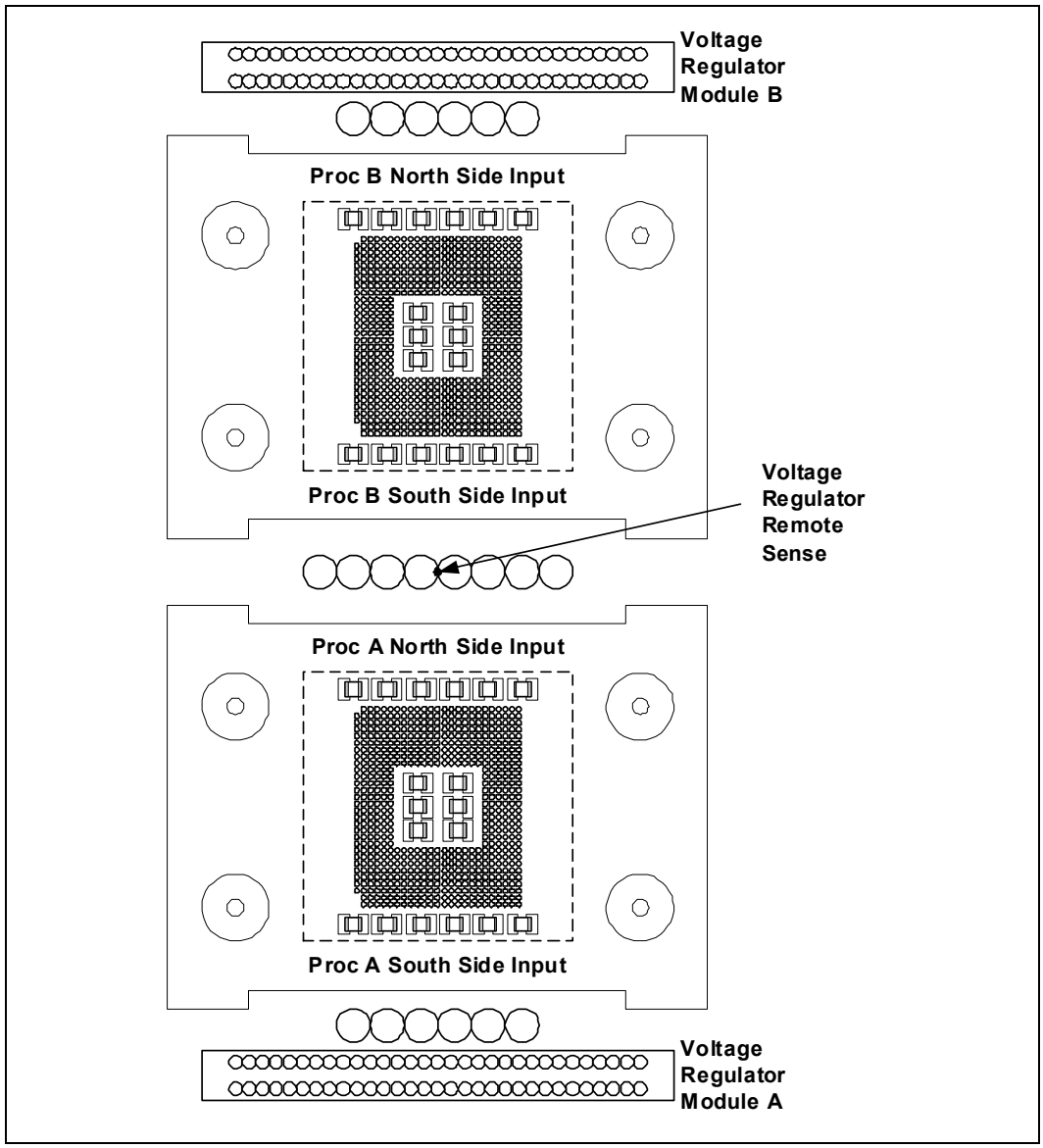
The VRM 9.1 Module, which provides VCC_CPU supply to the Intel Xeon processor, has the capability of supplying a broad range of voltages (+1.1 V to +1.85 V).

It is highly desirable in DP applications that a current-sharing capability be available. The VRM 9.1 covers the specification for supporting this feature. A VRM 9.1 designed for current sharing must be capable of continuously producing a current that is higher than the rated value by a factor of half of the current sharing accuracy. For example, if a particular VRM 9.1 is designed to supply a 50 A processor as a maximum with 10% accuracy, the difference between the output currents of two or more VRM 9.1s in parallel may be as much as 5 A at any value of current actually produced, even to the point where one VRM 9.1 is producing 5 A, and one in parallel with it is producing no current in supplying a 5 A load. This is necessary to insure that the higher-current VRM 9.1 in a current-sharing pair does not operate above its limits due to current sharing errors. One pin of the VRM 9.1 is reserved for current sharing control for a VRM 9.1 designed for star-point or single-wire current sharing (i.e., Ishare). This pin will be connected to other VRM 9.1s within the system.

The VRM 9.1 output slew rate is specified at 50 A/µs. The slew rate for the Intel Xeon processor is 450 A/µs at the socket pins. The system designer must provide adequate bulk and high-frequency decoupling on the motherboard to meet the appropriate processor required slew rate.

Figure 11-5 shows the recommended VRM implementation referred to as the “row” pattern since the VRM and processor sockets are placed in a row with one another. The advantages of this placement is that the VRM current flow to its adjacent processor socket is not restricted by the other VRM.

Figure 11-5. "Row" Pattern with Voltage Regulator Module



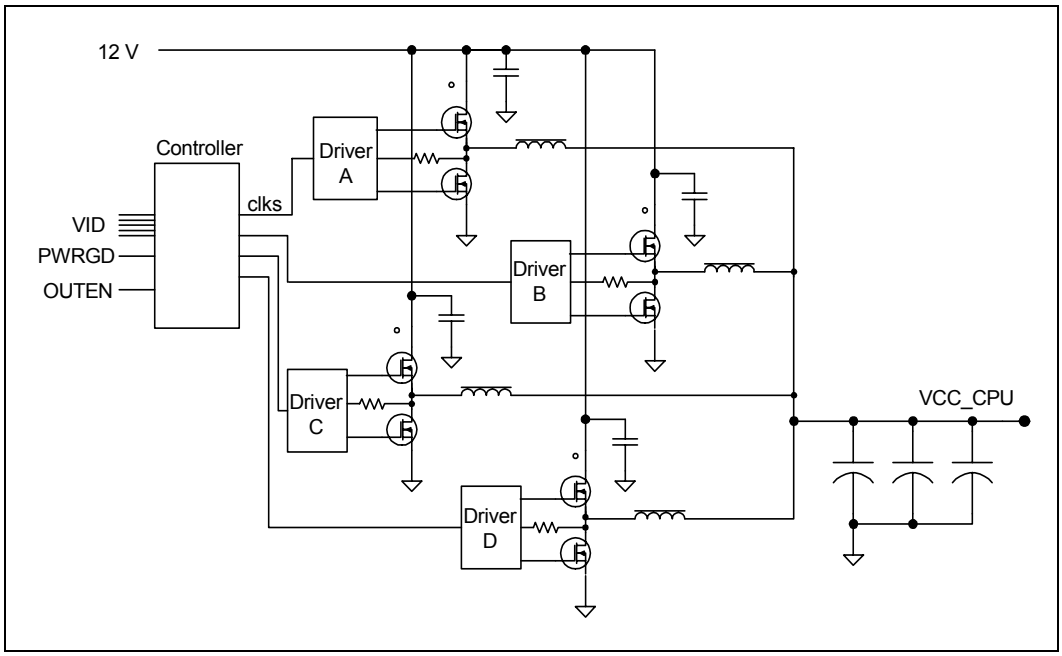
If available on the VRM, route the differential remote SENSE input signals (VO-sen+ and VO-sen-) from both VRM connectors to the middle of the VCC_CPU plane. These input signals allow the VRMs to sense output voltage and compensate for DC losses in the power distribution path. The round trip trace resistance of these signals should not be greater than 1 Ω. These voltage SENSE signals draw little current and should only have a minute voltage drop from the remote sense connection to the VRM socket.

Route the VO-sen+ signal for each VRM to the same point on the VCC_CPU power plane in the middle of and equidistant from both processors. Middle is defined as a point that provides the shortest geometrical mid-point between the centers of the processor sockets. Route the VO-sen- signal for each VRM to the same point at the corresponding X-Y location for the VO-sen+ route, but on the VCC_VSS ground plane. See Figure 11-5 for an example of sense point locations for the example VRM topology. The VO-sen+/VO-sen- signals should be routed directly from the VRM to the remote sense point without exceeding 5 inches in trace length.

11.2.5 VR Down Recommendations

Figure 11-6 is a simplified block diagram of a four-phase, interleaved VRD implementation.

Figure 11-6. Simplified VRD Circuit Example



11.2.5.1 VRD Placement

Figure 11-7 and Figure 11-8 show the two recommended VRD placements. Figure 11-7 is referred to as the "L" pattern since it has the two processor sockets and the VRD placed in an offset manner in the shape of an L. Figure 11-8 is referred to as the "row" pattern since the two sockets are placed in the same line, with the VRD directly beneath both sockets. The advantage of both VRD placements are that the VRD current can flow to both processor sockets without overlapping currents or causing interference between both sockets. These placements also minimize and equalize the distance from the VRD to each socket.

Figure 11-7. “L” Pattern with Voltage Regulator Down

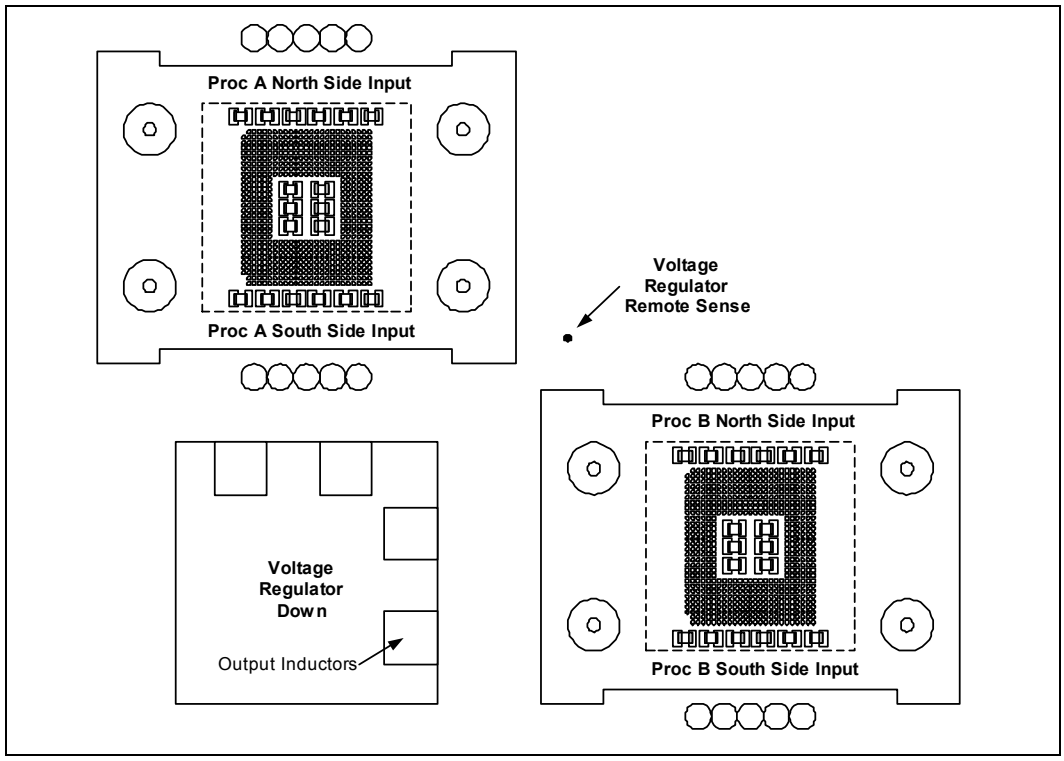
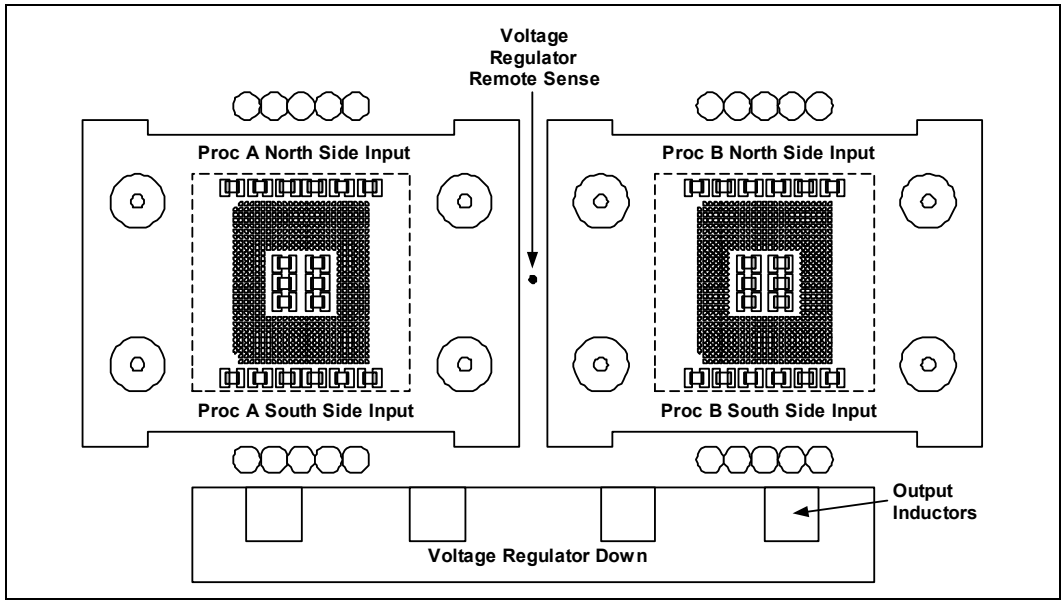


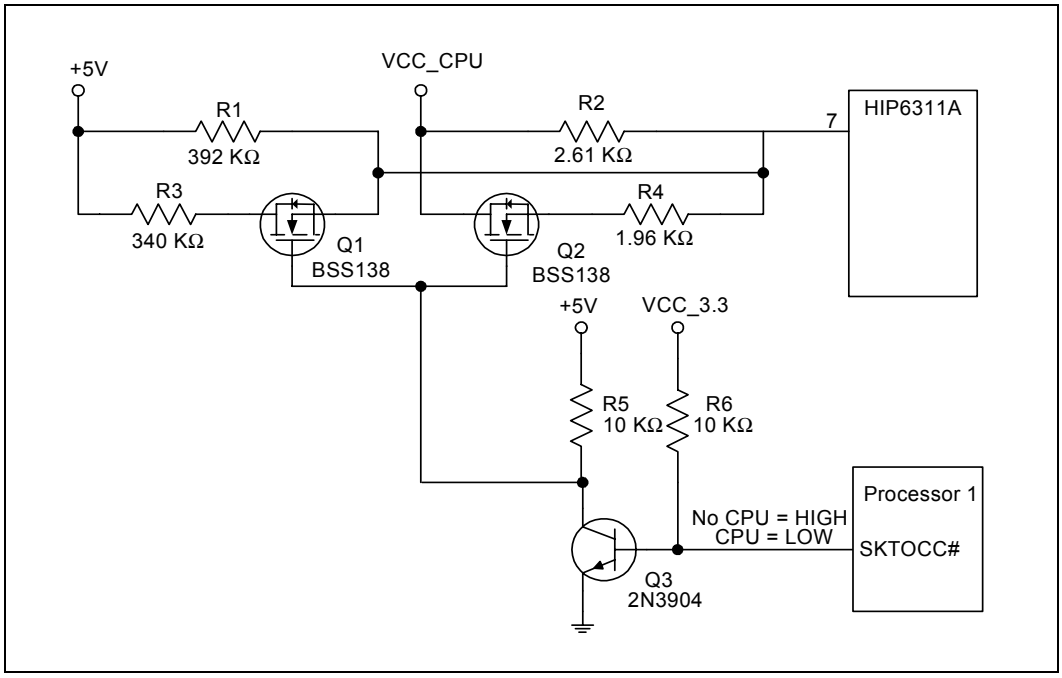
Figure 11-8. “Row” Pattern with Voltage Regulator Down



11.2.5.2 Loadline Selection Circuitry

Many OEMs require that a dual-processor VRD supplying an Intel processor's common voltage plane operate with either one or two processors installed on the board (i.e., the design must meet the static and transient voltage characteristics of both the dual- and single-processor load lines). Failure to adjust the voltage regulator's loadline output based on the number of processors installed will deteriorate the regulator's ability to meet the processor's static loadline requirements under varying loads when one and two processors are installed. A solution is to adjust the load line for the number of installed processors. OEMs that want jumper-free systems can do this with logic that detects the presence of processors in each of the sockets, and selects resistor combinations to produce the right slopes. For example: no processors (00) = disable VRD; one processor (01 or 10) = single-processor load line; both processors (11) = dual-processor load line. Figure 11-9 shows an example of how to implement such circuitry.

Figure 11-9. Example Load Line Selection Circuit



The theory of operation of the dual processor load line selection circuit is straightforward. If a second processor (Processor 1) is not present, the base of Q3 will be pulled high. This causes Q3's collector to go to ground, turning off Q1 and Q2. The VCC_CPU voltage will then go through R2 (droop resistor) to pin 7 (FB) of the HIP6311A controller. The offset voltage comes from the +5 V source through R1 into pin 7 of the controller. R3 and R4 will have no effect.

If a second processor is present, the base of Q3 will be pulled low and Q3's collector will be high, turning on Q1 and Q2. The droop resistor, R2, will now be paralleled by R4, providing the droop required for a two-processor system. The offset resistor, R1, will be paralleled by R3 providing the offset for a two-processor system.

11.2.5.3 VRD Circuit Implementation

This section contains general VRD circuit and layout implementation recommendations. For specific VRD design details, refer to the *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines* and VRD vendor documentation.

Route the VRD's voltage sense input signal to the middle of the VCC_CPU plane. The location of this plane connection and route is not critical. The voltage regulator Pulse Width Modulation (PWM) uses the voltage sense pin to monitor the VRD output voltage, which is used to generate the VRD power good signal.

The VRD circuit should contain low-pass filters (RC) on the output of each MOSFET phase. This filter reduces output noise and helps stabilize the VRD's operation. The exact filter values will depend on the voltage regulator PWM controller and MOSFET components used. Include series inductors at the output of each MOSFET phase. The exact value should be carefully chosen and will depend on the actual VR components used. Lowering the inductance value increases the transient current (dI/dt) capability of each output phase, but will increase power dissipation from the MOSFETs.

Carefully select the switching frequency of the PWM controller using the methods specified by the PWM vendor. The switching frequency should be chosen to support the static and transient requirements of both processors. Increasing the frequency will increase the response of the VRD, but will also increase the power dissipation of the phase drivers and MOSFETs.

Route the positive (and negative if the VRD provides differential inputs) voltage feedback inputs for the VRD to the VCC_CPU plane with the following conditions.

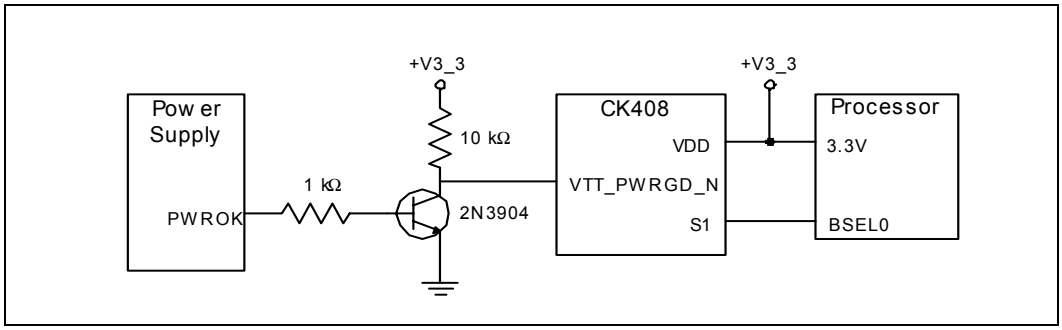
- They must be connected to the power plane through a series resistor. This resistor should be sized to provide the correct droop to satisfy the load line requirement.
- They must affect less than 1 Ω roundtrip resistance to minimize the voltage drop between the sense point and VR input.
- Route the positive feedback line to a point on the VCC_CPU power plane in the middle of and equidistant from both processors. Middle is defined as a point that provides the shortest geometrical mid-point between the centers of the processor sockets.
- Route the negative feedback line to the corresponding X-Y location, but on the VCC_VSS ground plane. See Figure 11-7 and Figure 11-8 for an example of sense point locations for the example VR topologies.
- Route each of the feedback lines with less than 5 inches total trace length. Do not route near signal lines unless shielding is provided.
- The trace(s) should be carefully routed to avoid picking up noise.

11.2.6 Voltage Sequencing

When designing a system with multiple voltages, there is always the issue of ensuring that no damage occurs to the system during voltage sequencing. Voltage sequencing is the timing relationship between two or more voltages such as VCC_CPU and SM_VCC/VID_VCC. SM_VCC/VID_VCC is defined as 3.3 V for the processor.

The processor's BSEL[1:0] outputs use an active driver. A 3.3 V source connected to the processor's 3.3 V pins supplies the VID output. The BSEL[1:0] outputs will be valid within 1 ms after the 3.3 V supply reaches 95% of its nominal value. The system logic must ensure that the clock driver device (e.g., CK408) does not use these inputs until after the BSEL[1:0] signals are valid. An example implementation could utilize the CK408's VTT_PWRGD_N input signal by keeping it deasserted until BSEL is valid. Depending on the design of the system's power sequencing logic, the PWR_OK signal from the power supply may be used to drive this CK408 input signal. Or, this signal could be driven by existing power sequencing delay logic that monitors the 3.3 V supply. See Figure 11-10 for an example of this implementation.

Figure 11-10. CK408 / Processor Power Sequencing Requirement



A voltage of 3.3 V is required for correct operation of the processor VID logic. The processor's VID outputs use an active driver. As shown in Figure 11-11, the VID outputs will be valid within 1 ms after the 3.3 V supply reaches 95% of its nominal value. The system power supply should generate PWR_OK no less than 100 ms after all of its outputs reach their respective 95% values. PWR_OK may be used to enable the VR output. For example a supply adhering to ATX12V design guidelines meets this requirement. The VR's PWRGD output may be used to generate the PWRGOOD input to the processor. PWR_OK should be deasserted when any output of the supply falls below 95% of its nominal value (also consistent with ATX12V). It is important to maintain SM_VCC anytime the output of the VR is enabled. Driving the VR's OUTEN control input with the PWR_OK signal will ensure correct sequencing at both power-up and power-down.

Figure 11-11. Power-Up Sequencing

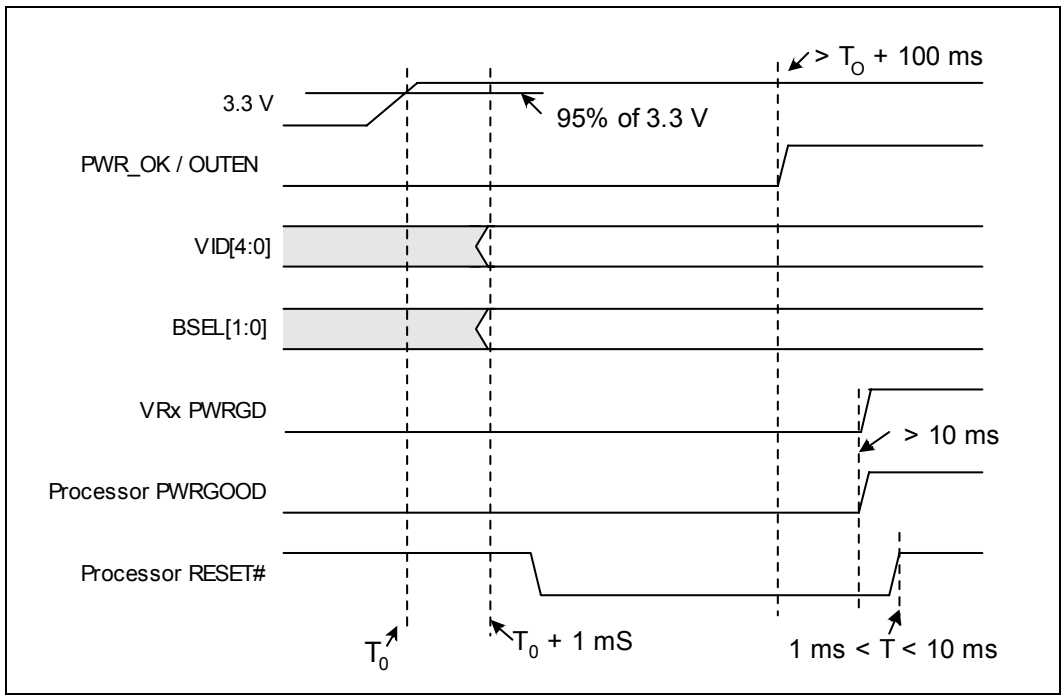
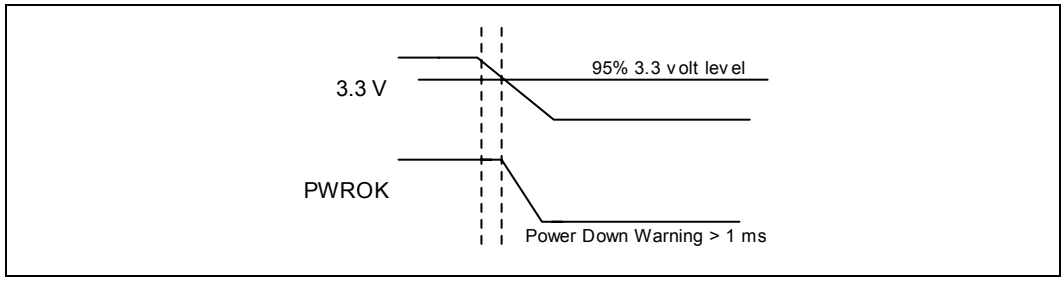


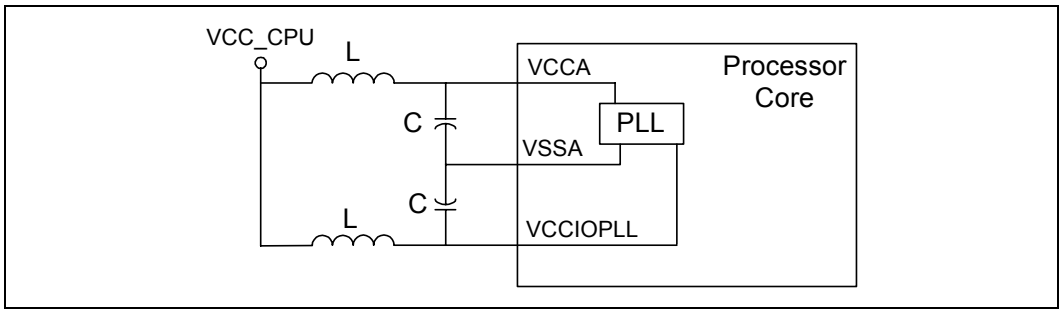
Figure 11-12. Power-Down Sequencing



11.2.7 VCCA, VCCIOPLL, and VSSA Filter Specifications

VCCA and VCCIOPLL are required by the processor's internal PLL. These voltages are created by using a low pass filter on VCC_CPU. The processor has internal analog PLL clock generators that require quiet power supplies for minimum jitter. Jitter is detrimental to a system; it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). The filter topology is shown in Figure 11-13. Not shown in the figure are the parasitics of connecting traces, circuits, and components.

Figure 11-13. Processor Filter Topology



The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation; it also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity, we are addressing the recommendation for VCCA filter design. The same characteristics and design approach are applicable for VCCIOPLL filter design.

Other requirements:

- Filter should support DC current > 30 mA.
- DC voltage drop from VCC_CPU to the processor interposer pin VCCA should be < 33 mV, which in practice implies series R < 1.1 Ω; this also means pass band (from DC to 1 Hz) attenuation < 0.5 dB for VCC_CPU = 1.1 V, and < 0.35 dB for VCC_CPU = 1.7 V.

Table 11-2 and Table 11-3 list some recommended components for the filter. Values in the table are for reference only. For specific vendor information, contact your preferred vendor.

Table 11-2. Component Recommendation—Inductor

Part Number (Reference Designator)	Value	Tol	SRF	Rated I	DCR
TDK MLF2012A4R7KT	4.7 µH	10%	35 MHz	30 mA	0.56 Ω (1 Ω max)
Murata LQG21N4R7K10	4.7 µH	10%	47 MHz	30 mA	0.7 Ω (± 50%)

Table 11-3. Component Recommendation—Capacitor

Part Number (Reference Designator)	Value	Tol	ESL	ESR
Kemet T495D336M016AS	33 µF	20%	2.5 nH	0.225 Ω
AVX TPSD336M020S0200	33 µF	20%	TBD	0.2 Ω

To satisfy damping requirements, total series resistance in the filter (from VCC_CPU to the top plate of the capacitor) must be at least 0.35 Ω. This includes the DCR of the inductor and any resistance (routing or discrete components) between VCC_CPU and capacitor top plate. Keep the routing short and wide. If the total is less than 0.35 Ω, add a discrete resistor to make up the difference. For example, if the selected filter inductor has a minimum of 0.1 Ω DCR and a negligible routing resistance (less than 10 mΩ), add a discrete resistor of approximately 0.3 Ω. The total maximum resistance in each route cannot be more than 1.1 Ω as measured from VCC_CPU (the baseboard via that connects the PLL filter to the VCC_CPU plane) to the processor interposer pin. It is important to keep the total resistance of each of the PLL filter circuits on the motherboard no larger than necessary. Figure 11-14 and Figure 11-15 illustrate the recommended filter circuit. This path includes the total trace resistance (denoted "R-TRACE" in the following figures), discrete resistor (if needed), inductor DCR, and Socket resistance (0.025 Ω). It is important to note that "R-TRACE" includes the total trace resistance between VCC and the processor socket pin, but is represented in the figures as a single resistor to simplify the circuit representation.

Other Routing Requirements:

- C should be as close as possible to VCCA and VSSA pins in the socket (typically < 0.02 Ω per route).
- Route away from clocks and fast switching signals.
- VCCA route should be parallel and next to VSSA route (to minimize loop area).
- VCCIOPLL route should be parallel and next to VSSA route (to minimize loop area).
- L should be close to C; any routing resistance should be inserted between VCC_CPU and L.
- Any discrete R (if needed to meet minimum resistance) should be inserted between VCC_CPU and L.

Figure 11-14. Filter Implementation 1: Using Discrete Resistor

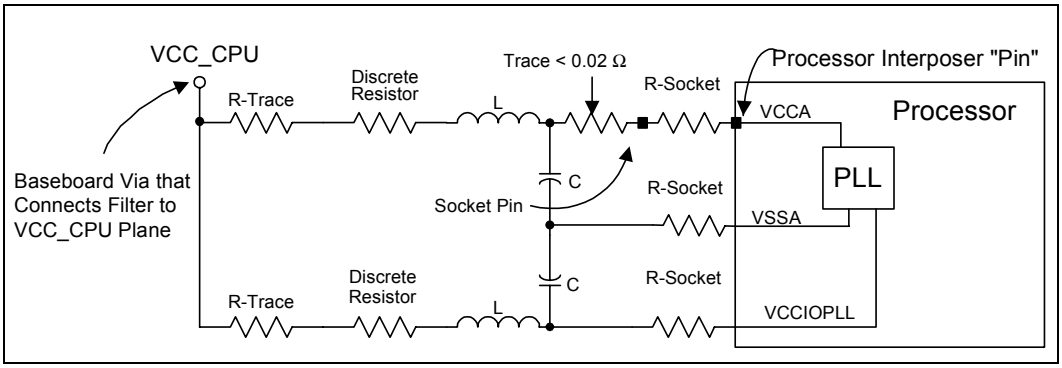
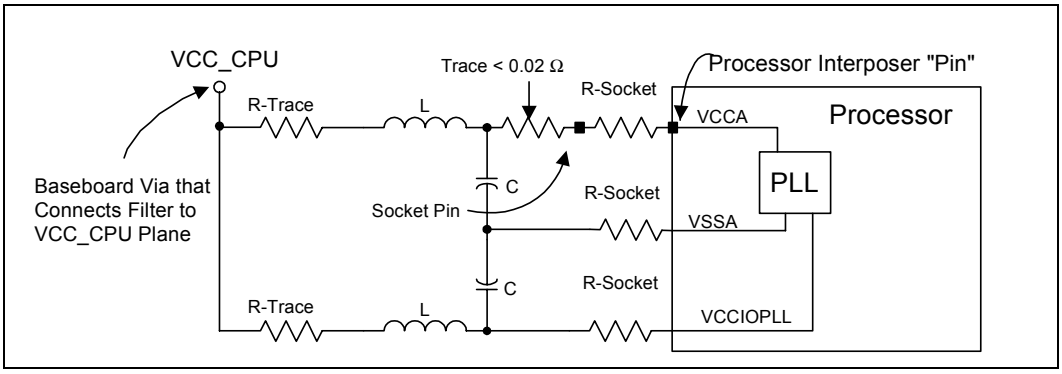


Figure 11-15. Filter Implementation 2: No Discrete Resistor



11.2.8 Power Planes

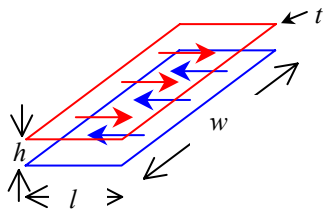
VCC_CPU static and transient tolerances of the processor, and the corresponding voltage regulator tolerances assume power distribution paths with round trip resistances no greater than 300 μΩ and inductances any greater than 100 pH. Power must be distributed as a plane. This plane can be constructed as an *island* on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. Processor power should never be distributed by traces alone.

Because processor voltage is unique to most system designs, a voltage island will probably be the most cost-effective means of distributing power to the processors. This island from the source of power to the load should not have any breaks, so as to minimize inductance in the plane. It should also completely surround all of the pins of the source and all of the pins of the load.

The imperfections of the power planes themselves may introduce unwanted resistance and inductance into the power distribution system. Assuming layer thickness is smaller than skin depth, the metal layer resistance can be calculated as:

$$R = \rho \cdot \frac{l}{w \cdot t}$$

Where ρ is the copper resistivity (ρ = 0.667 mΩ-mil), *l*, *w*, and *t* are the length, width and thickness of the metal layer, respectively.



The loop inductance can be calculated as:

$$L = 31.9 \frac{\text{pH}}{\text{mil}} \cdot \frac{l \cdot h}{w \cdot (N-1)}$$

Where *N* is the number of VCC_CPU/VSS_CPU planes. To minimize parasitic layer inductance, it is important to reduce the distance from decoupling capacitors to the processor socket (reducing *l*) and to use islands for power distribution (increasing *w*). To reduce *h*, it is recommended to select the VCC_CPU/VSS_CPU planes in the layer stack-up that are interleaved and have small spacing in between. As a practical matter, it is impossible to get the requisite baseboard inductance without locally dedicating at least 4 planes to carry power from the baseboard capacitors to the power pins of the processor.

There are impedance consequences for signals that cross over or under the edges of the Power Island that exists on another layer. While neither of these may be necessary for most designs, there are two reasonable options to consider which can protect a system from these consequences:

- Processor power islands can be isolated from signals by one of the solid power plane layers such as the ground layer. This forces a particular stack-up model.
- Another option that helps, but does not completely eliminate radiation effects, is to decouple the edges of the processor power islands to ground on regular intervals of about 1 inch using good high-frequency decoupling capacitors (1206 packages). This requires more components but does not require any particular board stack-up.

In either case, for controlling emissions, all planes and islands should be well decoupled. The exact board layout, and the chassis design will determine the amount of decoupling required for controlling emissions. Proper designs will incorporate additional pads for capacitors to be added in case they are found to be necessary during EMI testing.

Signals routed over power islands or islands in the ground plane create a discontinuity in the return path of that signal. This discontinuity can have detrimental effects on the timing and signal quality of that signal and other signals referencing the same planes. Avoid routing signals over splits in power planes or ground planes at all times.

11.2.9 Processor Decoupling

The inductance of the system due to cables and power planes slows the power supply's ability to respond quickly to a current transient. Decoupling a power plane can be broken into several independent parts. The closer to the load the capacitor is placed, the more inductance is bypassed. By bypassing the inductance of leads, power planes etc., less capacitance is required. However, closer to the load there is less room for capacitance. Therefore, trade-offs must be made.

Using capacitors with the wrong ESR, ESL, and/or package can mitigate their intended operation and result in violations of the processor power specifications. For example, capacitors with the wrong package or with ESR/ESL properties in excess of the recommendations may have increased transient response times that are unable to respond to the processor’s current transients.

11.2.9.1 High-Frequency Decoupling

The system boards should include high-frequency capacitors as close to the socket power and ground pins as possible. A motherboard’s power and ground plane inductance can cancel the usefulness of these low-inductance capacitors if they are not placed close to the socket. Place as many capacitors as possible in the socket cut out area. Table 11-4 lists the recommended high-frequency capacitance for Intel Xeon processor baseboards.

Table 11-4. Processor High-Frequency Capacitance Recommendations Per Processor

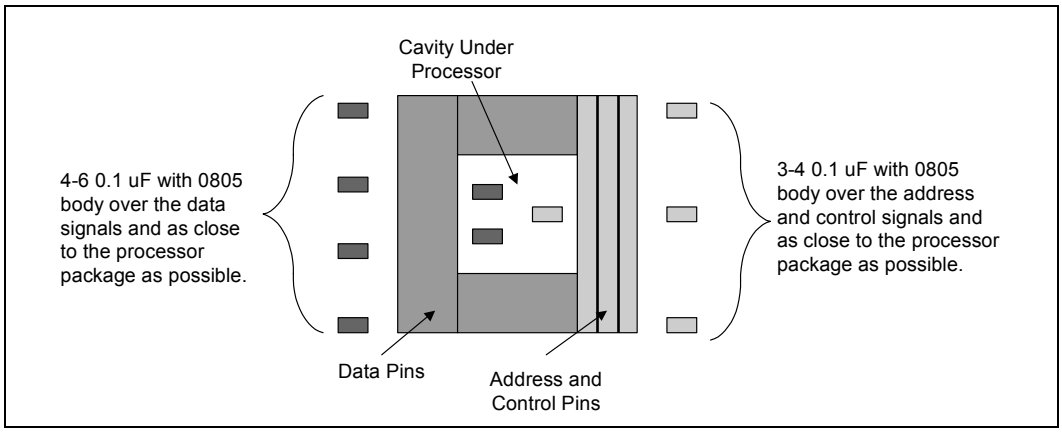
High-Frequency Capacitance	Quantity	ESR	ESL
0805 Package, 1 µF (Signal Integrity)	4	8 mΩ	702 pH
0603 Package, 0.1 µF (Signal Integrity)	3	6 mΩ	630 pH
1210 Package, 22 µF (Power Decoupling)	20	10 mΩ	1.1 nH

If there is difficulty in placing the 1210 size 22 µF capacitors (as listed in Table 11-4), replace those with a same number of 1206 size 10 µF capacitors using similar placement guidelines. However, increase the number of OS-CONs (as defined in Table 11-5) from 10 to 11 to compensate for the reduced total capacitance.

In addition, high-frequency decoupling may be required for signal integrity. System boards designed using striplines with VCC_CPU and ground references should not require high-frequency decoupling beyond the recommendations listed in Table 11-4. For systems using microstrip configurations, a return path discontinuity will exist between the processor and the baseboard due to the baseboard traces having only one reference plane. These systems should distribute decoupling capacitors, as shown in Figure 11-16 and described as follows:

- 4 minimum, 6 preferred 1 µF capacitors with 0805 packages distributed evenly over the data lines.
- 3 minimum, 4 preferred 0.1 µF capacitors with 0603 packages distributed evenly over the address and control lines.

Figure 11-16. Decoupling Example for a Microstrip Baseboard Design



11.2.9.2 Bulk Decoupling

The Intel Xeon processor causes very large switching transients. These sharp surges of current occur at the transition between low-power mode and high-power mode. The designer must support a current slew rate of 450 A/µs at the socket pins.

Load-change transients for the Intel Xeon processor are on the order of 55 A. A load-change transient occurs when coming out of or entering a low-power mode. These are not only quick changes in current demand, but also long lasting average current requirements. This occurs when the STPCLK# pin is asserted or de-asserted, and during Auto HALT. Auto HALT is a low power state the processor enters by issuing a HALT instruction, and a HALT bus cycle is generated.

Note: Note that even during normal operation (not STPCLK# or Halt), the processor current requirements can change by as much as 70% (± 10%) of the max current very quickly.

Table 11-5 lists the recommended bulk capacitance parameters for Intel Xeon processors. The following recommendations indicate the decoupling suggested for each processor in the system.

Table 11-5. Processor Bulk Capacitance Recommendation Per Processor

Bulk Capacitance	Quantity	ESR	ESL	RMS Current Rating
OS-CON, 560 µF	10	12 mΩ	3.1 nH Max	5.04 Arms

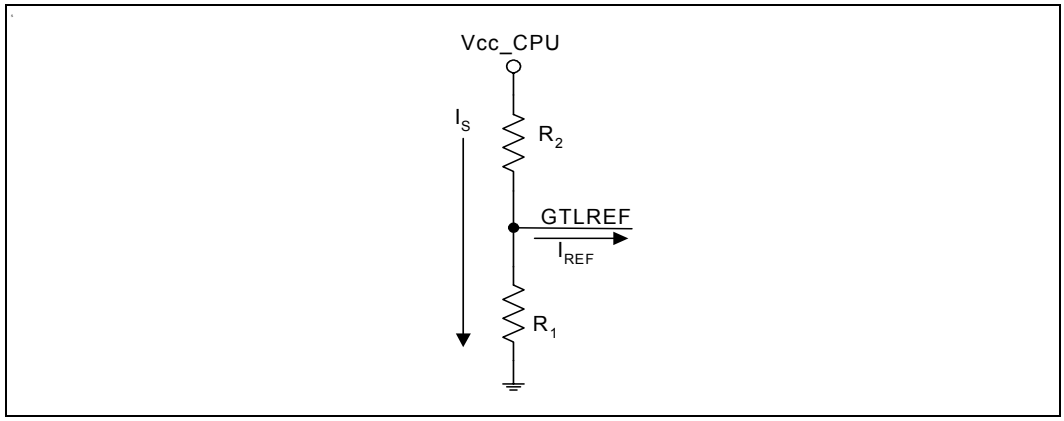
Place some bulk decoupling on the baseboard as close to the processor socket as possible (maximum of 0.5 inch away). The location of bulk capacitance is not as critical as the high-frequency decoupling because more inductance is already expected for these components. However, good placement of these components will affect the transient response of the system for the better, as shown in simulation. Place the remaining bulk capacitors next to the voltage converter module.

Place half on one side of the processor socket, half on the other side as close as the logic analyzer interface (LAI), retention mechanism (RM) and heatsink keep-out zones allow. Capacitors should be placed a maximum of 0.5 inch from the processor socket. Check with your LAI, RM and heatsink vendors for those keep-out zone requirements. When using the Intel Xeon processor boxed processor solution, refer to the *Intel® Xeon™ Processor Datasheet* for keep-out zone details.

11.2.10 AGTL+ Reference Voltage

The processor GTLREF[3:0] and MCH HDVREF[3:0], HAVREF[1:0], and HCCVREF are low current inputs (less than 15 µA each) to the differential receivers within each of the components on the AGTL+ bus. Use a voltage divider to generate a GTLREF[3:0] of 0.63*VCC_CPU ± 2%.

Figure 11-17. GTLREF Divider



R1 and R2 should be small enough values that the current drawn by the GTLREF inputs (IREF) is negligible versus the current through R2 and R1. Equation 11-1 shows GTLREF, where "n" is the number of IREF inputs supplied by the divider.

Equation 11-1. GTLREF

$$GTLREF = \frac{V_{CC}/R_2 - n \times I_{REF}}{1/R_2 + 1/R_1}$$

The worst case GTLREF should be analyzed with IREF at the maximum and minimum values determined for the number of loads being supplied. If the number of loads can change from model to model because of upgrades, this should be taken into account as well. Analyze Equation 11-1 with R1 and R2 at the extremes of their tolerance specifications.

Use two voltage dividers for each processor, and one for the chipset component. Assume a maximum of 15 µA of leakage current per load. These leakage currents can be positive or negative.

The following discussion illustrates using a single voltage divider to support two GTLREF loads assuming VCC_CPU of 1.50 V. Using an 84.5 Ω ± 1% resistor for R1 and a 49.9 Ω ± 1% resistor for R2 in Figure 11-18 creates a static usage of 11.2 mA (1.500 V/149.9 Ω) per voltage divider. The worst case solution for Equation 11-1 can be found with IREF at 30 µA, R1 at the low end of its tolerance specification (83.7 Ω), and R2 at the high end of its tolerance specification (50.4 Ω), yielding Equation 11-2. The target of 0.63 of VCC_CPU is 0.945 V (0.63 * 1.50). This resistive setting satisfies the ± 2% specification.

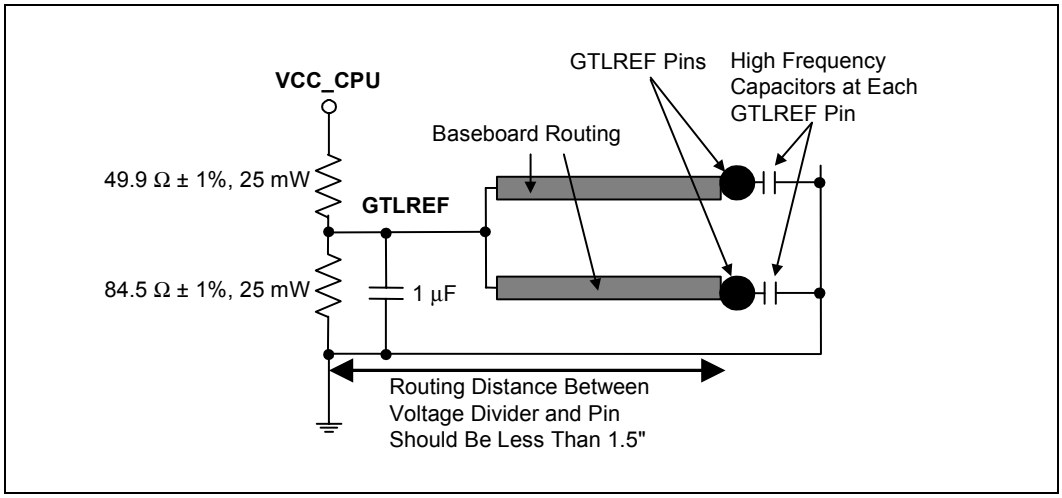
Equation 11-2. Resistor Tolerance Analysis

$$GTLREF = \frac{1.50/50.4 - 0.000030}{1/50.4 + 1/83.7} = 0.927V$$

Decouple GTLREF[3:0] at each pin with a 220 pF capacitor to ground. Decoupling GTLREF to ground at the voltage divider with a 1 µF capacitor may further enhance the ability for GTLREF to track VCC.

When routing GTLREF to the pins, use a 30-mil to 50-mil trace (the wider the better), and keep it as short as possible (less than 1.5 inches). Also, keep all other signals at least 20 mils away from the GTLREF trace. This provides a low impedance line without the cost of an additional plane or island.

Figure 11-18. Suggested GTLREF Generation



11.2.11 Component Models

Acquire component models from their respective manufacturers. Intel cannot guarantee the specifications of other manufacturers' components. Table 11-6 contains some of the models developed by Intel for internal simulations.

Table 11-6. Various Component Models Used at Intel (Not Vendor Specifications)

Component of Simulation	ESR (Ω)	ESL (nH)
0.1 µF Ceramic 0603 package	0.006	0.63
1 µF Ceramic 0805 package	0.080	0.702
10.0 µF Ceramic 1206 package	0.010	0.880
22.0 µF Ceramic 1210 package	0.010	0.880
560 µF OS-CONS	0.012	2.7

11.3 MCH Power Delivery Guidelines

The following guidelines are recommended for an optimal MCH power delivery. The main focus of these guidelines is to minimize chipset power noise and signal integrity problems. The guidelines are not intended to replace thorough system validation of products.

11.3.1 DDR_VTT (1.25 V) Decoupling

To reduce noise on the DDR termination voltage (1.25 V) around the MCH, two 0.1 µF and two 0.01 µF capacitors per-channel are recommended. Evenly distribute placement of decoupling capacitors along the VTT plane around the MCH within 1 inch of the outer row of balls. Ceramic 0603 body type capacitors are recommended.

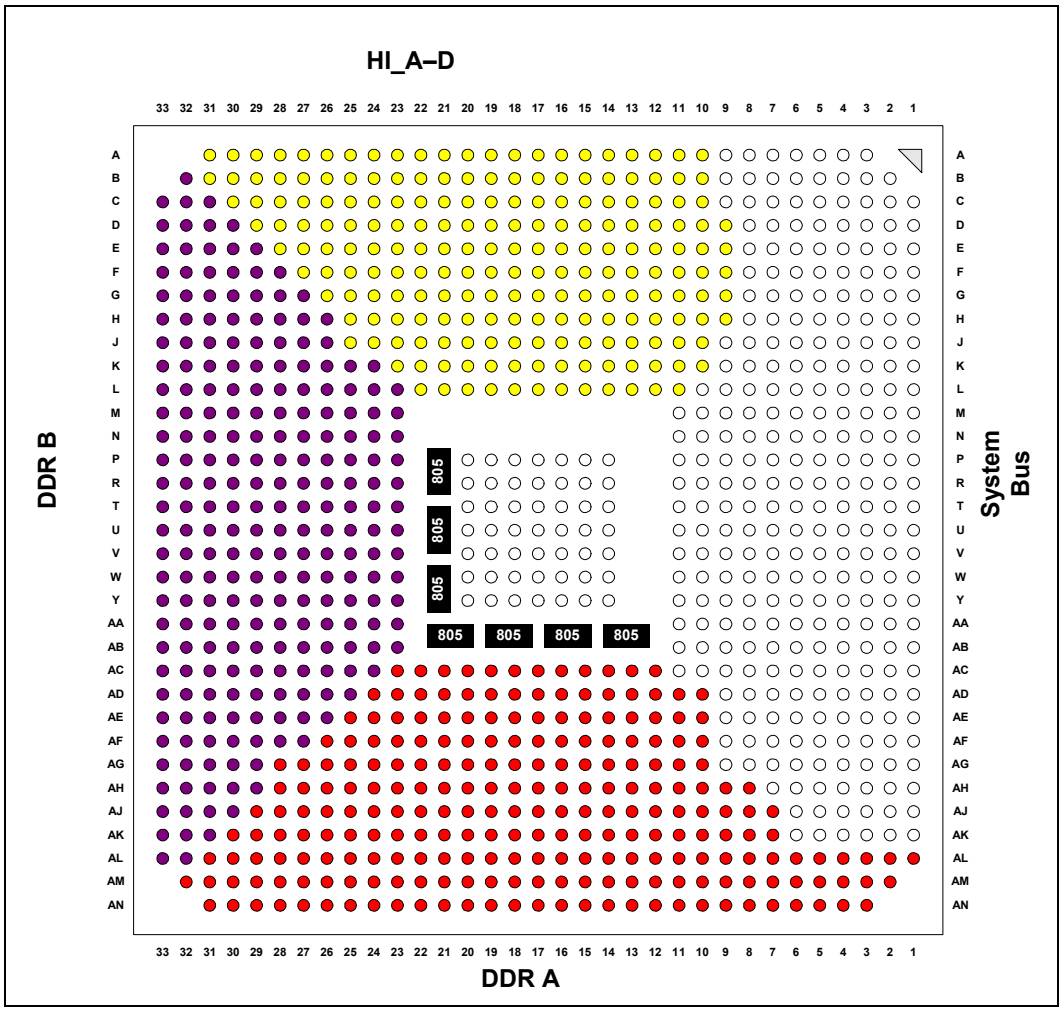
11.3.2 VCC_CPU (1.50 V Power Plane)

A maximum of five, 0.1 µF capacitors (minimum of four) are recommended (with 900 pH to 1.1 nH inductance) to be placed under the MCH for System Bus 1.50 V power plane decoupling. The designer should evenly distribute placement of decoupling capacitors among the System Bus interface signal field. In addition to the minimum decoupling capacitors under the MCH, the designer should place a maximum of nine, evenly-spaced capacitors for the System Bus, at least seven of which must be within 0.5 inch of the outer row of balls to the MCH.

11.3.3 DDR (2.5 V Power Plane)

A maximum of seven 0.1µF (minimum of five) capacitors are recommended (with 900 pH to 1.1 nH inductance) to be placed under the MCH for DDR 2.5 V power plane decoupling (see Figure 11-19). The designer should evenly distribute placement of decoupling capacitors among the DDR interface signal field. It is recommended that the designer use ceramic capacitor 0402 or 0805 body type. In addition to the minimum decoupling capacitors under the MCH, the designer should place a maximum of 15, evenly-spaced capacitors for both DDR channels, and at least 10 must be within 0.5 inch of the outer row of balls to the MCH.

Figure 11-19. MCH Decoupling (Backside View)



11.3.4 Hub Interface (1.2 V Power Plane)

A maximum of four, 0.1 µF capacitors should be used to improve I/O power delivery to the MCH. These capacitors should be placed within 150 mils of the MCH package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the ground side of the board should connect the VCC1_2 side of the capacitors to the VCC1_2 power pins. Similarly, if layout allows, metal fingers running on the VCC1_2 side of the board should connect the ground side of the capacitors to the VSS power pins.

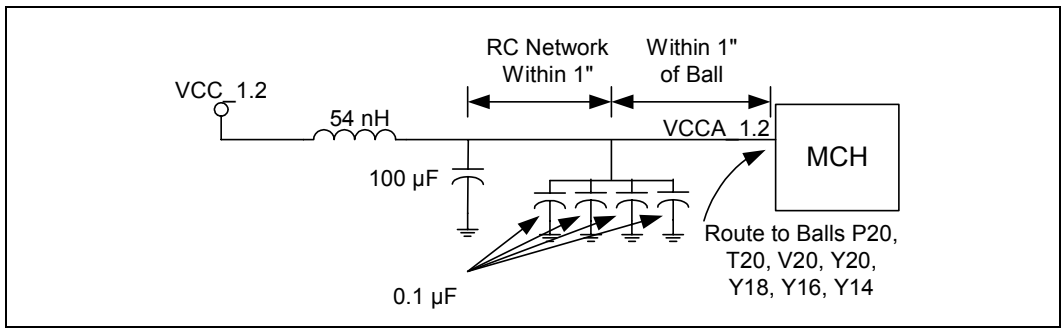
11.3.5 Filter Specifications (1.2 V Power Plane)

VCCA1_2 and VCCAHI1_2 are created by using a low pass filter on VCC1_2. VCCACPU is created by using a low pass filter on VCC_CPU. The MCH has internal analog PLL clock generators, that require quiet power supplies for minimum jitter. Jitter is detrimental to a system; it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency).

When designing the VCCA1_2 filter (Figure 11-20), follow these guidelines:

- One 54 nH Inductor close to the edge of the package (within 1 inch of the die).
- One 100 µF or 150 µF LF capacitor close to the edge of the package.
- Minimum of two (four preferred) Low ESL HF capacitors, 0.22 µF or 0.1 µF, on the backside of the motherboard under the die.
- Route the VCCA1_2 trace 1 inch, 35 mils wide with 15-mils spacing on three signal layers of the motherboard; connect to VCCA1_2 island on signal layers directly under the MCH core.

Figure 11-20. Filter Topology for VCCA1_2 (DDR Interface)



When designing the VCCA1_2 and VCCACPU filters (Figure 11-21 and Figure 11-22), follow these guidelines:

- One 100 nH Inductor close to the edge of the package (within 1 inch of the die).
- One 100 µF or 150 µF LF capacitor close to the edge of the package.
- Minimum of one Low ESL HF capacitor, 0.1 µF on the motherboard backside, under the die.

Figure 11-21. Filter Topology for VCCAHI1_2 (HUB Interface)

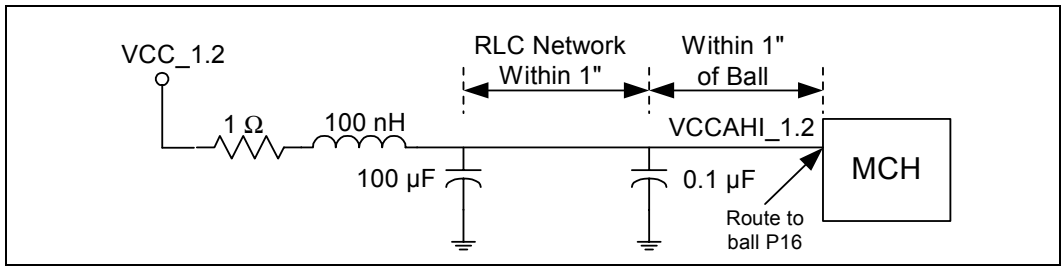
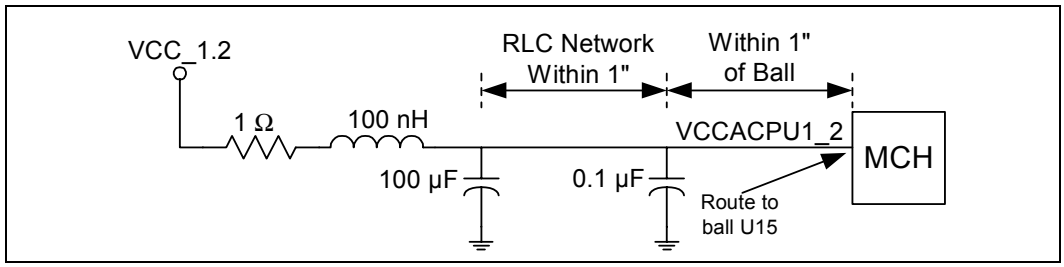


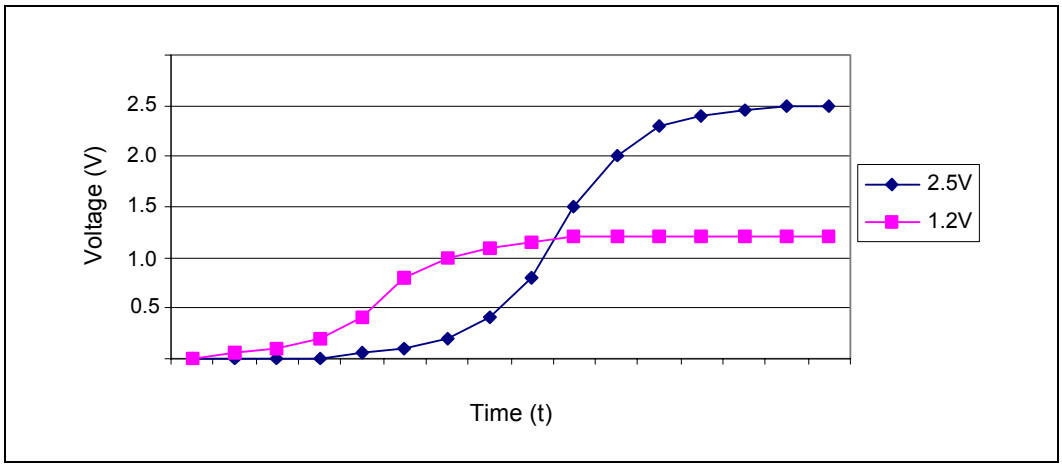
Figure 11-22. Filter Topology for VCCACPU_1.2 (System Bus)



11.3.6 MCH Power Sequencing Requirement

The MCH has only one power sequencing requirement. The MCH requires that 1.2 V rises with or before 2.5 V to avoid electrical overstress of oxide layers and possible component damage. This means that at any point during system power up, the 2.5 V power plane voltage must not be higher than the 1.2 V power plane voltage until the 1.2 V voltage is within 1.2 V regulation. This is depicted in Figure 11-23. Notice that at no point before 1.2 V is ramped does the 2.5 V plane exceed the 1.2 V plane's value.

Figure 11-23. Power Sequencing Requirement

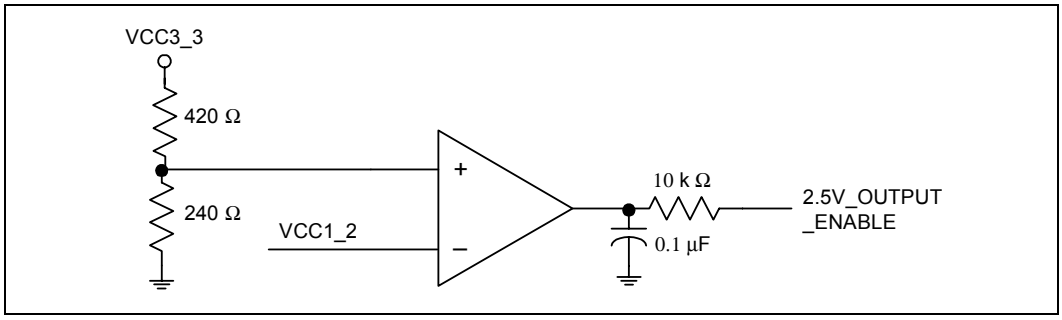


NOTE: This graph does not represent specific values or requirements on data/time frames.

A possible solution to safeguard against 2.5 V coming up before 1.2 V, is to tie the power good signal of the 1.2 V regulator to the output enable pin of the 2.5 V voltage regulator.

If the same voltage regulator is used to derive both 1.2 V and 2.5 V, then other logic must be used. A solution is to use a comparator to 1.2 V, and connect the output of the comparator to the output enable signal of the 2.5 V regulator. Figure 11-24 shows this implementation.

Figure 11-24. Sample 2.5 V Output Enable Control Logic



11.4 Intel® ICH3-S Power Delivery Guidelines

11.4.1 1.8 V/3.3 V Power Sequencing

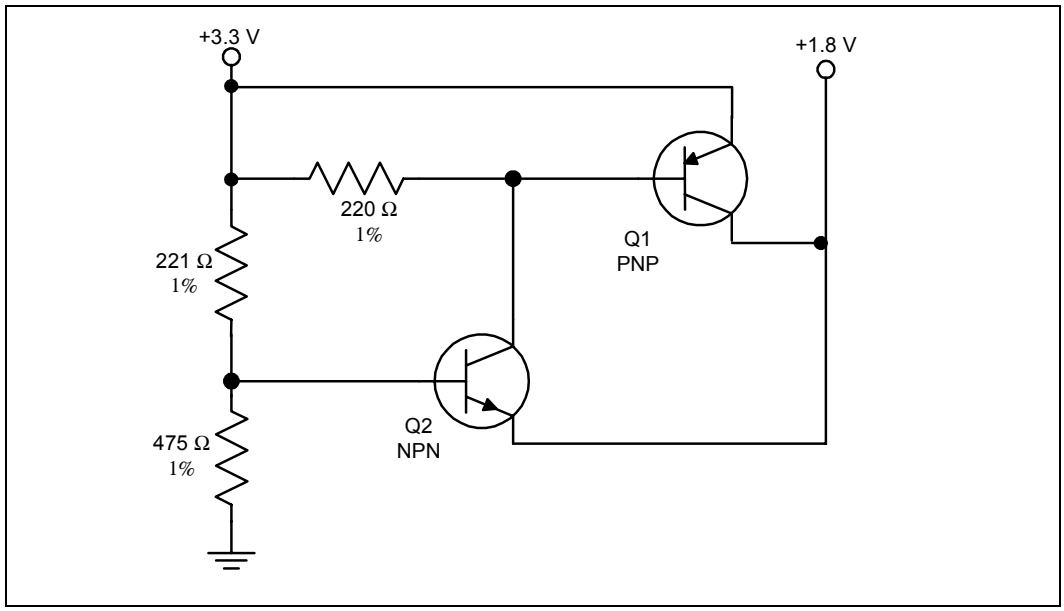
The ICH3-S has two pairs of associated 1.8 V and 3.3 V supplies. These are {VCC1_8, VCC3_3} and { VCCSus1_8, VCCSus3_3}. **The difference between the two associated supplies must never be greater than 2.0 V**. The 1.8 V supply may come up before the 3.3 V supply without violating this rule (though this generally does not occur because the 1.8 V supply is typically derived from the 3.3 V supply with a linear regulator). One serious consequence of violation of this "2 V Rule" is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH3-S I/O buffers are driven by the 3.3 V supplies but are controlled by logic powered by the 1.8 V supplies. Therefore, another consequence of faulty power sequencing arises if the 3.3 V supply comes up first. In this case, the I/O buffers will be in an undefined state until the 1.8 V logic is powered up. Some signals that are defined as "Input-only" actually have output buffers that are normally disabled, and the ICH3-S may unexpectedly drive these signals if the 3.3 V supply is active while the 1.8 V supply is not.

Note: These power sequencing circuits require that a linear regulator derive the ICH3-S 1.8 V power rail. These circuits are all designed with the assumption that 3.3 V is derived by the system power supply and that a 1.8 V linear regulator is used. Such circuitry is not needed if the voltage regulator guarantees the 2 V Rule.

Figure 11-25 is an example of power-on sequencing circuit using a Linear Regulator that ensures the 2 V Rule is obeyed. This circuit uses an NPN (Q2) and a PNP (Q1) transistor to ensure the 1.8 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.8 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8 V plane, current will not flow from the 3.3 V supply into 1.8 V plane when the 1.8 V plane reaches 1.8 V. It is important to use 1% resistors for precise operating conditions. When the NPN gets hot (junction temperature exceeds 125°C), it can overdrive the 1.8 V rail as high as 2 V.

Figure 11-25. Example 1.8 V/3.3 V Power Sequencing Circuit Using a Linear Regulator



When analyzing systems that may be “marginally compliant” to the 2 V Rule, attention must be paid to the behavior of the ICH3-S’s RSMRST# and PWROK signals because they control internal isolation logic between the various power planes:

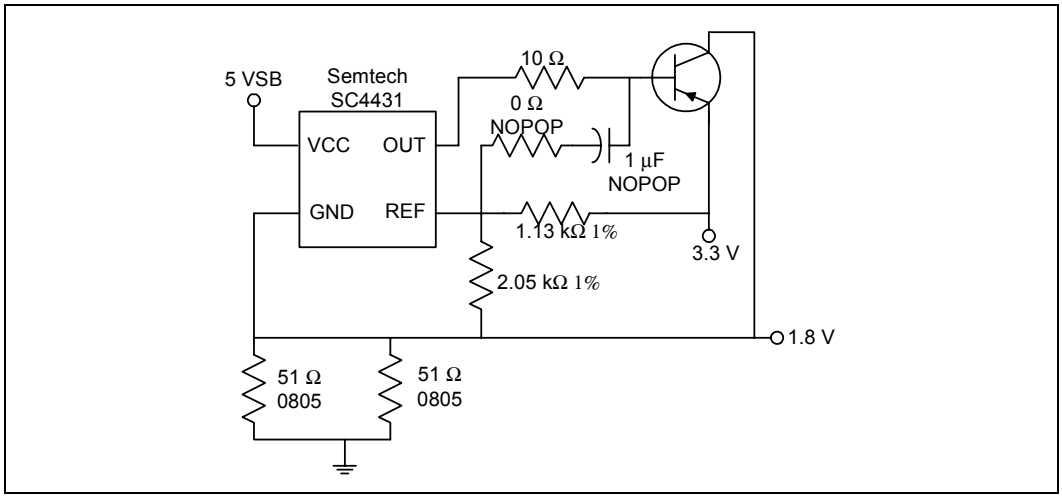
- RSMRST# controls isolation between the RTC well and the resume wells.
- PWROK controls isolation between the resume wells and main wells.

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

The circuit in Figure 11-26 may, under high temperature and parameter corner conditions, inject charge onto the 1.8 V rail at steady state. The circuit in Figure 11-25 does not have this characteristic; however, it is more susceptible to layout variations and should be fully analyzed and tested to make sure that the implementation meets the 2 V specification. When choosing between the two circuits a designer should understand the trade-offs with respect to their linear regulator design and application.

The Semtech SC4431 monitors the difference between the reference pin (from 3.3 V) and the ground pin (1.8 V). The SC4431 turns on its output when the difference between 1.8 V and 3.3 V is over 1.9 V. Connecting the SC4431 ground pin to 1.8 V requires a series resistor from 1.8 V to ground to complete the current path from the SC4431 VCC (5 VSB) to system ground. The series resistor must be able to dissipate 0.25 W. This can be achieved using a 25 Ω resistor in a 1206 package, or two 51 Ω resistors in 0805 packages. The 1.8 V rail should be able to sink the current from the SC4431 and the 1.13 kΩ / 2.05 kΩ divider.

Figure 11-26. Another Example 1.8 V/3.3 V Power Sequencing Circuit



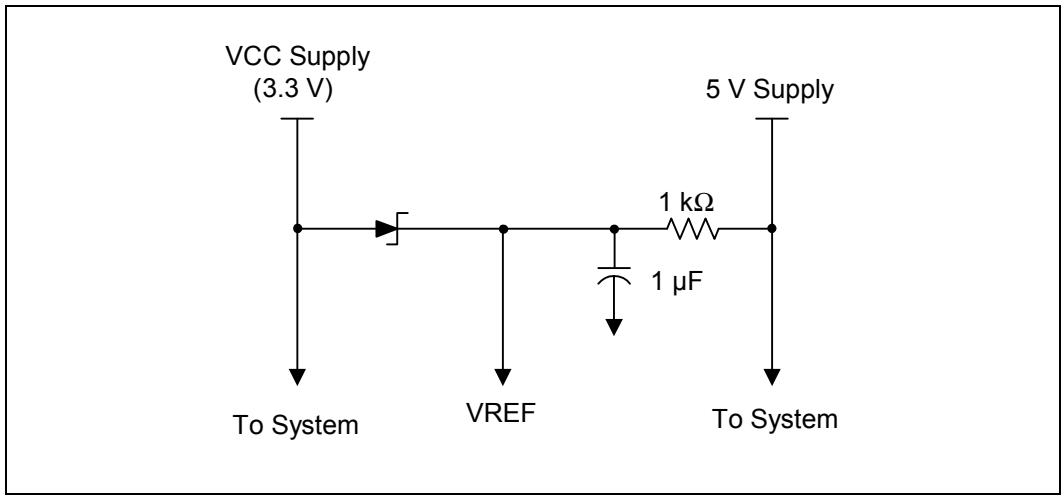
NOTE: This circuit has not yet been validated. Resistor values are subject to change.

11.4.2 3.3 V/V5REF Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH3-S. V5REF must be powered up before VCC3_3, or be no less than 0.7 V less than VCC3_3. Thus, VCC3_3 must never be more than 0.7 V higher than V5REF. Also, V5REF must power down after VCC3_3, or before VCC3_3 within 0.7 V. The rule must be followed in order to ensure the safety of the ICH3-S. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 11-27 shows a sample implementation of how to satisfy the V5REF/ 3.3 V sequencing rule.

This rule also applies to the standby rails, but in most platforms, the VCCSus3_3 rail is derived from the VCCSus5 rail and therefore, the VCCSus3_3 rail will always come up after the VCCSus5 rail. As a result, V5REF_SUS will always be powered up before VCCSus3_3. In platforms that do not derive the VCCSus3_3 rail from the VCCSus5 rail, this rule must be enforced on the platform.

Figure 11-27. Example 3.3 V/V5REF Sequencing Circuitry



11.4.3 Intel® ICH3-S Power Rails

The ICH3-S refers to its standby rails as suspend. Table 11-7 lists the nomenclature.

Table 11-7. Intel® ICH3-S Power Rail Terminology

Platform Terminology	Intel® ICH3-S Terminology
5 V Standby	5 V Suspend
3.3 V Standby	3.3 V Suspend
1.8 V Standby	1.8 V Suspend

11.4.4 Intel® ICH3-S Decoupling Recommendations

The ICH3-S is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the decoupling capacitors specified in Table 11-8 to ensure that the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (200 mils nominal). It is recommended that for prototype board designs, the designer include pads for extra power plane decoupling capacitors.

Table 11-8. Intel® ICH3-S Decoupling Recommendations

Power	Decoupling Requirements	Decoupling Placement
V_CPU_IO	Use one 0.1 µF decoupling capacitor.	• Locate within 100 mils of the Intel® ICH3-S processor interface balls.
VCCRTC	Use one 1.0 µF decoupling capacitor. See Figure 9-11 for the External Circuitry.	• Locate within 100 mils of the VCCRTC interface ball (ball AB6).
VCC3_3	Requires six 0.1 µF decoupling capacitors.	• Distribute around the ICH3-S package sides within 100 mils of the package balls: – Top near AUX/PCI – Left across the PCI and LPC – Bottom near IDE – Right near GPIO[43]
VCCSus3_3	Requires two 0.1 µF decoupling capacitors.	• Place one capacitor on the top side within 200 mils of the USB center. • Place one capacitor on the bottom side near the VCCSus3_3 supply.
VCC1_8	Requires four 0.1 µF decoupling capacitors.	• Locate 2 capacitors distributed local to the hub interface, within 50 mils of the package HI balls. • Distribute the remaining capacitors on the left and bottom sides of the package for core delivery.
VCCSus1_8	Requires one 0.1 µF decoupling capacitor.	• Locate within 200 mils of the ICH3-S, Balls B23 and C23.
5VREF_SUS	Requires one 0.1 µF decoupling capacitor. V5REF_SUS is the reference voltage for some 5 V tolerant inputs in the ICH3-S (USB data and over current signals). VCCSus3_3 must never exceed 0.7 V higher than V5REF_SUS. For most platforms, this power sequencing is not an issue as VCCSus3_3 is derived from 5VREF_SUS.	
V5REF	Requires one 0.1 µF decoupling capacitor. V5REF is the reference voltage for most 5 V tolerant inputs in the ICH3-S. Tie to pins V5REF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.	

11.5 Intel® P64H2 Power Requirements

11.5.1 Intel® P64H2 Current Requirements

Table 11-9. Intel® P64H2 Max Sustained Currents

Voltage at PCI/PCI-X Interface	Max Sustained Current
1.8 V at 33 MHz PCI (both segments)	1970 mA
1.8 V at 66 MHz PCI/PCI-X (both segments)	2170 mA
1.8 V at 100 MHz PCI-X (both segments)	2550 mA
1.8 V at 133 MHz PCI-X (both segments)	2660 mA
3.3 V at 33 MHz PCI 6 loads (both segments)	930 mA
3.3 V at 66 MHz PCI 2 loads (both segments)	690 mA
3.3 V at 66 MHz PCI-X 4 loads (both segments)	1300 mA
3.3 V at 100 MHz PCI-X 2 loads (both segments)	1050 mA
3.3 V at 133 MHz PCI-X 1 load (both segments)	770 mA

For more information, refer to the *Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Thermal Design Guide*.

11.5.2 Intel® P64H2 Decoupling Requirements

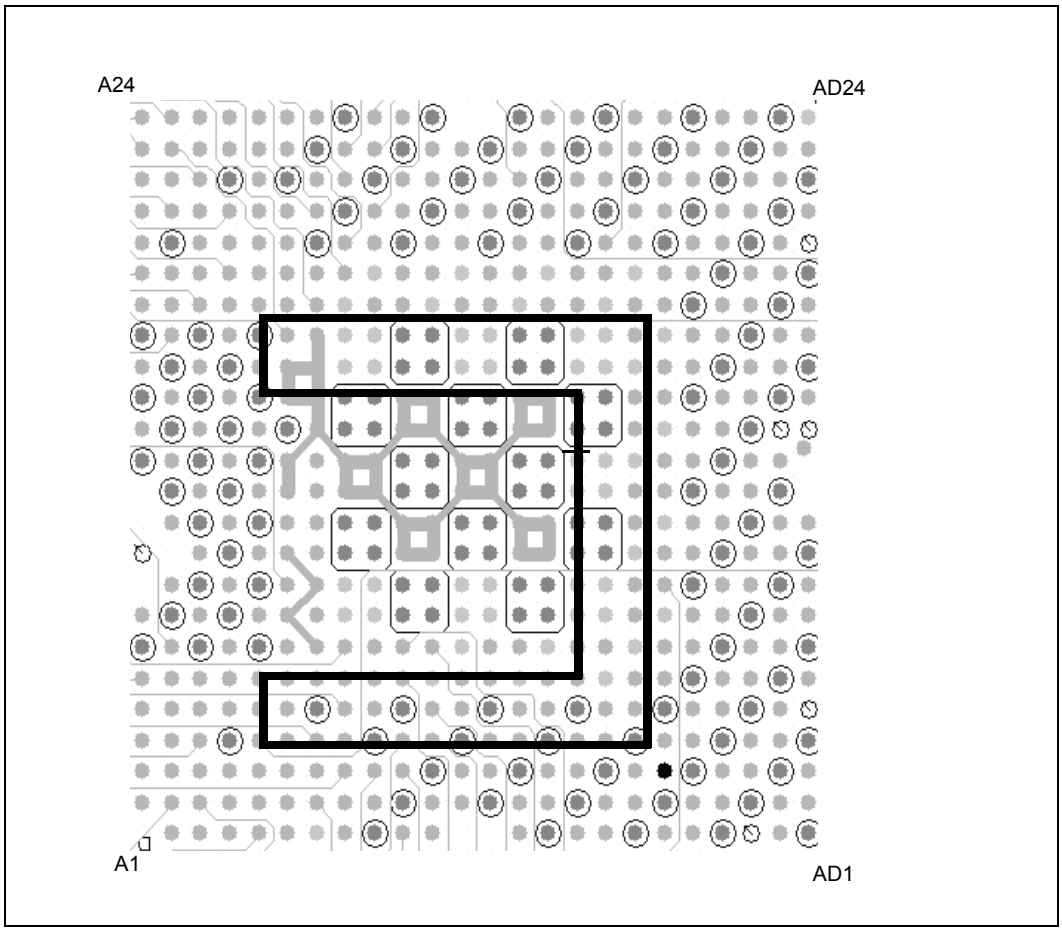
The P64H2 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in the table below to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible.

Table 11-10. Decoupling Capacitor Recommendations

Power Plane/Pins	Number of High-Frequency Decoupling Capacitors	High-Frequency Capacitor Values	Number of Bulk Decoupling Capacitors	Bulk Capacitor Values
1.8 V Core (VCC)	8	0.1 µF	2	4 µF (near Intel® P64H2)
1.8 V HI 2.0 (VCC1_8)	2	1.0 µF	1	100 µF (near regulator)
3.3 V PCI/PCI-X (VCC3_3)	20[1]	0.1 µF	2	4 µF (near P64H2)
	6	1.0 µF	1	100 µF (near regulator)

NOTES:
1. In the case of the 20 0.1 µF decoupling capacitors for the Vcc3.3 plane, it is recommended that at least five of these capacitors be placed near the die on the back of the board between ground and the VCC-PCI vias, as shown in Figure 11-28. This is not a strict requirement, but is recommended to reduce the power resonance frequency at 66 Hz.

Figure 11-28. 3.3V PCI/PCI-X (VCC3_3) Capacitor Placement on Backside



NOTE: The outlined area in the figure is the 3.3 V plane. Place at least five 0.1 µF capacitors in this area.

11.5.3 PCIRST# Implementation

PCI-X requires a 100 ms delay from valid power (PWRGD) to reset deassertion (PCIRST#). The system design must ensure this requirement is met.

The P64H2 reset must be deasserted within 60 ns of the MCH reset deassertion. Intel strongly recommends customers measure this timing relationship on their boards. Failure to meet this guideline may result in a system failing to boot.

11.5.4 Intel® P64H2 Power Sequencing Requirement

The 1.8 V voltage must be valid before the first CLK66 pulse is driven to the P64H2. This can be guaranteed by gating the CK408 clocks using a power good signal from the 1.8 V regulator. When the first CLK66 pulse is driven before 1.8 V is valid, the P64H2 PLL may fail to correctly lock.

The 1.8 V must drop with or before 3.3 V. This can be achieved by deriving 1.8 V from 3.3 V. When 1.8 V drops after 3.3 V, a noise spike on PCIRST# approaches V_{IH} minimum levels.

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12.1 Return Path

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, or integrated circuits. The return path is based on electro-magnetic field effects. It is useful to think of the return path as the path of least impedance nearest the signal conductor. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths must be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance.

The following sets of return path rules apply to all designs:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near system bus signals.
- Do not allow signal layer changes that force the return path to make a reference plane change, even if it is from one ground layer to another ground layer.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not route over via anti-pads or socket anti-pads

If reference plane changes must be made:

- Change from a ground reference to a ground reference and place a via that connects the two planes as close as possible to the signal via. This also applies when making a change from VCC to VCC.
- For symmetric stripline, return path vias for both ground and VCC must be provided.
- Do not switch reference from VCC to ground or vice versa.

12.2 Decoupling Theory

The primary objective of the decoupling guidelines is to minimize the impact of return path discontinuities and to ensure that the I/O has adequate power decoupling. The worst-case return path discontinuity anticipated is for systems that use microstrip structures on the motherboard. If a motherboard uses symmetric stripline with VCC and ground references, then a discontinuity does not exist and additional decoupling is not necessary. If the motherboard routing references only a single reference plane (VCC or ground), then a return path discontinuity exists.

The inductance of the system due to cables and power planes slows the power supply's ability to respond quickly to a current transient. Decoupling a power plane can be broken into several independent parts. The closer to the load the capacitor is placed, the more inductance is bypassed. By bypassing the inductance of leads, power planes etc., less capacitance is required. However, closer to the load there is less room for capacitance. Therefore, trade-offs must be made.

12.2.1 Bulk Decoupling

Larger bulk storage components, such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition.

Power bypassing is required due to the relatively slow speed at which a DC-to-DC converter can react. Bulk capacitance supplies energy from the time the high-frequency decoupling capacitors are drained, until the power supply can react to the demand. More correctly, the bulk capacitors in the system slow the transient requirement seen by the power source to a rate it is able to supply, while the high-frequency capacitors slow the transient requirement seen by the bulk capacitors to a rate they can supply.

Maintaining voltage tolerance during changes in current requires high-density bulk capacitors with low Effective Series Resistance (ESR), and low Effective Series Inductance (ESL). Use thorough analysis when choosing these components.

12.2.2 High-Frequency Decoupling

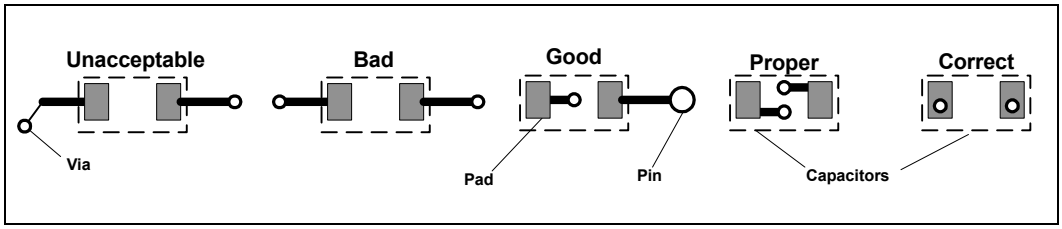
The system boards should include high-frequency capacitors as close to the load power and ground pins as possible. Place as many capacitors as possible in the load cut out area.

In addition, high-frequency decoupling may be required for signal integrity. For systems using microstrip configurations, a return path discontinuity will exist due to the baseboard traces having only one reference plane.

Place high-frequency decoupling as close to the power pins of the load as physically possible. Use both sides of the board if necessary for placing load to achieve the optimum proximity to the power pins. This is vital because the inductance of the board's metal plane layers could cancel the usefulness of these low inductance components.

Shorten the path from the capacitor pads to the pins the capacitor is decoupling. If possible, place the vias connecting to the planes within the pad of the capacitor. If this is not possible, keep the traces as short and wide as is feasible. Possibly one or both ends of the capacitor can be connected directly to the pins of the load without the use of a via. Figure 12-1 illustrates these concepts.

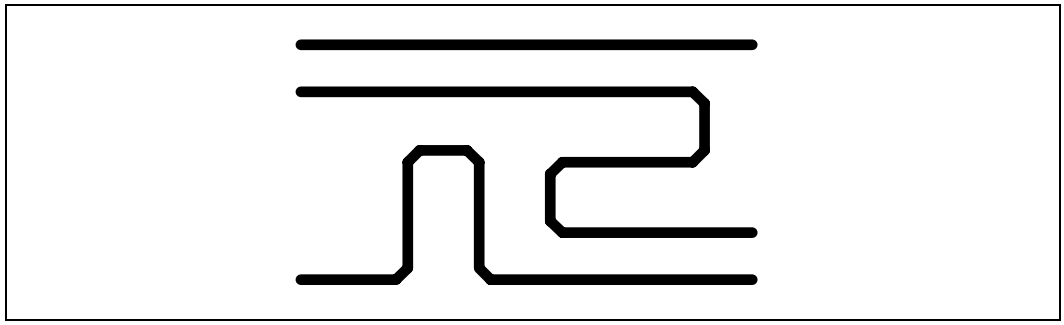
Figure 12-1. Proper Decoupling Capacitor Placement with Respect to Vias



12.3 Serpentine Routing

A serpentine net is a transmission line that is routed in such a manner that sections of the net double back and couple to other segments of the same net.

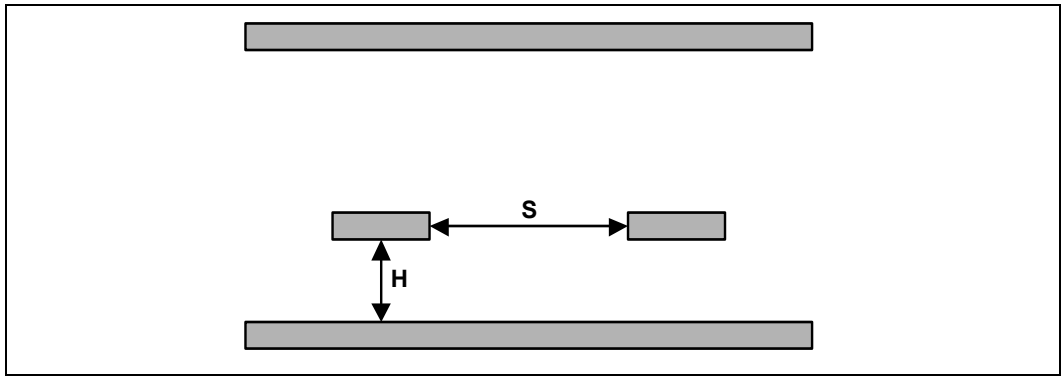
Figure 12-2. Serpentine Routing



Serpentining a transmission line is sometimes necessary to properly match lengths between nets. It is important to properly control the serpentine to avoid signal integrity and timing problems. The primary impact of a serpentined trace is an observed decrease in the flight time when compared to a straight trace of equal length. This decrease in the flight time is a result of the crosstalk between parallel sections of the serpentined net. As the signal travels down the transmission line, a component of the signal follows the transmission line and behaves as though it were a straight line with no serpentine. However, another portion of the energy propagates perpendicular to the parallel routed portions of the serpentined net via the mutual capacitance and mutual inductance. This creates an extra mode that arrives at the receiver significantly earlier than the other component of the signal. If the coupling between parallel sections is high, significant timing skew can occur when attempting to match trace lengths on a bus. Furthermore, if the coupling is very high, significant signal integrity problems can result.

Serpentine routing requirements are defined using two parameters, as depicted in Figure 12-3. Parameter ‘S’ is the distance between the two segments of the serpentined trace. Parameter ‘H’ is the distance between the signal and the referenced plane. The ratio is specified as S/H.

Figure 12-3. Serpentine Spacing - Spacing to Reference Plane Height Ratio



12.4 EMI Design Considerations

As microprocessor amperage and speeds increase, the ability to contain the corresponding electromagnetic radiation becomes more difficult. Frequencies generated by these processors will be in the low gigahertz (GHz) range, which will impact both the system design and the electromagnetic interference (EMI) test methodology.

This section is intended to provide electrical and mechanical design engineers with information that will aid in developing a platform that will meet government EMI regulations. Heatsink grounding, processor shielding, differential and spread spectrum clocking, and the test methodology impact to FCC Class B requirements are specifically discussed.

Designers should be aware that implementing all the recommendations in this guideline will not guarantee compliance to EMI regulations. Rather, these guidelines may help to reduce the emissions from processors and motherboards and make chassis design easier.

12.4.1 Brief EMI Theory

Electromagnetic energy transfer can be viewed in four ways: radiated emissions, radiated susceptibility, conducted emissions, and conducted susceptibility. For system designers, reduction of radiated and conducted emissions is the way to achieve EMC compliance. Susceptibility is typically not a major concern in the server environment, although it may be more important in an industrial environment.

The main component of EMI is a radiated electromagnetic wave, which consists of both electric (E-fields), and magnetic (H-fields) waves traveling together and oriented perpendicular to one another. Although E- and H-fields are intimately tied together, they are generated by different sources. E-fields are created by voltage potentials, while H-fields are created by current flow. In a steady state environment (where voltage or current is unchanging), E- and H-fields are also static and of no concern to EMI. Changing voltages and currents are of concern since they contribute to EMI. If a dynamic E-field is present, then there must be a corresponding dynamic H-field, and vice versa. Motherboards with fast processors generate high-frequency E- and H-fields from currents and voltages present in the component silicon and signal traces.

Two methods exist for minimizing E- and H-field system emissions: prevention, and containment. Prevention is achieved by implementing design techniques that minimize the ability of the motherboard to generate EMI fields. Containment is used in a chassis environment to contain radiated energy within the chassis. Careful consideration of board layout, trace routing, and grounding may significantly reduce a motherboard's radiated emissions and make the chassis design easier.

12.4.2 EMI Regulations and Certifications

Original Equipment Manufacturers (OEMs) ensure EMC compliance by meeting EMI regulatory requirements. System designers must ensure that their computer systems do not exceed the emission limit standards set by applicable regulatory agencies. Regulatory requirements referenced in this document include:

- United States Federal Communication Commission (FCC) Part 15 Class B.
- International Electrotechnical Commission's International Special Committee on Radio Interference (CISPR) Publication 22 Class B limits.

The FCC rules require any OEM that sells an "off-the-shelf" motherboard in the United States to pass an open chassis test. Open chassis testing is defined as removing the chassis cover (or top and two sides), and testing for EMI compliance (although permitted emission levels are allowed to be higher). Removing the cover greatly reduces the shielding provided by the chassis and increases the amount of EMI radiation. The purpose of this regulation is to ensure that system boards have reasonable emission levels since they are one of the main contributors to EMI.

12.4.3 Spread Spectrum Clocking (SSC)

Spread Spectrum Clocking is defined as continuously ramping (or modulating) the processor clock frequency over a predefined range (see Figure 12-4). SSC reduces radiated emissions by spreading the radiated energy over a wider frequency band (see Figure 12-5). Thus, instead of maintaining a constant system frequency, SSC modulates the clock frequency along a predetermined path (or modulating profile). Figure 12-4 shows an example of a predetermined modulation frequency. The modulation frequency is usually selected to be larger than 30 kHz (above the audio band), and small enough not to upset system timings (less than 0.8% of the clock frequency). SSC has been demonstrated to effectively reduce peak radiation levels, making EMC compliance easier to achieve.

To conserve the minimum period requirement for bus timing, the SSC clock is modulated between fnom and (1-δ)*fnom, where fnom is the nominal frequency for a constant frequency clock. The"δ" specifies the total amount of spreading as a relative percentage of fnom. The modulation percentage is always a function of 1-δ and not 1+δ, as increasing the clock frequency above the rated speed of the processor may cause unpredictable operation.

Figure 12-4. Spread Spectrum Modulation Profile

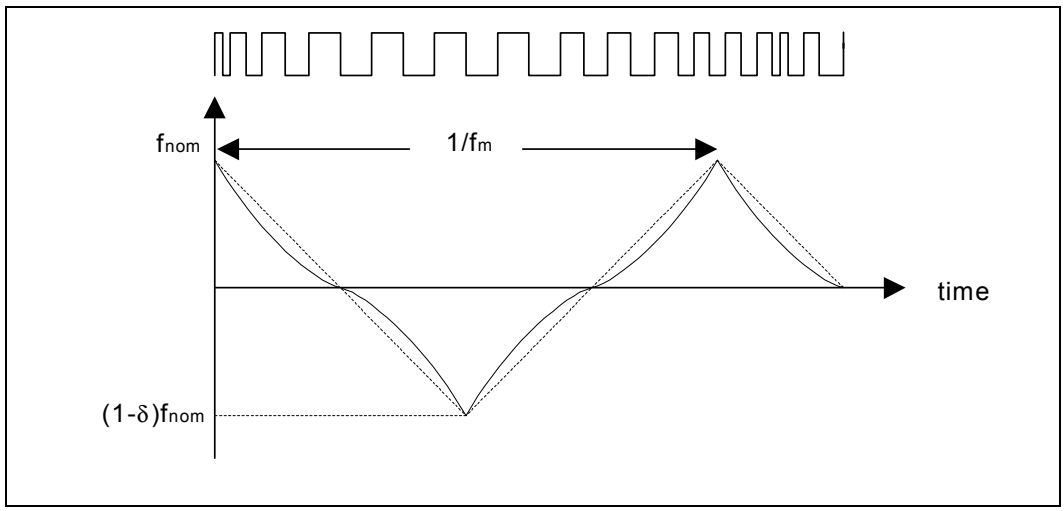
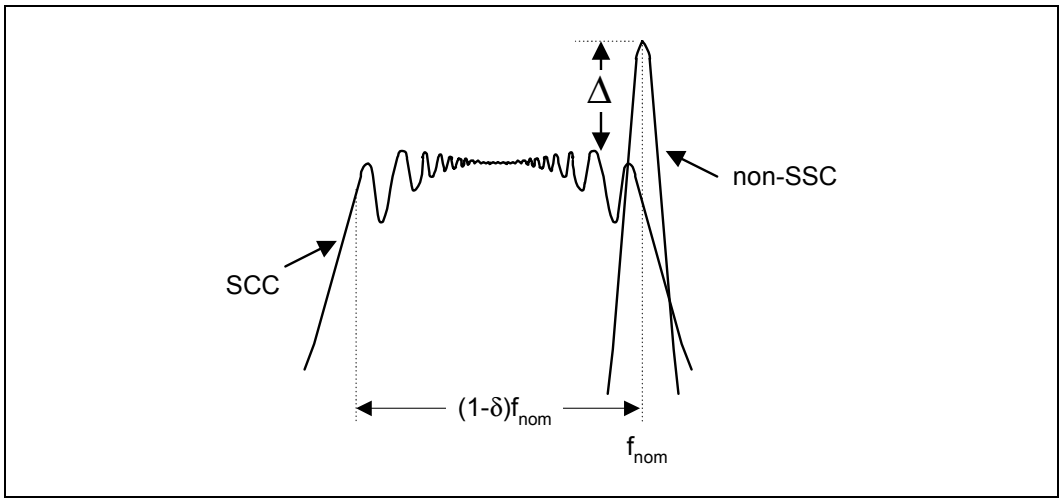


Figure 12-5. Impact of Spread Spectrum Clocking on Radiated Emissions

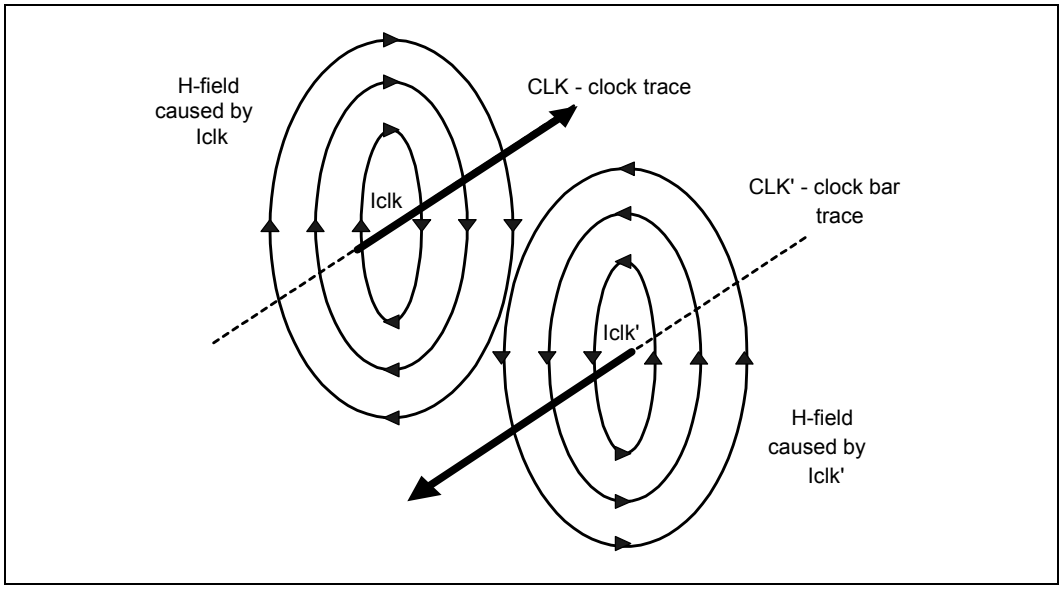


12.4.4 Differential Clocking

Differential clocking requires that the clock generator supply both clock and clock-bar traces. Clock-bar has equal and opposite current as the primary clock, and is also 180 degrees out of phase. To maximize the benefit of differential clocking, both clock lines must be routed parallel to each other for their entire length. Devices connected to the clock must also be designed to accept both the clock and clock-bar signals.

EMI reduction due to differential clocking is caused by H-field cancellation. Since H-field orientation is generated by and is dependent upon current flow, two equal currents flowing in opposite directions and 180 degrees out of phase will have their H-fields cancelled (see Figure 12-6). Lower H-fields will result in reduced EMI radiation.

Figure 12-6. Cancellation of H-fields through Inverse Currents



Differential clocking can also reduce the amount of noise coupled to other traces, which improves signal quality and reduces EMI. I/O signals are particularly important because they often leave the system chassis (serial and parallel ports, keyboards, mouse, etc.), and radiate noise that has been induced onto them. A single-ended clock's return path is usually a reference plane, which is shared by other signals/traces. When noise is created on a single-ended clock, the noise will appear on the reference plane and may be coupled to I/O traces. A differential clock's return path is the clock-bar signal/trace, which is more isolated than the reference plane and minimizes potential I/O trace coupling.

For best results, the trace lengths and routing of the clock lines must be closely matched, and spacing between the two traces should be kept as small as possible. This minimizes loop area and maximizes H-field cancellation. In addition, the real and parasitic terminations of each signal of a differential pair should be the same. Also, the skew between the signal level transitions on the two lines must be small compared to the rise time of the level transitions.

Placing ground traces on the outside of the differential pair may further reduce emissions. Intermediate vias to ground may be needed to reduce the opportunity for re-radiation from the ground traces themselves. Distance between vias should be less than ¼ of a wavelength of the fifth harmonic of the processor core frequency.

12.4.5 PCI Bus Clock Control

Experimental data has indicated a reduction in EMI may be possible by disabling the clocks to unused (and therefore unterminated) PCI slots. CK408B, the clock chip that has been specified and designed for this platform, supports individual control of the various PCI clocks. Designers have the option to enable or disable individual PCI clocks depending upon their specific system configuration requirements. Refer to the *CK408B Clock Synthesizer Design Guidelines* for details on how to configure the PCI clocks.

12.4.6 EMI Test Capabilities

FCC regulations in the United States specify the maximum test frequency for products with clocks in excess of 1 GHz is five times the highest clock frequency or 40 GHz, which ever is lower. OEMs are advised to inquire into the capabilities of their preferred EMC test lab to ensure they are able to scan up to the required frequency range.

Processor performance and frequency double approximately every two years. With this in mind, it is advisable to be prepared for the frequencies that will need to be scanned in the next few years.

Since the FCC rules ultimately require testing to 40 GHz, commercial test equipment has been developed that is capable of making measurements to that frequency. Although it will be some time before processors require testing at this frequency, it may be cheaper to upgrade to 40 GHz now, rather than making several intermediate steps.

It is also possible to upgrade various parts at different times. The spectrum analyzer may be upgraded to 40 GHz today with only the necessary antennas to support the initial processor frequencies. As processor speed increases, the necessary antennas and cables can be purchased that support testing to the higher levels.

12.5 Length Tuning

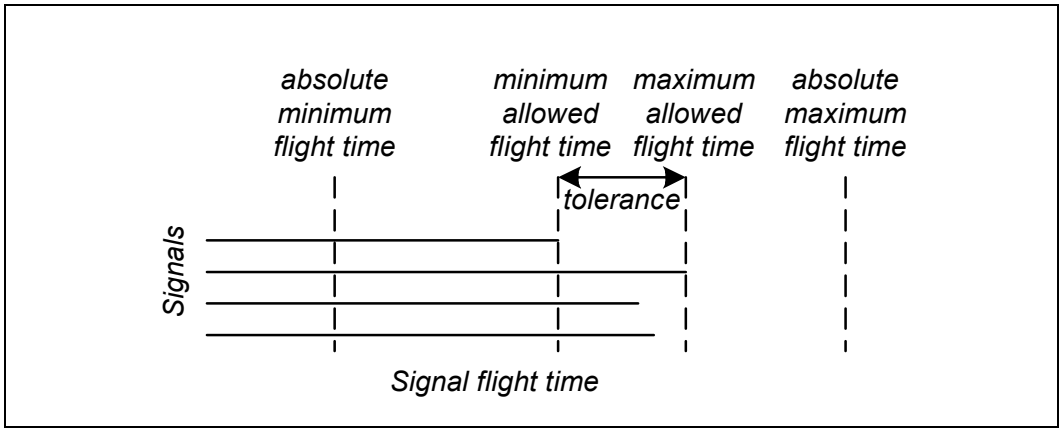
Note: This section does not apply to the Processor System Bus.

High speed source synchronous interfaces have very small setup and hold window.s As a result, the signals as a group are very sensitive to skew. A common way to reduce skew is to tune all of the lengths such that the setup and hold windows have the same positional relationship. Length tuning is the matching of two or more signals' total flight time, within a tolerance, to center the setup and hold windows.

Length tuning has several key parameters: signal to be tuned, absolute minimum flight time, absolute maximum flight time, and tolerance. The absolute minimum and maximum flight times define the flexible solution space which lengths may fall within. For a signal to be properly tuned, it must fall within that solution space **and** be within the length tuning tolerance. Figure 12-7 shows the relationship of these parameters.

A tolerance is a value specifying how far off from exact is allowed. Typically, tolerance is specified in a specific direction, such as –1 ps or ± 2 ps. In the first instance, the total tolerance window or solution space is 1 ps; the second the solution space is 4 ps.

Figure 12-7. Length Tuning Parameters



The minimum and maximum allowed flight times are at the end points of the tolerance window. The tolerance window may fall anywhere within the range between absolute minimum flight time and maximum flight time. The remainder of this section will simply refer to "minimum allowed flight time" as "minimum flight time" and will refer to "maximum allowed flight time" as "maximum flight time."

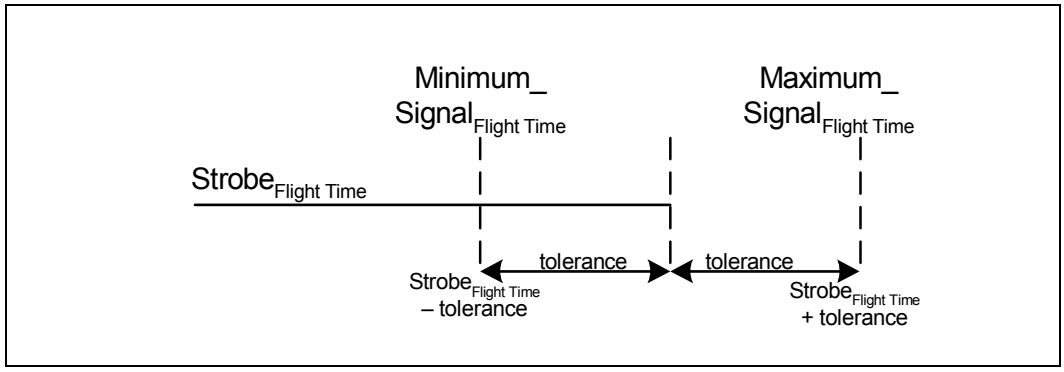
12.5.1 Signal to Strobe Flight Time Relationships

High speed interfaces are commonly latched off of a strobe or a clock. Length tuning ensures that the required setup and hold times of the data signal to the strobe signal or clock signal are not violated due to motherboard routing effects. As a result, each data signal is length tuned with respect to the strobe signal or clock signal. This means that the data signals are all within tolerance of the strobe signal:

$$Minimum\_Signal_{Flight\ Time} = Strobe_{Flight\ Time} - Tolerance$$

$$Maximum\_Signal_{Flight\ Time} = Strobe_{flight\ Time} + Tolerance$$

Figure 12-8. Signal Length Solution Space with One Strobe

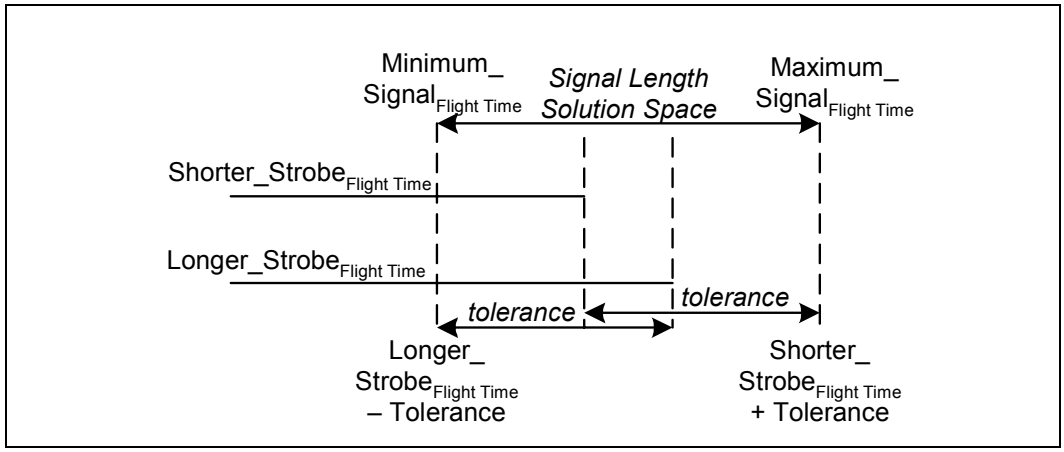


Some groups of high speed signals need to be length tuned to **two** strobes or clocks. In this situation, all signals must be length matched to **both** strobes or clocks and the strobes or clocks must be length matched to each other as well.

$$Minimum\_Signal_{Flight\ Time} = Longer\_Strobe_{Flight\ Time} - Tolerance$$

$$Maximum\_Signal_{Flight\ Time} = Shorter\_Strobe_{Flight\ Time} + Tolerance$$

Figure 12-9. Signal Length Solution Space with Two Strobes

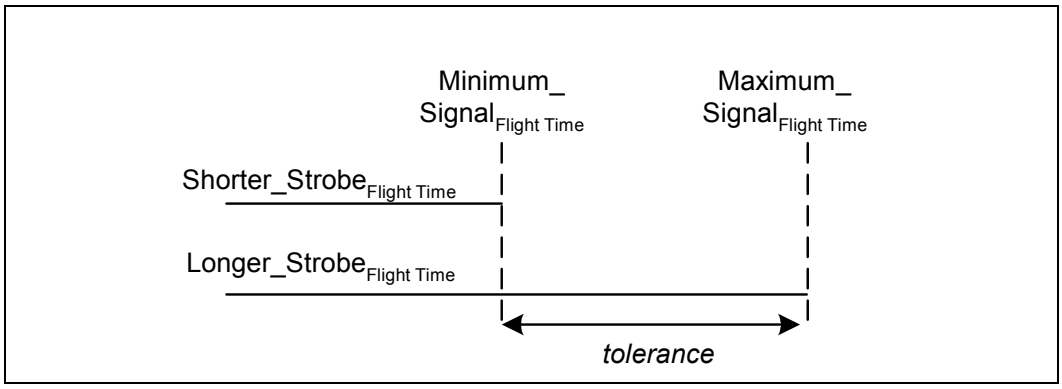


If the strobes are the furthest apart (i.e., as far apart as allowed for signals of the same group), then their difference is the total allowed tolerance. This means that all signals must fall between them, or have a solution space which is "tolerance" wide.

$$Longer\_Strobe_{Flight\ Time} = Shorter\_Strobe_{Flight\ Time} + Tolerance$$

$$Shorter\_Strobe_{Flight\ Time} = Longer\_Strobe_{Flight\ Time} - Tolerance$$

Figure 12-10. Signal Length Solution Space with Maximum Tolerance Strobes



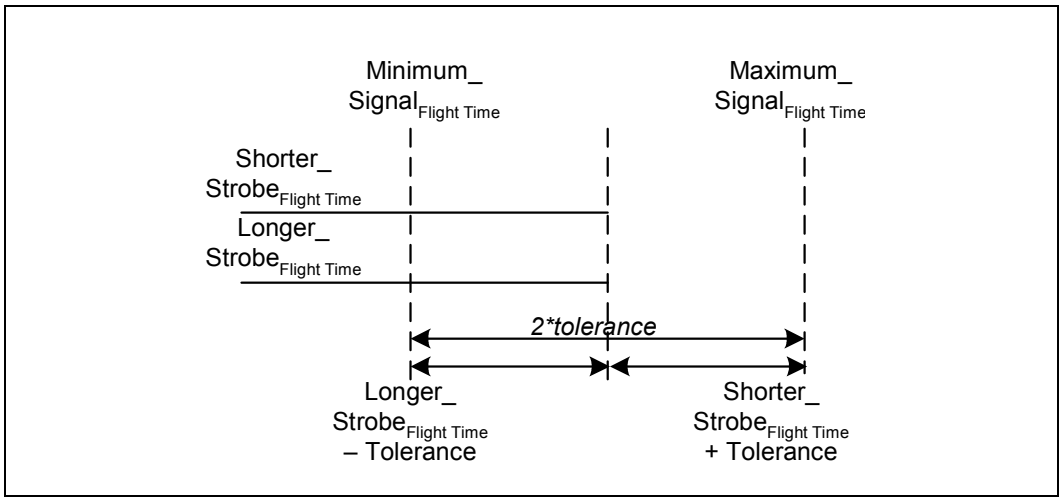
If the strobes have exactly the same flight time, then the signals have a solution space which is "2*tolerance" wide.

$$Strobe_{Flight\ Time} = Longer\_Strobe_{Flight\ Time} = Shorter\_Strobe_{Flight\ Time}$$

$$Minimum\_Signal_{Flight\ Time} = Strobe_{Flight\ Time} - Tolerance$$

$$Maximum\_Signal_{Flight\ Time} = Strobe_{Flight\ Time} + Tolerance$$

Figure 12-11. Signal Length Solution Space with Matched Strobes



12.5.2 Flight Time Segment Analysis

Length matching often requires package compensation. Every time a signal changes innerconnect or layer, there is an affect on flight time. The most effective way to calculate flight time is to break up each signal into segments of “constant” flight time, analyze those segments, and then add the segments together.

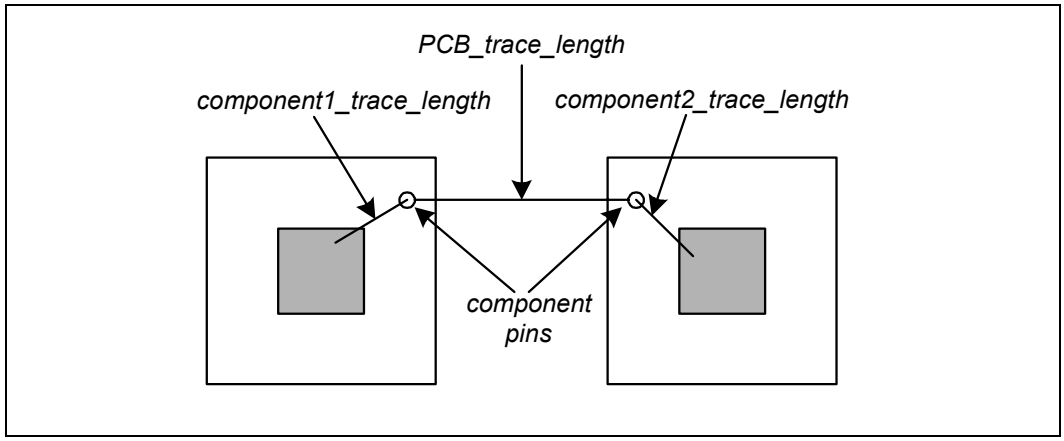
Flight time is directly proportional to trace length by a constant trace velocity:

Flight Time = Trace_Length / Trace_Velocity

To determine the total flight time, each segment with a constant trace velocity must be identified. These segments are commonly defined at component interconnects. For example, a signal which connects two different components via a PCB would be calculated as follows:

$$Total\_Signal_{Flight\ Time} = Signal_{Componet1\ Flight\ Time} + Signal_{PCB\ Flight\ Time} + Signal_{Component2\ Flight\ Time}$$

Figure 12-12. Total Signal Length with Two Components



Using the segment lengths and velocities yields:

Equation 12-1. Total Flight Time Equation

$$total\_flight\_time = \frac{component1\_length}{component1\_velocity} + \frac{PCB\_length}{PCB\_velocity} + \frac{component2\_length}{component2\_velocity}$$

12.5.3 Length Tuning Equation Derivation

When routing a motherboard, only one piece of the equation is a variable: **PCB trace length**. For example, if signals are tuned with respect to the strobe, the final equation used by a motherboard designer is derived as follows. First, two equations are defined:

$$\text{Total\_Strobe}_{\text{Flight Time}} = \text{Strobe}_{\text{Component1 Flight Time}} + \text{Strobe}_{\text{PCB Flight Time}} + \text{Strobe}_{\text{Component2 Flight Time}}$$

$$\text{Total\_Signal}_{\text{Flight Time}} = \text{Signal}_{\text{Component1 Flight Time}} + \text{Signal}_{\text{PCB Flight Time}} + \text{Signal}_{\text{Component2 Flight Time}}$$

Combining these equations yields:

$$\text{Total\_Strobe}_{\text{Flight Time}} = \text{Total\_Signal}_{\text{Flight Time}} \pm \text{Tolerance}$$

$$\text{Strobe}_{\text{Component1 Flight Time}} + \text{Strobe}_{\text{PCB Flight Time}} + \text{Strobe}_{\text{Component2 Flight Time}} = \text{Signal}_{\text{Component1 Flight Time}} + \text{Signal}_{\text{PCB Flight Time}} + \text{Signal}_{\text{Component2 Flight Time}} \pm \text{Tolerance}$$

Solving for $\text{Signal}_{\text{PCB Flight Time}}$ yields:

$$\text{Signal}_{\text{PCB Flight Time}} = \text{Strobe}_{\text{Component1 Flight Time}} + \text{Strobe}_{\text{PCB Flight Time}} + \text{Strobe}_{\text{Component2 Flight Time}} - \text{Signal}_{\text{Component1 Flight Time}} - \text{Signal}_{\text{Component2 Flight Time}} \pm \text{Tolerance}$$

Now substituting in velocities and trace lengths, we conclude with Equation 12-2.

Equation 12-2. Tuning for 1 Signal with Respect to 1 Strobe

$$\begin{aligned}\text{Signal}_{\text{PCB Trace Length}} = (&(\text{Strobe}_{\text{Component1 Trace Length}} / \text{Strobe}_{\text{Component1 Trace Velocity}}) \\ &+ (\text{Strobe}_{\text{PCB Trace Length}} / \text{Strobe}_{\text{PCB Trace Velocity}}) \\ &+ (\text{Strobe}_{\text{Component2 Trace Length}} / \text{Strobe}_{\text{Component2 Trace Velocity}}) \\ &- (\text{Signal}_{\text{Component1 Trace Length}} / \text{Signal}_{\text{Component1 Trace Velocity}}) \\ &- (\text{Signal}_{\text{Component2 Trace Length}} / \text{Signal}_{\text{Component2 Trace Velocity}})) \\ &* \text{Signal}_{\text{PCB Trace Velocity}} \pm \text{Tolerance}\end{aligned}$$

12.5.4 DDR Example

The DDR Source Synchronous bus requires groups of 8 signals and 2 strobes to be length tuned within 25 mils. Given that the PCB trace length for DDRA_DQS2 is 3.85 inches, what is the solution space for DDRA_DQS11 and DDRA_DQ20?

To determine the PCB solution space for the signal DDRA_DQ20, you need the PCB length of the strobe DDRA_DQS11. So, we will find the length for DDRA_DQS11 first. Using Equation 12-2 as a basis:

$$\begin{aligned} DDRA\_DQS11_{PCB\_length} = & \ ((DDRA\_DQS2_{MCH\_length} / DDRA\_DQS2_{MCH\_velocity}) \\ & + (DDRA\_DQS2_{PCB\_length} / DDRA\_DQS2_{PCB\_velocity}) \\ & - (DDRA\_DQS11_{MCH\_length} / DDRA\_DQS11_{MCH\_velocity})) \\ & * DDRA\_DQS11_{PCB\_velocity} \pm Tolerance \end{aligned}$$

We can find the MCH package velocities and trace lengths in the *Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet*, "Chipset Interface Trace Length Compensation" Chapter. The datasheet states that the trace delay due to signal velocity is the inverse of velocity. The MCH package trace delay due to signal velocity is 150 ps/in, so the velocity is (150 ps/in) $^{-1}$. The PCB trace delay due to signal velocity is 175 ps/in, so the velocity is (175 ps/in) $^{-1}$. The MCH package trace length for DDRA_DQS2 is 356.06 mils, DDRA_DQS11 is 567.48 mils, and DDRA_DQ20 is 690.51 mils.

$$\begin{aligned} DDRA\_DQS11_{PCB\_length} = & \ ((0.35606 \text{ in} * 150 \text{ ps/in}) \\ & + (3.850 \text{ in} * 175 \text{ ps/in}) \\ & - (0.56748 \text{ in} * 150 \text{ ps/in})) \\ & / 175 \text{ ps/in} \pm 0.025 \text{ in} \\ & = 3.669 \text{ in} \pm 0.025 \text{ in} \end{aligned}$$

By setting the PCB length of DDRA_DQS11 as close to 3.669 in as possible, we can have a wider solution space for all 8 of the signals which need to be length tuned to DDRA_DQS2 and DDRA_DQS11. Next, let's find the PCB length for DDRA_DQ20. Using Equation 12-2 as a basis:

$$\begin{aligned} DDRA\_DQ20_{PCB\_length} = & \ ((DDRA\_DQS2_{MCH\_length} * DDRA\_DQS2_{MCH\_velocity}) \\ & + (DDRA\_DQS2_{PCB\_length} * DDRA\_DQS2_{PCB\_velocity}) \\ & - (DDRA\_DQS20_{MCH\_length} * DDRA\_DQS20_{MCH\_velocity})) \\ & * DDRA\_DQ20_{PCB\_velocity} \pm Tolerance \end{aligned}$$

Then, using the values from above and simplifying the velocity yields:

$$\begin{aligned} DDRA\_DQS11_{PCB\_length} = & \ ((0.35606 \text{ in} * 150 \text{ ps/in}) \\ & + (3.850 \text{ in} * 175 \text{ ps/in}) \\ & - (0.69051 \text{ in} * 150 \text{ ps/in})) \\ & / 175 \text{ ps/in} \pm 0.025 \text{ in} \\ & = 3.563 \text{ in} \pm 0.025 \text{ in} \end{aligned}$$

12.5.5 Bus Length Tuning Methodology

Many buses, such as memory and processor system bus, require length tuning a group of signals. A common way to do this is by routing the bus first to determine what the approximate length range is. Then, you can pick an arbitrary signal. Sometimes this signal may be the most difficult to route or adjust to tune. Using the PCB trace length for this signal, you can determine the solution space for the remainder of the signals and strobes in the group.

Intel commonly provides a length tuning calculator spreadsheet. This calculator uses a "seed value." This is the PCB length of an arbitrary signal, typically the signal with the shortest PCB length. Then, the calculator uses all the routing parameters specified in the Platform Design Guide (minimum and maximum lengths, tolerances, signal groups, etc.) to determine the solution space for the bus in question.

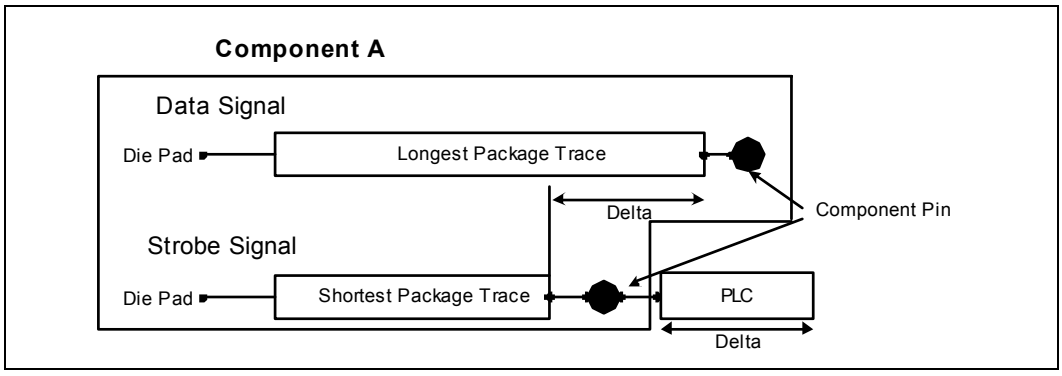
12.6 Processor Bus Tuning

Routing the processor system bus requires length matching within source synchronous groups. A major difference between the processor system bus and other source synchronous buses is the loading effects from the middle socket processor. As a result, pure propagation-based length matching cannot be used. Instead, length matching is based on both propagation and additional signal integrity factors to account for the strobe-to-signal skew effects from the middle socket processor. These two factors are described in the next two sections, followed by a routing example in the last section.

12.6.1 Compensating for Package Trace Length Differences

The first factor in length matching involves compensating for package trace length differences for signals within the same strobe group. The "package trace length" is defined as the trace segment between the die pad and component package pin. The package lengths on the processor and MCH introduce skew between different signals as illustrated in the example given in Figure 12-13. Note that "Component A" represents a processor or MCH. The example uses a strobe and data signal, which happen to have the shortest and longest package trace lengths respectively. Each of the signals will have varying amounts of package skew. The amount of skew for a particular signal is based on the difference between that signal's package trace length and the longest signal's package trace length in the same signal group. E.g., signals with shorter package length will have more package trace length compensation than signals with package lengths closer to the longest package trace.

Figure 12-13. Package Trace Length Differences



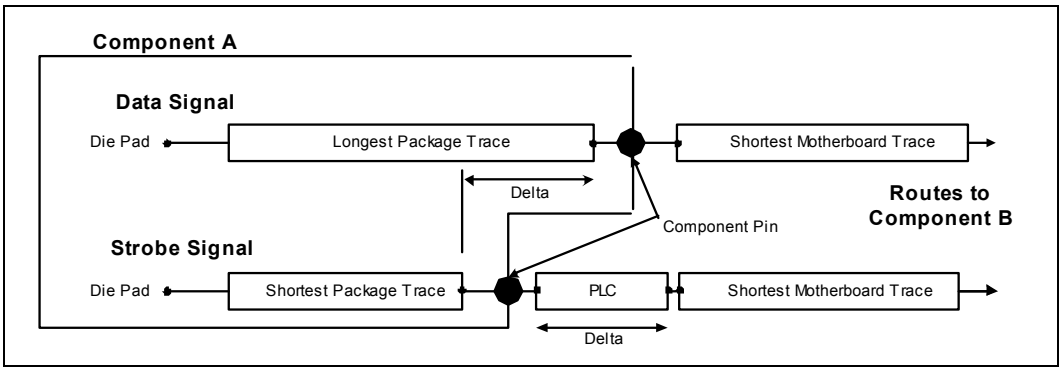
To compensate for package-induced skew, all source synchronous motherboard trace lengths are adjusted by the exact amount of Package Length Compensation (PLC). Equation 12-3 defines PLC for a particular signal. Signal X is any signal in the group that does not have the longest package length. This includes the strobe signals.

Equation 12-3. Package Length Compensation (PLC) Definition

$$SignalX_{PLC} = Maximum\_Signal\_in\_Group_{Package\ Length} - SignalX_{Package\ Length}$$

The signals with a package length less than the longest package trace in that group will require additional motherboard trace length equal to $SignalX_{PLC}$. Equation 12-3 yields a zero PLC for the signal with the longest package length. So the signal with the longest package length would require no amount of additional motherboard trace length. Figure 12-14 illustrates PLC using a data signal as the longest package trace and strobe signal as "Signal X".

Figure 12-14. Example of PLC Compensation on the Motherboard



12.6.2 Signal Integrity Adjustment Factor

The second factor in length matching the system bus source synchronous signals involves adjusting motherboard trace lengths to compensate for signal integrity effects that will affect the relationship of the signal and associated strobe at each receiver. The signal integrity effects include edge rate degradation and reflections caused by the stubs created by the Processor 1 package. These stub lengths act as capacitive loads and transmission lines, and thus degrade the edge rate as the signal travels from Processor 0 to the MCH and from the MCH to Processor 0.

The Processor 0 signals with longer stubs will see more degradation than those with shorter stubs. For source synchronous signals, the goal is to reduce skew between a signal and its associated strobe. Since strobe signals typically have short package lengths, they will not see much edge rate degradation. However, since other signals can have stub lengths up to approximately 600 mils, the edge rate degradation can be dramatic relative to that of the strobe. These large differences in the slope and shape of the edges at the receiver results in a significant skew between the longer and shorter signals within the same signal group. I.e. the additional noise of longer processor package signals will cause them to cross the VREF threshold at a later time than the shorter processor package signals. The net effect could result in source synchronous timing violations if uncompensated.

To compensate for this signal integrity degradation, a specific length is added to the motherboard trace lengths for signals that have shorter stub lengths. This will achieve similar VREF threshold crossing times for a signal and its strobe at the receiver. This motherboard length is referred to as the Signal Integrity (SI) Adjustment Length. The methodology for calculating SI Adjustment Length is dependent on the system bus topology, edge rates of the processor and MCH, signal velocities for package and motherboard, VCC_CPU termination voltage, I/O capacitance of the

buffers, balancing setup and hold time requirements of the receiver, and other electrical factors verified in simulation and system bus validation. For the system bus recommendations included in this document, Equation 12-4 is used:

Equation 12-4. Signal Integrity Adjustment Length

$$\text{Signal } X_{SI\ Adj} = 0.78 * \text{Signal}X_{PLC}$$

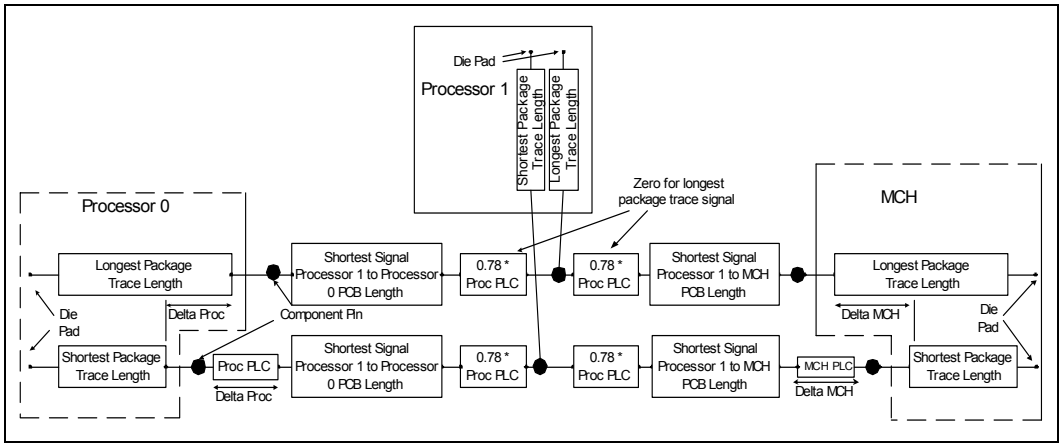
The 0.78 compensation factor was determined to be the optimum adjustment for the system bus recommendations given in this platform design guide.

12.6.3 Final Length Matching Equation

This section explains the final length matching compensation scheme, associated equations, and an explanation for determining the motherboard trace lengths. Processor Length Matching is only dependant upon a signals PLC and the SI motherboard. To determine an actual PCB length, the designer can use one signal as a reference signal to calculate the PCB length of the remaining signals in a group. For simple illustrative purposes, the formulas and examples used are based upon the shortest PCB trace length. However, the formulas could be based off any signal in the group. For simple illustrative purposes, the example also assumes the shortest and longest signals on the processor package are the shortest and longest for the MCH package as well. This is not necessarily the case.

Figure 12-15 contains the final length matching example that accounts for PLC and SI Adjustment Length compensation in the motherboard trace lengths. The signal whose motherboard trace length between Processor 0 and Processor 1 has the longest Processor package length has no Signal Adjustment Length Compensation (denoted as "SI") in the Processor 0/Processor 1 path. All source synchronous signals with less than the longest processor and MCH package length require varying amounts of PLC and SI motherboard length segments added to $\text{Shortest Signal}_{\text{Processor 0 to Processor 1 PCB Length}}$ and $\text{Shortest Signal}_{\text{Processor 1 to MCH PCB Length}}$ respectively. The example in Figure 12-15 shows SI adjustment for the strobe signal, but the strobe signal could be replaced with any data signal with a processor package length that is not the maximum in that group.

Figure 12-15. Final Illustration of PLC and SI Length Matching



It is important to note that PLC is only performed for the components at the endpoints of the system bus (i.e., Processor 0 and the MCH). At the components in the middle of the bus, the SI factors is used. Since SI is a scaling factor of the PLC, the PLC is still taken into consideration at the middle of the bus. Additional PLC segments on both sides of Processor 1 would certainly balance the total pad-to-pad length for the Processor 0/Processor 1 and Processor 1/MCH paths.

However, it would unbalance the Processor 0/MCH path by a total length of 2*SignalX_{PLC} since this path does not contain propagation along the Processor 1 package. The Processor 0/MCH path has the longest propagation in the system and presents the highest risk of mismatch between the signals and associated strobe due to the Processor 1 package stubs. The best pad-to-pad compensation for the Processor 0/MCH direction, excludes 2 SignalX_{PLC} lengths at Processor 1.

The length matching equations are based on the PLC and SI concepts explained in the previous two sections. The total pad-to-pad length is represented by the following equations for each of the three possible driver/receiver paths and can be derived by adding the total lengths as illustrated in Figure 12-15.

Equation 12-5. Processor 0/Processor 1 Length Matching

$$\begin{aligned}\text{Signal X}_{\text{Processor 1 Die Pad-to-Processor 0 Die Pad}} &= \text{SignalX}_{\text{Processor Package Length}} \\ &+ \text{SignalX}_{\text{Processor PLC}} + \text{Shortest Signal}_{\text{Processor 0 to Processor 1 PCB Length}} \\ &+ \text{Signal X}_{\text{SI Adj}} + \text{SignalX}_{\text{Processor Package Length}}\end{aligned}$$

Equation 12-6. Processor 1/MCH Length Matching

$$\begin{aligned}\text{SignalX}_{\text{Processor 1 Die Pad-to-MCH Die Pad}} &= \text{SignalX}_{\text{Processor Package Length}} + \text{SignalX}_{\text{SI Adj}} \\ &+ \text{Shortest Signal}_{\text{Processor 1 to MCH PCB Length}} + \text{SignalX}_{\text{MCH PLC}} \\ &+ \text{SignalX}_{\text{MCH Package Length}}\end{aligned}$$

Equation 12-7. Processor 0/MCH Length Matching

$$\begin{aligned}\text{SignalX}_{\text{Processor 0 Die Pad-to-MCH Die Pad}} &= \text{SignalX}_{\text{Processor Package Length}} \\ &+ \text{SignalX}_{\text{Processor PLC}} + \text{Shortest Signal}_{\text{Processor 0 to Processor 1 PCB Length}} \\ &+ \text{SignalX}_{\text{SI Adj}} + \text{SignalX}_{\text{SI Adj}} + \text{Shortest Signal}_{\text{Processor 1 to MCH PCB Length}} \\ &+ \text{SignalX}_{\text{MCH PLC}} + \text{SignalX}_{\text{MCH Package Length}}\end{aligned}$$

Equation 12-3 and Equation 12-4 are used to generate the various PLC and SI Adjustment Length parameters for these equations. Extracting specific parameters from Equation 12-5, the total motherboard length for Signal X in the Processor 0/Processor 1 path is defined in Equation 12-8. Similarly, extracting specific parameters from Equation 12-6, the total motherboard length for Signal X in the Processor 0/Processor 1 path is defined in Equation 12-9.

Equation 12-8. Processor 0 to Processor 1 PCB Length Definition

$$\begin{aligned}\text{SignalX}_{\text{Processor 0 to Processor 1 PCB Length}} &= \text{SignalX}_{\text{Processor PLC}} + \text{SignalX}_{\text{SI Adj}} \\ &+ \text{Shortest Signal}_{\text{Processor 0 to Processor 1 PCB Length}}\end{aligned}$$

Equation 12-9. Processor 1 to MCH PCB Length Definition

$$\begin{aligned}\text{SignalX}_{\text{Processor 1 to MCH PCB Length}} &= \text{SignalX}_{\text{MCH PLC}} + \text{SignalX}_{\text{SI Adj}} \\ &+ \text{Shortest Signal}_{\text{Processor 1 to MCH PCB Length}}\end{aligned}$$

$SignalX_{Processor\ 0\ to\ Processor\ 1\ PCB\ Length}$ and $SignalX_{Processor\ 1\ to\ MCH\ PCB\ Length}$ should be chosen to allow all signals in the same signal group to meet the specific system bus routing guidelines documented in Chapter 5 of this document. The PLC and SI Adjustment Length motherboard segments adjust the motherboard trace lengths to account for the processor and MCH package effects.

Using this relationship, if $SignalX_{Processor\ 0\ to\ Processor\ 1\ PCB\ Length}$ and $SignalX_{Processor\ 1\ to\ MCH\ PCB\ Length}$ are known, then $SignalY_{Processor\ 0\ to\ Processor\ 1\ PCB\ Length}$ and $SignalY_{Processor\ 1\ to\ MCH\ PCB\ Length}$ can be determined using Equation 12-10 and Equation 12-11 respectively.

Equation 12-10. SignalY Processor 0/Processor 1 Motherboard Lengths

$$SignalY_{Processor\ 0\ to\ Processor\ 1\ PCB\ Length} = SignalX_{Processor\ 0\ to\ Processor\ 1\ PCB\ Length} - SignalX_{Processor\ PLC} - SignalX_{SI\ Adj} + SignalY_{Processor\ PLC} + SignalY_{SI\ Adj}$$

Equation 12-11. SignalY Processor 1/MCH Motherboard Lengths

$$SignalY_{Processor\ 1\ to\ MCH\ PCB\ Length} = SignalX_{Processor\ 1\ to\ MCH\ PCB\ Length} - SignalX_{Processor\ PLC} - SignalX_{SI\ Adj} + SignalY_{MCH\ PLC} + SignalY_{SI\ Adj}$$

These equations operate by first starting with the known total motherboard length for Signal X and then subtracting Signal X's PLC and SI Adjustment Length compensations. The PLC and SI Adjustment compensations for Signal Y are then added.

12.6.4 System Bus Length Matching Example

Note: Example component values are used in this example and should not be relied upon for actual design of the system bus.

The system bus 4X data source synchronous signal group requires groups of 17 signals and 2 associated strobes to be length matched within ± 25 mils between components.

Part 1. Given that routing has started with DSTBN0# routed between Processor 0 and Processor 1 with a pin-to-pin route of exactly 5.0 inches, what is the DSTBP0# Processor 0/Processor 1 motherboard length?

Part 2. Given that routing has started with DSTBN0# routed between Processor 1 and MCH with a pin-to-pin route of exactly 4.0 inches, what is the DSTBP0# Processor 1/MCH motherboard length?

The processor and MCH package trace lengths can be obtained from the Intel® E7501 chipset System Bus Length Matching Spreadsheet. Contact your Intel representative for information about the Length Matching Spreadsheet tool. For this example, we will use the following processor and MCH values:

- Maximum processor package length is this group is 0.578 inch
- DSTBN0# processor package length is 0.208 inch
- DSTBP0# processor package length is 0.134 inch
- Maximum MCH package length is this group is 1.060 inches
- DSTBN0# MCH package length is 0.842 inch
- DSTBP0# MCH package length is 0.738 inch

Part 1 Solution: By definition, the DSTBN0# signal 5-inch route already includes the PLC and SI motherboard trace components. The PLC and SI values are determined for DSTBN0# and DSTBP0# using Equation 12-3 and Equation 12-4.

$$DSTBN0\#_{Processor\ PLC} = Maximum\ in\ Group_{Processor\ Package\ Length} - DSTBN0\#_{Processor\ Package\ Length}$$

$$= 0.578\ inch - 0.208\ inch = 0.370\ inch$$

$$DSTBN0\#_{SI\ Adj} = 0.78 * DSTBN0\#_{Processor\ PLC}$$

$$= 0.78 * 0.370\ inch = 0.289\ inch$$

$$DSTBP0\#_{Processor\ PLC} = Maximum\ in\ Group_{Processor\ Package\ Length} - DSTBP0\#_{Processor\ Package\ Length}$$

$$= 0.578\ inch - 0.134\ inch = 0.444\ inch$$

$$DSTBP0\#_{SI\ Adj} = 0.78 * DSTBP0\#_{Processor\ PLC}$$

$$= 0.78 * 0.444\ inch = 0.346\ inch$$

The DSTBP0# Processor 0/Processor 1 motherboard lengths are calculated using Equation 12-10.

$$DSTBP0\#_{Processor\ 0\ to\ Processor\ 1\ PCB\ Length} = DSTBP0\#_{Processor\ 0\ to\ Processor\ 1\ PCB\ Length} - DSTBN0\#_{Processor\ PLC} - DSTBN0\#_{SI\ Adj} + DSTBP0\#_{Processor\ PLC} + DSTBP0\#_{SI\ Adj}$$

$$= 5.000 - 0.370 - 0.289 + 0.444 + 0.346 = 5.131\ inches$$

Since the system bus data signals must be length matched within ± 25 mils between components, the DSTBP0# Processor 0/Processor 1 motherboard length is 5.131 ± 0.025 inch.

Part 2 Solution: By definition, the DSTBN0# signal 4-inch route already includes the PLC and SI motherboard trace components. The SI value can be used from Part 1. The MCH PLC values are determined for DSTBN0# and DSTBP0# using Equation 12-3.

$$DSTBN0\#_{MCH\ PLC} = Maximum\ in\ Group_{MCH\ Package\ Length} - DSTBN0\#_{MCH\ Package\ Length}$$

$$= 1.060\ inch - 0.842\ inch = 0.218\ inch$$

$$DSTBP0\#_{MCH\ PLC} = Maximum\ in\ Group_{MCH\ Package\ Length} - DSTBP0\#_{MCH\ Package\ Length}$$

$$= 1.060\ inches - 0.738\ inch = 0.322\ inch$$

The DSTBP0# Processor 1/MCH motherboard lengths are calculated using Equation 12-11.

$$DSTBP0\#_{Processor\ 1\ to\ MCH\ PCB\ Length} = DSTBN0\#_{Processor\ 1\ to\ MCH\ PCB\ Length} - DSTBN0\#_{MCH\ PLC} - DSTBN0\#_{SI\ Adj} + DSTBP0\#_{MCH\ PLC} + DSTBP0\#_{SI\ Adj}$$

$$= 4.000 - 0.218 - 0.289 + 0.322 + 0.346 = 4.161\ inches$$

Since the system bus data signals must be length matched within ± 25 mils between components, the DSTBP0# Processor 1/MCH motherboard length is 4.161 ± 0.025 inch.

The above example demonstrates the importance of the first routed motherboard traces since these will establish the routing lengths for the remaining signals in the same signal group. Therefore, the $DSTBP0\#_{Processor\ 0\ to\ Processor\ 1\ PCB\ Length}$ and $DSTBP0\#_{Processor\ 1\ to\ MCH\ PCB\ Length}$ values should be chosen carefully based on routing studies to avoid multiple iterations of length matching computations for each signal.

Schematic Checklist 13

13.1 Processor Schematic Checklist

Table 13-1. Processor Schematic Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments
A20M# IGNNE# INIT# LINT0/INTR LINT1/NMI SMI# SLP# STPCLK#	• Connect to both processors and Intel® ICH3-S. Include 200 Ω ± 5% pull-up to VCC_CPU.	• Asynchronous GTL+ Input Signal. • Refer to Section 5.3.6.
A[35:3]#[1] ADSTB[1:0]#[2] D[63:0]#[3] DBI[3:0]# DSTBN[3:0]#[4] DSTBP[3:0]#[5] REQ[4:0]#[6]	• Connect to both processors and the MCH.	• AGTL+ Source Synchronous I/O. • Refer to Section 5.1.
ADS# AP[1:0]# DBSY# DP[3:0]# DRDY# LOCK# BPRI# DEFER# RS[2:0]# RSP# TRDY#[8]	• Connect to both processors and the MCH.	• AGTL+ Common Clock I/O. • AGTL+ Common Clock Input • Refer to Section 5.2.
FERR#/PBE# IERR# PROCHOT# THERMTRIP#	• If supported, connect to both processors and the ICH3-S. Terminate at both ends with 56 Ω ± 5% pull-up to VCC_CPU. • If not supported, leave as no-connect or connect to a Baseboard Management Controller (BMC).	• Asynchronous GTL+ Output. • Refer to Section 5.3.2.
BINIT# BNR# HIT# HITM# MCERR#	• Connect to both processors and the MCH. • Route as common clock signal.	• AGTL+ Common Clock I/O Wired-OR signals. • Refer to Section 5.2.1.
BCLK[1:0]	• Connect to a 49.9 Ω 1% pull-down and to a series resistor (20 – 33 Ω). Connect other side of series resistor to CK408.	• System Bus Clock. • Refer to Section 4.1. **NOTE:** BCLK[1:0] are processor pin names that are connected to clocks in the Host_CLK clock group on CK408B.

Table 13-1. Processor Schematic Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments
BPM[5:0]#		• For all ITP interface signal schematic, layout and routing recommendations, refer to the *ITP700 Debug Port Design Guide*.
BR[3:0]#	• Connect BR[0]# to the MCH's BREQ0# pin, Processor 0's BR0# pin, and Processor 1's BR1# pin. Terminate using a 50 Ω ± 5% pull-up resistor at Processor 0. • Connect BR[1]# signal to Processor 0's BR1# pin and Processor 1's BR0# pin. Terminate both ends of the bus using 50 Ω ± 5% pull-up resistors. • BR[3:2]# should be pulled-up to VCC_CPU using a 50 Ω ± 5% individually at each processor or be connected between processors and terminated at one end.	• BR0# is an AGTL+ Common Clock I/O. • BR[3:1]# are AGTL+ Common Clock Inputs. • These signals do not have on-die processor termination and must be terminated on the motherboard. • Refer to Section 5.2.3.
BSEL[1:0]	• Connect to external comparator logic that verifies both processors are specified to operate at the same system bus frequency. Also use these signals to select the clock driver to operate at either 100 or 133 MHz. • 1 kΩ 5% pull-up to 3.3 V, if using recommended circuit.	• Driven by processor to indicate specified system bus frequency. • Refer to Section 5.6.3.
COMP[1:0]	• Terminate to ground separately using 49.9 Ω ± 1% resistors.	• Power/Other. • Refer to Section 5.3.3.
GTLREF[3:0]	• 49.9 Ω ± 1% pull-up to VCC_CPU. • 84.5 Ω ± 1% pulldown to ground. • At the divider, decouple with a 1 µF and at the component pin, decouple with a 220 pF.	• Power/Other. • Refer to Section 11.2.10.
ODTEN	• Enable on-die termination (ODT) on Processor 0 (end processor) by pulling up to VCC_CPU with a 50 Ω ± 20% resistor. • Disable ODT for Processor 1 by pulling down to ground with a 50 Ω ± 20% resistor.	• Input. • Refer to Section 5.3.4.
PWRGOOD (CPUPWRGOOD)	• 300 Ω ± 5% pull-up to VCC_CPU. • Connect to both processors and ICH3-S.	• Power/Other. • Refer to Section 5.3.1.
Reserved	• Reserved signals must remain as No Connect (NC).	
RESET#[7]	• 51 Ω ± 5% pull-up to VCC_CPU. • Connect to MCH and both processors. Note that this signal is dual terminated at both ends of transmission line.	• AGTL+ Common Clock Input. • Refer to Section 5.2.2. • If using ITP, for signal connection to ITP, refer to the *ITP700 Debug Port Design Guide* for all schematic, layout and routing recommendations.
SKTOCC#	• If supported, pull-up to 3.3 V and use in external logic to detect whether one or two processors are installed. • If unused, leave as NC.	• Power/Other • Refer to Section 5.6.2.

Table 13-1. Processor Schematic Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments
SM_ALERT# SM_CLK SM_DAT	• Connect to both processors and SMBus. • A pull-up resistor to 3.3 V. Resistor value is based on the number of devices on the SMBus.	• These signals have 10 kΩ pull-downs on the Intel® Xeon™ processor with 512-KB L2 cache and are not supported on the Intel® Xeon™ processor with 533 MHz system bus • Refer to Section 5.5 and Section 9.5.4.
SM_EP_A[2:0]	• Leave as no connect to set bit low, or pull-up to 3.3 V through 100 Ω ± 5% resistor to set bit high. • Use these address bits to set a unique SMBus address for the memory devices on the processor.	• SMBus Input. • These signals have 10 kΩ pull-downs on the Intel Xeon processor with 512-KB L2 cache and are not supported on the Intel Xeon processor with 533 MHz system bus. • Refer to Section 5.5 and the *Intel® Xeon™ Processor with 512-KB L2 Cache at 1.80 GHz to 2.80 GHz Datasheet* for more details.
SM_TS_A[1:0]	• Use these address bits to set a unique SMBus address for the thermal devices on the processor. • Leave as no connect to set bit to high-impedance state. • Pull-up to 3.3 V through 1 kΩ ± 5% to set bit high. • Pull-down to ground through 1 kΩ ± 5% to set bit low.	• SMBus Input. • These signals are not supported on the Intel Xeon processor with 533 MHz system bus. • Refer to Section 5.5 and the *Intel® Xeon™ Processor with 512-KB L2 Cache at 1.80 GHz to 2.80 GHz Datasheet* for more details
SM_VCC / VID_VCC	• Connect to 3.3 V power supply.	
SM_WP	• 100 Ω ± 5% pull-up to 3.3 V to write-protect the processor's Scratch EEPROM. • Leave as no connect (NC) to disable write-protecting of Scratch EEPROM.	• SMBus Input. • Refer to Section 5.5.
TESTHI[6:0]	• Option 1: Recommend separate 50 Ω ± 20% pull-up to VCC_CPU. • Option 2: TESTHI[3:0] and TESTHI[6:5] may all be tied together and pulled up to VCC_CPU with a single 50 Ω resistor if desired. However, boundary scan test cannot be performed if these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins.	• Input. • Refer to Section 5.3.5.
THERMDA THERMDC	• Connect to the Cathode and Anode pins of the thermal sensor.	• Refer to Section 5.5.2.
VCCA	• Use discrete RLC filter to provide clean power.	• An isolated power for internal PLL. • Refer to Section 11.2.7.
VCCIOPLL	• Use discrete RLC filter to provide clean power.	• An isolated power for internal PLL. • Refer to Section 11.2.7.

Table 13-1. Processor Schematic Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments
VCCSENSE	• Leave No Connect.	• Isolated low impedance connection to processor core VCC_CPU. • Refer to Section 11.2.2.
VID[4:0]	• Individually pull-up to 3.3 V using 1 kΩ resistor, provided a VRx 9.1 compliant regulator is used and recommended comparator is used. • Should be routed individually from each processor to the voltage regulator supplying its VCC_CPU supply. • Compare VIDs from both processors using glue logic to disable VR/VRM if VIDs of both processors do not match.	• Processor drives these signals to indicate maximum core voltage allowed. SM_VCC must be correct and stable before the VRM should rely on these outputs. • Refer to Section 5.6.1, Section 5.6.4, and Section 11.2.
VSSA	• Use discrete RLC filter to provide clean power.	• Isolated ground for internal PLLs. • Refer to Section 11.2.7.
VSSSENSE		• An isolated low impedance connection to processor core VSS. • Refer to Section 11.2.2.
VCC_CPU Decoupling	• Minimum of capacitors per processor with the following package and electrical properties: • 10 - 560 µF (OSCONs): ESR < 12 mΩ; ESL < 3.1 nH • 20 - 22.0 µF (Ceramic 1210 package): ESR < 10 mΩ; ESL < 1.1 nH • 4 - 1.0 µF (Ceramic 0805 package): ESR < 8 mΩ; ESL < 0.702 nH • 3 - 0.1 µF (Ceramic 0603 package): ESR < 6 mΩ; ESL < 0.630 nH	• Refer to Section 11.2.9.1 and Section 11.2.9.2. • Contact your capacitor vendor to verify these electrical properties.

NOTES:
1. A[35:3]# pins on the processor correspond to HA[35:3]# pins on the MCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the MCH.
3. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the MCH.
4. DSTBN[3:0]# pins on the processor correspond to HADSTBN[3:0]# pins on the MCH.
5. DSTBP[3:0]# pins on the processor correspond to HADSTBP[3:0]# pins on the MCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the MCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the MCH.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the MCH.

13.2 MCH Schematic Checklist

Table 13-2. MCH Schematic Checklist (Sheet 1 of 3)

Checklist Items	Recommendations	Comments
Host Interface		
ADS# AP[1:0] BINIT# BNR# BPRI# BREQ0#[1] CPURST#[2] DBI[3:0]# DBSY# DEFER# DP[3:0]# DRDY# HA[35:3]#[3] HD[63:0]#[4] HADSTB[1:0]#[5] HDSTBN[3:0]#[6] HDSTBP[3:0]#[7] HIT# HITM# HLOCK# HREQ[4:0]#[8] HTRDY#[9] RS[2:0]# RSP# XERR#[10]	• See processor section of this checklist.	
DDR Interfaces A and B / Connector		
DQ_x[63:0] CB_x[7:0] DQS_x[17:0]	• Dependant upon configuration.	• Refer to Section 6.2.
MA_x[12:0] BA_x[1:0] RAS_x# CAS_x# WE_x#	• Terminate these signals to DDR VTERM (1.25 V).	• Refer to Section 6.4.
CS[7:0]_x#	• Terminate these signals to DDR VTERM (1.25 V).	• Refer to Section 6.5.
CMDCLK_x[3:0] CMDCLK_x[3:0]#	• Connect directly to the corresponding DIMM.	• Refer to Section 6.3.
CKE_x	• Terminate to DDR VTERM (1.25 V).	• Refer to Section 6.6.
RCVENIN_x# RCVENOUT_x# RCVEN_x	• Connect as shown in Figure 6-12.	• Refer to Section 6.7.1. • RCVENIN_x# and RCVENOUT_x# are on the Intel® E7500 chipset MCH and RCVEN_x is on the Intel® E7501 chipset MCH.
DDRCOMP_x	• For E7500 chipset MCH, 6.98 Ω ± 1% pull-up to DDR VTERM (1.25 V). • For E7501 chipset MCH, 24.9 Ω ± 1% pull-down to Ground.	• Refer to Section 6.7.2.

Table 13-2. MCH Schematic Checklist (Sheet 2 of 3)

Checklist Items	Recommendations	Comments
DDRCVOL_x DDRCVOH_x DDRCVO_x	• Connect as shown in Figure 6-17.	• Refer to Section 6.7.4. • DDRCVOL_x and DDRCVOH_x are on the E7500 chipset MCH and DDRCVO_x is on the E7501 chipset MCH.
Hub Interface A		
HI[11:0] HI_STBF[11] HI_STBS[11]	• Connect to ICH3-S. • Must **not** have pull-up, pull-down, or series resistors.	• Refer to Section 7.3.1.
HIRCOMP_A	• 24.9 Ω ± 1% pull-up to VCC1_2	• Refer to Section 7.3.3.
Hub Interface B, C, D		
HI[18:0] HI[21:20] PSTRBF PSTRBS PUSTRBF PUSTRBS	• Connect to P64H2. • Must **not** have pull-up, pull-down, or series resistors.	• Refer to Section 7.2.1.
HIRCOMP_B HIRCOMP_C HIRCOMP_D	• 24.9 Ω ± 1% pull-up to VCC1_2	• Refer to Section 7.2.3.
Unused 16 bit interfaces	• All data, strobe, HISWNG_x, and HIRCOMP_x signals can be left as no connect. • HIVREF_[D:B] must be connected to ground.	• The MCH has integration detection logic that detects unpopulated 16-bit interfaces without external pull-ups and pull-downs. • Refer to Section 7.2.5.
Clocks, Reset, Miscellaneous Signals		
HCLKINP HLCKINN	• Connect to CK408 through a 33 Ω ± 1% series resistor with a 49.9 Ω ± 1% pull-down resistor to ground.	• Refer to Section 4.1.
CLK66	• Connect to CK408 66BUF pin using a 43 Ω ± 5% series resistor.	• Refer to Section 4.2.
RSTIN#	• Connect to PCIRST# output of the ICH3-S.	
Miscellaneous Signals		
XORMODE#	• 4.7 kΩ ± 5% pull-up to 3.3 V.	• Required for normal operation.
Reserved (Ball B30)	• 4.7 kΩ ± 5% pull-up to 3.3 V.	• Required for normal operation.
Reserved (Ball D29)	• 1 kΩ ± 5% pull-down to Ground.	• Required for normal operation.
HXRCOMP HYRCOMP	• Tie each COMP pin to a 25 Ω ± 1% pull-down to ground.	• Refer to Section 5.3.3.

Table 13-2. MCH Schematic Checklist (Sheet 3 of 3)

Checklist Items	Recommendations	Comments
Voltage References – Power Planes		
HDVREF[3:0] HAVREF[1:0] HCCVREF	• Use one dedicated voltage divider for all these signals. • Decouple the voltage divider with a 1 µF capacitor and use a 220 pF at the MCH pins.	• To provide constant and clean power delivery to the data, address and common clock signals of the host AGTL+ interface. • Refer to Section 11.2.10.
DDRVREF_x[5:0]	• Decouple each signal to ground with 0.1 µF parallel capacitor at each DIMM and MCH pin.	• Refer to Section 6.7.3.
HXSWING HYSWING	• 150 Ω ± 1% pull-down to ground • 301 Ω ± 1% pull-up to VCC_CPU • C1 = C2 = 0.01 µF	• Refer to Section 5.3.3.
HISWNG_[D:A], HIVREF_[D:A]	• MCH Hub reference swing voltage = 0.800 V ± 5%. • MCH Hub reference voltage = 0.350 V ± 5%. • R1 = 392 Ω ± 1%, R2 = 499 Ω ± 1%, R3 = 453 Ω ± 1%. • Decouple the MCH pin with a 0.01 µF. • Decouple the network nodes with a 0.1 µF	• Refer to Section 7.2.2 and Section 7.3.2.
Voltage Sequencing Requirement		
1.2 V and 2.5 V	• 1.2 V must rise with or before 2.5 V.	• Refer to Section 11.3.6.
Decoupling Requirements		
1.25 V (DDR VTERM)	• Two 0.1 µF and two 0.01 µF.	• Refer to Section 11.3.1
VCC_CPU	• Fourteen 0.1 µF	• Refer to Section 11.3.2
2.5 V	• Twenty-three 0.1 µF	• Refer to Section 11.3.3
1.2 V (Hub Interface)	• Four 0.1 µF	• Refer to Section 11.3.4
VCCA1_2 VCCAHI1_2 VCCACPU_1.2	• RLC network	• Refer to Section 11.3.5

NOTES:
1. The BREQ0# pin on the MCH corresponds to the BR0# pin on the processor.
2. The CPURST# pin on the MCH corresponds to the RESET# pin on the processor.
3. HA[35:3]# pins on the MCH correspond to A[35:3]# pins on the processor.
4. HD[63:0]# pins on the MCH correspond to D[63:0]# pins on the processor.
5. HADSTB[1:0]# pins on the MCH correspond to ADSTB[1:0]# pins on the processor.
6. HADSTBN[3:0]# pins on the MCH correspond to DSTBN[3:0]# pins on the processor.
7. HADSTBP[3:0]# pins on the MCH correspond to DSTBP[3:0]# pins on the processor.
8. HREQ[4:0]# pins on the MCH correspond to REQ[4:0]# pins on the processor.
9. The HTRDY# pin on the MCH corresponds to the TRDY# pin on the processor.
10. The MCH XERR# pin can be connected to the processor IERR# pin or the processor MCERR# pin.
11. In HI1.0 mode, HI_STBF and HI_STBS used to be referred as HI_STB# and HI_STB respectively.

13.3 Intel® ICH3-S Schematic Checklist

Note: There are no inputs to the ICH3-S that can be left floating.

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 1 of 6)

Checklist Items	Recommendations	Comments
Processor Signals		
A20M# CPUPWRGD CPUSLP# (SLP#) FERR# IGNNE# INIT# LINT1[1] LINT0[1] SMI# STPCLK#	• Refer to the signal recommendations under the Processor Schematic Checklist.	
RCIN# A20GATE	• Pull-up is required if driven by an open drain signal (the value of the resistor is determined by the driver), otherwise none needed.	• Typically driven by Open Drain external Micro-controller.
FWH Interface		
FWH[3:0]/ LAD[3:0] LDRQ[1:0]	• No extra pull-ups required. Connect straight to FWH/LPC and, if supported, a BMC.	• Intel® ICH3-S Integrates 24 kΩ pull-up resistors on these signal lines.
GPIO		
GPIO[7:0]	• Unused core well inputs must use a 8.2 kΩ – 10 kΩ pull-up to 3.3 V. • GPIO[1:0] can be used as REQ[B:A]#. • GPIO[1] can be used as PCI REQ[5]#. • GPIO[5:2] can be used as PIRQ[H:E]#. • These signals are 5 V tolerant.	• These pins are in the Main Power Well. Pull-ups must use the 3.3 V plane. • Ensure all unconnected signals are **outputs only.**
GPIO[8] and GPIO[13:11]	• Unused resume well inputs must use a 8.2 kΩ – 10 kΩ pull-up to VCCSUS3_3. • These are the only GPIs that can be used as ACPI compliant wake events. • These signals are not 5 V tolerant. • GPIO[11] can be used as SMBALERT#.	• These pins are in the resume power well. Pull-ups go to VCCSUS3_3 plane. • These are the only GPI signals in the resume well with associated status bits in the GPE1_STS register.
GPIO[23:16]	• GPIO[22] is open drain. • GPIO[17:16] can be used as GNT[B:A]#. • GPIO[17] can be used as PCI GNT[5]#.	• Fixed as output only. Can be left NC. • In main power well.
GPIO[28,27,25,24]	• Can be left NC. • From resume power well (VCCSUS3_3).	• I/O pins. Defaults as an output.
GPIO[43:32]	• From main power well (3.3 V).	• I/O pins. Defaults as an output when enabled as GPIOs.

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 2 of 6)

Checklist Items	Recommendations	Comments
Hub Interface		
HI[11:0] HI_STBS HI_STBF	• No pull-up resistor required.	• Refer to Section 7.3.1.
HICOMP	• 78.7 Ω ± 1% pull-up to 1.8 V.	• Refer to Section 7.3.3.
HIREF HITERM	• HREF = 0.350 V ± 5%. • HITERM = 0.700 V ± 5%. • R4 = 261 Ω ± 1%, R5 = 825 Ω ± 1%. • Decouple the ICH3-S pin with a 0.01 µF. • Decouple the network nodes with a 0.1 µF	• Refer to Section 7.3.2.
IDE Checklist		
PDD[15:0] SDD[15:0]	• No extra series termination resistors or other pull-ups/pull-downs are required. • PDD7/SDD7 does not require a 10 kΩ pull-down resistor.	• Refer to ATA ATAPI-6 specification.These signals have integrated series resistors. • Refer to Section 9.1.3. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω, but can range from 31 Ω to 43 Ω.
PDIOW# PDIOR# PDDACK# PDA[2:0] PDCS1# PDCS3# SDIOW# SDIOR# SDDACK# SDA[2:0] SDCS1# SDCS3#	• No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	• These signals have integrated series resistors. • Refer to Section 9.1.3. • **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω, but can range from 31 Ω to 43 Ω.
PDREQ SDREQ	• No extra series termination resistors. • No pull-down resistors required.	• These signals have integrated series resistors in the ICH3-S. • These signals have integrated pull-down resistors in the ICH3-S. • Refer to Section 9.1.3.
PIORDY SIORDY	• No extra series termination resistors. • 4.7 ± 5% kΩ pull-up to 3.3 V	• These signals have integrated series resistors in the ICH3-S. • Refer to Section 9.1.3.
IRQ14 IRQ15	• 8.2 kΩ – 10 kΩ pull-up to 3.3 V • No extra series termination resistors.	• Open drain outputs from drive. • Refer to Section 9.1.3.
IDERST#	• The PCIRST# signal should be buffered to form the IDERST# signal. A 22 – 47 Ω series resistor is recommended on this signal.	• Refer to Section 9.1.3.

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 3 of 6)

Checklist Items	Recommendations	Comments
Host Side / Device Side Cable Detection	• Connect IDE pin PDIAG#/CBLID# to an ICH3-S GPI pin. Connect a 10 kΩ resistor to ground on the signal line.	• The 10 kΩ resistor to ground prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. • Refer to Section 9.1.2.1.
Interrupt Interface		
APICCLK	• Pull-down directly to ground.	
APICD[1:0]	• 10 kΩ ± 5% pull-down to ground.	
PIRQ[D:A]#	• These signals require a pull-up resistor. • 2.7 kΩ ± 5% pull-up to 5 V or an 8.2 kΩ ± 5% pull-up to 3.3 V.	• Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: – PIRQ[A]# is connected to IRQ16. – PIRQ[B]# is connected to IRQ17. – PIRQ[C]# is connected to IRQ18. – PIRQ[D]# is connected to IRQ19. This frees the ISA interrupts.
PIRQ[H:E]#/ GPIO[5:2]	• These signals require a pull-up resistor. • 2.7 kΩ ± 5% pull-up to VCC_5 or an 8.2 kΩ ± 5% pull-up to 3.3 V.	• These signals are connected to the internal I/O APIC in the following fashion: – PIRQ[E]# is connected to IRQ20. – PIRQ[F]# is connected to IRQ21. – PIRQ[G]# is connected to IRQ22. – PIRQ[H]# is connected to IRQ23. This frees the ISA interrupts.
SERIRQ	• 8.2 kΩ ± 5% pull-up to 3.3 V.	• Open drain signal.
LAN Interface		
LAN_CLK, LAN_RXD[2:0], LAN_TXD[2:0], LAN_RSTSYNC	• Connect to Platform LAN Connect Device.	• Refer to Section 9.7. • LAN Connect Interface Signals can be left as NC if not used because the Input buffers are internally terminated.
Miscellaneous Signals		
SPKR	• No extra pull-up resistors.	• Refer to Section 9.2.
TP[0]	• 8.2 kΩ – 10 kΩ pull-up to VCCSUS3_3.	
AC_SDOUT	• No extra pull-down needed.	• This ball has a weak internal pull-down.

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 4 of 6)

Checklist Items	Recommendations	Comments
EE_DOUT	• Connect to EE_DIN of EEPROM. (Input from EEPROM perspective and output from ICH3-S perspective.) • If unused, leave No Connect.	• ICH3-S contains an integrated pull-up resistor for this signal.
EE_DIN	• Connect to EE_DOUT of EEPROM. (Ouput from EEPROM perspective and input from ICH3-S perspective.) • If unused, leave No Connect.	• ICH3-S contains an integrated pull-up resistor for this signal.
PCI Interface		
PERR# SERR# PLOCK# STOP# DEVSEL# TRDY# IRDY# FRAME# REQ[4:0]# GPIO[0]/REQ[A]# GPIO[1]/REQ[B]#/ REQ[5]#	• 8.2 kΩ ± 5% pull-up to 3.3 V, or a 2.7 kΩ ± 5% pull-up to 5 V.	• See the *PCI Local Bus Specification, Revision 2.2* for pull-up recommendations for 3.3 V and 5 V.
PCIRST#	• Depending on the load, this signal may have to be buffered.	• Improves Signal Integrity.
GNT[4:0]#	• No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented, they must be pulled up to 3.3 V.	• These signals are actively driven by the ICH3-S.
PME#	• No extra pull-up needed.	• This signal has integrated pull-up of 18 kΩ to 42 kΩ.
GNT[A]# /GPIO[16] GNT[B]#/ GNT[5]#/ GPIO[17]	• No extra pull-up needed.	• These signals have integrated pull-ups of 24 kΩ. • GNT[A] has an added strap function of “top block swap.” The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function.
Power Decoupling		
V_CPU_IO	• Connect to VCC_CPU. • Use one 0.1 µF decoupling capacitor.	• Refer to Section 11.4.4.
VCCRTC	• No clear CMOS jumper on VCCRTC. Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for Clear CMOS. • Requires one 0.1 µF decoupling capacitor.	• Refer to Section 11.4.4.
VCC3_3	• Use six 0.1 µF decoupling capacitors.	• Refer to Section 11.4.4.
VCCSus3_3	• Use two 0.1 µF decoupling capacitors.	• Refer to Section 11.4.4.
VCC1_8	• Use four 0.1 µF decoupling capacitors.	• Refer to Section 11.4.4.
VCCSus1_8	• Use one 0.1 µF decoupling capacitor.	• Refer to Section 11.4.4.

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 5 of 6)

Checklist Items	Recommendations	Comments
V5REF_Sus	• If USB is implemented in the platform, V5REF_Sus must be connected to VSUS5. • Use one 0.1 µF decoupling capacitor.	• Refer to Section 11.4.4.
V5REF	• Requires one 0.1 µF decoupling capacitor.	• Refer to Section 11.4.4.
Power Sequencing Requirements		
V5REF_Sus and VCCSus3_3	• V5REF_Sus must power up before or simultaneous to VCCSus3_3. It must power down after or simultaneous to VCCSus3_3. (For most platforms this sequencing is not an issues because VCCSus3_3 is derived from V5SUS.)	• Refer to Figure 11-27 for an example circuit schematic that may be used to ensure the proper V5REF sequencing.
V5REF and VCC3_3	• V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.	• Refer to Section 11.4.2.
VCC3_3 and VCC1_8	• The difference between VCC3_3 and VCC1_8 must never be greater than 2.0 V.	• Refer to Section 11.4.1.
VCCSus3_3 and VCCSus1_8	• The difference between VCCSus3_3 and VCCSus1_8 must never be greater than 2.0 V.	• Refer to Section 11.4.1.
Power Management		
THRM#	• Connect to temperature Sensor. • If not used: 8.2 kΩ ± 5% pull-up to 3.3 V.	• Input to ICH3-S cannot float. THRM# polarity bit defaults THRM# to active low.
SLP_S3# SLP_S5#	• No pull-up/down resistors needed. Signals driven by ICH3-S.	• Signals driven by ICH3-S.
PWROK	• This signal should be connected to power monitoring logic and should go high no sooner than 10 ms after both 3.3 V and 1.8 V have reached their nominal voltages. • Use external weak pull-down.	• Refer to Section 9.6.8.
PWRBTN#	• Connect to a momentary switch tied to ground. No extra pull-up resistors.	• This signal has an integrated pull-up of 18 kΩ – 42 kΩ.
RI#	• 8.2 kΩ ± 5% pull-up to VCCSUS3_3.	• If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set, and the system will interpret that as a wake event.
RSMRST#	• Can be tied to LAN_RST#. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCCSUS3_3 and VCCSUS1.8 have reached their nominal voltages. • 10 kΩ ± 5% pull-down to ground.	• Refer to Section 9.6.8.
SUS_STAT#	• Do not connect. • On remaining LPC bus devices, use 8.2 kΩ pull-up to 3.3 V.	

Table 13-3. Intel® ICH3-S Schematic Checklist (Sheet 6 of 6)

Checklist Items	Recommendations	Comments
RTC		
VBIAS	• Use one 0.047 µF capacitor.	• For noise immunity on VBIAS signal. • Refer to Figure 9-11.
RTCRST		• Refer to Section 9.6.8.
RTCX1 RTCX2	• Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 MΩ resistor. Decouple each signal dependant upon the crystal oscillator's characteristics. • RTCX1 may optionally be driven by an external oscillator instead of a crystal. These signals are 1.8 V only, and must not be driven by a 3.3 V source.	• Refer to Section 9.6.1 and Section 9.6.3.
System Management		
SMBDATA SMBCLK SMLINK[1:0]	• Connect SMBCLK to SMLink0 and SMBDATA to SMLink1. • Require external pull-up resistors, dependant upon bus capacitance and termination power plane.	• Refer to Section 9.5. • Value of pull-up resistors determined by line load, from Section 9.5.4.
SMBALERT#/ GPIO[11]	• See GPIO section if SMBALERT# not implemented.	
INTRUDER#	• 10 kΩ ± 5% pull-up to VCCRTC (VBAT) if not needed.	• Refer to Section 9.6.8.
USB		
USBRBIAS	• 18.2 Ω ± 1% pull-down to ground.	
USBP[5:0]P USBP[5:0]N	• No external resistors are required.	• Integrated 15 kΩ pull-down, effective output driver impedance of 45 Ω provided.
OC[5:0]#	• If not used: 10 kΩ ± 5% pull-up to VCCSUS3_3.	• Inputs must not float.

NOTES:
1. LINT1 and LINT0 map to INTR and NMI in the ICH3-S.

13.4 Intel® 82870P2 P64H2 Schematic Checklist

Table 13-4. Intel® P64H2 Schematic Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments
Hub Interface		
HI_[21,20,18:0] PUSTRBF PUSTRBS PSTRBF PSTRBS	• Connect to the MCH.	• Refer to Section 7.2.1
HI_[19]	• HI[19] must be left as no connect.	
HI_RCOMP	• 61.9 Ω ± 1% pull-up to 1.8 V.	• Refer to Section 7.2.3
HI_VREF HI_VSWING	• P64H2 Hub reference swing voltage = 0.800 V ± 5%. • P64H2 Hub reference voltage = 0.350 V ± 5%. • R4 = 261 Ω ± 1%, R5 = 332 Ω ± 1%, R6 = 750 Ω ± 1%. • Decouple the P64H2 pin with a 0.01 µF. • Decouple the network nodes with a 0.1 µF	• Refer to Section 7.2.2
PCI/PCI-X Bus Interface		
PxAD[63:32] PxC/BE[7:4]# PxDEVSEL# PxFRAME# PxIRDY# PxTRDY# PxSTOP# PxPERR# PxSERR# PxREQ[5:0]# PxGNT[5:4,2:0]# PxPLOCK# PxPAR64 PxACK64# PxREQ64#	• 8.2 kΩ ± 5% pull-up to 3.3 V. • Pull-ups on PxAD[63:32], PxC/BE[7:4]#, PxPAR64 not needed if bus only contains 64-bit devices	• See the *PCI Specification, Revision 2.2*.
PAGNT3#	• 8.2 kΩ ± 5% pull-down to ground.	
PBGNT3#	• 8.2 kΩ ± 5% pull-down to ground.	
IDSEL	• The series resistor to the device IDSEL should be 100 Ω. **NOTE:** The P64H2 does not have an IDSEL pin. Instead, the designer can chose a pin from PxAD[31:17].	• This has changed from the *PCI-X 1.0 Specification*. There is a specification change that allows for values other than the original 2 kΩ value.
3.3Vaux	• Leave this as unconnected on the PCI slots.	• The P64H2 does not support PCI bus power management.
PxPCIXCAP	• 8.2 kΩ ± 5% pull-up to 3.3 V.	• See *PCI-X Specification* recommendations for PxPCIXCAP connection.
Px_133EN	• For 133 MHz (max) PCI-X capable bus: 8.2 kΩ ± 5% pull-up to 3.3 V. • For 100 MHz (max) PCI-X capable bus: 8.2 kΩ ± 5% pull-down to ground.	• Only active if Px_PCIXCAP pins are high.

Table 13-4. Intel® P64H2 Schematic Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments
Interrupt Interface		
PAIRQ[15:0] PBIRQ[15:0]	• 8.2 kΩ ± 5% pull-up to 3.3 V.	
APICCLK APICD[1:0]	• 8.2 kΩ ± 5% pull-up to 3.3 V.	
Hot-Plug Interface Enabled		
PxPCIXCAP	• 8.2 kΩ ± 5% pulled up to 3.3 V.	• These PCI signals are connected to separate pins on the Intel® P64H2. See Section 8.2.6.4, Section 8.2.7.3, and Section 8.2.8.4 for the corresponding Hot-Plug mode implementation. Unused inputs should not float.
M66EN	• 8.2 kΩ ± 5% pulled up to 3.3 V.	• Unused inputs should not float.
HxSWITCH	• Connect to MRL Sensor. Open MRL should pull HxSWITCH to 3.3 V. Closed MRL should pull HxSWITCH to GND.	• Refer to Section 8.2.2
HxPRSNT1# HxPRSNT2#	• 5.6 kΩ ± 5% pull-up to 3.3 V . • If implementing Attention Button, PRSNT1# is the XOR of the momentary push-button and Slot Present signal.	• Refer to Section 8.2.2.
Hot-Plug – Single Slot Parallel Mode Specific		
HPx_SLOT[2:0][1]	SLOT[0]: 8.2 kΩ pull-up to 3.3 V. SLOT[1]: 8.2 kΩ pull-down to ground. SLOT[2]: 8.2 kΩ pull-down to ground.	• This is a strapping pin for enabling single-slot parallel mode which is latched during reset. SLOT[1] also functions as the HxPCIXCAP2A input when not in reset. SLOT2 also functions as the HxPCIXCAP1A input when not in reset. Refer to Table 8-15.
PxIRQ[14:8][1]	• 8.2 kΩ ± 5% pull-up to 3.3 V.	• These signals are mapped to Hot-Plug functions in single-slot Hot-Plug mode.
PxIRQ15[1]	• 8.2Ω – 10 kΩ pull-up to 3.3 V.	• A logic 1 on this pin indicates to the controller that the PCI slot should be immediately powered off. This signal is also connected to a SPST switch to ground which, when pressed, indicates by means of a logic 0 that the slot can be powered on.

Table 13-4. Intel® P64H2 Schematic Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments
Hot-Plug – Dual-Slot Parallel Mode Specific		
HPx_SLOT[2:0][1]	SLOT[0]: 8.2 kΩ pull-down to ground. SLOT[1]: 8.2 kΩ pull-up to 3.3 V. SLOT[2]: 8.2 kΩ pull-down to ground.	• This is a strapping pin for enabling single slot parallel mode which is latched during reset. SLOT[1] also functions as the HxPCIXCAP2A input when not in reset. SLOT2 also functions as the HxPCIXCAP1A input when not in reset. Refer to Table 8-15.
PxIRQ15[1] PxIRQ10[1]	• 8.2Ω – 10 kΩ pull-up to 3.3 V.	• A logic 1 on this pin indicates to the controller that the PCI slot should be immediately powered off. This signal is also connected to a SPST switch to ground which when pressed indicates by means of a logic 0 that the slot can be powered on.
PxIRQ[9:8][1] PxIRQ[14:11][1]	• 8.2 kΩ ± 5% pull-up to 3.3 V.	• These signals are mapped to Hot-Plug functions in dual-slot Hot-Plug mode.
PxSID[1]	• 8.2 kΩ ± 5% pull-down to ground.	• This insures that the LED for slot B on busses A and B remain off during reset.
Hot-Plug – Serial Mode Specific		
HPx_SLOT[2:0][1]	• Pulled to 3.3 V or ground through an 8.2 kΩ ± 5% resistor depending on the number of PCI Hot-Plug slots to be enabled.	• Refer to Section 8.2.5.1.
Hot-Plug – Disabled		
HPx_SLOT[2:0]	• 8.2 kΩ ± 5% pull-down to ground.	• HPx_SLOT[2:0] signals should be strapped to zero to disable Hot-Plug mode.
HPx_SID	• 8.2 kΩ ± 5% pull-up to 3.3 V or pull-down to ground.	• Unused inputs should not float.
HPx_SIC HPx_SIL# HPx_SOR# HPx_SORR# HPx_SOC HPx_SOL HPx_SOLR HPx_SOD	• If disabling Hot-Plug mode, these signals can be left as no connect.	
SMBus Interface		
SDTA SCLK	• 8.2 kΩ ± 5% pull-up to 3.3 V. Note that only one pull-up is needed per signals on the entire bus.	• Value of pull-up resistors determined by line load, from Section 9.5.4.

Table 13-4. Intel® P64H2 Schematic Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments
Power Decoupling Requirements		
VCC (1.8 V)	• Eight 0.1 µF capacitors near the P64H2. • Two 4.0 µF capacitors near regulator.	• Refer to Section 11.5.2.
VCC1_8	• Two 1.0 µF capacitors near the P64H2. • One 100.0 µF capacitors near regulator.	• Refer to Section 11.5.2.
3.3 V	• Twenty 0.1 µF capacitors near the P64H2. • Six 1.0 µF capacitors near the P64H2. • Two 4.0 µF capacitors near regulator. • One 100.0 µF capacitors near regulator.	• Refer to Section 11.5.2.
VCC5REF	• Connect to 5 V Power Supply.	• 5 V.
Power Sequencing Requirements		
1.8 V and CLK66	• 1.8 V must be valid before first CLK66 pulse.	• Refer to Section 11.5.4.
1.8 V and 3.3 V	• 1.8 V must drop before 3.3 V.	• Refer to Section 11.5.4.
PWRGD to PCIRST#	• PCIRST# must lag PWRGD by 100 ms. • PCIRST# must deassert with 60 ns of MCH reset.	• Refer to Section 11.5.3
Miscellaneous Signals		
BPCLK100 BPCLK133	• These can be left as no connects.	
CLK200 CLK200#	• 8.2 kΩ ± 5% pull-up to 3.3 V.	
TP0	• 8.2 kΩ ± 5% pull-up to 3.3 V.	
TEST#	• 8.2 kΩ ± 5% pull-up to 3.3 V.	
RASERR#	• 8.2 kΩ ± 5% pull-up to 3.3 V.	

NOTE:

1. x = A or B

13.5 CK408 Schematic Checklist

For additional information, refer to the *CK408 Clock Synthesizer/Driver Specification* and your component's datasheet.

Table 13-5. CK408 Schematic Checklist

Checklist Items	Recommendations	Reason/Impact
V3_CLK, V3_CLKA	• Isolate from the 3.3 V power plane and use extra decoupling.	• Refer to Section 4.7.
66BUFF[2:0]	• Connect to an Intel® P64H2 using a series 43 Ω ± 5% resistor.	• Refer to Section 4.2.
66IN	• No Connect.	
3V66_0	• Connect to Intel® ICH3-S using a series 43 Ω ± 5% resistor.	• Refer to Section 4.2.
3V66_1_VCH	• Connect to MCH using a series 43 Ω ± 5% resistor.	• Refer to Section 4.2.
CPU[3:0] CPU[3:0]#	• Connect to the processor, MCH, or ITP using a series 33 Ω ± 5% resistor, and terminate to ground through a 49.9 Ω ± 1% resistor. On the ITP port, use a 10 kΩ ± 5% pull-up resistor to V3_CLK close to CK408B.	• Refer to Section 4.1.
DOT_48MHz	• No Connect.	
IREF	• 475 Ω ± 1% pull-down to ground.	
MULT0	• 10 kΩ ± 5% pull-up to V3_CLK.	
PCI[4:0]	• Connect to a series 33 Ω ± 5% resistor for PCI33_CLK33, VIDEO_CLK33, FWH_CLK33, SIO_CLK33, and LPC_CLK33.	• Refer to Section 4.4.
PCI[6:5]	• No Connect.	
PCIF[0]	• Connect to a series 33 Ω ± 5% resistor for ICH3_CLK33.	• Refer to Section 4.3.
PCIF[2:1]	• No Connect.	
PCI_STOP#	• 10 kΩ ± 5% pull-up to V3_CLK.	
PWRDWN#	• Connect to SLP_S3_N.	
REF0	• Connect to a series 22 Ω ± 5% resistor for CLK 14 output to LPC, VIDEO, SIO, and ICH3-S.	• Refer to Section 4.5.
S[1]	• Connect to Processor 0 BSEL0.	• Refer to Section 5.6.3.
SCLK, SDTA	• Connect to 3.3 V SMBus partition.	
USB_48MHz	• Connect to ICH3-S using a 33 Ω ± 5% series resistor to ICH3 CLK48 pin.	• Refer to Section 4.6.
VDD, VDD_48MHz, VDDA	• Terminate to V3_CLK_A.	• Refer to Section 4.8.
VSS, VSS_48MHz, VSS_IREF	• Terminate to ground.	• Refer to Section 4.8.
VTT_PWRGD#	• Do not enable until Processor 0 is driving valid BSEL.	• Refer to Section 11.2.6.
XTAL_IN XTAL_OUT	• Terminate to ground.	

13.6 SSI Schematic Checklist

For additional information, refer to the *Intel® Xeon™ Processor and Intel® E7501 Chipset Server System Design Guide* and the *SSI EEB Specification*.

Table 13-6. SSI Schematic Checklist

Checklist Items	Recommendations	Reason/Impact
Main Power Connector	• Use a 24 pin Molex 44472 family connector or equivalent • Refer to Table 3-3 for pinout.	• *SSI EEB Specification*, Section 5.3.1.2
+12 Volt Power Connector	• Use an 8 pin Molex 44472 family connector or equivalent • Refer to Table 3-4 for pinout.	• *SSI EEB Specification*, Section 5.3.1.3
Auxiliary Connector	• Use a 5 pin Molex 70545 family connector or equivalent • Refer to Table 3-5 for pinout.	• *SSI EEB Specification*, Section 5.3.1.4
Cooling Fan Connector	• Use a 3 pin AMP 644953-3 connector or equivalent • Refer to Table 3-6 for pinout.	• *SSI EEB Specification*, Section 5.3.4

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Layout Checklist 14

All trace width and spacing recommendations are derived from a target impedance and crosstalk sensitivity. This is based upon the stackup defined in Section 3.1. Any deviation from this stackup must be simulated.

14.1 Processor Checklist

Table 14-1. Processor Layout Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments
A20M# IGNNE# INIT# LINT0/INTR LINT1/NMI SMI# SLP# STPCLK#	• Trace impedance = 50 Ω ± 10%. • Route traces using 5/10-mil spacing. • Try to keep signals on the same layer for the whole bus, but not at expense of AGTL+ Source Synchronous I/O. • Maximum agent to agent length is 10". Place pull-up resistor within 3" of Processor 1.	• Asynchronous GTL+ Input Signals. • Refer to Section 5.3.6.
A[35:3]#[1] ADSTB[1:0]#[2] DSTBN[3:0]#[3] DSTBP[3:0]#[4] DBI3:0]# D[63:0]#[5] REQ[4:0]#[6]	• Trace impedance = 50 Ω ± 10%. • Route Strobes 5/25 and others 5/15. • Route all signals as groups, on the same layer (do not change layer), and balance within group ± 25 mils with respect to the strobe. • The distance from processor pin to processor pin is between 3.0" and 7.0". • The distance from processor pin to MCH pin is between 3.0" and 6.5". • Do not route a stub to Processor 1.	• AGTL+ Source Synchronous I/O. • Refer to Section 5.1.
ADS# AP[1:0] BINIT# BNR# BR0# DBSY# DP[3:0]# DRDY# HIT# HITM# LOCK# MCERR# BPRI# BR[3:0]# DEFER# RESET#[7] RS[2:0]# RSP# TRDY#[8]	• Trace impedance = 50 Ω ± 10%. • Route traces using 5/15-mil spacing. • May change layers throughout the bus. • Route traces with at least 50% of the trace width directly over a reference plane. • The distance from processor pin to processor pin is between 3.0" and 7.0". • The distance from processor pin to MCH pin is between 3.0" and 6.5". • Do not route a stub to Processor 1. • Total bus length must not exceed 13.5".	• AGTL+ Common Clock Signals. • Refer to Section 5.2.
BCLK[1:0]	• BCLKs to all processors should be length matched, and the BCLK to the MCH should be offset accordingly. See Table 4-3.	• System Bus Clock. • Refer to Section 4.1.

Table 14-1. Processor Layout Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments
BPM[5:0]#		• For all ITP interface signal schematic, layout and routing recommendations, refer to the *ITP700 Debug Port Design Guide*.
FERR#/PBE# IERR# PROCHOT# THERMTRIP#	• Connect to both processors and ICH3-S. • Trace impedance = 50 Ω ± 10%. • Route traces using 5/15-mil spacing. • Try to keep signals on the same layer for the whole bus, but not at expense of AGTL+ Source Synchronous I/O. • Maximum agent to agent length is 10". Place pull-up resistor within 3" of Processor 1 and ICH3-S.	• Async GLT+ Output. • Refer to Section 5.3.2.
COMP[1:0] ODTEN SKTOCC# TESTHI[6:0] VID[4:0]	• There are no routing requirements for these signals.	• Input. • Refer to Section 5.3.
Reserved	• Reserved signals must remain as a No Connect (NC).	
SM_ALERT# SM_CLK SM_DAT SM_EP_A[2:0] SM_TS_A[1:0] SM_WP	• There are no routing requirements for these signals.	• SMBus I/O. • Refer to Section 5.5.1.
VCCA	• To satisfy damping requirements, total series resistance in the filter (from VCC_CPU to the top plate of the capacitor) must be at least 0.35 Ω. It includes the minimum DCR of the inductor, and any resistance (routing or discrete components) between VCC_CPU and capacitor top plate. • The total maximum resistance cannot be greater than 1.1 Ω as measured from VCC (more specifically, the baseboard via that connects the PLL filter to the VCC plane) to the processor VCCA interposer pin. Also, maximum trace resistance from the filter capacitor to processor socket pin should be less than 0.02 Ω.	• An isolated power for internal PLL. • Refer to Section 11.2.7.
VSSA VCCIOPLL	• There are no routing requirements for these signals.	• Refer to Section 11.2.7.
VCCSENSE VSSSENSE	• Route traces using 5/15-mil spacing. • Place via next to the processor socket's pin for measurement of VCC_CPU/VSS.	• Refer to Section 11.2.2.

NOTES:
1. A[35:3]# pins on the processor correspond to HA[35:3]# pins on the MCH.
2. ADSTB[1:0]# pins on the processor correspond to HADSTB[1:0]# pins on the MCH.
3. DSTBN[3:0]# pins on the processor correspond to HADSTBN[3:0]# pins on the MCH.
4. DSTBP[3:0]# pins on the processor correspond to HADSTBP[3:0]# pins on the MCH.
5. D[63:0]# pins on the processor correspond to HD[63:0]# pins on the MCH.
6. REQ[4:0]# pins on the processor correspond to HREQ[4:0]# pins on the MCH.
7. The RESET# pin on the processor corresponds to the CPURST# pin on the MCH.
8. The TRDY# pin on the processor corresponds to the HTRDY# pin on the MCH.

14.2 Processor Power Delivery Layout Checklist

All recommendations in this checklist apply to the power distribution design of the processor's "VCC_CPU" and ground supply. This checklist assumes the voltage regulator solution adheres to the guidelines documented in either the *VRM 9.1 DC-DC Converter Design Guidelines* or *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines* depending on which solution is implemented.

Table 14-2. Processor Power Delivery Layout Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments
Power / Ground Plane Copper Weight	• Use at least 2 oz total copper for the combined weight of all processor power planes (VCC_CPU). • Use at least 2 oz copper for the combined weight of all processor ground planes. • These layers can be implemented using two 1 oz copper layers or four ½ oz copper layers.	• Refer to Section 11.2.2.
Power / Ground Plane Geometry	• The power / ground supply to both processor sockets can be distributed as a dedicated layer of the PCB, a voltage supply plane with other power islands, or an island on a signal layer. • Never distribute processor power with traces. • Do not route capacitors to the processor socket using traces. • The island or plane connecting the Voltage Regulator Module (VRM) or Voltage Regulator Down (VRD) supply to both processor sockets should not have any breaks or voids.	• A "trace" is any etch that is less than the width of the processor socket.
Power / Ground Plane Processor Socket Breakout	• The power / ground planes should completely surround all of the pins of the VRM or VRD and processor socket. • Minimize the size of the processor socket vias anti-pads where possible. Anti-pads should be no larger than 35 mils. • Locations of the capacitor pads on the outer power layer should not hinder power distribution by creating a "slot"-shaped geometry in the plane. • Avoid vias around the socket breakout area as much as possible.	• Refer to Section 11.2.2. • Section 11.2.2 contains an example of good socket power / ground plane routing for an inner layer.
Voltage Regulator Placement and Sense / Feedback Lines		
VRM-based topology	• Use the "Row" pattern topology.	• Refer to Section 11.2.4.
VRD-based topology	• Use the "L" pattern or "Row" pattern topology.	• Refer to Section 11.2.5.1
VRD sense point	• Route the VRD's voltage sense input signal to the middle of the VCC_CPU plane. The location of this plane connection and route is not critical.	• Refer to Section 11.2.5.3.

Table 14-2. Processor Power Delivery Layout Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments
Power / Ground Planes		
VRM VO-sen+ / VO-sen- remote sense	• If available on the VRM, route the VR's differential remote sense input signals to the middle of the VCC_CPU plane. • Route the positive feedback line to a point on the VCC_CPU power plane in the middle of and equidistant from both processors. Route the negative feedback line to the corresponding X-Y location, but on the VCC_VSS ground plane. • The traces should be carefully routed to avoid picking up noise • They must affect less than 1 Ω round-trip resistance to minimize the voltage drop between the sense point and VR input. • Route each of the feedback lines with less than 5 inches total trace length. Do not route near signal lines unless shielding is provided.	• Refer to Section 11.2.4 for an example of sense point locations for the example VRM topology. • Middle is defined as a point that provides the shortest geometrical mid-point between the centers of the processor sockets.
VRD voltage feedback	• Route the positive (and negative if the VRD provides differential inputs) voltage feedback inputs for the VRD to the VCC_CPU plane with the following conditions. • They must be connected to the power plane through a series resistor. This resistor should be sized to provide the correct droop to satisfy the load line requirement. • They must affect less than 1 Ω round-trip resistance to minimize the voltage drop between the sense point and VR input. • Route the positive feedback line to a point on the VCC_CPU power plane in the middle of and equidistant from both processors. • Route the negative feedback line to the corresponding X-Y location, but on the VCC_VSS ground plane. • Route each of the feedback lines with less than 5 inches total trace length. Do not route near signal lines unless shielding is provided. • The trace(s) should be carefully routed to avoid picking up noise.	• Refer to Section 11.2.5 for an example of sense point locations for the example VRD topologies. • Contact your VRD component vendors for their specific recommended implementation. Refer to the applicable CRB schematics for feedback details specific to these platforms and specific VRD solution used. The recommendations included in this entry are generic. • Middle is defined as a point that provides the shortest geometrical mid-point between the centers of the processor sockets.
VCCSENSE / VSSSENSE	• Do not connect the VRD / VRM inputs to the processor VCCSENSE / VSSSENSE signals.	• Refer to Section 11.2.2. • These processor SENSE signals are measurement points used for processor power validation purposes only. • Connecting these processor signals to the VRD/VRM will result in incorrect VRD/VRM sensing operation.

Table 14-2. Processor Power Delivery Layout Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments
Voltage Regulator Down Circuit Implementation (for VRD designs only!)		
Loadline Selection Circuit	• For designs based on a VRD solution, the system must include loadline selection circuitry that adjusts the voltage regulator's loadline output (offset and slope) based on whether one or two processors are installed.	• Section 11.2.5.2 shows example logic that supports this function without the use of jumpers.
Low-pass filter on output of MOSFET phases	• Include an RC filter at the output of each of the four MOSFET phases. The exact value will depend on the actual voltage regulator Pulse Width Modulation (PWM) controller component and MOSFETs used.	• Refer to Section 11.2.5.3. • Contact your VRD component vendors for their suggested implementation.
Series inductors on output of MOSFET phases	• Include series inductors at the output of each of the four MOSFET phases. Exact value will depend on the actual VR components used.	• Refer to Section 11.2.5.3. • Contact your VRD component vendors for their suggested implementation. Refer to the applicable CRB schematics for inductor values specific to these platforms and VRD solution.
Switching frequency	• Carefully select the switching frequency of the PWM controller for each of the four MOSFET phases.	• Refer to Section 11.2.5.3. • Contact your VRD component vendors for their suggested implementation. Refer to the applicable CRB schematics for details on the switching frequency setting specific to these platforms and VRD solution.
Decoupling Capacitors		
OSCON decoupling capacitors and placement	• Use at least ten, 560 µF OSCON capacitors per processor socket. Place half on one side of the processor socket, half on the other side as close as the logic analyzer interface (LAI), retention mechanism (RM) and heatsink keep-out zones allow. Capacitors should be placed a maximum of 0.5 inch from the processor socket.	• Refer to Section 11.2.9.2 for placement examples. • Check with your LAI, RM and heatsink vendor for those keep-out zone requirements. When using the Intel Xeon processor boxed processor solution, refer to the *Intel® Xeon™ Processor Datasheet* for keep-out zone details.

Table 14-2. Processor Power Delivery Layout Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments
1.0 µF and 22.0 µF decoupling capacitor quantity and placement	• Use at least twenty, 22.0 µF ceramic capacitors per processor socket. • Use at least eight ,1.0 µF ceramic capacitors per processor socket. • Place one quarter of the caps on one side of the processor socket, one quarter on the other side, and half in the processor socket cavity if using both sides of the motherboard. • If using single-sided motherboards, place as close to half the total quantity as possible, and place the remaining caps on the outside of the socket. • Place capacitors as close to the power/ ground pins of the processor socket as physically possible. • Place capacitor vias within their pad. If this technology is not feasible, then keep traces between the pad and via as short and as wide as feasible. Possibly one or both ends of the capacitor may be connected directly to the processor socket pin without the use of a via • Microstrip configurations require additional decoupling capacitors.	• Refer to Section 11.2.9.1. • Refer to the *Intel® Xeon™ Processor Datasheet* for the processor pinout.
0.1 µF decoupling capacitor quantity and placement	• Distribute four minimum (six preferred) 0.1 µF capacitors evenly across the VCC_CPU / ground pins that are located in the portion of the processor socket pinout where system bus data lines are located. • Distribute three minimum (four preferred) 0.1 µF capacitors evenly across the VCC_CPU / ground pins that are located in the portion of the processor socket pinout where address and common clock signals are located. • Place all capacitors as close to the power/ ground pins of the processor socket as physically possible. • Place capacitor vias within their pad. If this technology is not feasible, then keep traces between the pad and via as short and as wide as feasible. Possibly one or both ends of the capacitor may be connected directly to the processor socket pin without the use of a via.	• Refer to Section 11.2.9.1 for a placement example. • Refer to the *Intel® Xeon™ Processor Datasheet* for the processor pinout.

14.3 MCH Layout Checklist

Table 14-3. MCH Layout Checklist (Sheet 1 of 3)

Checklist Items	Recommendations	Comments
Host Interface		
ADS# AP[1:0] BINIT# BNR# BPRI# BREQ0#[1] CPURST#[2] DBSY# DEFER# HA[35:3]#[3] HD[63:0]#[4] HADSTB[1:0]#[5] HDSTBN[3:0]#[6] HDSTBP[3:0]#[7] HIT# HITM# HLOCK# HREQ[4:0]#[8] HTRDY#[9] DP[3:0]# DRDY# RS[2:0]# RSP# XERR#[10] DBI[3:0]#	• See processor section of this checklist.	
DDR Interfaces A & B / Connector		
General Guidelines	• 5 on 15 is maintained for Data/Strobe/ CMD signals; 5 on 7.5 is maintained for CMDCLK_x/CMDCLK_x# signals. • If using the recommended stack-up, outer layer routing of DDR signals should be kept to a minimum (except for reference voltages). Via up close to passive devices, and immediately via back down following the device. • Try to maintain same ground reference when transitioning layers—add stitching via if reference plane changes. • Connect termination resistors directly to termination plane (flood is on outer layer). • Space traces out as much as possible through the DIMMs.	
DQ_x[63:0] CB_x[7:0] DQS_x[17:0]	• Route entirely on the same layer from MCH to DIMM to termination (no layer transitions). Place the series resistor < 800 mils from the first DIMM connector. All signals in a data group must be length matched to the associated DQS within ± 25 mils. Place termination resistor within 800 mils from the last DIMM connector.	• Refer to Section 6.2.

Table 14-3. MCH Layout Checklist (Sheet 2 of 3)

Checklist Items	Recommendations	Comments
RAS_x# CAS_x# WE_x# MA_x[12:0] BA_x[1:0]	• Place termination resistor within 800 mills from last DIMM connector. No more then 2 vias/layer transitions, not including breakout and passive devices.	• Refer to Section 6.4.
CS_x[7:0]#	• Place termination resistor within 1.5" from the connector.	• Refer to Section 6.5.
CMDCLK_x[3:0] CMDCLK_x[3:0]#	• Clock signals within a differential pair must be matched to each other within ± 2 mils. These signals must be routed 5 on 7.5, and must be at least 20 mils away from any other signal. Use exact lengths as defined in Table 6-5.	• Refer to Section 6.3.
CKE_x	• Route 40 Ω using a 7.5-mil wide trace. The CKE signal must be length matched to the clock signal at each DIMM within 2 inches. Place termination resistor within 800 mils from last DIMM connector. If routing creates stubs, keep the stub length less than 300 mils.	• Refer to Section 6.6.
RCVENIN_x# RCVENOUT_x# RCVEN_x	• Route 50 Ω using a 5-mil wide trace with 15-mil wide spacing. Use topology in Figure 6-12.	• Refer to Section 6.7.1. • RCVENIN_x# and RCVENOUT_x# are on the E7500 chipset MCH and RCVEN_x is on the E7501 chipset MCH.
DDRCOMP_x	• Route 15-mil wide trace with 20-mil wide spacing. Place pull-up resistor within 1 inch of the MCH.	• Refer to Section 6.7.2.
DDRCVOL_x DDRCVOH_x DDRCVO_x	• Route 15-mil wide trace with 20-mil wide spacing. Place resistive network within 1 inch of the MCH.	• Refer to Section 6.7.4. • DDRCVOL_x and DDRCVOH_x are on the E7500 chipset MCH and DDRCVO_x is on the E7501 chipset MCH.
DDRVREF_x	• Place a 0.1 µF capacitor next to each MCH pin.	•
Decoupling	• Spread termination decoupling capacitors evenly around the termination plane. • Spread 2.5 V decoupling capacitors evenly around the DIMMs.	• Refer to Section 6.9.
Hub Interfaces		
General Guidelines	• Hub interface spacing of 5 on 15 for data, and 5 on 35 for strobes. • Space signals out as much as possible on breakout from the BGA. • Hub interface data group signals are routed on the same layer, transitioning together if a layer change is required. • Maximum length of 20" (stripline routing). • Length match Hub Interface 2.0 strobes within 1" from data. Length match according to Figure 7-2. • Hub Interface 1.5: Length match data ± 100 mils and strobes exactly.	• Refer to Section 7.2.1 and Section 7.3.1of this document.

Table 14-3. MCH Layout Checklist (Sheet 3 of 3)

Checklist Items	Recommendations	Comments
HIRCOMP_x HIVREF_[D:A] HISWNG_[D:A]	• RCOMP, VSWING, VREF resistor networks are less than 1” away from the MCH. • VSWING, VREF trace width is greater than 15 mils. • HIRCOMP_x must have a 50 Ω impedance.	• Refer to Section 7.2.2, Section 7.2.3, Section 7.3.2, and Section 7.3.3.
Clocks, Reset, Miscellaneous Signals		
HCLKINP HLCKINN	• HCLKs should be length matched to all processors BCLKs. See Table 4-3 for routing guidelines.	• Refer to Section 4.1.
CLK66	• Place series resistor close to CK408B.	• Refer to Section 4.2.
RSTIN#	• Connect to PCIRST# output of the Intel® ICH3-S.	
Miscellaneous Signals		
XORMODE#		
HXRCOMP HYRCOMP		• This signal is used to calibrate the Host AGTL+ I/O buffers characteristics to specific board characteristic. • Refer to Section 5.3.3.
Voltage References – Power Planes		
HDVREF[3:0] HAVREF[1:0] HCCVREF	• Use one dedicated voltage divider for all these signals. Decouple the voltage divider with a 1 µF capacitor.	• To provide constant and clean power delivery to the data, address, and common clock signals of the host AGTL+ interface. • Refer to Section 11.2.10.
DDRVREF_x[5:0]		• Refer to Section 6.7.
HXSWING HYSWING		• The HXSWING and HYSWING inputs of MCH are used to provide reference voltage for the compensation logic. • Refer to Section 5.3.3.
VCCA	• High-frequency decoupling for VCCA planes is located as close as possible to the associated MCH ball.	

NOTES:
1. The BREQ0# pin on the MCH corresponds to the BR0# pin on the processor.
2. The CPURST# pin on the MCH corresponds to the RESET# pin on the processor.
3. HA[35:3]# pins on the MCH correspond to A[35:3]# pins on the processor.
4. HD[63:0]# pins on the MCH correspond to D[63:0]# pins on the processor.
5. HADSTB[1:0]# pins on the MCH correspond to ADSTB[1:0]# pins on the processor.
6. HADSTBN[3:0]# pins on the MCH correspond to DSTBN[3:0]# pins on the processor.
7. HADSTBP[3:0]# pins on the MCH correspond to DSTBP[3:0]# pins on the processor.
8. HREQ[4:0]# pins on the MCH correspond to REQ[4:0]# pins on the processor.
9. The HTRDY# pin on the MCH corresponds to the TRDY# pin on the processor.
10. The MCH XERR# pin can be connected to the processor IERR# pin or the processor MCERR# pin.

14.4 Intel® ICH3-S Layout Checklist

Table 14-4. Intel® ICH3-S Layout Checklist (Sheet 1 of 4)

Checklist Items	Recommendations	Comments
Processor Signals		
A20M# CPUSLP# FERR# IGNNE# INIT# LINT[1:0] SMI# STPCLK#	• See processor section of this checklist.	
FWH Interface		
Decoupling	• 0.1 µF capacitors should be placed between the VCC supply balls and the VSS ground balls, and no less than 390 mils from the VCC supply balls. • 4.7 µF capacitors should be placed between the VCC supply balls and the VSS ground balls, and no less than 390 mils from the VCC supply balls.	
Hub Interface - See MCH section		
IDE Checklist		
General Guidelines	• Traces are routed 5-mil wide with 7-mil spacing. • Max trace length is 8 inches long. • The maximum length difference between the longest and shortest trace length is 0.5 inch.	• Refer to ATA ATAPI-4 specification. • Refer to Section 9.1.3.
LAN Interface		
General Guidelines	• Traces: 5 mils wide, 10-mil spacing.	• Refer to Section 9.7.
	• LAN Max Trace Length Intel® ICH3-S to CNR: L = 3" to 9" (0.5" to 3" on card).	• To meet timing requirements.
	• Stubs due to R-pak CNR/LOM stuffing option should not be present.	• To minimize inductance.
	• Maximum Trace Lengths: – ICH3-S to 82562EH: L = 4.5" to 10" – 82562ET: L = 3.5" to 10" – 82562EM: L = 3.5" to 10".	• To meet timing requirements.
	• Maximum mismatch between the length of a clock trace and the length of any data trace is 0.5" (clock must be the longest trace).	• To meet timing and signal quality requirements.
	• Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN phy.	• To meet timing and signal quality requirements.

Table 14-4. Intel® ICH3-S Layout Checklist (Sheet 2 of 4)

Checklist Items	Recommendations	Comments
General Guidelines, cont.	• Keep the total length of each differential pair under 4".	• Issues found with traces longer than 4": – IEEE phy conformance failures – excessive EMI and or degraded receive BER.
	• Do not route the transmit differential traces closer than 100 mils to the receive differential traces.	• To minimize crosstalk.
	• Distance between differential traces and any other signal line must be at least 100 mils. (300 mils recommended).	• To minimize crosstalk.
	• Route 5 mils on 7 mils for differential pairs (out of LAN phy).	• To meet timing and signal quality requirements.
	• Differential trace impedance should be controlled to be ~100 Ω.	• To meet timing and signal quality requirements.
	• For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, use two 45-degree bends.	• To meet timing and signal quality requirements.
	• Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	• This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
	• Do not route traces and vias under crystals or oscillators.	• This prevents coupling to or from the clock.
	• Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	• To control trace EMI radiation.
	• Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	• Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.
	• Vias to decoupling capacitors should be sufficiently large in diameter.	• To decrease series inductance.
	• Isolate I/O signals from high speed signals.	• To minimize crosstalk.
	• Avoid routing high-speed LAN or Phone line traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar device.	• To minimize crosstalk.
	• Place the 82562ET/EM part more than 1.5" away from any board edge.	• This minimizes the potential for EMI radiation problems.
	• Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the Intel® 82562ET/EM.	• Research and development has shown that this is a robust design recommendation.
	• Place decoupling capacitors (0.1 µF) as close to the 82562ET/EM as possible.	

Table 14-4. Intel® ICH3-S Layout Checklist (Sheet 3 of 4)

Checklist Items	Recommendations	Comments
Power Decoupling		
V_CPU_IO[2:0]	• Use one 0.1 µF decoupling capacitor. Locate within 100 mils of the ICH3-S processor interface balls.	• Used to pull-up all processor I/F signals.
VCC3_3	• Requires six 0.1 µF decoupling capacitors. Distribute around the ICH3-S package sides within 100 mils from the package balls: – Top near AUX/PCI – Left across the PCI and LPC – Bottom near IDE.	
VCCSus3_3	• Requires two 0.1 µF decoupling capacitors. Place one capacitor on the top side within 200 mils of the USB center. Place other on bottom side near the VCCSus3_3 supply.	
VCC1_8	• Requires four 0.1 µF decoupling capacitors. Locate two capacitors distributed local to the hub interface; within 50 mils of the package hub interface balls. Distribute remaining capacitors on the left and bottom sides of the package for core delivery.	
VCCSus1_8	• Requires one 0.1 µF decoupling capacitor. Locate within 200 mils of balls B23 and C23 of the ICH3-S.	
V5REF_Sus	• Requires one 0.1 µF decoupling capacitor.V5REF_Sus affects only 5-V tolerance for USB OC[5:0]# balls, and can be connected to VCCSus3_3 if 5 V tolerance on these signal is not required.	
V5REF	• Requires one 0.1 µF decoupling capacitor. V5REF is the reference voltage for 5-V tolerant inputs in the ICH3-S. Tie to balls V5REF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.	
RTC		
General Guidelines	• RTC ball to crystal termination trace length should be less than 1.0”. • Minimize capacitance between RTCX1 and RTCX2. • Put ground plane underneath Crystal components. • Do not route switching signals under the external components (unless on other side of board).	

Table 14-4. Intel® ICH3-S Layout Checklist (Sheet 4 of 4)

Checklist Items	Recommendations	Comments
USB		
General Guidelines	• Route all traces over continuous planes (ground) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.) • Keep traces at least 50 mils away from the edge of the reference ground plane. This helps prevent the coupling of the signal onto adjacent wires, and helps prevent free radiation of the signal from the edge of the PCB. • Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. (Recommended: 5 on 6 spacing with 4-layer 4.5-mil prepreg stack-up). • Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 20 mils, though it is recommended to keep clocks and PCI traces at least 50 mils from the USB differential pairs if possible. • Use 20 mil minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk. • USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as USBP2P and USBP2N) should be no greater than 150 mils. • No termination resistors needed for USB. ICH3-S has internal 15 kΩ resistors. • 47 pF parallel capacitors may be placed as close to the USB connector as possible.	

Schematics 15

This appendix contains a set of schematics for the Intel® Xeon™ processor / Intel® E7500/E7501 chipset compatible platform Customer Reference Board (CRB).

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Intel® Xeon™ Processor with 533 MHz System Bus/ Intel® Xeon™ Processor with 512-KB L2 Cache and Intel® E7500/E7501 Chipset Customer Reference Board Schematics

Rev 2.0

11/18/02

THESE SCHEMATICS ARE SUBJECT TO CHANGE.

TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD			REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630		DRAWN BY:	PROJECT: KC533
		LAST REVISED: 11/18/02	1 OF 85

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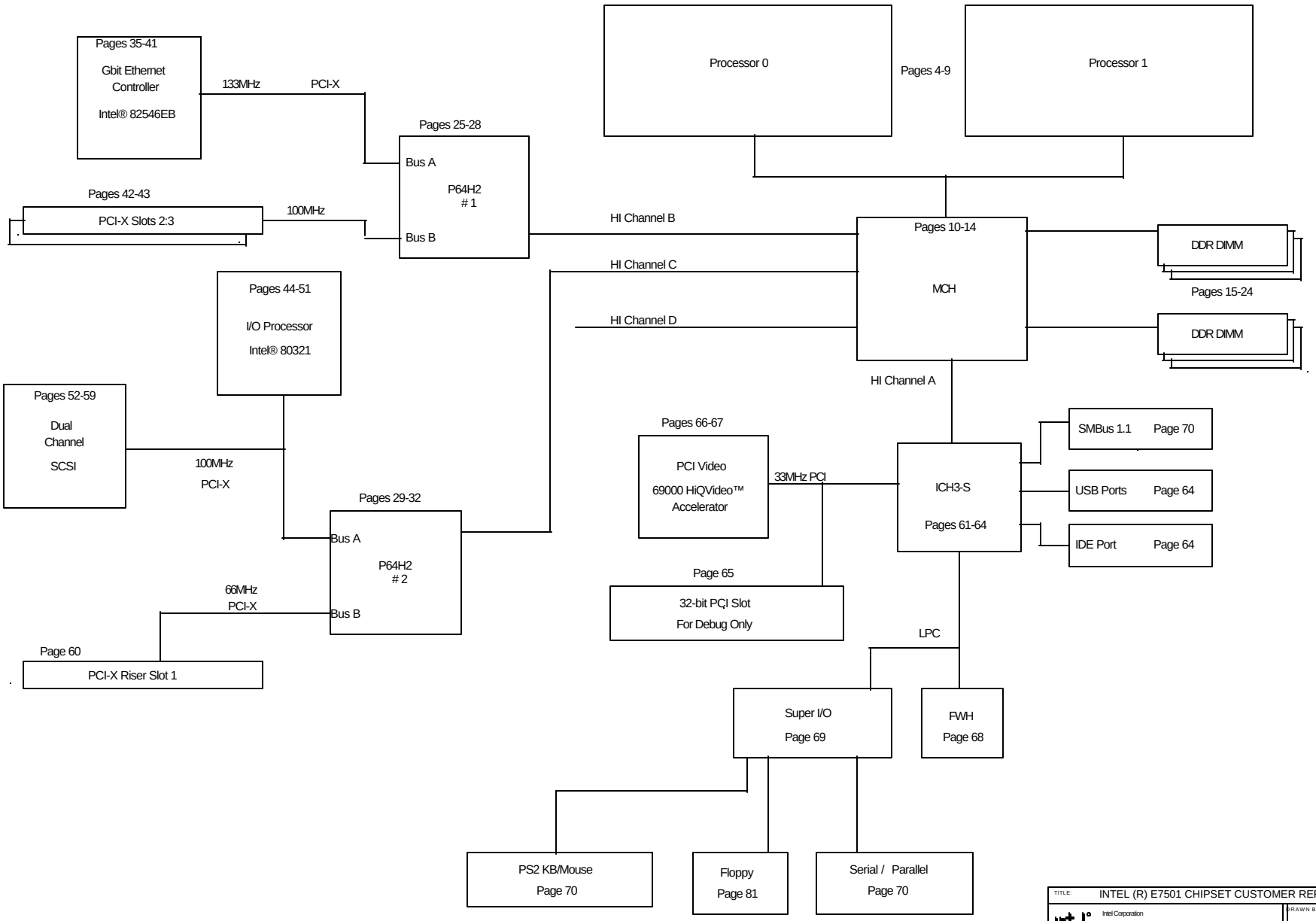
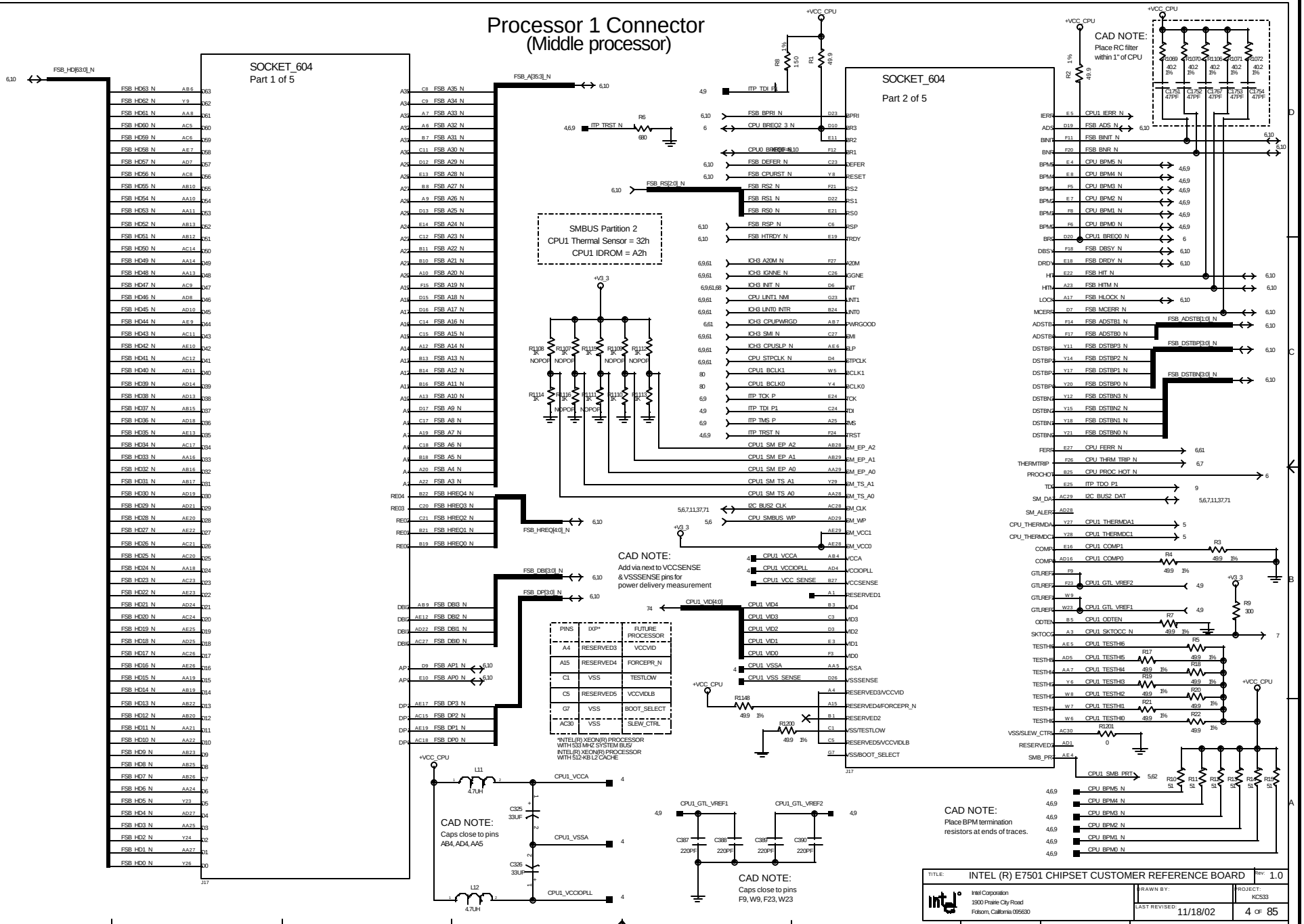
Intel Corporation 1900 Prairie City Road Folsom, California 095630		DRAWN BY:	PROJECT: KC533
		LAST REVISED: 11/18/02	2 OF 85

Simplified System Block Diagram

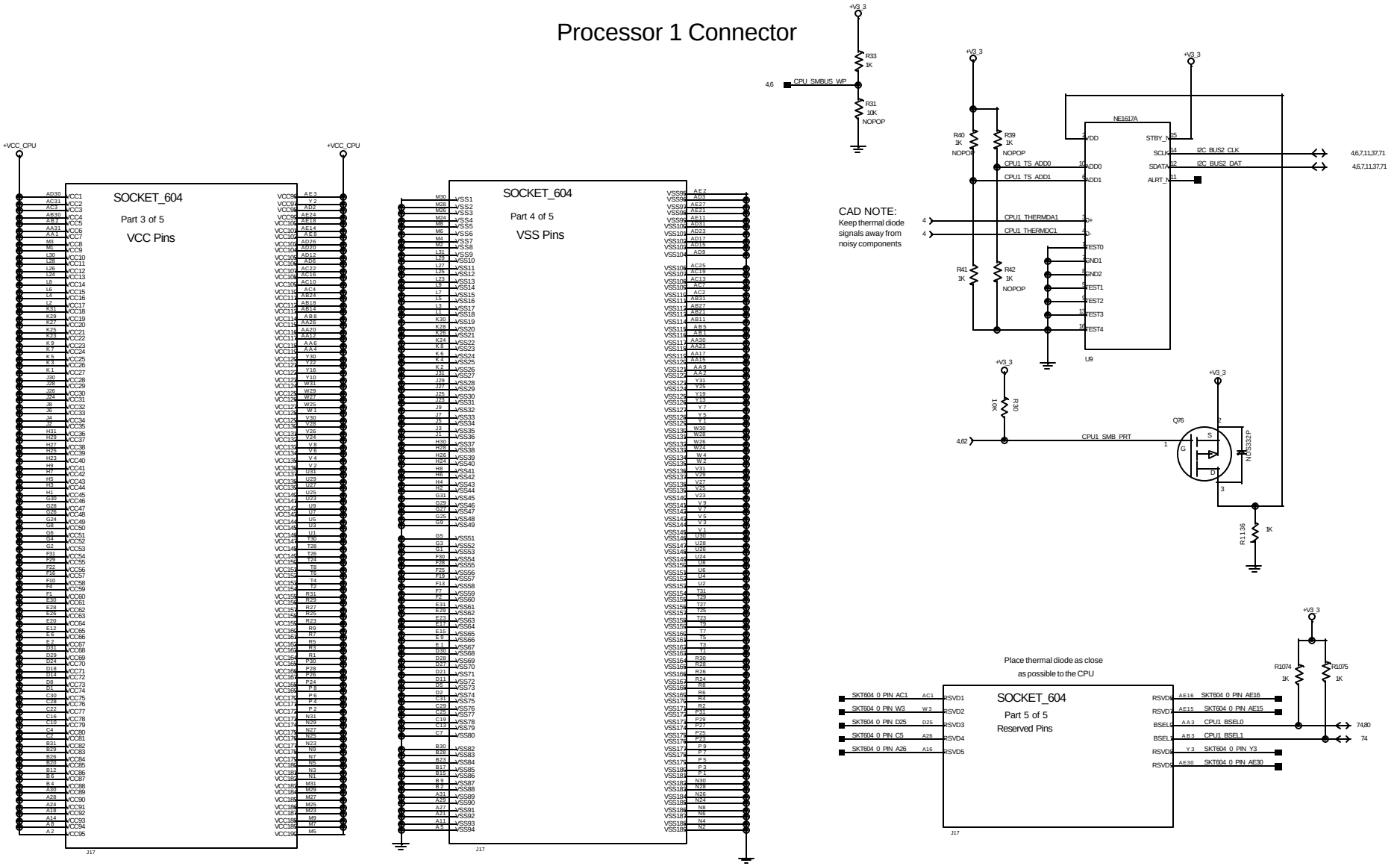


TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV.	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT:	KC533
	LAST REVISED: 11/18/02		3 OF 85

Processor 1 Connector
(Middle processor)



Processor 1 Connector



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SIZE:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	
DRAWN BY:	
PROJECT:	KC533
LAST REVISED:	11/18/02
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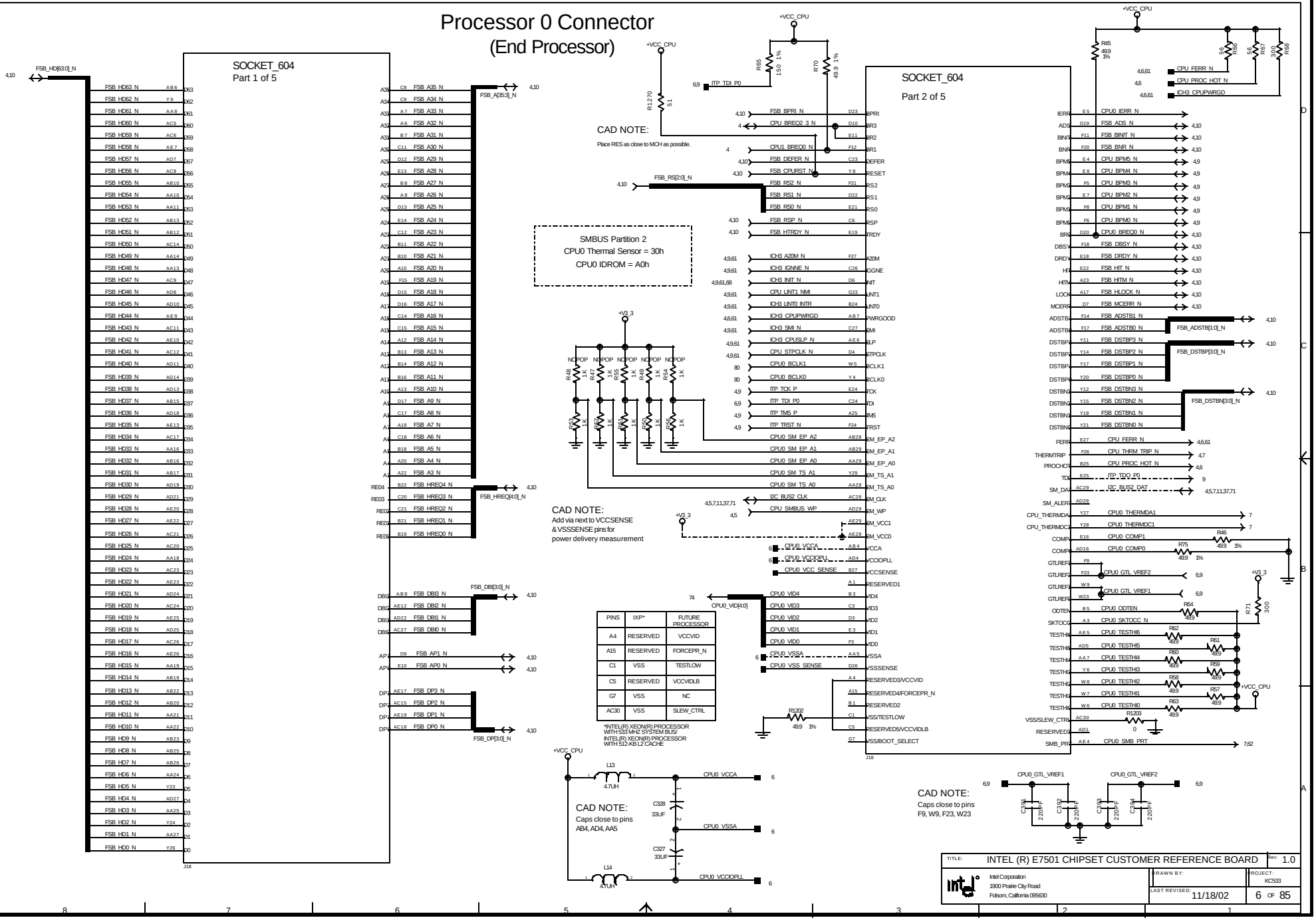
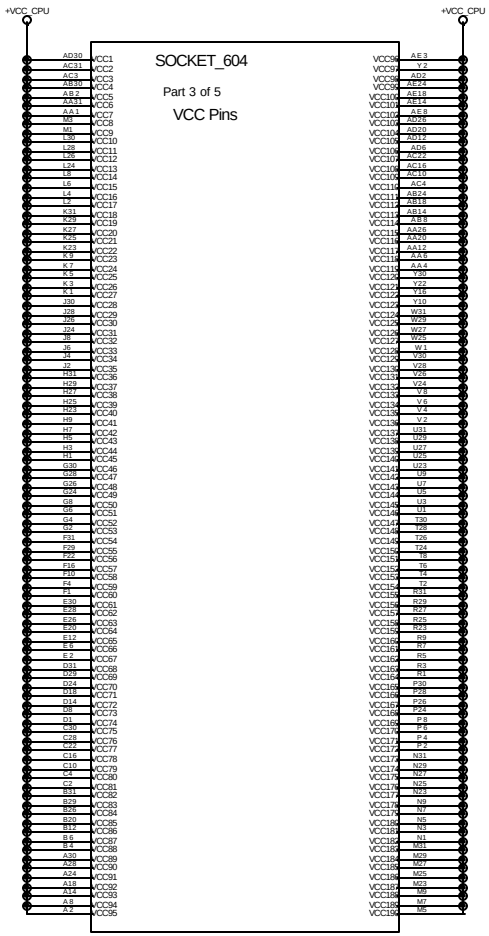
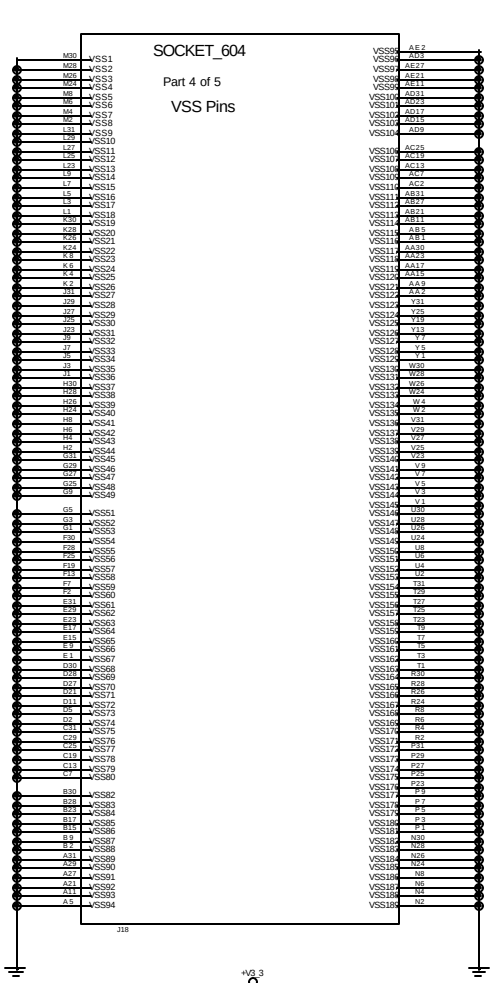
Processor 0 Connector
(End Processor)



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT:	KC533
	LAST REVISED: 11/18/02	6 OF 85	

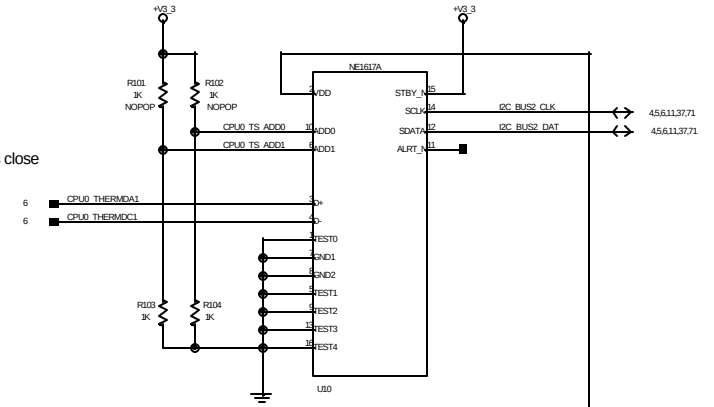
Processor 0 Connector

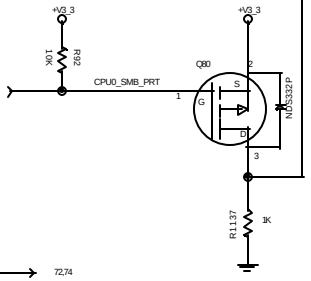


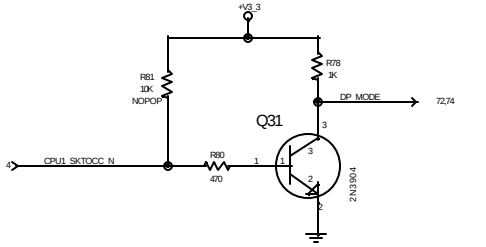


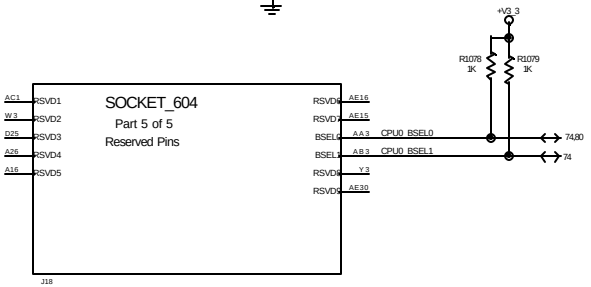
Place thermal diode as close as possible to the CPU

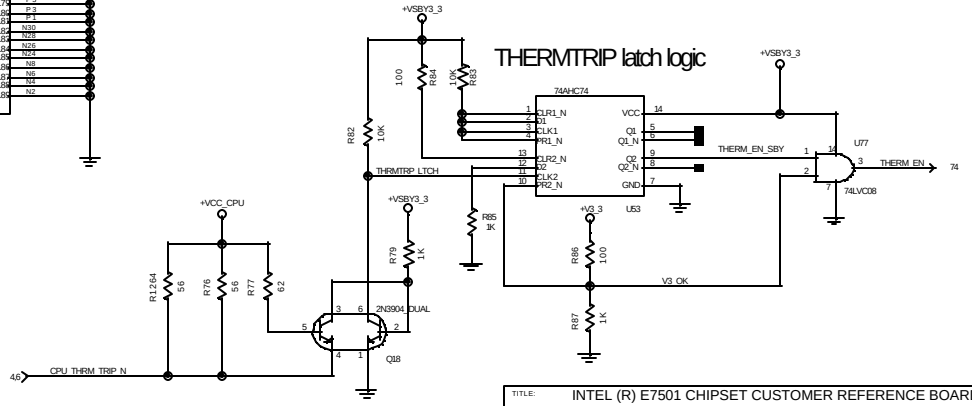
Keep thermal diode signals away from noisy components











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Intel Corporation 1900 Prairie City Road Folsom, California 095630	
DRAWN BY:	
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LAST REVISED:	11/18/02
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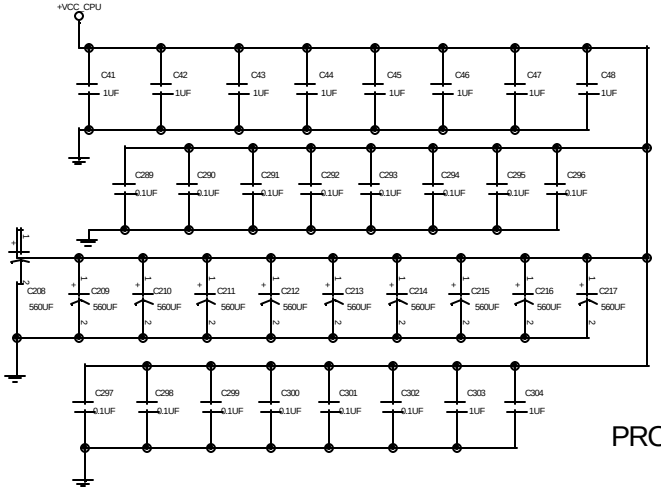
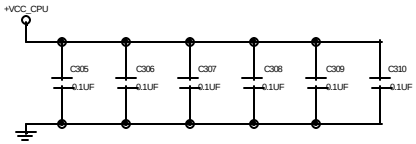
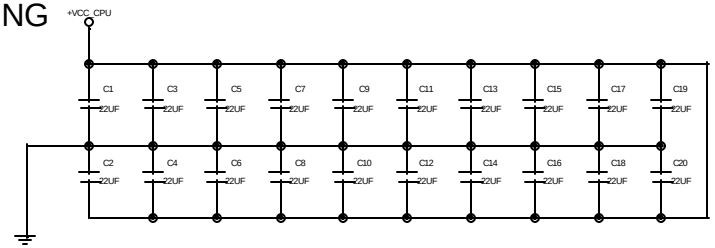
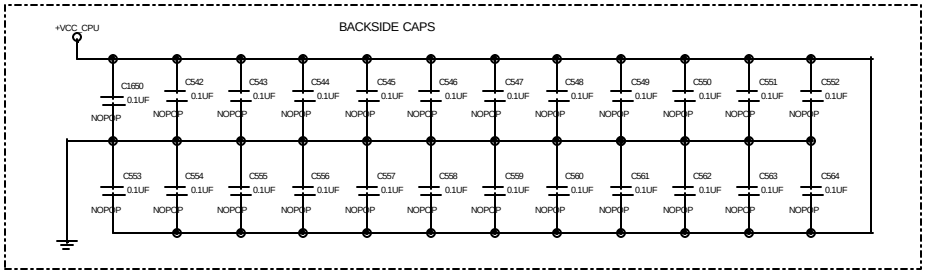
PROCESSOR 0 and 1 DECOUPLING

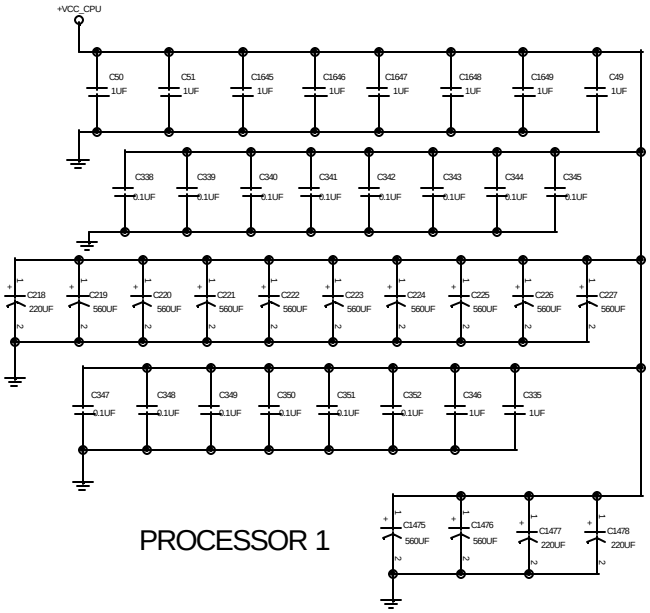


PROCESSOR 0

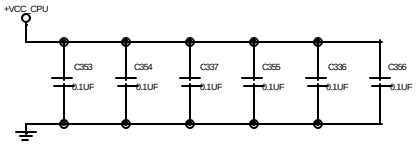


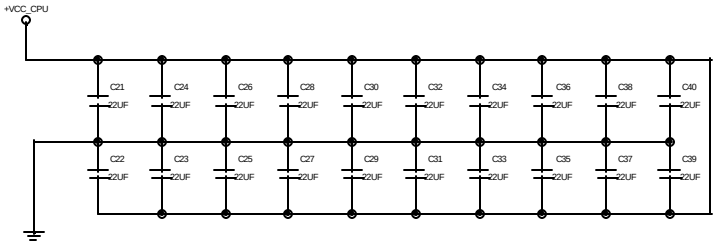


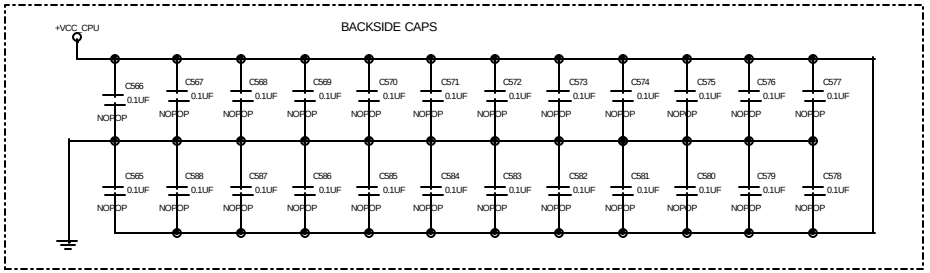




PROCESSOR 1



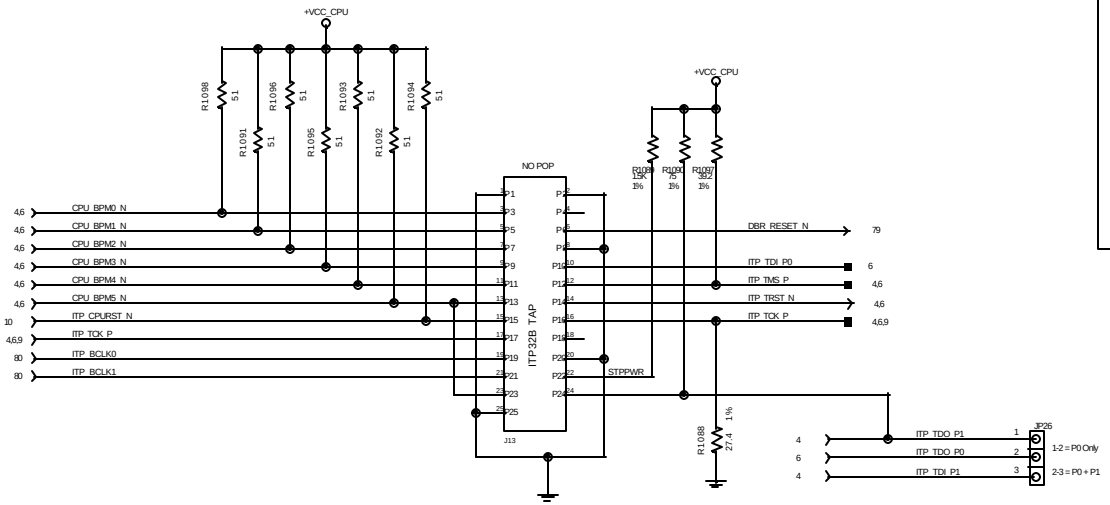


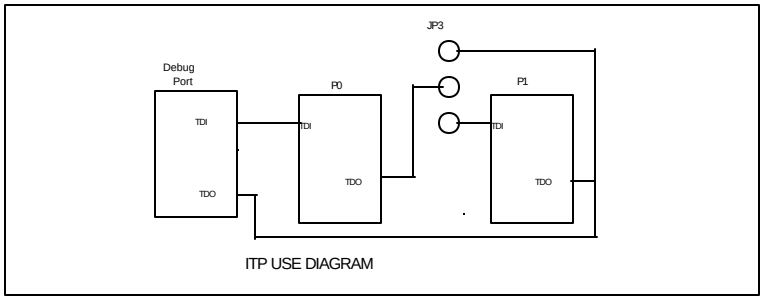


TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT:	KC533
	LAST REVISED: 11/18/02	8 OF 85	

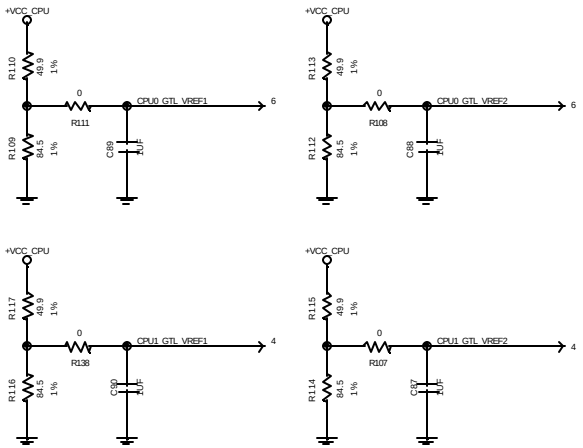
ITP

Place these termination
resistors at the ends of the traces.

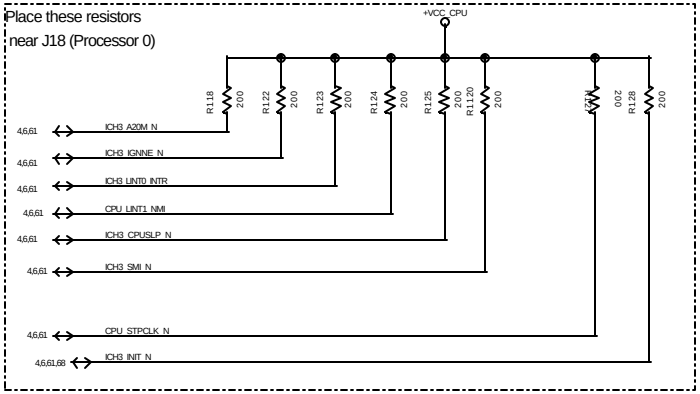




VREF circuits for GTL+



Place these resistors
near J18 (Processor 0)



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Intel Corporation	1900 Prairie City Road, Folsom, California 095630
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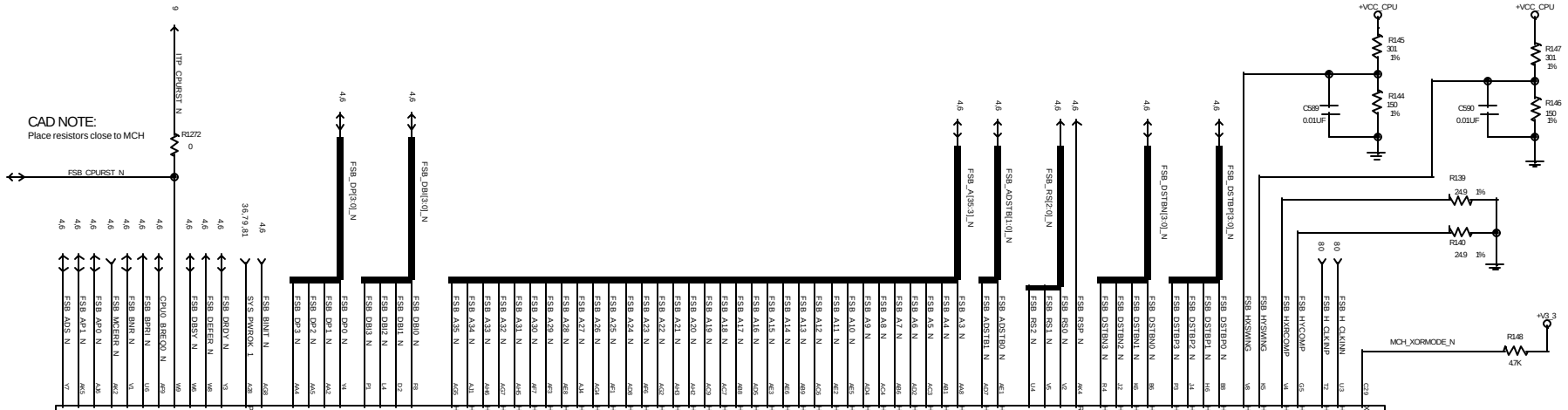
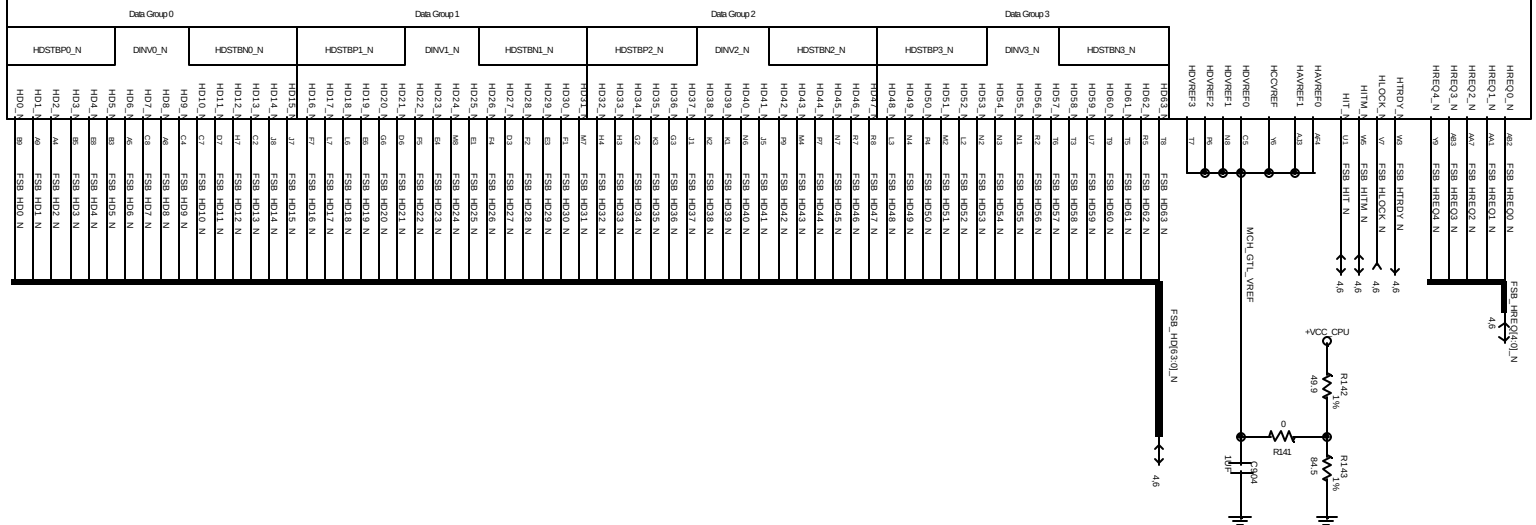
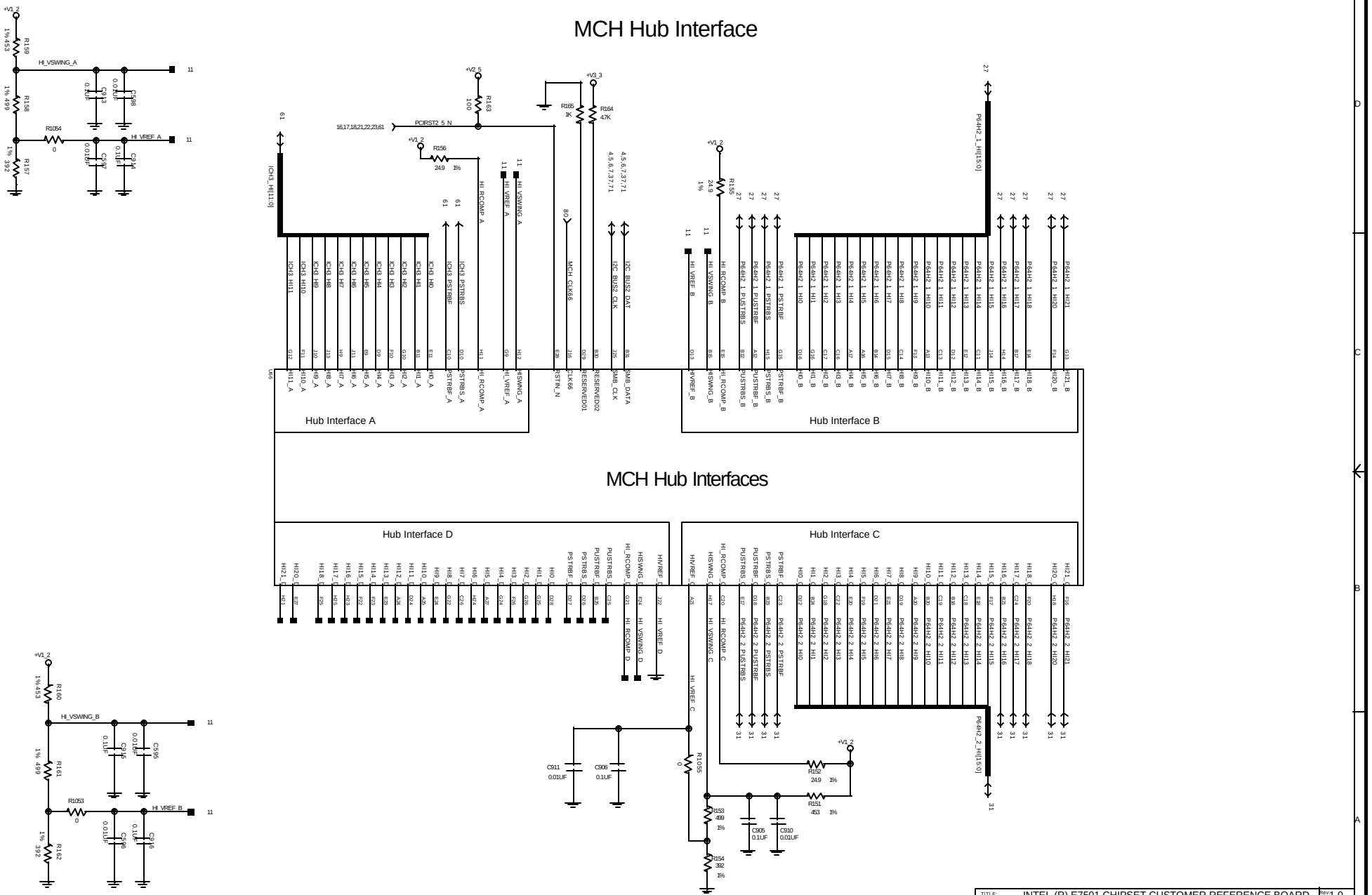
MCH System Bus



MCH System Bus I/F



MCH Hub Interface



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	Intel Corporation 1900 Prairie City Road Folsom, California 095630
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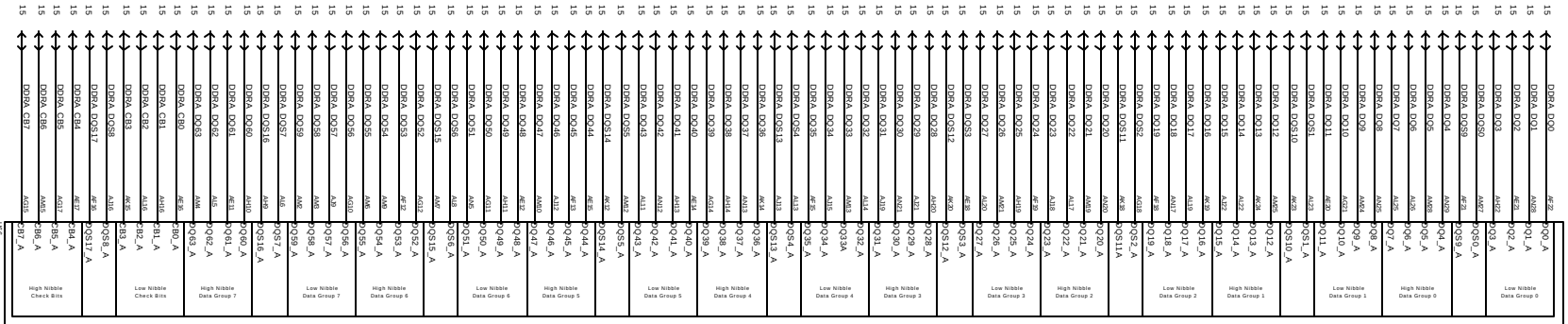
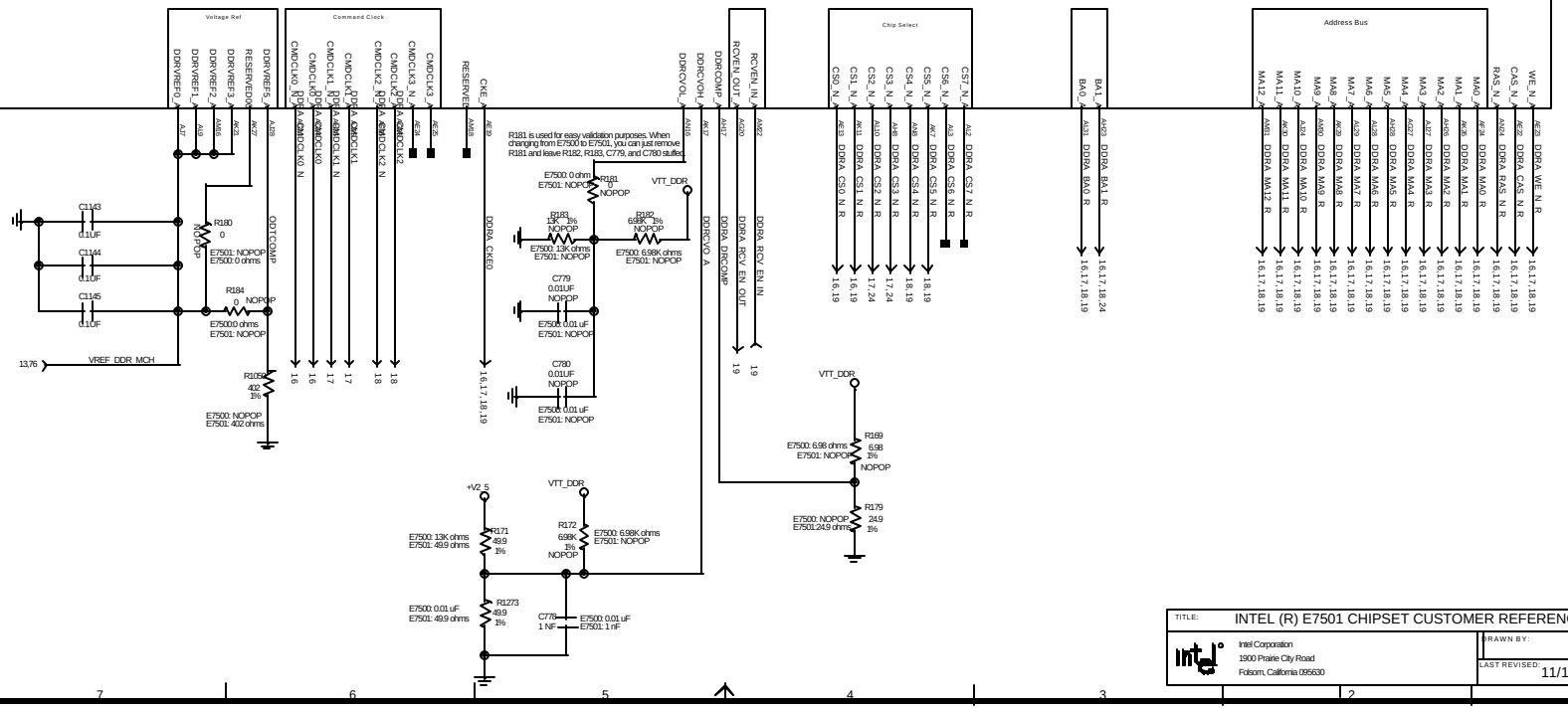
MCH DDR Channel A



MCH DDR A



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV:	1.0
Intel Corporation	1900 Prairie City Road, Folsom, California 095630
DRAWN BY:	
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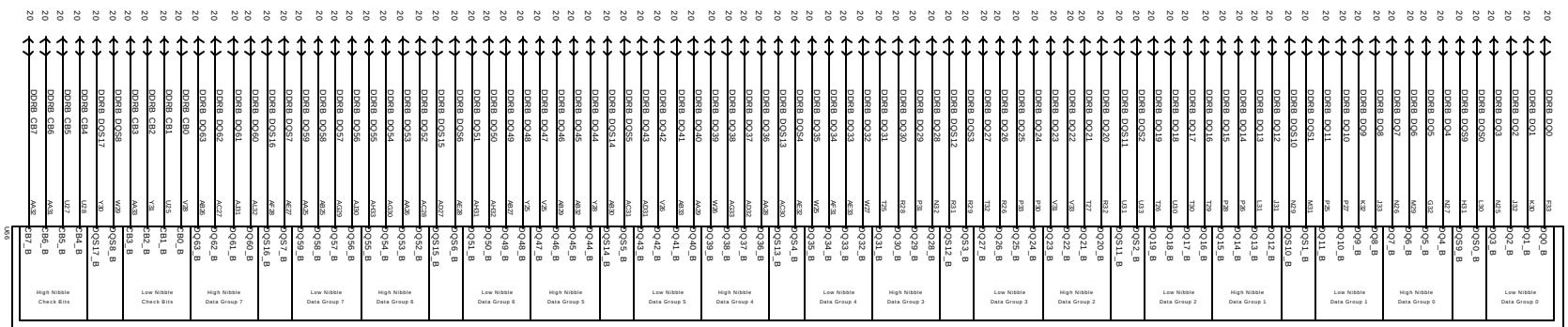
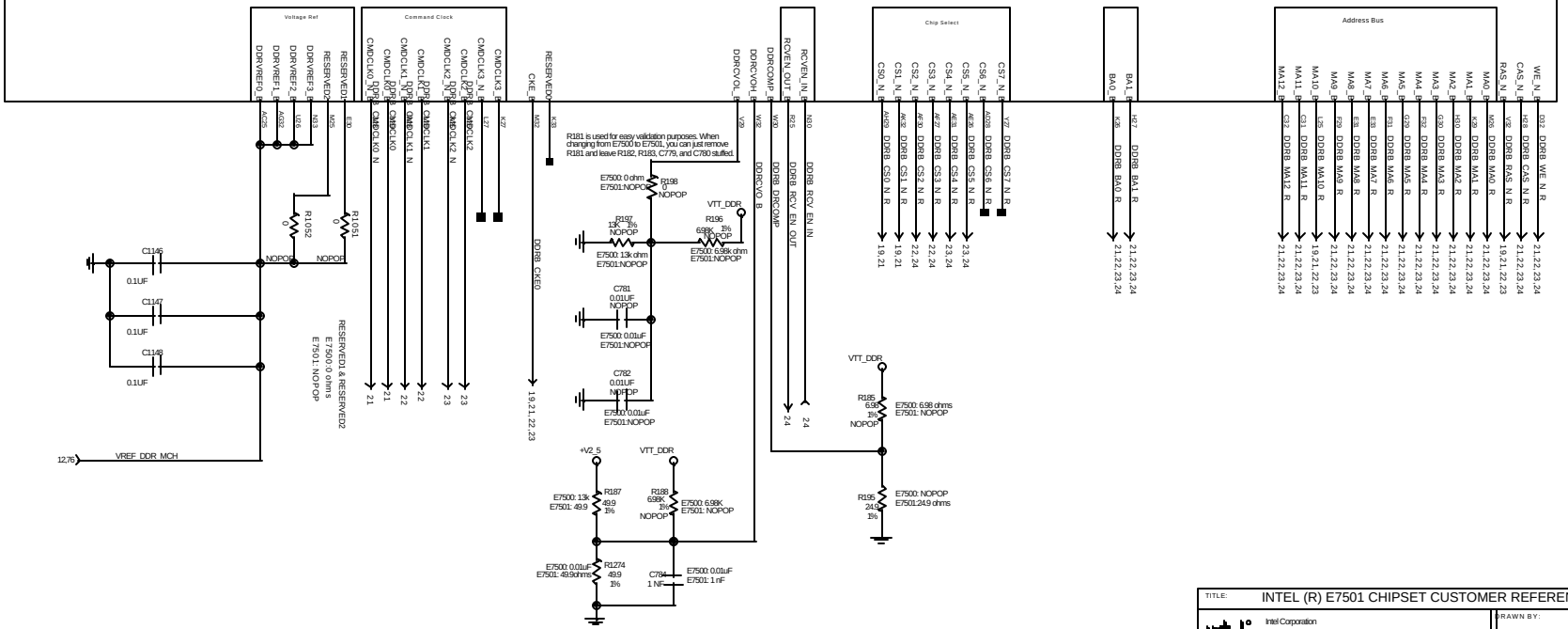
MCH DDR Channel B



MCH DDR B



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	
DRAWN BY:	
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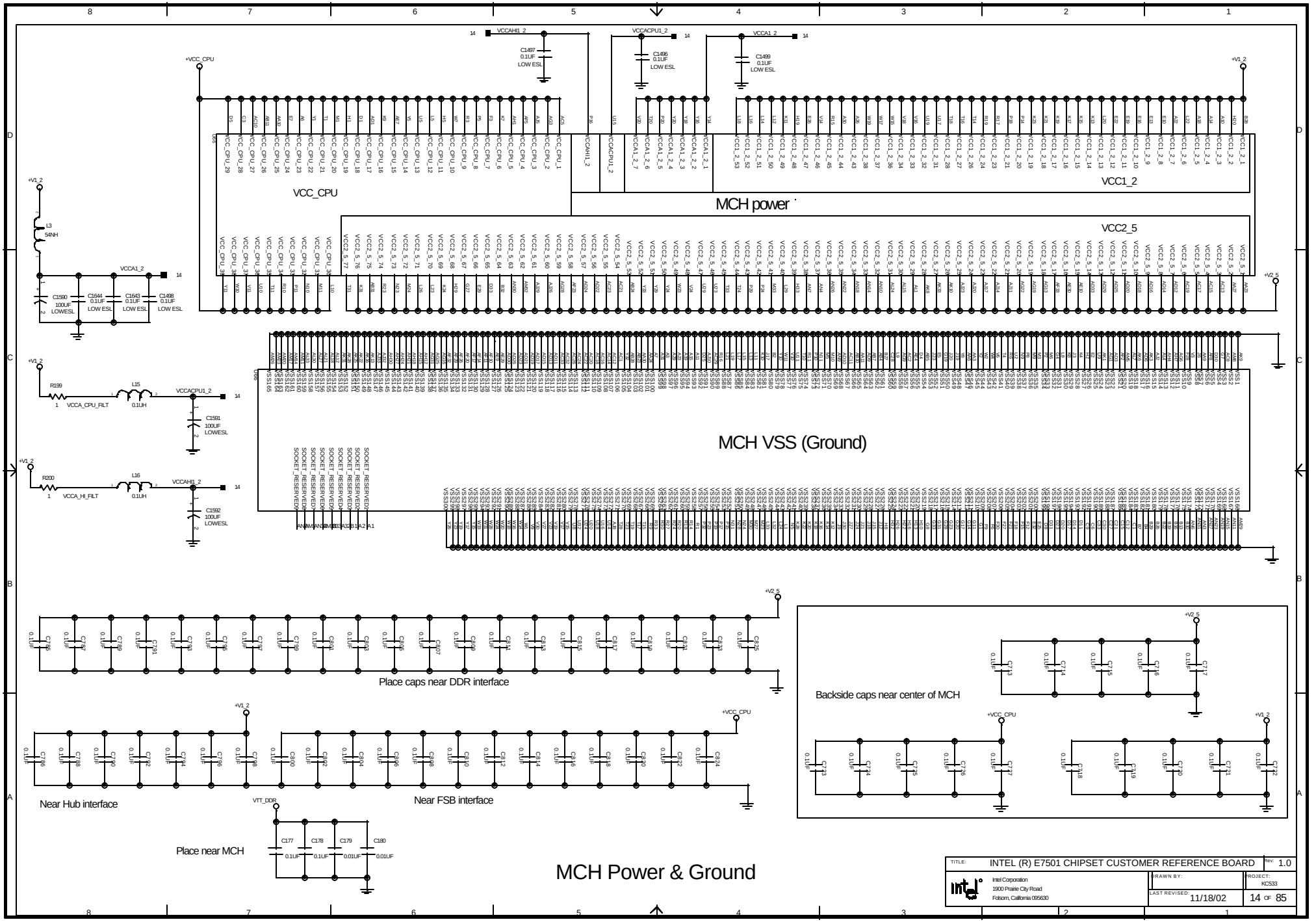
VCCAH1_2
VCCACPU1_2
VCCA1_2
+VCC_CPU
+V1_2
C1497 0.1UF LOW ESL
C1496 0.1UF LOW ESL
C1499 0.1UF LOW ESL
VCC_CPU
VCC1_2
MCH power
VCC2_5
+V2_5
L3 54NH
C1500 100UF LOWESL
C1644 0.1UF LOW ESL
C1643 0.1UF LOW ESL
C1498 0.1UF LOW ESL
R199
L15
VCCA_CPU_FILT
0.1UH
C1591 100UF LOWESL
R200
L16
VCCA_HI_FILT
C1592 100UF LOWESL
MCH VSS (Ground)
Place caps near DDR interface
Backside caps near center of MCH
Near Hub interface
Near FSB interface
Place near MCH
VTT_DDR
C177 0.1UF
C178 0.1UF
C179 0.01UF
C180 0.01UF
MCH Power & Ground
TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV: 1.0
Intel Corporation
1900 Prairie City Road
Folsom, California 095630
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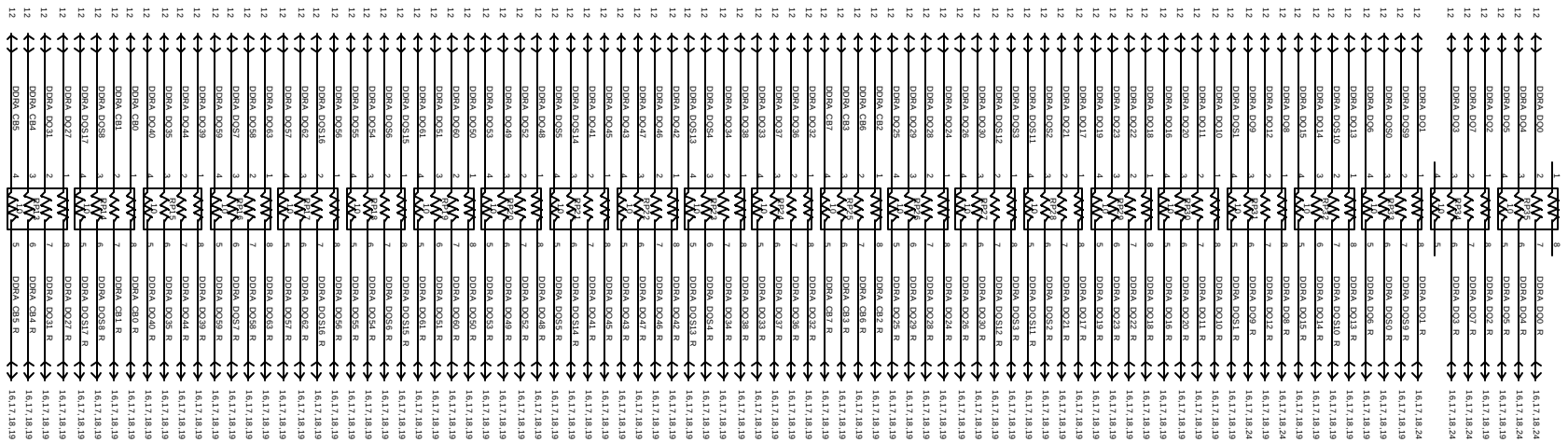
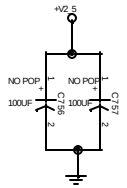
DDR Channel A Series Resistors

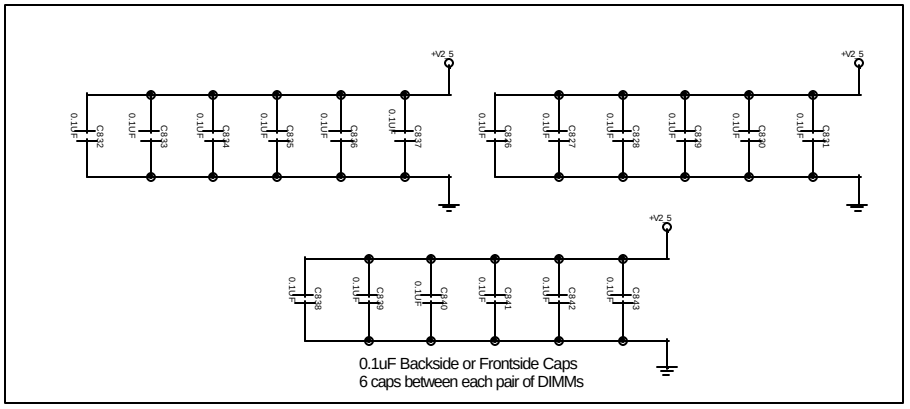
Place near DIMM A-1





Place 100uf caps surrounding channel B DIMMs

CAD Note: All caps should have a direct attachment to the 2.5V plane, and 2 vias to GND.



0.1uF Backside or Frontside Caps
6 caps between each pair of DIMMs

TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
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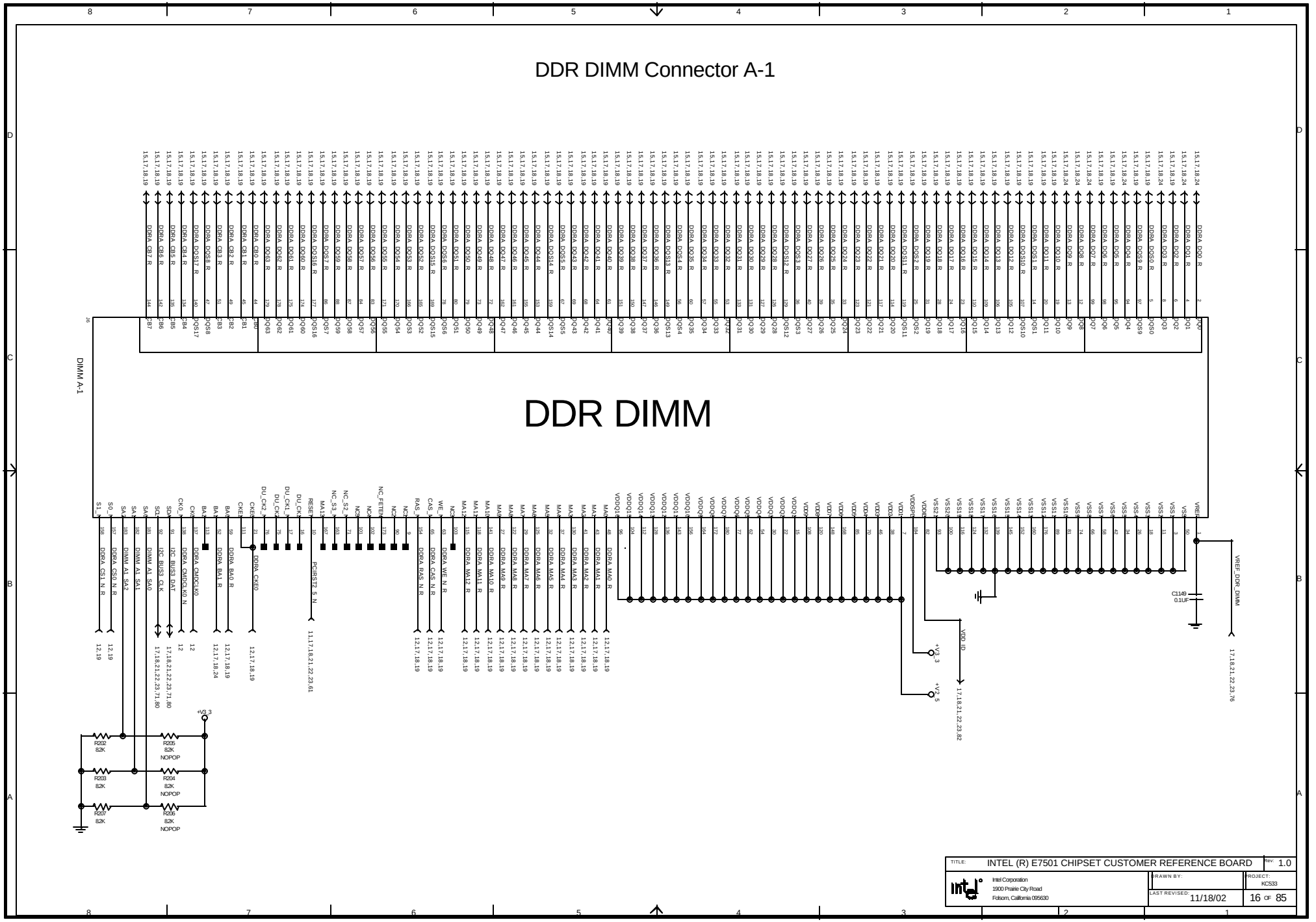
DDR DIMM Connector A-1
DDR DIMM
DIMM A-1
VREF_DDR_DIMM
C1149
0.1UF
VDD_ID
+V3_3
+V2_5
R202
82K
R205
82K
NOPOP
R203
82K
R204
82K
NOPOP
R207
82K
R206
82K
NOPOP
TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV: 1.0
Intel Corporation
1900 Prairie City Road
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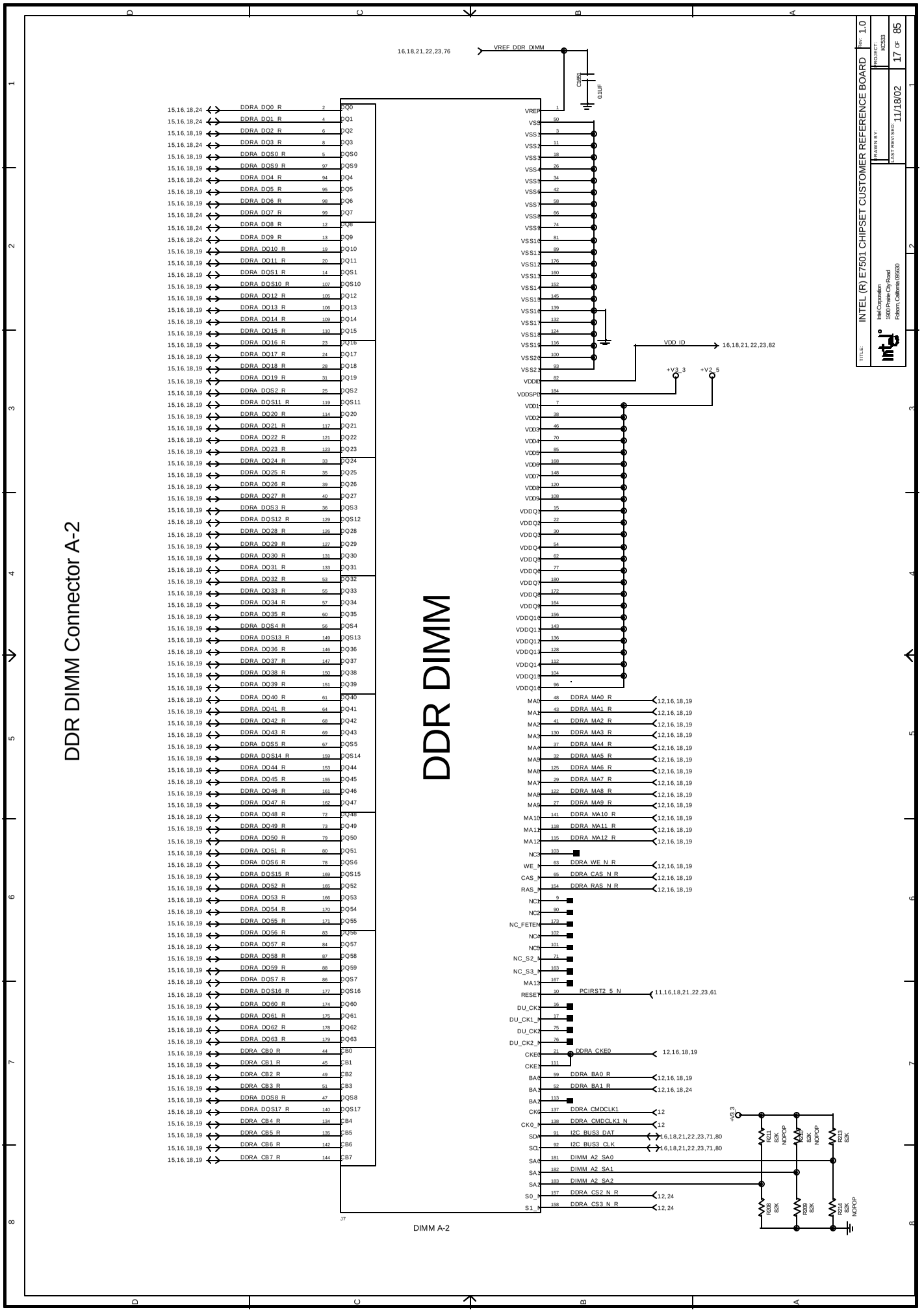
DDR DIMM Connector A-2
DDR DIMM
DIMM A-2
INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
Intel Corporation
3600 Prairie City Road
Folsom, California 95630
DRAWN BY:
LAST REVISED: 11/18/02
PROJECT: MCS33
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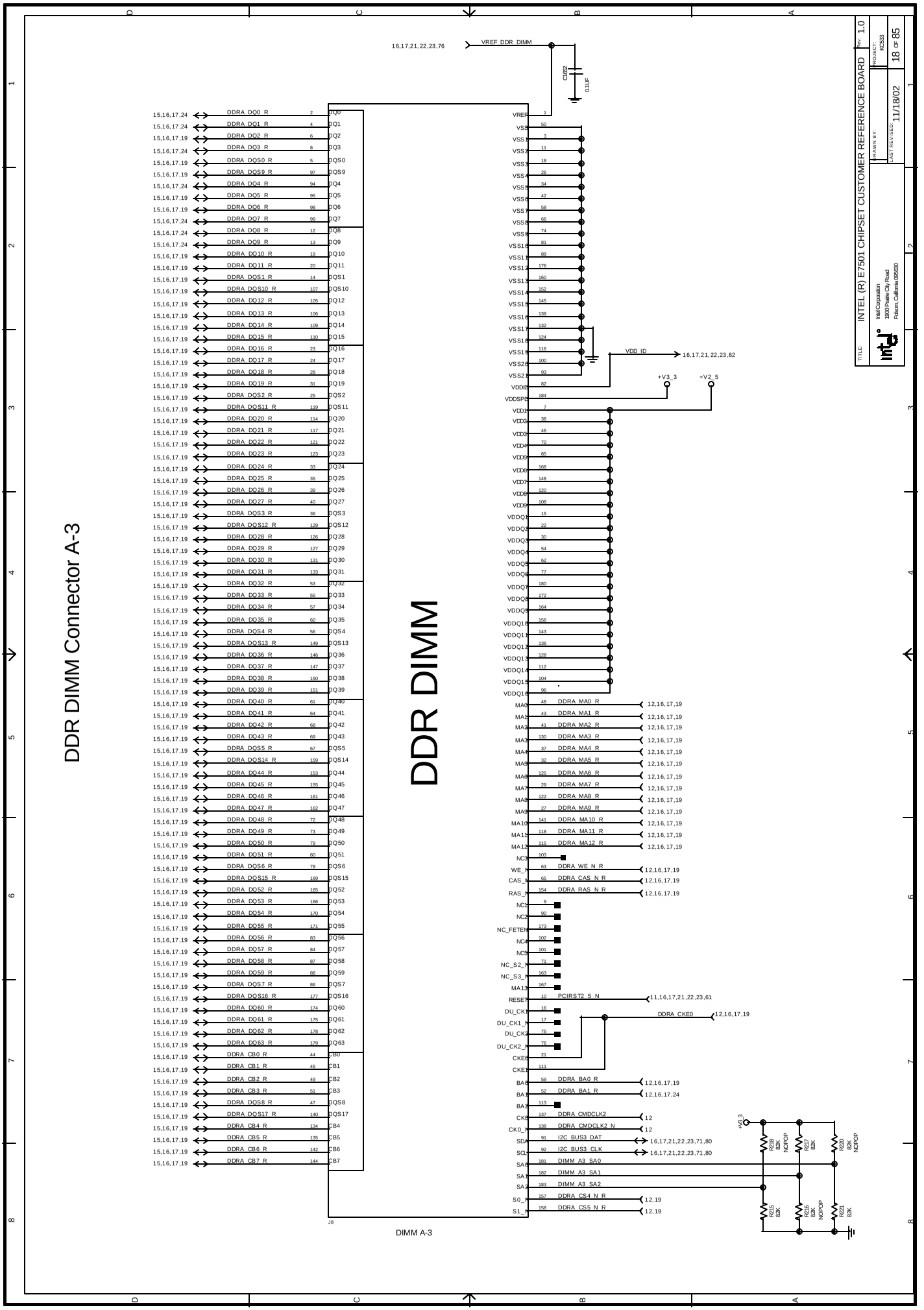
REV: 1.0
VREF_DDR_DIMM
VDD_ID
+V3_3
+V2_5
PCIRST2_5_N
DDRA_CKE0
DDRA_CMDCLK1
DDRA_CMDCLK1_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_A2_SA0
DIMM_A2_SA1
DIMM_A2_SA2
DDRA_CS2_N_R
DDRA_CS3_N_R
DDRA_WE_N_R
DDRA_CAS_N_R
DDRA_RAS_N_R
DDRA_BA0_R
DDRA_BA1_R
DDRA_MA0_R
DDRA_MA1_R
DDRA_MA2_R
DDRA_MA3_R
DDRA_MA4_R
DDRA_MA5_R
DDRA_MA6_R
DDRA_MA7_R
DDRA_MA8_R
DDRA_MA9_R
DDRA_MA10_R
DDRA_MA11_R
DDRA_MA12_R


DDR DIMM Connector A-3
DDR DIMM
DIMM A-3
INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
Intel Corporation
3600 Prairie City Road
Folsom, California 95630
DRAWN BY:
LAST REVISED: 11/18/02
PROJECT: KCS33
REV: 1.0
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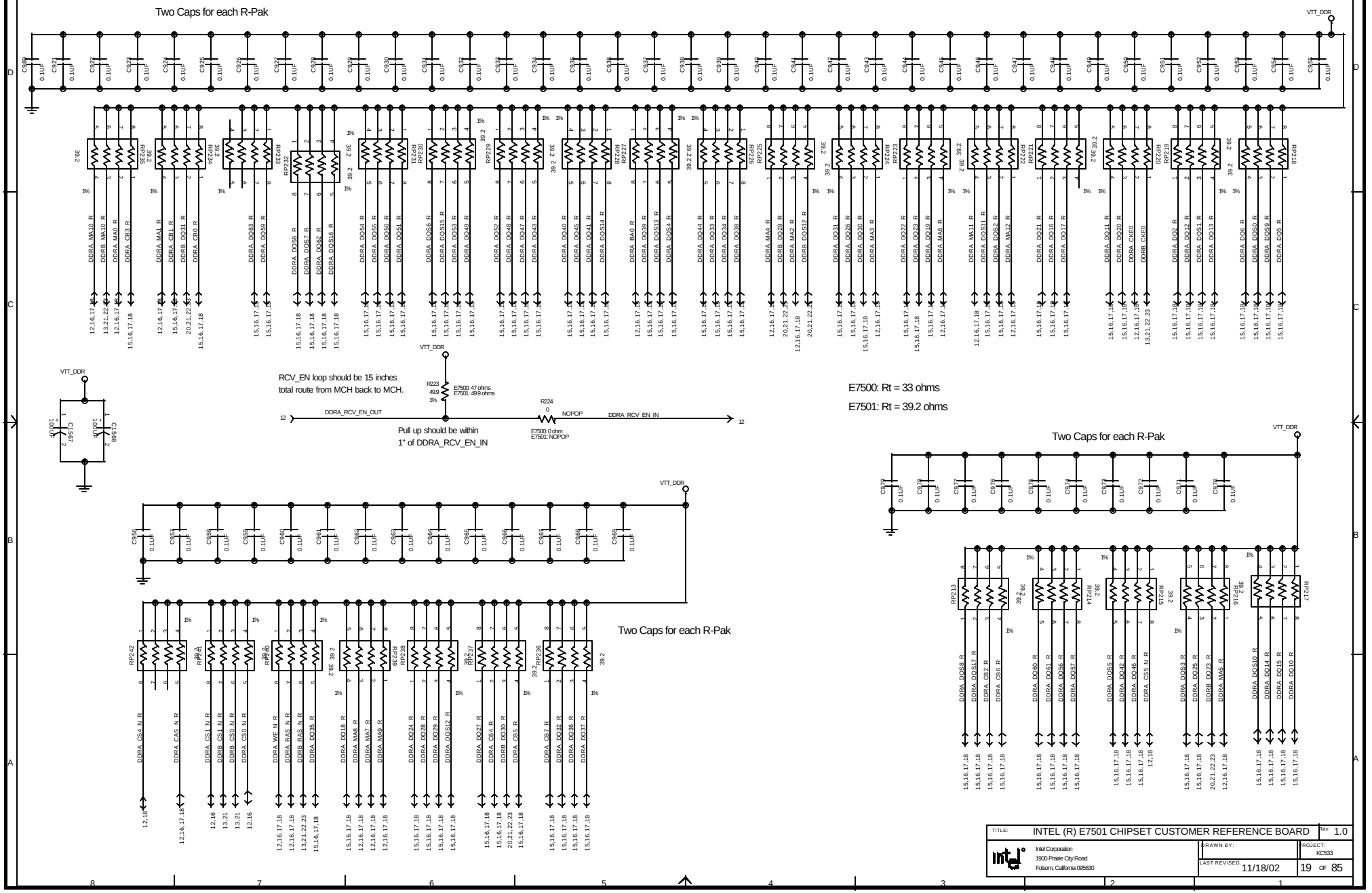
VREF_DDR_DIMM
VDD_ID
+V3_3
+V2_5
DDRA_CMDCLK2
DDRA_CMDCLK2_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_A3_SA0
DIMM_A3_SA1
DIMM_A3_SA2
DDRA_CS4_N_R
DDRA_CS5_N_R
DDRA_CKE0
PCIRST2_5_N

DDR Channel A Termination



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630		DRAWN BY:	PROJECT: KC533
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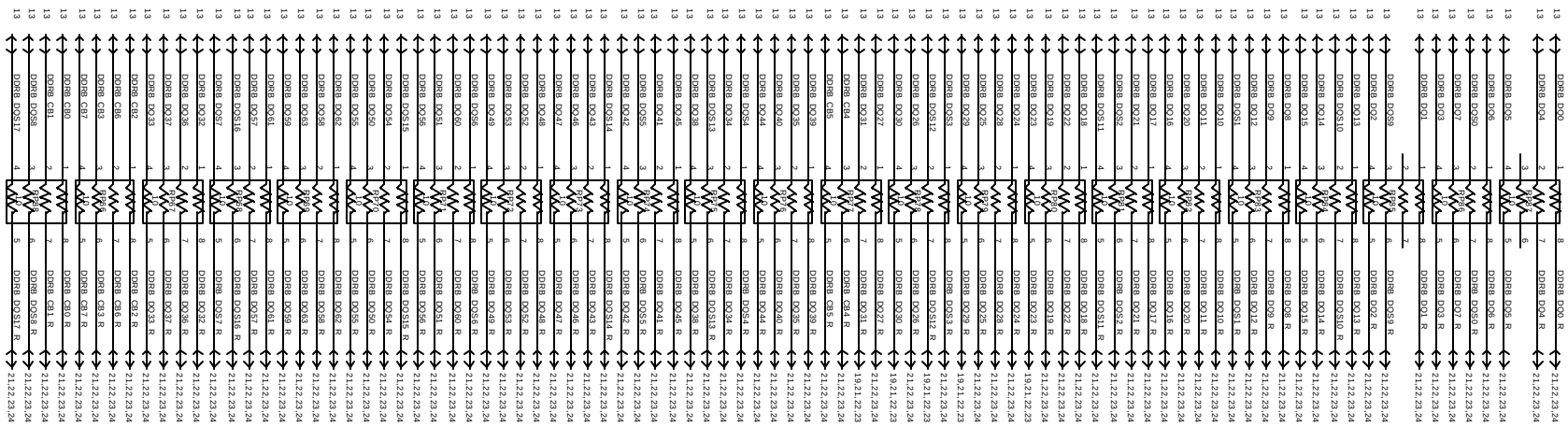
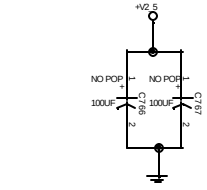
DDR Channel B Series Resistors

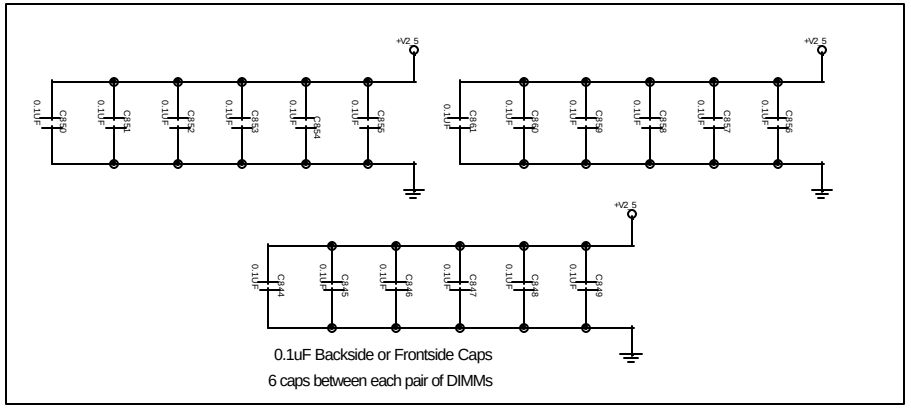
Place near DIMM B-1





Place 100uf caps surrounding channel B DIMMs

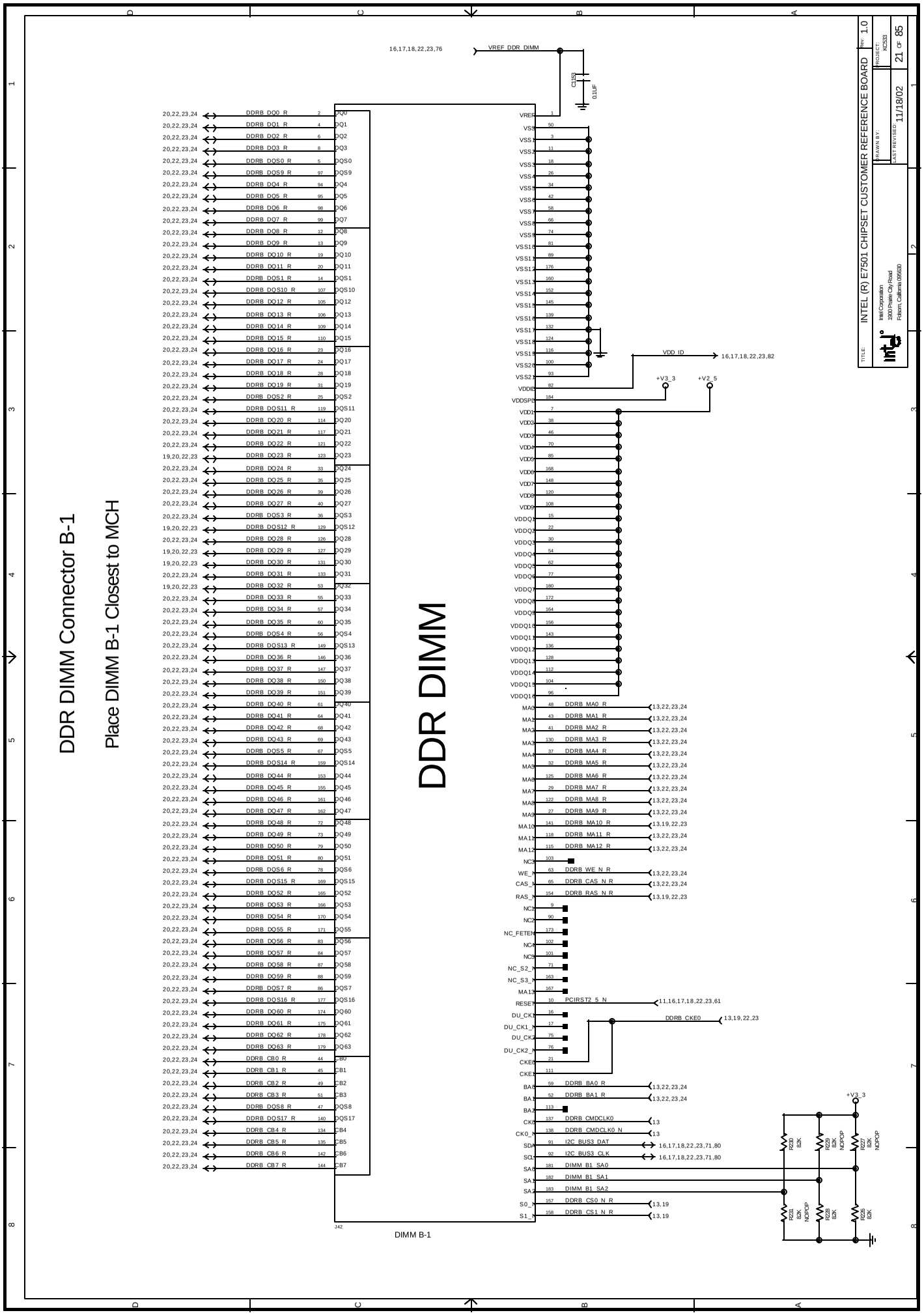
CAD Note: All caps should have a direct attachment to the 2.5V plane, and 2 vias to GND.



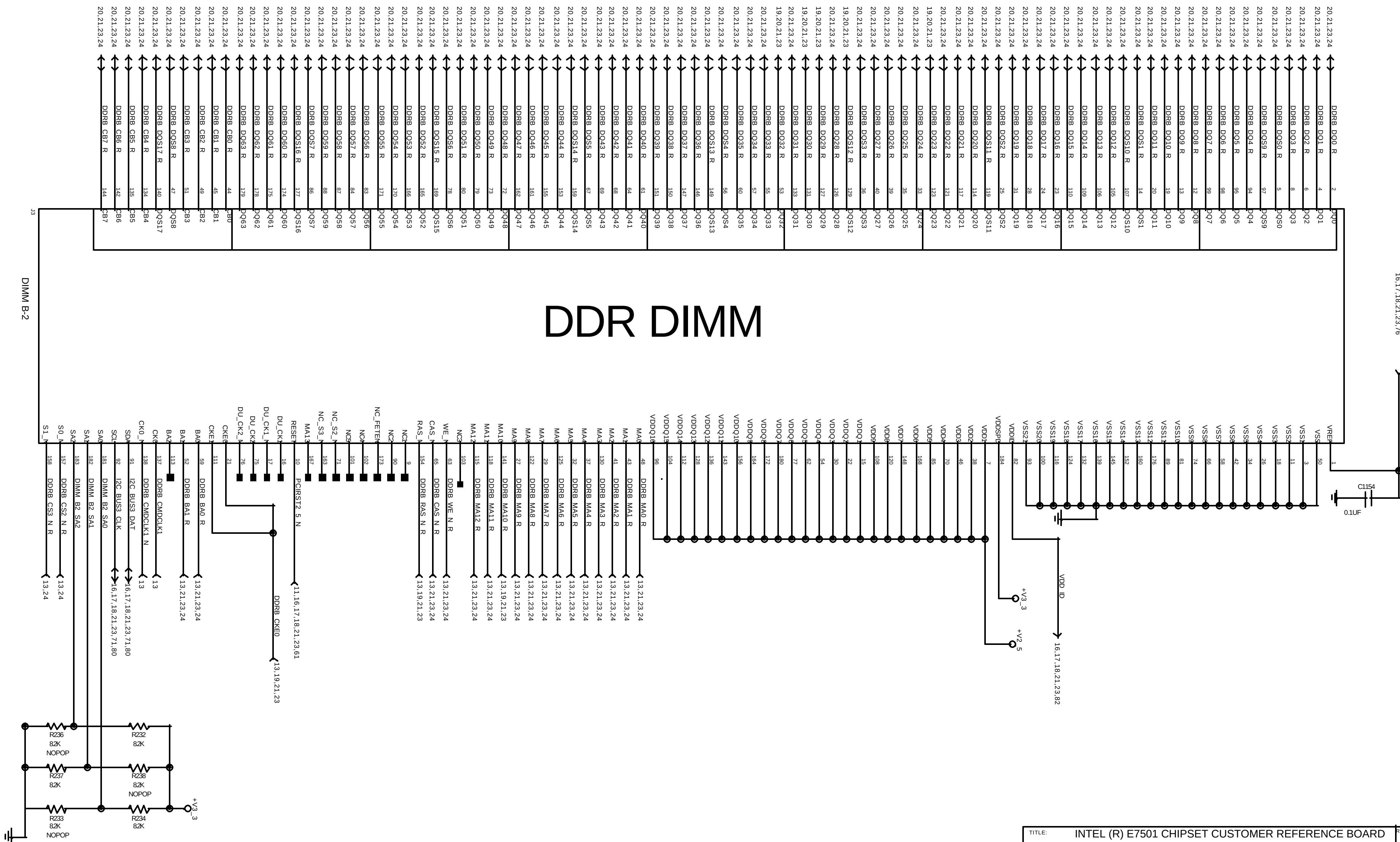
0.1uF Backside or Frontside Caps

6 caps between each pair of DIMMs

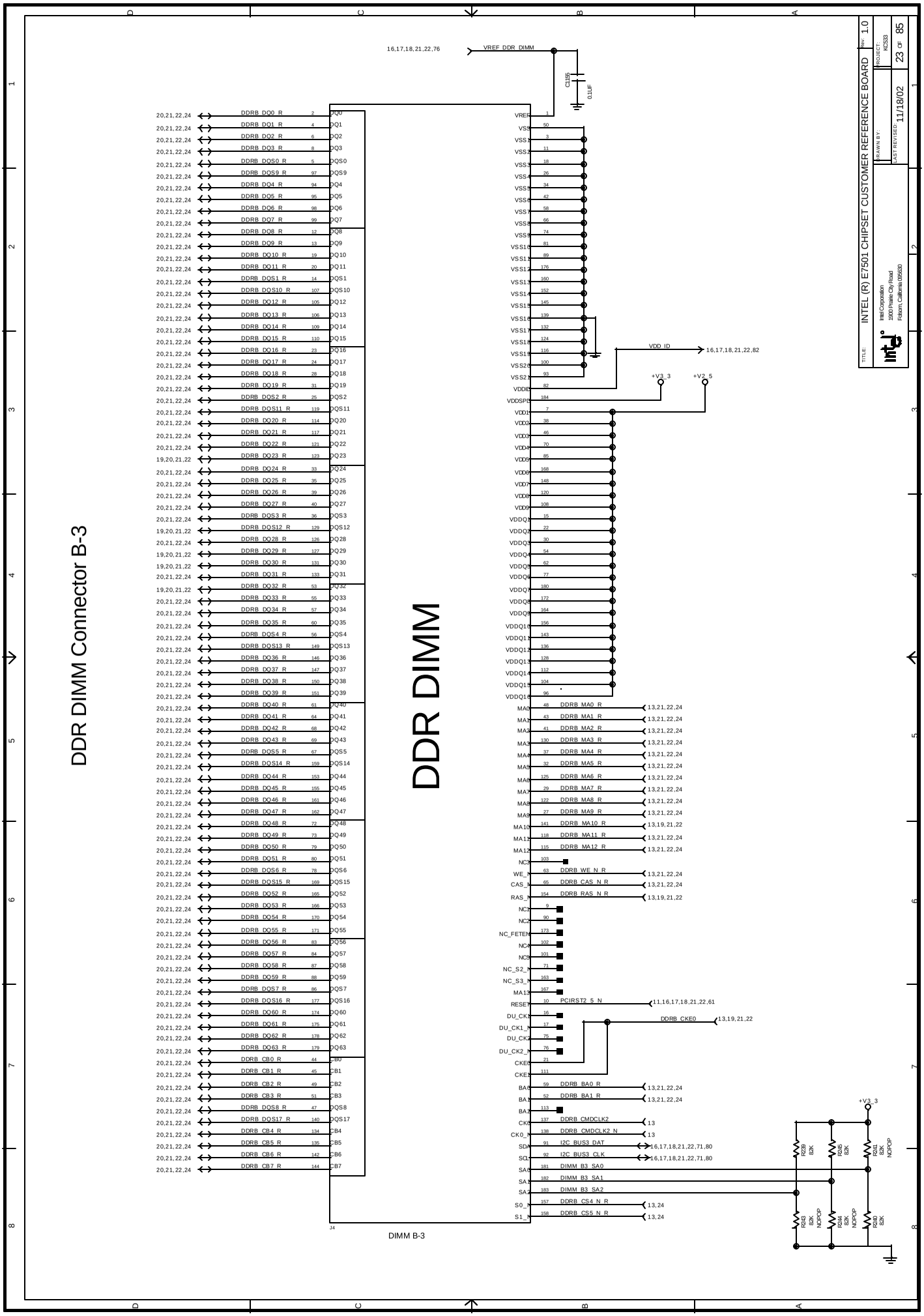
TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630		DRAWN BY:	PROJECT: KC533
		LAST REVISED: 11/18/02	20 OF 85


DDR DIMM Connector B-1
Place DIMM B-1 Closest to MCH
DDR DIMM
DIMM B-1
INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
Intel Corporation
3600 Prairie City Road
Folsom, California 95630
DRAWN BY:
LAST REVISED: 11/18/02
PROJECT: MCS33
REV: 1.0
21 OF 85
VREF_DDR_DIMM
16,17,18,22,23,76
VDD_ID
16,17,18,22,23,82
+V3_3
+V2_5
DDRB_CKE0
PCIRST2_5_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DDRB_CMDCLK0
DDRB_CMDCLK0_N
DDRB_CS0_N_R
DDRB_CS1_N_R
DDRB_WE_N_R
DDRB_CAS_N_R
DDRB_RAS_N_R
DIMM_B1_SA0
DIMM_B1_SA1
DIMM_B1_SA2

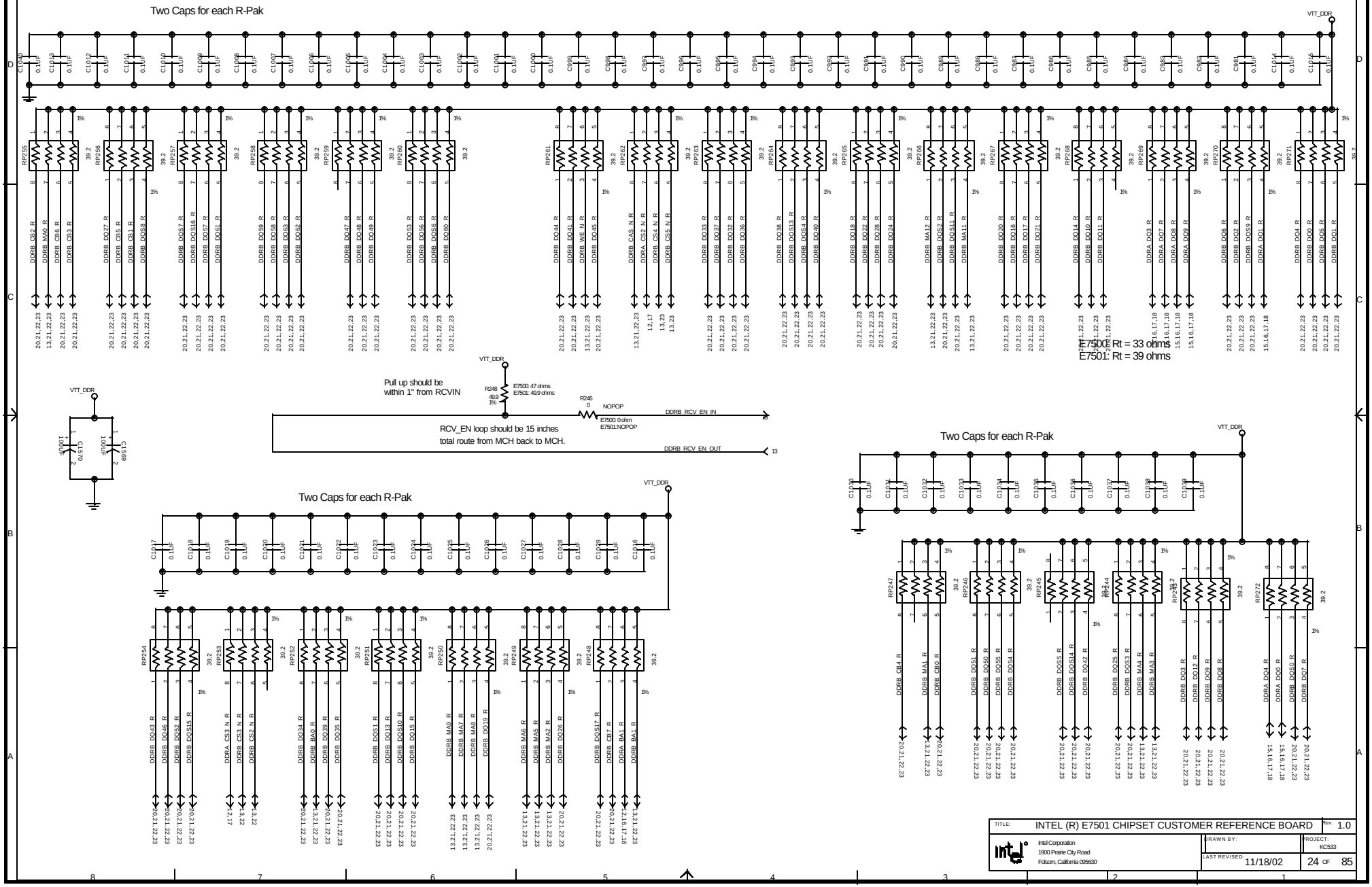
DDR DIMM Connector B-2



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
Rev:	1.0
	Intel Corporation 1900 Prairie City Road Folsom, California 095630
DRAWN BY:	
PROJECT:	KC533
LAST REVISED:	11/18/02
	22 OF 85

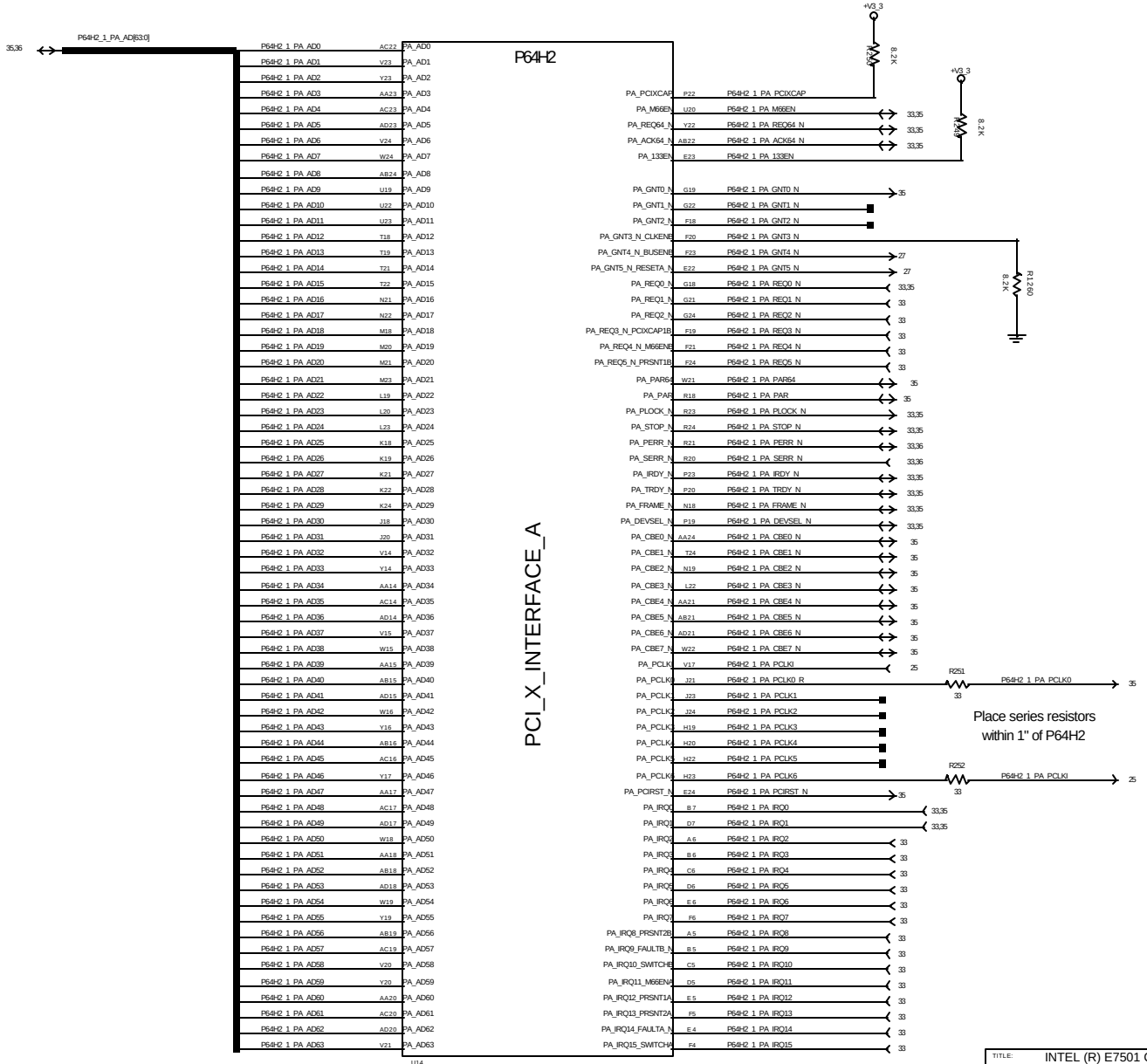

DDR DIMM Connector B-3
DDR DIMM
DIMM B-3
VREF_DDR_DIMM
C1155
0.1UF
VDD_ID
+V3_3
+V2_5
DDRB_CMDCLK2
DDRB_CMDCLK2_N
I2C_BUS3_DAT
I2C_BUS3_CLK
DIMM_B3_SA0
DIMM_B3_SA1
DIMM_B3_SA2
DDRB_CS4_N_R
DDRB_CS5_N_R
PCIRST2_5_N
DDRB_CKE0
DDRB_WE_N_R
DDRB_CAS_N_R
DDRB_RAS_N_R
R239 82K
R245 82K
R241 82K NOPOP
R243 82K NOPOP
R244 82K NOPOP
R240 82K
INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
Intel Corporation
3600 Prairie City Road
Folsom, California 95630
DRAWN BY:
LAST REVISED: 11/18/02
PROJECT: MCS33
REV: 1.0
23 OF 85

DDR Channel B Termination



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630		DRAWN BY:	PROJECT: KC533
		LAST REVISED: 11/18/02	24 OF 85

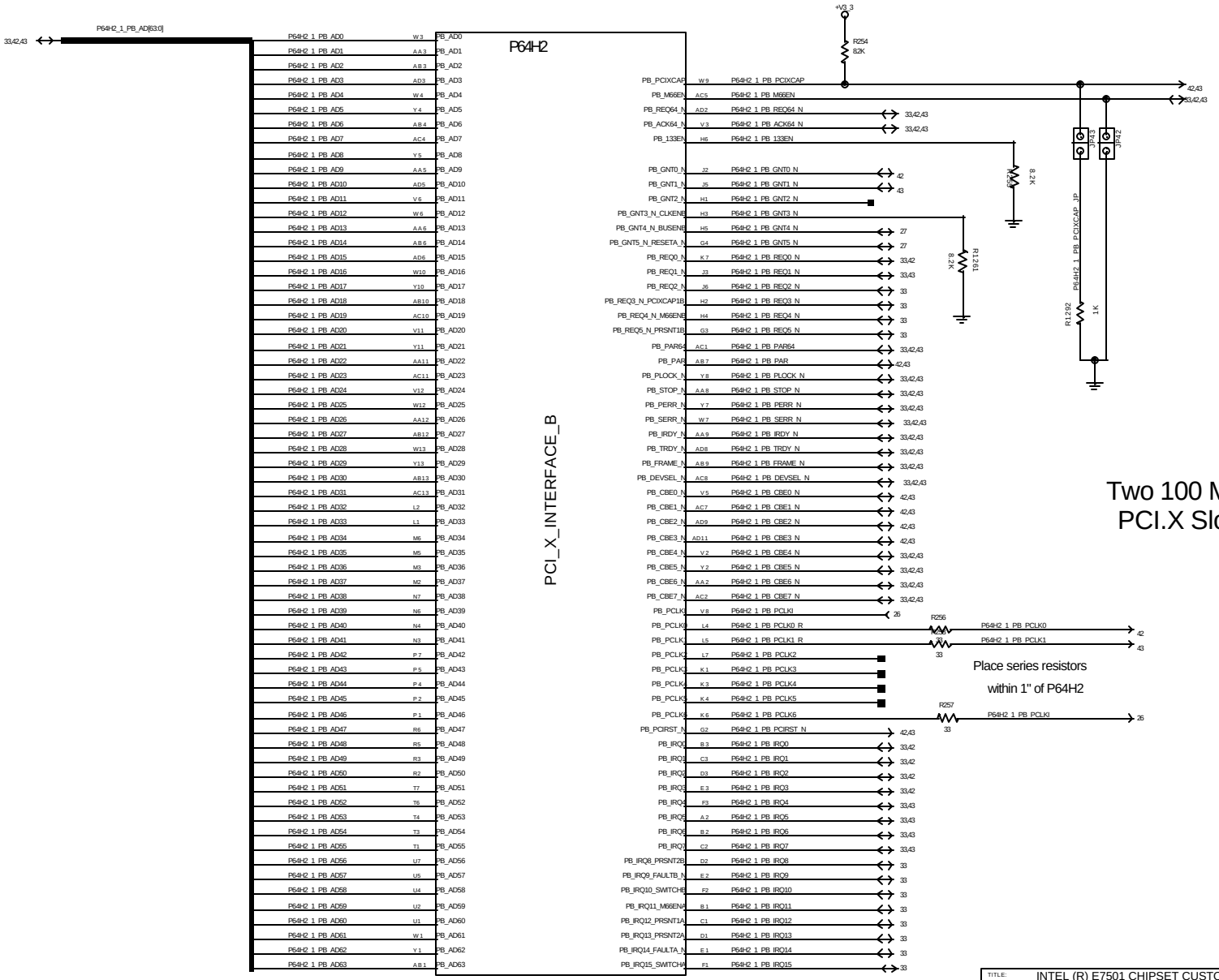
P64H2 #1 - PCI.X Interface A



133 MHz
Gigabit Ethernet
Controller

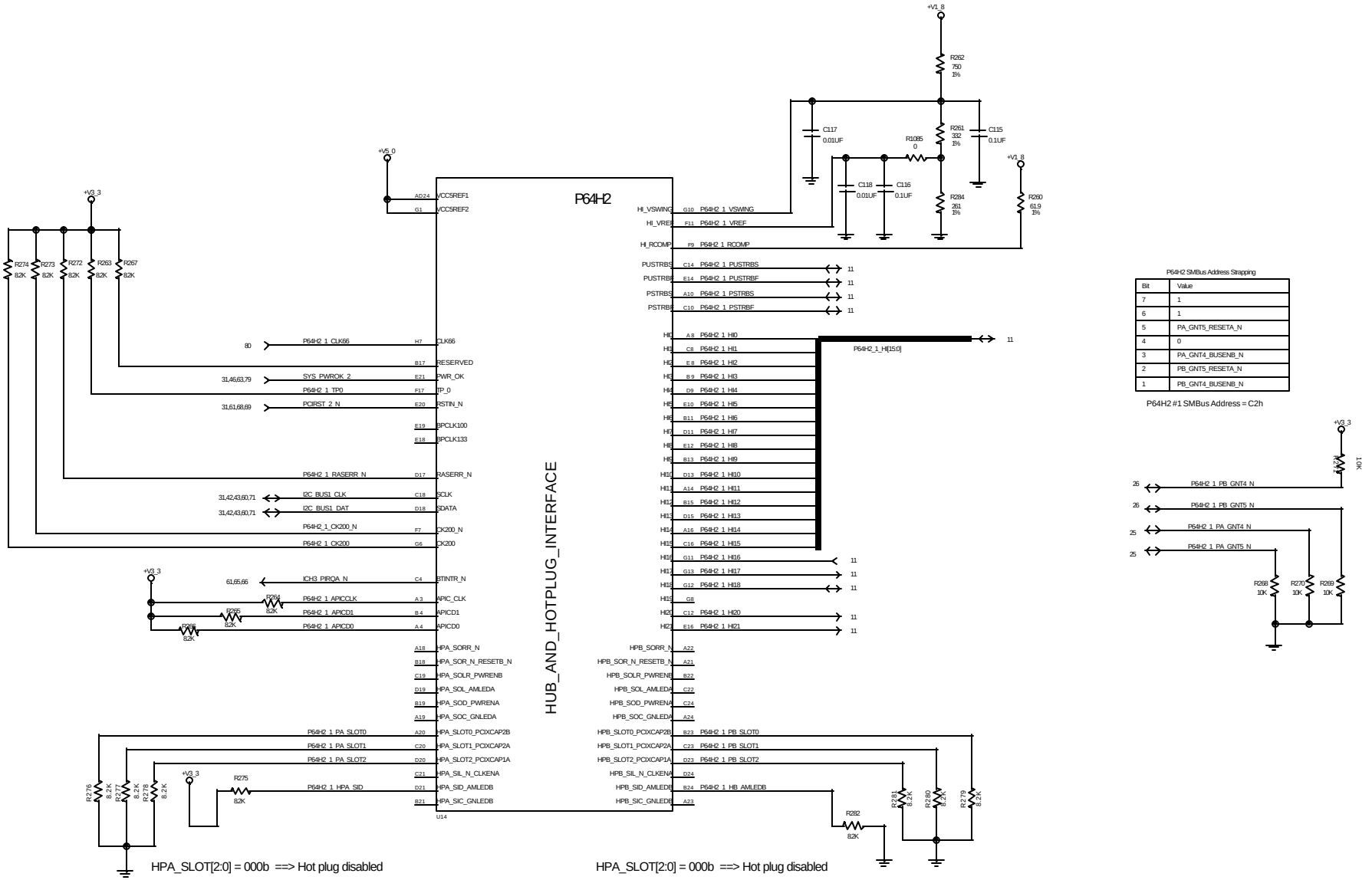
TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV:	1.0
Intel Corporation	1900 Prairie City Road, Folsom, California 095630
DRAWN BY:	
PROJECT:	KC533
LAST REVISED:	11/18/02
	25 OF 85

P64H2 #1 - PCI.X Interface B



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV:	1.0
Intel Corporation	1900 Prairie City Road, Folsom, California 095630
DRAWN BY:	
PROJECT:	KC533
LAST REVISED:	11/18/02
	26 OF 85

P64H2 #1 - Hot Plug Interface



P64H2 SMBus Address Strapping

Bit	Value
7	1
6	1
5	PA_GNT5_RESETA_N
4	0
3	PA_GNT4_BUSENB_N
2	PB_GNT5_RESETA_N
1	PB_GNT4_BUSENB_N

P64H2 #1 SMBus Address = C2h

HPA_SLOT[2:0] = 000b ==> Hot plug disabled

HPA_SLOT[2:0] = 000b ==> Hot plug disabled

TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
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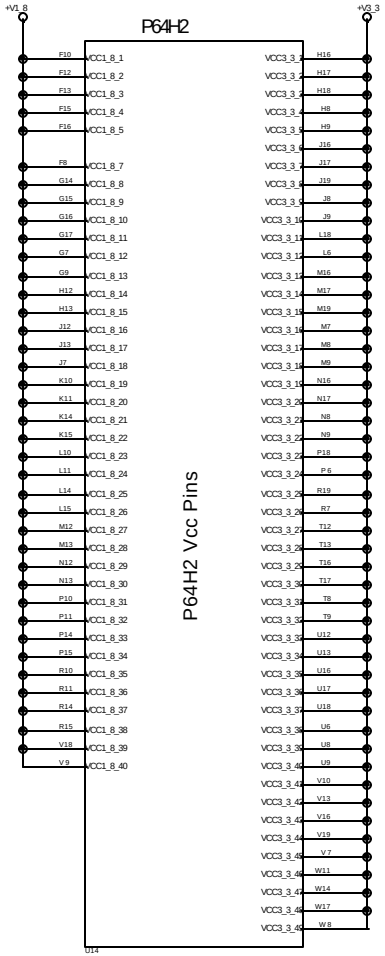
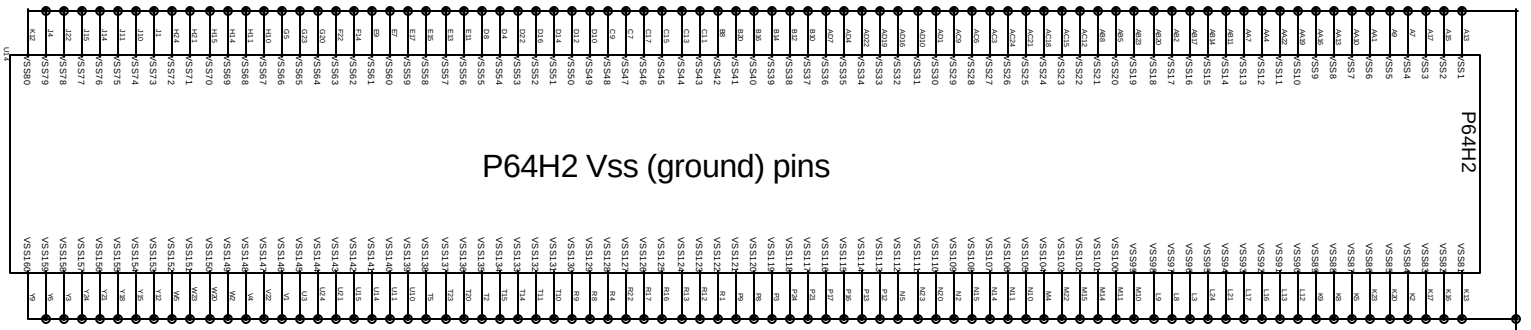
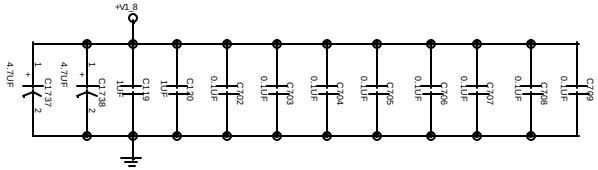
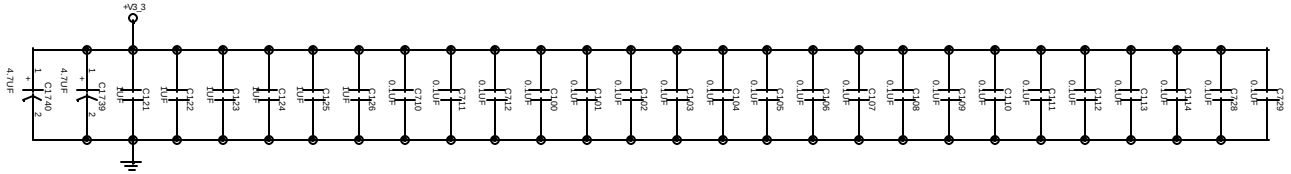
	LAST REVISED: 11/18/02		27 OF 85

P64H2 #1 - Power, Ground and Decoupling



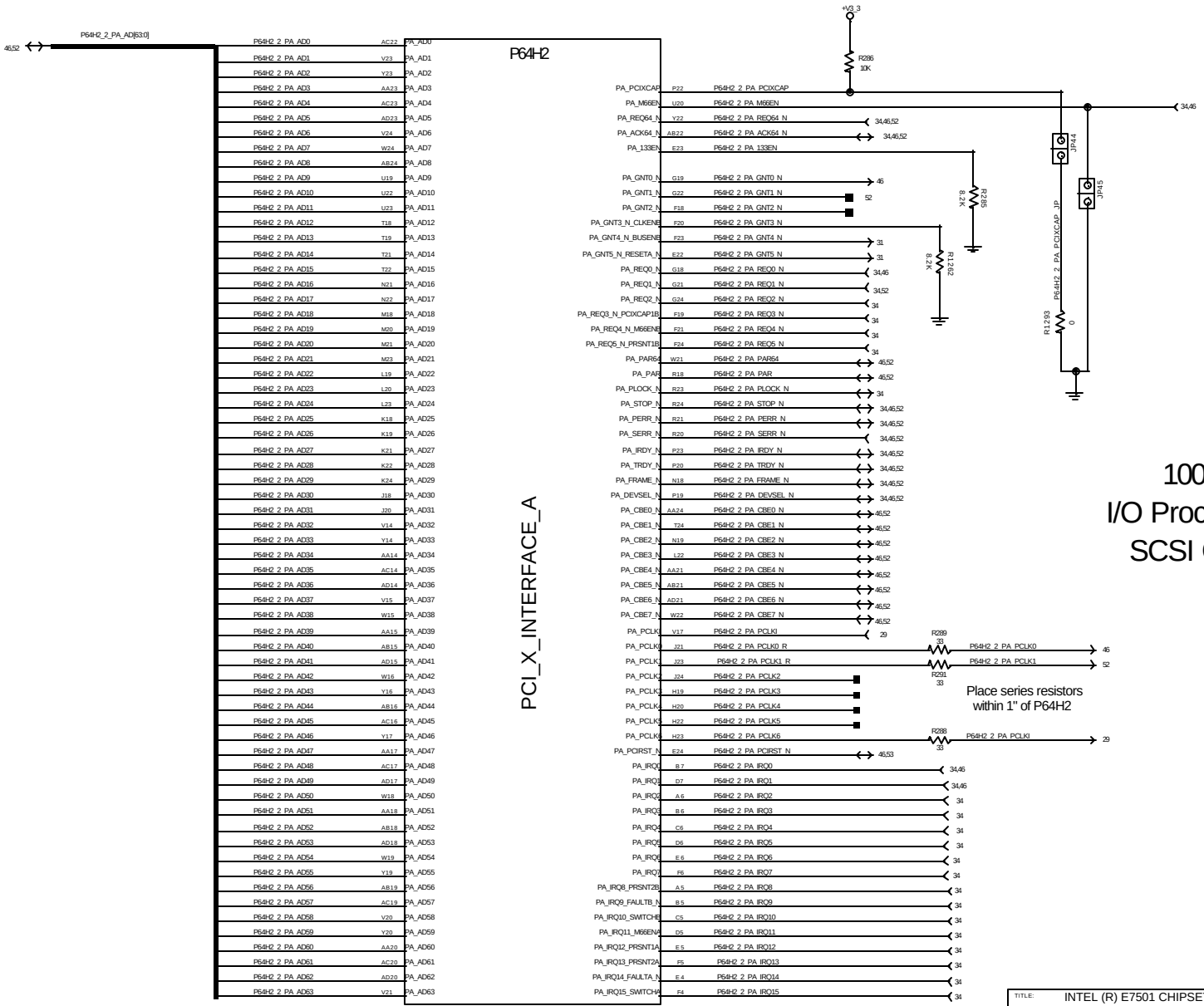






TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV.	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT:	KC533
	LAST REVISED: 11/18/02		28 OF 85

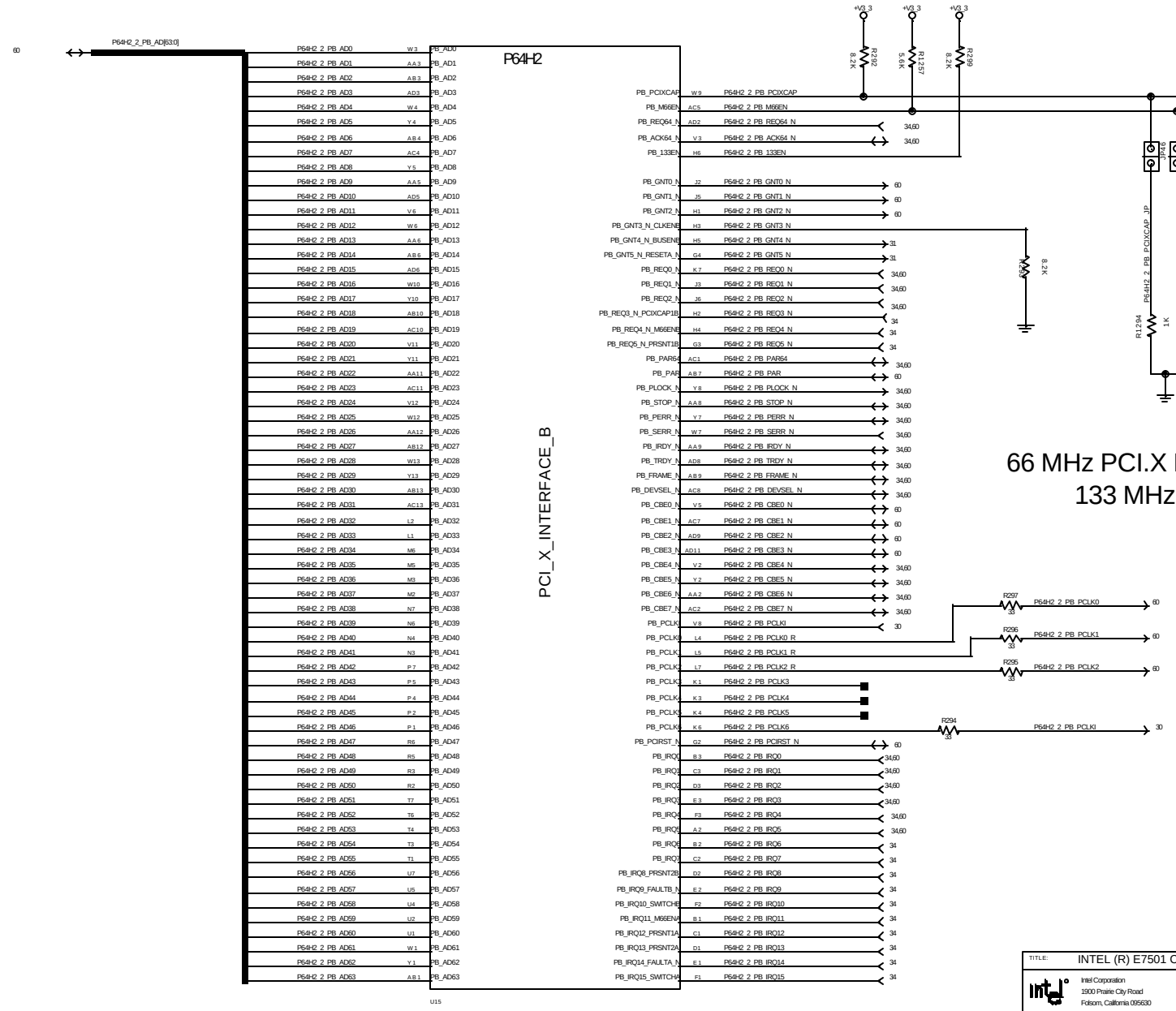
P64H2 #2 - PCI.X Interface A



100MHz
I/O Processor and
SCSI Controller

TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV:	1.0
Intel Corporation	1900 Prairie City Road, Folsom, California 095630
DRAWN BY:	
PROJECT:	KC533
LAST REVISED:	11/18/02
	29 OF 85

P64H2 #2 - PCI.X Interface B



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV:	1.0
Intel Corporation	1900 Prairie City Road, Folsom, California 095630
DRAWN BY:	
PROJECT:	KC533
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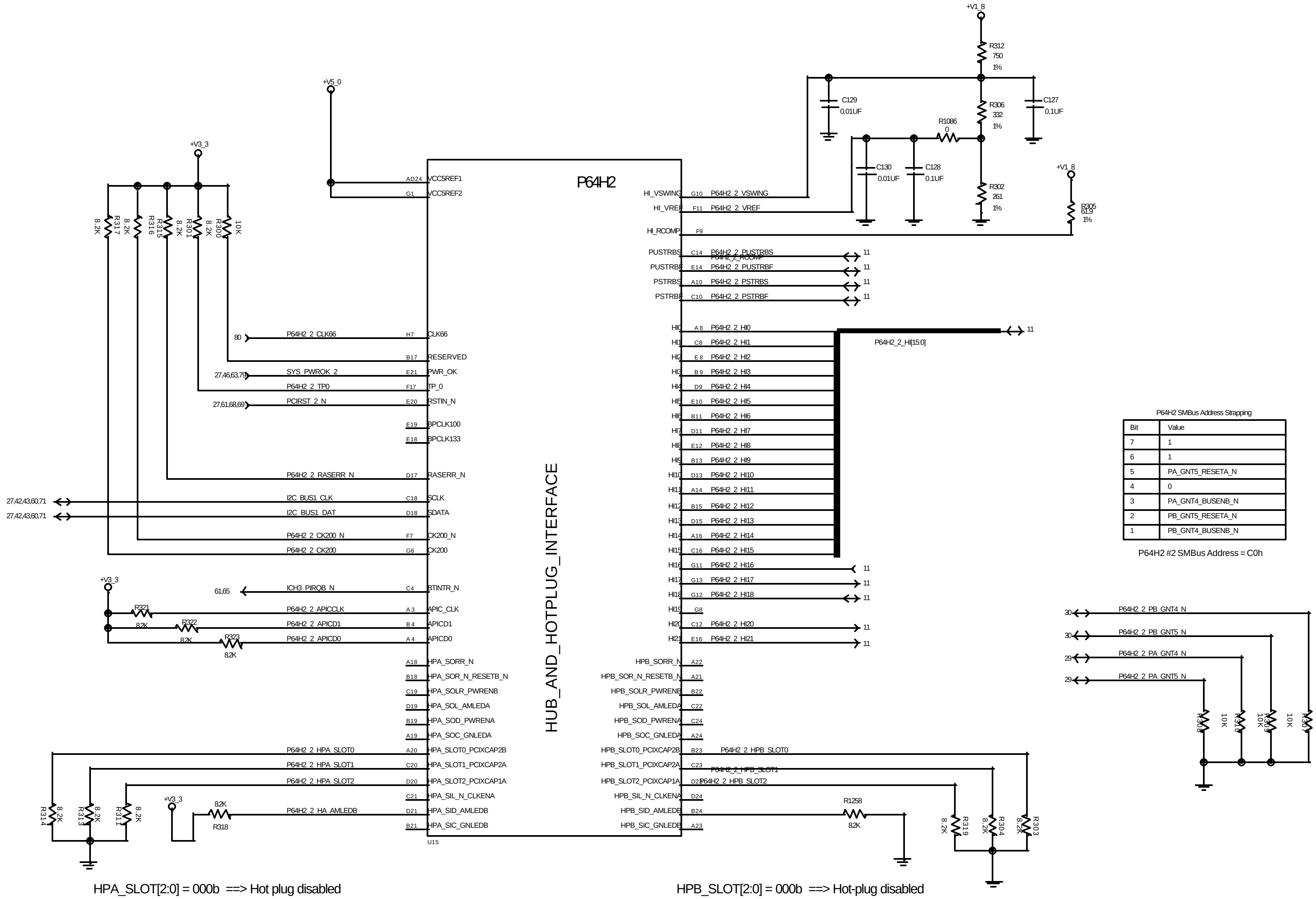
P64H2 #2 - Hot Plug Interface



P64H2 SMBus Address Strapping

Bit	Value
7	1
6	1
5	PA_GNT5_RESETA_N
4	0
3	PA_GNT4_BUSENB_N
2	PB_GNT5_RESETA_N
1	PB_GNT4_BUSENB_N

P64H2 #2 SMBus Address = C0h

HPA_SLOT[2:0] = 000b ==> Hot plug disabled

HPB_SLOT[2:0] = 000b ==> Hot-plug disabled

TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD Rev: 1.0

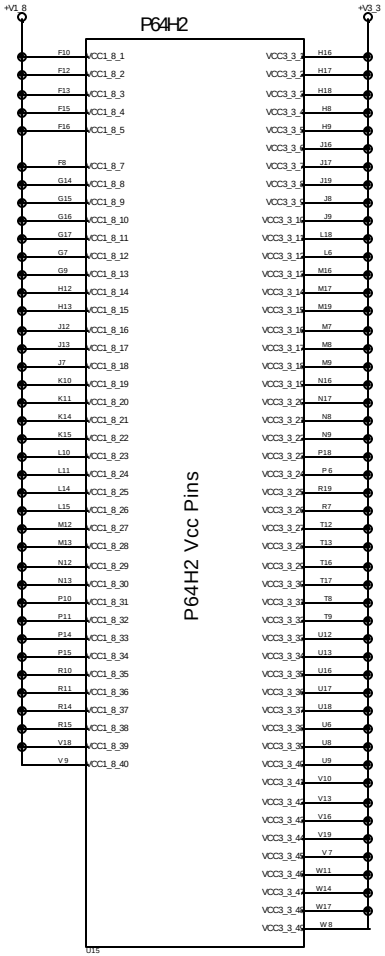
Intel Corporation
1900 Prairie City Road
Folsom, California 095630

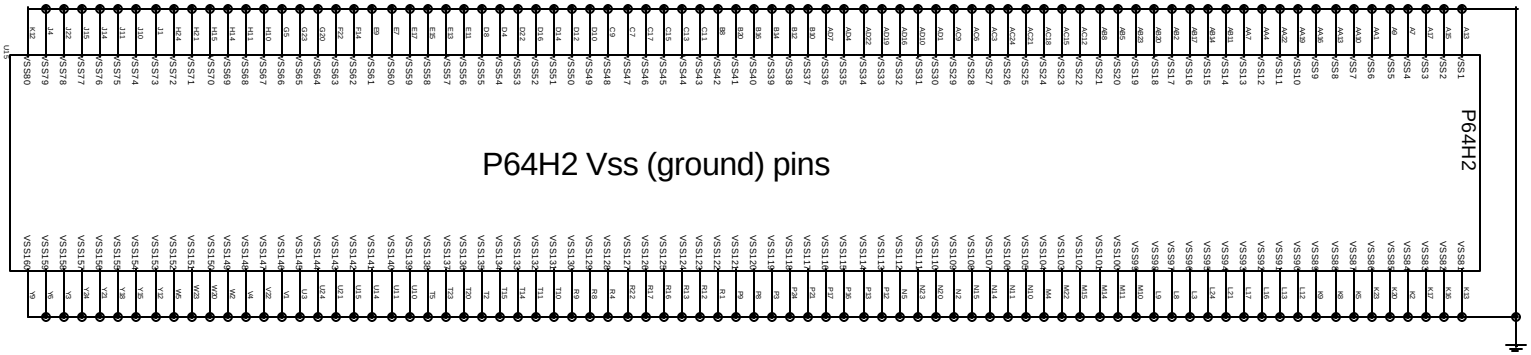
DRAWN BY:

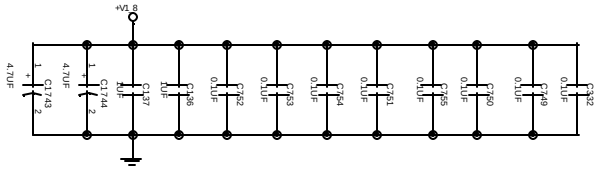
PROJECT: KC533

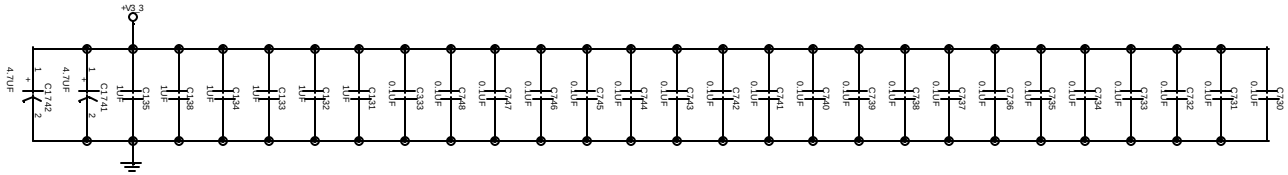
LAST REVISED: 11/18/02

P64H2 #2 - Power, Ground and Decoupling









TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
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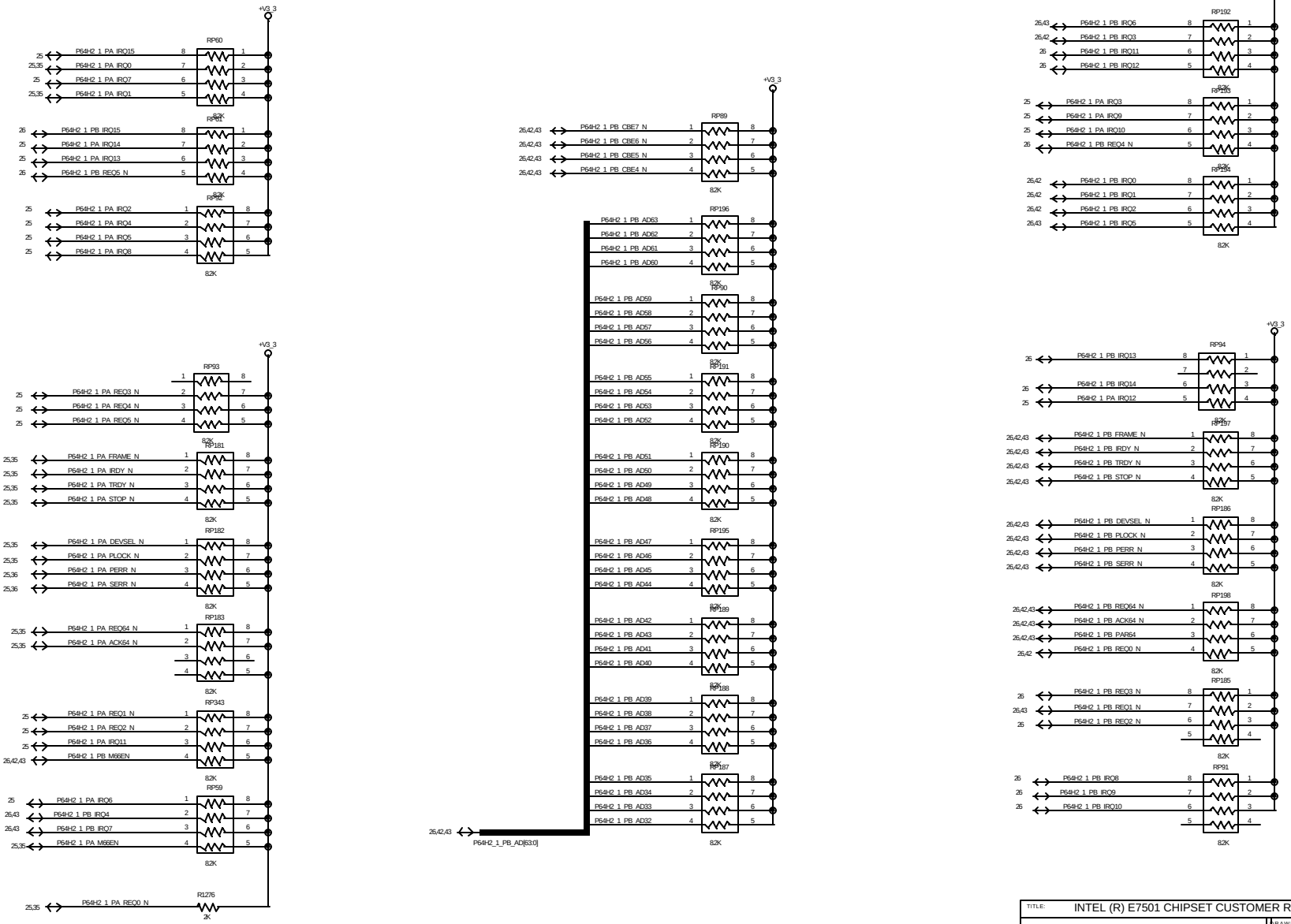
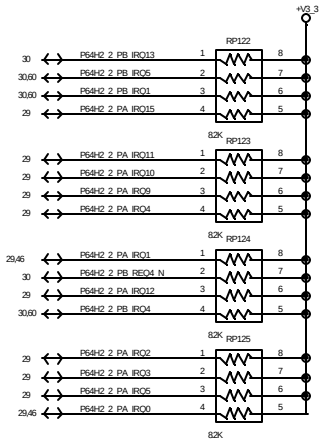
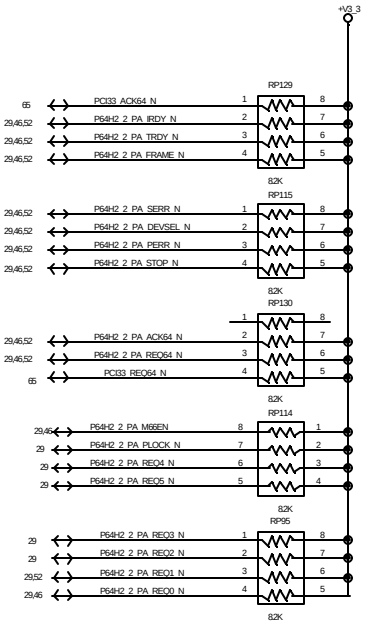
P64H2 #1 - PCI.X Pull-Ups

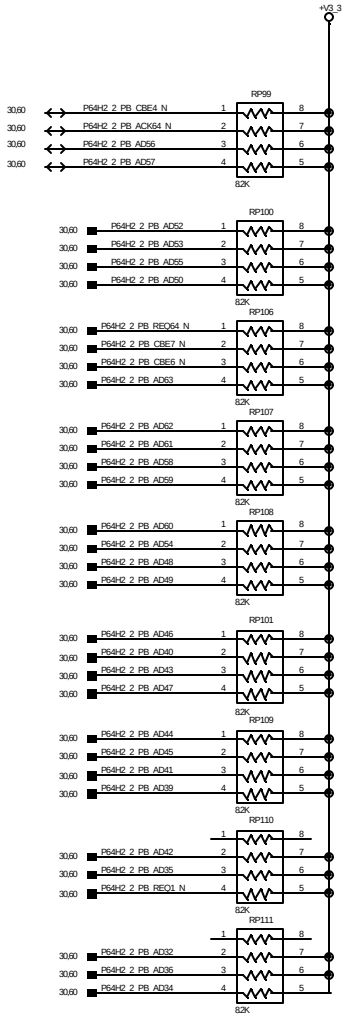


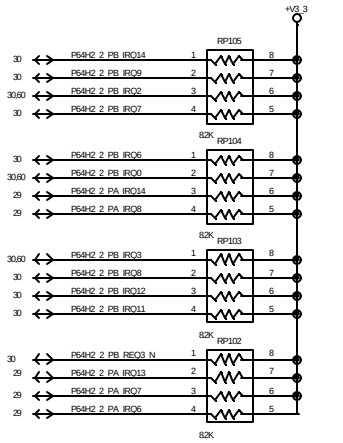
TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV.	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630		DRAWN BY:	PROJECT: KC533
		LAST REVISED: 11/18/02	33 OF 85

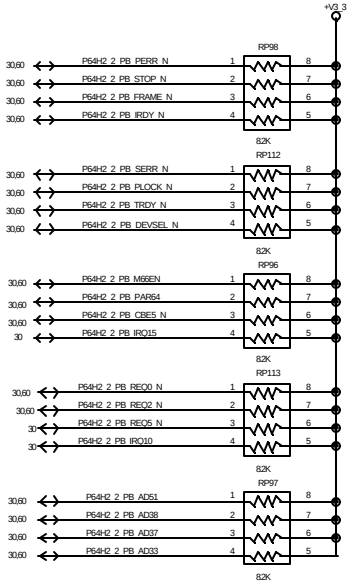
P64H2 #2 - PCI.X Pull-Ups





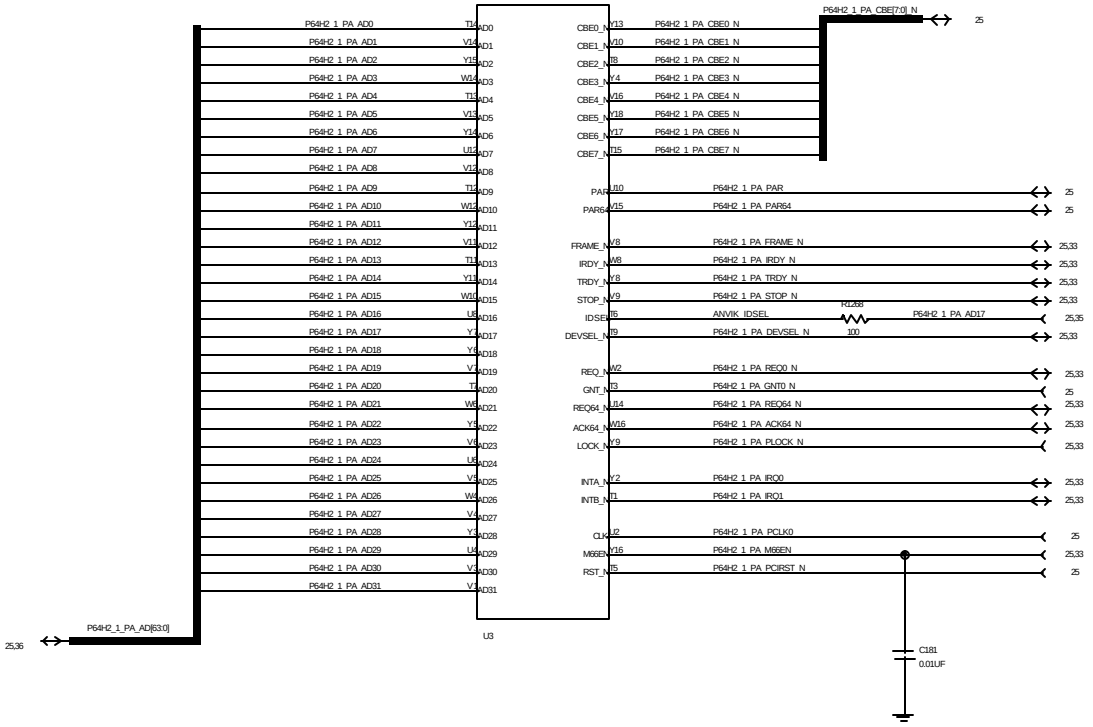






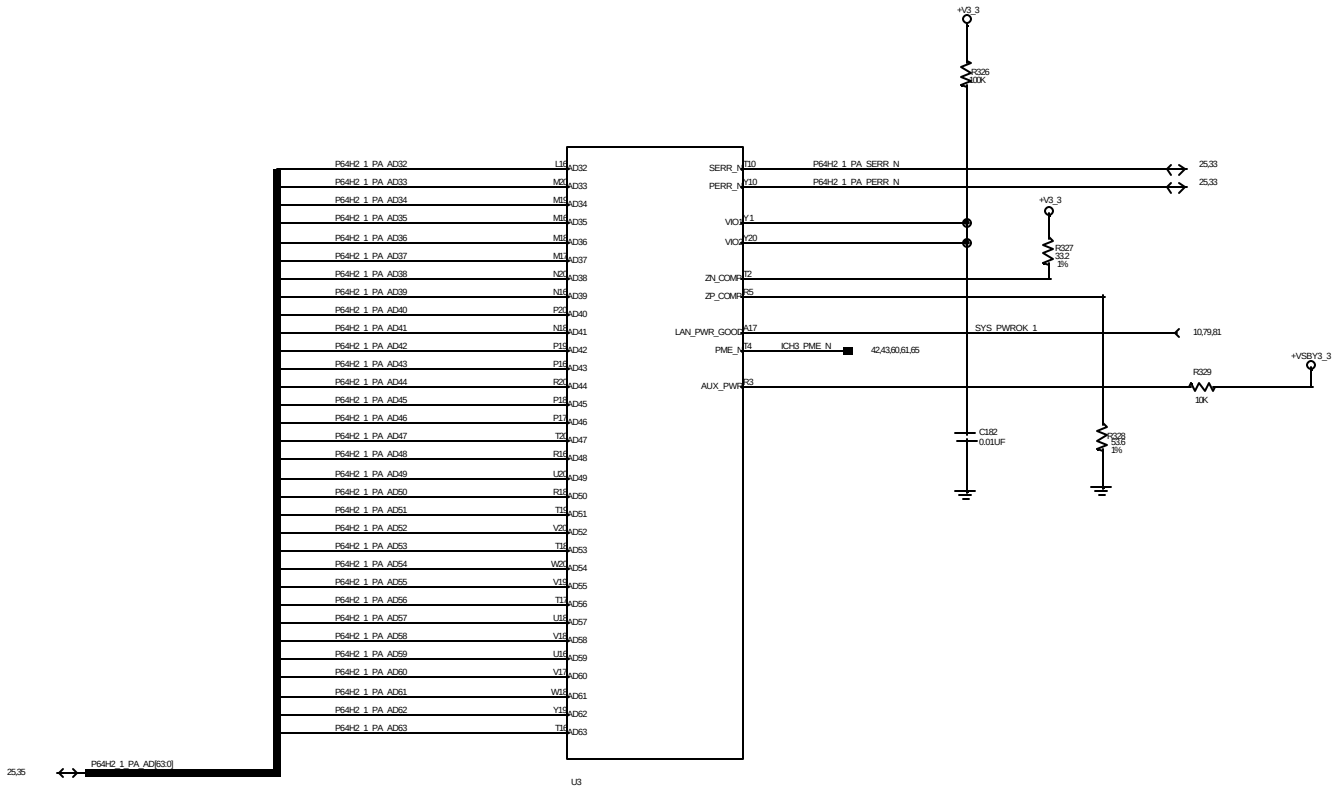
TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630		DRAWN BY:	PROJECT: KC533
		LAST REVISED: 11/18/02	34 OF 85

Gigabit Ethernet Controller (Part 1)



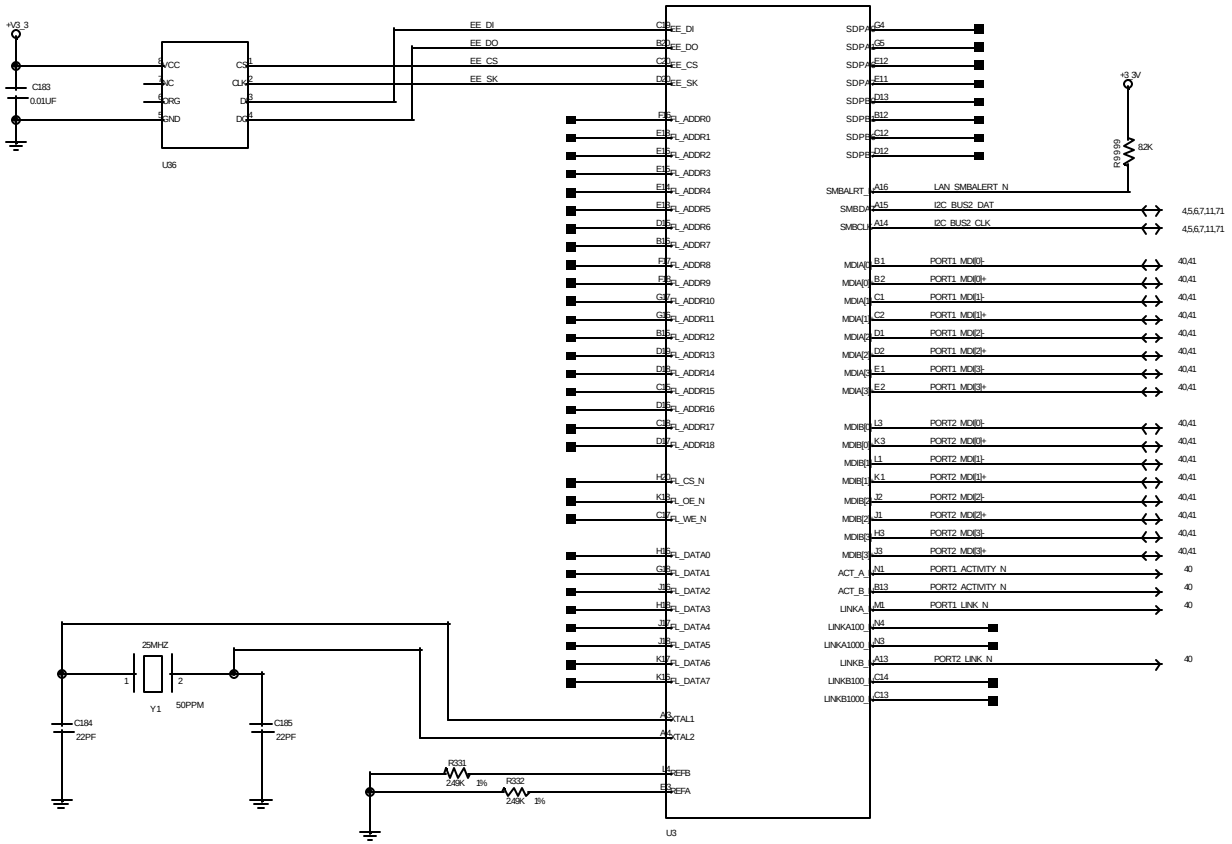
TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD			REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:		PROJECT: KC533
	LAST REVISED: 11/18/02		35 OF 85

Gigabit Ethernet Controller (Part 2)



TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
	LAST REVISED: 11/18/02	36 OF 85

Gigabit Ethernet Controller (Part 3)



Port 2 is not available for
Intel (R) 82545EM Gigabit Etherenet controller

REFB is NC for Intel (R) 82545EM Gigabit Etherenet controller

TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV:	1.0
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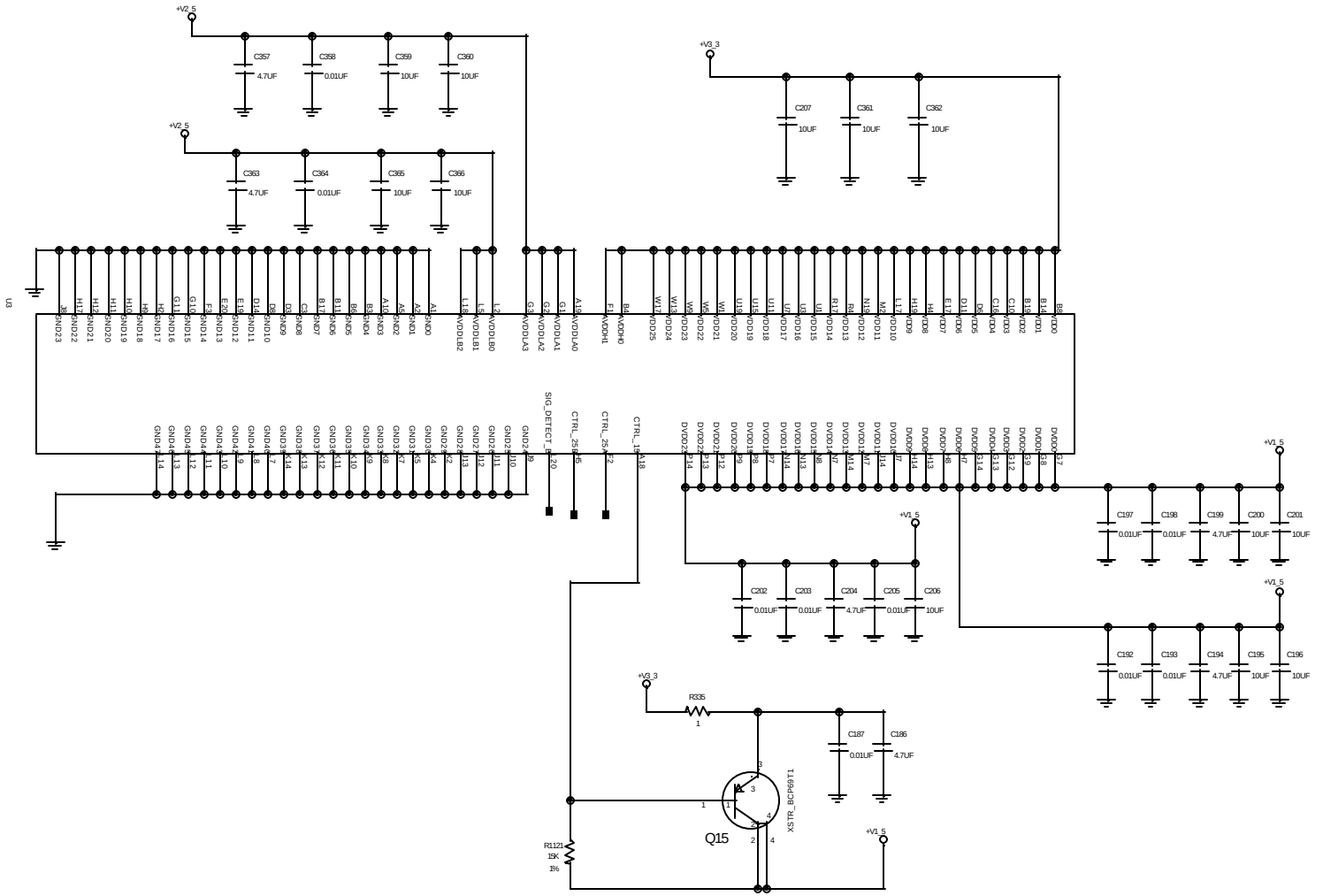
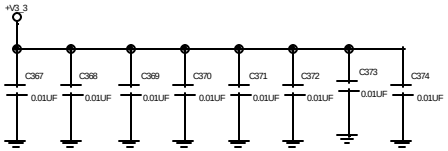
	LAST REVISED: 11/18/02	37 OF 85	

Gigabit Ethernet Controller (Part 4)



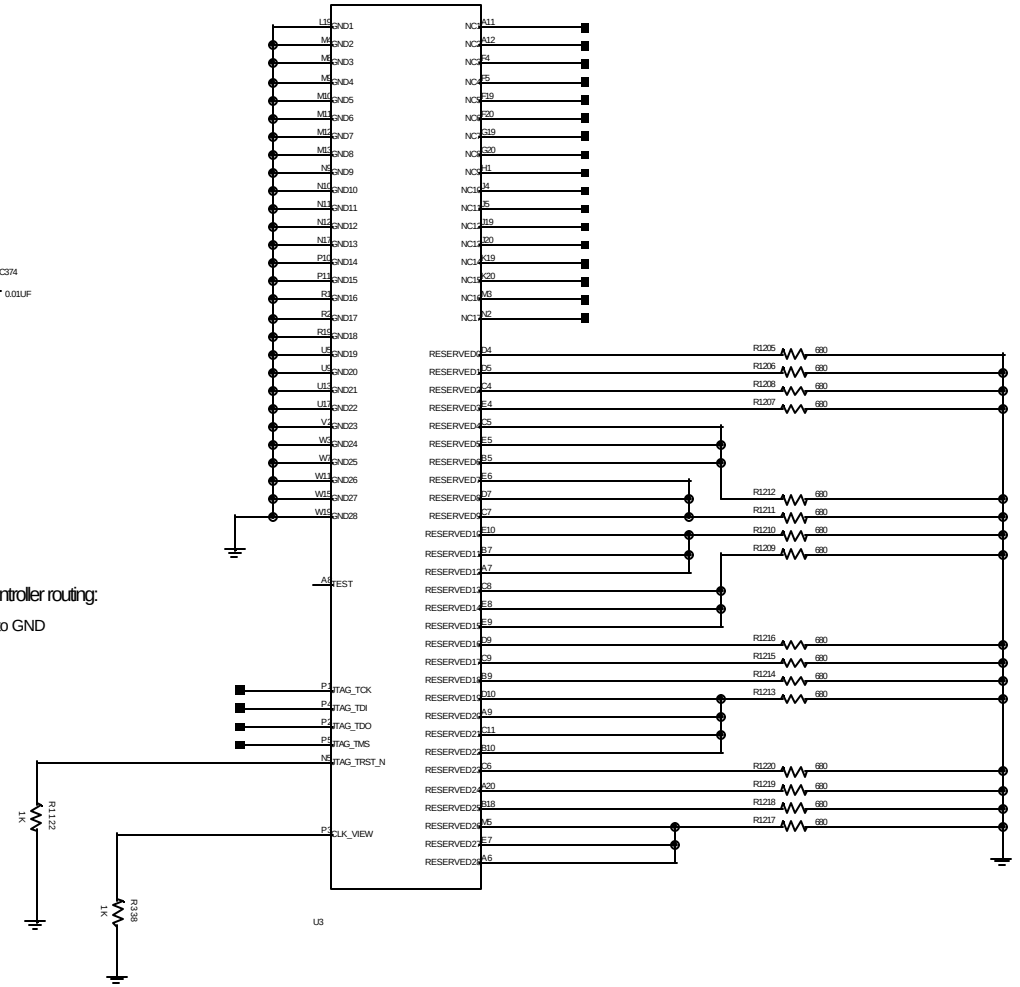
TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
	LAST REVISED: 11/18/02	38 OF 85

Gigabit Ethernet Controller (Part 5)



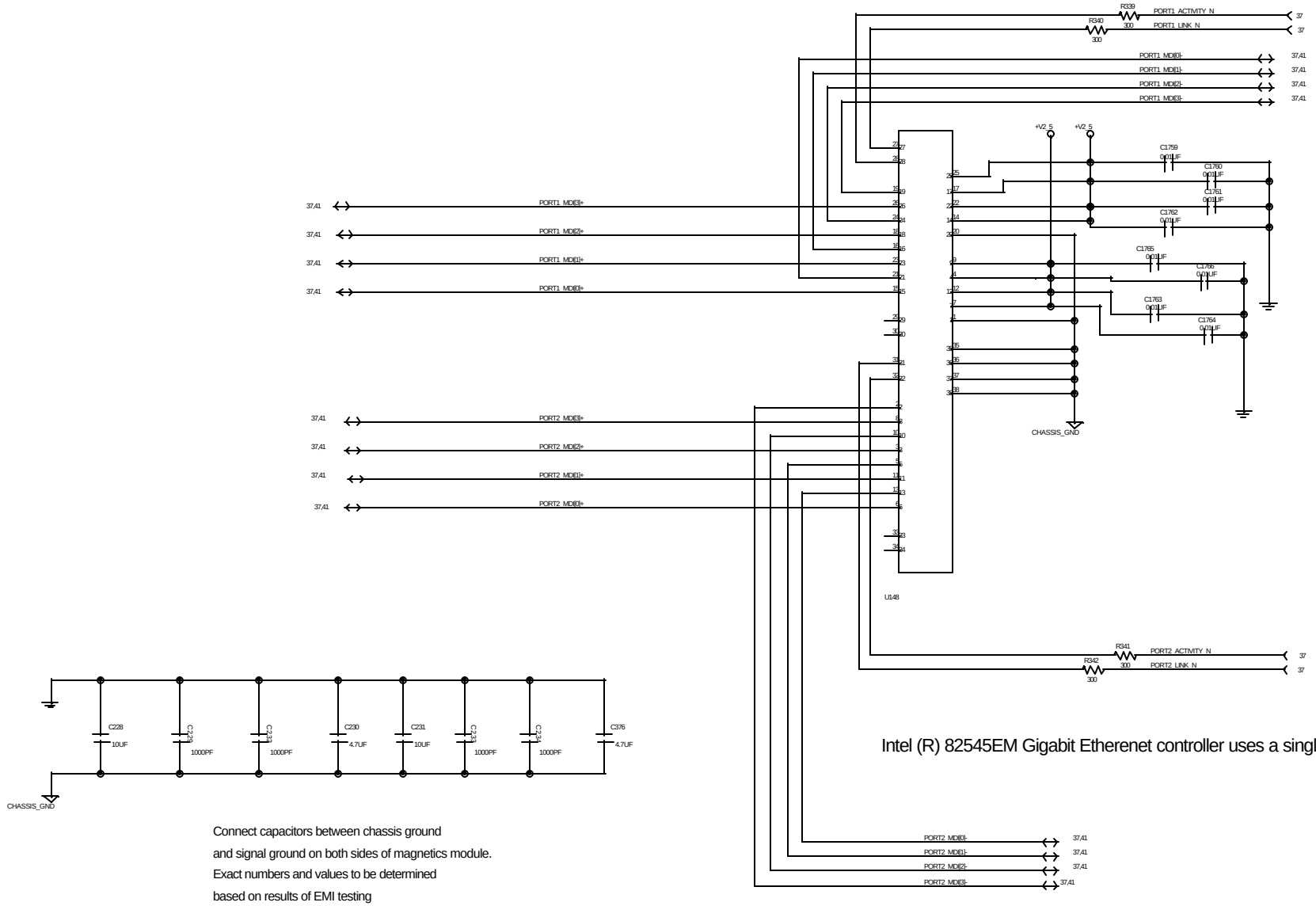
Intel (R) 82545EM Gigabit Etherenet controller routing:

Pins A20, B18, M5 tie to GND



TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
	LAST REVISED: 11/18/02	39 OF 85

Dual RJ-45 Ethernet Connectors

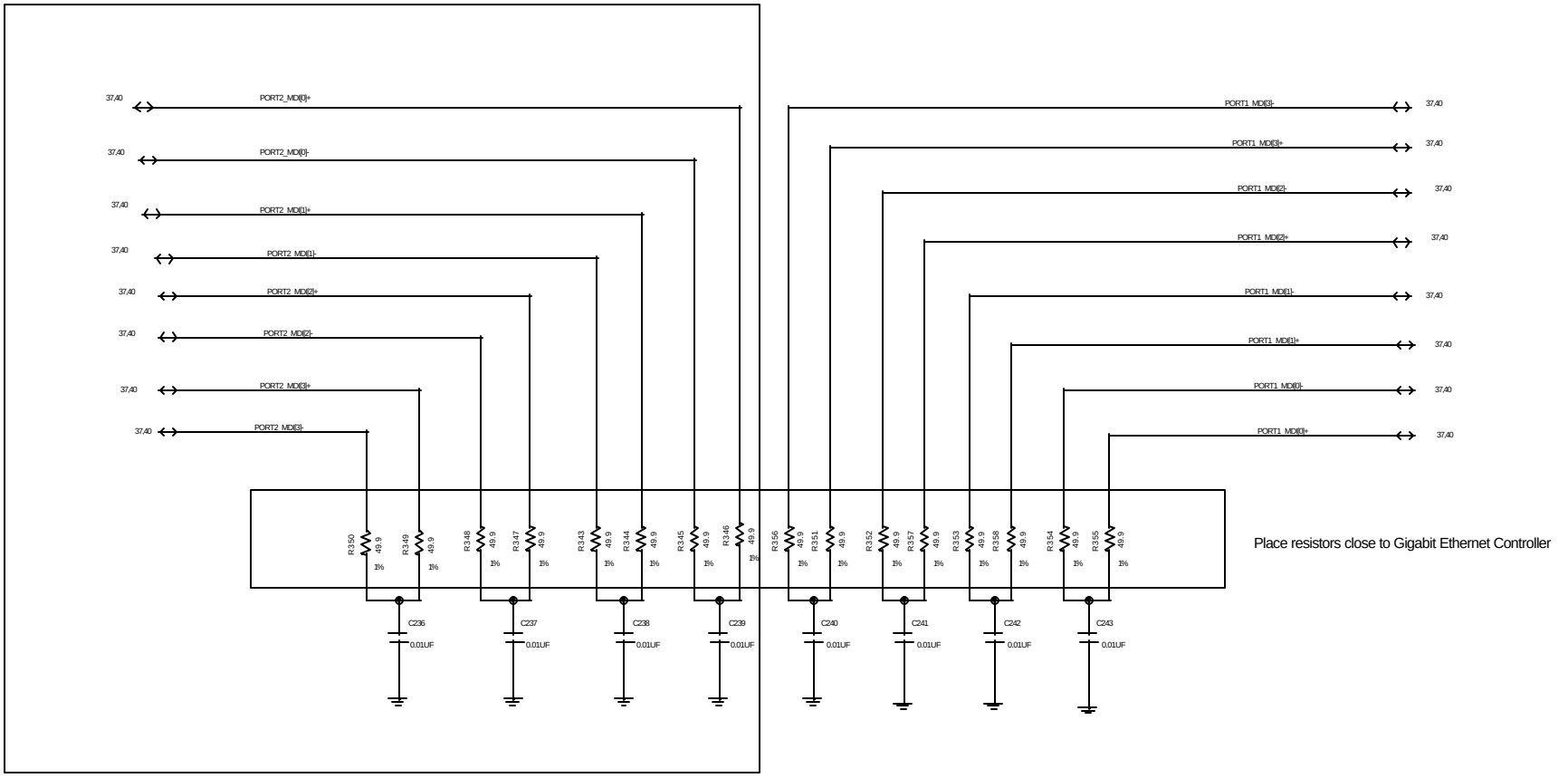


Intel (R) 82545EM Gigabit Etherenet controller uses a single RJ-45 port

Connect capacitors between chassis ground
and signal ground on both sides of magnetics module.
Exact numbers and values to be determined
based on results of EMI testing

TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
	LAST REVISED: 11/18/02	40 OF 85

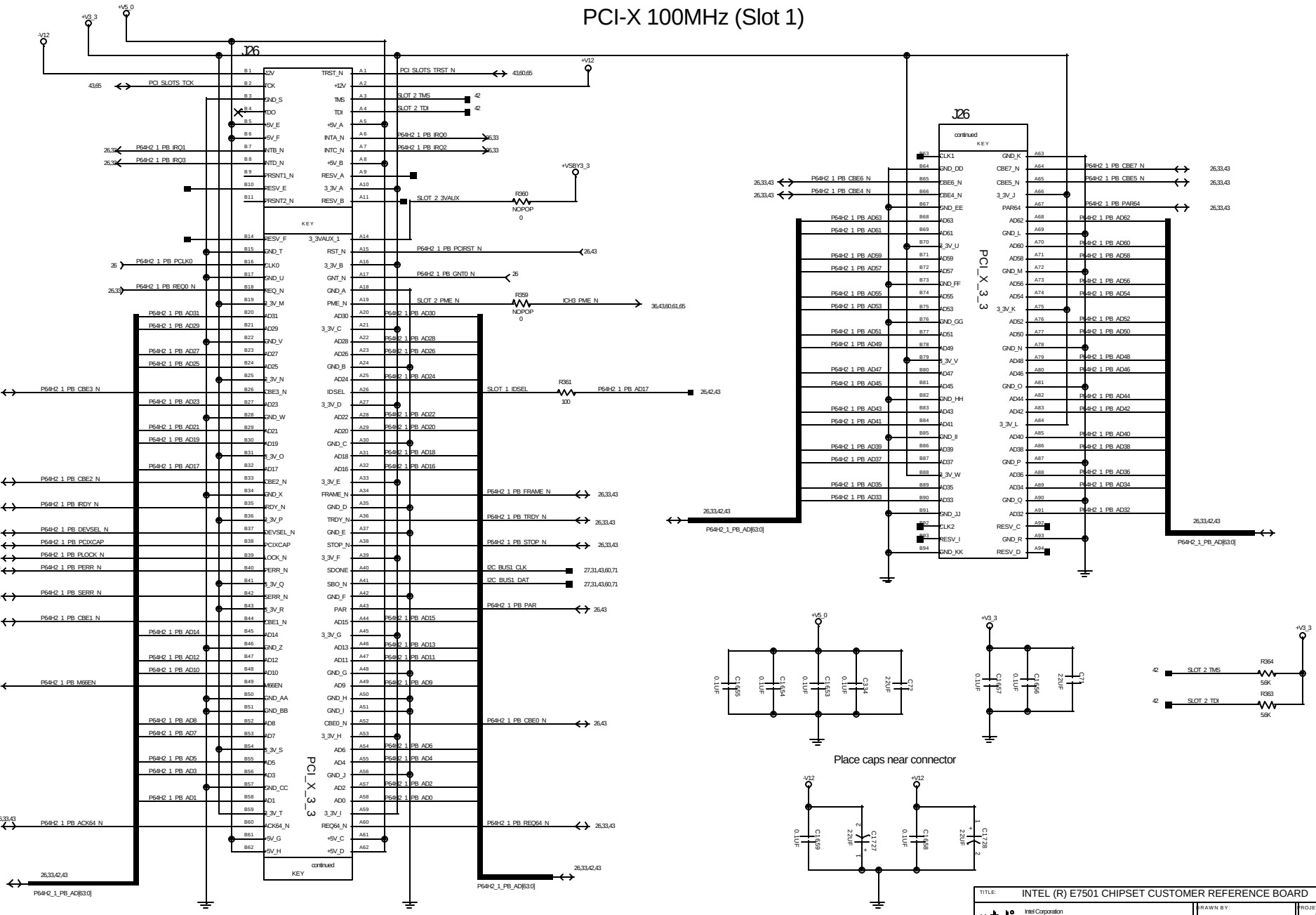
Ethernet Port Terminators



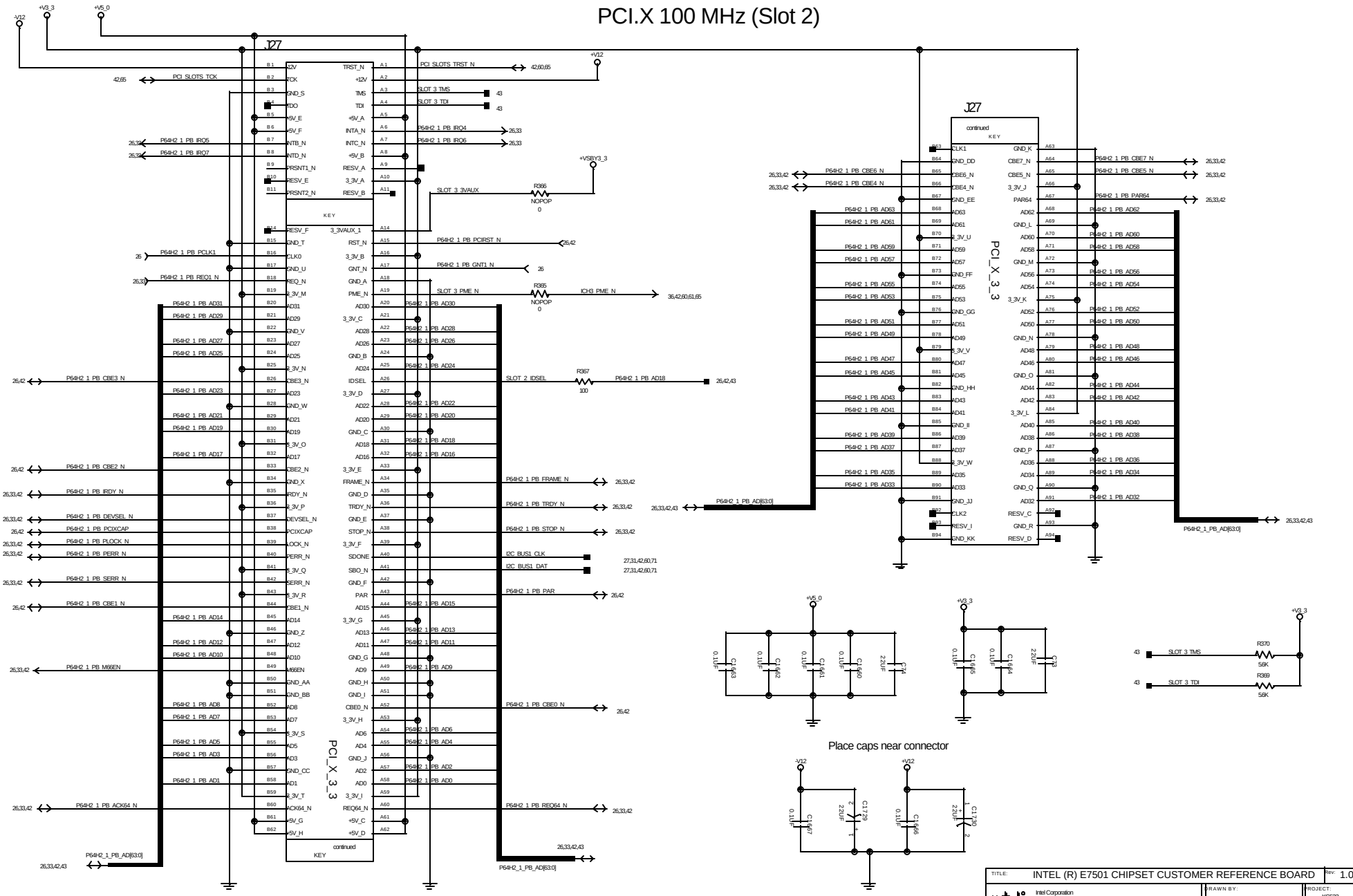
For use on Intel(R) 82546 EB

TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD			REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533	
	LAST REVISED: 11/18/02	41 OF 85	

PCI-X 100MHz (Slot 1)



PCI.X 100 MHz (Slot 2)



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REV:	1.0
Intel Corporation	1900 Prairie City Road, Folsom, California 095630
DRAWN BY:	
PROJECT:	KC533
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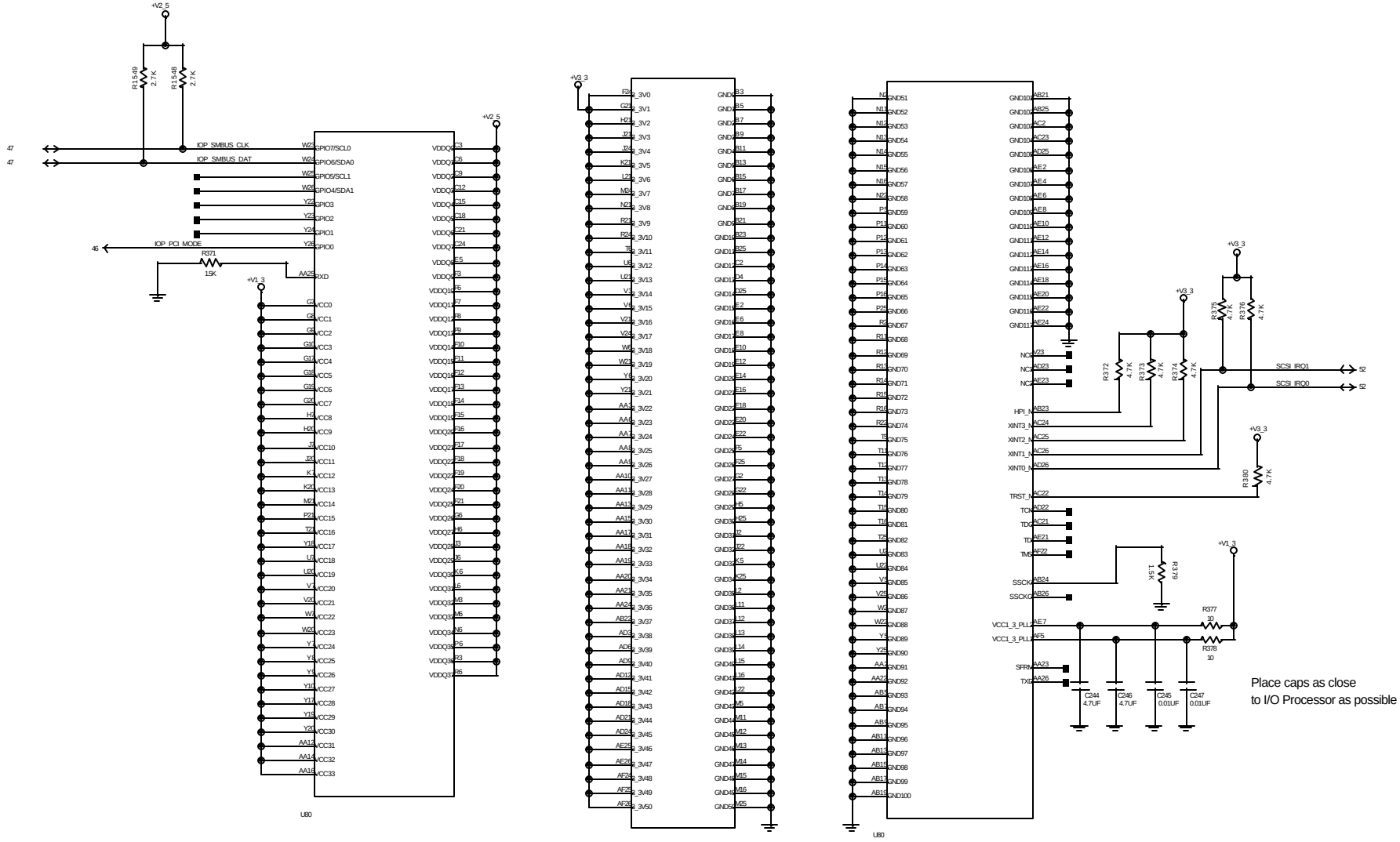
I/O Processor (Part 1)



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
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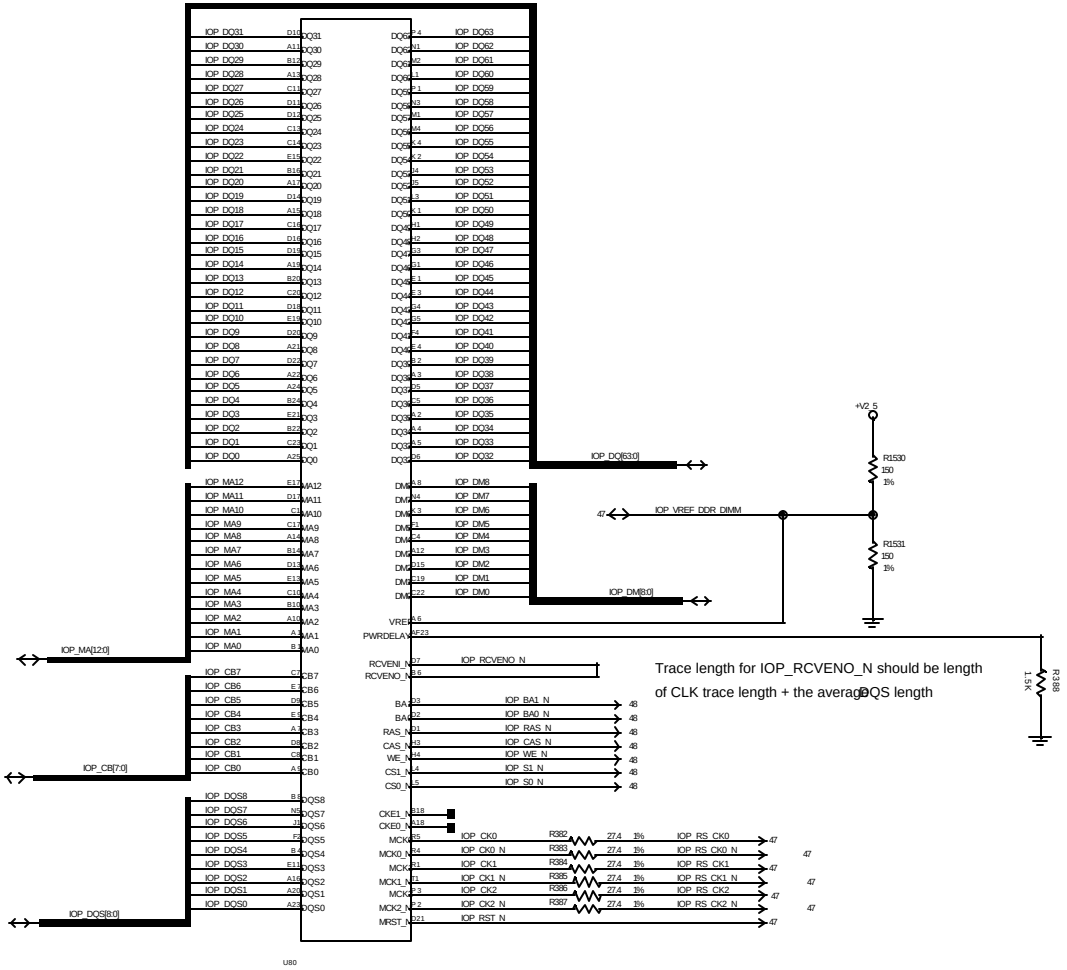
I/O Processor (Part 2)

IOP DDR Interface



TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
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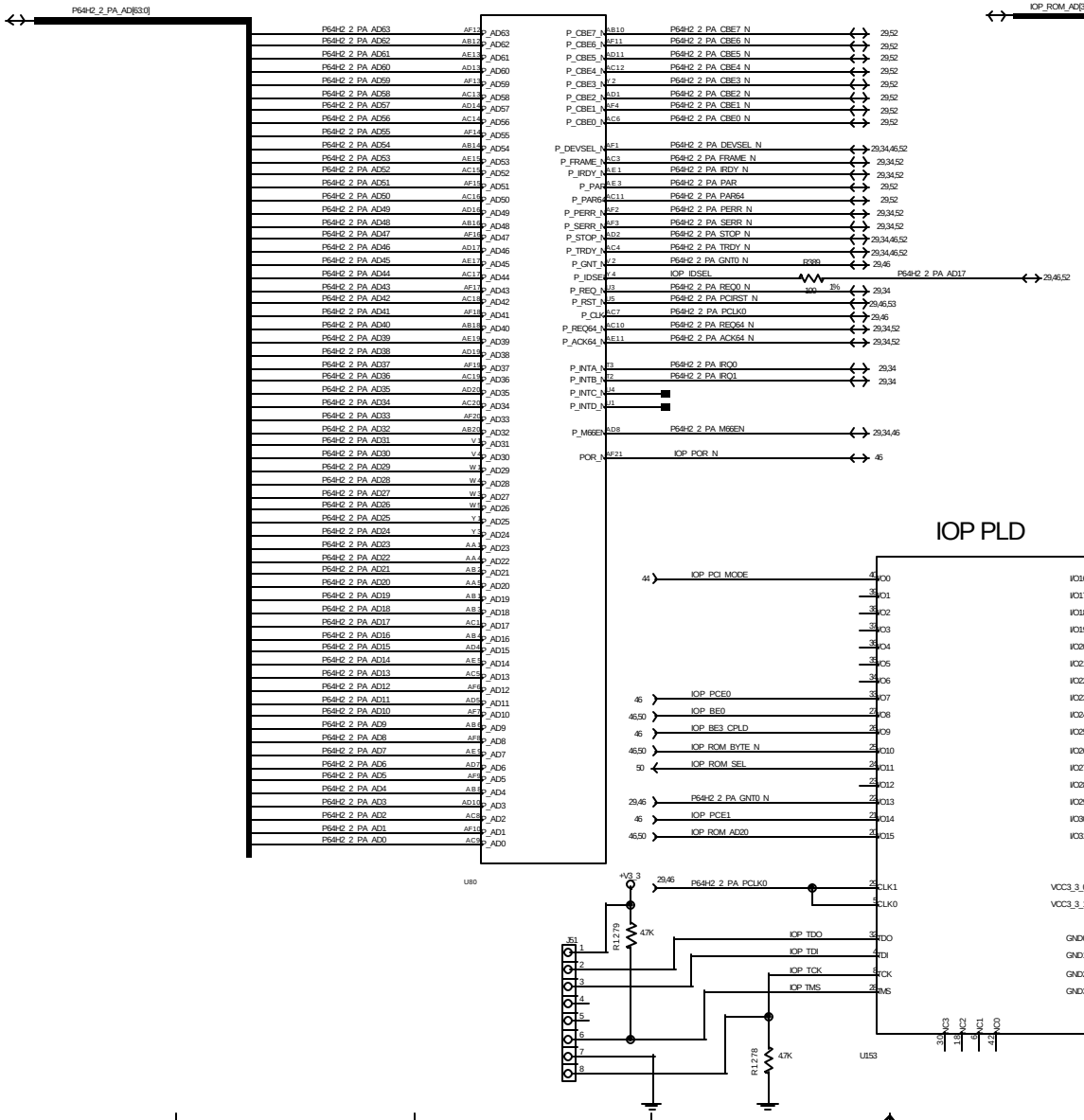
I/O Processor (Part 3)

IOP PCI.X Interface



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	
DRAWN BY:	
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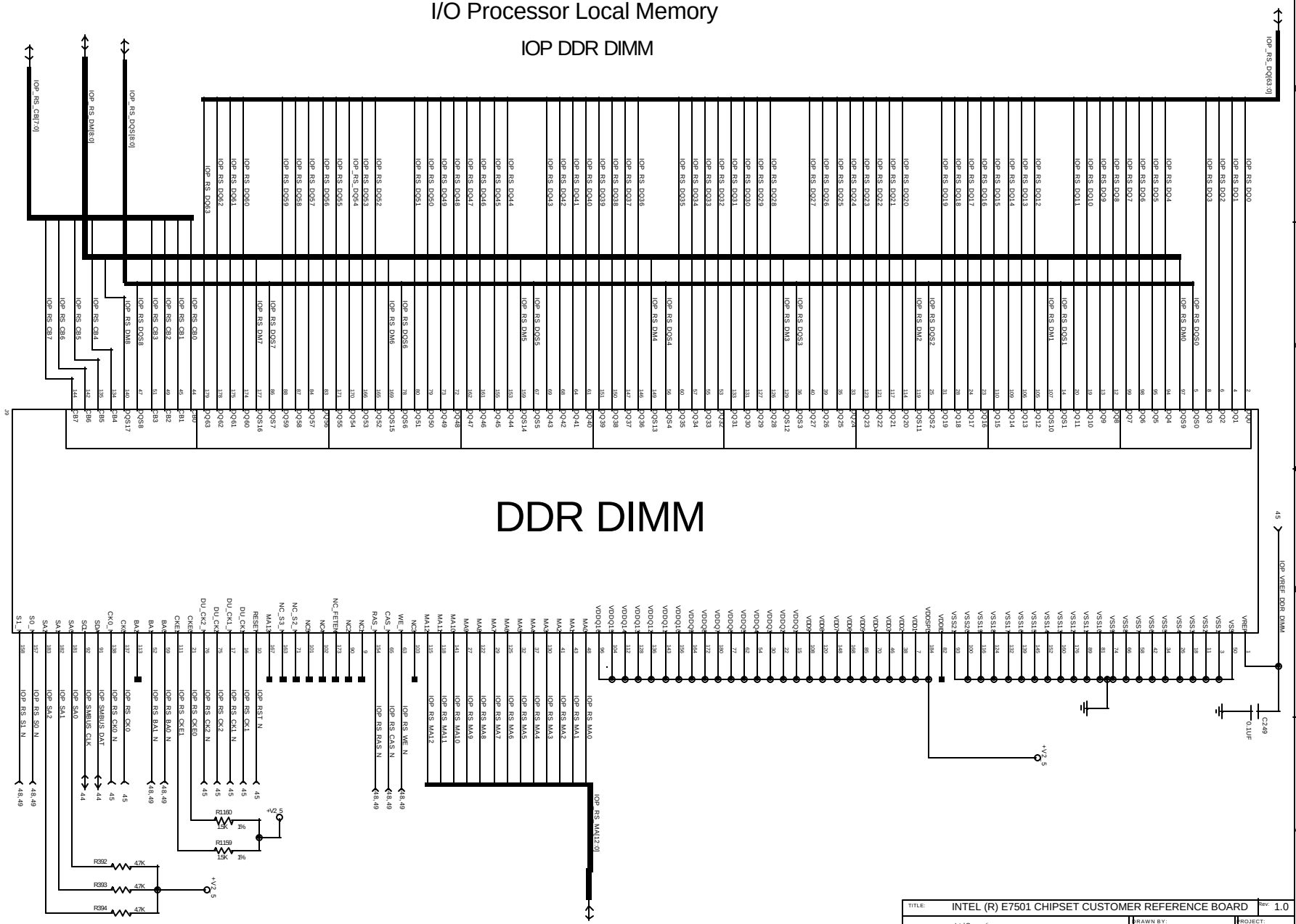
I/O Processor Local Memory

IOP DDR DIMM



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Intel Corporation 1900 Prairie City Road Folsom, California 095630	
DRAWN BY:	
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LAST REVISED:	11/18/02
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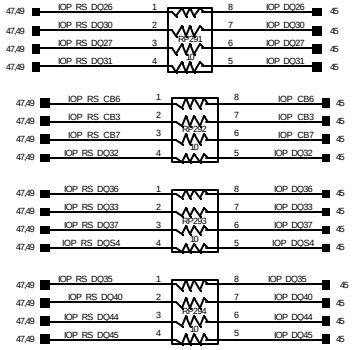
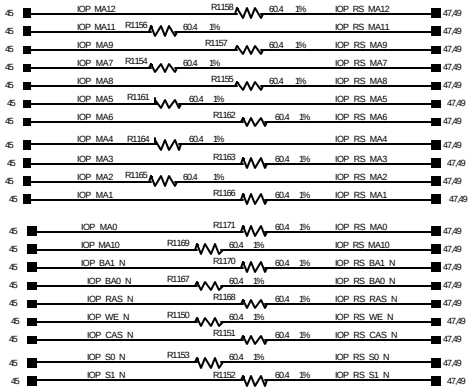
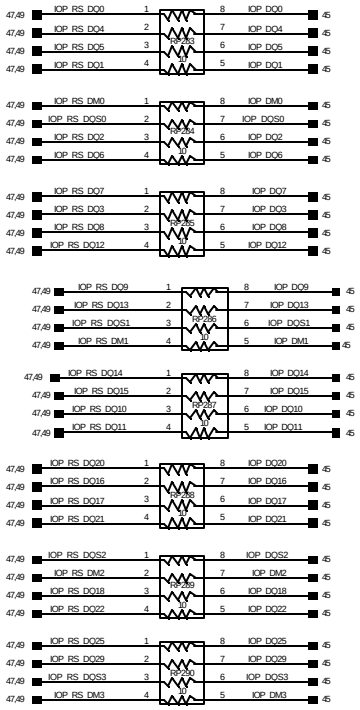
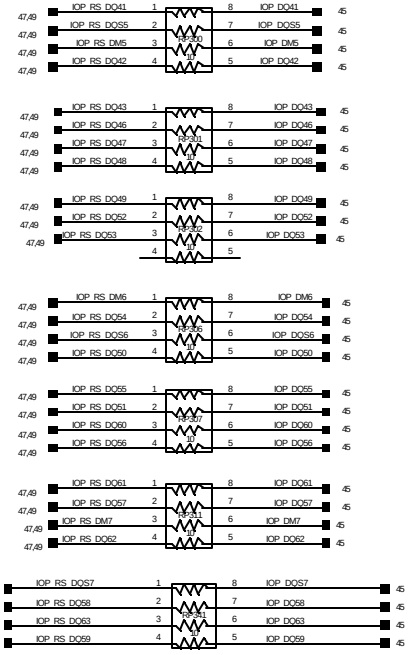
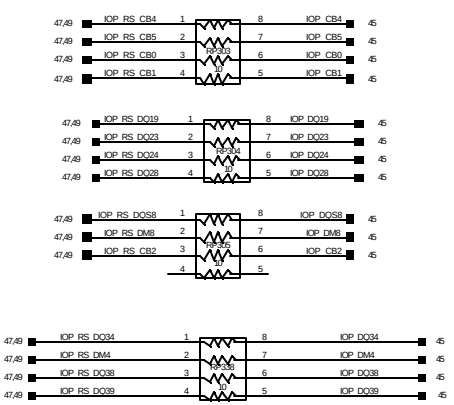
I/O Processor Local Memory Series Resistors











TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
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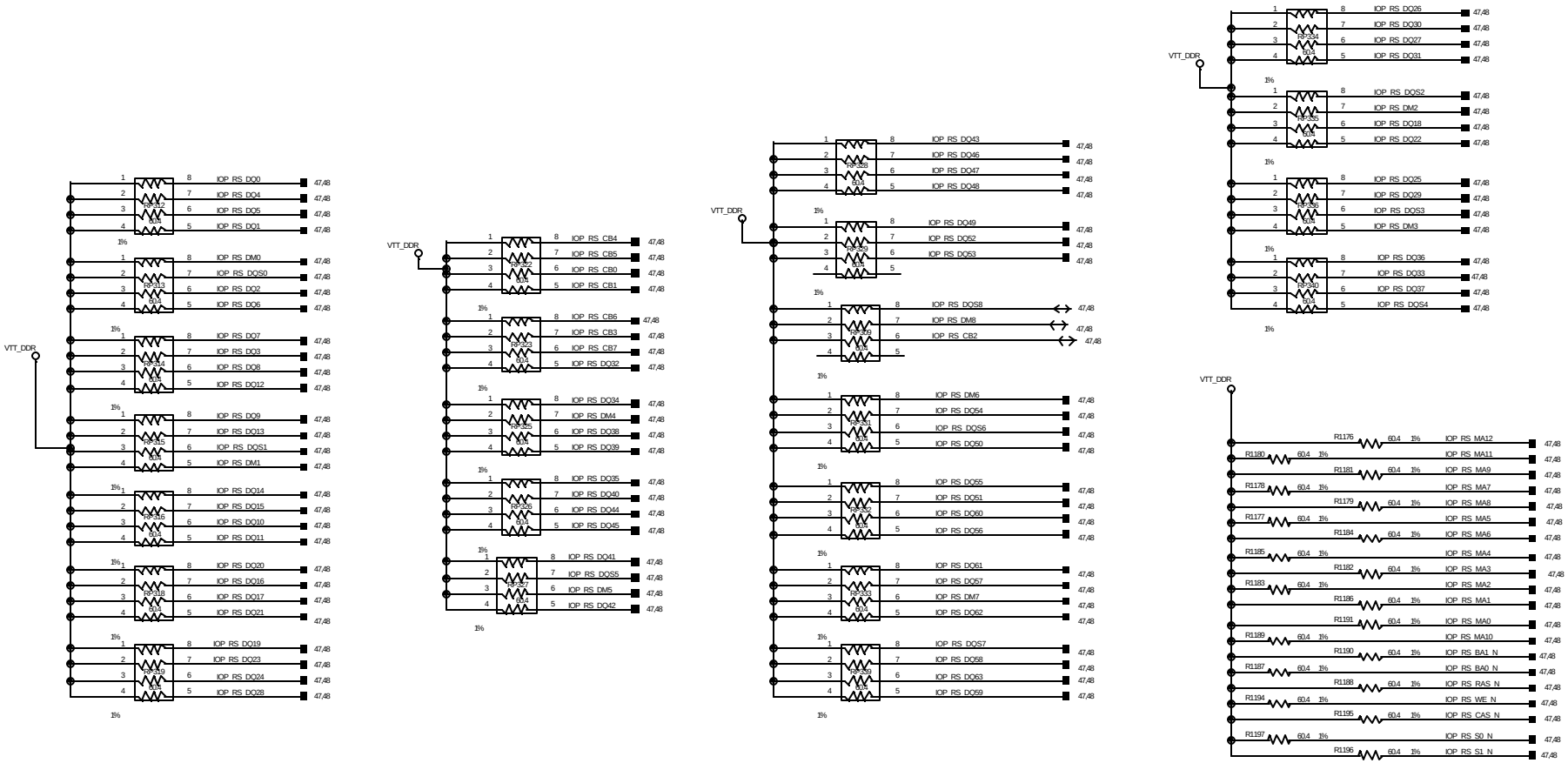
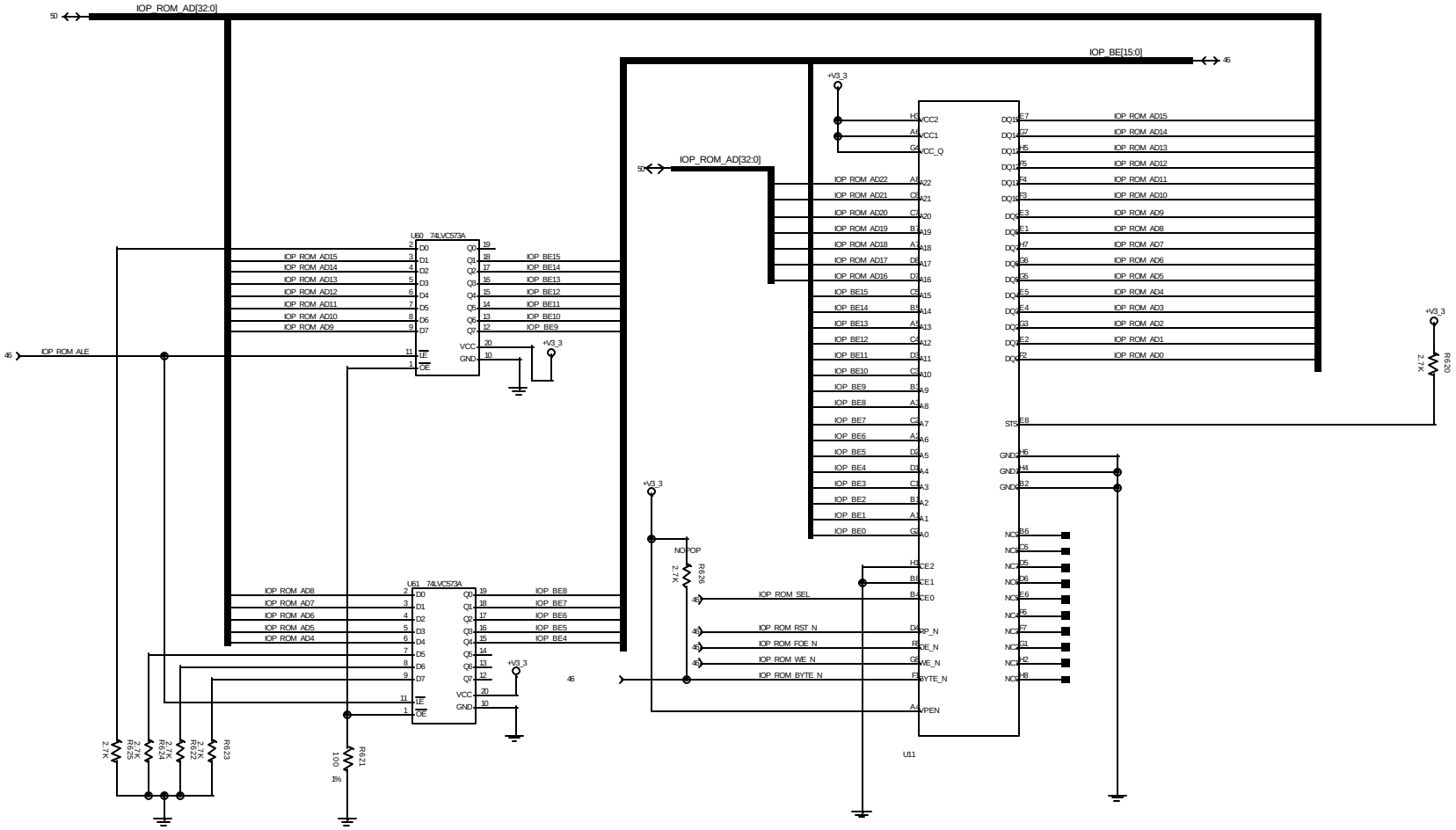
I/O Processor Local Memory Termination Resistors



All 60.4 ohm pull up resistors should be 1% tolerant

TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD			REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533	
	LAST REVISED: 11/18/02	49 OF 85	

I/O Processor ROM



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV:	1.0
Intel Corporation	1900 Prairie City Road, Folsom, California 095630
DRAWN BY:	
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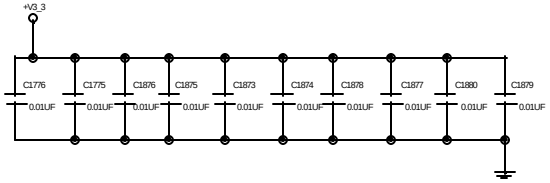
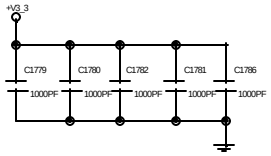
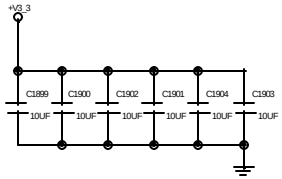
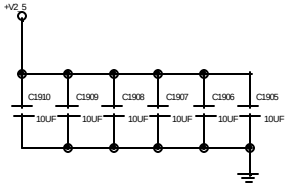
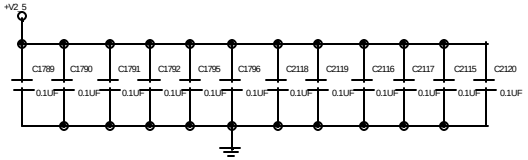
I/O Processor Decoupling

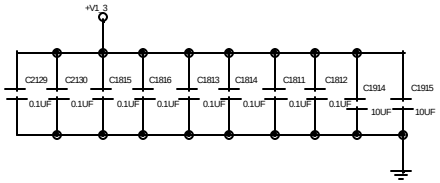


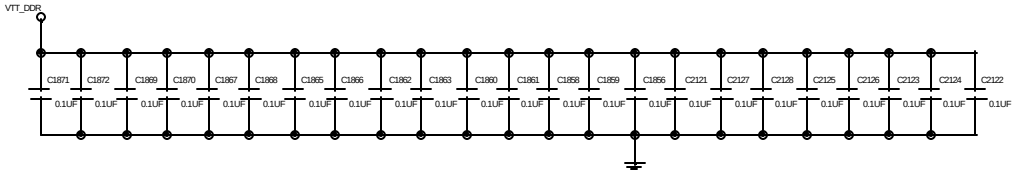












TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD			REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533	
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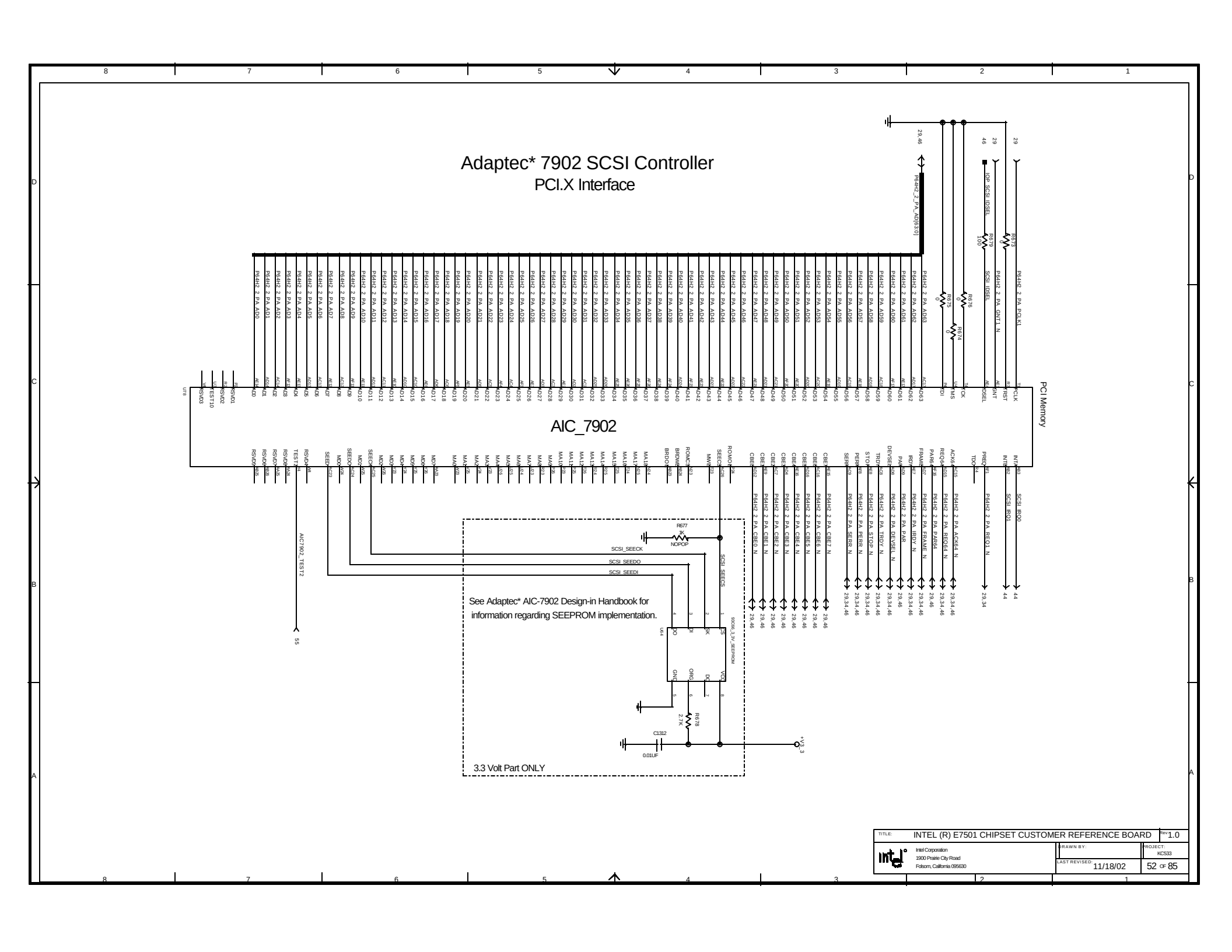
Adaptec* 7902 SCSI Controller
PCI.X Interface
AIC_7902
PCI Memory
See Adaptec* AIC-7902 Design-in Handbook for information regarding SEEPROM implementation.
3.3 Volt Part ONLY
SCSI_SEECK
SCSI_SEEDO
SCSI_SEEDI
SCSI_SEECS
93C66_3.3V_SEEPROM
R677
1K
NOPOP
R678
2.7K
C1312
0.01UF
R675
0
R676
0
R674
0
R679
100
R673
0
SCSI_IDSEL
SCSI_IRQ0
SCSI_IRQ1
TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV 1.0
Intel Corporation
1900 Prairie City Road
Folsom, California 095630
DRAWN BY:
PROJECT: KC533
LAST REVISED: 11/18/02
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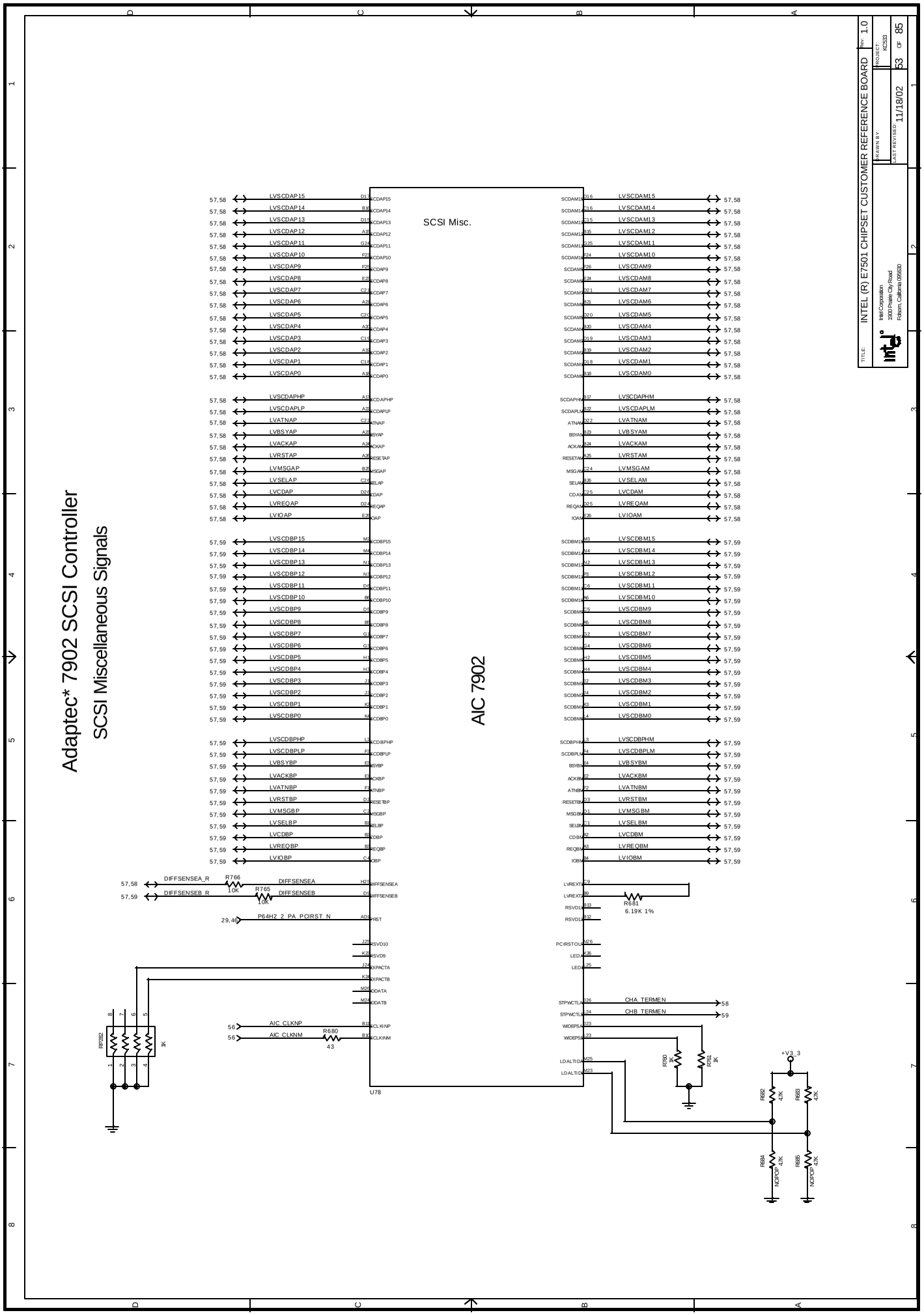
Adaptec* 7902 SCSI Controller
SCSI Miscellaneous Signals
SCSI Misc.
AIC 7902
U78
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LVSCDAP14
LVSCDAP13
LVSCDAP12
LVSCDAP11
LVSCDAP10
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LVSCDAP8
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LVSCDAP6
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LVSCDAPLM
LVATNAM
LVBSYAM
LVACKAM
LVRSTAM
LVMSGAM
LVSELAM
LVCDAM
LVREQAM
LVIOAM
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LVBSYBM
LVACKBM
LVATNBM
LVRSTBM
LVMSGBM
LVSELBM
LVCDBM
LVREQBM
LVIOBM
R681
6.19K 1%
CHA_TERMEN
CHB_TERMEN
R760
1K
R761
1K
+V3.3
R682
47K
R683
47K
R684
47K
NOPOP
R685
47K
NOPOP
TITLE:
INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV: 1.0
PROJECT:
KCS33
DRAWN BY:
LAST REVISED:
11/18/02
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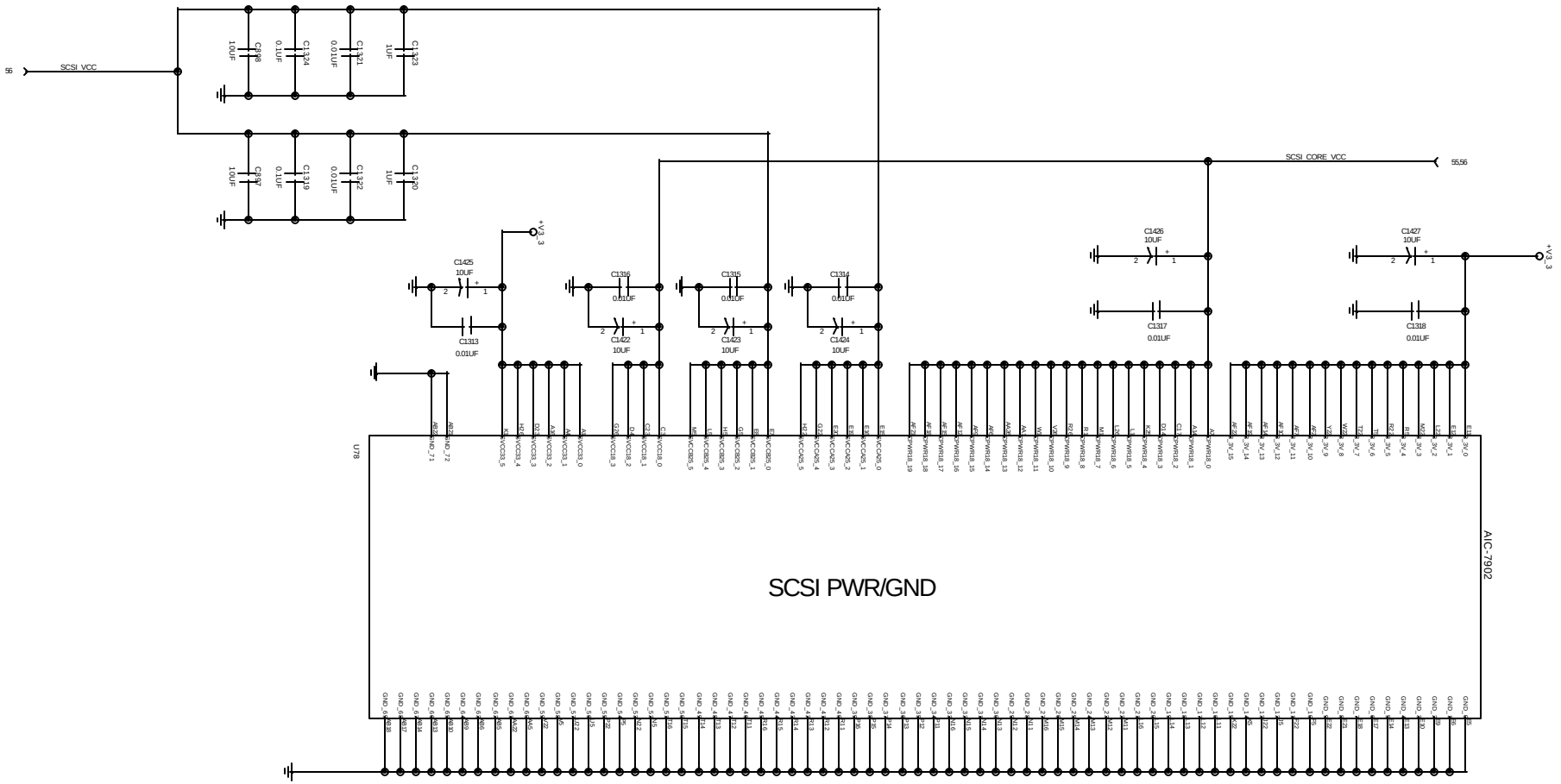
OF
85
Intel Corporation
3300 Prairie City Road
Folsom, California 95630

Adaptec* 7902 SCSI Controller

Power & GND



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REV:	1.0
Intel Corporation	1900 Prairie City Road, Folsom, California 095630
DRAWN BY:	
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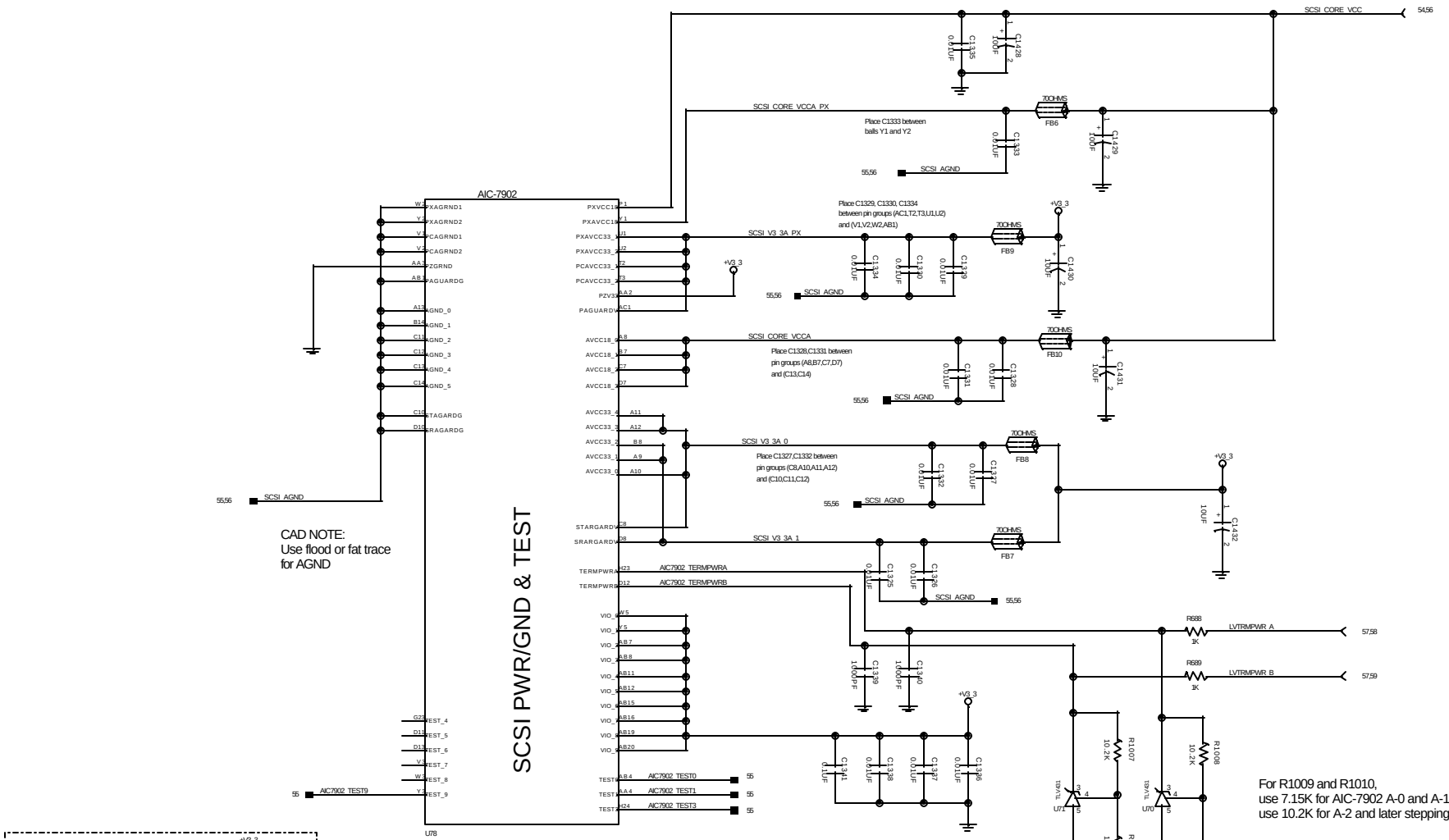
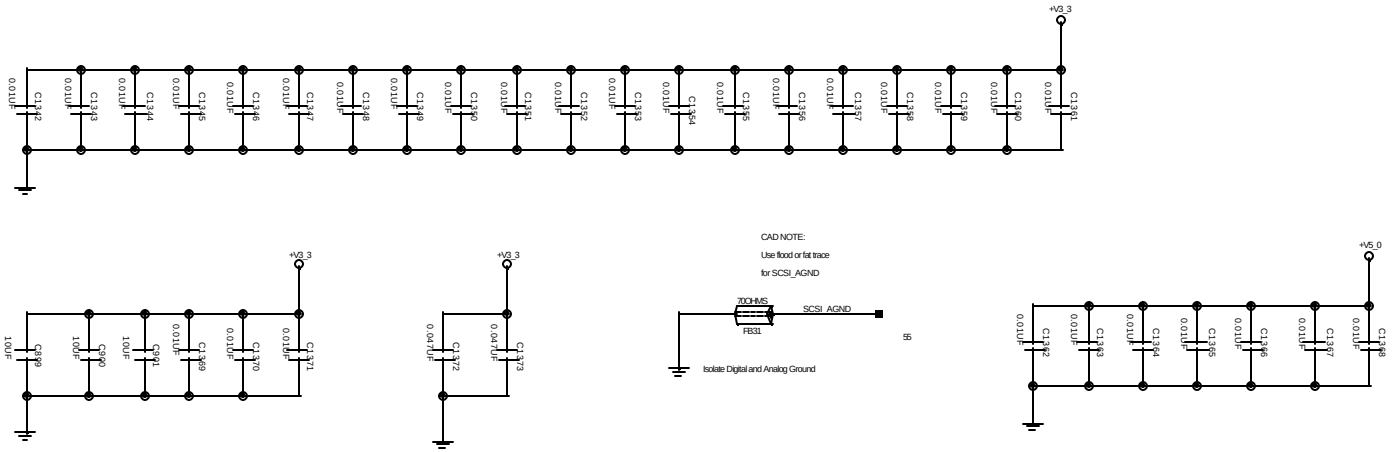
Adaptec* 7902 SCSI Controller

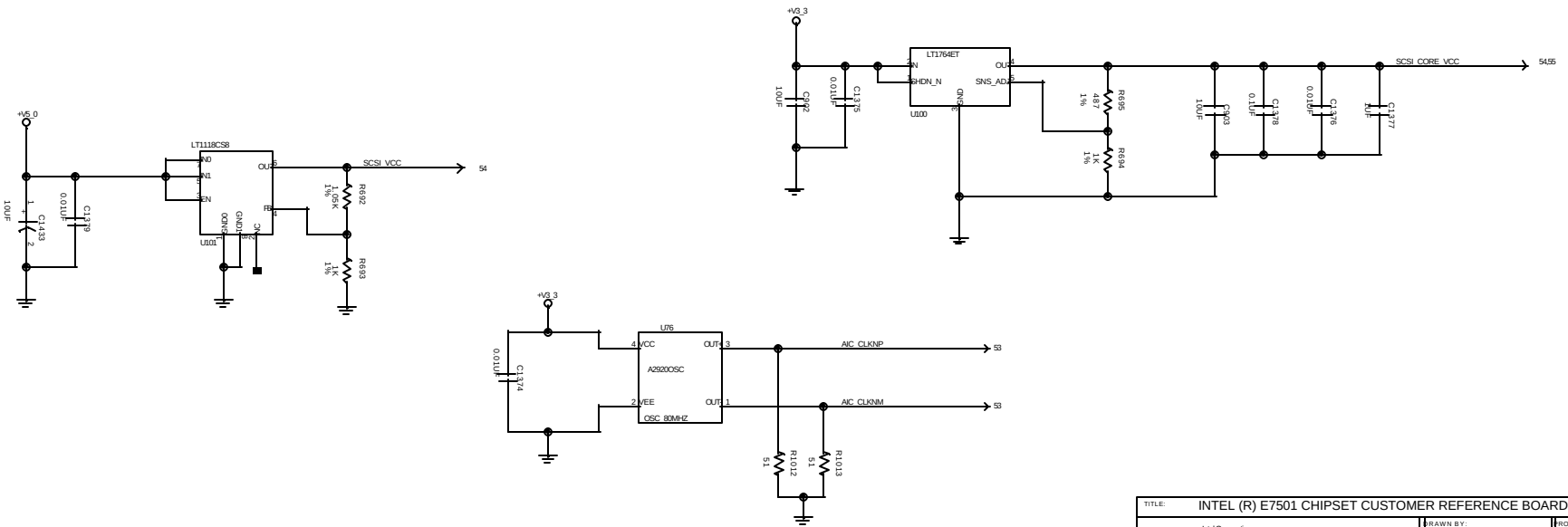


TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV.	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT:	KC533
	LAST REVISED: 11/18/02	55 OF 85	

AIC-7902 SCSI Decoupling



SCSI Voltage Regulators and SCSI Clock



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
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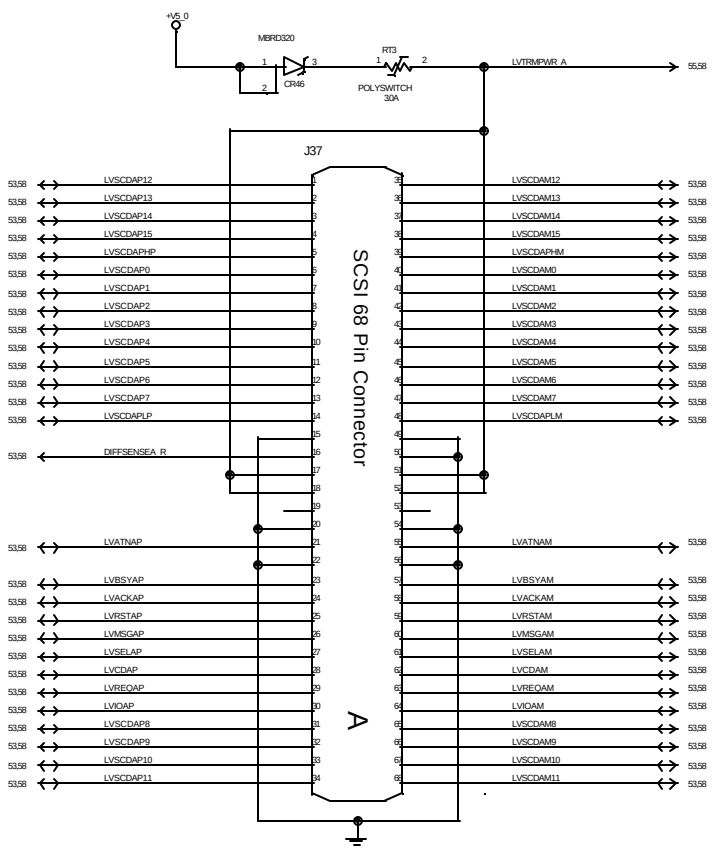
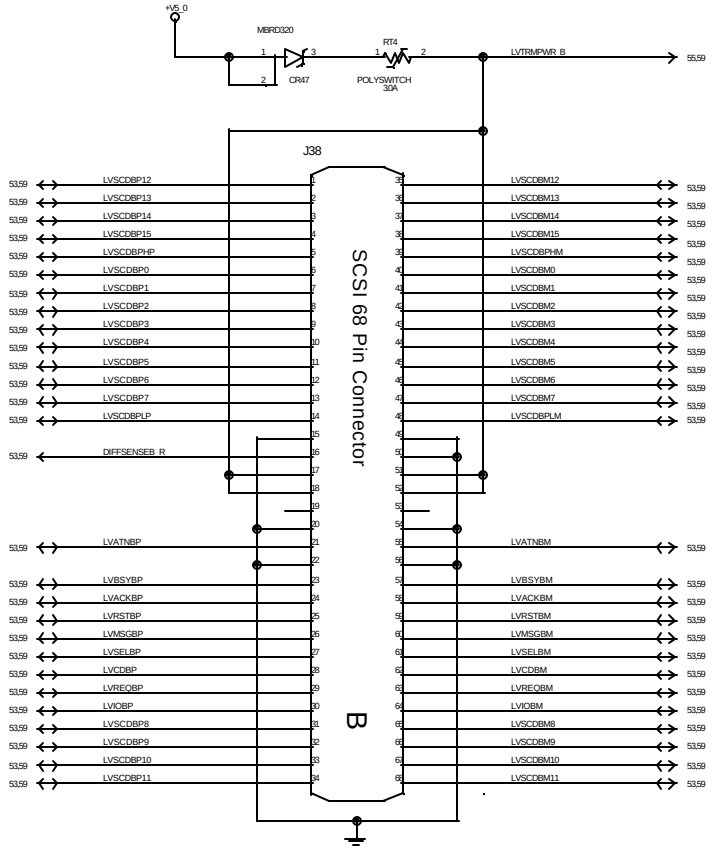
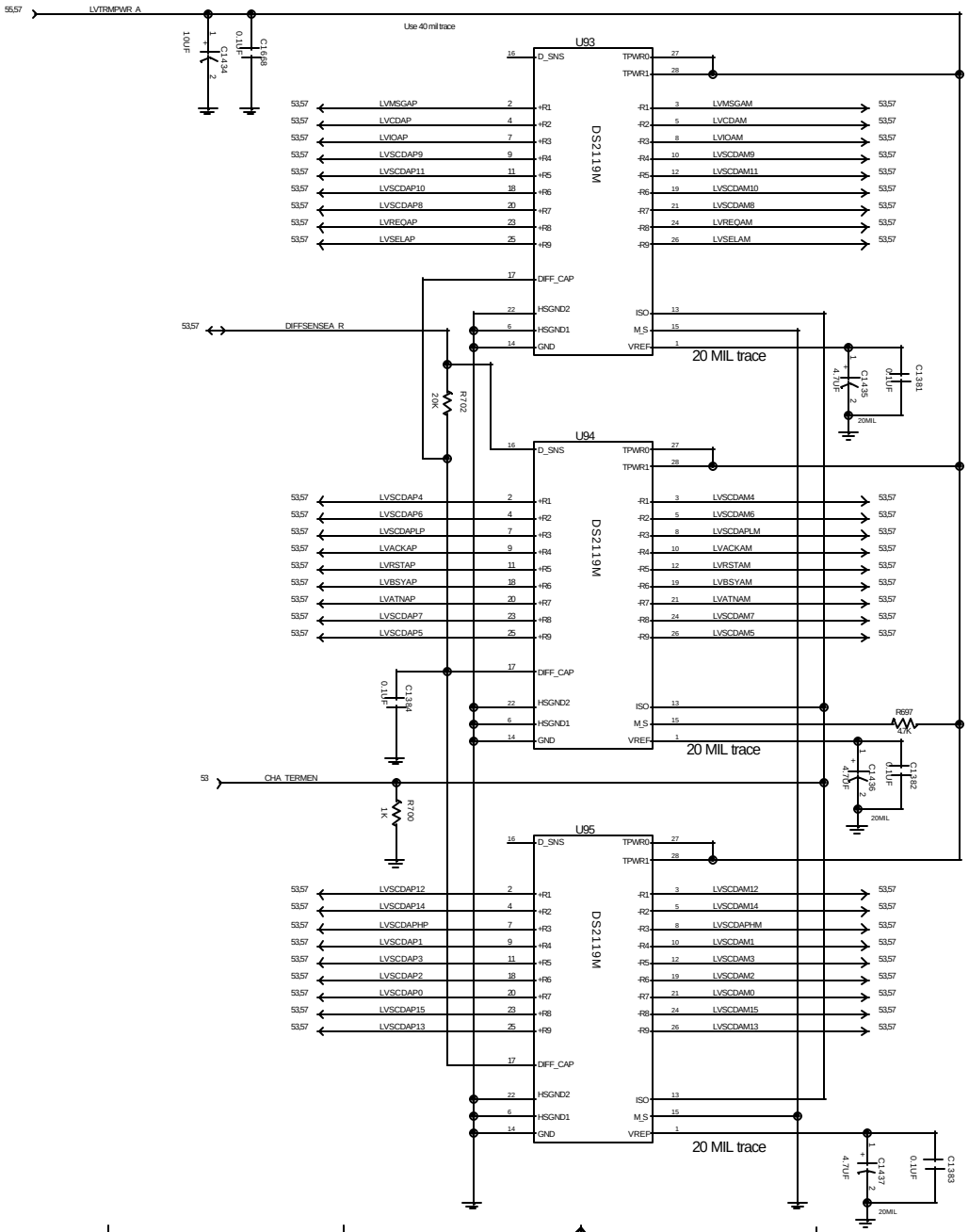
SCSI Connectors A and B





TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT:	KC533
	LAST REVISED: 11/18/02		57 OF 85

LVD/SE Termination for SCSI Channel A



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV:	1.0
Intel Corporation	1900 Prairie City Road, Folsom, California 095630
DRAWN BY:	
PROJECT:	KC533
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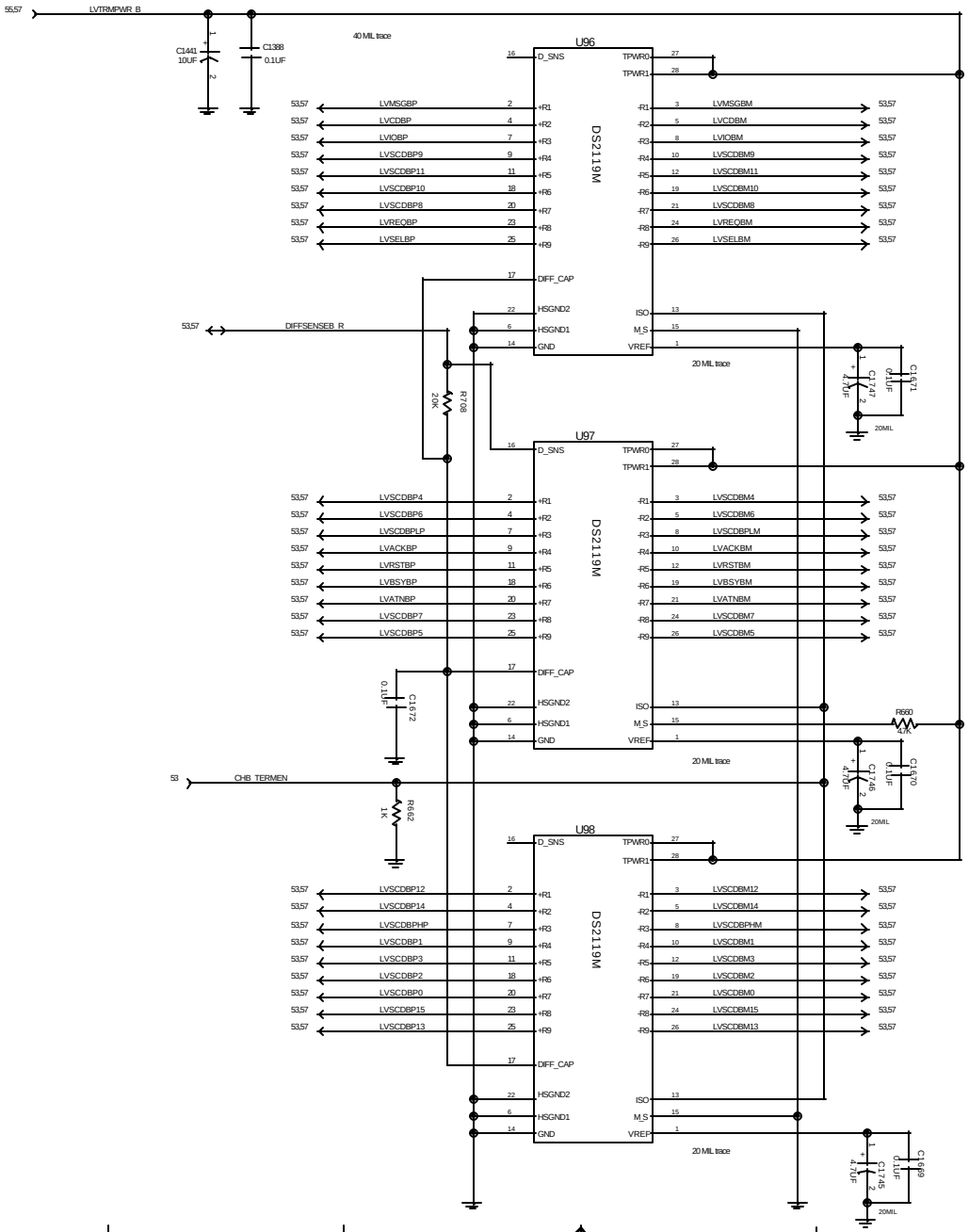
LVD/SE Termination for SCSI Channel B



TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
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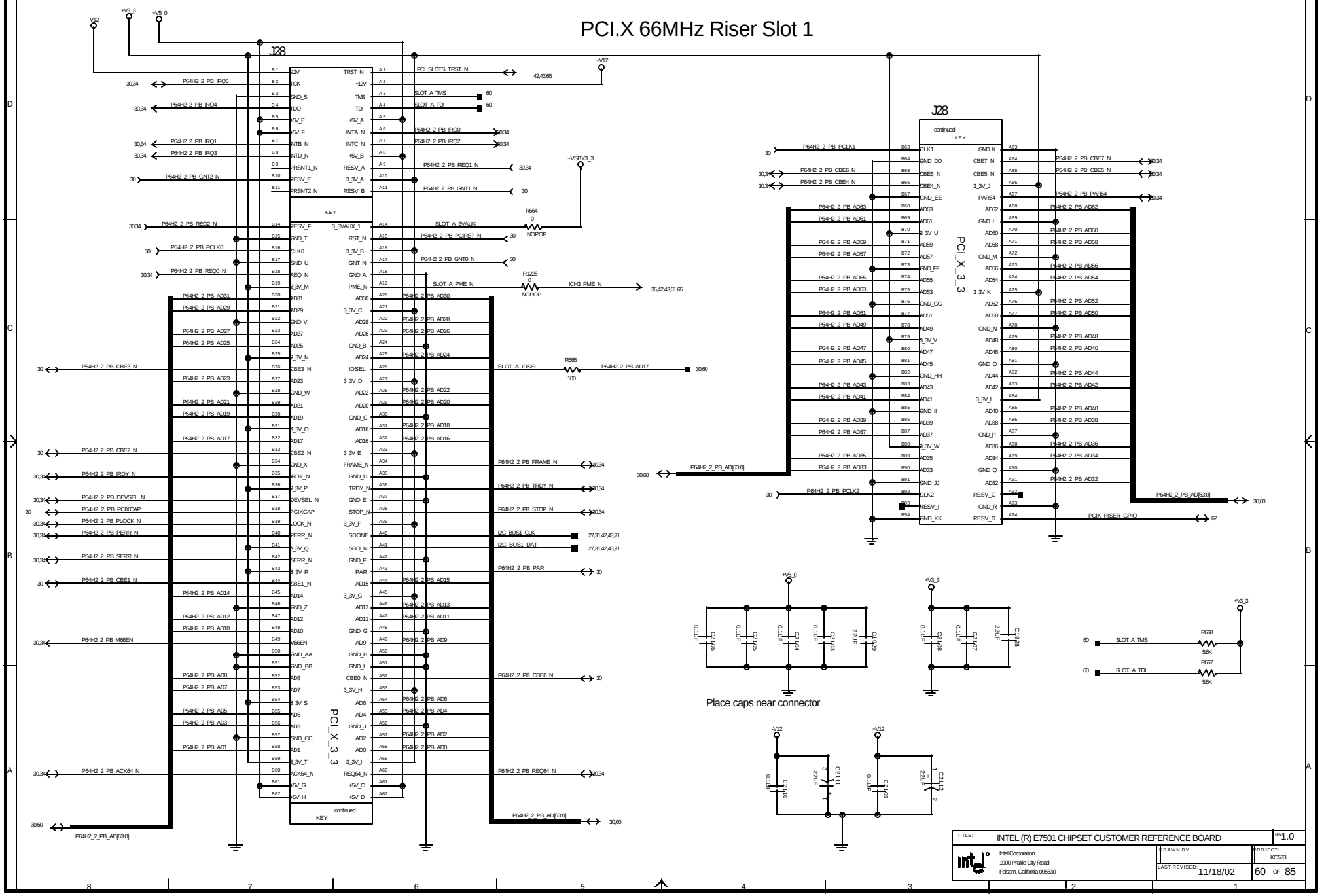
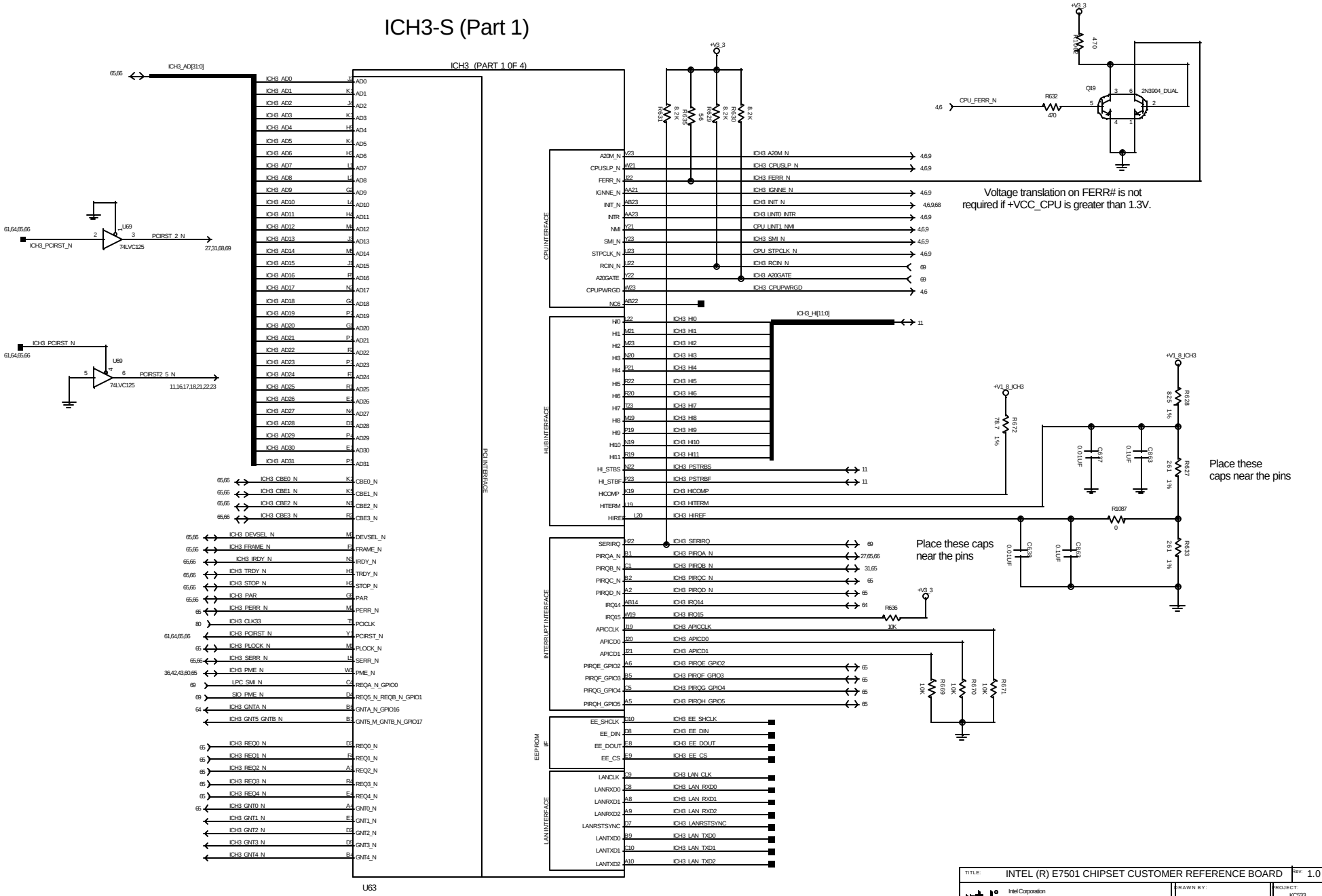
PCI.X 66MHz Riser Slot 1



ICH3-S (Part 1)


ICH3 (PART 1 0F 4)
ICH3_AD[31:0]
PCI INTERFACE
CPU INTERFACE
HUB INTERFACE
INTERRUPT INTERFACE
EEPROM I/F
LAN INTERFACE
U63
74LVC125
U69
ICH3_PCIRST_N
PCIRST_2_N
PCIRST2_5_N
CPU_FERR_N
2N3904_DUAL
Voltage translation on FERR# is not required if +VCC_CPU is greater than 1.3V.
Place these caps near the pins
Place these caps near the pins
TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
REV: 1.0
Intel Corporation
1900 Prairie City Road
Folsom, California 095630
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PROJECT: KC533
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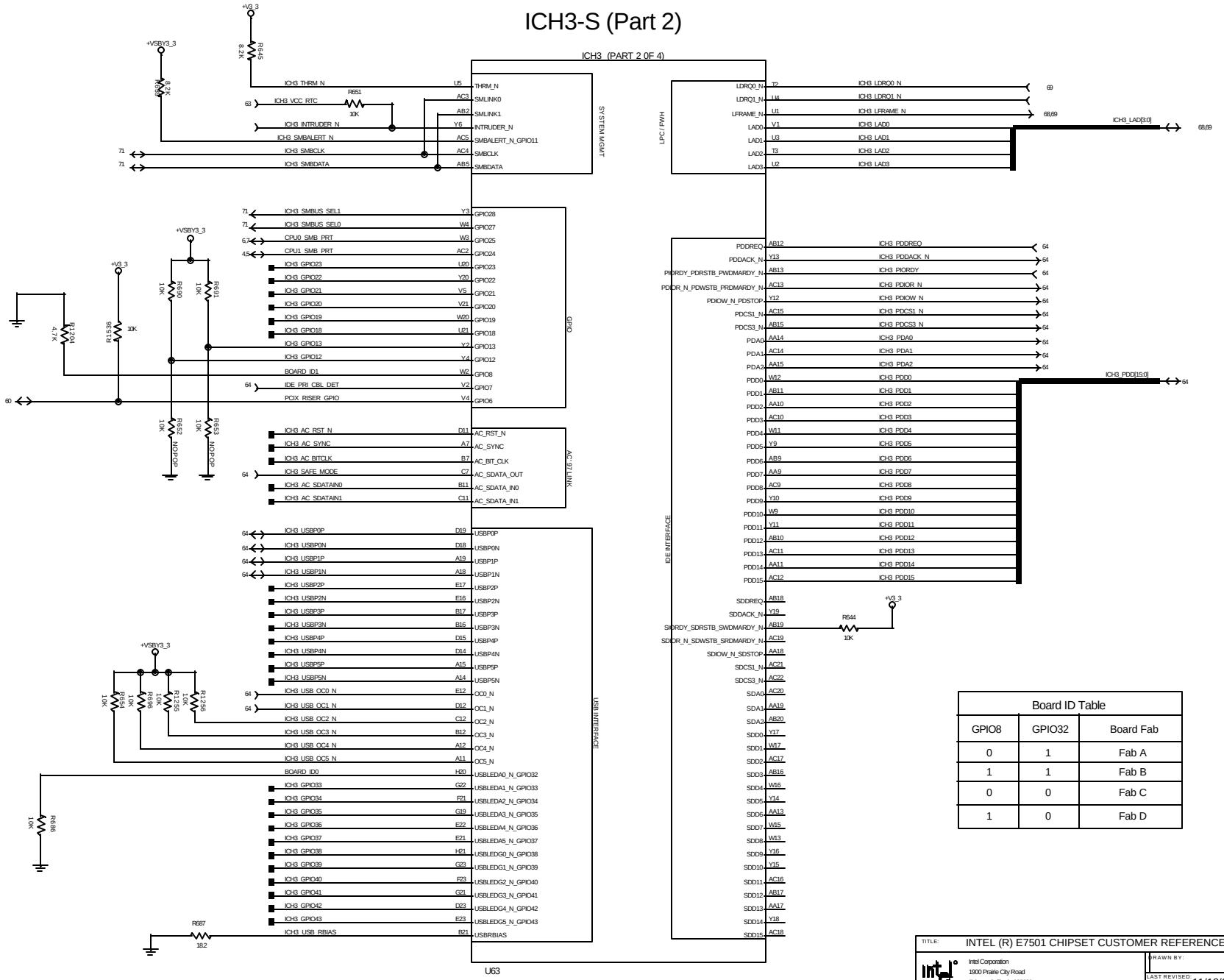
ICH3-S (Part 2)



Board ID Table		
GPIO8	GPIO32	Board Fab
0	1	Fab A
1	1	Fab B
0	0	Fab C
1	0	Fab D

TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD			REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533	
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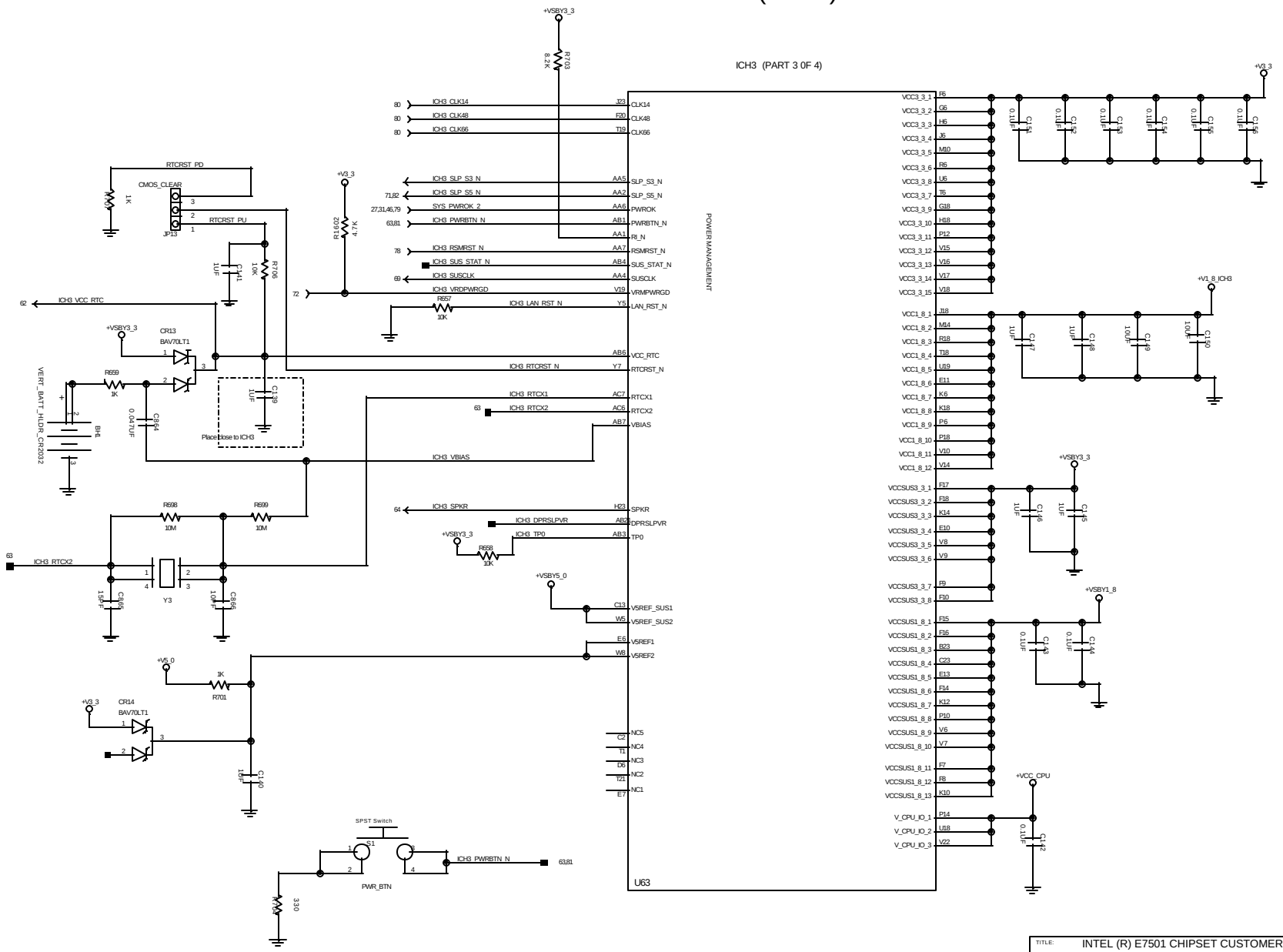
ICH3-S (Part 3)



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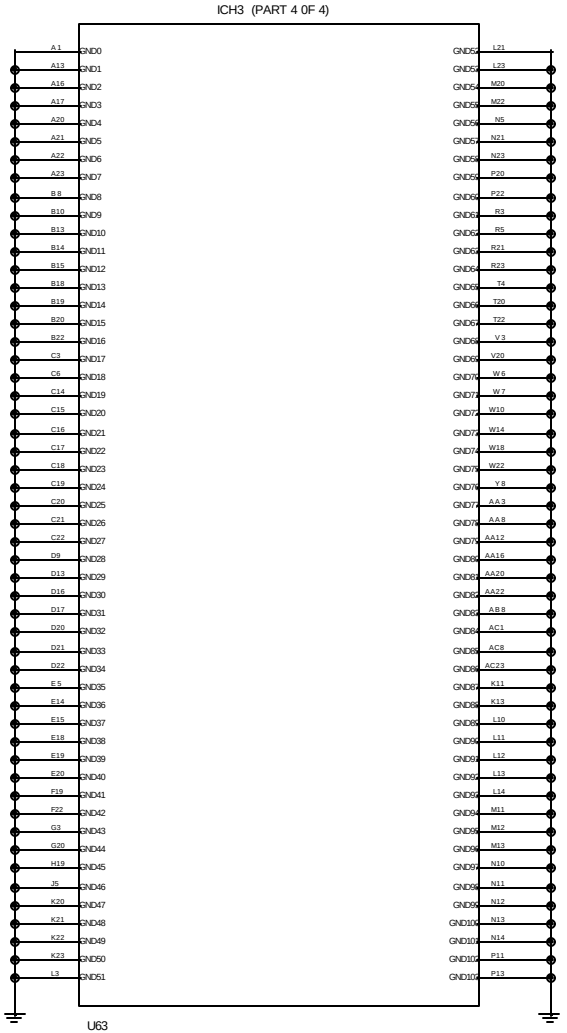
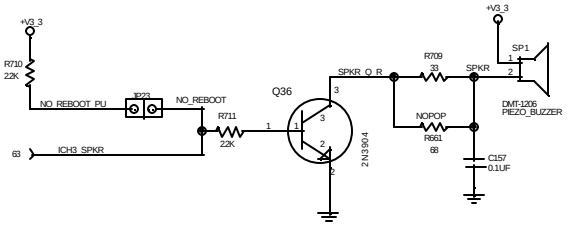
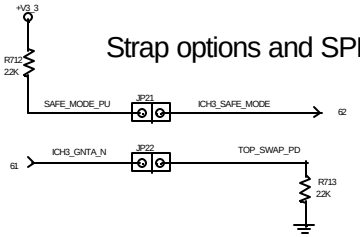
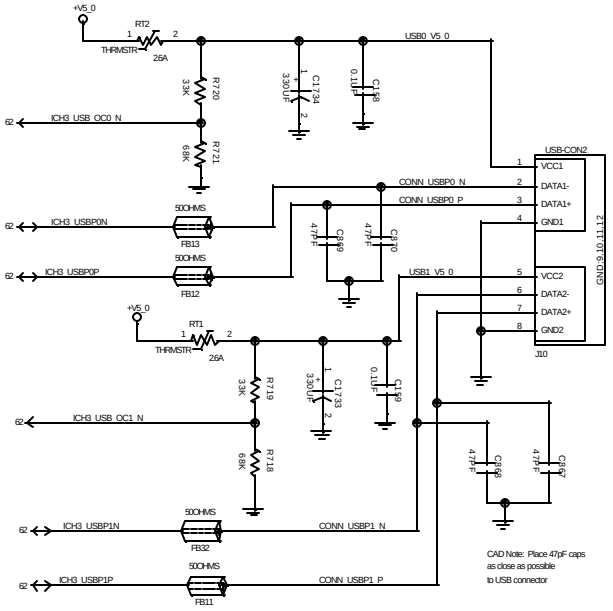
ICH3-S (Part 4)



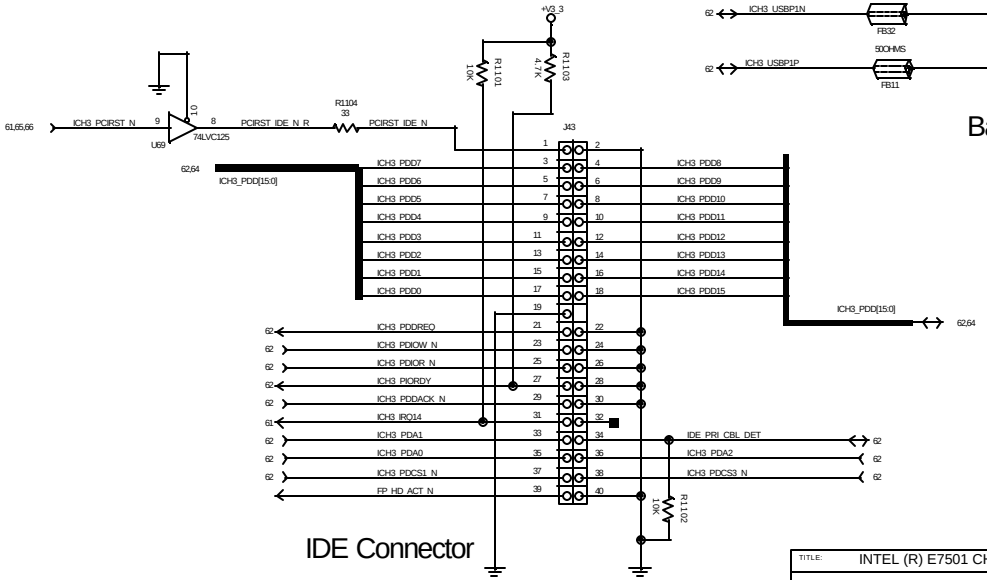


Strap options and SPKR circuit





Backplane USB Connectors



IDE Connector

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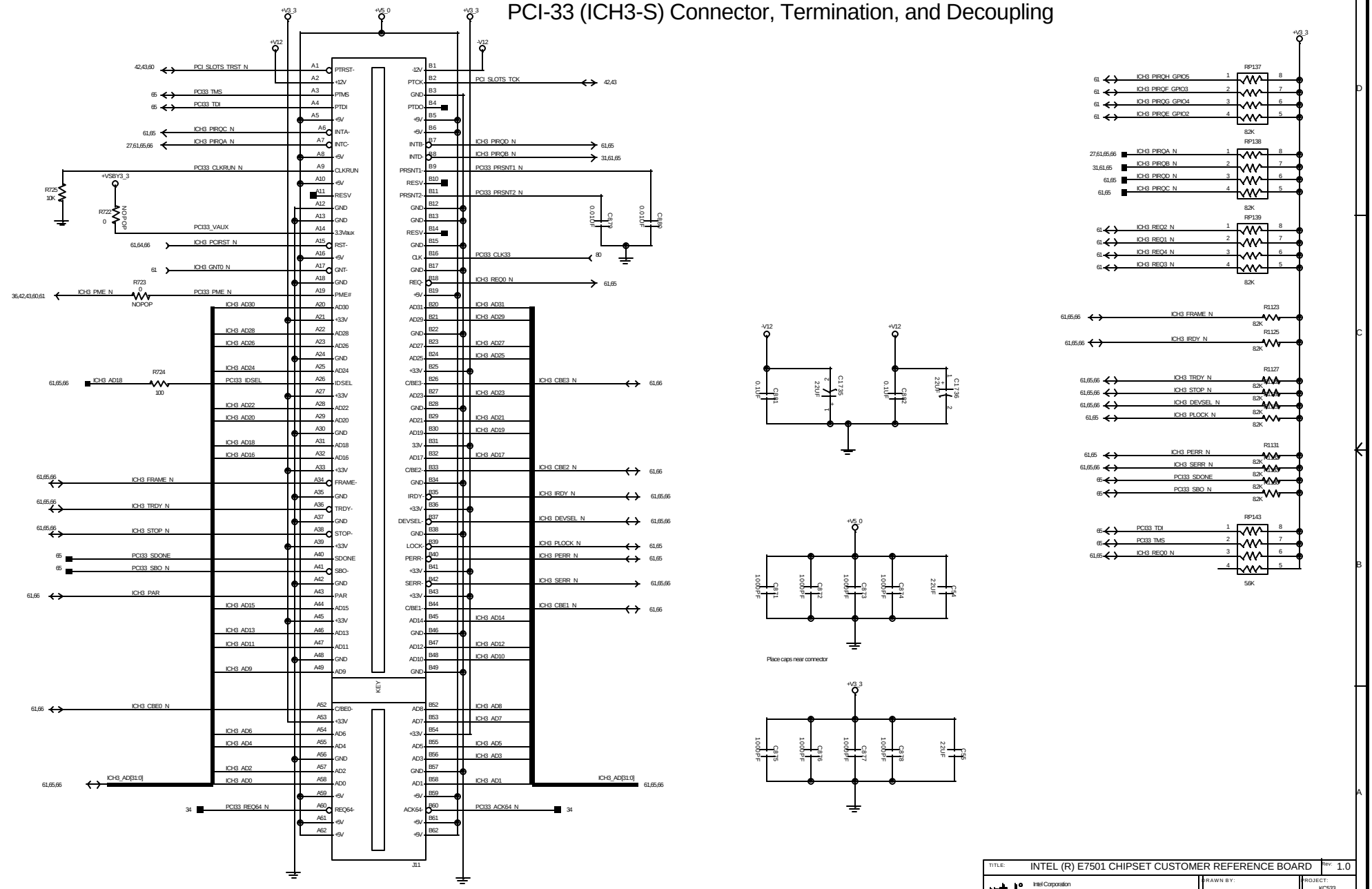
PCI-33 (ICH3-S) Connector, Termination, and Decoupling



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Intel Corporation	1900 Prairie City Road, Folsom, California 095630
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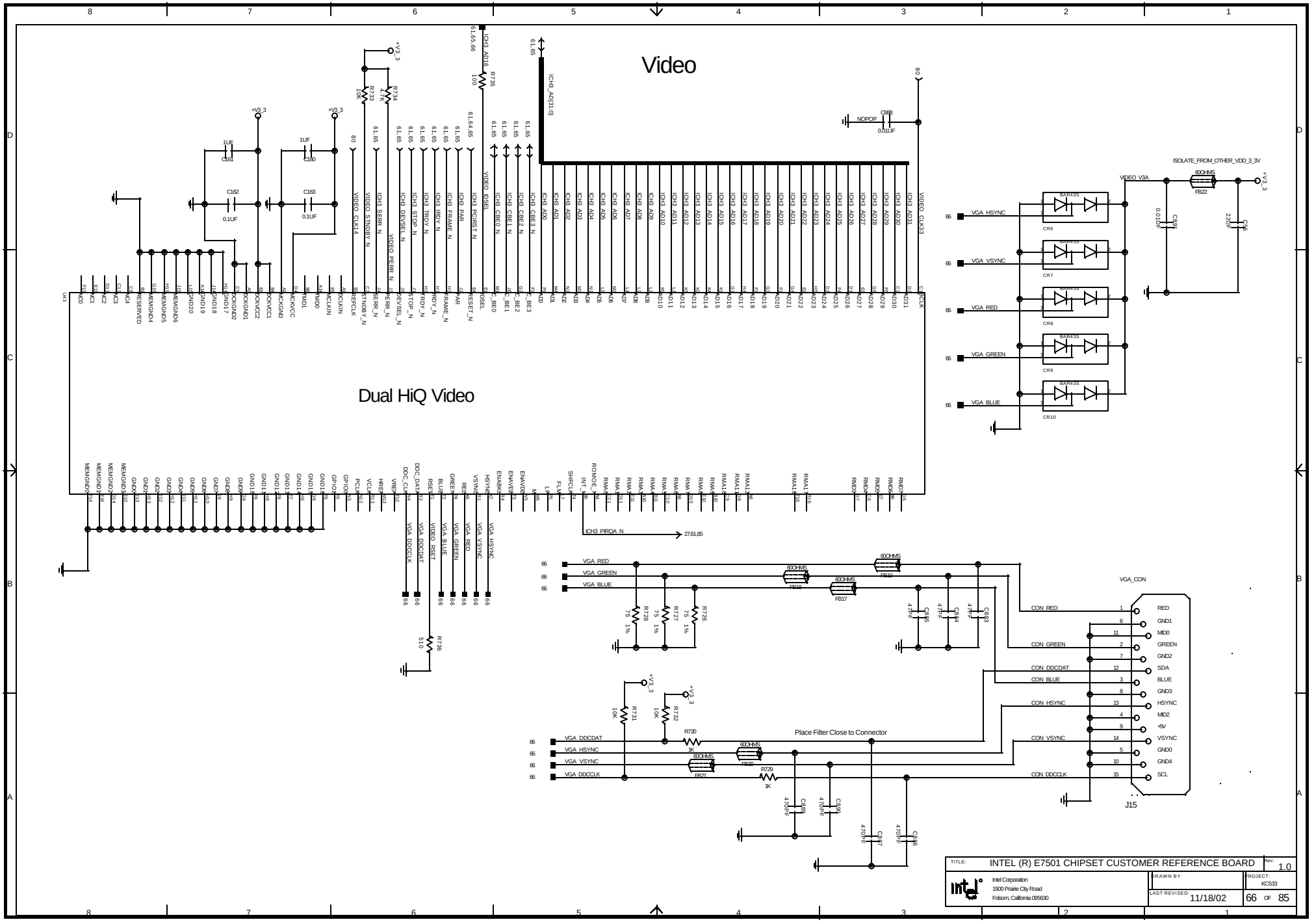
Video
Dual HiQ Video
ISOLATE_FROM_OTHER_VDD_3_3V
VIDEO_V3A
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_DDCDAT
VGA_DDCCLK
VGA_CON
Place Filter Close to Connector
CON_RED
CON_GREEN
CON_BLUE
CON_HSYNC
CON_VSYNC
CON_DDCDAT
CON_DDCCLK
J15
TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
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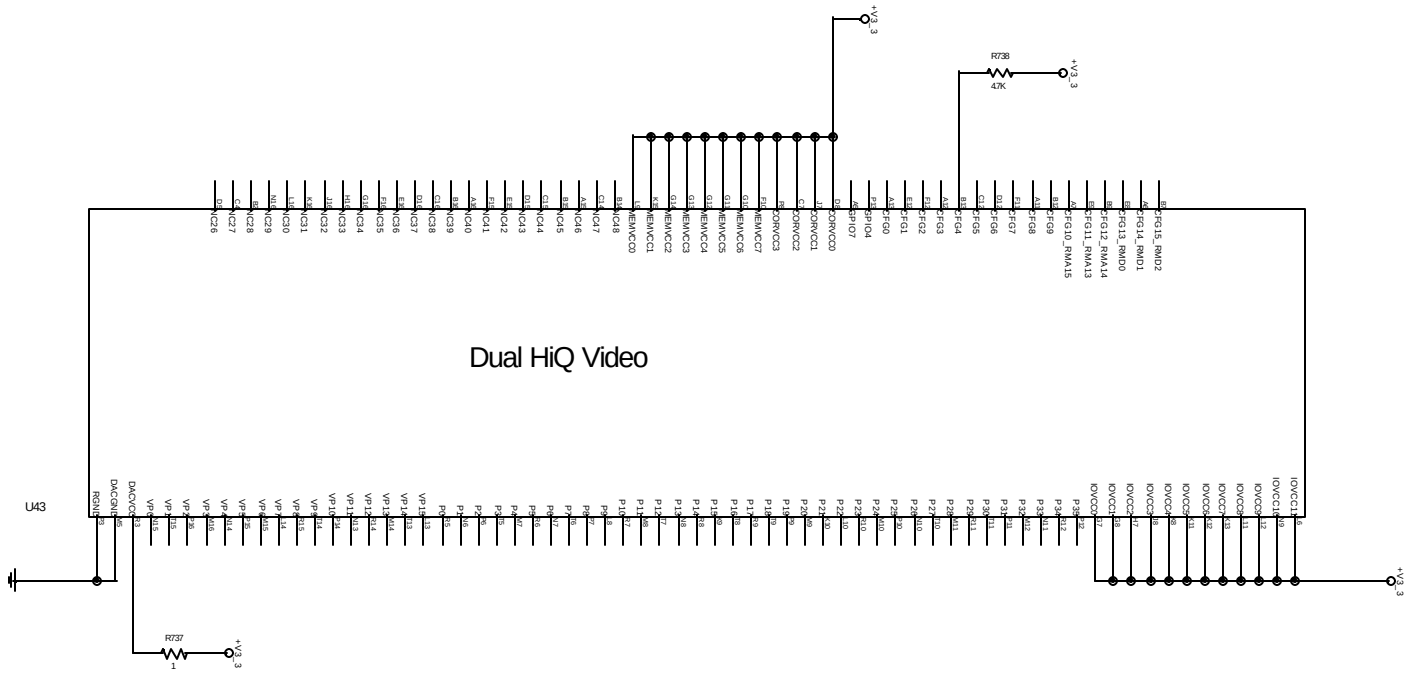
Video



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT:	KC533
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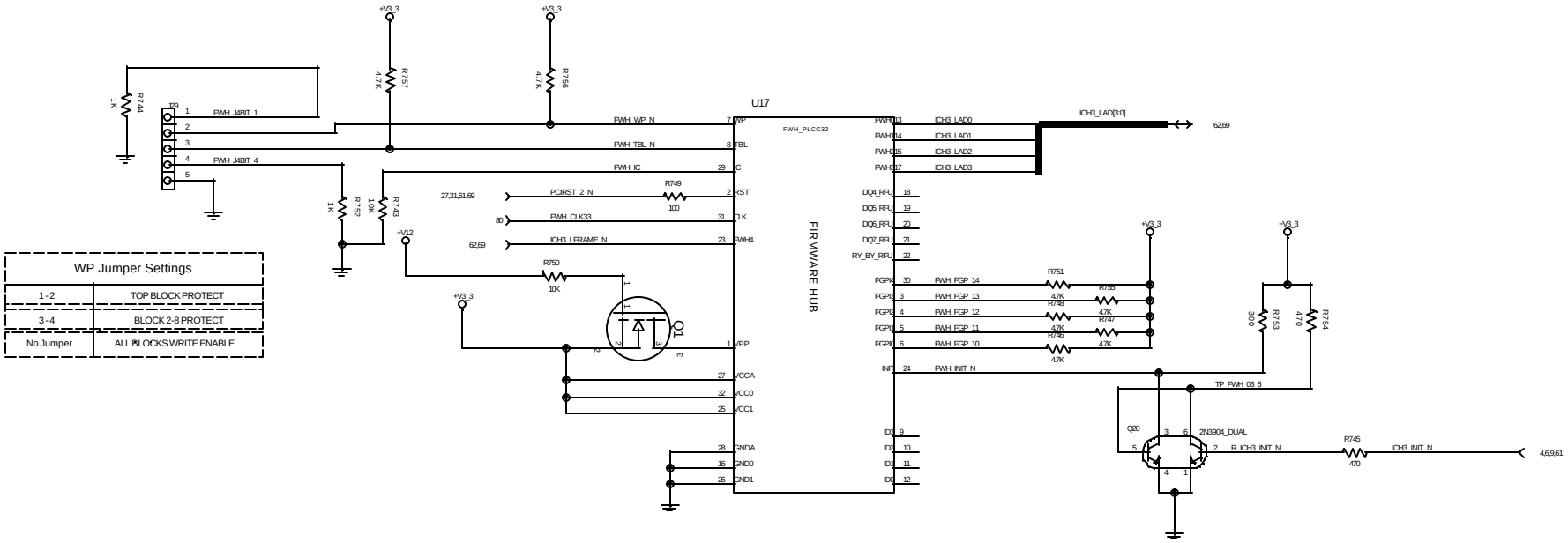
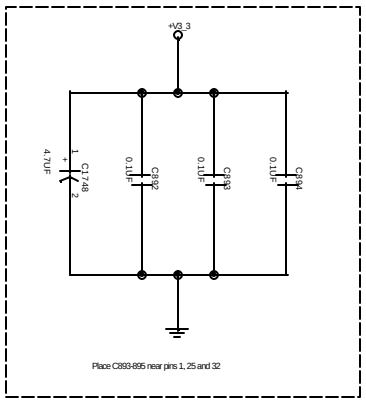
FWH



WP Jumper Settings	
1 - 2	TOP BLOCK PROTECT
3 - 4	BLOCK 2-8 PROTECT
No Jumper	ALL BLOCKS WRITE ENABLE



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV.	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT:	KC533
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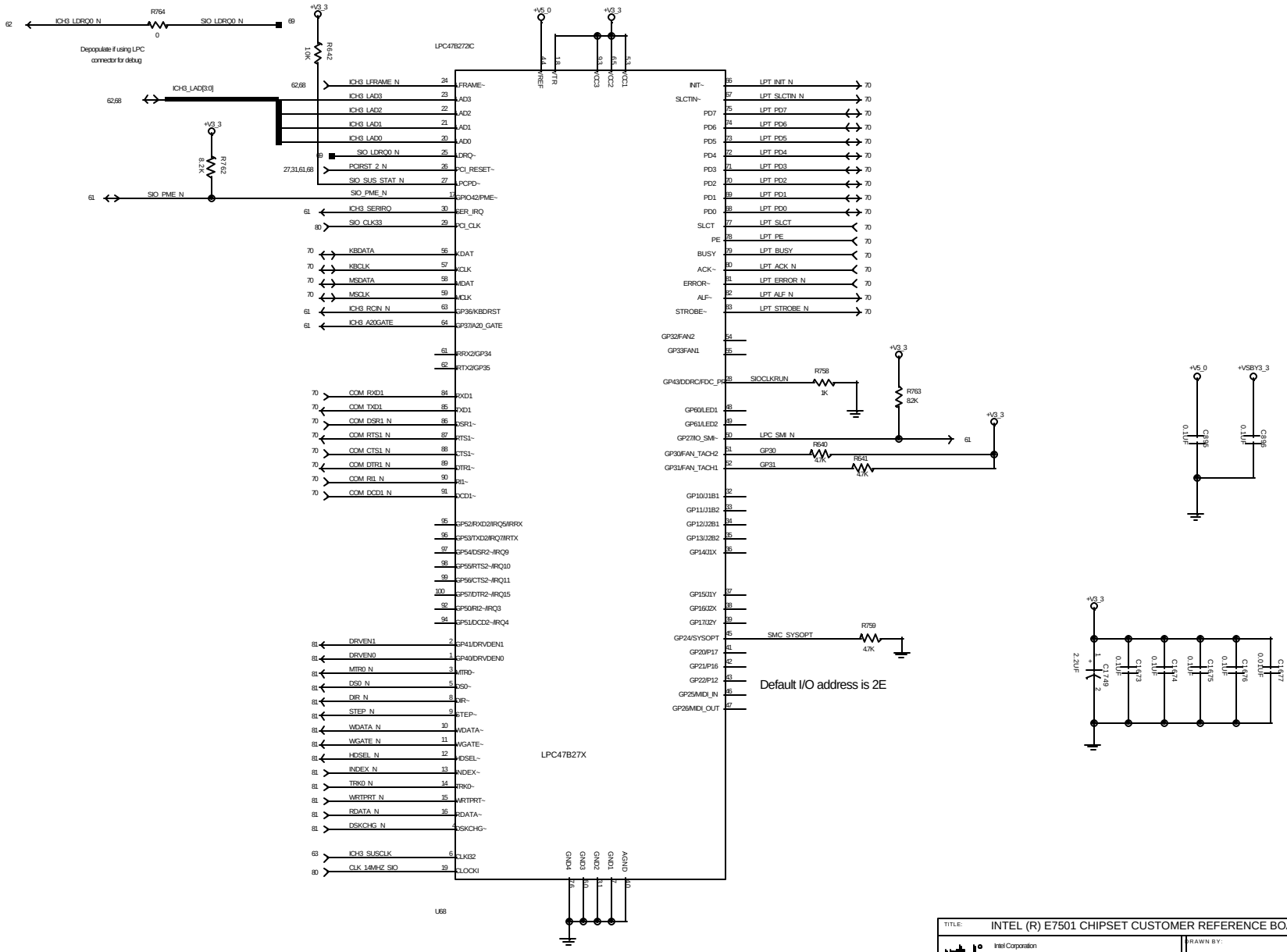
Super I/O



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Intel Corporation 1900 Prairie City Road Folsom, California 095630	
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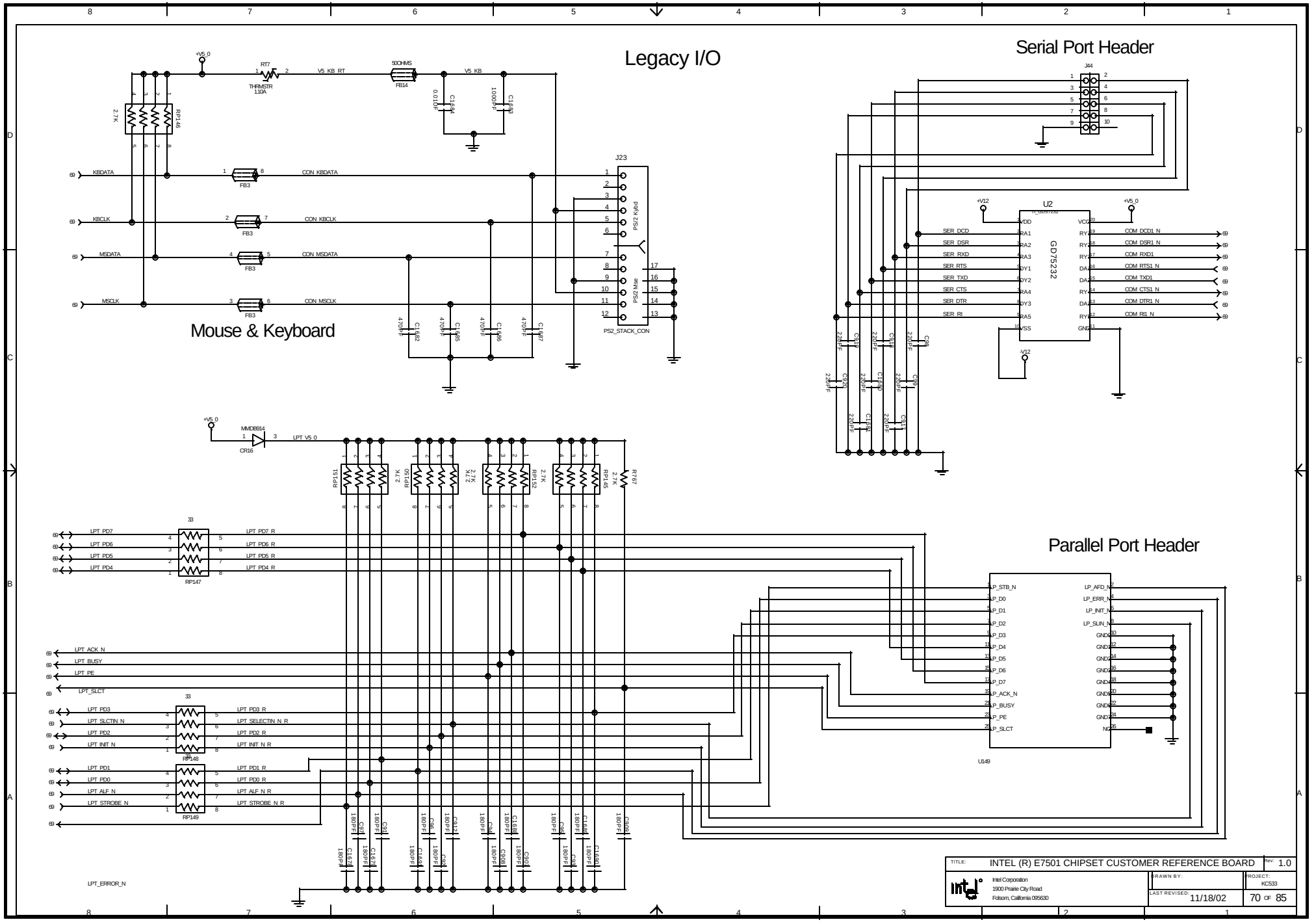

TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630		DRAWN BY:	PROJECT: KC533
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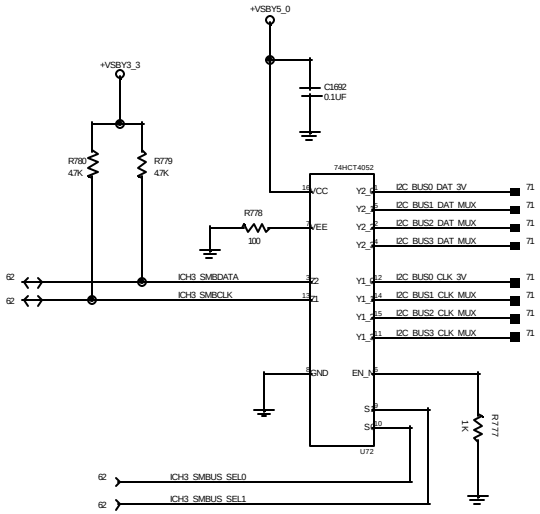
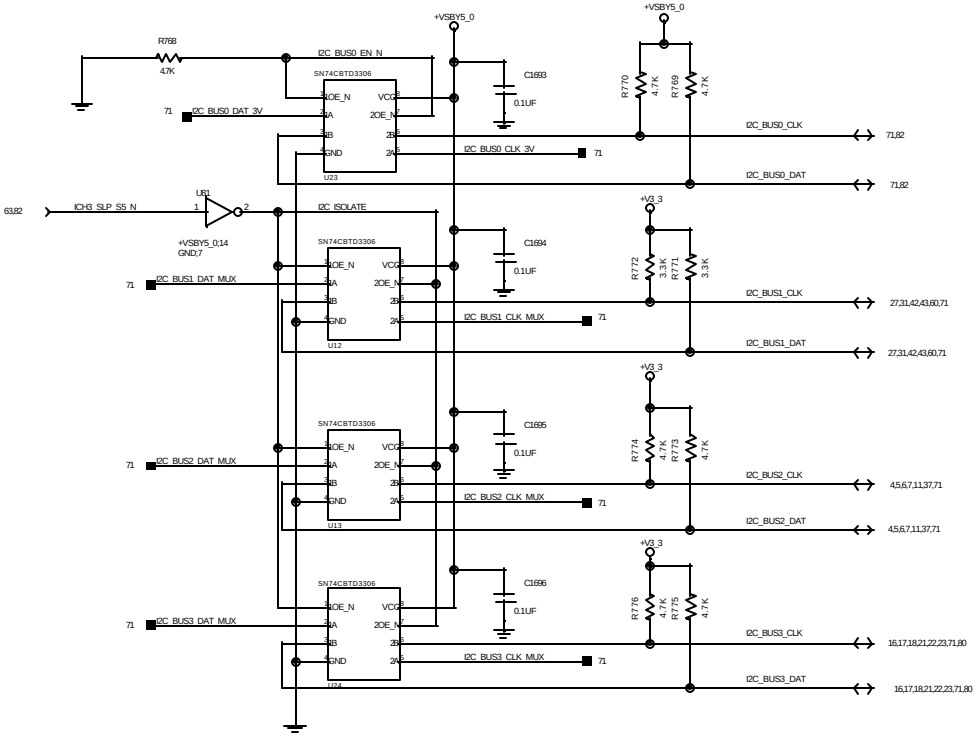
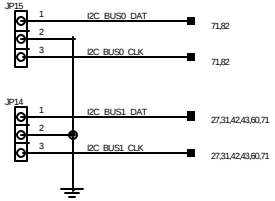
SMBus Mux

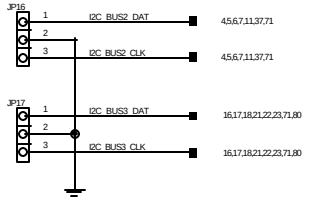


SEL1	SEL0	SMBus Partition
0	0	Bus 0
0	1	Bus 1
1	0	Bus 2
1	1	Bus 3 (default)

SMBus Isolation and Voltage Translation







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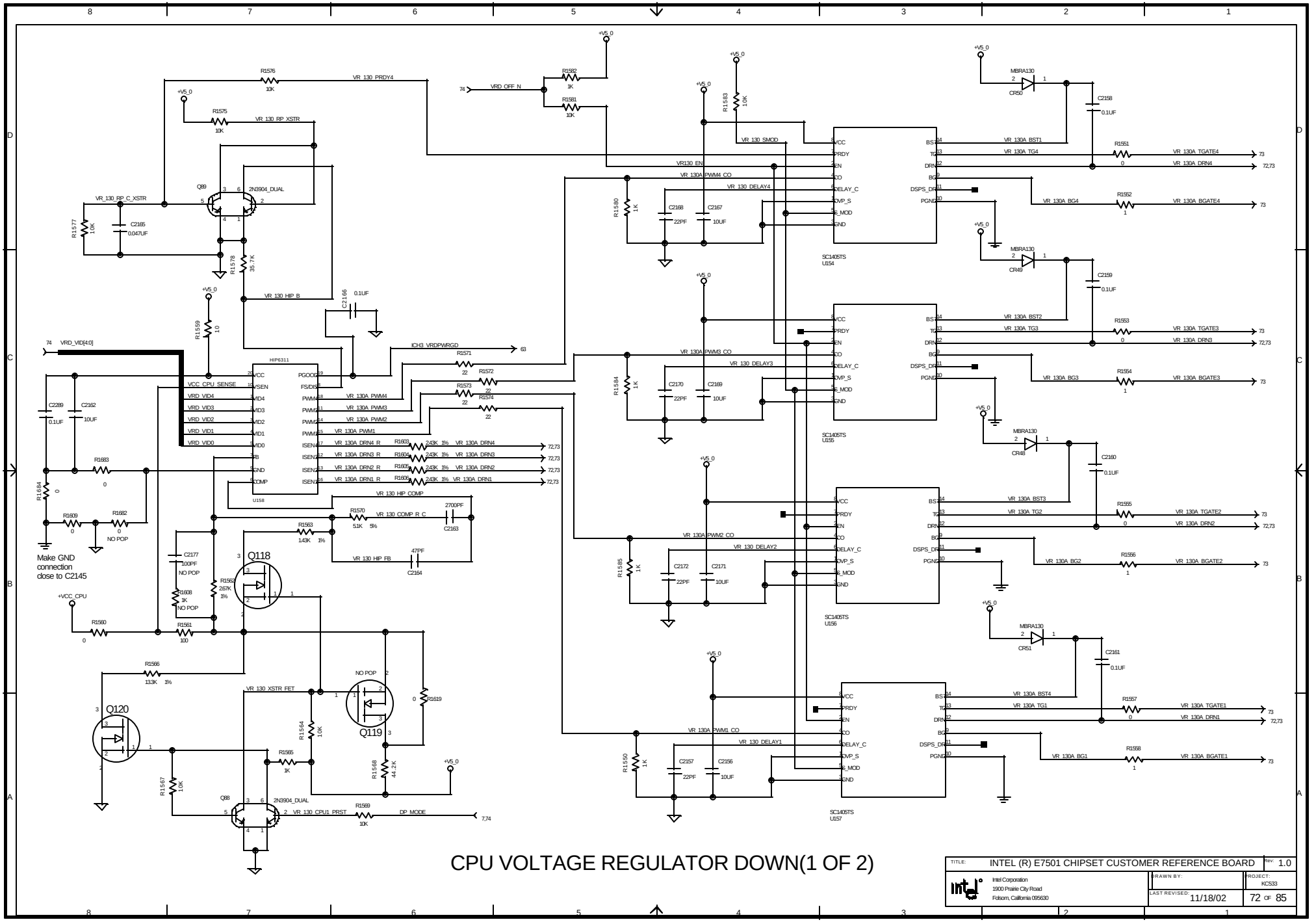

CPU VOLTAGE REGULATOR DOWN(1 OF 2)

TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.0
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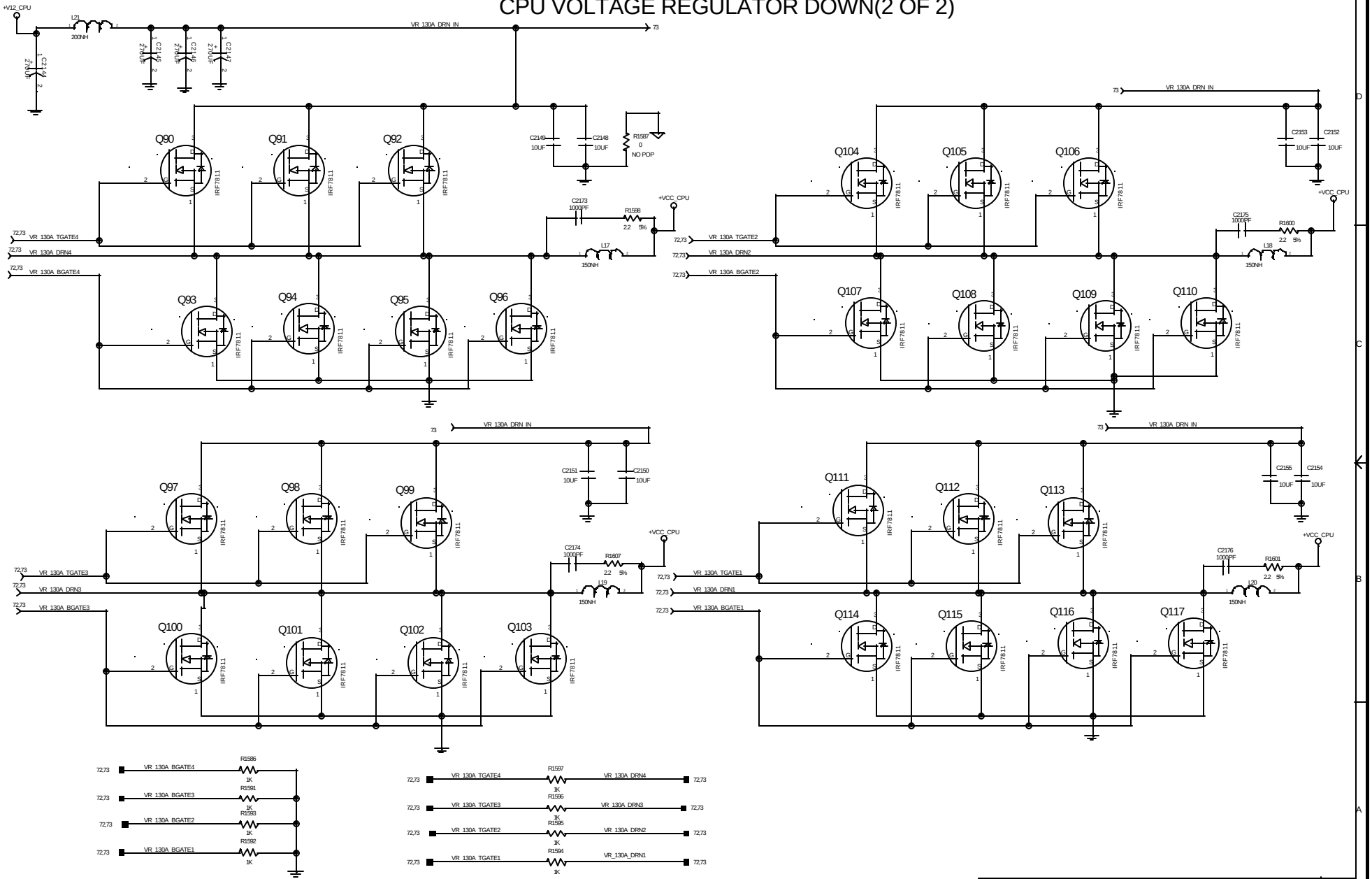
CPU VOLTAGE REGULATOR DOWN(2 OF 2)



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
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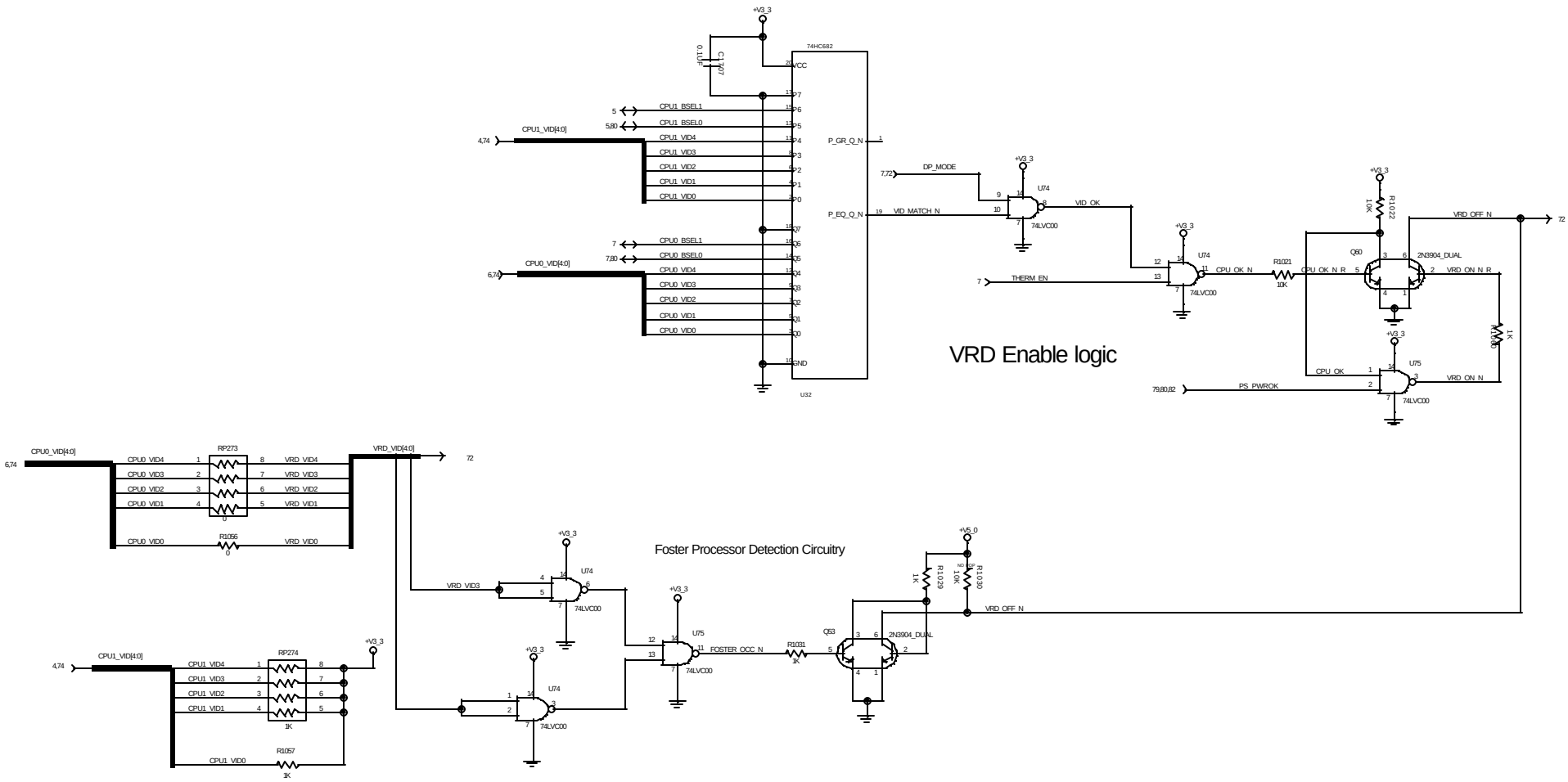
CPU Load Line Circuitry & VID Manual Override(Debug Only)



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
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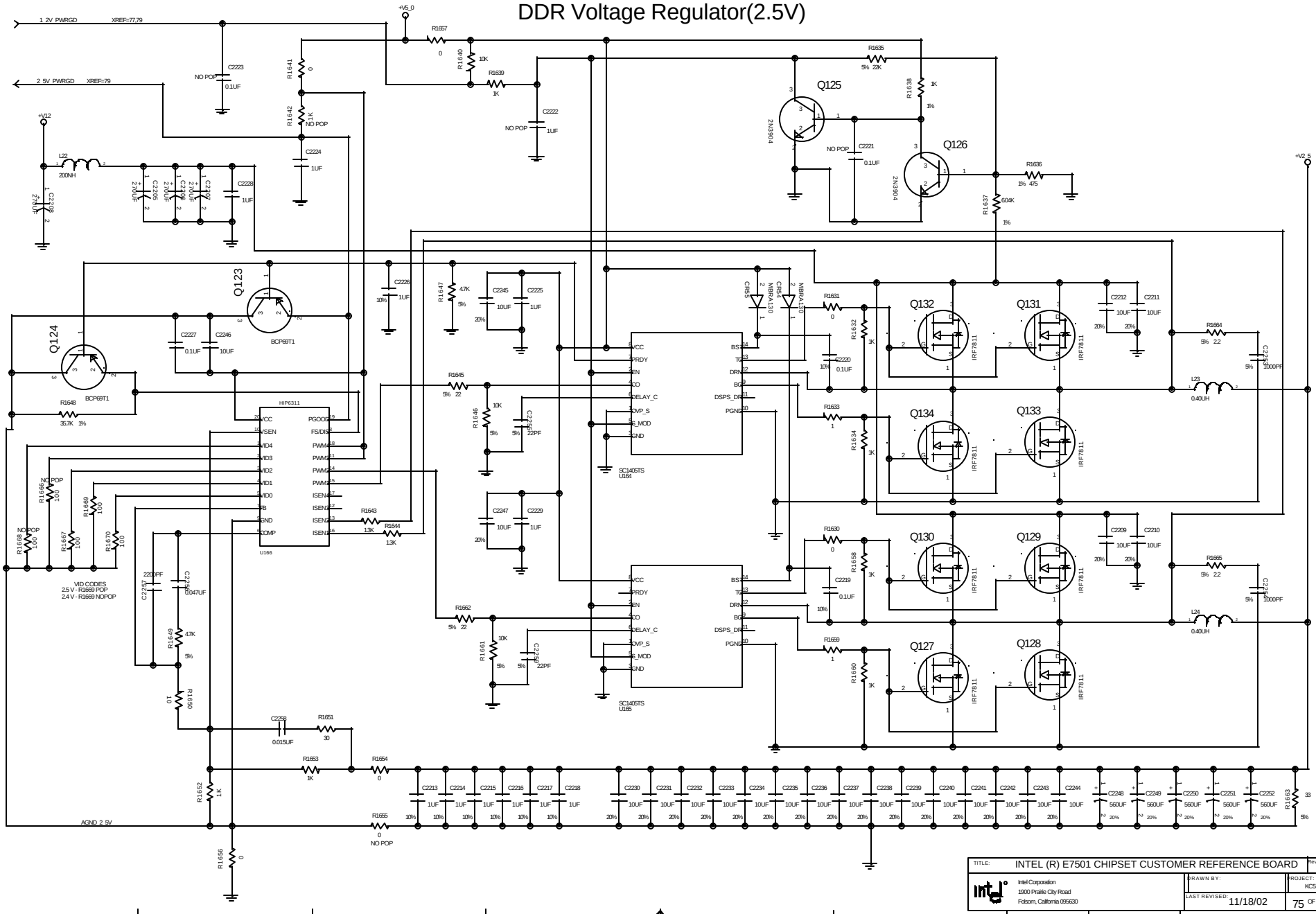
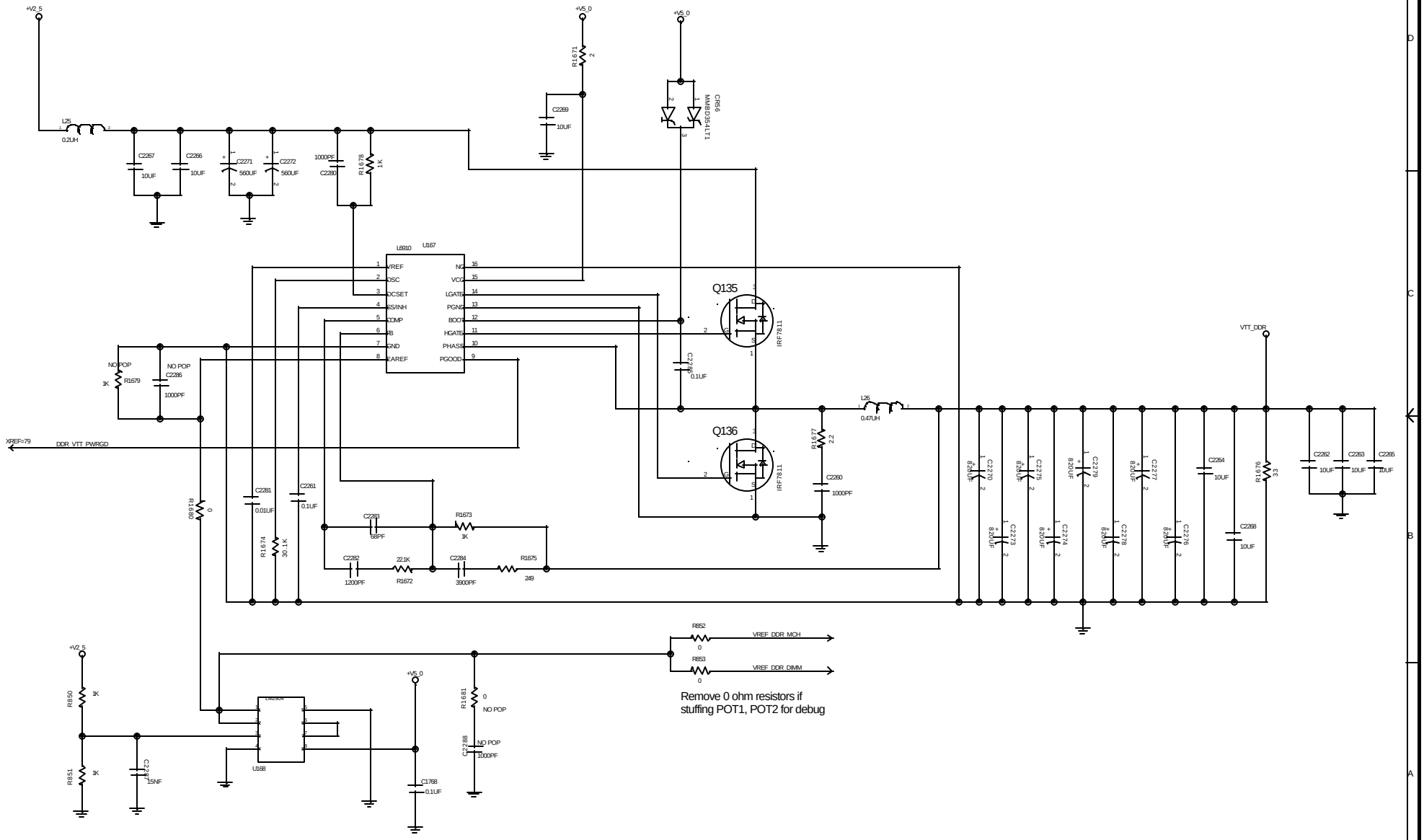
DDR Voltage Regulator(2.5V)



DDR VTT Regulation



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Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
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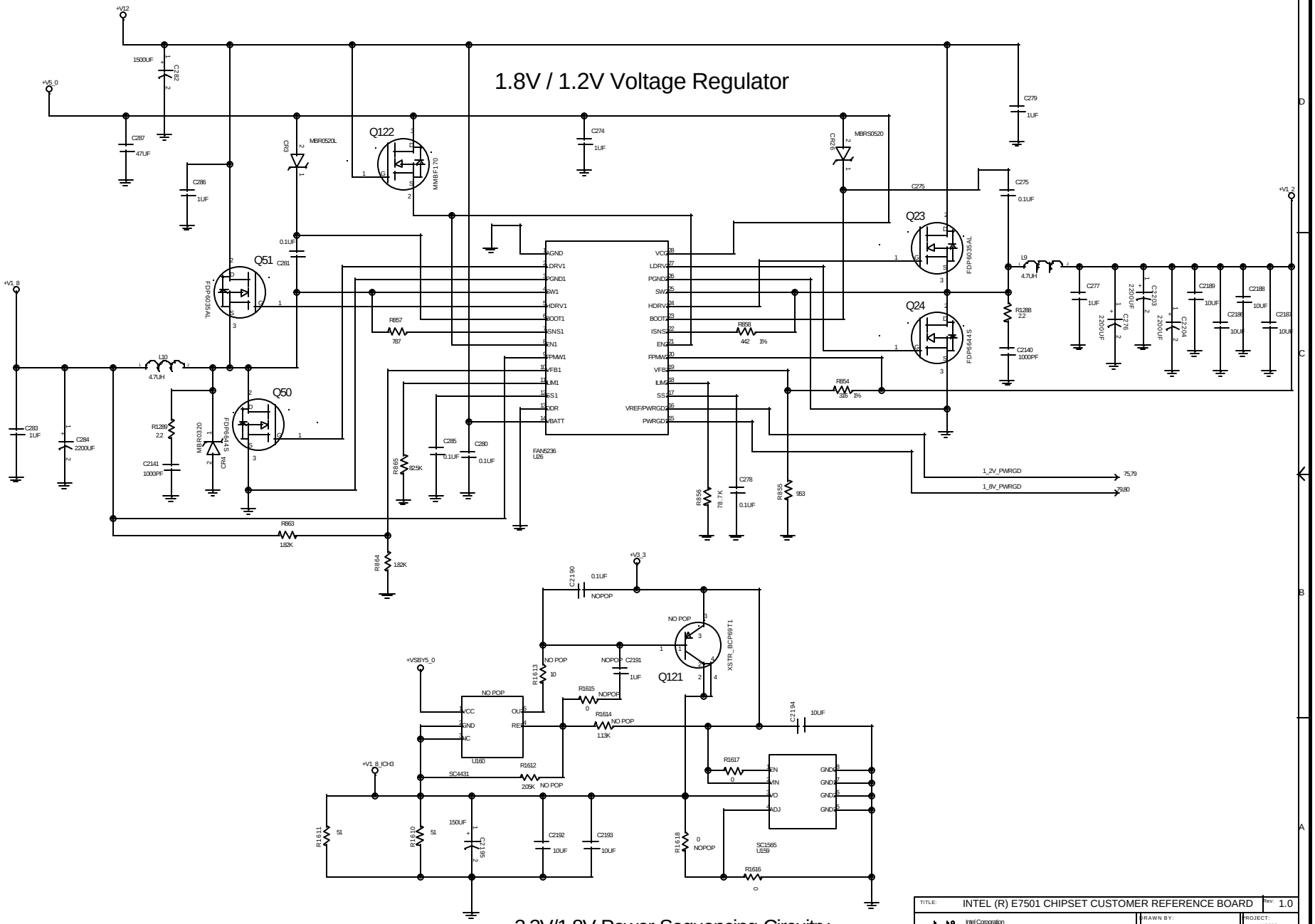
1.8V / 1.2V Voltage Regulator
+V12
+V5_0
+V1_8
+V1_2
+V3_3
+VSBY5_0
+V1_8_ICH3
Q122
MMBF170
Q51
FDP6035AL
Q50
FDP6644S
Q23
FDP6035AL
Q24
FDP6644S
Q121
XSTR_BCP69T1
U26
FAN5236
U160
SC4431
U159
SC1565
1_2V_PWRGD
1_8V_PWRGD
3.3V/1.8V Power Sequencing Circuitry
INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD
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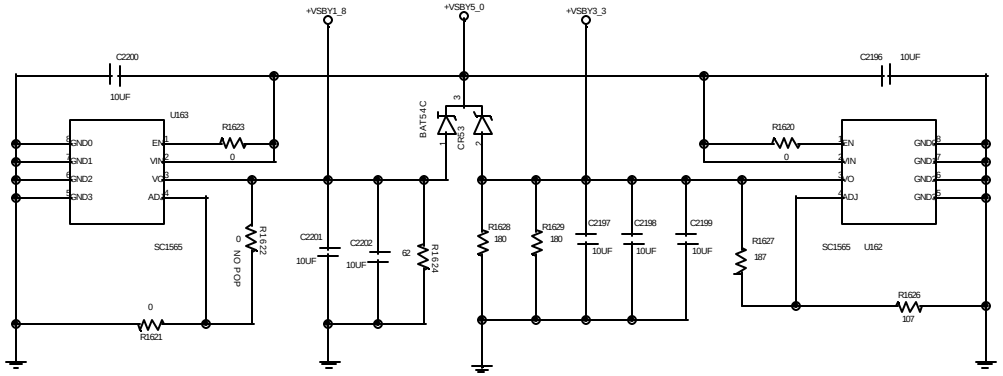
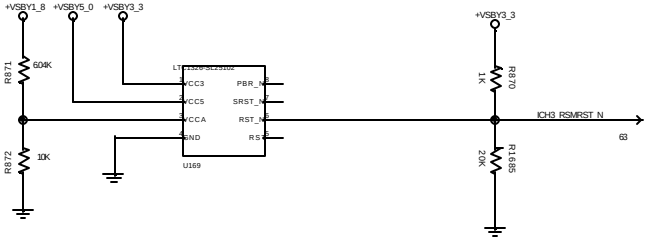
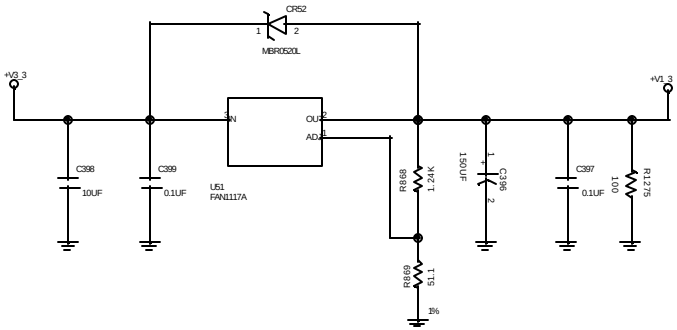
Standby Voltage Regulators



Standby supply monitor



1.3V Voltage Regulator (I/O Processor Core)



TITLE:	INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD	REV:	1.0
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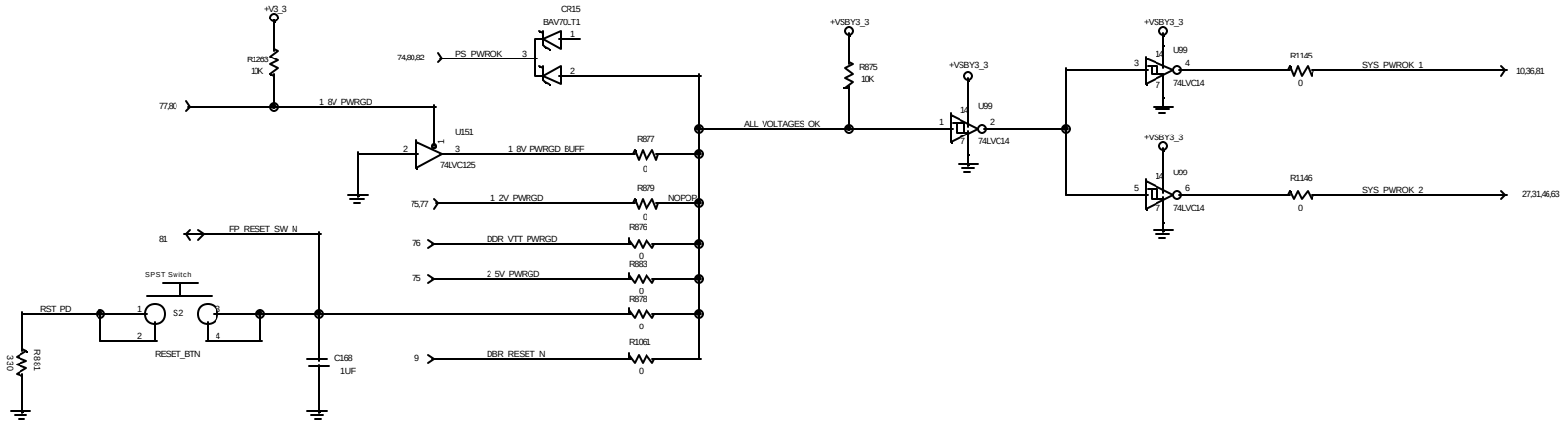
PWROK Circuitry



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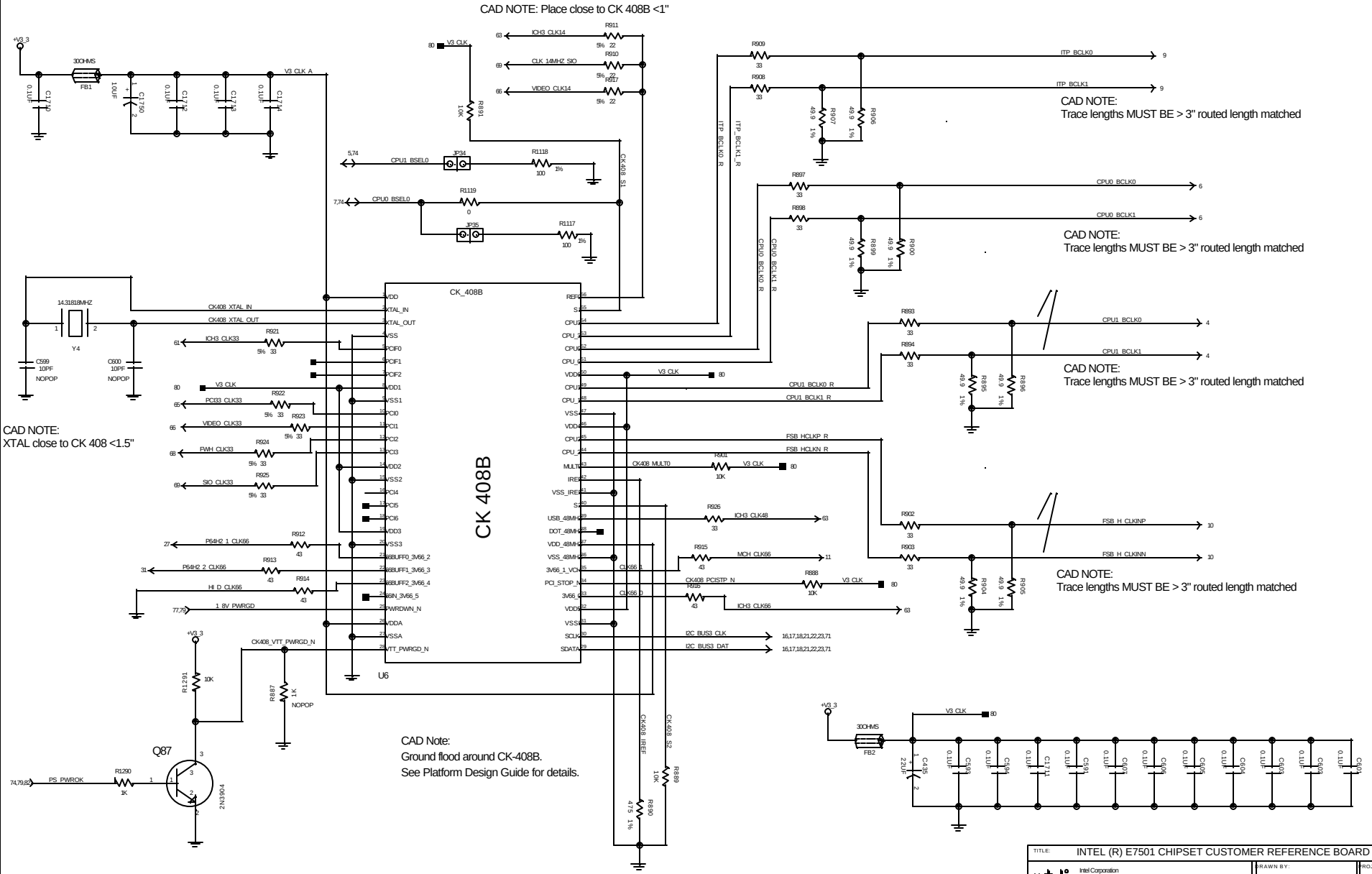
CK-408B Clock Synthesizer



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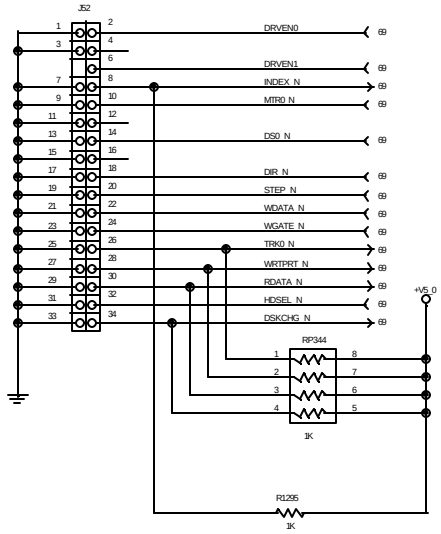
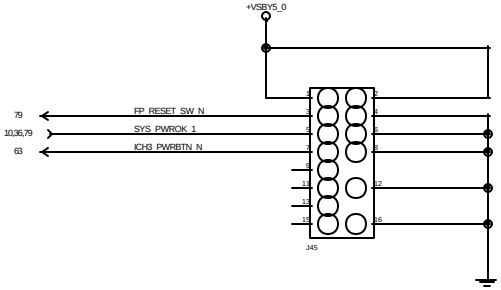
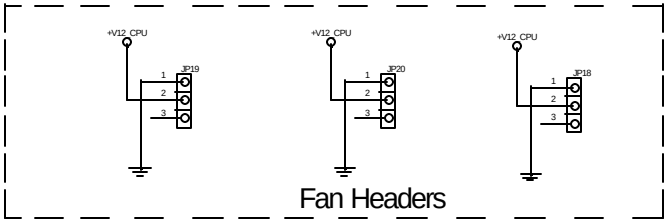
Front Panel Connector / Floppy Connector

Floppy Connector



Front Panel Connector





TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
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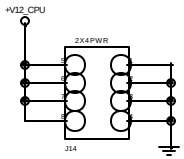
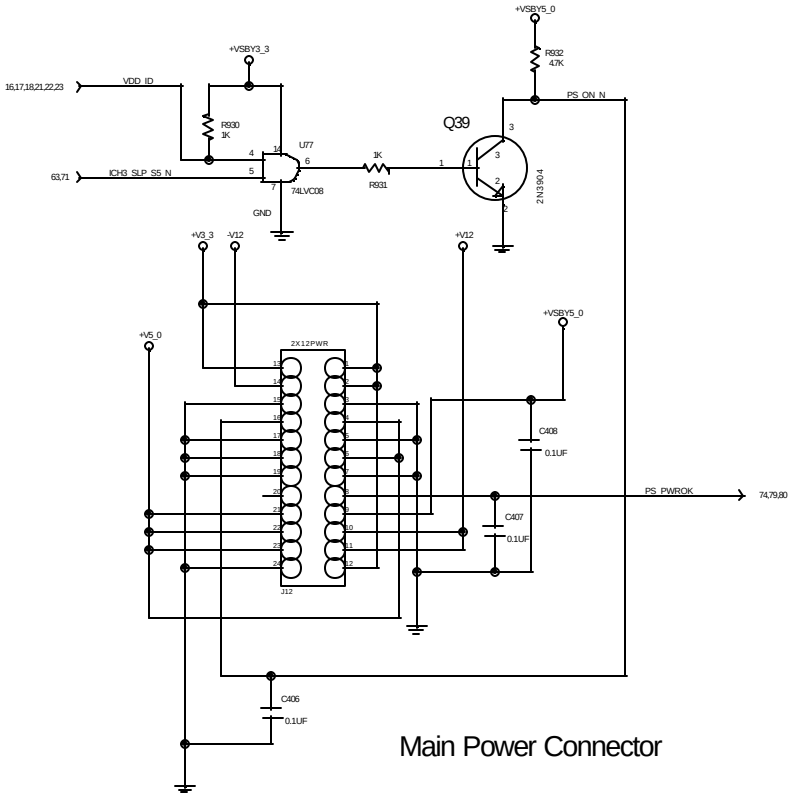
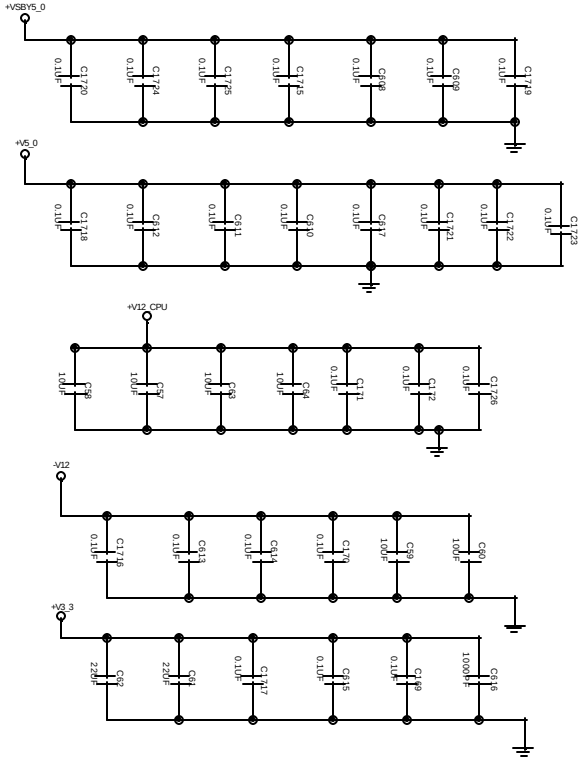
Power Connectors



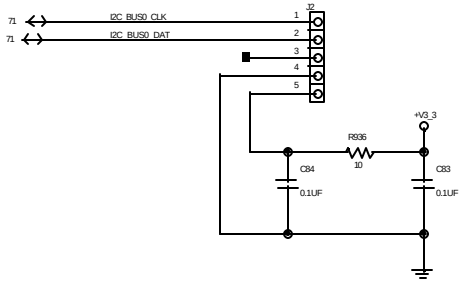
CPU +12V Power Connector



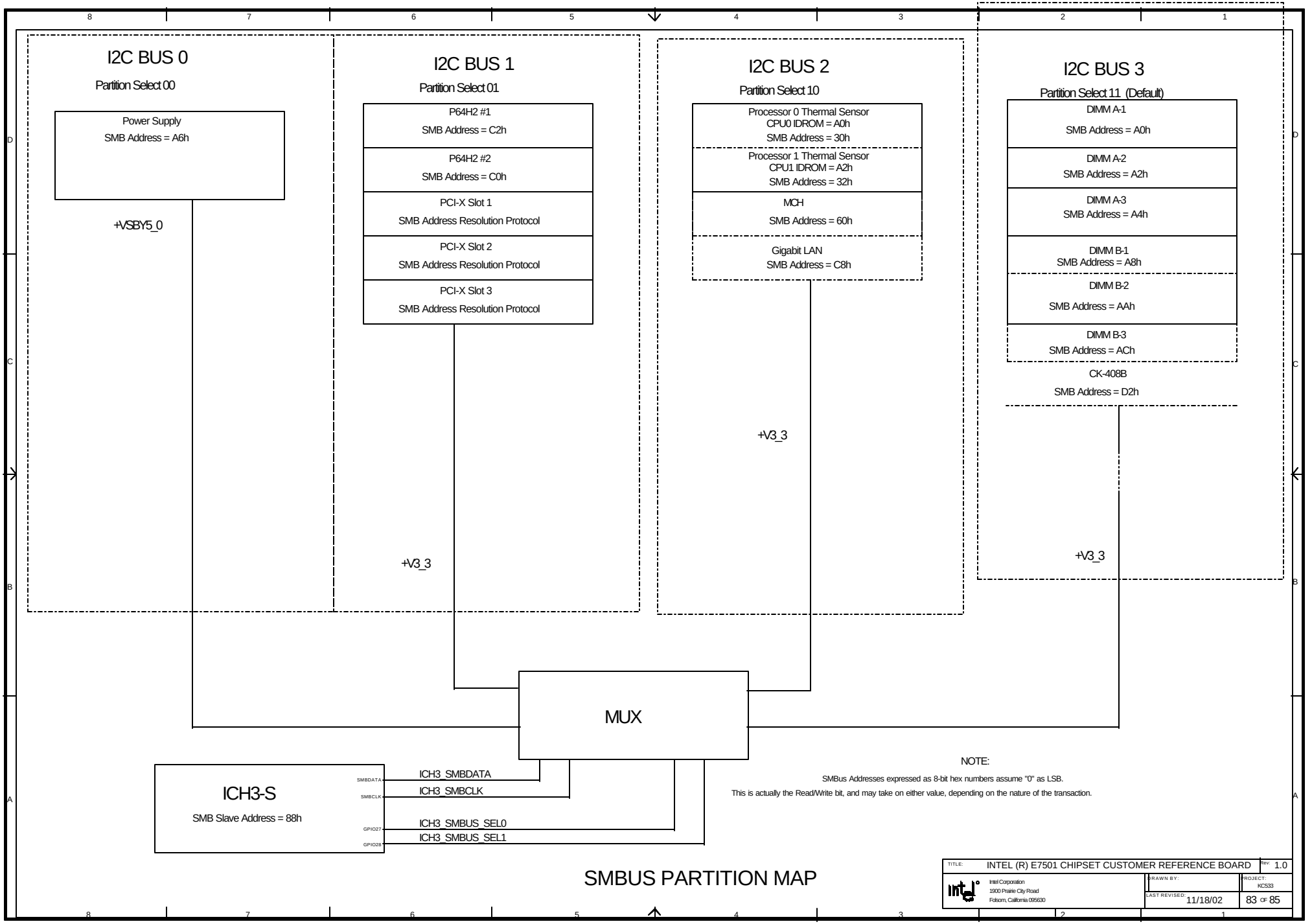
Main Power Connector



Power Supply SMBus Interface



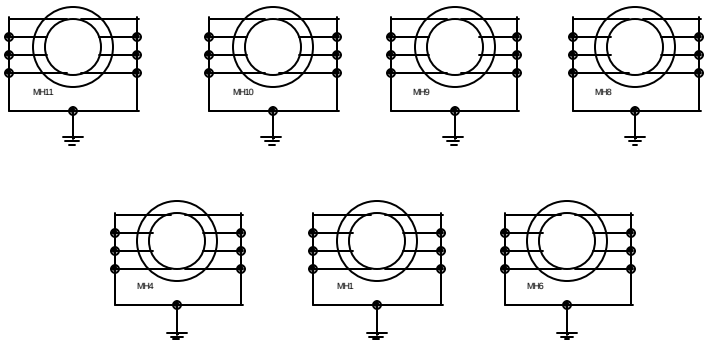
TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
	LAST REVISED: 11/18/02	82 OF 85



SMBUS PARTITION MAP

TITLE: INTEL (R) E7501 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
Intel Corporation 1900 Prairie City Road Folsom, California 095630	DRAWN BY:	PROJECT: KC533
	LAST REVISED: 11/18/02	83 OF 85

Mounting Holes



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		LAST REVISED: 11/18/02	84 OF 85

PCI.X INTERRUPT MAPPING

Component	IDSEL	REQ/GNT	IRQ
82546EB	P64H2_1_PA_AD17	P64H2_1_PA_REQ/GNT0	P64H2_1_PA_IRQ[0:3]
PCI.X Slot 2	P64H2_1_PB_AD17	P64H2_1_PB_REQ/GNT0	P64H2_1_PB_IRQ[0:3]
PCI.X Slot 3	P64H2_1_PB_AD18	P64H2_1_PB_REQ/GNT1	P64H2_1_PB_IRQ[4:7]
I/O Processor	P64H2_2_PA_AD17	P64H2_2_PA_REQ/GNT0	P64H2_2_PA_IRQ[0:3]
SCSI	P64H2_2_PA_AD18	P64H2_2_PA_REQ/GNT1	P64H2_2_PA_IRQ[0:1]
PCI.X Slot 1 (3 Slot Riser)	P64H2_2_PB_AD17	P64H2_2_PB_REQ/GNT[0:2]	P64H2_2_PB_IRQ[0:5]