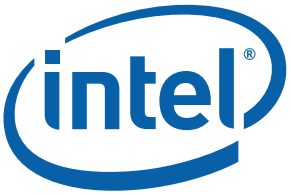


Intel® IP Network Server NSW1U

Technical Product Specification

January 2009

Rev 1.6

Order Number: D55559-007

Contents

Figures

Tables

Revision History

Date	Version	Description
January 2009	007	Corrected DC Power Supply Module information in Table 21
April 2008	006	Edited processor information to include Quad-Core Intel® Xeon® processors 5400 series. Removed SysCon information. Added Intel Z-U130 Solid State Drive. Minor grammar and formatting changes.
June 2007	005	Updated block diagrams in “System Overview” to include NIC port numbers. Updated multiple panel illustrations in “System Overview” to correct colors of NIC LEDs. Updated front panel layout figures in “System Overview” to indicate NIC port numbering. Added information to “System Overview” and “Ethernet Front Panel (EFP) Board” about second MAC address on Ethernet port 1 for IPMI access to baseboard management controller. Updated multiple figures in “System Overview” to illustrate isolated fan mounting brackets. Updated rear panel illustrations in “System Overview” and illustration in “AC Power Subsystem” to show correct power supply module numbering. Updated optical drive illustrations in “System Overview” to reflect new interposer board. Updated acoustic specification and added cooling requirements to environmental specifications in “System Overview”. Updated interconnection block diagram in “Cables and Connectors” to include SysCon cable connection and correct descriptions of LEDs on control panel. Added info about permanently connected EFP power harness for Bypass configuration to interconnection diagram and EFP power cable section of “Cables and Connectors”. Updated information on IDE signal cable, optical drive power cable, and SysCon cable in “Cables and Connectors”. Added section for GCM interface connector to “Cables and Connectors”. Updated block diagrams in “Ethernet Front Panel (EFP) Board” to include NIC port numbers. Corrected SysCon connector location in illustration in “Ethernet Front Panel (EFP) Board”. Added note in “SysCon Board” regarding non-support of SDHC cards. Updated figures in “SysCon Board” to match production version of board. Added notes about permanently connected EFP power harness for Bypass configuration to “AC Power Subsystem”. Corrected input voltages in input connector pin-out in “DC Power Subsystem”.
March 2007	004	Replaced single block diagram with separate diagram for each of three variants. Added information on software RAID support (levels 0 & 1). Updated power supply unit numbering in rear panel illustrations in “System Overview” and illustration in “AC Power Subsystem”. Updated front-panel Flex cable information to include server board signal names as well as EFP board signal names. Updated illustrations of PCIe and PCI-X riser cards.
December 2006	003	Updated descriptions of system status LED, ID LED, and PCI/PCI Express adapter subsystem and updated non-operating temperature and altitude specifications in “System Overview”. Corrected pin-outs for USB and Ethernet connectors and added details on configuring serial ports in “Cables and Connectors”. Corrected description of system status LED in “Ethernet Front Panel (EFP) Board”, and moved all cable/connector pin-out information to “Cables and Connectors” chapter. Updated bus speeds and replaced PCI Super Slot pin-out with PCI/PCI-X card slot pin-out in “PCI/PCI-X Riser Card”. Replaced PCI Super Slot pin-out with PCIe card slot pin-out in “PCI Express Riser Card”.
November 2006	002	Initial document release specific to IP Network Server NSW1U. Updated for SRA/Gold release.
September 2006	001	Initial document release for product TRA release. (Was combined document for IP Network Server NSW1U and Carrier Grade Server TIGW1U.)

1.0 Introduction

This document provides an overview of the Intel® IP Network Server NSW1U, including information about the chassis hardware, cables, connectors, system boards, power subsystem, and regulatory requirements.

Note: The NSW1U server is available in three different I/O configurations. Most server features are common to all three configurations so that there is no need to distinguish among the three variations. The following terminology will be used when it is necessary to describe any of the configurations individually:

- NSW1U-F or NSW1U-FNIC = server configuration with front panel Ethernet connections
- NSW1U-R or NSW1U-RNIC = server configuration with rear Ethernet connections
- NSW1U-B or NSW1U-Bypass = server configuration with both front and rear Ethernet access and bypass capability for front-panel connections

1.1 Document Structure and Outline

This document is organized into the following chapters:

Chapter 1.0, "Introduction" — Provides an overview of this document.

Chapter 2.0, "System Overview" — Provides an overview of the Intel® IP Network Server NSW1U chassis hardware.

Chapter 3.0, "Cables and Connectors" — Describes the cables and connectors used to interconnect the system board set and the server system components.

Chapter 4.0, "Ethernet Front Panel (EFP) Board" — Describes the specifications of the front panel I/O board.

Chapter 5.0, "Intel® Z-U130 Value Solid State Drive" — Describes the specifications of the optional Intel® Z-U130 Value Solid State Drive.

Chapter 6.0, "PCI Express* Riser Card" — Describes the specifications of the standard PCI Express riser card.

Chapter 7.0, "PCI/PCI-X* Riser Card" — Describes the specifications of the optional PCI-X riser card.

Chapter 8.0, "AC Power Subsystem" — Describes the specifications of the AC-input power subsystem.

Chapter 9.0, "DC Power Subsystem" — Describes the specifications of the DC-input power subsystem.

Chapter 10.0, "Regulatory Specifications" — Describes system compliance to regulatory specifications.

2.0 System Overview

This chapter describes the features of the Intel® IP Network Server NSW1U.

This chapter is organized into the following sections.

- Introduction
- External Chassis Features
- Internal Chassis Features
- Server Management
- Specifications

2.1 Introduction

The Intel® IP Network Server NSW1U is a compact, high-density, rack-mount server system with support for one Quad-Core Intel® Xeon® processor 5400 series or one Dual-Core Intel® Xeon® processor 5100 series and up to 24 Gbytes of DDR2-667 FBD ECC DIMM memory. The IP Network Server NSW1U supports high availability features such as hot-swap and redundant power supply modules. The scalable architecture of the IP Network Server NSW1U supports a variety of operating systems.

The IP Network Server NSW1U is available in three different I/O configurations. Most server features are common to all three configurations. The following terminology will be used when it is necessary to describe any of the configurations individually:

- NSW1U-F or NSW1U-FNIC — server configuration with front panel Ethernet connections.
- NSW1U-R or NSW1U-RNIC — server configuration with rear Ethernet connections.
- NSW1U-B or NSW1U-Bypass — server configuration with both front and rear Ethernet access and bypass capability for front-panel connections.

Figure 1 shows the IP Network Server NSW1U system assembled. Figure 2 shows the system with the top cover and the front bezel removed. These figures show the IP Network Server NSW1U-FNIC (front panel Ethernet access) configuration with optional additional Ethernet ports.

Figure 1. Intel® IP Network Server NSW1U (Top Cover On)

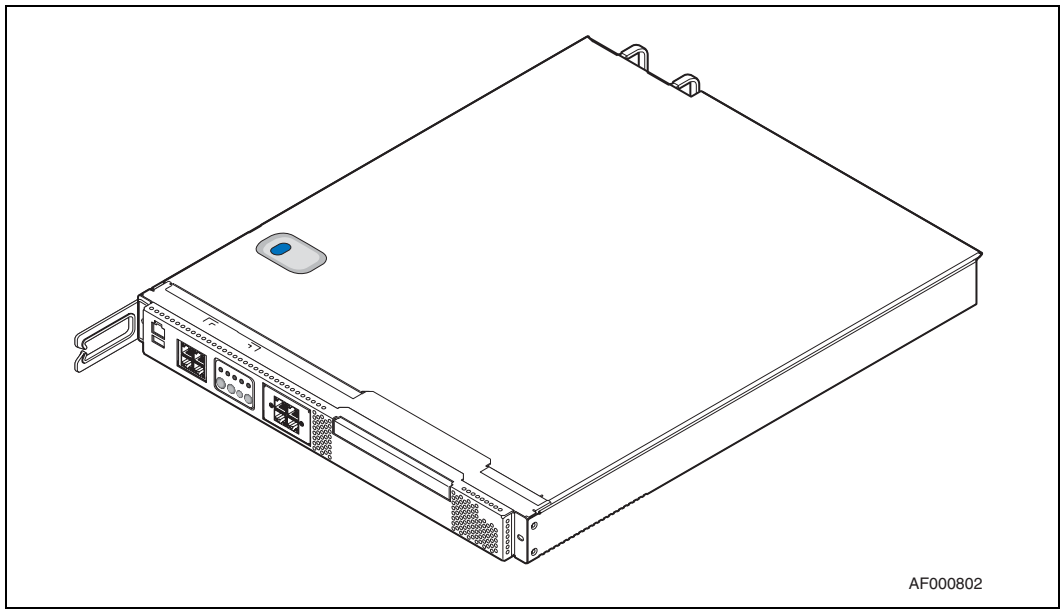
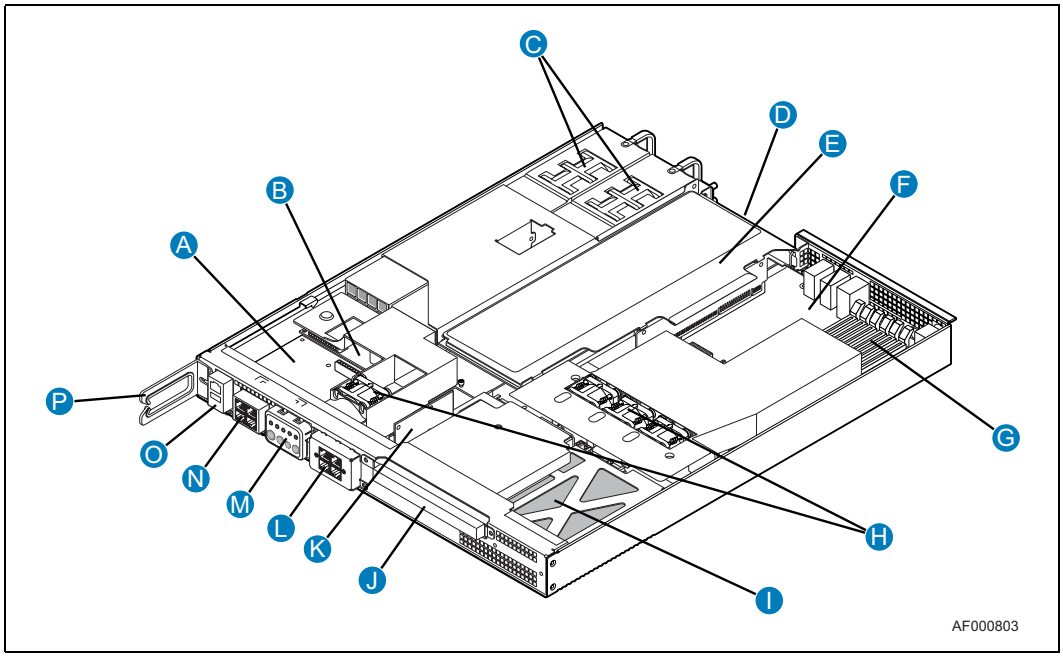


Figure 2. Intel® IP Network Server NSW1U (Top Cover Off)



Item	Description	Item	Description
A	Front panel board	I	2x SATA hard disk drive bays
B	Power distribution board (PDB)	J	Optical drive (optional) or filler panel
C	Power supply units, AC or DC input (one PSU standard, second PSU optional)	K	Intel® Z-U130 Value Solid State Drive (optional)
D	PCI-X* or PCI Express* card bracket	L	4x GbE NIC connectors (optional)
E	Adapter card/riser card assembly (PCI-X or PCI Express)	M	Front panel LEDs and switches
F	Server Board S5000PHB	N	4x GbE NIC connectors (NSW1U-FNIC and NSW1U-Bypass only)
G	System memory	O	Serial port (RJ45) and USB 2.0 connectors
H	System fans	P	Cable management bracket (optional)

2.1.1 IP Network Server NSW1U Features

Table 1 provides a list and brief description of the features of the IP Network Server NSW1U.

Table 1. IP Network Server NSW1U Feature List

Feature	Description
Compact, high-density system	Rack-mount server with a height of 1U (1.75 inches) and a depth of 20.0 inches
Configuration flexibility	One-way capability in low profile and cost/value-effective packaging Stand-alone system Quad-Core Intel® Xeon® processor 5400 series or Dual-Core Intel® Xeon® processor 5100 series. Note: Quad-Core Intel® Xeon® processor 5400 series support is available only on NSW1U-R and NSW1U-B that have product codes NSRA0201W, NSRD0201W, or NSRA0401W
Serviceability	Rear access to hot-swappable power supplies
Availability	Support for two, hot-swappable, 450 W power supplies in a redundant (1+1) configuration (with optional second PSU) Integrated software RAID 0 or RAID 1 with two internal SATA disk drives Memory rank sparing
Manageability	Remote management and diagnostics support Emergency management port (serial and LAN) IPMI 2.0 compliant Support for Intel® Z-U130 Value Solid State Drive (optional)
Upgradeability and investment protection	Supports Quad-Core Intel® Xeon® processor 5400 series or Dual-Core Intel® Xeon® processor 5100 series. Note: Quad-Core Intel® Xeon® processor 5400 series support is available only on NSW1U-R and NSW1U-B that have product codes NSRA0201W, NSRD0201W, or NSRA0401W Multi-generational chassis Supports Intel® 64 architecture (formerly known as Extended Memory 64 Technology)

Table 1. IP Network Server NSW1U Feature List (Continued)

Feature	Description	
System-level scalability	24 Gbyte DDR2-667 MHz Registered SDRAM FBD DIMM memory support Single Quad-Core Intel® Xeon® processor 5400 series or Dual-Core Intel® Xeon® processor 5100 series. Note: Quad-Core Intel® Xeon® processor 5400 series support is available only on NSW1U-R and NSW1U-B that have product codes NSRA0201W, NSRD0201W, or NSRA0401W Riser cards support one full-length, full-height PCI Express or PCI/PCI-X slot Two internal fixed 3.5-inch SATA hard disk drives Support for low-profile PATA optical drive (CD or DVD)	
Front panel	Power switch Reset switch NMI switch ID switch	Main power LED System status LED HDD activity LED NIC activity LED ID LED
I/O	Front Access • Four standard GbE NIC ports on NSW1U-F and NSW1U-B only (no front NIC ports on NSW1U-R) • Four optional NIC ports (requires Intel® PRO/1000 AT Quad Port Bypass Adapter (for copper connectivity) or Intel® PRO/1000 AF Quad Port Bypass Adapter for fiber connectivity) • Serial B/COM2 port (RJ45) • One USB 2.0 port	Rear Access • Four standard GbE NIC ports on NSW1U-R and NSW1U-B only (no rear NIC ports on NSW1U-F) • Four optional NIC ports (requires Intel® PRO/1000 AT Quad Port Bypass Adapter (for copper connectivity) or Intel® PRO/1000 AF Quad Port Bypass Adapter for fiber connectivity) • Serial B/COM2 port (RJ45) • Two USB 2.0 ports • GCM 100 Mbps management port (requires optional Intel® RMM2 kit) • Two PS/2 ports for keyboard and mouse • Video port

The Intel® Server Board S5000PHB is mounted horizontally toward the rear of the chassis, behind the system fan array. The server board uses an LGA 771 processor socket, and has six DIMM slots for up to 24 Gbytes of error checking and correcting (ECC) FBD memory. The server board also contains one PCI Super Slot to accommodate a full-height, full-length PCI, PCI-X, or x8 PCI Express (PCIe) add-in board by means of a riser card, plus input/output (I/O) ports and various controllers.

The hot-swappable power supply modules are installed at the left-rear of the chassis, as shown in Figure 2. Both AC-input and DC-input modules are available, and two 450 W power supply modules can be installed for a 1+1 redundant configuration. A filler module for the empty power supply location is supplied for systems without power supply redundancy.

One or two 3.5-inch SATA hard drives can be mounted in fixed drive trays in the bottom front of the IP Network Server NSW1U chassis. Figure 2 shows the location of the SATA fixed drive trays, which can only be accessed with the top cover removed. Integrated support for software RAID levels 0 and 1 is provided.

One slim-line (0.5 inch) IDE optical drive (CD-ROM or DVD) can be mounted using a drive tray assembly inserted into the front of the system. The optical drive is located above the hard drives as shown in Figure 2. Product codes NSRA0201W, NSRD0201W, and NSRA0401W include mounting hardware for optical devices in the accessory package. Users with earlier product codes can purchase the TMWCDRMC01W kit.

The front panel I/O board (referred to in this document as the *Ethernet front panel board* or *EFP board*) is located in front of the power supplies and extends behind the fixed SATA hard drives. The SATA drives connect into the EFP board for power and signals. The EFP board also provides the user interface for the system's front panel and for the SIO (system management) serial port. Three unique EFP board assemblies are used to provide the different Ethernet port configurations of the different NSW1U variants:

- The NSW1U-FNIC system uses an EFP board that provides four GbE NIC ports that are accessible from the front of the system when the bezel is installed. No NIC ports are accessible from the rear of a standard NSW1U-F system.
- The NSW1U-RNIC has four GbE NIC ports that are mounted on the server board and are accessible from the rear of the chassis. No NIC ports are accessible from the front of a standard NSW1U-R system.
- The NSW1U-Bypass has four GbE NIC ports that are mounted on the server board and are accessible from the rear of the chassis (ports 1 through 4), and four GbE NIC ports that are provided by a unique EFP board assembly and are accessible from the front of the chassis (ports 5 through 8). The four front-accessible NIC ports have bypass capability, where one pair of ports can be directly connected to the other pair through bypass relays to electrically bypass the server.

All three NSW1U configurations support the optional addition of four GbE NIC ports through the installation of an Intel® PRO/1000 AT Quad Port Bypass Adapter (for copper connectivity) or an Intel® PRO/1000 AF Quad Port Bypass Adapter for fiber connectivity). Each of the two pairs of ports can be connected together through relays to electrically bypass the server. Two versions of the Quad Port Bypass Adapter card are available. One version of the card mounts the RJ45 connectors on the card's I/O bracket to make the additional NICs available at the server's rear panel; this version is most commonly used with the NSW1U-R server configuration. The other card version has no connectors on the I/O bracket, but is supplied with a cable/connector assembly and escutcheon to mount the additional NICs on the server's front panel.

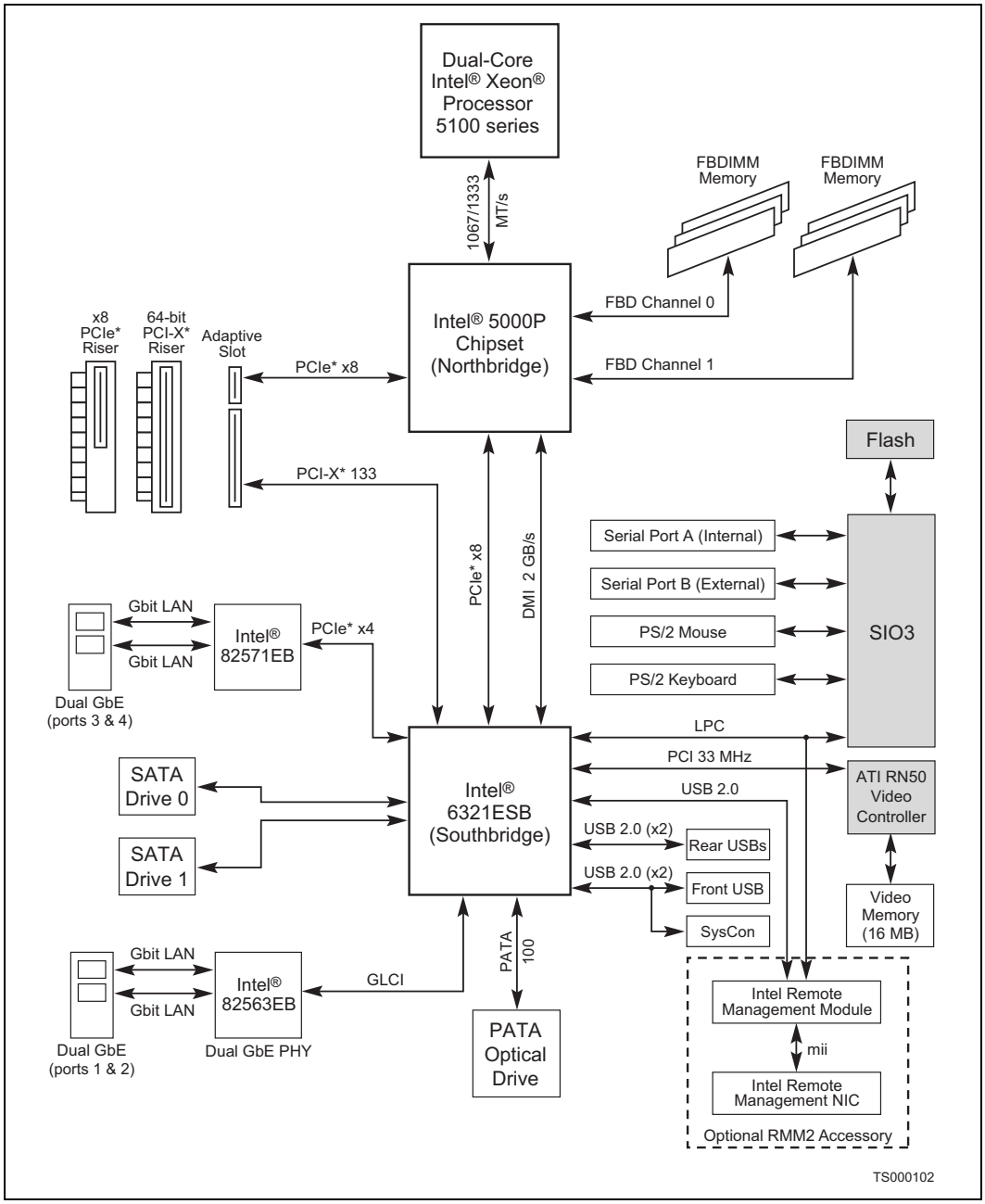
The front bezel can be painted to meet OEM industrial design requirements. The bezel design allows adequate airflow to cool the system components.

The system contains one 40 × 40 × 28 mm, single-rotor fan to cool the PCI area of the server board and three more of these fans to cool the CPU, memory, and other server board components. The PCI fan is located to the left of the hard drive area and in front of the power distribution board (PDB). The CPU/memory fans are installed directly behind the SATA hard drives and directly in front of the server board as shown in Figure 2. The PCI fan connector is located on the EFP board to the left of the PCI fan. The connectors for the CPU/memory fans are located on the EFP board in front of the fans. A fan failure is indicated by one of the fault light-emitting diodes (LEDs) located on the EFP board.

For clarity, separate functional block diagrams are provided for the three different configurations of the IP Network Server NSW1U:

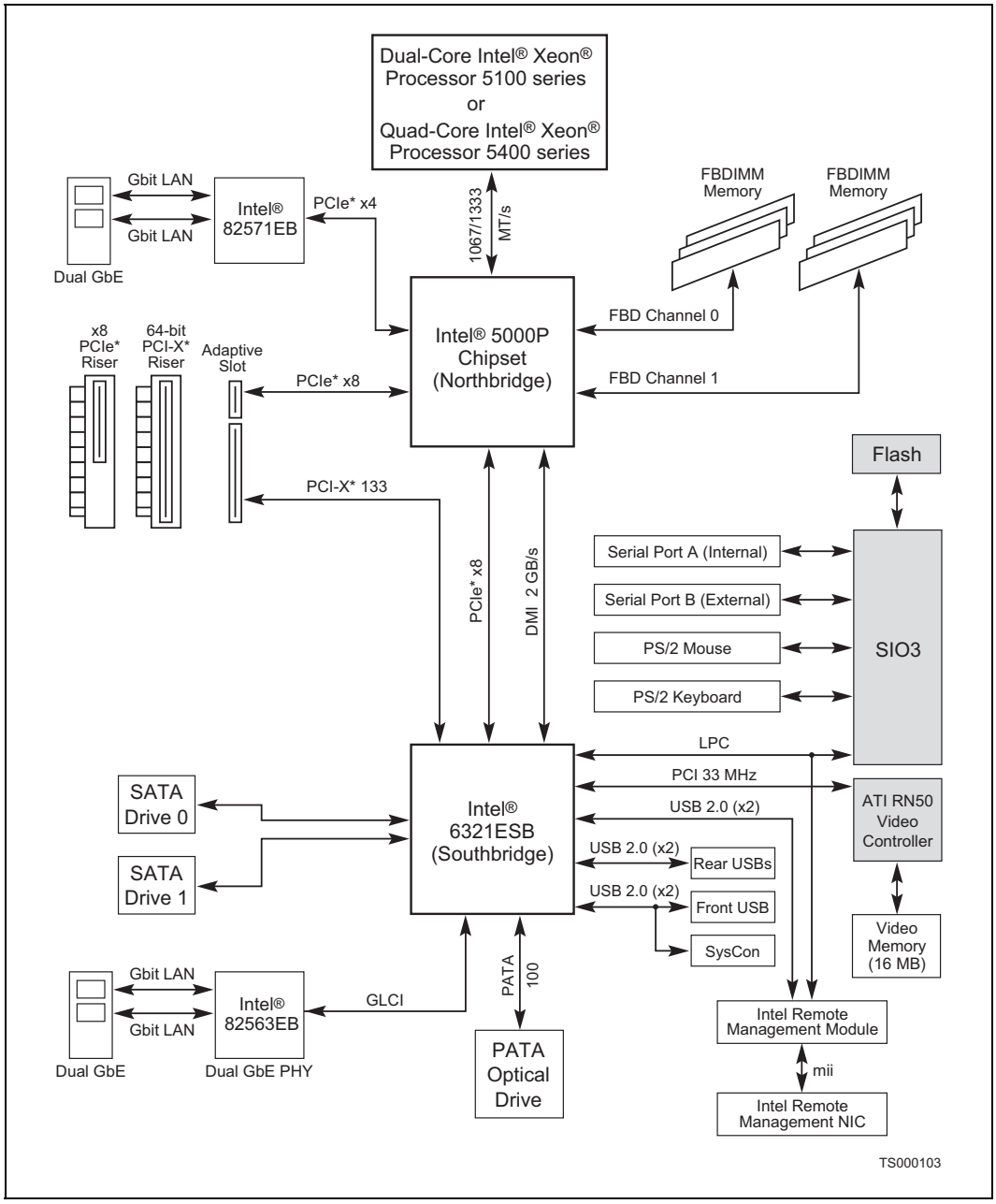
- Figure 3 shows a functional block diagram of the Front NIC version (NSW1U-F).
- Figure 4 shows a functional block diagram of the Rear NIC version (NSW1U-R).
- Figure 5 shows a functional block diagram of the NIC Bypass version (NSW1U-B).

Figure 3. IP Network Server NSW1U Functional Block Diagram, Front NIC Configuration



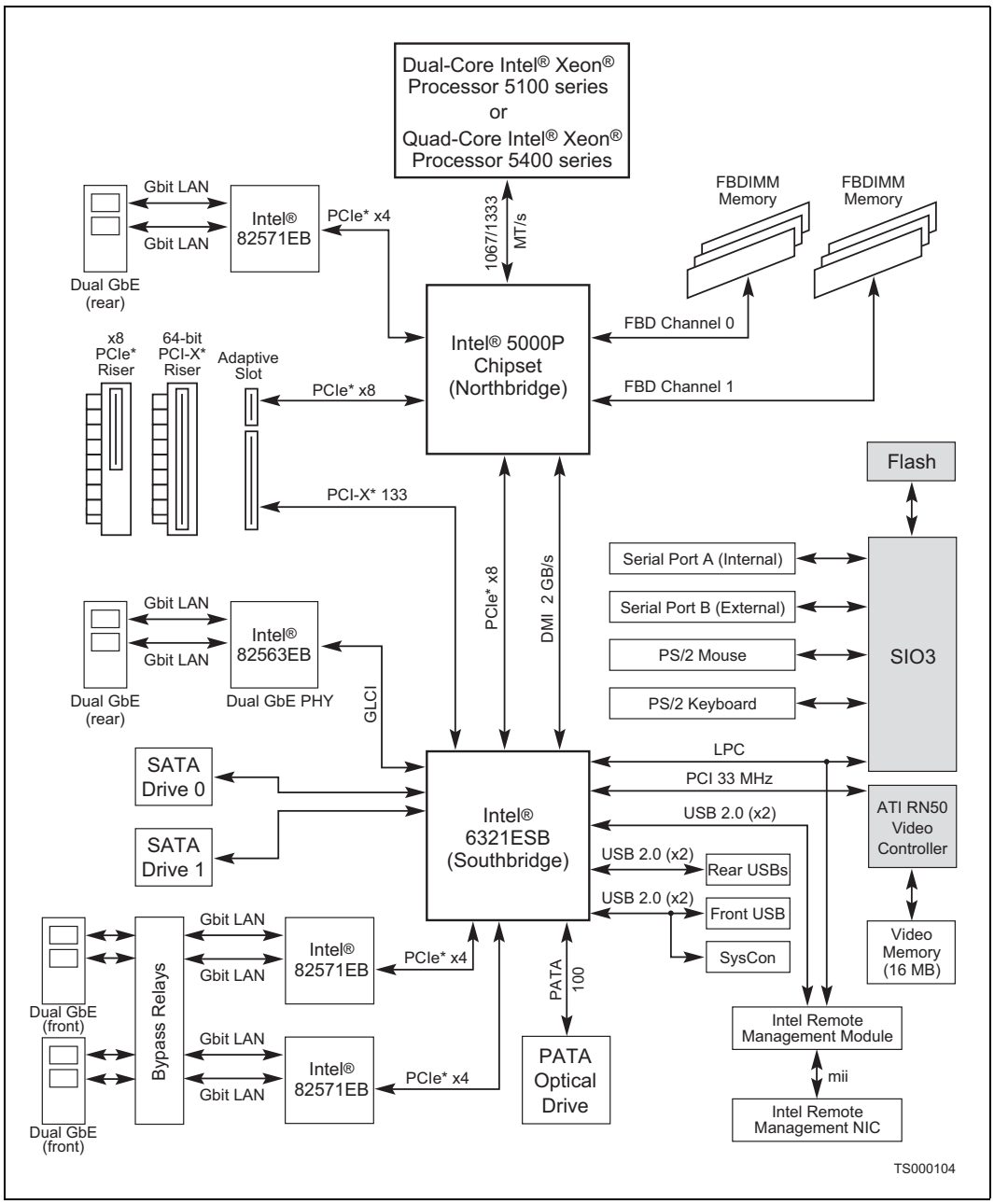
Note: The NSW1U-F has no NIC ports on the rear of the system chassis.

Figure 4. IP Network Server NSW1U Functional Block Diagram, Rear NIC Configuration



Note: The NSW1U-R has no NIC ports on the EFP board or the front panel of the chassis.

Figure 5. IP Network Server NSW1U Functional Block Diagram, NIC Bypass Configuration



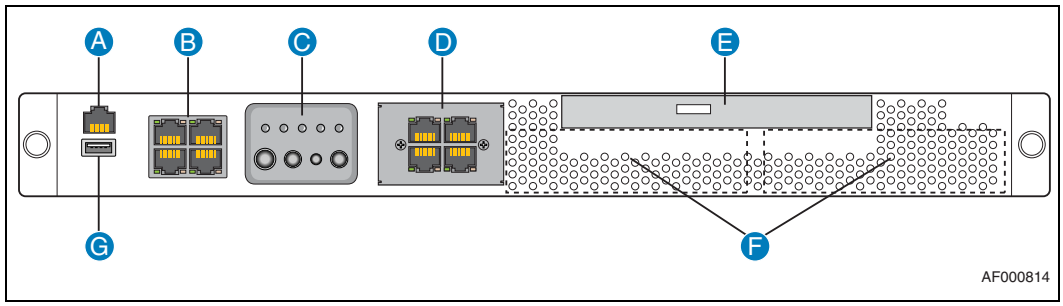
2.2 External Chassis Features

2.2.1 NSW1U-F/NSW1U-B System Chassis Front Panel

2.2.1.1 NSW1U-F/NSW1U-B System Front View

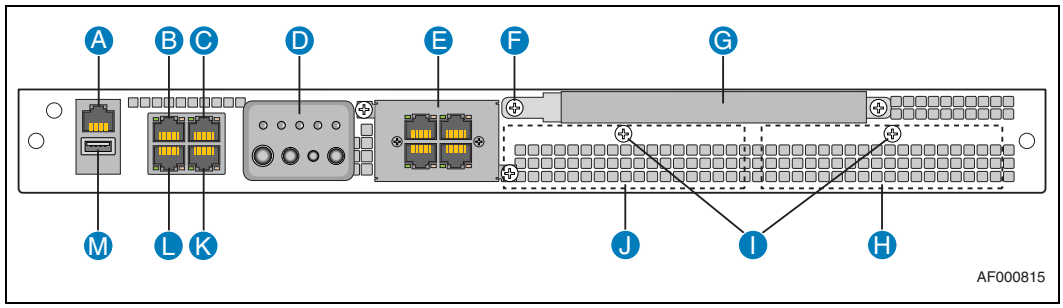
Figure 6 shows the front view of an NSW1U-FNIC or NSW1U-Bypass system with the bezel installed. Figure 7 shows the front view of the system with the bezel removed.

Figure 6. Front View of NSW1U-F/NSW1U-B System (Bezel Installed)



Item	Description	Item	Description
A	COM2/Serial B serial port connector (RJ45)	E	Optical drive (optional) or filler panel
B	4x GbE NIC port connectors	F	3.5-inch hard drive bays 0 and 1
C	Front-panel control switches and status LEDs	G	USB 2.0 port connector, port 2
D	4x GbE NIC port connectors (optional)		

Figure 7. Front View of NSW1U-F/NSW1U-B Systems (Bezel Removed)



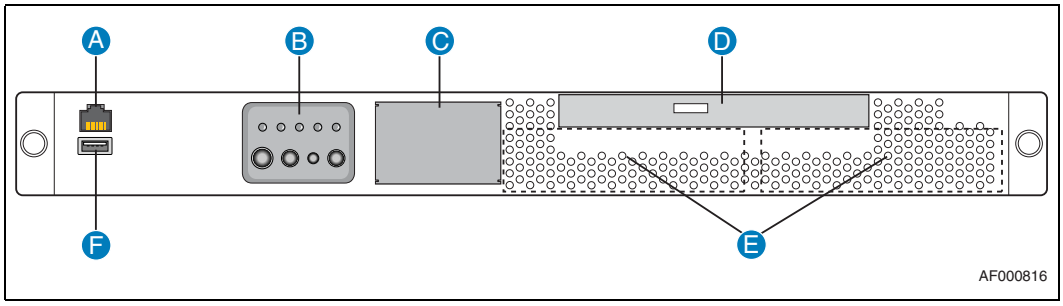
Item	Description	Item	Description
A	COM2/Serial B serial port connector (RJ45)	H	Hard drive bay 0
B	GbE NIC port connector, port 3 †	I	Hard drive retaining screws
C	GbE NIC port connector, port 1 †	J	Hard drive bay 1
D	Front-panel control switches and status LEDs	K	GbE NIC port connector, port 2 †
† ‡	On NSW1U-Bypass systems, front panel NIC ports 1-4 are identified in BIOS as 5-8, respectively. On NSW1U-FNIC systems only, Port 1 has a second MAC address that provides access to the baseboard management controller to enable remote IPMI management over LAN.		

Item	Description	Item	Description
E	4x GbE NIC port connectors (optional), port numbers as indicated on escutcheon	L	GbE NIC port connector, port 4 † ‡
F	Optical drive captive fastener	M	USB 2.0 port connector, port 2
G	Optical drive or filler panel (as shown here)		
† ‡	On NSW1U-Bypass systems, front panel NIC ports 1-4 are identified in BIOS as 5-8, respectively. On NSW1U-FNIC systems only, Port 1 has a second MAC address that provides access to the baseboard management controller to enable remote IPMI management over LAN.		

2.2.1.2 NSW1U-R System Front View

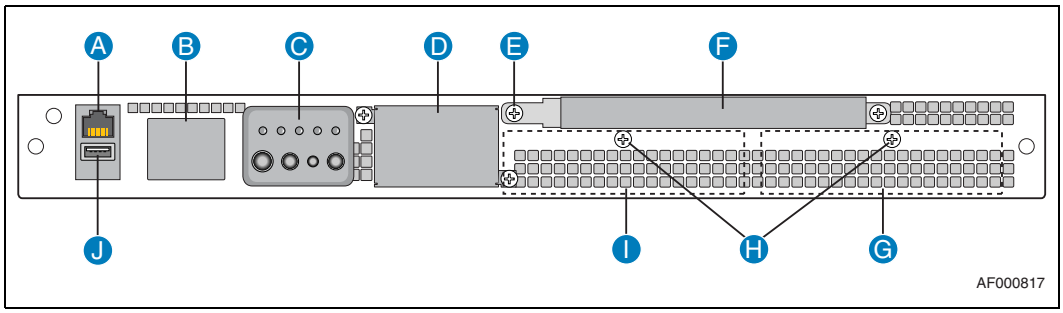
Figure 8 shows the front view of the NSW1U-RNIC system with the bezel installed. Figure 9 shows the front view of the system with the bezel removed.

Figure 8. Front View of NSW1U-R System (Bezel Installed)



Item	Description	Item	Description
A	COM2/Serial B serial port connector (RJ45)	D	Optical drive (optional) or filler panel
B	Front-panel control switches and status LEDs	E	3.5-inch hard drive bays 0 and 1
C	4x GbE NIC connectors (optional) or filler panel (shown)	F	USB 2.0 port connector (port 2)

Figure 9. Front View of NSW1U-R System (Bezel Removed)



Item	Description	Item	Description
A	COM2/Serial B serial port connector (RJ45)	F	Optical drive or filler panel (as shown here)
B	Filler panel	G	Hard drive bay 0 (behind panel)
C	Front-panel control switches and status LEDs	H	Hard drive retaining screws
D	4x GbE NIC connectors (optional) or filler panel (shown)	I	Hard drive bay 1 (behind panel)
E	Optical drive captive fastener	J	USB 2.0 port connector (port 2)

2.2.2 Front Panel Features

The front panel features are shown in Figure 10 and described in Figure 2. All front panel control switches and status LEDs are located on the EFP system board. (See Section 4.3, “Front Panel Switches, LEDs, and Relays” on page 57, for a detailed description of the control switches and status LEDs contained on the EFP board.)

Figure 10. IP Network Server NSW1U Front Panel Details

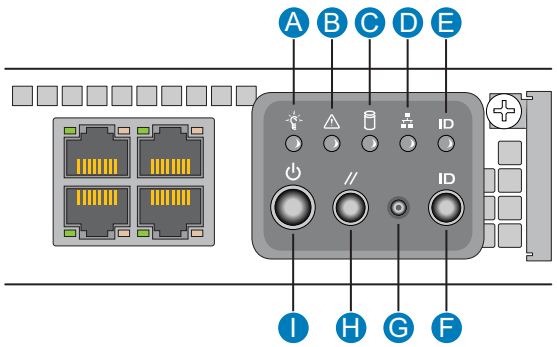


Table 2. Front Panel Features

Item	Feature	Description
	Front Panel Status LEDs	
A	Main power LED (green)	When continuously lit, this indicates the presence of DC power in the server. The LED turns off when the input power is turned off or if the power source is disrupted.
B	System Status (green/amber)	Indicates system status: • Steady green indicates system in standby or ready for operation. • Blinking green indicates degraded operation (e.g., power supply redundancy loss, battery failure, non-critical sensor threshold crossed, non-critical fan failure). • Blinking amber indicates one or more non-fatal fault conditions (e.g., excessive memory errors, critical sensor threshold crossed, insufficient fans operating). • Steady amber indicates one or more fatal fault conditions (e.g., power system failure, no good memory, CPU error or thermal condition).
C	HDD activity LED (green)	Indicates HDD activity when lit. This is an OR’ed indication for both HDDs.
D	NIC activity LED (green)	Indicates NIC activity when lit.

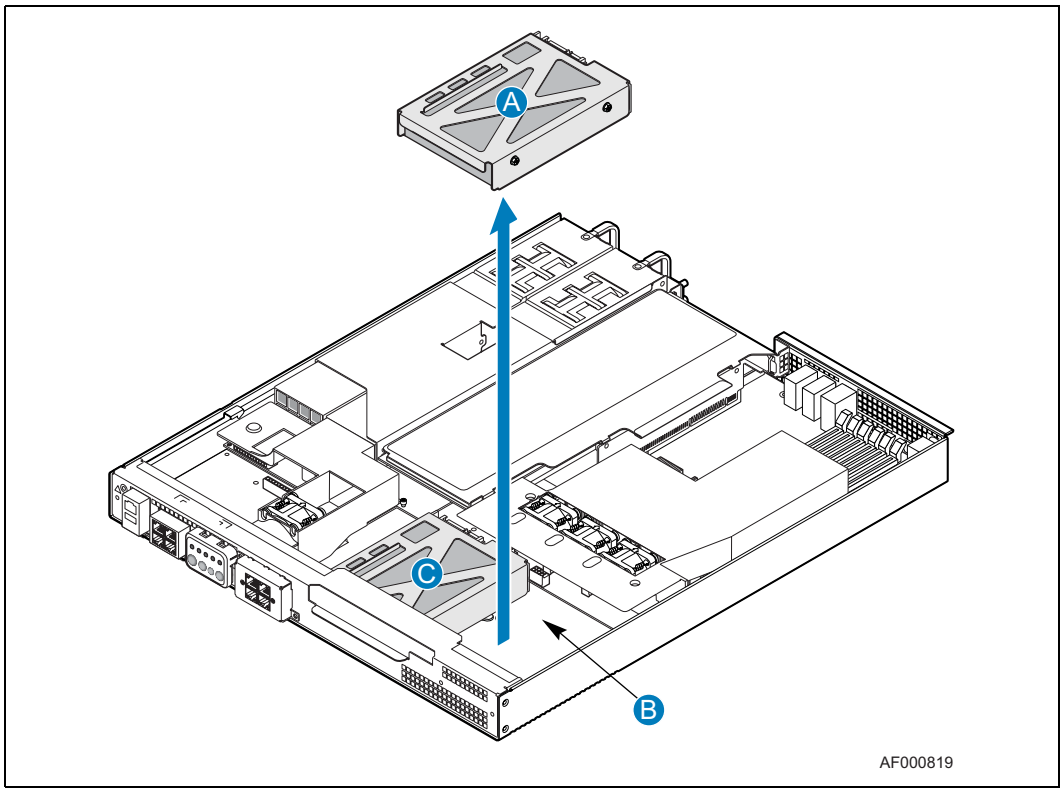
Table 2. Front Panel Features (Continued)

Item	Feature	Description
E	System ID LED (blue)	Can be toggled remotely or by front-panel ID switch for identification purposes.
	Front Panel Switches	
F	ID switch	Toggles system ID LED.
G	NMI switch	Asserts NMI to server board.
H	Reset switch	Resets the system.
I	Power switch	Toggles the system power.

2.2.3 Hard Drives

The chassis provides two fixed hard drives that are accessible from the front of the system when the system's top cover is removed. SATA 3.5-inch hard disk drives are mounted in fixed drive trays that are secured to the chassis base with two screws.

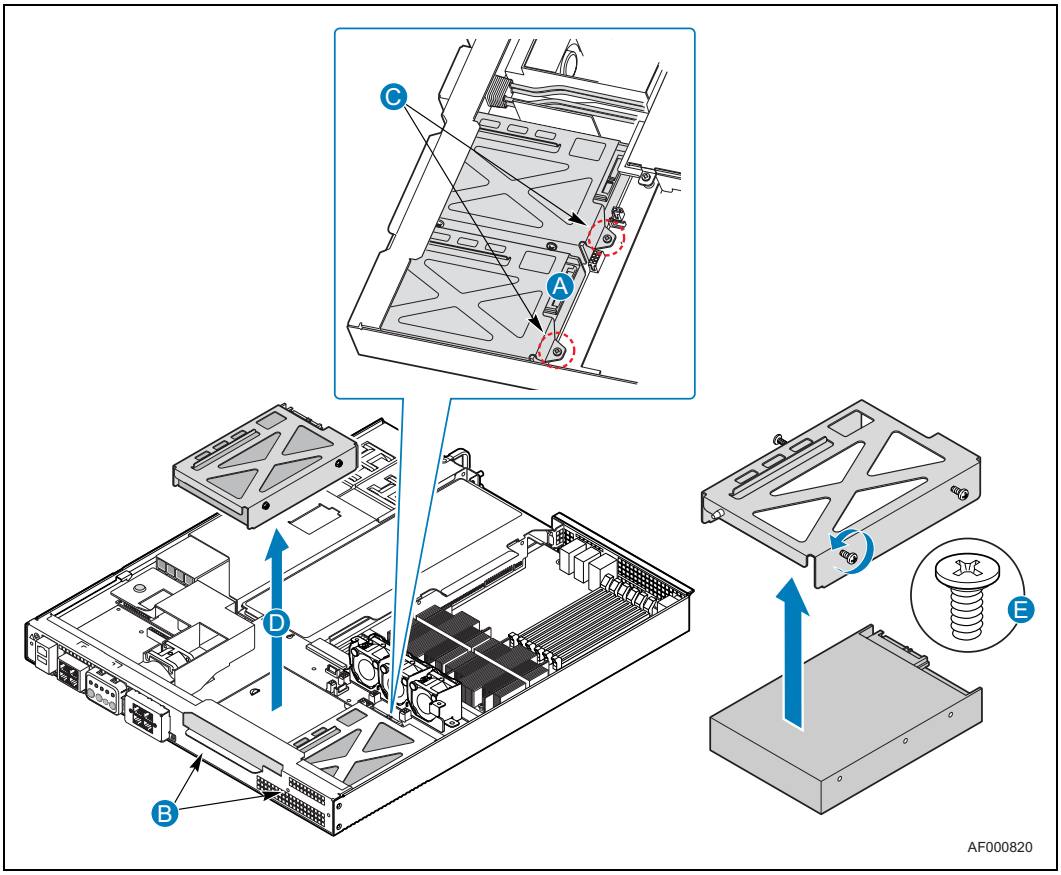
Figure 11. Hard Drive Locations



2.2.3.1 SATA Hard Drive Tray Assembly

Each hard drive must be mounted to a fixed drive tray using three captive, grommet-isolated screws inserted into the sides of the drive as shown in Figure 12.

Figure 12. Hard Drive Tray Assembly

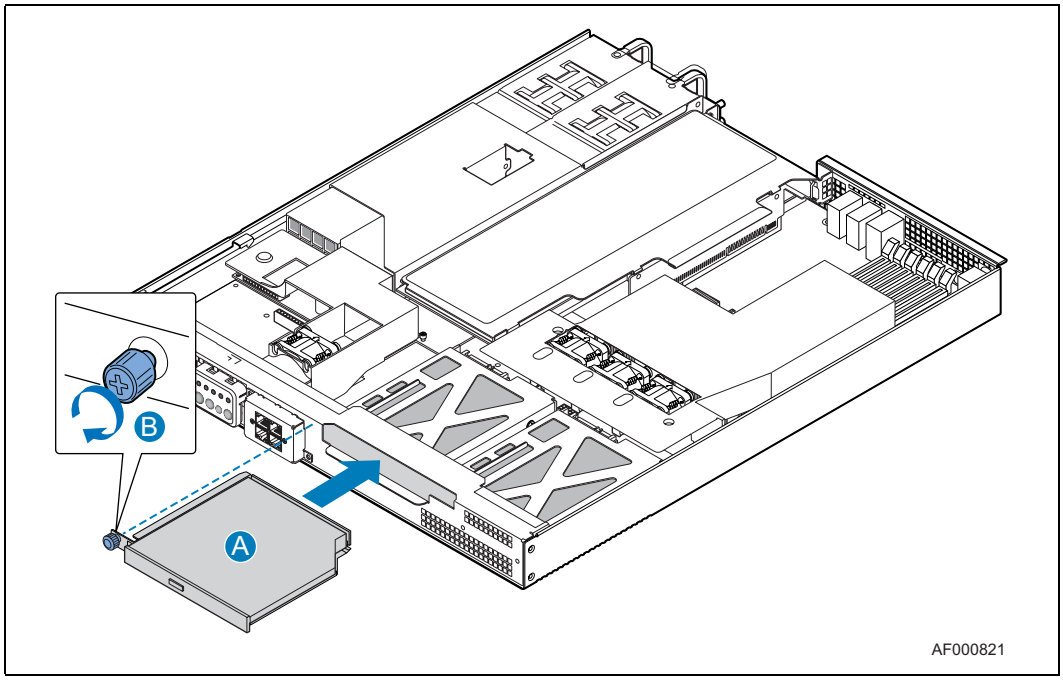


2.2.4 Optical Drive

The chassis provides for a front-accessible optical drive (CD-ROM or DVD). This drive is mounted in a non-hot swappable tray at the front of the system. The bezel must be removed to install or remove the optical drive. See Figure 13. The tray is secured by one captive fastener. The optical drive tray assembly accommodates a 0.5-inch (12.7 mm) slim-line optical drive.

Caution: The optical drive tray assembly can be removed only when the system is powered off and the IDE signal and optical drive power cables are disconnected from the back of the drive tray assembly.

Figure 13. Optical Drive Tray Mounting



2.2.4.1 Optical Drive Tray Assembly

The optical drive is installed in a drive tray assembly before installing it into the server system. An interposer board that provides power and signal cable connections is installed on the rear of the optical drive. An exploded view of the optical drive tray assembly is shown in Figure 14.

Two cables are required to interconnect the optical drive interposer board to the server board and the EFP board:

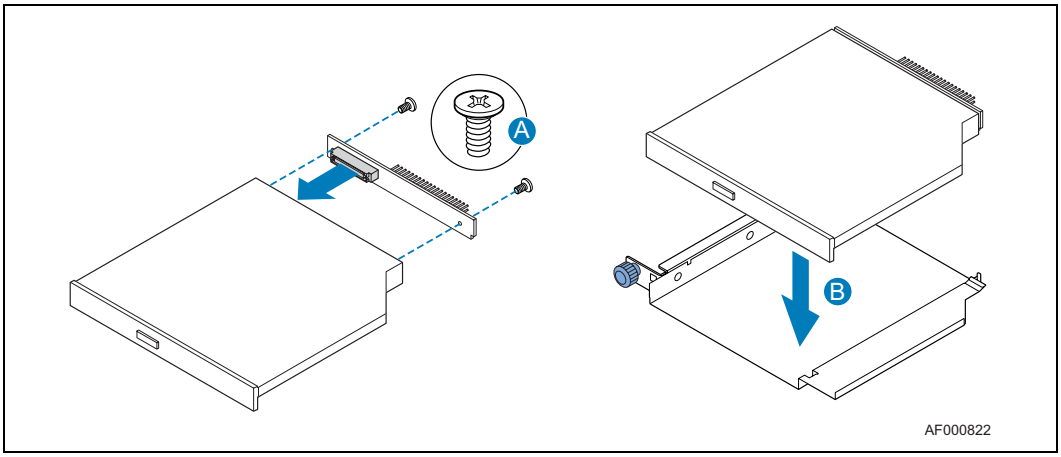
- A 40-wire IDE cable connect the 2×20 IDE connector on the optical drive interposer board to the 2×20 IDE connector on the server board.
- A two-wire discrete power cable connects the 1×4 connector on the interposer board to the EFP board.

Product codes NSRA0201W, NSRD0201W, and NSRA0401W include the mounting hardware for optical devices. The following mounting hardware is in the accessory kit in your product box:

- Interposer
- IDE cable
- Power cable
- Mounting screws
- Mounting bracket

See Section 3.2.2 and Section 3.2.3 for cable details.

Figure 14. Optical Drive Tray Assembly

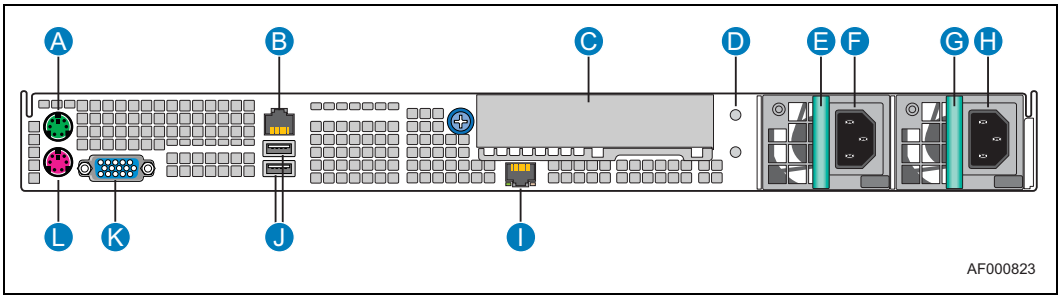


Item	Description	Item	Description
A	Interposer board and two screws to secure the board to the optical drive	B	Optical drive and drive tray metal housing

2.2.5 Chassis Rear Panel

2.2.5.1 NSW1U-F System Rear View

Figure 15. Rear View of NSW1U-F

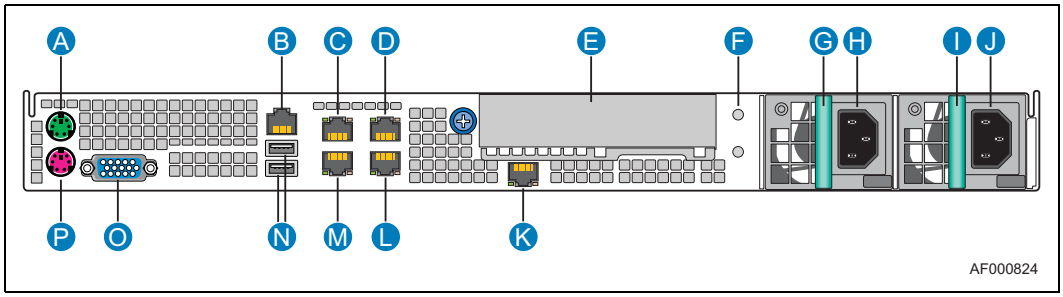


Item	Description	Item	Description
A	PS/2 mouse connector	G	Power supply 2 (optional) or filler panel †
B	COM2/Serial B serial port connector (RJ45)	H	Power supply 2 AC input connector †
C	PCI-X/PCIe I/O bracket or filler panel (shown)	I	GCM management port (requires optional Remote Management Module) or filler panel
D	Ground studs (used for DC-input systems)	J	USB connectors, ports 0 (bottom) and 1 (top)
E	Power supply 1 †	K	Video connector
F	Power supply 1 AC input connector †	L	PS/2 keyboard connector
†	Items E through H in Figure 15 illustrate the AC-input configuration of the IP Network Server NSW1U. DC-input power supply modules are also available.		

Note: Rear NIC ports are not accessible and are closed off by an EMI gasket.

2.2.5.2 NSW1U-R/NSW1U-B System Rear View

Figure 16. Rear View of NSW1U-R/NSW1U-B



Item	Description	Item	Description
A	PS/2 mouse connector	I	Power supply 2 (optional) or filler panel †
B	COM2/Serial B serial port connector (RJ45)	J	Power supply 2 AC input connector †
C	GbE NIC port 3 connector	K	GCM management port (requires optional Remote Management Module) or filler panel
D	GbE NIC port 2 connector	L	GbE NIC port 1 connector ††
E	PCI/PCIe I/O bracket or filler panel (shown)	M	GbE NIC port 4 connector
F	Ground studs (used on systems with DC-input power supplies)	N	USB connectors, ports 0 (bottom) and 1 (top)
G	Power supply 1 †	O	Video connector
H	Power supply 1 AC input connector †	P	PS/2 keyboard connector
†	Items G through J in Figure 16 reflect the AC-input configuration of the IP Network Server NSW1U. DC-input power supply modules are also available.		
††	Port 1 has a second MAC address that provides access to the baseboard management controller to enable remote IPMI management over LAN.		

2.3 Internal Chassis Features

2.3.1 Intel® Server Board S5000PHB

See the *Intel® Server Board S5000PHB Technical Product Specification* for detailed information about this server board.

2.3.2 PCI/PCI Express Adapter Subsystem

The Server Board S5000PHB implements a PCI super slot that contains the signals necessary for a PCI-X* or PCI Express* (PCIe*) expansion slot. One of two different low-profile riser cards is inserted into the super slot to access the appropriate signals and provide the appropriate connector for a PCI/PCI-X or PCI Express adapter card. The server accommodates full-length, full-height adapter cards with the card's I/O bracket accessible through an opening in the rear panel of the system.

The server is delivered with the PCIe riser card installed in the system board riser slot. To use a PCI/PCI-X adapter card, the PCIe riser card must be replaced with a PCI/PCI-X riser card, which may be ordered as an accessory.

To add an adapter card to the system, a user removes the riser card assembly from the system and removes the I/O filler panel from the rear of the server. After attaching the appropriate riser card to the PCI or PCIe adapter card, this assembly is plugged into the

super slot connector near the center of the Server Board S5000PHB. See the *Intel® Server Board S5000PHB Technical Product Specification* for electrical characteristics for this PCI/PCIe adapter subsystem.

Note: See the Intel® IP Network Server NSW1U *Tested Hardware and Operating System List* (THOL) for a list of supported adapter cards.

The PCI-X riser card implements a 64-bit PCI slot with bus speeds of 33 MHz or 66 MHz for PCI adapter cards or 66 MHz, 100 MHz, or 133 MHz for PCI-X cards.

The PCI Express riser card implements a x8 link interface, and can be used with adapter cards that implement x1, x4, or x8 interfaces.

2.3.3 Power Subsystem

The power subsystem consists of up to two hot-swappable power supply units (PSU) and a power distribution board (PDB). The system can be configured and operated with either an AC or DC input PSU located at the left rear of the chassis and dock into a common PDB. The system can contain up to two PSUs and can be configured as follows:

- Two PSUs installed, (1+1) power redundancy for maximally loaded system
- One PSU installed, non-redundant for maximally loaded system

When the system is configured with two power supply modules, the hot-swap feature allows the user to replace a failed PSU without interrupting system operation. To ensure that all components remain within specification under all system environmental conditions, it is recommended that PSU hot-swap operations not exceed two minutes in duration.

Power from the power subsystem is carried directly to the server board through a docking connector between the PDB and the server board. Front panel board power is provided from the PDB through a cable. Peripheral devices are powered from the front panel board via discrete cables between the device and the front panel board. One PSU is capable of handling the worst-case power requirements for a fully configured IP Network Server NSW1U system. This includes one Dual-Core Intel® Xeon® processor, 24 Gbytes of memory, two 3.5-inch SATA hard drives at 18 W per drive (typical worst case for 3.5-inch by 1.0-inch, 15 k RPM drive), and one full-height, full-length PCI or PCI Express add-in board at 25 W.

Note: The total power requirements for the IP Network Server NSW1U system exceeds the 240 VA energy hazard limits, which defines an operator-accessible area. Only qualified technical individuals should access the processor, memory, and I/O areas on the Intel® Server Board S5000PHB while the system is energized.

See Chapter 8.0, “AC Power Subsystem”, or Chapter 9.0, “DC Power Subsystem”, in this document for detailed power specifications.

Figure 17. AC-input Power Supply Module (Input End)

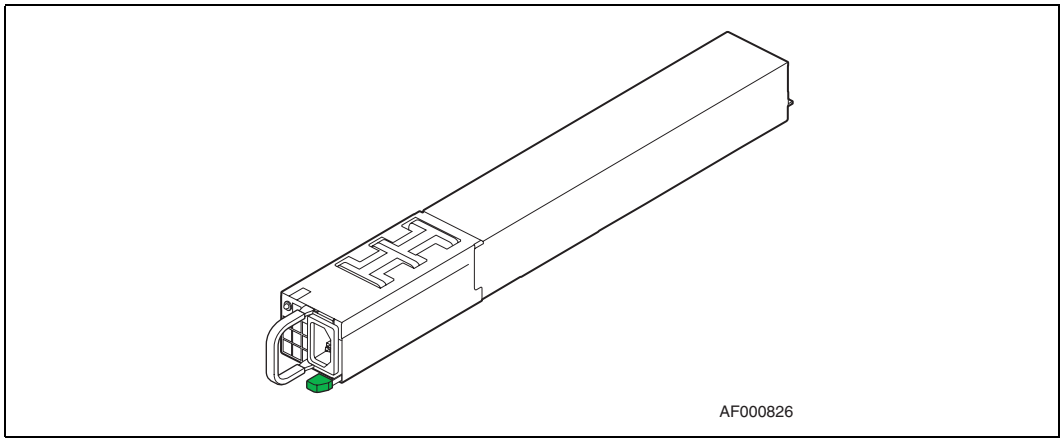


Figure 18. DC-input Power Supply Module (Input End)

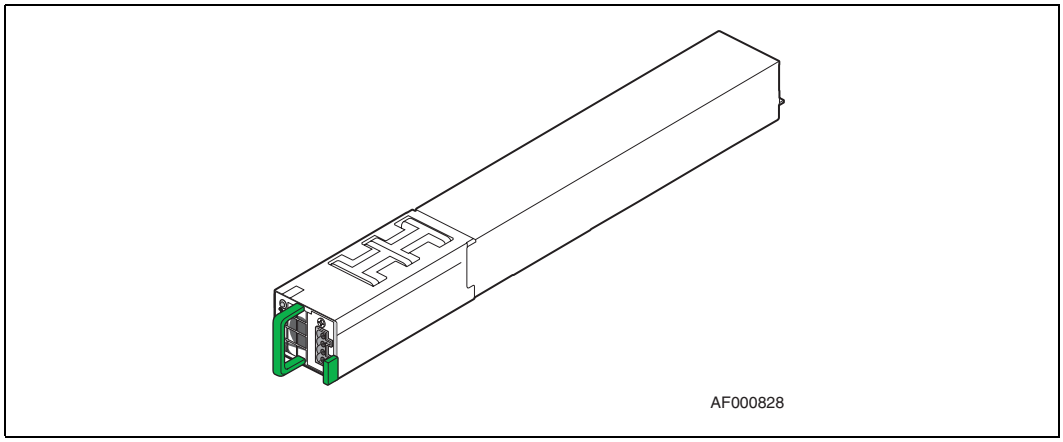
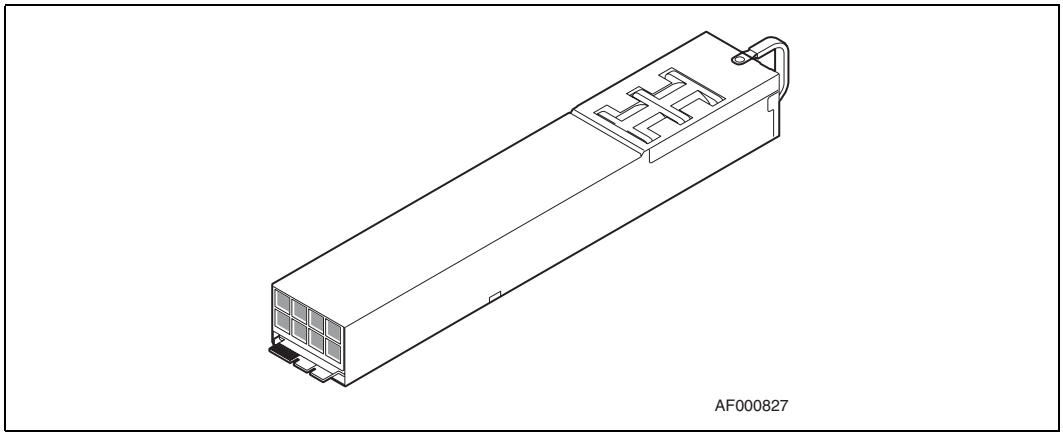


Figure 19. AC-input or DC-input Power Supply Module (Output End)

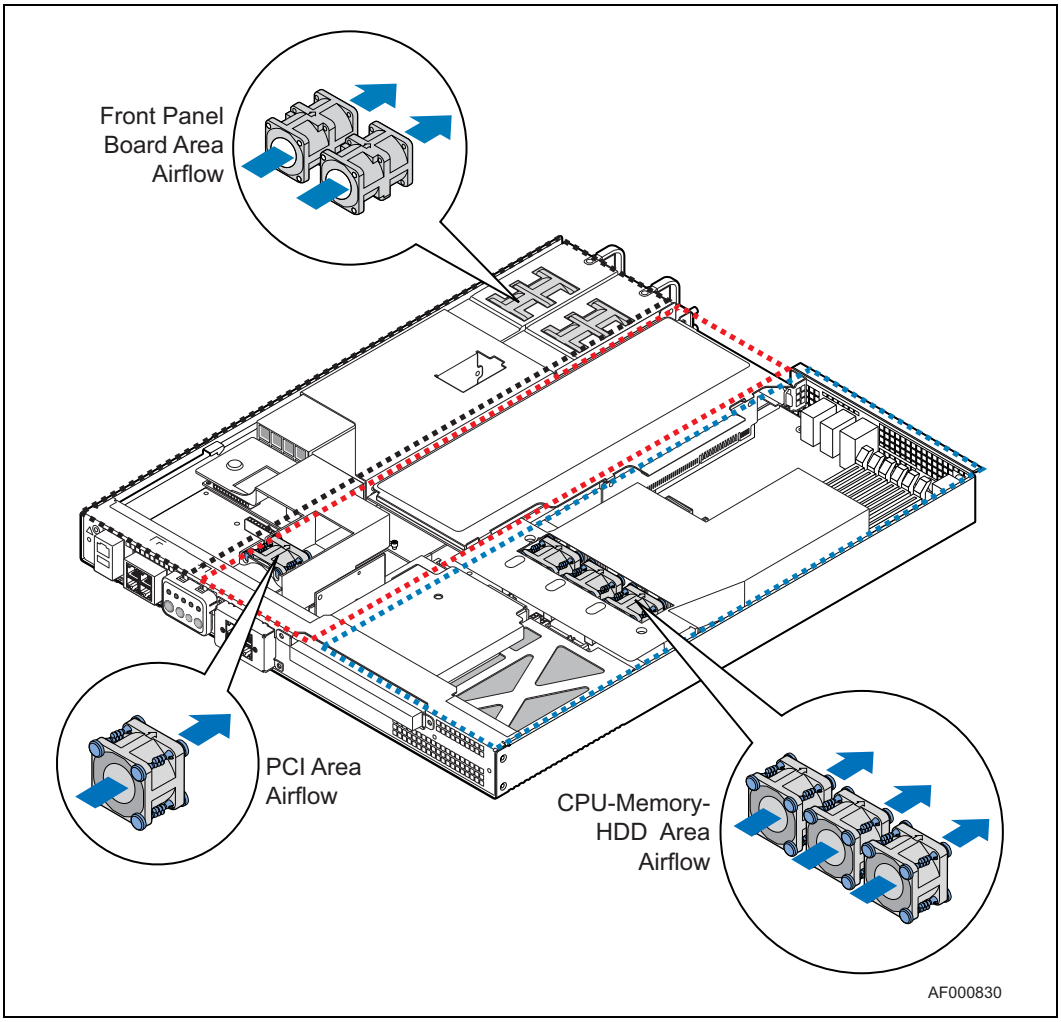


2.3.4 Cooling Subsystem

There are three cooling areas in the IP Network Server NSW1U system:

- Front panel board area
- PCI area
- CPU/memory/HDD area

Figure 20. IP Network Server NSW1U System Cooling Areas



2.3.4.1 Front Panel Board Cooling Area

The left one-fourth of the front panel board and the portion of the PDB in this area as shown in Figure 20 are cooled by the 40 × 40 × 56 mm dual-rotor fans in the PSU modules. One PSU is sufficient to cool this portion of the front panel board area and two PSUs provide cooling redundancy for this area.

The PSU fans draw air in through the bezel from the front of the system and from vents in the left front side of the chassis over this portion of the front panel board and PDB, through the PSU and exhausting out the rear of each PSU. The left wall of the PCI fan air duct and the PSU guide wall provide an air flow barrier between the front panel board cooling area and the PCI cooling area

2.3.4.2 PCI Cooling Area

The 40 × 40 × 28 mm single-rotor PCI fan cools the portions of the server board, PDB, and front-panel board that are in this area as shown in Figure 20, as well as any PCI or PCI Express adapter card installed in the riser card.

The PCI fan draws in air through the front beze The air is exhausted out the rear of the system. A plastic air duct:

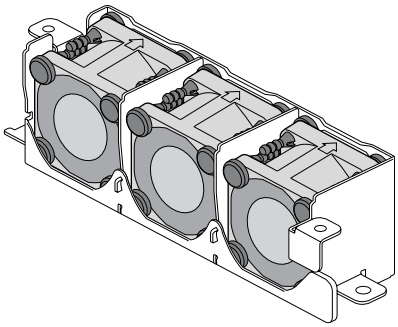
- Directs the air flow in this area.
- Houses the PCI fan.
- Provides air flow barriers between:
  - — The front panel board and the PCI cooling areas.
  - — The PCI and the CPU-memory-HDD cooling areas.

A second plastic part located behind the PCI air duct continues the air flow barrier between the PCI cooling area and the CPU/memory/HDD cooling area. The riser card provides the third and final portion of the air flow barrier between the PCI cooling area and the CPU/memory/HDD cooling area.

2.3.4.3 CPU/Memory/HDD Cooling Area

The system uses three 40 × 40 ×2 8 mm single rotor fans that are assembled to a sheet metal bracket as shown in Figure 21.

Figure 21. CPU/Memory/HDD Cooling Area Fan Assembly



Air is drawn in through the bezel from the front of the system and exhausted out the rear of the chassis. PCI air ducts and riser card isolate the CPU/memory/HDD cooling area air flow path from the rest of the system. Air entering the CPU/memory air duct is preheated by the hard drives.

2.3.4.4 Fan Speed Control

The Server Board S5000PHB contains three pulse width modulation (PWM) circuits that provide duty cycle-controlled PWM signals to the system fans in three separate domains. The PSU fans are not controlled by the system:

- PWM 1 controls the memory area fan.
- PWM 2 controls the CPU fans.
- PWM 3 controls the PCI cooling area fan.

See Figure 22.

The fan speeds are set per Table 3 based on ambient temperature feedback from the front panel board, and server board (PCI area) sensors. If the processors reach their throttling temperature the fans will ramp to higher speeds. If a system fan fails, then all of the remaining system fans will be set for maximum speed.

Figure 22. IP Network Server NSW1U Fan PWM Domains

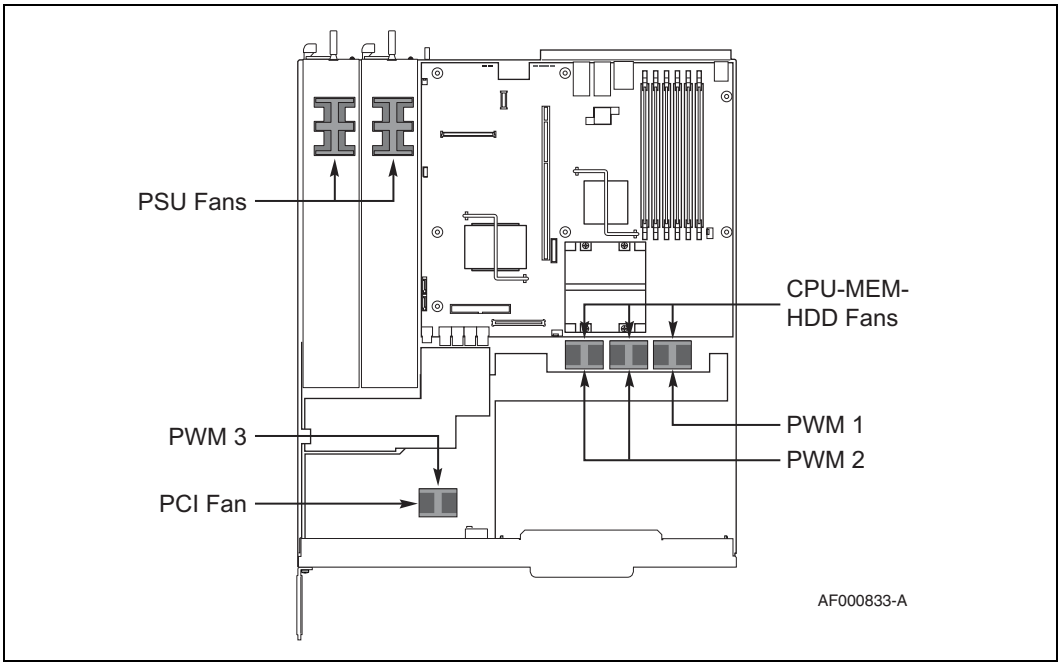


Table 3. Fan Speed Settings

Temperature	PCI Area Fan PWM Duty Cycle	CPU Area Fan PWM Duty Cycle	Mem Area Fan PWM Duty Cycle
0° C to 23° C	55%	55%	55%
24° C	56%	56%	56%
25° C	57%	57%	57%
26° C	58%	58%	58%
27° C	59%	59%	59%
28° C	60%	60%	60%
29° C	62%	62%	62%
30° C	66%	66%	66%

Table 3. Fan Speed Settings (Continued)

Temperature	PCI Area Fan PWM Duty Cycle	CPU Area Fan PWM Duty Cycle	Mem Area Fan PWM Duty Cycle
31° C	71%	71%	71%
32° C	77%	77%	77%
33° C	84%	84%	84%
34° C	92%	92%	92%
35° C	100%	100%	100%

2.3.4.5 Cooling Summary

The cooling subsystem provides cooling for:

- One processor
- 24 Gbytes of 667 MHz DRx8 FBD memory
- Two 10,000 RPM SATA 3.5-inch hard drives at a maximum of 18 W per drive
- One PCI, PCI-X, or PCI Express card at a maximum of 25 W

The cooling subsystem meets acoustic and thermal requirements at the lower fan speed settings. At the higher fan speed settings, thermal requirements are met for the maximum ambient temperatures, but acoustic requirements are not met. The environmental specifications are summarized in Section 2.5.1, "Environmental Specifications".

2.4 Server Management

See the *Intel® Server Board S5000PHB Technical Product Specification* and the Bensley Core (ESB2) EPS for a detailed description of the Server Management design and features.

The server management sub-system consists of a micro-controller, communication buses, sensors, system BIOS, and server management firmware. The baseboard management controller (BMC) component of the ESB2-E provides standard on-board platform instrumentation.

Table 4 summarizes the supported features:

Table 4. Server Management Features

Element	Supported?
IPMI Messaging, Commands, and Abstractions	Yes
Baseboard Management Controller (BMC)	Yes
Sensors	Yes
Sensor Data Records (SDRs) and SDR Repository	Yes
FRU Information	Yes
Autonomous Event Logging	Yes
System Event Log (SEL)	3276 Entries
BMC Watchdog Timer, covering BIOS and run-time software	Yes
IPMI Channels, and Sessions	Yes
† Requires optional Remote Management Module 2 (Intel® RMM2)	

Table 4. Server Management Features (Continued)

Element	Supported?
EMP (Emergency Management Port) - IPMI Messaging over Serial/Modem. This feature is also referred to as DPC (Direct Platform Control) over serial/modem.	Yes
Serial/Modem Paging	Yes
Serial/Modem Alerting over PPP using the Platform Event Trap (PET) format	Yes
DPC (Direct Platform Control) - IPMI Messaging over LAN (available via both on-board network controllers) Available over dedicated management port (ESB2 NIC 1)	Yes
LAN Alerting using PET	Yes
Platform Event Filtering (PEF)	Yes
ICMB (Intelligent Chassis Management Bus) - IPMI Messaging between chassis	Yes
PCI SMBus support	Yes
Fault Resilient Booting	Yes
BIOS logging of POST progress and POST errors	Yes
Integration with BIOS console redirection via IPMI v2.0 Serial Port Sharing	Yes
Access via web browser	No †
SNMP access	Yes
Telnet access	No
DNS support	Yes
DHCP support (dedicated NIC only)	Yes
Memory Sparing/Mirroring sensor support * does not support mirroring	Yes/No*
Alerting via Email	Yes
Keyboard, Video, Mouse (KVM) redirection via LAN	No †
High speed access to dedicated NIC	Yes
† Requires optional Remote Management Module 2 (Intel® RMM2)	

2.5 Specifications

2.5.1 Environmental Specifications

The system is tested to the environmental specifications indicated in Table 5. All testing is performed per procedures defined in *Bellcore GR-63-CORE NEBS Physical Protection*, *Bellcore GR-1089-CORE EMC and Electrical Safety — Generic Criteria for Network Telecommunications Equipment*, and the *Intel Environmental Standards Handbook*.

Table 5. Environmental Specifications Summary

Environment	Specification
Temperature, operating	+10° C to +35° C (+50° F to +95° F)
Temperature, non-operating	-40° C to +70° C (-104° F to +158° F)
Altitude	0 to 900m (2,950 ft.) @ 35° C, temperature derated by 1° C for each additional 300m (985 ft.)
Humidity, non-operating	95%, non-condensing at temperatures of 23° C (73° F) to 40° C (104° F)
Vibration, operating	Swept sine survey at an acceleration amplitude of 0.1 G from 5 to 100 Hz and back to 5 Hz at a rate of 0.1 octave/minute, 90 minutes per axis on all three axes as per Bellcore GR-63-CORE standards

Table 5. Environmental Specifications Summary (Continued)

Environment	Specification
Vibration, non-operating	Swept sine survey at an acceleration amplitude of 0.5 G from 5 to 50 Hz at a rate of 0.1 octaves/minute, and an acceleration amplitude of 3.0 G from 50 to 500 Hz at a rate of 0.25 octaves/minute, on all three axes as per Bellcore GR-63-CORE standard. 2.2 Grms, 10 minutes per axis on all three axes as per the *Intel Environmental Standards Handbook*
Shock, operating	Half-sine 2 G, 11 ms pulse, 100 pulses in each direction, on each of the three axes as per the *Intel Environmental Standards Handbook*
Shock, non-operating	Trapezoidal, 25 G, 170 inches/sec delta V, three drops in each direction, on each of the three axes as per *Intel Environmental Standards Handbook*
Acoustic	Sound power: ≤ 7 bels at ambient temperatures <24° C measured at bystander positions in operating mode
System Cooling Requirement	1200 BTU/hr with single power supply unit 1250 BTU/hr with dual power supply units
RoHS	Complies with RoHS Directive 2002/95/EC

2.5.2 Physical Specifications

Table 6 provides the physical dimensions of the IP Network Server NSW1U system.

Table 6. Physical Dimensions

Height	1.70 inches (43.2 mm)
Width	16.93 inches (430.0 mm)
Depth	20.0 inches (508 mm)
Front clearance	2.0 inches (76 mm)
Side clearance	1.0 inches (25 mm)
Rear clearance	3.6 inches (92 mm)

3.0 Cables and Connectors

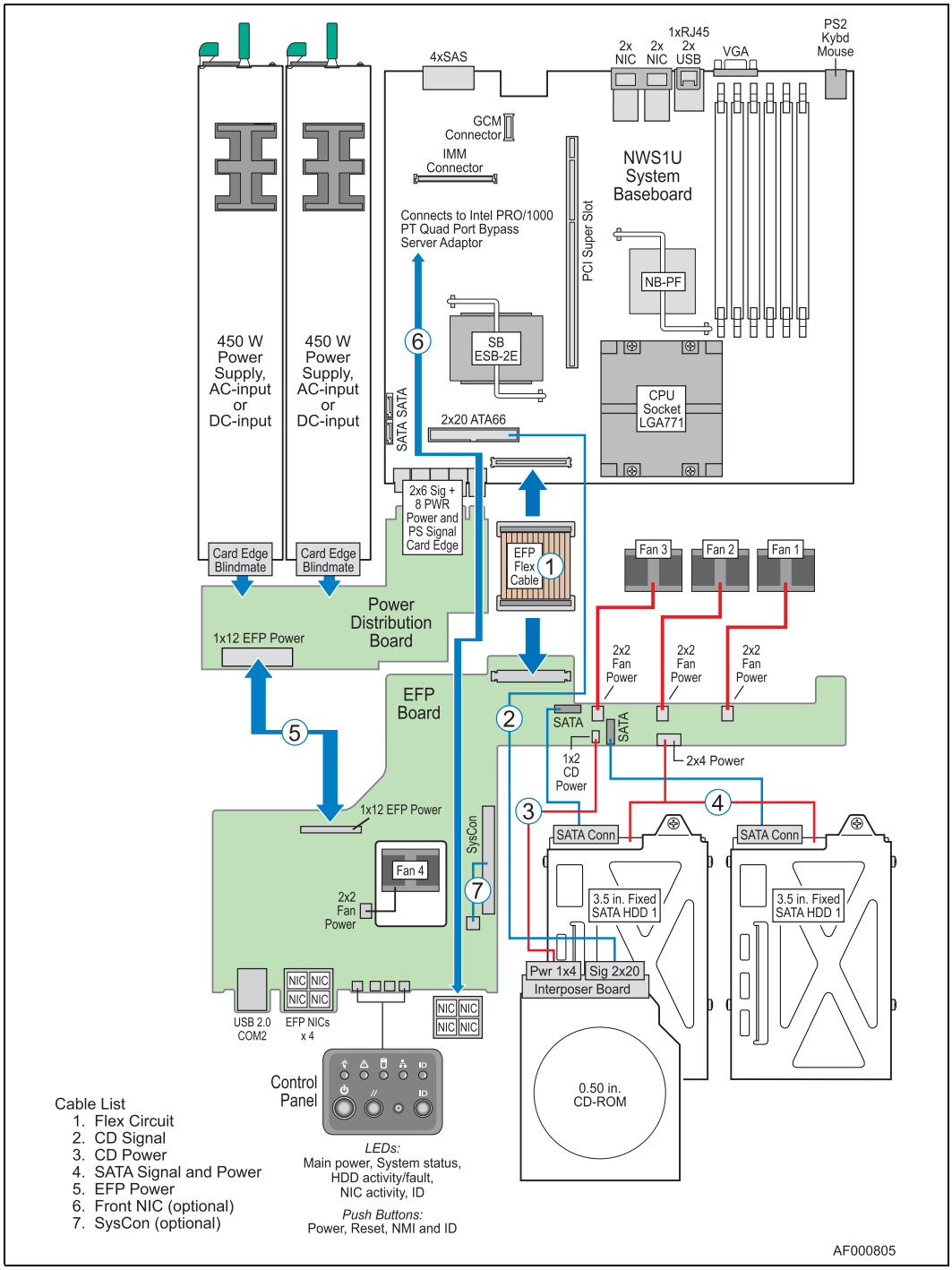
This chapter describes interconnections between the components of the Intel® IP Network Server NSW1U and provides overview diagrams and tables to describe the signals and pin-outs for the system connectors. See the *Intel® Server Board S5000PHB Technical Product Specification* for connector signal descriptions and pin-outs not listed in this section.

The information in this chapter is organized into the following sections:

- System Interconnect Block Diagram
- Cable and System Interconnect Descriptions
- User-Accessible Interface Connections

3.1 System Interconnect Block Diagram

Figure 23. Interconnect Block Diagram



Note: In the NSW1U-Bypass configurations only, Cable #5 in Figure 23 is permanently connected to the power distribution board.

3.2 Cable and System Interconnect Descriptions

3.2.1 Flex Circuit

The flex circuit is an impedance-controlled flexible circuit with 140 signal connections which interconnects the EFP to the server board.

This cable routes all of the signals between the server board and the SFP board including:

- All of the front panel I/O signals
- The SATA signals routed from the server board to the EFP board in support the SATA drives.

Figure 24. Flex Circuit Cable Connection

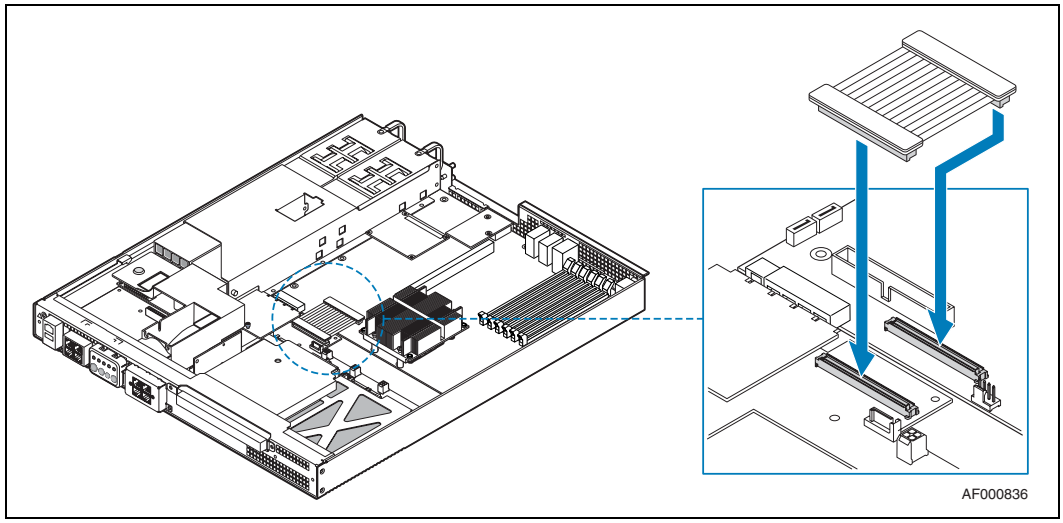


Table 7 lists the pin-out for the front panel flex connector to the server board.

Table 7. EFP Board Flex Cable Pin-out (Sheet 1 of 5)

Pin #	EFP Signal Name	Baseboard Signal Name
1	FP_FLEX_PRES2	FLEX_PRES2
2	SYSCON_USB_P	USB_P3P
3	ESB_SMBCLK3	SMB_CLK
4	SYSCON_USB_N	USB_P3N
5	ESB_SMBDAT3	SMB_DATA
6	GND	GND
7	FP_USB_FLT_N	OC_N[3]
8	DNW_NIC_SRC_P	CLK_100M_PCIE_P
9	GND	GND
10	DNW_NIC_SRC_N	CLK_100M_PCIE_N
11	EXP4_MCH_TX3_N	PCIE2_TX3_N
12	TP_FLEX_SPARE5	NC

Table 7. EFP Board Flex Cable Pin-out (Sheet 2 of 5)

Pin #	EFP Signal Name	Baseboard Signal Name
13	EXP4_MCH_TX3_P	PCIE2_TX3_P
14	GND	GND
15	HDD_ACT_N	DU_HD_LED
16	EXP4_MCH_RX3_N	PCIE2_RX3_N
17	GND	GND
18	EXP4_MCH_RX3_P	PCIE2_RX3_P
19	EXP4_MCH_TX2_N	PCIE2_TX2_N
20	HDD_FLT	DU_LED4
21	EXP4_MCH_TX2_P	PCIE2_TX2_P
22	GND	GND
23	LED_STATUS_GREEN_N	DU_LED2
24	EXP4_MCH_RX2_N	PCIE2_RX2_N
25	GND	GND
26	EXP4_MCH_RX2_P	PCIE2_RX2_P
27	EXP4_MCH_TX1_N	PCIE2_TX1_N
28	TP_TELCO_LED_SELECT	TELCO_LED_SELECT
29	EXP4_MCH_TX1_P	PCIE2_TX1_P
30	GND	GND
31	LED_STATUS_RED_N	DU_LED3
32	EXP4_MCH_RX1_N	PCIE2_RX1_N
33	GND	GND
34	EXP4_MCH_RX1_P	PCIE2_RX1_P
35	EXP4_MCH_TX0_N	PCIE2_TX0_N
36	FP_PWR_EN	PWR_ENABLE
37	EXP4_MCH_TX0_P	PCIE2_TX0_P
38	GND	GND
39	FP_PWR_GOOD	FP_PWR_GOOD
40	EXP4_MCH_RX0_N	PCIE2_RX0_N
41	GND	GND
42	EXP4_MCH_RX0_P	PCIE2_RX0_P
43	TP_EXP2_ESB_TX3_C_N	PCIE1_TX3_N
44	FP_NIC_ACT_LED_N	NIC_ACT_LED_N
45	TP_EXP2_ESB_TX3_C_P	PCIE1_TX3_P
46	GND	GND
47	FP_PWR_LED_N	PWR_LED_N
48	TP_EXP2_ESB_RX3_C_P	PCIE1_RX3_N
49	GND	GND
50	TP_EXP2_ESB_RX3_C_N	PCIE1_RX3_P
51	TP_EXP2_ESB_TX2_C_N	PCIE1_TX2_N
52	FP_NMI_BTN_N	NMI_BTN_N

Table 7. EFP Board Flex Cable Pin-out (Sheet 3 of 5)

Pin #	EFP Signal Name	Baseboard Signal Name
53	TP_EXP2_ESB_TX2_C_P	PCIE1_TX2_P
54	GND	GND
55	FP_PWR_BTN_N	PWR_BTN_N
56	TP_EXP2_ESB_RX2_C_P	PCIE1_RX2_N
57	GND	GND
58	TP_EXP2_ESB_RX2_C_N	PCIE1_RX2_P
59	TP_EXP2_ESB_TX1_C_N	PCIE1_TX1_N
60	FP_RST_BTN_N	RST_BTN_N
61	TP_EXP2_ESB_TX1_C_P	PCIE1_TX1_P
62	GND	GND
63	FP_ID_BTN_N	ID_BTN_N
64	TP_EXP2_ESB_RX1_C_P	PCIE1_RX1_N
65	GND	GND
66	TP_EXP2_ESB_RX1_C_N	PCIE1_RX1_P
67	TP_EXP2_ESB_TX0_C_N	PCIE1_TX0_N
68	FP_ID_LED_N	ID_LED_BUF_N
69	TP_EXP2_ESB_TX0_C_P	PCIE1_TX0_P
70	GND	GND
71	FP_TEMP_PWM	TEMP_SENSOR
72	TP_EXP2_ESB_RX0_C_P	PCIE1_RX0_N
73	GND	GND
74	TP_EXP2_ESB_RX0_C_N	PCIE1_RX0_P
75	FP_USB_N	USB_P2N
76	GND	GND
77	FP_USB_P	USB_P2P
78	GND	GND
79	GND	GND
80	SYSCON_USB_FLT_N	USB_OC_N[2]
81	FAN1_CPU_TACH	FAN1_TACH
82	FAN2_CPU_TACH	FAN2_TACH
83	FAN3_CPU_TACH	FAN3_TACH
84	OPHIR_A_DIS_N	FAN4_TACH
85	TP_FAN5_CPU_TACH	FAN5_TACH
86	OPHIR_B_DIS_N	FAN6_TACH
87	FP_PE_WAKE_N	FAN7_TACH
88	TP_FAN8_TACH	FAN8_TACH
89	FAN9_PCI_TACH	FAN9_TACH
90	FAN_MEM_PWM1	FAN_CPU1_PWM
91	FAN9_PCI_PWM	FAN_PWM
92	FAN_CPU_PWM2	FAN_CPU2_PWM

Table 7. EFP Board Flex Cable Pin-out (Sheet 4 of 5)

Pin #	EFP Signal Name	Baseboard Signal Name
93	GND	GND
94	GND	GND
95	EMP_DTR_L	DTR2_N
96	EMP_INUSE_L	EMP_INUSE_L
97	EMP_RTS_L	RTS2_N
98	EMP_SOUT	SOUT2
99	EMP_SIN	SIN2
100	EMP_CTS_L	CTS2_N
101	EMP_DSR_L	DSR2_N
102	EMP_DCD_L	DCD2_N
103	GND	GND
104	GND	GND
105	FP_SATA_RX0_P	SAS_RX7_P
106	SYS_RESET_N	SYS_RESET_N
107	FP_SATA_RX0_N	SAS_RX7_N
108	GND	GND
109	TP_FLEX_SPARE2	RAID_MODE_R
110	FP_SATA_TX0_N	SAS_TX7_N
111	GND	GND
112	FP_SATA_TX0_P	SAS_TX7_P
113	FP_SATA_RX1_P	SAS_RX6_P
114	TP_FLEX_SPARE4	IBUTTON_PRES_N
115	FP_SATA_RX1_N	SAS_RX6_N
116	GND	GND
117	FAN_LED_SHIFT_CLK	SMB_SERIAL_CLK1
118	FP_SATA_TX1_N	SAS_TX6_N
119	GND	GND
120	FP_SATA_TX1_P	SAS_TX6_P
121	ESB_LAN_SETP1	SAS_TX4_P
122	FAN_LED_SHIFT_DATOUT	FAULT_LED_SHIFT_OUT
123	ESB_LAN_SETN1	SAS_TX4_N
124	GND	GND
125	FAN_LED_SHIFT_RST	RSM_RST_N
126	ESB_LAN_SERN1	SAS_RX4_N
127	GND	GND
128	ESB_LAN_SERP1	SAS_RX4_P
129	ESB_LAN_SERP0	SAS_RX5_P
130	TP_FAN_LED_SHIFT_DATIN	SAS_RAID_SPKR
131	ESB_LAN_SERN0	SAS_RX5_N
132	GND	GND

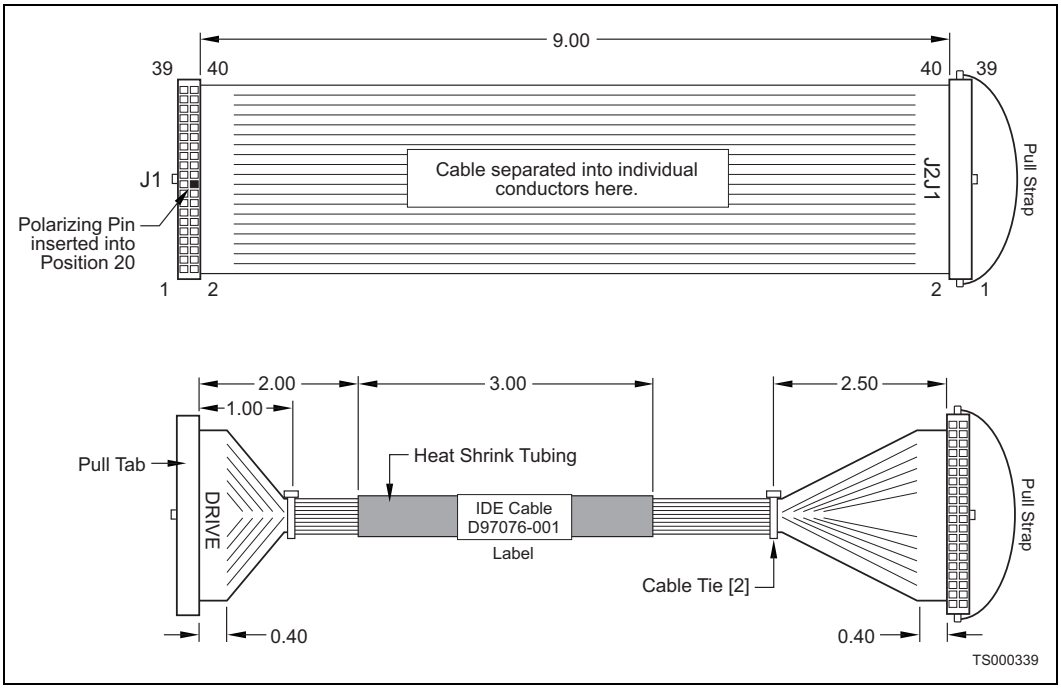
Table 7. EFP Board Flex Cable Pin-out (Sheet 5 of 5)

Pin #	EFP Signal Name	Baseboard Signal Name
133	TP_FLEX_SPARE3	SAS_DISABLE_N
134	ESB_LAN_SETN0	SAS_TX5_N
135	GND	GND
136	ESB_LAN_SETP0	SAS_TX5_P
137	P3V3_STBY	P3V3_STBY
138	GND	GND
139	P3V3_STBY	P3V3_STBY
140	FP_FLEX_PRES1_N	GND
MP1	GND	
MP2	GND	

3.2.2 IDE Signal Cable

The IDE signal cable is a standard 40-conductor (28 AWG) ribbon cable with 2×20 position, 0.050 inch centers connectors. This cable connects between the optical drive interposer board and connector J2J1 on the server baseboard. Figure 25 illustrates the physical details of the cable assembly. Dimensions are in inches.

Figure 25. IDE Signal Cable Physical Details



3.2.3 Optical Drive Power Cable

Figure 26 illustrates the physical details of the optical drive power cable assembly. Dimensions are in inches. This cable connects between the 4-pin power connector on the optical drive interposer board and a 2-pin power connector on the Ethernet front panel board.

Figure 26. Optical Drive Power Cable Physical Details

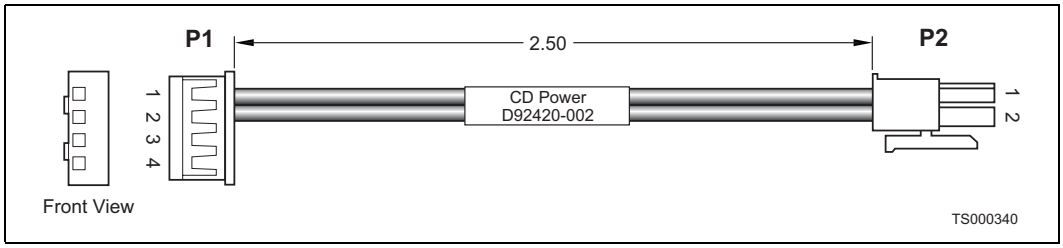


Table 8. Optical Drive Power 1×4 Connector Pin-Out

Drive-end Pin #	EFP-end Pin #	Signal
1	1	P5V
2	2	GND
3		
4		

3.2.4 Front Panel Board Power Cable

A 12-conductor, 20 AWG discrete-wire harness with 1×12 connectors is used to connect the Front Panel Board to supply voltages on the Power Distribution Board (PDB). For the NSW1U-Bypass configuration only, this wiring harness is permanently attached to the PDB. NSW1U-FNIC and NSW1U-RNIC configurations use a separate cable assembly as shown in Figure 27 (Dimensions are in inches). Table 9 describes the pin-out of the 1×12 connectors used on the EFP power harness.

Figure 27. Front Panel Board Power Cable Physical Details

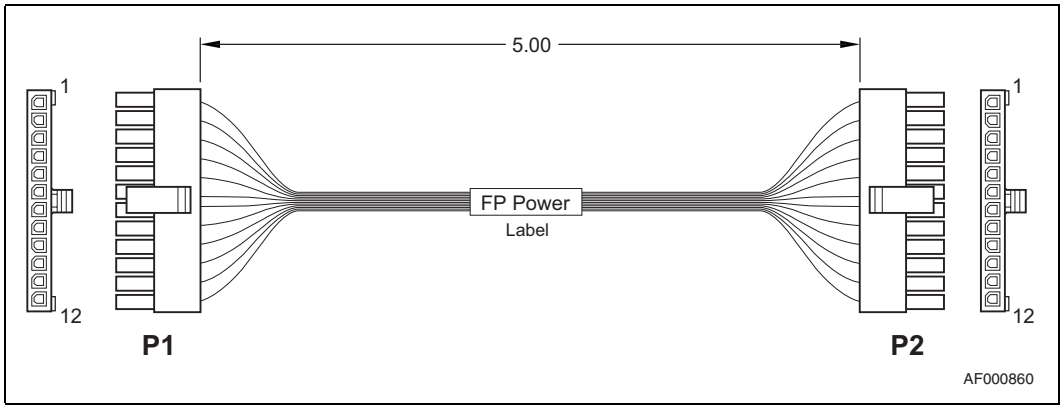


Table 9. Front Panel Board Power Cable Connector Pin-Out

Pin #	Signal
1	P3V3
2	P5V_STBY
3	GND
4	GND
5	P12V
6	P12V
7	P12V
8	GND
9	GND
10	P5V
11	P5V
12	GND

3.2.5 Intel® Z-U130 Value Solid State Drive Signal and Power Cable (Optional)

The optional Intel® Z-U130 Value Solid State Drive connects to the SFP board with a single signal and power cable. The physical details of this cable are shown in Figure 28 (all dimensions in inches), and the pin-out of the connectors is given in Table 10.

Figure 28. Intel® Z-U130 Value Solid State Drive Signal and Power Cable Physical Details

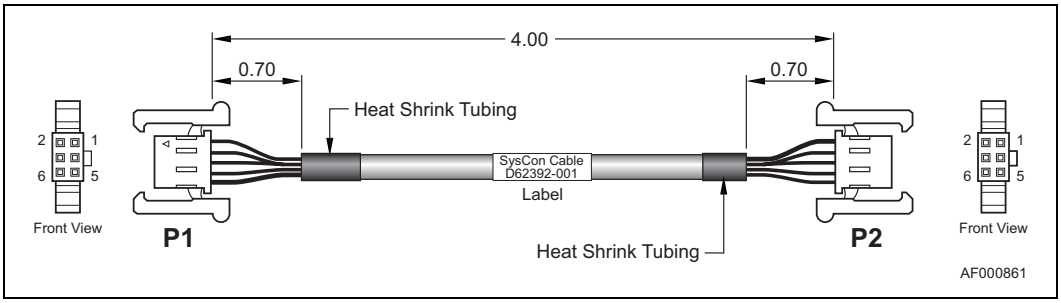


Table 10. Intel® Z-U130 Value Solid State Drive 2 x 3 Connector Pin-Out

Pin #	Signal
1	GND
2	Keyed (no connect)
3	SYSCON_USB_P
4	SYSCON_PWR
5	SYSCON_USB_N
6	GND

3.2.6 SATA Hard Drive Power and Signal Cable Assembly

Figure 29 illustrates the physical details of the cable assembly that provides signal and power connections between both SATA hard drives and the EFP board. The pin-outs of the SATA signal connectors and the power connector on the EFP end of the cable assembly are given in Table 11 and Table 12, respectively.

Figure 29. SATA Hard Drive Power and Signal Cable Physical Details

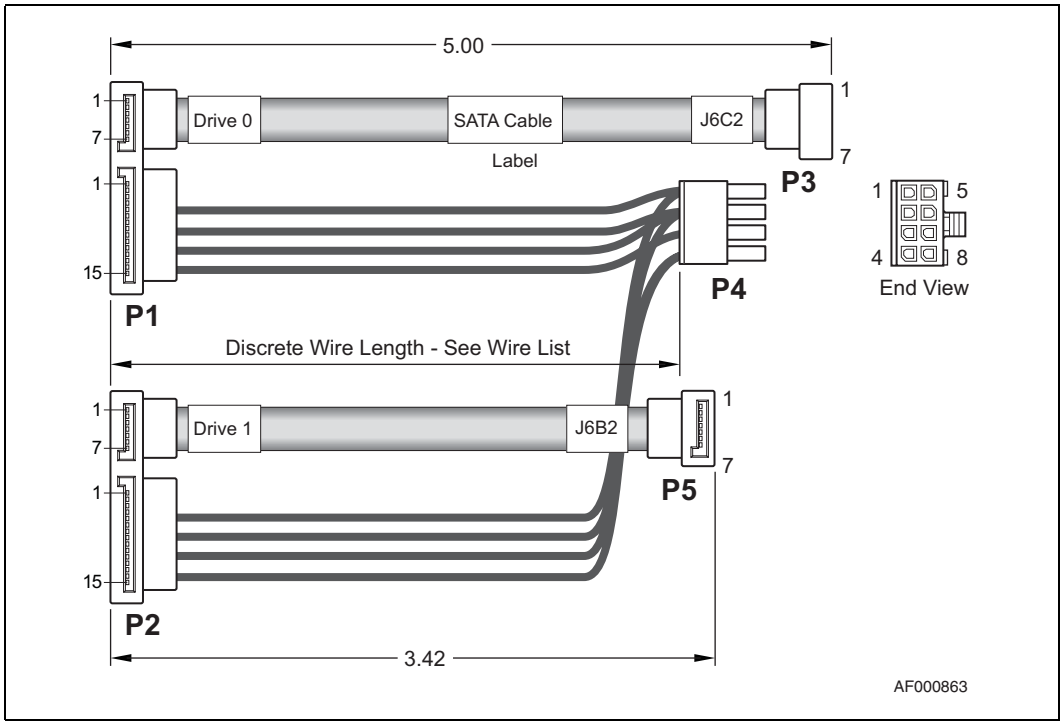


Table 11. SATA Hard Drive Signal Connector Pin-Out

Pin #	I/O	Signal Name	Description
1	PWR	GND	GND
2	O	FP_DATA_RX0(1)_P	Positive receive data to drive
3	O	FP_DATA_RX0(1)_N	Negative receive data to drive
4	PWR	GND	GND
5	I	FP_DATA_TX0(1)_N	Negative transmit data from drive
6	I	FP_DATA_TX0(1)_P	Positive transmit data from drive
7	PWR	GND	GND

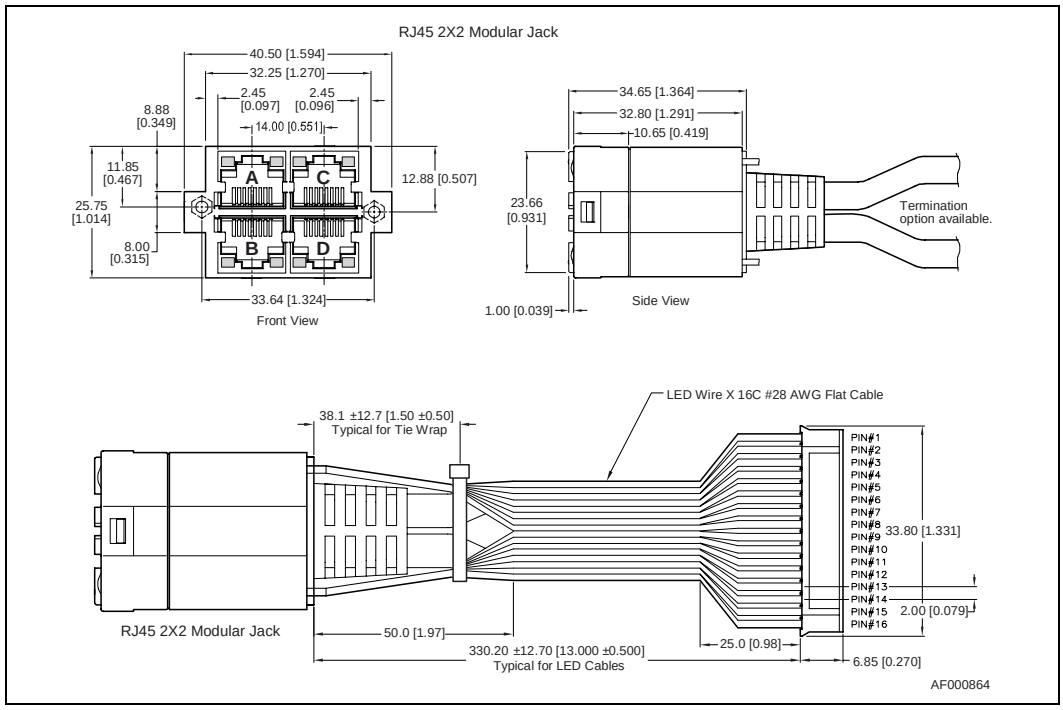
Table 12. SATA Hard Drive 2×4 Power Connector (P4) Pin-Out

Pin #	Signal
1	P5V
2	GND
3	P12V
4	GND
5	P5V
6	GND
7	P12V
8	GND

3.2.7 Front NIC 4x Ethernet PCI Card Cable (Optional)

This cable assembly is supplied as a component of the optional Intel PRO/1000 AT Quad-Port Bypass Adapter or Intel PRO/1000 AF Quad-Port Bypass Adapter. The cable provides four additional front-panel NIC connectors that may be installed in an IP Network Server NSW1U, and connects to the Quad-Port Bypass Adapter that is installed in the PCI super-slot riser.

Figure 30. Front NIC 4x Ethernet PCI Card Cable Physical Details



3.2.8 Fan Power Cables

All system fans in the IP Network Server NSW1U use the same type of wire harness assembly which terminate in 4-pin connectors that mate to connectors on the EFP board. The connector pin-out is shown in Table 13.

Table 13. Fan 2 x 2 Connector Pin-Out

Pin #	Signal
1	P12V
2	Fan Tachometer Signal
3	GND
4	Fan Speed Control

3.3 User-Accessible Interface Connections

3.3.1 Keyboard and Mouse Ports

Two stacked PS/2 ports support both a keyboard and a mouse. Each port can support either a mouse or keyboard. Table 14 details the pin-out of the PS/2 connector.

Figure 31. Keyboard and Mouse Connectors

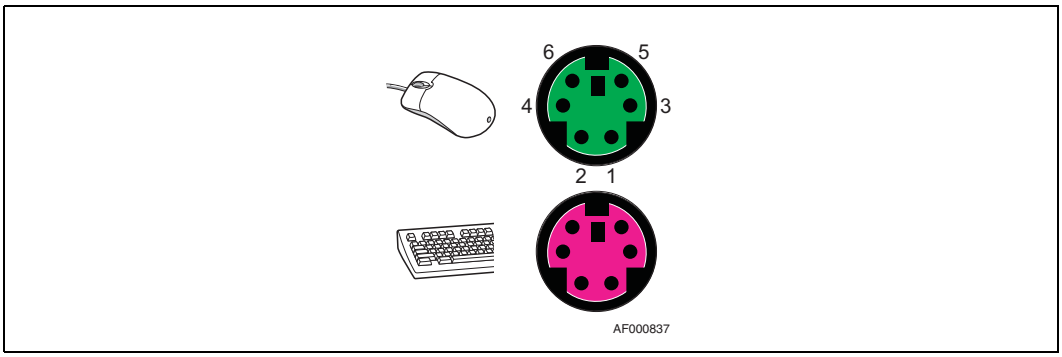


Table 14. Keyboard and Mouse Port Pin-Out

Pin #	Signal
1	KEYDAT (keyboard data)
2	MSEDAT (mouse data)
3	GND (ground)
4	Fused Vcc (+5V)
5	KEYCLK (keyboard clock)
6	MSECLK (mouse clock)

3.3.2 Serial Port B

Two serial port connectors (Serial B) are provided, one on the front panel and one at the rear I/O panel, both using 8-pin RJ45 connectors. An RJ45 connector allows connection to serial port concentrators. For applications that require a DB-9 serial port connection, an adapter cable must be used.

Both the front and rear serial port connectors connect to COM2. Users can connect to either the front or the rear serial port connector, but should *never* connect to *both* connectors at the same time.

The connector pin-out differs slightly between the front-panel and rear-panel connectors, specifically in relation to Pin 6 and Pin 7. On the front-panel serial port connector, Pin 6 is used as a serial port selection input. Grounding the EMP_INUSE_L signal that appears on Pin 6 disables the rear-panel serial port connection so that only the front-panel connection is active. This allows users to plug into and use the front-panel connector without regard for whether anything is connected to the rear-panel connector. The front-panel serial port connector always carries the DSR signal on Pin 7.

On the rear-panel serial port connector, a server board jumper configures Pin 7 to carry either the DSR (Data Set Ready) signal or the DCD (Data Carrier Detect) signal as required by a particular serial port concentrator. The default jumper setting selects the DSR signal, which conforms to the Cisco* serial port standard. See the *Intel® Server Board S5000PHB Technical Product Specification* for details about this jumper or if you need to change the DSR/DCD configuration.

Figure 32. Serial B Port Connector

Table 15. Front-Panel Serial Port B (RJ45) Connector Pin-out

Pin #	EFP Board Signal Name	Description
1	SPB_EMP_RTS_L	RTS (Request To Send)
2	SPB_EMP_DTR_L	DTR (Data Terminal Ready)
3	SPB_EMP_SOUT	TXD (Transmit Data, serial data out)
4	GND	Ground
5	EMP_INUSE_L	When grounded, disables rear-panel serial port
6	SPB_EMP_SIN	RXD (Receive Data, serial data in)
7	SPB_EMP_DSR_L	DSR (Data Set Ready)
8	SPB_EMP_CTS_L	CTS (Clear To Send)

Table 16. Rear-Panel Serial B Port (RJ45) Connector Pin-Out

Pin #	Signal
1	RTS (Request To Send)
2	DTR (Data Terminal Ready)
3	TXD (Transmit Data)
4	GND
5	RIA (Ring Indicator)
6	RXD (Receive Data)
7	Configurable (using jumper J2A2 on system board) to carry either: • DSR (Data Set Ready) [default, Cisco port concentrator compatible] • DCD (Data Carrier Detect)
8	CTS (clear to send)

For server applications that require a DB9 serial connector, an 8-pin RJ45-to-DB9 adapter must be used. The following table provides the pin-out required for the adapter to provide RS-232 support.

Table 17. RJ-45-to-DB9 Adapter Pin Assignments

RJ45 Pin No.	Signal	Description	DB9 Pin No.
1	RTS	Request to Send	7
2	DTR	Data Terminal Ready	4
3	TD	Transmitted Data	3
4	SGND	Signal Ground	5
5	RI	Ring Indicator	9
6	RD	Received Data	2
7	DSR	Data Signal Ready	6 †
8	CTS	Clear To Send	8
†	When using the rear-panel Serial B port connector, the wiring of the RJ45-to-DB9 adapter should match the configuration of the RJ45 pin-out. If the port has been configured for the DCD rather than DSR on Pin 7, the adapter cable should connect Pin 1 of the DB9 rather than Pin 6.		

3.3.3 Video Port

The video port interface is a standard VGA compatible, 15-pin connector. On-board video is supplied by an ATI* Rage XL video controller with 8 MB of on-board video SGRAM.

Figure 33. Video Connector

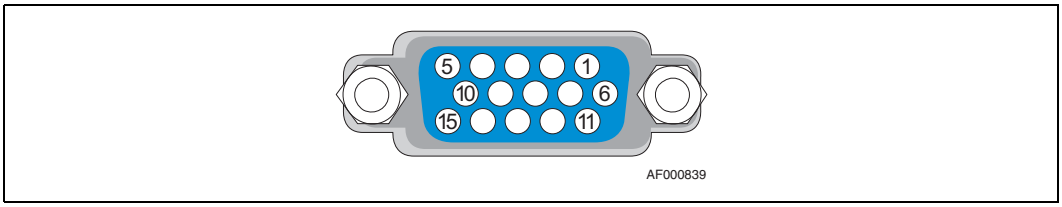


Table 18. Video Connector Pin-Out (Sheet 1 of 2)

Pin #	Signal
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND
6	GND
7	GND
8	GND
9	Fused Vcc (+5V)
10	GND
11	No connection
12	DDCDAT

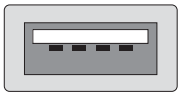
Table 18. Video Connector Pin-Out (Sheet 2 of 2)

13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	DDCCLK

3.3.4 Universal Serial Bus (USB) Interface

The server board provides four USB ports. USB ports 0 and 1 are brought to the rear. USB ports 2 and 3 are routed to the front panel board where USB port 2 is brought to the front of the system and USB port 3 is used internally for interfacing to the optional Intel® Z-U130 Value Solid State Drive. The built-in external USB ports permit direct connection of three USB peripherals without an external hub. If more devices are required, an external hub can be connected to any of the built-in ports.

Figure 34. External USB Connector



AF000840

Table 19. USB Connector Pin-Out

Pin #	Signal
1	Fused Vcc (+5V w/over-current monitor of ports 0, 1, 2, and 3)
2	DATAL0 (differential data line paired with DATAH0)
3	DATAH0 (differential data line paired with DATAL0)
4	GND

3.3.5 Ethernet Connectors

The IP Network Server NSW1U provides either four or eight RJ45 Ethernet NIC connectors, with the location of the connectors differing between the three configurations of the server.

- On the NSW1U-RNIC, the four standard NIC connectors are located at the back edge of the Intel® Server Board S5000PHB and are accessible on the rear I/O panel; four additional rear-access connections can be implemented using an Intel PRO/1000 AT Quad Port Bypass Adapter (for copper connectivity) or an Intel PRO/1000 AF Quad Port Bypass Adapter for fiber connectivity).
- On the NSW1U-FNIC configuration, four standard NIC connectors are located on the EFP board and are accessible on the server's front panel; four optional connectors may be installed near the center of the front panel with the installation of an Intel PRO/1000 AT Quad Port Bypass Adapter (for copper connectivity) or an Intel PRO/1000 AF Quad Port Bypass Adapter for fiber connectivity) in the PCI Express riser card.
- On the NSW1U-Bypass, four connectors are located on the Intel® Server Board S5000PHB and area accessible on the server's rear panel exactly as in the NSW1U-R configuration, and four connectors are provided on the front panel in the same location as the standard connectors of the NSW1U-F configuration. Four additional ports can be added to either the front panel or rear panel through the installation of an Intel PRO/1000 AT Quad Port Bypass Adapter (for copper

connectivity) or an Intel PRO/1000 AF Quad Port Bypass Adapter for fiber connectivity).

The Ethernet connectors appear as stacked pairs as illustrated in Figure 35. The pin-out of each connector is identical and is defined in Table 20.

Figure 35. Stacked Ethernet Connector Pair

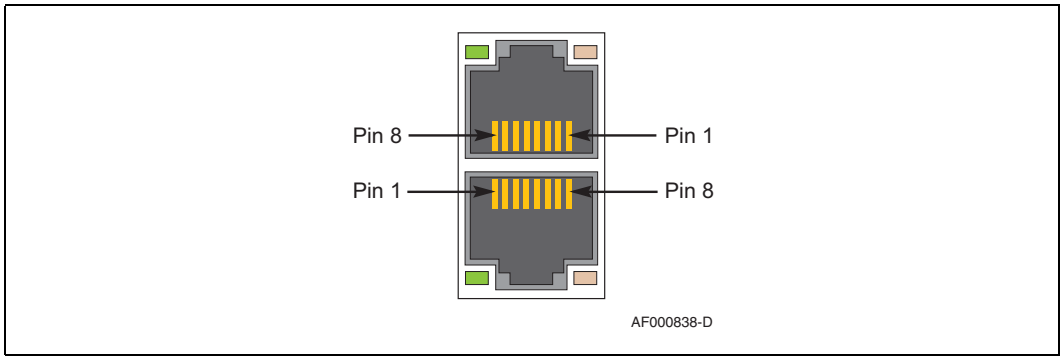


Table 20. Ethernet Connector Pin-Out

Pin #	Signal Name	Description
1	BI_DA+	Bi-directional pair A, +
2	BI_DA–	Bi-directional pair A, –
3	BI_DB+	Bi-directional pair B, +
4	BI_DC+	Bi-directional pair C, +
5	BI_DC–	Bi-directional pair C, –
6	BI_DB–	Bi-directional pair B, –
7	BI_DD+	Bi-directional pair D, +
8	BI_DD–	Bi-directional pair D, –

For each Ethernet connector there are two status indicator LEDs integrated into the connector assembly, a green LED to the left of the connector and a bi-color LED to the right of the connector.

The green LED indicates the connection status for each port. If the port is connected to a network but there is no current activity, the green LED is continuously illuminated. When there is activity on the connected network the green LED blinks.

The bi-color LED indicates the connection speed. If the green LED indicates a network connection but the bi-color LED is not lit, then the connection speed is 10 Mbps. If the bi-color LED shows a solid green indication, then the connection speed is 100 Mbps. If the bi-color LED is solid amber, then the connection speed is 1 Gbps.

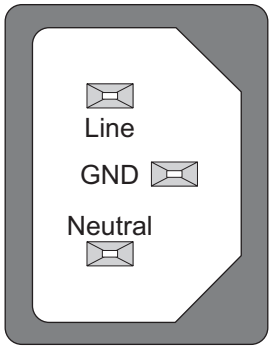
3.3.6 GCM Remote Management Module Connector

The IP Network Server NSW1U supports the installation of an optional Intel® Remote Management Module 2, which provides a 1000 Mbps Ethernet interface through a GCM connector module. The connector outline, pin-out, and LED indications for the GCM connector are the same as for the server's standard Ethernet connectors, as described above.

3.3.7 AC Power Input for AC-Input Power Supply

An IEC320-C13 receptacle is at the rear of each AC-input power module. An appropriately sized power cord and AC main is recommended. See Chapter 8.0, "AC Power Subsystem", for system voltage, frequency, and current draw specifications.

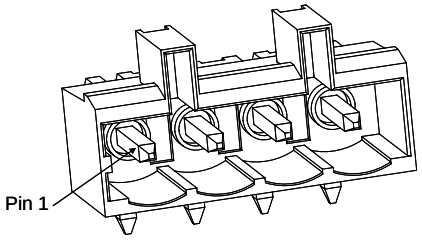
Figure 36. AC Power Input Connector



3.3.8 DC Power Input for DC-Input Power Supply

A Molex* MTC 4-pin DC connector (Molex p/n 55757-0420 or an equivalent) is used in the DC power supply modules to provide the DC-input power connection. The required mating connector is a Molex 54927-0420 or equivalent. Use an appropriately-sized power wire and DC main. See Chapter 9.0, "DC Power Subsystem" for system DC voltage and current draw specifications.

Figure 37. DC Power Input Connector



The pin-out of the DC input connector is in Table 21.

Table 21. DC Power Supply Module Input Pin Assignments

Pin#	Description
1	RTN
2	RTN
3	–48V
4	-48V

4.0 Ethernet Front Panel (EFP) Board

This chapter describes the basic functions and interface requirements of the Ethernet front panel (EFP) system board for the Intel® IP Network Server NSW1U.

The information contained in this chapter is organized into the following sections:

4.1 Features

- Four switches to control power-on, reset, NMI, and the system ID
- One RS-232 front panel port
- One USB 2.0 front panel port
- One USB 2.0 interface to the optional Intel® Z-U130 Value Solid State Drive
- Four fan connectors to provide power, control, and monitoring of the three CPU fans and one PCI fan
- One power connector for the optical drive port
- Two power connectors for the two SATA drives
- One system ID LED that can be controlled remotely or by the system ID switch
- Two system activity LEDs that indicate power-on and NIC activity
- One system status LED to indicate system health status
- One hard drive activity LED that provides an OR'ed indication for both SATA drives

4.2 Introduction

The Ethernet front panel (EFP) board has three variant assemblies that support various functions through use of component population/depopulation options. The primary differences for each variation of the EFP can be summarized as follows:

- Both dual-Ethernet controllers depopulated (EFPR board for NSW1U-RNIC server variant)
- Two dual-Ethernet controllers populated with ports accessible at the server front panel (EFPF board for NSW1U-FNIC server variant)

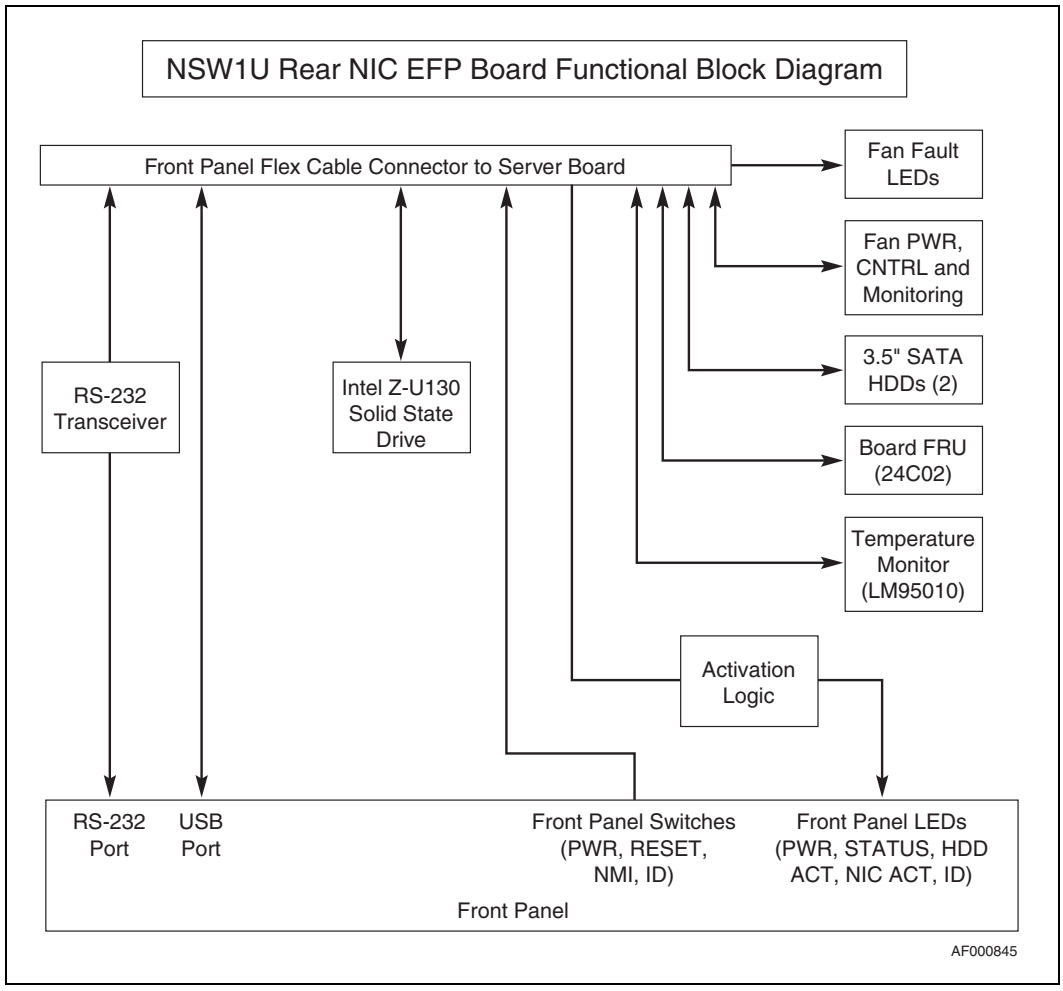
- Two dual-Ethernet controllers populated with ports accessible at the front panel, with the added capability to bypass the on-board Ethernet controllers during a system power failure (EFPB board for NSW1U-Bypass server variant)

In addition to the above features, all versions of the EFP system board provide switches and indicators that are accessible from the front panel to control system operation and monitor system status. The EFP board contains connectors to provide power to the optical drive, SATA drives, system cooling fans, and optional Intel® Z-U130 Value Solid State Drive, and signal interfaces to support both SATA drives, a front-panel USB port, a front-panel RJ45 serial port, and the Intel® Z-U130 Value Solid State Drive.

The following figures present functional block diagrams of the each of the different EFP board variants.

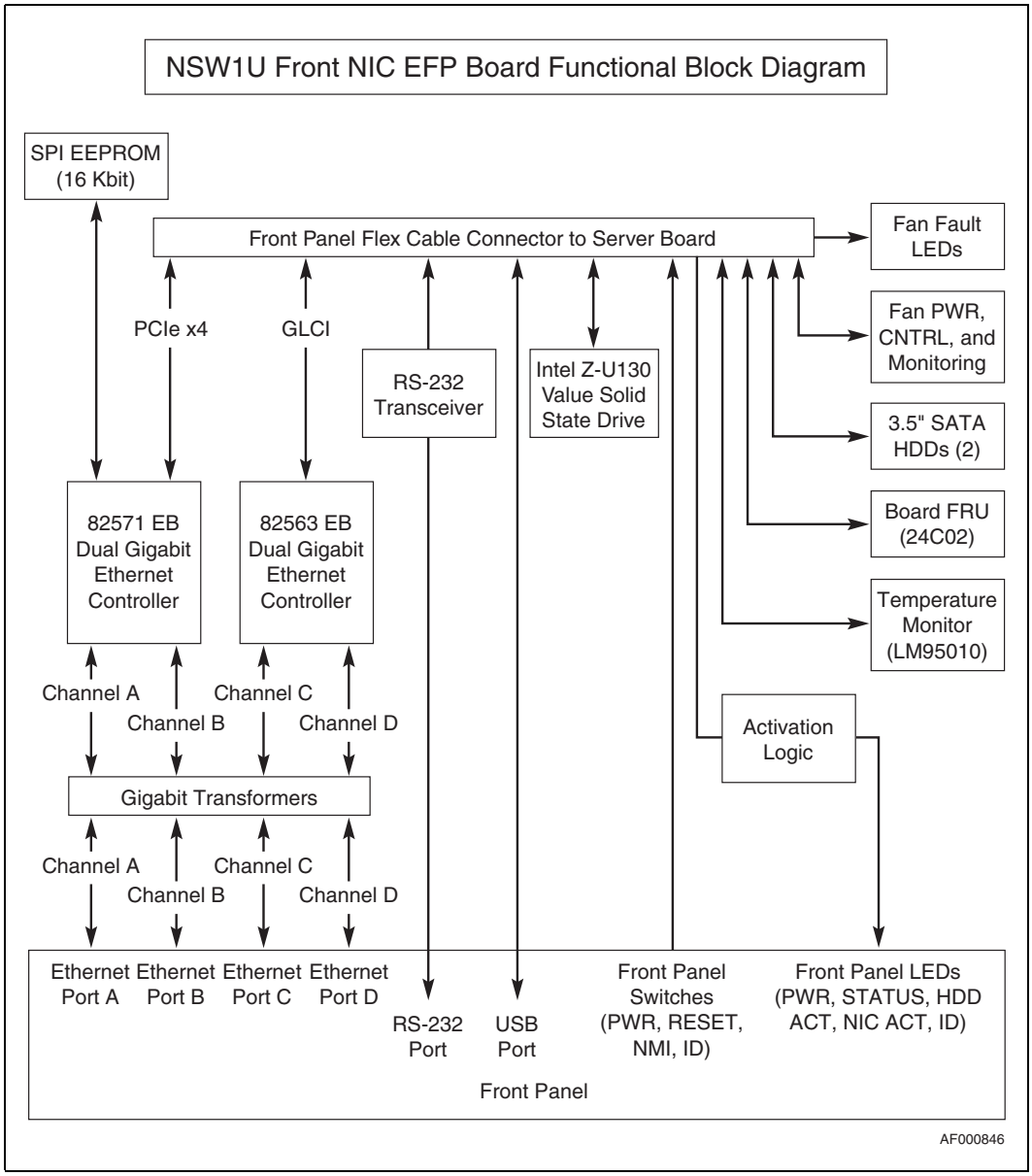
A block diagram of the EFPR board is shown in Figure 38.

Figure 38. IP Network Server NWS1U System EFPR Board Block Diagram



A block diagram of the EFPF system board is shown in Figure 39.

Figure 39. IP Network Server NSW1U System EFPF Board Block Diagram



A block diagram of the EFPB is shown in Figure 40.

Figure 40. IP Network Server NSW1U System EFPB Board Block Diagram

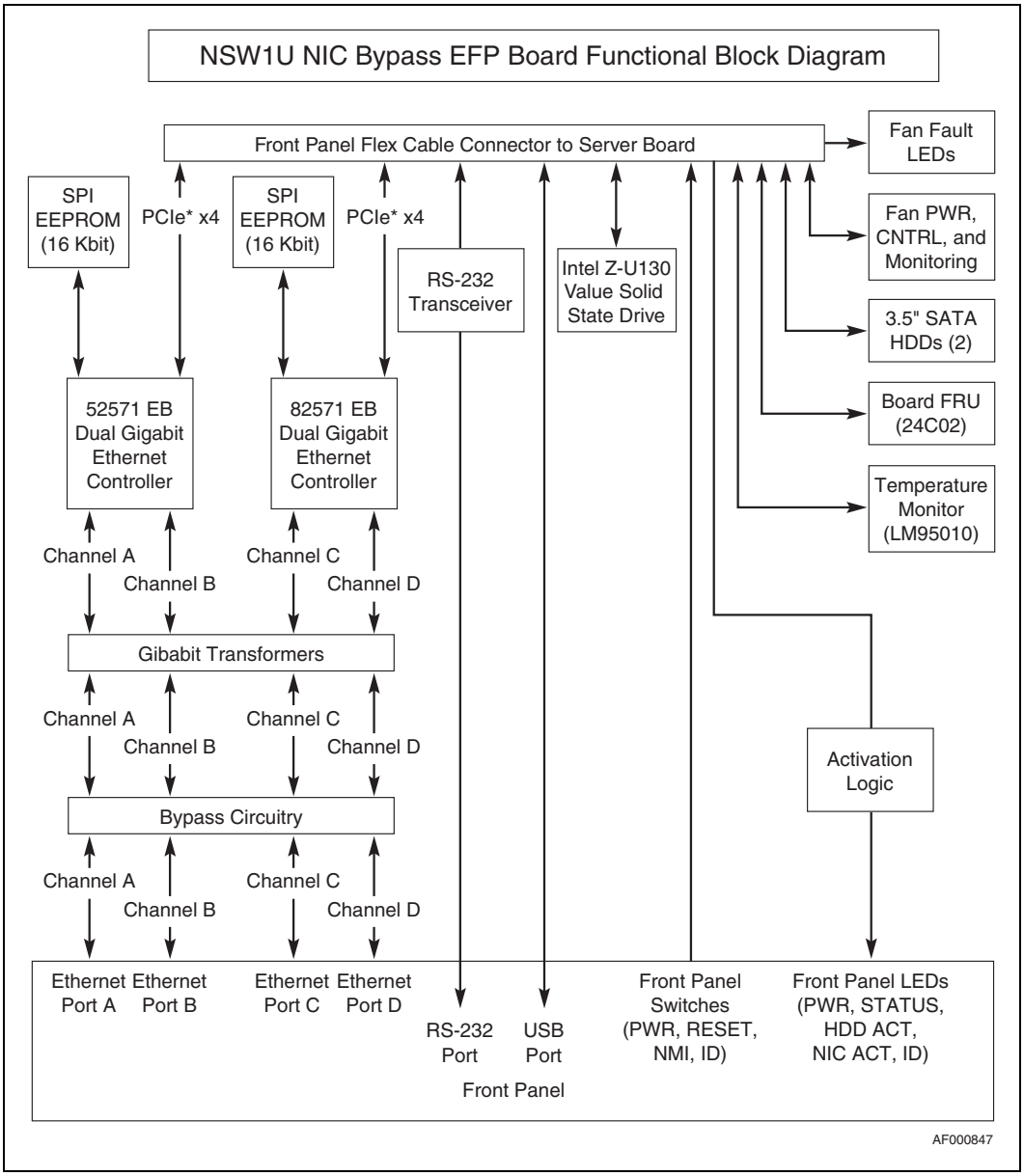
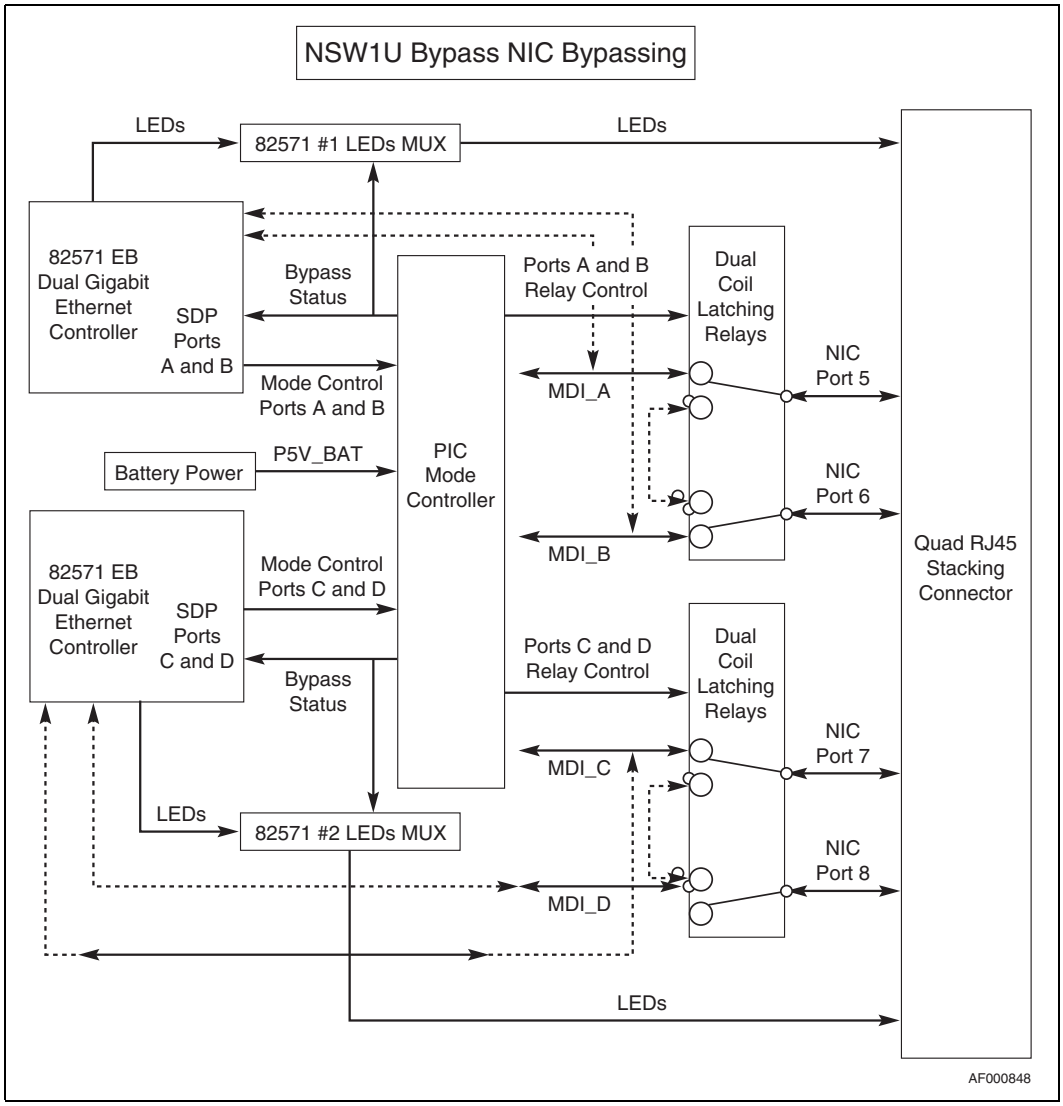


Figure 41 is an EFPB block diagram showing NIC bypassing.

Figure 41. EFPB Board Diagram (NIC Bypass)



4.3 Front Panel Switches, LEDs, and Relays

4.3.1 Front Panel Switches

The IP Network Server NSW1U front panel has a power switch, a reset switch, an NMI switch, and a system ID switch. The function of these switches is described in Table 22.

Table 22. Front Panel Switch Description

Switch	Function
Power Switch	Toggles system power on/off. Functions as a sleep button if enabled by an ACPI-compliant operating system.
Reset Switch	Resets the system when it is in the power-on state.
NMI Switch	Instructs the processor to copy system memory to hard disk.
System ID Switch	Instructs the processor to toggle the state of the system ID LED.

4.3.2 Front Panel LEDs

Table 23 lists the front panel LED specifications.

Table 23. Front Panel LED Specifications

LED and Function		LED Color	Peak Wavelength (nm)	Luminous Intensity Typ (mcd) @20mA	Luminous Intensity Min (mcd) @20mA
ID		Blue	470	1.1	0.5
NIC		Green	560	12	6.0
ON		Green	560	12	6.0
HDD		Green	565	12	4.0
STATUS	GOOD	Green	565	12	4.0
	MINOR	Yellow	596	24	8.0
	SEVERE	Red	627	12	4.0
PWR		Green	560	12	6.0

4.3.3 System Status LEDs

There are five FPIO board system status LEDs. The function of each of these system status LEDs is described in Table 24.

Table 24. FPIO Board System Status LEDs

Status LED	Function
Power	The green power LED indicates that system power is on when it is illuminated continuously. When it blinks green, it indicates that the system is in ACPI sleep mode.
NIC	The green NIC activity LED indicates network link presence and activity on any of the front or rear NIC ports.
System ID	The blue ID LED is used to identify a particular system. The LED can be toggled remotely or locally with the front-panel System ID Switch.
Status	The green/amber bi-color LED indicates system status as follows • Steady green indicates system in standby or ready for operation. • Blinking green indicates degraded operation (e.g., power supply redundancy loss, battery failure, non-critical sensor threshold crossed, non-critical fan failure). • Blinking amber indicates one or more non-fatal fault conditions (e.g., excessive memory errors, critical sensor threshold crossed, insufficient fans operating). • Steady amber indicates one or more fatal fault conditions (e.g., power system failure, no good memory, CPU error or thermal condition).
Hard Drive	The green HDD LED indicates activity of either or both of the hard disk drives.

4.3.4 Fan Fault LEDs

The EFP board contains an 8-bit serial-in, parallel-out shift register to control the on-board fan fault LEDs. Each of the four fan LEDs is mapped to the bits of the shift register as indicated in Table 25.

Table 25. Front Panel Fan Fault LEDs

Fan ID	Shift Register Bit Location
FAN1 (in front of DIMMs)	Bit 7
FAN2 (in front of CPU0)	Bit 6
FAN3 (in front of CPU1)	Bit 5
FAN9 (in front of PCI conn.)	Bit 4

4.4 Temperature Sensor, SATA Drive Support, and I²C Interface

4.4.1 Temperature Sensor

The EFP board provides an LM95010 single-wire interface temperature sensor that the server board can read. The temperature sensor address pins are strapped to ground, which corresponds to the assignment of device number 001. The temperature sensor has an accuracy of ±2º C and provides a temperature reading range of -20º C to +125º C.

4.4.2 SATA Drive Support

The EFP board supports connections to two independent SATA 3.5-inch fixed hard drives. The EFP board supports a transmission rate of 1.5 Gbps using 7200 RPM and 10,000 RPM SATA drives. The ESB-2 (Southbridge) device on the Server Board S5000PHB provides integrated support for software RAID levels 0 and 1.

A pin-out of the SATA connections is shown in Table 11 on page 44.

4.4.3 I²C Interface

The EFP board contains an on-board FRU serial EEPROM for storing system information according to the IPMI specifications. The server board uses the I²C interface to write data to the 2-Kbit serial EEPROM by accessing address AEh. The server board uses the I²C interface to read data from the 2-Kbit serial EEPROM by accessing address AFh.

4.5 Connector Information

Figure 42 shows the location of all the connectors on the EFP board. Table 26 identifies the reference designator, function, and destination for each connector. Connector pin-outs and physical details of the cable assemblies that connect to the EFP board are in Section 3.2 of this specification.

Figure 42. EFP Board Connector Locations

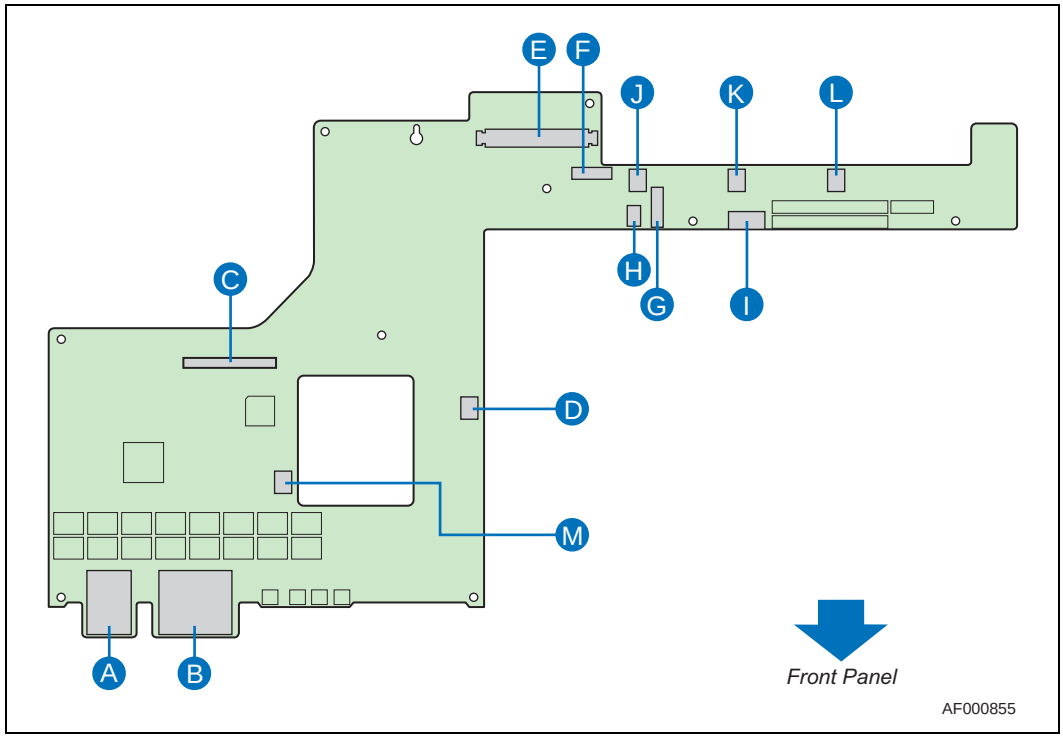


Table 26. EFP Board Connections

Item	Ref Des	Function	Connects to
A	J1J1	Stacked Serial/USB external connector	External devices
B	JA2J1	Quad GbE connector	External Ethernet devices
C	J2E1	Power input connector	Power distribution board
D	JA4F1	Intel® Z-U130 Value Solid State Drive interface	Optional Intel® Z-U130 Value Solid State Drive
E	J6A1	Front panel flex connector	Server board
F	J6B2	SATA Drive 0 connector	SATA HDD0
G	J6C2	SATA Drive 1 connector	SATA HDD1
H	J6C1	Optical drive power	Optional optical device

Table 26. EFP Board Connections (Continued)

Item	Ref Des	Function	Connects to
I	J7C1	SATA power	SATA HDD0 and HDD1
J	J6B3	Fan power	Fan 3 (CPU area)
K	J7B1	Fan power	Fan 2 (CPU area)
L	J8B1	Fan power	Fan 1 (DIMM area)
M	J3G1	Fan power	Fan 9 (PCI area)

4.6 EFP Board Ethernet Functionality

There are three different EFP board configurations; EFPR, EFPF, and EFPB. Depending on the population option, the EFP board consists no Ethernet functionality to a maximum of four Ethernet ports.

- The rear NIC design, EFPR, has no Ethernet controllers.
- The front NIC design, EFPF, contains one 82571EB dual Ethernet controller and one 82563EB dual Ethernet controller to support a total of four ports.
- The EFP bypass NIC design, EFPB, contains two dual 82571EB Ethernet controllers to support a total of four ports. This configuration uses a different board layout from the other configurations to include circuitry for port bypass mode.

Each of the Ethernet controllers on the EFP board consists of two integrated Media Access Controller (MAC) ports plus two physical layer (PHY) ports. Each controller supports 10Base-T, 100Base-T, and 1000Base-T full and half duplex applications across IEEE 802.3-compliant Category 5 twisted pair cabling.

4.6.1 Intel 82571EB Dual Ethernet Controller

During normal EFP Ethernet operations, the 82571EB Ethernet controller (a single 82571EB controller on an NSW1U-FNIC or two such controllers on an NSW1U-Bypass) communicates with the server board I/O controller hub using a x4 PCI Express (PCIe) interface. Clocking and synchronization are based on a 100 MHz PCIe differential clock that is sourced from the server board across the front panel flex connector.

Each 82571EB has its own 16-Kbit EEPROM to hold configuration information, including the MAC addresses of the NICs.

Table 27 outlines a list of signals that are critical to the operation of the 82571EB Ethernet Controller.

Table 27. 82571EB Ethernet Controller Signal List

Signal Name	Signal Function	Comments
DNW_NIC_SRC_P(N)	Differential 100 MHz PCI Express clock	Clock pair is sourced from the server board and requires 300 ppm frequency tolerance
EXPD4_MCH_TX[3:0]_P(N)	Differential 2.5 Gbps 4-lane PCI Express input data to 82571EB	Signals require blocking caps that are located at the server board transmitter
EXPD4_MCH_RX[3:0]_P(N)	Differential 2.5 Gbps 4-lane PCI Express output data from 82571EB	Signals contain blocking caps that are located near the output pins of the 82571EB
FP_PE_WAKE_N	Open drain output to notify the server manager of a valid wake-on-LAN packet	

Table 27. 82571EB Ethernet Controller Signal List

Signal Name	Signal Function	Comments
SYS_RESET_N	PCI Express Reset	Active low signal that forces all PCI Express functions into reset mode. Signal should go high only after power is stable and the PCIe reference clock is available
OPHIR_MDI[3:0]_P(N)	4-channel Media Dependent Interface signals	Analog front end IEEE802.3 copper Ethernet signals
AUX_PWR_STRAP	Auxiliary power present	This signal is strapped high to indicate controllers are supported by standby power in the event of power loss
OPHIR_DIS_N	Individual Ethernet port disable inputs	State is latched upon a rising edge of SYS_RESET_N or a PCI-e reset event
OPHIR_SDPA(B)_[3:0]	Software-definable pins	SDP pins are used to control and monitor system NIC bypass modes
OPHIR_EE_DI(DO,SK,CS_N)	4-wire SPI interface to external EEPROM	

4.6.2 Intel 82563EB Dual Ethernet PHY

During normal EFP Ethernet operations, the 82563EB Ethernet controller in an NSW1U-F server communicates with the server board I/O controller hub using the high speed serial GLCI interface.

The MAC addresses for the 82563EB are configured on the server board; the base MAC address, which is used for the NIC 1 port, is indicated in barcode and alphanumeric formats on a label on the Server Board S5000PHB. In addition to the NIC port, each channel of the 82563EB supports a second port that provides access to the baseboard management controller (BMC) that is embedded in the ESB-2 (Southbridge) to support IPMI remote management over LAN. These IPMI ports share the same physical port connections and IP addresses as the NIC ports, but have their own MAC addresses with +2 and +3 offsets from the base MAC address.

Table 28 summarizes the 82563EB controller signals.

Table 28. 82563EB Ethernet Controller Signal List

Signal Name	Signal Function	Comments
ESB_LAN_SERP(N)0(1)	Differential high-speed GLCI serial input data to 82563EB	Signals require blocking caps that are located at the server board transmitter
ESB_LAN_SETP(N)0(1)	Differential high-speed GLCI serial output data from 82563EB	Signals require blocking caps that are located at the server board transmitter
GILGAL_PWR_P1V2_CTRL	1.2 V linear voltage regulator reference	The chip is strapped to internally generate 1.2V. This pin controls an external PNP transistor to produce a linearly-regulated supply
GILGAL_PWR_P1V8_CTRL	1.9 V linear voltage regulator reference	The chip is strapped to internally generate 1.9V. This pin controls an external PNP transistor to produce a linearly-regulated supply
SYS_RESET_N	Power-on reset	Active low signal that forces the entire chip to enter the reset state
GILGAL_MDI[3:0]_P(N)	4-channel Media Dependent Interface signals	Analog front end IEEE802.3 copper Ethernet signals

4.6.3 Ethernet Indicators

The EFP board provides two indicator LEDs for each of the four Ethernet ports. The LEDs are integrated into the quad RJ45 stacking connector and are designed to support link and activity indications for each of the four Ethernet ports. The green LED to the left of each connector indicates the status and activity of the link, and the bi-color LED to the right of each Ethernet connector indicates link speed. Table 29 lists the various LEDs indication combinations and their meanings.

Table 29. Ethernet Status LED Indications

Link LED Indication	Speed LED Indication	Meaning
Off	Off	Port disconnected; no link
Solid green	Off	Port connected at 10 Mbps, no link activity
Solid green	Solid green	Port connected at 100 Mbps, no link activity
Solid green	Solid amber	Port connected at 1 Gbps, no link activity
Blinking green	Off	Port connected at 10 Mbps, activity on link
Blinking green	Solid green	Port connected at 100 Mbps, activity on link
Blinking green	Solid amber	Port connected at 1 Gbps, activity on link

4.6.4 Clocks

Each of the two EFP Ethernet controllers is directly connected to a 25 MHz crystal with a frequency tolerance of 30 ppm.

4.6.5 EEPROM

The 82571EB Ethernet controller contains a dedicated serial EEPROM (2 Kbyte) that is used to store configuration data, including the MAC addresses. Access to the EEPROM is performed over the 4-wire SPI bus.

Configuration data for the 82563EB resides on the server board and is managed by the server board I/O controller hub.

4.6.6 Power-Up Sequencing Requirement

Power sequencing is required to ensure that the devices operate properly after power-up and to minimize reliability issues. To meet 375 mA inrush current requirements on the two Ethernet controllers, the power supply ramp rates are set at 24 ms ramp. In addition, the P3V3_AUX rail will begin to ramp and stabilize before P1V8_AUX. Likewise, the P1V8_AUX will begin to ramp and stabilize before P1V1_AUX. Since the 82563EB Ethernet Controller is strapped to generate 1.2 V and 1.9 V internally, no additional power-up sequencing is needed on the board.

4.6.7 EFPF Board Wake-On-LAN

The EFPF board supports wake-on-LAN for both Ethernet controllers. The EFP board is capable of entering sleep mode (i.e., power down mode), but, the Ethernet controllers remain actively powered by switching their power rails to standby power. The EFP contains switching circuitry to detect power loss and to switch to standby power for each controller in the event of a power loss or power down. When the EFP receives the specified Ethernet frame or “magic packet” from the LAN interface, it alerts the I/O hub to enable the server board to come out of sleep mode and begin servicing requests from the remote device.

The Ethernet controller operates in 10Base-T or 100Base-T only when entering wake-on-LAN mode in order to conserve power.

4.7 EFPB NIC Bypass Functionality

The EFPB board supports the ability to bypass the on-board Ethernet controllers and to route LAN analog front end signals back onto their adjacent ports. The EFPF board is currently designed to loop data from port A to port B and port C to port D. During normal operations, all four Ethernet ports are connected to the two on-board dual Ethernet controllers. In order to enter the bypass mode, the on-board PIC microcontroller receives commands from the 82571EB via the SDP pins to activate bypass. Once valid commands are received, the PIC proceeds to send a 3 mS pulse to the 16 on-board electromechanical latching relays to energize the relays to the switch-over state. The PIC also takes control of the LED drive output by disconnecting the LED drivers from the 82571EB and routing the LED drivers via the on-board MUXes.

4.7.1 NIC Bypass Mode Control

Six software definable pins (SDP) on each 82571EB Ethernet controller are used to control and monitor the bypass functionality on the EFP. The SDPs are used to command the on-board relay controller (PIC16F876A) to enter the various bypass modes. The SDPs from each 82571EB controller have a dedicated mode control port on the PIC. The MODE_CTRL_A[3:0] port is used to command the PIC to connect Ethernet ports A and B, while the MODE_CTRL_B[3:0] port is used to command the PIC to connect Ethernet ports C and D. During power up, the mode control pins are low to ensure that the relays are in the non-bypass mode. The two remaining SDP pins on each 82571EB Ethernet controller are used to provide status on the state of the relays. A logic high signifies that the relays are non-bypass mode and a logic low signifies that the relays are in Bypass mode. Table 30 and Table 31 provide a summary of pin functions and bypass modes, respectively.

Table 30. NIC Bypass Mode Pin Function

Ethernet Controller Pin ID	Signal Name	Comments
82571EB Device A SDPA0	MODE_CTRL_A0	Controls RJ45 ports A&B bypassing
82571EB Device A SDPA2	MODE_CTRL_A1	Controls RJ45 ports A&B bypassing
82571EB Device A SDPB0	MODE_CTRL_A2	Controls RJ45 ports A&B bypassing
82571EB Device A SDPA2	MODE_CTRL_A3	Controls RJ45 ports A&B bypassing
82571EB Device A SDPA3	SPARE A	Reserved for future use
82571EB Device A SDPB3	BYPASS_STATUS_A	Input to 82571EB to verify state of relays
82571EB Device B SDPA0	MODE_CTRL_B0	Controls RJ45 ports C&D bypassing
82571EB Device B SDPA2	MODE_CTRL_B1	Controls RJ45 ports C&D bypassing
82571EB Device B SDPB0	MODE_CTRL_B2	Controls RJ45 ports C&D bypassing
82571EB Device B SDPA2	MODE_CTRL_B3	Controls RJ45 ports C&D bypassing
82571EB DEVICE B SDPA3	SPARE B	Pin Reserved for Future Use
82571EB Device B SDPB3	BYPASS_STATUS_B	Input to 82571EB to verify state of relays

Table 31. Bypass Modes

MODE_CTRL[3:0]	Function	Comments
0 0 0 0	Board not powered; don't do anything. This is the pin state while the board is first powering up. The hardware will not take any action with the relays until a valid value is sampled	
0 0 0 1	Normal - Hardware forces the relays into Normal Mode when this state is sampled	
0 0 1 0	Bypass On Power Fail - Hardware leaves relays in Normal Mode as long as power is on, but throws relays into bypass mode if power fails. Note that Power Fail Bypass can be enabled by EEPROM setting only and does not require any SW driver support to function.	
0 0 1 1	Force Bypass - Hardware forces the relays into Bypass Mode immediately when this state is sampled.	
0 1 0 0	Bypass on WDT timeout or Power Fail - WDT timer starts immediately once this state is sampled.	5 second WDT timeout
0 1 0 1	Bypass on WDT timeout or Power Fail - WDT timer starts immediately once this state is sampled.	10 second WDT timeout
0 1 1 0	Bypass on WDT timeout or Power Fail - WDT timer starts immediately once this state is sampled.	15 second WDT timeout
0 1 1 1	Bypass on WDT timeout or Power Fail - WDT timer starts immediately once this state is sampled.	20 second WDT timeout
1 0 0 X	Test Status - MODE_CTRL_X_0 is the clock used to serially clock out the 16-bit checksum of the microcontroller flash memory. The next 16 bits are undefined. The data will be available on BYPASS_STATUS_X. The microcontroller will change the data when the clock is low and the SDP will be read when the clock is high.	
1 0 X X	Invalid state -- don't do anything.	
1 1 X X	Watch Dog Timer Kick - SW sets this value to clear (or 'kick') the watchdog timer. In order to kick the WET, the SW should set bit 3 while maintaining a constant value on bits 2-0. If SW does not kick the WDT before it expires, the HW controller sets the port pair into Bypass Mode.	

4.7.2 Bypass Mode Controller

A PIC16F876A microcontroller implements the functions of the bypass modes. The microcontroller reads the SDPs from each 82571EB Ethernet controller and determines which functions need to be implemented. The PIC contains internal flash memory where the software can be stored. The LAN_PWR_GD signal is monitored to determine the status of the board. The power for the microcontroller is separate from the rest of the board, which allows it to come up before and turn off later than the rest of the board.

Table 32 describes the function of each I/O pin.

Table 32. Bypass Mode Controller I/O Pins

Signal Name	Function	Comments
POWER FAIL	Input signal to the controller to indicate board power rails are falling below their working thresholds	Input to microcontroller
LAN_PWR_GD	Input signal to the controller to indicate board power rails are within their working thresholds	Input to microcontroller
MODE_CTRL_A[3:0]	Mode bits for relay bank A	Input to microcontroller
MODE_CTRL_B[3:0]	Mode bits for relay bank B	Input to microcontroller
BYPASS_LED_A	Signal to toggle LEDs to indicate that ports A and B are in bypass mode	Output from microcontroller
BYPASS_LED_B	Signal to toggle LEDs to indicate that ports C and D are in bypass mode	Output from microcontroller
BYPASS_STATUS_A	Relay status lines for bank A. A logic high will signify that the relays are in bypass mode and a logic low signifies that the relays are in non-bypass mode	Output from microcontroller
BYPASS_STATUS_B	Relay status lines for bank B. a logic high will signify that the relays are in bypass mode and a logic low signifies that the relays are in non-bypass mode	Output from microcontroller
PIC_RESET_N	Local reset to the microcontroller	Input to microcontroller
RELAY_NORMAL_A	Drive for SET relay coil on bank A	Output from microcontroller
RELAY_BYPASS_A	Drive for RESET relay coil on bank A	Output from microcontroller
RELAY_NORMAL_B	Drive for SET relay coil on bank B	Output from microcontroller
RELAY_BYPASS_B	Drive for RESET relay coil on bank B	Output from microcontroller

4.7.3 Bypass Mode Controller Firmware

4.7.3.1 Input Debouncing

The digital inputs are de-bounced by reading the inputs every 1 mS and saving the readings. When an input is low for two consecutive readings and then high, this constitutes a valid low-to-high transition and a flag will be set to take the appropriate action. When an input is high for two consecutive readings and then low, this constitutes a valid high-to-low transition and a flag will be set to take the appropriate action.

4.7.3.2 Test Status

When the microcontroller enters Test Status Mode, it serially places the data on the BYPASS_STATUS_X line when MODE_CTRL_X_0 is low and does not modify the data even when the MODE_CTRL_X_0 line goes high. In this manner, the 16-bit checksum is shifted out LSB to MSB. Other bits can be defined and would be shifted out in the same manner.

4.7.3.3 Power-Up Sequence

When the microcontroller first comes out of reset, it will take no action until LAN_PWR_GD goes active. At that time the microcontroller reads the mode control pins to determine what actions are needed.

4.7.3.4 Watch Dog Timer (WDT)

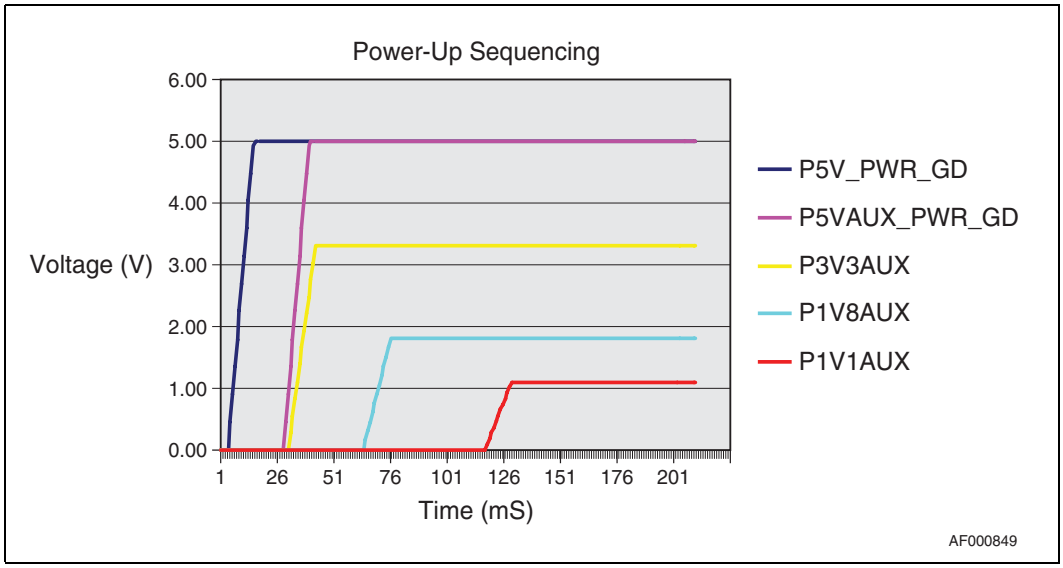
When the microcontroller enters WDT mode, a software countdown timer is loaded with the selected count down period. When the software uses the WDT kick command, the software count down timer is reset with the selected value. When the WDT times out, the microcontroller sets the relays to bypass mode. The relays stay in bypass mode until the microcontroller is commanded to normal mode.

4.8 Specifications

4.8.1 Electrical Specifications -- Power-Up Sequencing

The EFP board receives P5V, P12V, P5V_STBY, P3V3 and P3V3_STBY from either the power distribution board (PDB) or the server board. It generates P5V_AUX, P3V3_AUX, P1V8_AUX, P1V8_NIC, P1V2_NIC, P1V1_AUX, and P5V_BAT from the incoming P12V, P5V or P5V_STBY. The EFP board relies on the FP_PWR_EN signal from the server board in order to trigger its own power generation circuitry. When all power rails are stable and within the operating range, a FP_PWR_GD signal is driven back to the server board to indicate that the EFP board is up and alive. When all input power is good and stable, the EFP board begins the power-up sequencing illustrated in Figure 43.

Figure 43. EFP Board Power-Up Sequence



5.0 Intel® Z-U130 Value Solid State Drive

This chapter describes the basic functions and interface requirements of the Intel® Z-U130 Value Solid State Drive. The information contained in this chapter is organized into the following sections:

- Functional Description
- EFP Board Connector
- Architecture
- Installation

5.1 Functional Description

Key features of the Intel® Z-U130 Value Solid State Drive are:

- Capacity of 1, 2, or 4 Gbyte
- Sequential read performance of 28 Mbyte per second
- Sequential write performance of 20 Mbyte per second
- Supports the USB 2.0 / 1.1 specification

The Intel® Z-U130 Value Solid State Drive attaches to an interposer board and is used with the Ethernet front panel (EFP) board to provide local memory storage for various options including, but not limited to, operating system, system information, diagnostic partitions, and configuration data.

Figure 44 shows the Intel® Z-U130 Value Solid State Drive board as it attaches to the interposer board and Figure 45 gives the dimensions of the Solid State Drive.

Figure 44. Intel® Z-U130 Value Solid State Drive Connection to Interposer Board

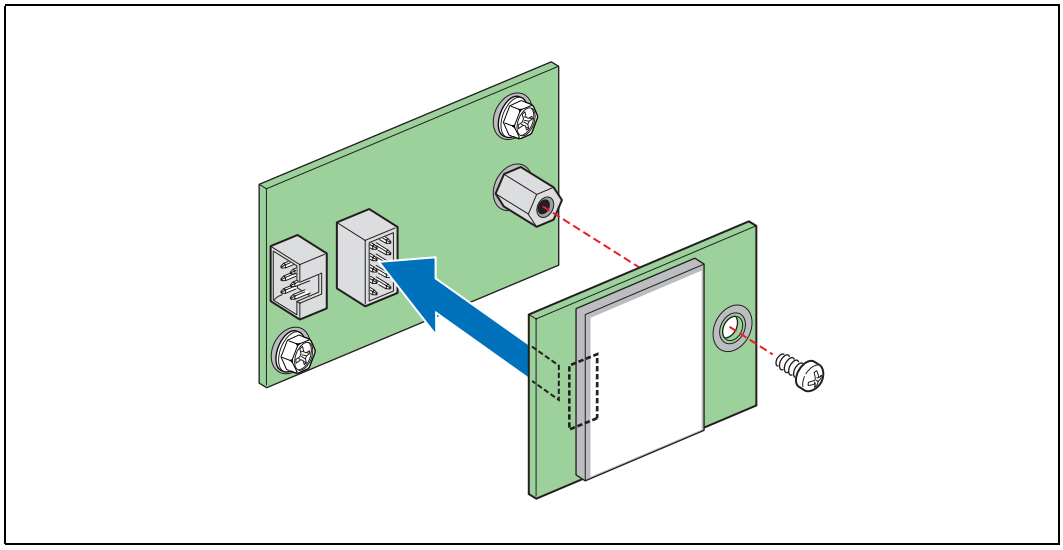
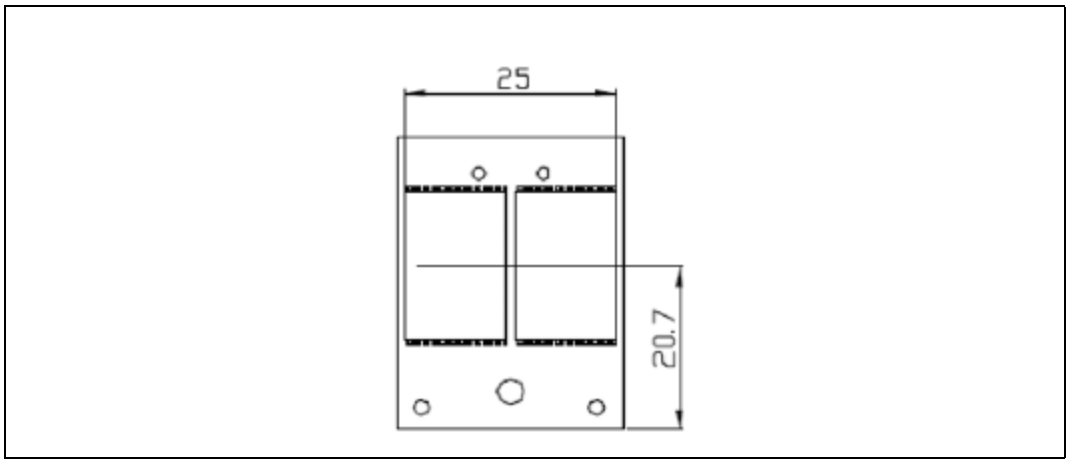


Figure 45. Intel® Z-U130 Value Solid State Drive Dimensions



Because this is a removable media device, it can be moved with the data intact from one system to another. This is useful for cloning system configurations and system options, and for other operations. The connection for the Intel® Z-U130 Value Solid State Drive is made by a USB channel provided by the EFP board.

5.2 EFP Board Connector

Table 33 lists the pinout of the 2 x 3 connector that interfaces to the EFP board.

Table 33. 2 x 3 Connector Pinout

Pin	Blind Mate Signal	Pin	Blind Mate Signal
1	GND	2	N/C (Pin Pulled)
3	USB_Data_Plus (D+)	4	VBUS (+5V)
5	USB_Data_Minus (D-)	6	GND

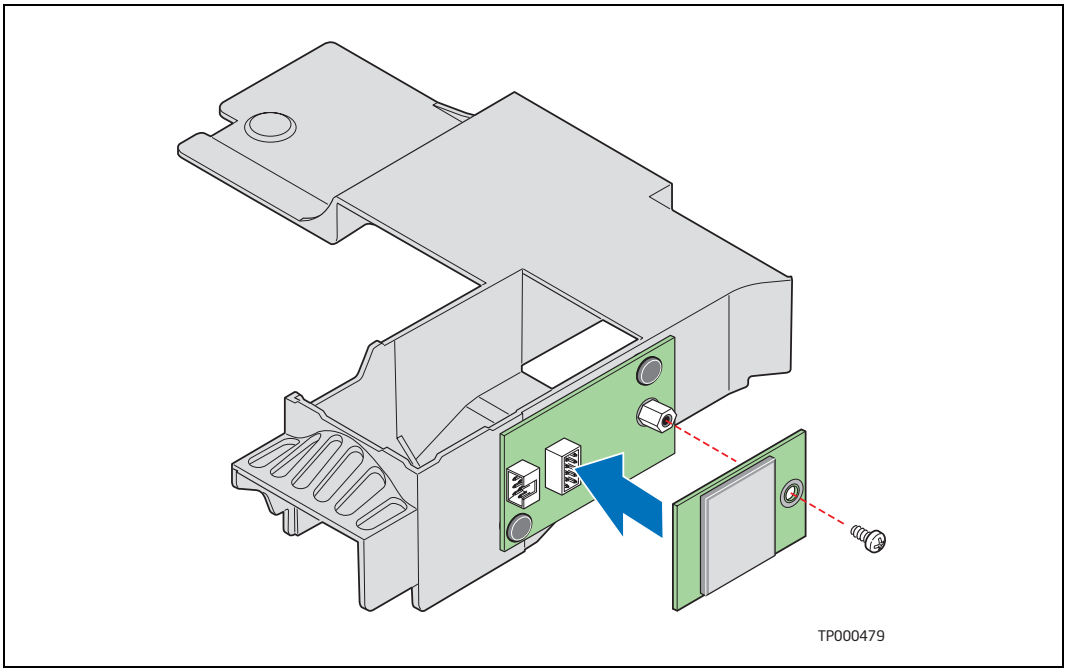
5.3 Architecture

The solid state drive combines Intel® NAND Flash memory and a USB controller to deliver a solution for embedded and thin client markets. The system is based on a single level cell (SLC) flash technology. Each capacity option (1, 2, or 4 Gbyte) contain two NAND flash devices. The high-speed USB 2.0 controller includes 4 symbol error correction capability and wear-leveling algorithms for enhanced NAND management. The controller is backward-compatible to the USB 1.1 specification and complies with USB Mass Storage Class Specification v1.0.

5.4 Installation

The Intel® Z-U130 Value Solid State Drive is installed onto an interposer board. The interposer board attaches to the side of the fan air duct.

Figure 46. Intel® Z-U130 Value Solid State Drive Installation



6.0 PCI Express* Riser Card

This chapter describes the design and external interface of the PCI Express* (PCIe*) riser card, which is standard on the Intel® IP Network Server NSW1U. The PCIe riser board implements one x8 PCI Express slot compatible with full-height, full-length x1, x4, and x8 PCI Express boards. The I/O bracket of the PCIe board is accessible through the server's rear panel.

The information contained in this chapter is organized into the following sections:

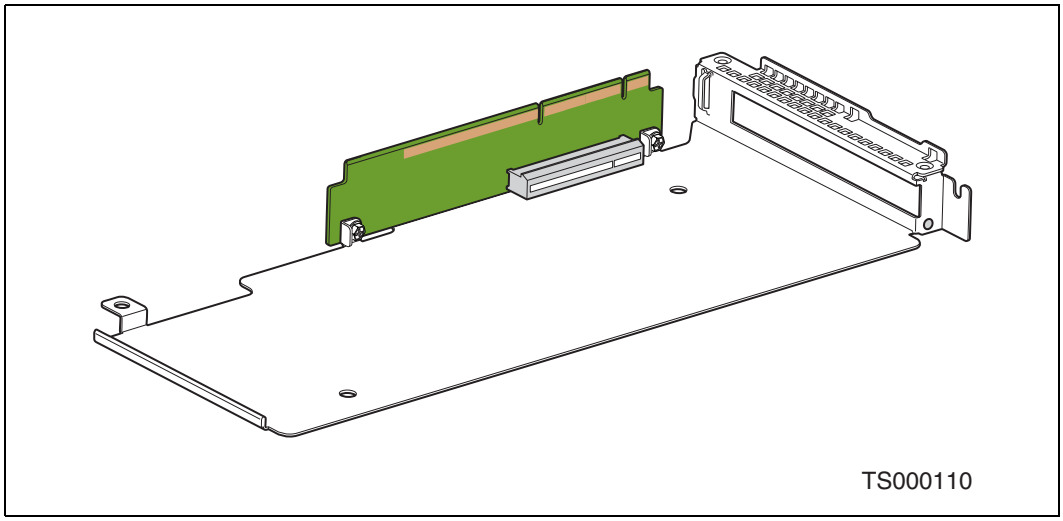
- Introduction
- Functional Description
- PCI Express Riser Card Connector Interface
- Electrical Specification

6.1 Introduction

The PCIe riser card supports one x8 PCIe slot. This is described in the *Intel® Server Board S5000PHB Technical Product Specification*.

Figure 47 shows the FH/FL PCIe riser card layout (upside down from its installed orientation).

Figure 47. PCI Express Riser Card Assembly



6.2 Functional Description

The FH/FL PCIe riser card has one x8 PCIe slot, which can accept x1, x4 or x8 PCI Express boards.

IDSELs are device ID 17 for slot 1.

6.3 PCI Express Riser Card Connector Interface

Table 34 provides the pin-out for the adapter card connector on the PCIe riser card.

Table 34. PCI Express Riser Slot Pin-Out (Sheet 1 of 2)

Pin #	Signal	Pin #	Signal
B1	+12V	A1	Reserved
B2	+12V	A2	+12V
B3	Reserved	A3	+12V
B4	GND	A4	GND
B5	SMCLK	A5	Reserved
B6	SMDATA	A6	Reserved
B7	GND	A7	Reserved
B8	+3.3V	A8	Reserved
B9	Reserved	A9	+3.3V
B10	+3.3VAUX	A10	+3.3V
B11	WAKE_N	A11	PWRGD
KEY			
B12	Reserved	A12	GND
B13	GND	A13	REFCLK+
B14	HSOP0+	A14	REFCLK-
B15	HSOP0-	A15	GND
B16	GND	A16	HSIP0+
B17	Reserved	A17	HSIP0-
B18	GND	A18	GND
B19	HSOP1+	A19	Reserved
B20	HSOP1-	A20	GND
B21	GND	A21	HSIP1+
B22	GND	A22	HSIP1-
B23	HSOP2+	A23	GND
B24	HSOP2-	A24	GND
B25	GND	A25	HSIP2+
B26	GND	A26	HSIP2-
B27	HSOP3+	A27	GND
B28	HSOP3-	A28	GND
B29	GND	A29	HSIP3+
B30	Reserved	A30	HSIP3-
B31	Reserved	A31	GND

Table 34. PCI Express Riser Slot Pin-Out (Sheet 2 of 2)

Pin #	Signal	Pin #	Signal
B32	GND	A32	Reserved
B33	HSOP4+	A33	Reserved
B34	HSOP4-	A34	GND
B35	GND	A35	HSIP4+
B36	GND	A36	HSIP4-
B37	HSOP5+	A37	GND
B38	HSOP5-	A38	GND
B39	GND	A39	HSIP5+
B40	GND	A40	HSIP5-
B41	HSOP6+	A41	GND
B42	HSOP6-	A42	GND
B43	GND	A43	HSIP6+
B44	GND	A44	HSIP6-
B45	HSOP7+	A45	GND
B46	HSOP7-	A46	GND
B47	GND	A47	HSIP7+
B48	Reserved	A48	HSIP7-
B49	GND	A49	GND

6.4 Electrical Specification

The maximum power per slot is 25 W. This conforms to *PCI Express Specification 2.0*.

7.0 PCI/PCI-X* Riser Card

This chapter describes the design and external interface PCI/PCI-X* riser card, which is an optional accessory for the Intel® IP Network Server NSW1U. The riser card implements one 3.3 V, 64-bit PCI/PCI-X slot, with access to the I/O bracket through the server's rear panel.

The information in this chapter is organized into the following sections:

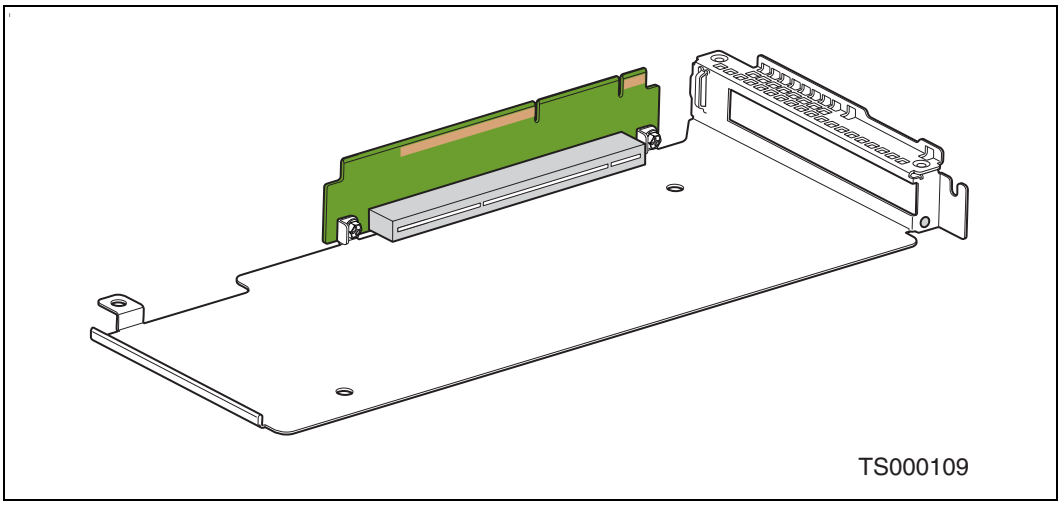
- Introduction
- Functional Description
- PCI-X Riser Card Connector Interface
- Electrical Specification

7.1 Introduction

The PCI/PCI-X riser card supports one 3.3 V, 64-bit slot. The bus speed varies from 33 MHz to 133 MHz depending on the PCI or PCI-X adapter card installed in the riser card. For a detailed description of this card, see the *Intel® Server Board S5000PHB Technical Product Specification*.

Figure 48 illustrates the riser board assembly (upside down from its installed orientation).

Figure 48. PCI-X Riser Card Assembly



7.2 Functional Description

The PCI/PCI-X riser card has one 64-bit slot that supports bus speeds of 33 MHz and 66 MHz for PCI add-in cards and 66 MHz, 100 MHz, and 133 MHz for PCI-X cards.

IDSELs are AD24 for slot 1.

7.3 PCI-X Riser Card Connector Interface

Table 35 lists the signals available on the PCI/PCI-X card slot.

Table 35. PCI/PCI-X Riser Card Slot Pin-Out (Sheet 1 of 3)

Pin #	Signal	Pin #	Signal
B1	-12V	A1	TRST#
B2	TCK	A2	+12V
B3	GND	A3	TMS
B4	Reserved	A4	TDI
B5	+5V	A5	+5V
B6	+5V	A6	P64IRQ0
B7	P64IRQ1	A7	P64IRQ2
B8	P64IRQ3	A8	+5V
B9	Reserved	A9	Reserved
B10	Reserved	A10	+3.3V
B11	Reserved	A11	Reserved
KEY			
B14	Reserved	A14	+3.3VAUX
B15	GND	A15	RST#
B16	CLK	A16	+3.3V
B17	GND	A17	GNT#
B18	REQ#	A18	GND
B19	+3.3V	A19	PME#
B20	AD31	A20	AD30
B21	AD29	A21	+3.3V
B22	GND	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	GND
B25	+3.3V	A25	AD24
B26	C/BE3#	A26	IDSEL
B27	AD23	A27	+3.3V
B28	GND	A28	AD22
B29	AD21	A29	AD20
B30	AD19	A30	GND
B31	+3.3V	A31	AD18
B32	AD17	A32	AD16
B33	C/BE2#	A33	+3.3V
B34	GND	A34	FRAME#
B35	IRDY#	A35	GND
B36	+3.3V	A36	TRDY#
B37	DEVSEL#	A37	GND

Table 35. PCI/PCI-X Riser Card Slot Pin-Out (Sheet 2 of 3)

Pin #	Signal	Pin #	Signal
B38	GND	A38	STOP#
B39	LOCK#	A39	+3.3V
B40	PERR#	A40	SMCLK
B41	+3.3V	A41	SMDATA
B42	SERR#	A42	GND
B43	+3.3V	A43	PAR
B44	C/BE1#	A44	AD15
B45	AD14	A45	+3.3V
B46	GND	A46	AD13
B47	AD12	A47	AD11
B48	AD10	A48	GND
B49	M66EN	A49	AD9
B50	GND	A50	GND
B51	GND	A51	GND
B52	AD8	A52	C/BE0#
B53	AD7	A53	+3.3V
B54	+3.3V	A54	AD6
B55	AD5	A55	AD4
B56	AD3	A56	GND
B57	GND	A57	AD2
B58	AD1	A58	AD0
B59	+3.3V	A59	+3.3V
B60	ACK64#	A60	REQ64#
B61	+5V	A61	+5V
B62	+5V	A62	+5V
KEY			
B63	Reserved	A63	GND
B64	GND	A64	C/BE7#
B65	C/BE6#	A65	C/BE5#
B66	C/BE4#	A66	+3.3V
B67	GND	A67	PAR64
B68	AD63	A68	AD62
B69	AD61	A69	GND
B70	+3.3V	A70	AD60
B71	AD59	A71	AD58
B72	AD57	A72	GND
B73	GND	A73	AD56
B74	AD55	A74	AD54
B75	AD53	A75	+3.3V
B76	GND	A76	AD52

Table 35. PCI/PCI-X Riser Card Slot Pin-Out (Sheet 3 of 3)

Pin #	Signal	Pin #	Signal
B77	AD51	A77	AD50
B78	AD49	A78	GND
B79	+3.3V	A79	AD48
B80	AD47	A80	AD46
B81	AD45	A81	GND
B82	GND	A82	AD44
B83	AD43	A83	AD42
B84	AD41	A84	+3.3V
B85	GND	A85	AD40
B86	AD39	A86	AD38
B87	AD37	A87	GND
B88	+3.3V	A88	AD36
B89	AD35	A89	AD34
B90	AD33	A90	GND
B91	GND	A91	AD32
B92	Reserved	A92	Reserved
B93	Reserved	A93	GND
B94	GND	A94	Reserved

7.4 Electrical Specification

The maximum power per slot is 25 W. This conforms to *PCI Specification 2.2*.

8.0 AC Power Subsystem

This chapter defines the features and functionality of the AC-input switching power subsystem of the Intel® IP Network Server NSW1U. The AC power subsystem has up to two AC-input power supply modules that can operate in redundant mode, and a power distribution board (PDB).

The information contained in this chapter is organized into the following sections:

- Features
- Power Distribution Board
- AC-input Power Supply Module

8.1 Features

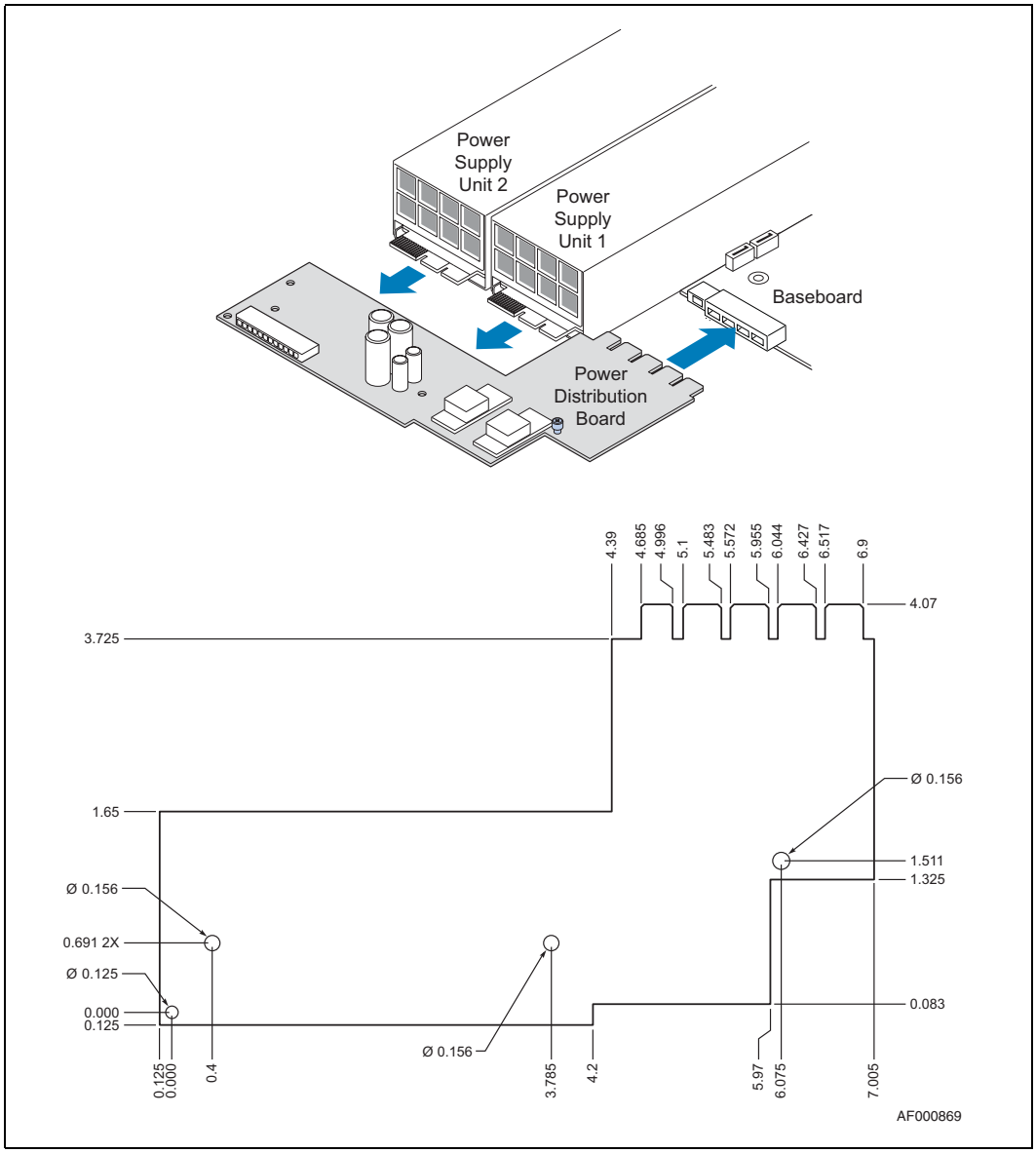
- 450 W output capability over full AC input voltage range
- Power good indication LEDs
- Predictive failure warning
- External cooling fans with multi-speed capability
- Remote sense of 3.3 V, 5 V, and 12 V DC outputs (on the PDB)
- Brown-out protection and recovery
- Built-in overloading protection capability
- Onboard field replaceable unit (FRU) information
- I^2C interface for server management functions
- Mechanical module latching feature
- Integral handle for insertion/extraction

8.2 Power Distribution Board

8.2.1 PDB Mechanical Specification

The AC-input PDB can support up to two 450 W PSUs in a 1+1 configuration or a 1+0 configuration. A mechanical drawing for the power distribution board is shown in Figure 49.

Figure 49. Power Distribution Board Mechanical Drawing



Note: In NSW1U-Bypass systems only, the power distribution board has a permanently connected wiring harness for the front panel board power rather than the 12-pin connector illustrated in Figure 49.

8.2.2 PDB System Interface

The power distribution board has three interconnections with other system components:

- The PDB has edge fingers that connects to the server board via a five-section blind-mate connector.
- The PDB has two, three-section blind-mate connectors that accept edge finger contacts on the hot-swappable power-supply units.

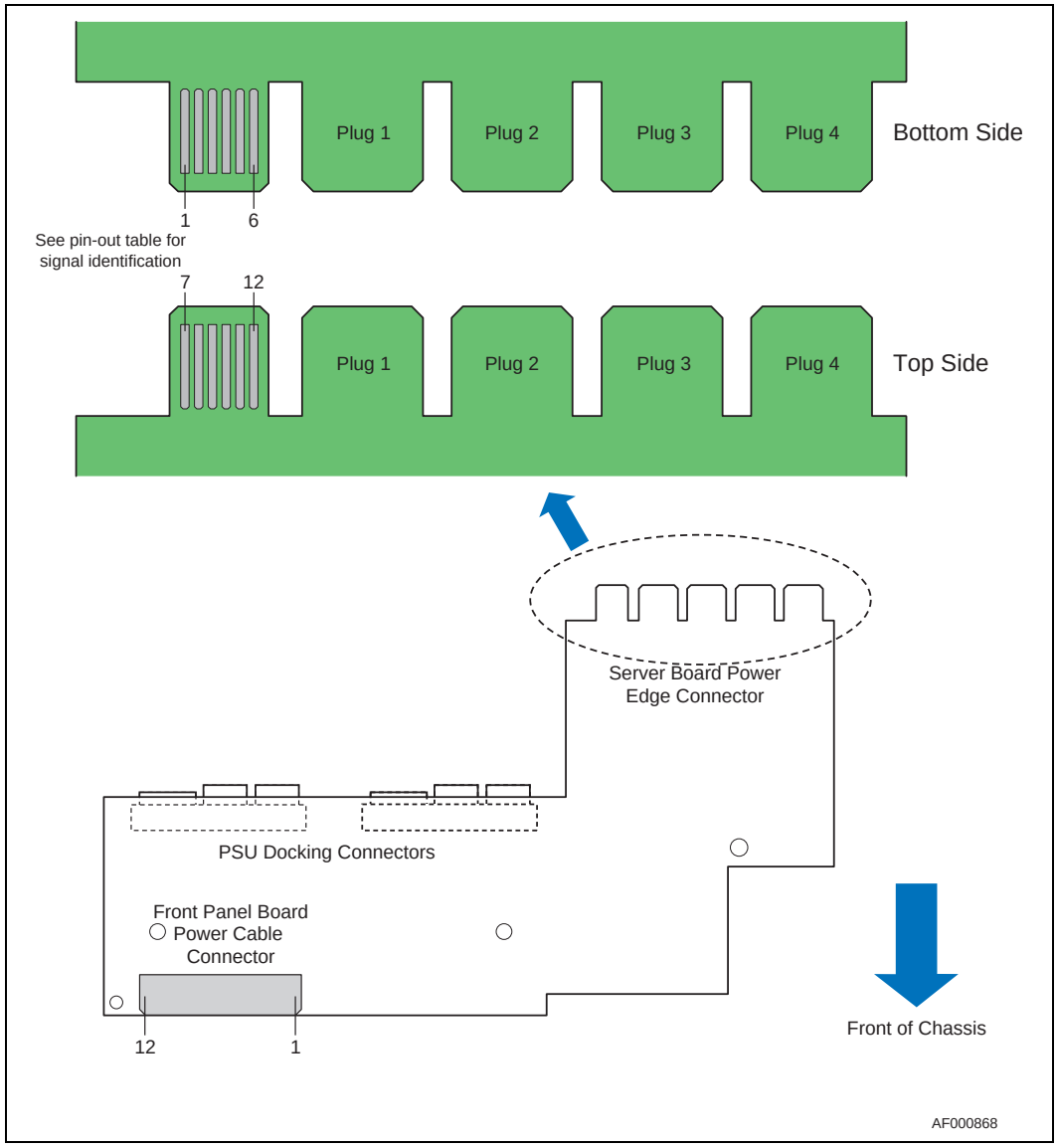
- The PDB has a discrete conductor wiring harness that connects to the front panel board via a single-row 12-pin connector.

All output wiring uses listed or recognized component appliance wiring material (AVLV2), VW-1 flame rating, rated 105° C min, 300 Vdc min.

8.2.2.1 PDB Interface to Server Board

Figure 50 show the connection between the PDB and the Server Board S5000PHB.

Figure 50. PDB Server Board Edge Finger Layout



Note: In NSW1U-Bypass systems only, the power distribution board has a permanently connected wiring harness for the front panel board power rather than the 12-pin connector illustrated in Figure 50.

Figure 51. Server Board Power Docking Connector

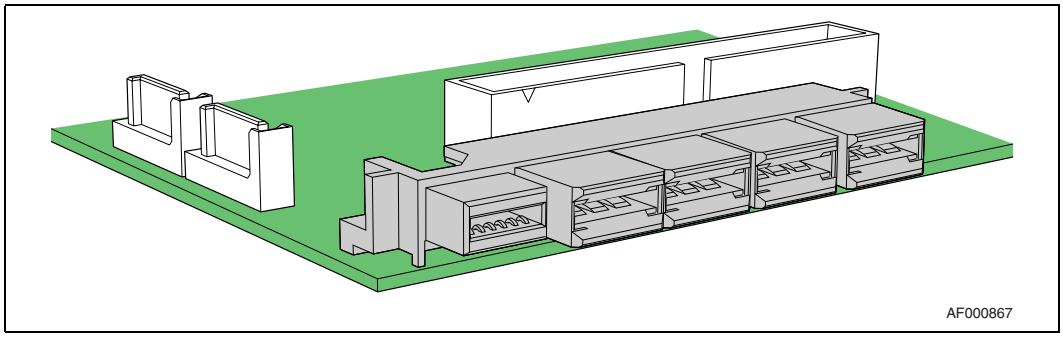


Table 36. PDB Server Board Edge Finger Pin-Out

Pin #	Pin Assignment	Pin #	Pin Assignment
1	PWR OK	7	ReturnS
2	PSON#	8	+3.3RS
3	-12V (0.1 A)	9	+5VSB (1.33 A)
4	I2C Clock	10	+5VSB (1.33 A)
5	I2C Data	11	+5V RS*
6	SMBAlert#	12	+5VSB (1.33 A)
P1 Bottom	COMM (19.61 A)	P1 Top	+12V3 (15.42 A)
P2 Bottom	COMM* (19.61 A)	P2 Top	+5VDC* (6.35 A)
P3 Bottom	COMM (19.61 A)	P3 Top	+3.3VDC* (18.146 A)
P4 Bottom	+12V2 (7.41 A)	P4 Top	+12V1 (7.41 A)

8.2.2.2 PDB Interface to PSUs

Figure 52, Figure 53, and Table 37 document the connection between each PSU module and the PDB.

Figure 52. PSU Docking Connector

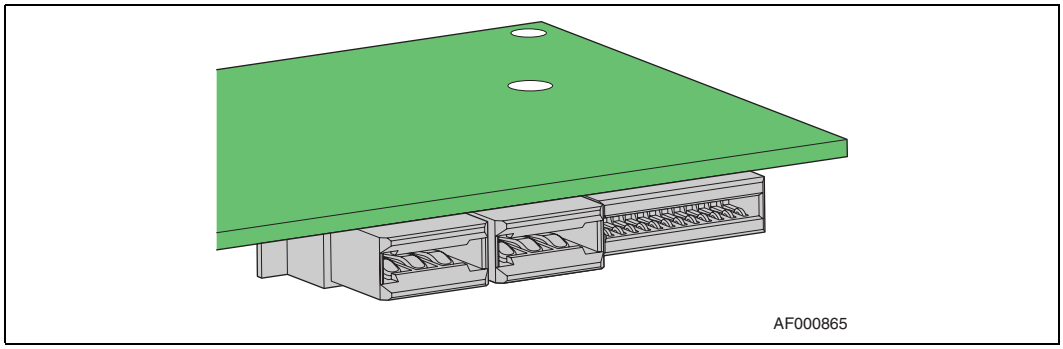


Figure 53. PSU Output Finger Layout

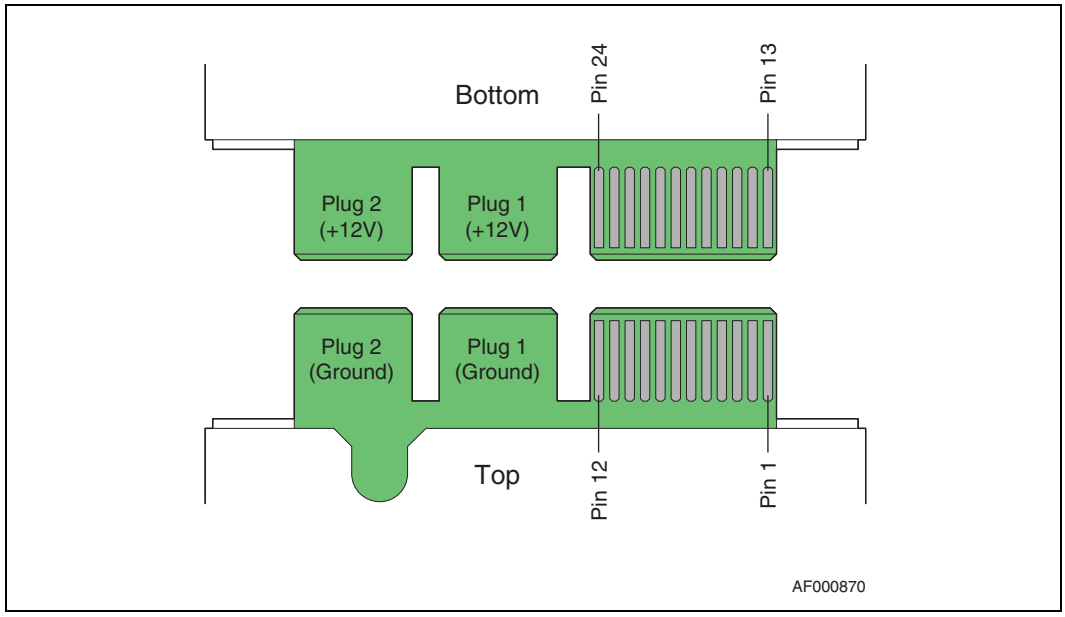


Table 37. PSU Docking Connector Pin Out

Pin #	Pin Assignment	Pin #	Pin Assignment
1	n/c	13	12V RS+
2	n/c	14	12V RS-
3	A0	15	12LS
4	n/c	16	SMB Alert
5	n/c	17	SDA
6	n/c	18	SCL
7	n/c	19	PS Kill
8	n/c	20	PS_ON
9	n/c	21	PWOK
10	n/c	22	A1
11	5VSB	23	5VSB
12	5VSB	24	5VSB
P1 Top	COMM	P1 Bottom	+12V
P2 Top	COMM	P2 Bottom	+12V

8.2.2.3 PDB to Front-Panel Board Interface

The power distribution board uses a 12-conductor, 20 AWG discrete wire harness to connect to the front panel board. On NSW1U_Bypass servers, this harness is permanently connected to the power distribution board. On NSW1U-FNIC and NSW1U-RNIC configurations, the front-panel board power interface is a detachable cable. Table 38 shows the 1 × 12 connector pin-out.

Table 38. Front Panel Board Power Harness Connector Pin-Out

Pin #	Signal
1	P3V3
2	P5V_STBY
3	GND
4	GND
5	P12V
6	P12V
7	P12V
8	GND
9	GND
10	P5V
11	P5V
12	GND

8.2.3 Output Current Requirements

This describes the +12 V output power requirements from the power distribution board with one or two 450 W PSUs plugged into the input of the power distribution board.

Table 39. +12 V Outputs Load Ratings

	+12V1	+12V2	+12V3	+12V4
MAX Load	16 A	16 A	16 A	16 A
MIN Static / Dynamic Load	0 A	0 A	0 A	0 A
Peak load (12 seconds)	18 A	18 A	18 A	18 A
Max Output Power	12 V x 16 A =192 W	12 V x 16 A =192 W	12 V x 16 A =192 W	12 V x 16 A =192 W
Notes: 1. The combined total power limit for all outputs is 450 W max. 2. +12V1/+12V2/+12V3/+12V4 combined output limit = 46.2 A / 63 A pk max.				

The following table defines power and current ratings of the two DC/DC converters located on the PDB, each powered from +12 V rail. The converters must meet both static and dynamic voltage regulation requirements for the minimum and maximum loading conditions.

Table 40. DC/DC Converters Load Ratings

	+12 VDC Input DC/DC Converters	
	+3.3 V Converter	+5 V Converter
MAX Load	15 A	12 A
MIN Static / **Dynamic** Load	0.0 A	0.0 A
Max Output Power	3.3 V x15 A =45 W	5 V x12 A =60 W
Note: 3.3 V / 5 V combined power limit: 95 W max.		

8.2.4 Hot-Swapping Power Modules

Hot swapping a power supply module is the process of extracting and inserting a PSU from a system that is powered on. The power subsystem is capable of supporting hot swapping of power supply modules in a 1 + 1 configuration.

8.2.5 Intelligent Power Subsystem Functions

The PSU and power distribution board (PDB) combination provides a monitoring interface over a server management bus. The device is compatible with both SMBus 2.0 “high power” and I^2C Vdd based power and drive. This bus may operate inside the PSU and PDB at 5 V (powered from stand-by voltage) but, looking from the system server management into the PSU and PDB combination, it is compatible with the 3.3 V bus. A bi-directional I^2C voltage translator IC, such as GTL2002 or similar, is employed on the PDB. The SMBus pull-ups are located on the server board.

The power distribution board’s I^2C bus will have a dual function: to provide PSU and PDB monitoring features and to convey the stored FRU data in the PSU and PDB EEPROM.

8.2.6 FRU Data

The PDB contains a 2 Kbyte EEPROM device that contains FRU data for the power subsystem according to the IPMI spec. Each separate output is given a different number for identification purposes.

8.3 AC-input Power Supply Module

The AC-input power system supports one 450 W SSI TPS (Thin Power Supply) module for a non redundant configuration, or two in a 1 + 1 redundant configuration.

8.3.1 AC-input PSU Mechanical Specification

The power supply module contains one 40 mm fan. The module provides a handle to assist in insertion and extraction and can be inserted and extracted without the assistance of tools.

8.3.2 PSU to PDB Interconnect

The PSU’s PCB extends beyond the PSU enclosure with edge finger contacts and blind mates to a Molex* LPH 45984-005 connector, or equivalent, located on the PDB (power distribution board). This connects the PSU’s output voltages and signals to the PDB. This connection is documented in Figure 52, Figure 53, and Table 37, above.

The PSU is provided with a reliable protective earth ground. All secondary circuits are connected to protective earth ground. Resistance of the ground returns to chassis can not exceed 1.0 mΩ. This path can be used to carry DC current.

8.3.3 AC Input Voltage Requirements

The power supply must operate within all specified limits over the following input voltage range, shown in Table 41. Harmonic distortion of up to 10% THD must not cause the power supply to go out of specified limits. Application of an input voltage below 85 VAC shall not cause damage to the power supply, including a fuse blow.

Table 41. AC Input Voltage Requirements

Parameter	MIN	Rated	Max	Max Input AC Current	Max Rated Input AC Current
Voltage (110)	90 V_{rms}	100-127 V_{rms}	140 V_{rms}	7.0 A_{rms} (See Notes 1 and 3)	6.3 A_{rms} (See Note 4)
Voltage (220)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}	3.5 A_{rms} (See Notes 2 and 3)	3.2 A_{rms} (See Note 4)
Frequency	47 Hz		63 Hz		

1. Maximum input current at low input voltage range shall be measured at 90 VAC, at max load.
2. Maximum input current at high input voltage range shall be measured at 180 VAC, at max load.
3. This is not to be used for determining agency input current markings.
4. Maximum rated input current is measured at 100 VAC and 200 VAC.

8.3.4 Air Flow

Each power supply module incorporates fans for self-cooling, which also contribute to overall system cooling. The cooling air enters the power module from the PDB side (pre-heated air from the system). The fan's variable speed is based on output load and ambient temperature. Under standby mode, the fans run at minimum RPM and provide 3.5 CFM of airflow per PSU module.

8.3.5 Thermal Protection

The PSU incorporates thermal protection that causes a shut-down if airflow through the PSU is insufficient. Thermal protection activates shutdown before the temperature of any PSU component passes the maximum rated temperature. This shutdown takes place before over-temperature-induced damage to the PSU.

9.0 DC Power Subsystem

This chapter defines the features and functionality of the DC-input switching power subsystem of the Intel® IP Network Server NSW1U. The DC power subsystem has up to two DC power supply modules capable of operating in redundant mode and a power distribution board (PDB).

The information contained in this chapter is organized into the following sections:

- Features
- DC-Input Power Distribution Board
- DC-Input Power Supply Module

9.1 Features

- 450 W power module output capability over full DC input voltage range
- 450 W subsystem output capability over full DC input voltage range
- Power good indication LEDs
- Predictive failure warning
- Internal cooling fans with multi-speed capability
- Remote sense of 3.3 V, 5 V, and 12 V DC outputs (on the PDB)
- DC_OK circuitry for brown out protection and recovery
- Built-in load sharing capability
- Built-in overloading protection capability
- Onboard field replaceable unit (FRU) information
- I^2C interface for server management functions
- Integral handle for insertion/extraction
- Mechanical module latching feature

9.2 DC-Input Power Distribution Board

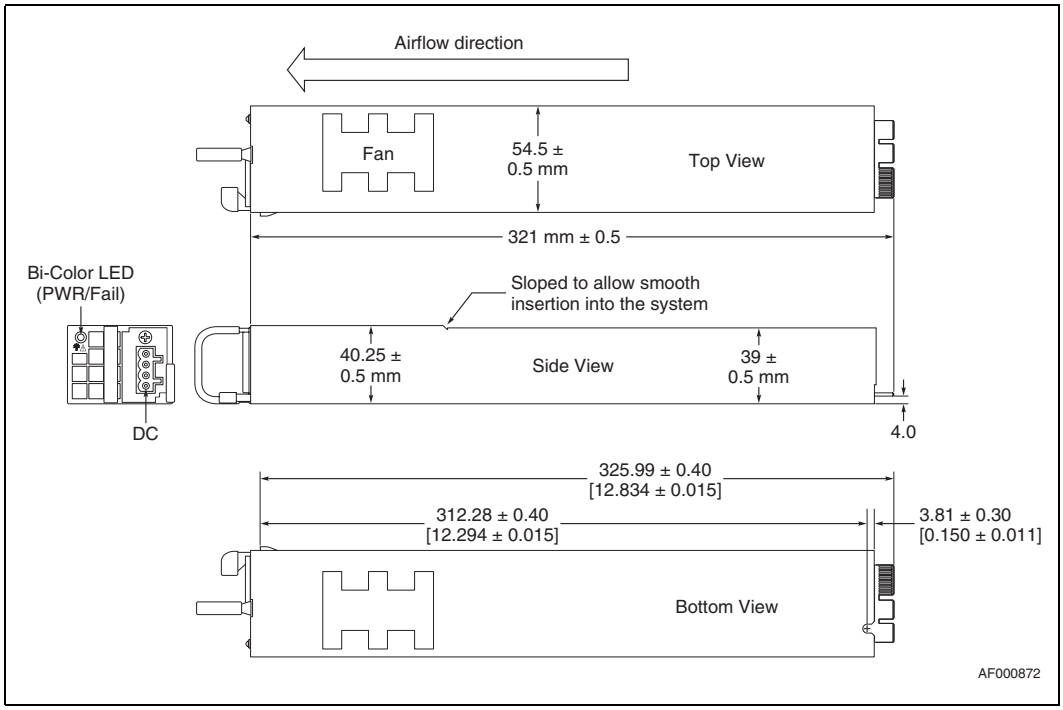
The DC-input power subsystem uses the same PDB as the AC-input subsystem. See Section 8.2, “Power Distribution Board”.

9.3 DC-Input Power Supply Module

9.3.1 PSU Enclosure

A mechanical drawing of the enclosure for the 450 W DC-input power supply module is shown in Figure 54.

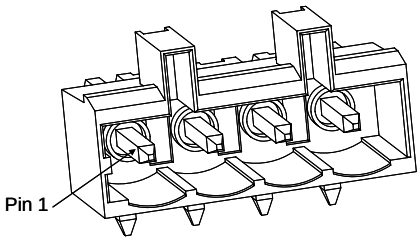
Figure 54. DC PSU Mechanical Drawing



9.3.2 DC Power Supply Unit Input Connector

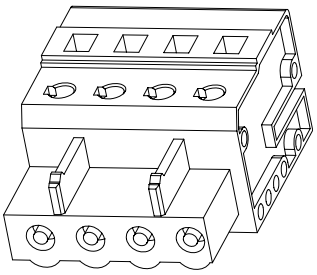
The DC input power is delivered to the PSU through a 4-pin connector (Molex* MTC 55757-0420 or equivalent) as shown in Figure 54.

Figure 55. DC Power Supply Module Input Connector



The mating connector for customer cable termination is a Molex 54927-0420 or equivalent, as shown in Figure 56.

Figure 56. DC Power Supply Module Power Input Mating Connector



The pin-out of the DC input connector is given in Table 42.

Table 42. DC Power Supply Module Input Pin Assignments

Pin#	Description
1	RTN
2	RTN
3	–48V
4	–48V

9.3.3 DC PSU to PDB Interconnect

The PSU's PCB extends beyond the PSU enclosure with edge finger contacts and blind mates to a Molex LPH 45984-005 connector, or equivalent, located on the PDB (power distribution board). This connects the PSU's output voltages and signals to the PDB.

The PSU is provided with a reliable protective earth ground. All secondary circuits are connected to protective earth ground. Resistance of the ground returns to chassis can not exceed 1.0 mΩ. This path can be used to carry DC current.

Figure 57, Figure 58, and Table 43 document the connection between each PSU module and the PDB.

Figure 57. PSU Docking Connector

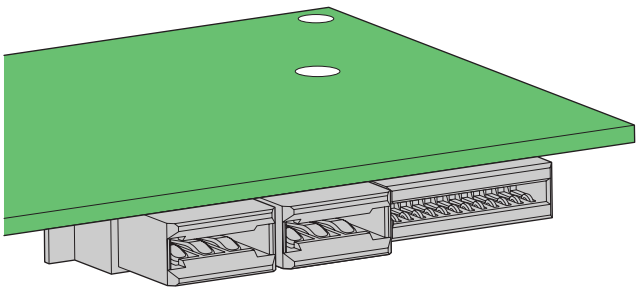


Figure 58. PSU Output Finger Layout

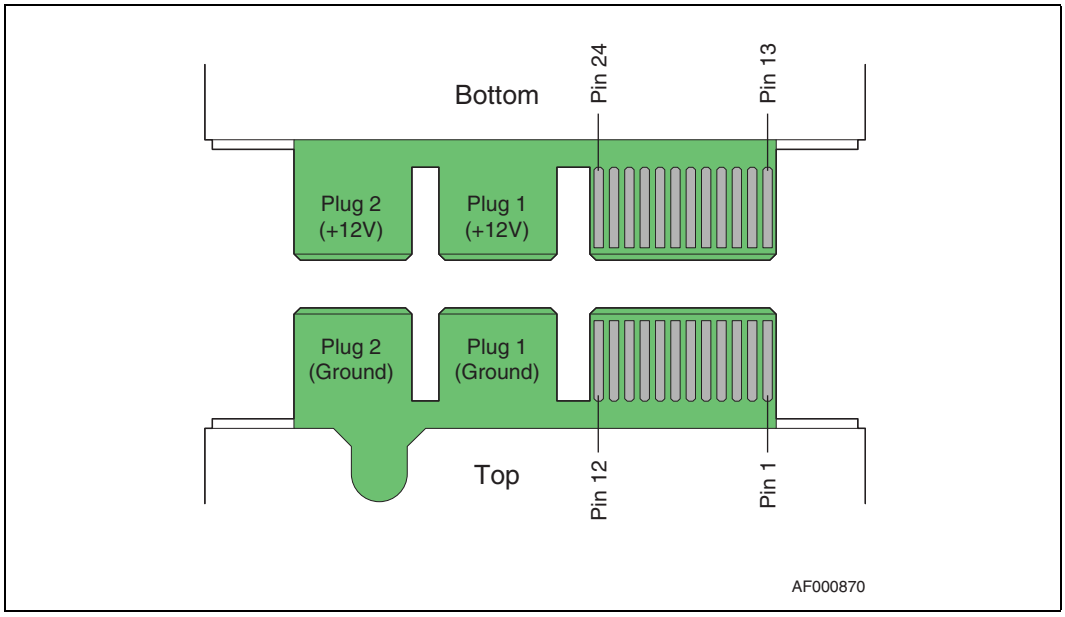


Table 43. PSU Docking Connector Pin Out

Pin #	Pin Assignment	Pin #	Pin Assignment
1	n/c	13	12V RS+
2	n/c	14	12V RS-
3	A0	15	12LS
4	n/c	16	SMB Alert
5	n/c	17	SDA
6	n/c	18	SCL
7	n/c	19	PS Kill
8	n/c	20	PS_ON
9	n/c	21	PWOK
10	n/c	22	A1
11	5VSB	23	5VSB
12	5VSB	24	5VSB
P1 Top	COMM	P1 Bottom	+12V
P2 Top	COMM	P2 Bottom	+12V

9.3.4 DC Input Voltage

The power supply must operate within all specified limits over the following input voltage range, shown in Table 44.

Table 44. DC Input Rating

Parameter	MIN	Rated	MAX
DC Voltage	-38 VDC	-48 VDC/-60 VDC	-75 VDC

Note: There are two rated input voltages. One is for 48 VDC battery plants, the other is for 60 VDC battery plants.

9.3.5 Output Current Ratings

The PSU provides two outputs, +12 V and +5 V standby voltage. The combined maximum output power of all outputs is 450 W (680 W peak). Each output has a maximum and minimum current rating as shown in Table 45.

Table 45. DC PSU Load Ratings

	+12V	+5V standby
MAX Load	37.0 A	3.0 A
MIN DYNAMIC Load	0.0 A	0.1 A
MIN STATIC Load	0.0 A	0.1 A
PEAK Load (12 seconds minimum)	42.0 A	3.5 A
Max Output Power (continuous), see note 1	12 V x 37 A = 444 W max	5 V x 3 A = 15 W max
Peak Output Power (12 sec. min.), see note 2	12 V x 42 A = 504 W pk	5 V x 3.5 A = 17.5 W pk

Notes:

1. At maximum load the output voltages are allowed to sag to -4%. For the 12 V output, this results in 11.52 V, so the actual max power will then be 11.52 V x 37 A = 426.2 W. For the 5 V standby output, the max load voltage can sag to 4.80 V so the actual max power is 4.80 V x 3 A = 14.4 W. The total max continuous power is therefore 426.2 + 14.4 = 440.6 W.
2. At peak load the output voltages are allowed to sag to -4%. For the 12 V output, this results in 11.52 V, so the actual max power will then be 11.52 V x 42 A = 483.8 W. For the 5 V standby output, the max load voltage can sag to 4.80 V so the actual max power is 4.80 V x 3.5 A = 16.8 W. The total max continuous power is therefore 483.8 + 16.8 = 500.6 W.

9.3.6 DC PSU LED Indicators

The PSU provides a single, external, bi-color LED to indicate the status of the power supply.

The LED blinks green when DC is applied to the PSU and standby voltages are available. The LED displays solid green when all the power outputs are available.

The LED displays solid amber when the PSU has failed or shut down due to over-current or over-temperature.

See the following table for conditions of the LED.

Table 46. DC PSU LED Indicators

Power Supply Condition	Bi-color LED Indication
No DC power to all power supplies	OFF
No DC power to this PSU only (for 1+1 configuration) or Power supply **critical event** causing a shutdown: failure, fuse blown (1+1 only), OCP(12V), OVP(12V), fan failed	Amber

Table 46. DC PSU LED Indicators

Power Supply Condition	Bi-color LED Indication
Power supply **warning events** where the power supply **continues to operate**: high temp, high power/high current, slow fan.	1 Hz Blinking Amber
DC present / Only 5 Vsb on (PS Off)	1 Hz Blinking Green
Output ON and OK	Green

9.3.7 Air Flow

The power supply module incorporates fans for self-cooling, which also contribute to overall system cooling. The cooling air enters the power module from the PDB side (pre-heated air from the system). The fan's variable speed is based on output load and ambient temperature. Under standby mode, the fans run at minimum RPM and provide 3.5 CFM of airflow per PSU module.

9.3.8 Thermal Protection

The PSU incorporates thermal protection that causes a shut down if airflow through the PSU is insufficient. Thermal protection activates shutdown before the temperature of any PSU component passes the maximum rated temperature. This shutdown takes place before over-temperature induced damage to the PSU.

10.0 Regulatory Specifications

The Intel® IP Network Server NSW1U meets the specifications and regulations for safety and EMC defined in this chapter.

10.1 Safety Compliance

USA/Canada	UL 60950-1, 1st Edition/CSA 22.2
Europe	Low Voltage Directive, 73/23/EEC TUV/GS to EN60950-1, 1st Edition
International	CB Certificate and Report to IEC60950-1, 1St Edition and all international deviations

10.2 Electromagnetic Compatibility

USA	FCC 47 CFR Parts 2 and 15, Verified Class A Limit
Canada	IC ICES-003 Class A Limit
Europe	EMC Directive, 89/336/EEC EN55022, Class A Limit, Radiated & Conducted Emissions EN55024 Immunity Characteristics for ITE EN61000-4-2 ESD Immunity (level 2 contact discharge, level 3 air discharge) EN61000-4-3 Radiated Immunity (level 2) EN61000-4-4 Electrical Fast Transient (level 2) EN61000-4-5 Surge EN61000-4-6 Conducted RF EN61000-4-8 Power Frequency Magnetic Fields EN61000-4-11 Voltage Fluctuations and Short Interrupts EN61000-3-2 Harmonic Currents EN61000-3-3 Voltage Flicker
Australia/New Zealand	EN55022, Class A Limit
Japan	VCCI Class A ITE (CISPR 22, Class A Limit)
Taiwan	BSMI Approval, CNS 13438, Class A and CNS13436 Safety
Korea	RRL Approval, Class A
China	CCC Approval, Class A (EMC and Safety)
Russia	Gost Approval (EMC and safety)
International	CISPR 22, Class A Limit, CISPR 24 Immunity

10.3 CE Mark

The CE marking on this product indicates that the IP Network Server NSW1U system is in compliance with the European Union's EMC Directive 89/336/EEC, and Low Voltage Directive 73/23/EEC.

10.4 ETSI Standards Compliance (DC Input Only)

The IP Network Server NSW1U with DC input is compliant with the following ETSI specifications:

- ETSI EN 300 386 — EMC requirements for Telecom Equip.
- ETS 300-019-2-1 — Storage Tests, Class T1.2
- ETS 300-019-2-2 — Transportation Tests, Class T2.3
- ETS 300-019-2-3 — Operational Tests, Class T3.2
- ETS 753 — Acoustic Noise

Appendix A: Glossary

This appendix contains important acronyms and terms used in the preceding chapters.

Term	Definition
A, Amp	Ampere
A/µs	Amps per microsecond
AC	Alternating current
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
APIC	Advanced Programmable Interrupt Controller
ASIC	Application specific integrated circuit
AWG	American wire gauge
BIOS	Basic input/output system
BMC	Bus management controller
Bridge	Circuitry that connects one computer bus to another
Byte	8-bit quantity
C	Centigrade
CE	Community European
CFM	Cubic feet per minute
CISPR	International Special Committee on Radio Interference
CSA	Canadian Standards Organization
CTS	Clear to send
DAT	Digital audio tape
dB	Decibel
dBA	Acoustic decibel
DC	Direct current
DIMM	Dual inline memory module
DMI	Desktop management interface
DOS	Disk operating system
DRAM	Dynamic random access memory
DSR	Data set ready
DTR	Data terminal ready
DWORD	Double word – 32-bit quantity
ECC	Error checking and correcting
EEPROM	Electrically erasable programmable read-only memory
EFP	Ethernet front panel

Term	Definition
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EMP	Emergency management port
EN	European Standard (Norme Européenne or Europäische Norm)
EPS	External product specification
ESCD	Extended system configuration data
ESD	Electrostatic discharge
ESR	Equivalent series resistance
F	Fahrenheit
FCC	Federal Communications Commission
FFC	Flexible flat connector
Flash ROM	EEPROM
FPC	Front panel controller
FRB	Fault resilient booting
FRU	Field replaceable unit
G	Acceleration in gravity units, 1 G = 9.8 m/s^2
Gbyte or GB	Gigabyte – 1024 Mbytes
GND	Ground
GPIO	General purpose input/output
Grms	Root mean square of acceleration in gravity units
GUI	Graphical user interface
HDD	Hard disk drive
HPIB	Hot-plug indicator board
HSC	Hot-swap controller
Hz	Hertz – 1 cycle/second
I/O	Input/output
I^2C*	Inter-integrated circuit bus
ICMB	Intelligent Chassis Management Bus
IDE	Integrated drive electronics
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IFLASH	Utility to update Flash EEPROM
IMB	Intelligent management bus
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Initiative
IRQ	Interrupt request line
ITE	Information technology equipment
ITP	In-target probe
JAE	Japan Aviation Electronics
KB	Kilobyte – 1024 bytes
kV	Kilovolt – 1,000 volts

Term	Definition
L2	Second-level cache
LAN	Local area network
LED	Light-emitting diode
LVDS	Low voltage differential SCSI
mA	Milliampere
Mbyte or MB	Megabyte – 1024 Kbytes
MEC	Memory expansion card
mm	Millimeter
MPS	Multiprocessor specification
MTTR	Mean time to repair
mΩ	Milliohm
NEMKO	Norges Elektriske Materiellkontroll (Norwegian Board of Testing and Approval of Electrical Equipment)
NIC	Network interface card
NMI	Nonmaskable interrupt
NWPA	NetWare* Peripheral Architecture
ODI	Open data-link interface
OEM	Original equipment manufacturer
OPROM	Option ROM (expansion BIOS for a peripheral)
OS	Operating system
OTP	Over-temperature protection
OVP	Over-voltage protection
PC-100	Collection of specifications for 100 MHz memory modules
PCB	Printed circuit board
PCI	Peripheral component interconnect
PCI-E	PCI Express peripheral component interconnect
PHP	PCI hot-plug
PID	Programmable interrupt device
PIRQ	PCI interrupt request line
PMM	POST memory manager
PnP	Plug and play
POST	Power-on Self Test
PSU	Power supply unit
PVC	Polyvinyl chloride
PWM	Pulse width modulation
RAS	Reliability, availability, and serviceability
RIA	Ring indicator
RPM	Revolutions per minute
RTS	Request to send
SAF-TE	SCSI Accessed Fault-Tolerant Enclosures
SCA	Single connector attachment
SCL	Serial clock

Term	Definition
SCSI	Small Computer Systems Interface
SDR	Sensor data records
SDRAM	Synchronous dynamic RAM
SEC	Single edge connector
SEL	System event log
SELV	Safety extra low voltage
SEMKO	Sverge Elektriske Materiellkontroll (Swedish Board of Testing and Approval of Electrical Equipment)
SFP	SAS front panel
SGRAM	Synchronous graphics RAM
SM	Server management
SMBIOS	System management BIOS
SMBus	Subset of I^2C bus/protocol (developed by Intel)
SMI	System management interrupt
SMM	Server management mode
SMP	Symmetric multiprocessing
SMRAM	System management RAM
SMS	Server management software
SPD	Serial presence detect
SSI	Server system infrastructure
TUV	Technischer Uberwachungs-Verein (A safety testing laboratory with headquarters in Germany)
UL	Underwriters Laboratories, Inc.
USB	Universal Serial Bus
UV	Under-voltage
V	Volt
VA	Volt-amps (volts multiplied by amps)
Vac	Volts alternating current
VCCI	Voluntary Control Council for Interference
Vdc	Volts direct current
VDE	Verband Deutscher Electrotechniker (German Institute of Electrical Engineers)
VGA	Video graphics array
VRM	Voltage regulator module
VSB	Voltage standby
W	Watt
WfM	Wired for Management
Ω	Ohm
µF	Microfarad
µS	Microsecond

Appendix B: Additional References

This appendix contains information on additional reference documents that contain useful information on the indicated subjects:

Ethernet

- Intel 82559 Fast Ethernet Multifunction PCI/Cardbus Controller Datasheet
  http://developer.intel.com/design/network/datashts/738259.htm

MPS

- MultiProcessor Specification, Version 1.4, Intel Corporation
  http://www-techdoc.intel.com/design/intarch/manuals/242016.htm

PCI

- PCI Bus Power Management Interface Specification, Revision 1.1, PCI Special Interest Group
  http://www.pcisig.com/specifications/conventional/pci_bus_power_management_interface
- PCI Local Bus Specification Revision 3.0, PCI Special Interest Group
  http://www.pcisig.com/specifications/conventional/pci_30

Plug and Play

- Plug and Play ISA Specification, Version 1.0a, Microsoft Corp.
  http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM
- Clarification to Plug and Play ISA Specification, Version 1.0a, Microsoft Corp.
  http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM

Power Supply

- AC ERP1U 450 W Power Supply Module Specification, Intel Corporation.
- DC ERP1U 450 W Power Supply Module Specification, Intel Corporation.
- AC / DC ERP1U 450 W Power Supply Power Distribution Board Specification, Intel Corporation.

Server Management

- Emergency Management Port v1.0 Interface External Product Specification, Revision 0.83, Intel Corporation.
- Intelligent Platform Management Interface (IPMI) Specification, Version 2.0, Intel Corporation.
  http://developer.intel.com/design/servers/ipmi/spec.htm