Silicon Nanotechnology

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Agenda

- What is Nanotechnology?
- Nanoscaling
- Nonclassical CMOS
- Novel Devices
- Summary

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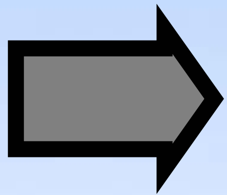
Agenda



What is Silicon Nanotechnology?

CMOS Nanoscaling

Nonclassical CMOS

Novel Devices

Summary

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Nanotechnology Definition

"Research and technology development at the atomic, molecular or macromolecular levels, in the length scale of approximately **1 - 100 nanometer** range."

Dr. Mike Roco, National Science and Technology Council, February 2000

Intel started sub-100nm production in Q3'00

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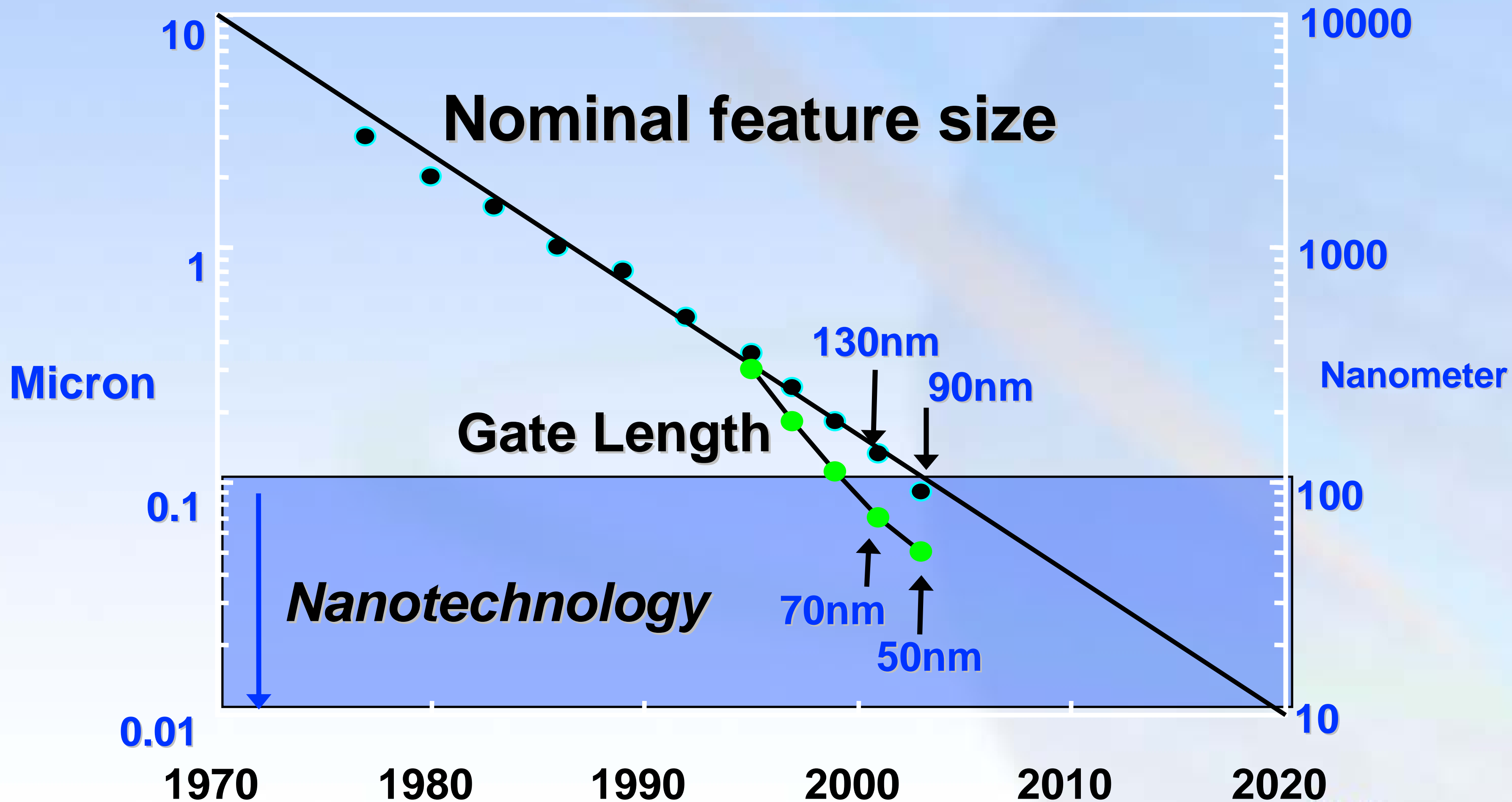
Technology Scaling



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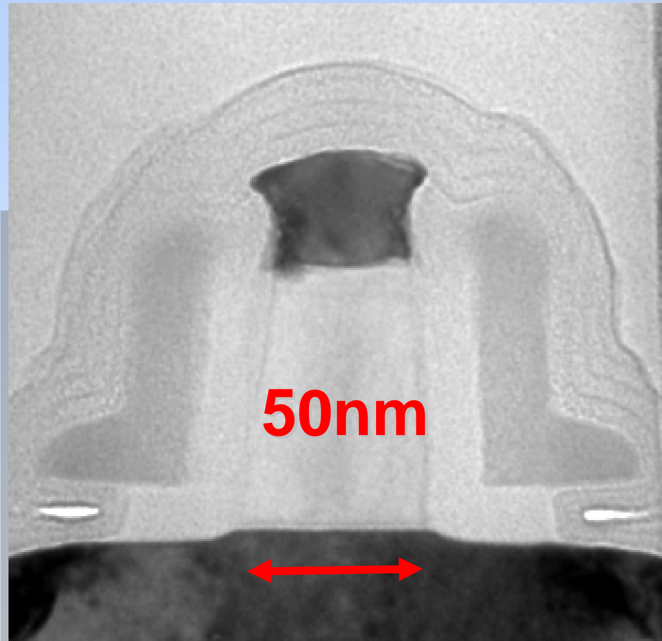
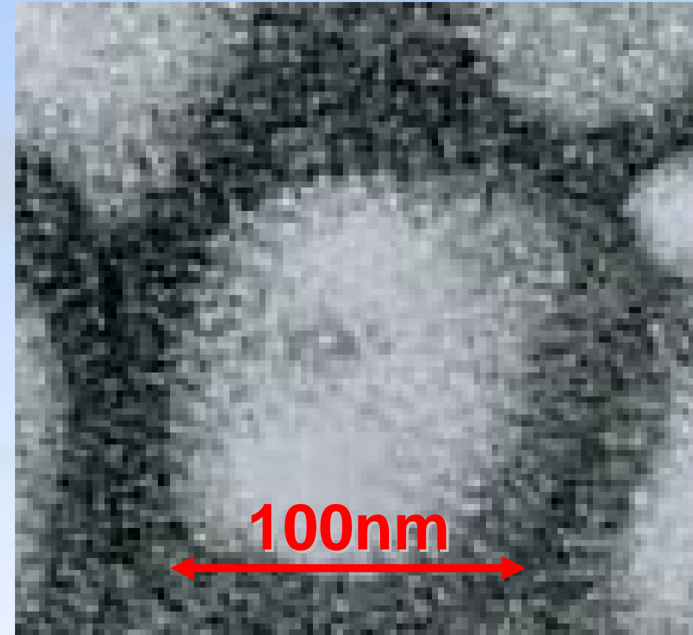
Nanotechnology Today

Example of today's technology: 50 nm transistor dimension



Transistor for 90nm-node
Gate oxide=1.2nm
Source: Intel



Influenza virus
Source: CDC

Intel 2003 Silicon Nanotech Product Revenue >$20B

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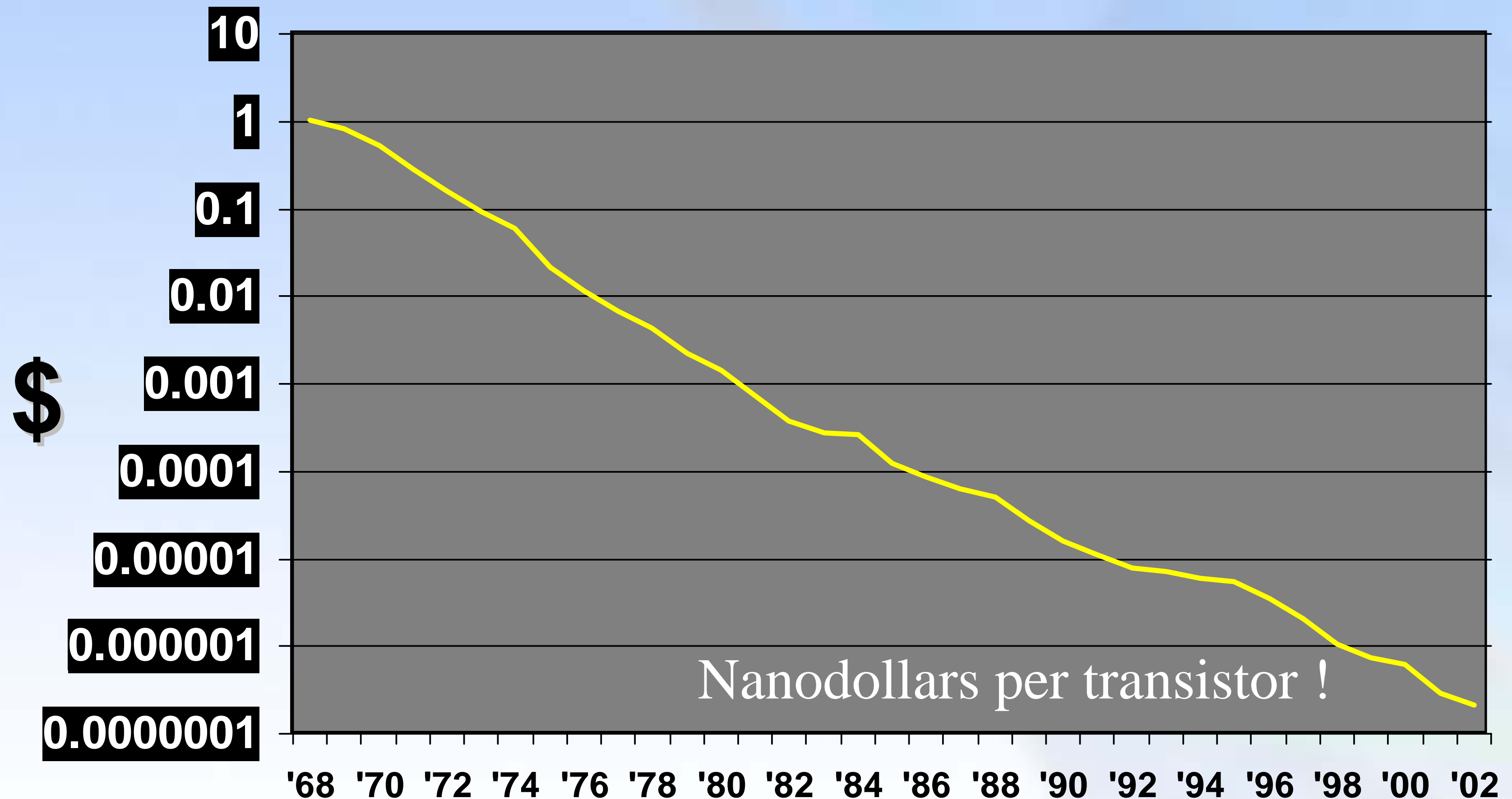
Scaling => Nanoscaling

Nearly 7 Orders Of Magnitude Reduction in Cost/Transistor



Source: WSTS/Dataquest/Intel, 8/02

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Silicon Nanotechnology Evolution

- Continued CMOS Nanoscaling
  -materials, lithography innovation
- Implement Non-classical CMOS
  - new architectures, new structures
- Transition to Novel devices
  -alternative state variables
  -must meet device requirements and demonstrate integrability

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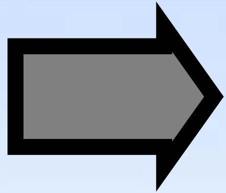
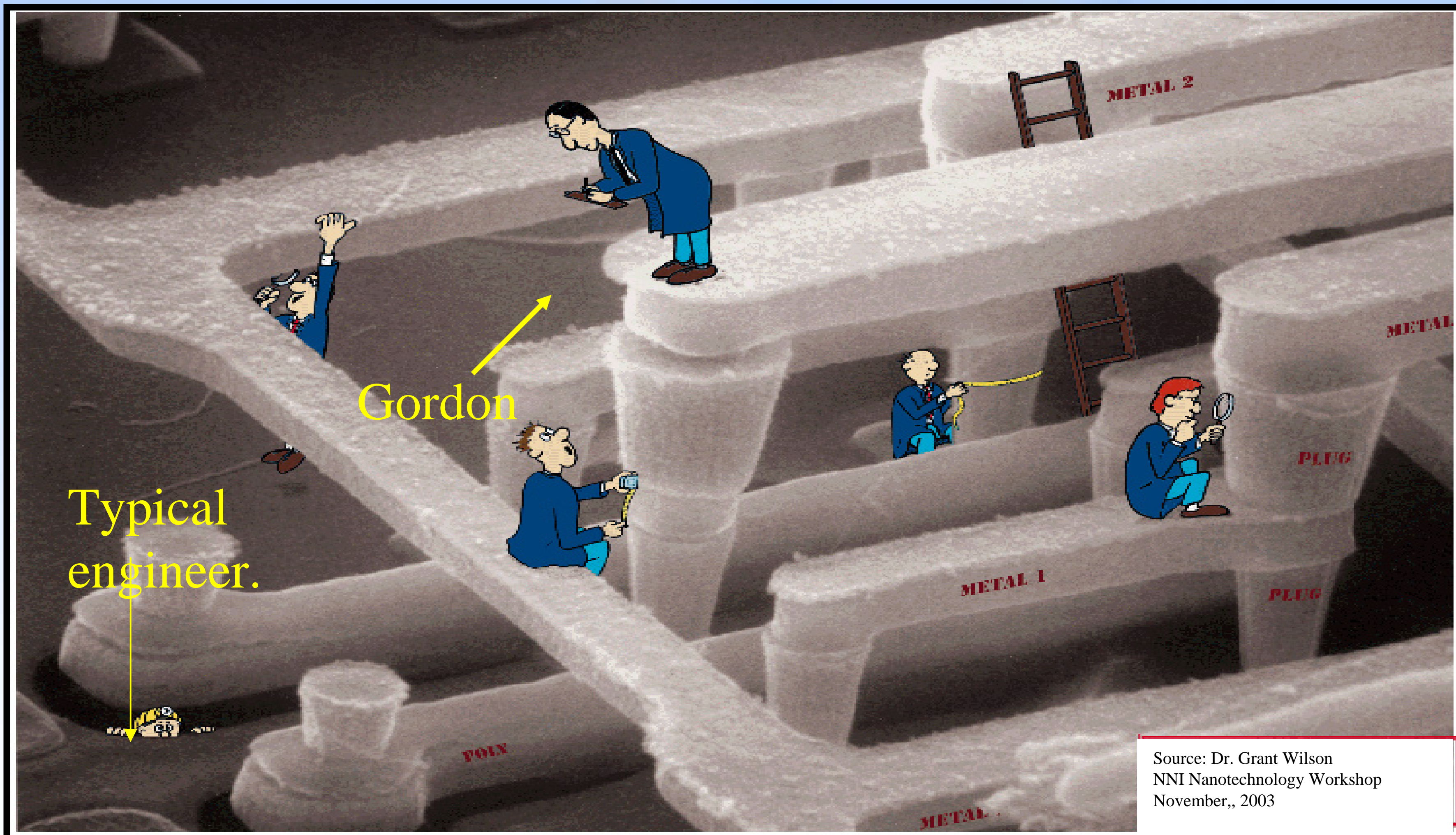
Agenda

- What is Silicon Nanotechnology?



- **CMOS Nanoscaling**
- Nonclassical CMOS
- Novel Devices
- Summary

CMOS Nanoscaling….Extending Moore's Law



New Materials, Devices Extend Si Scaling

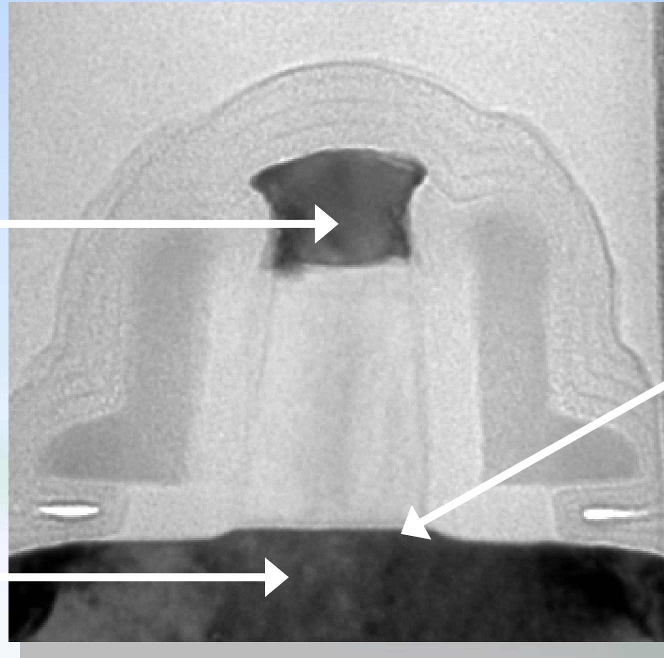
Changes Made

Gate

Silicide added

Channel

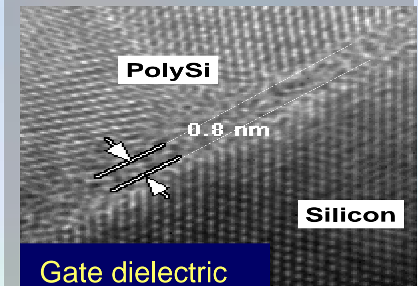
Strained silicon



Transistor

Future Options

High-k gate dielectric



Gate dielectric less than 3 atomic layers thick

Source: Intel

Source: Intel

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New Materials, Devices Extend Si Scaling

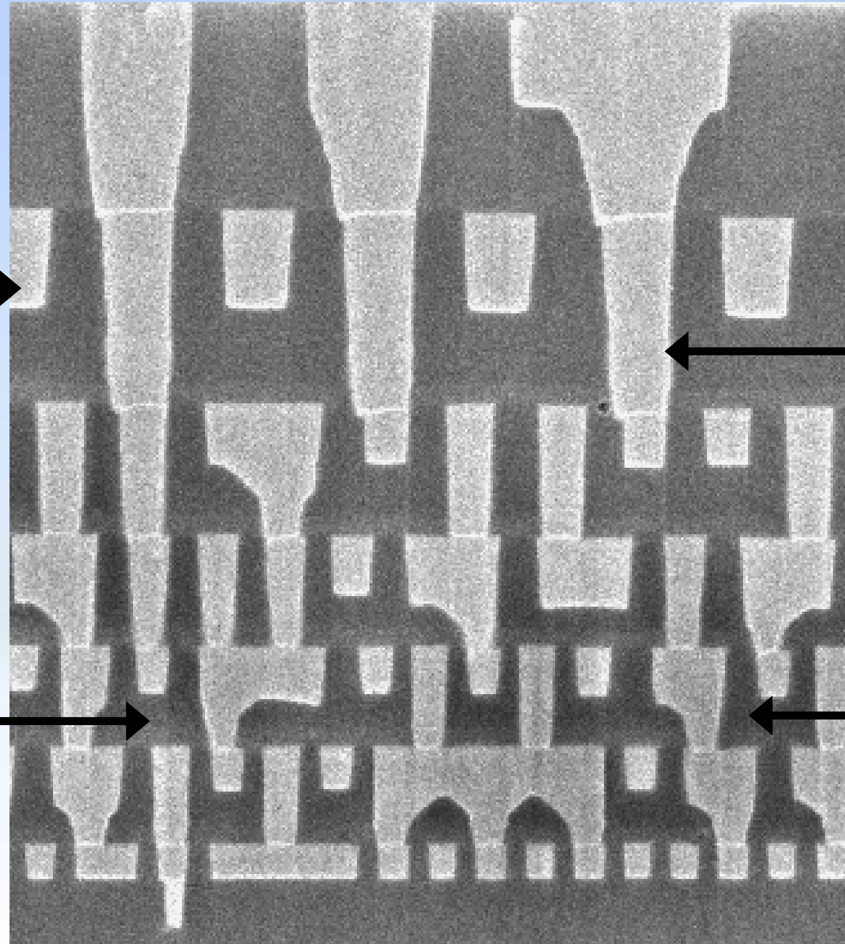
Changes Made

Metal lines

Al → Cu

Insulating dielectric

SiO_2 → SiOF → CDO (low-k)



Interconnects

Source: Intel

Future Options

New Thinner Barrier Layers

Ultra Low-k Dielectric

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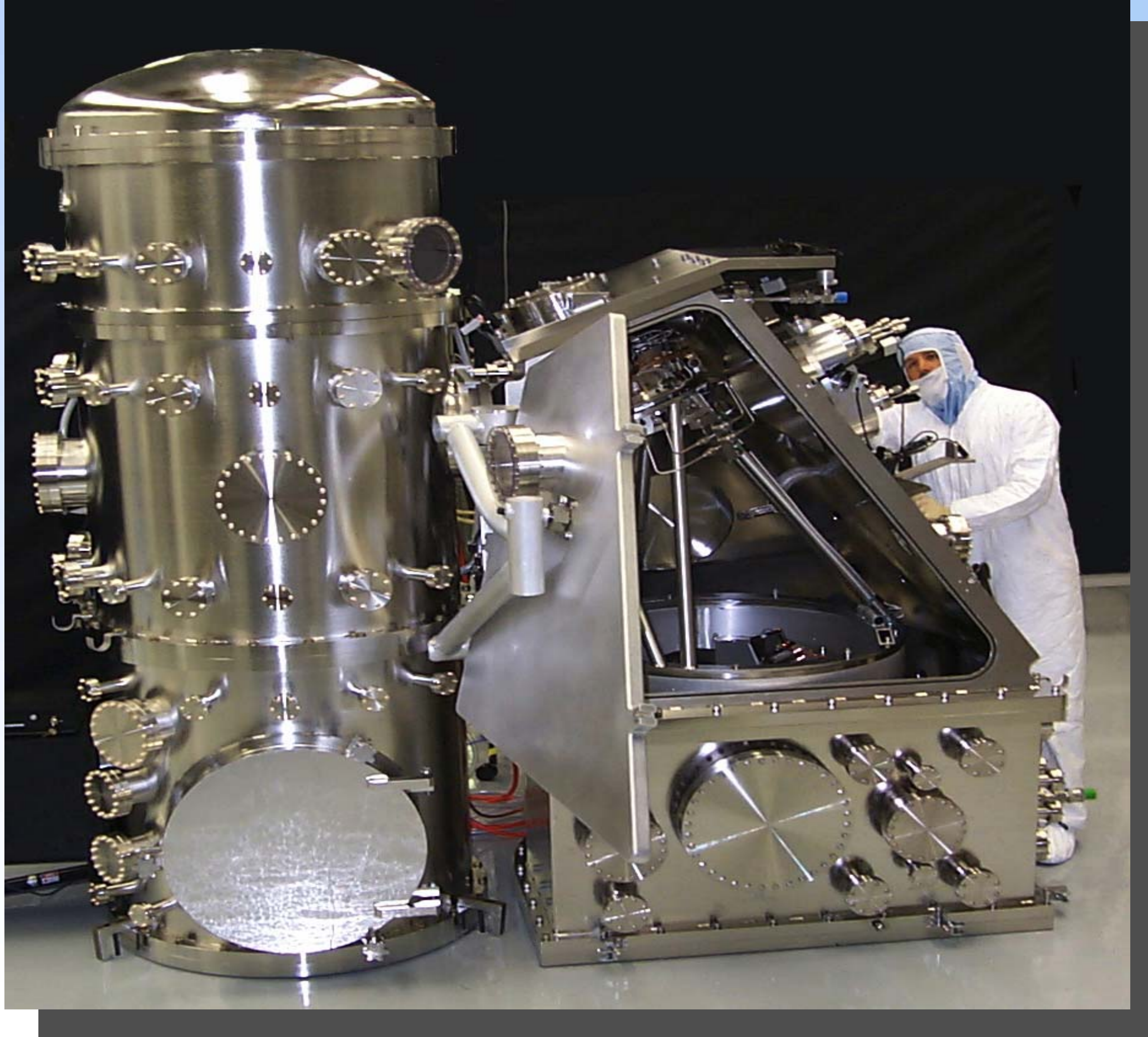
EUV LLC Consortium Demonstrates EUVL with Prototype Exposure Tool

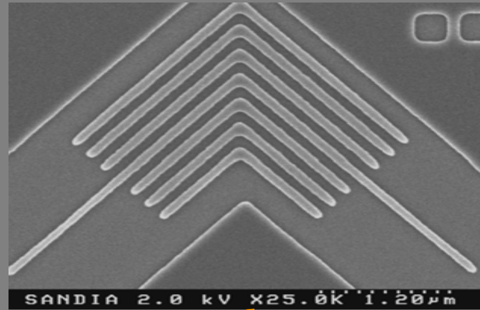


Source: Sandia

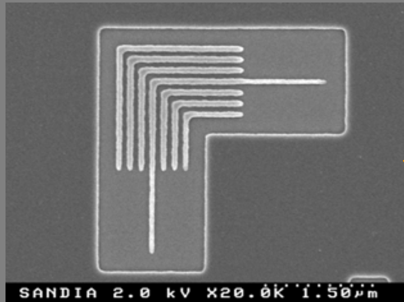
EUV Lithography - Full Field ETS Images

(using 0.1 NA system)

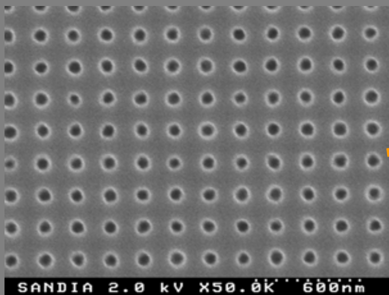
100 nm Elbows 1:1

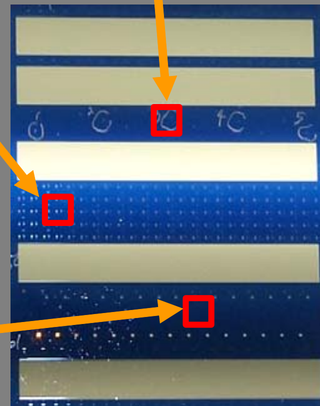


80 nm Elbows 1:1

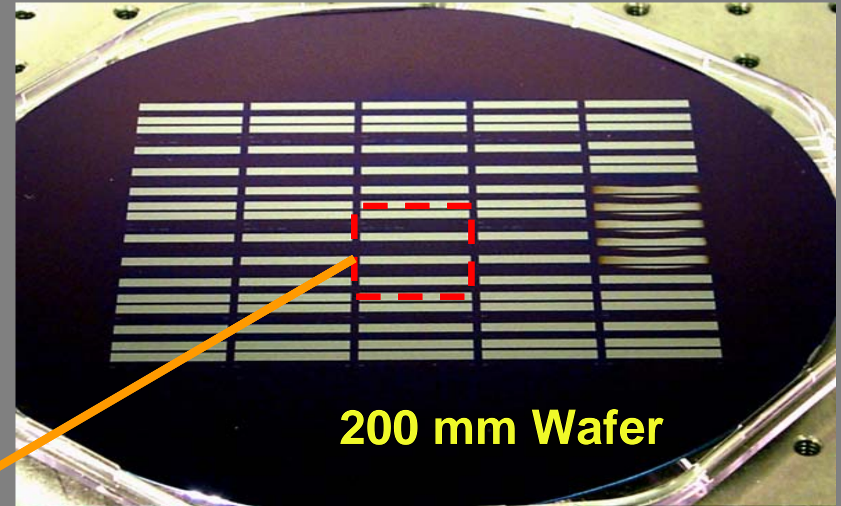


100 nm contacts 1:1

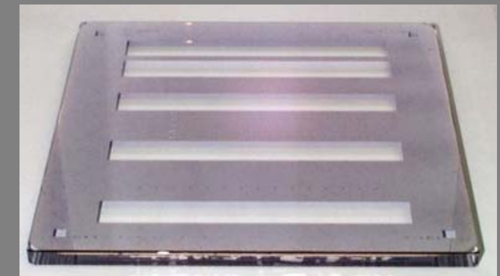




24 x 32.5 mm^2 field



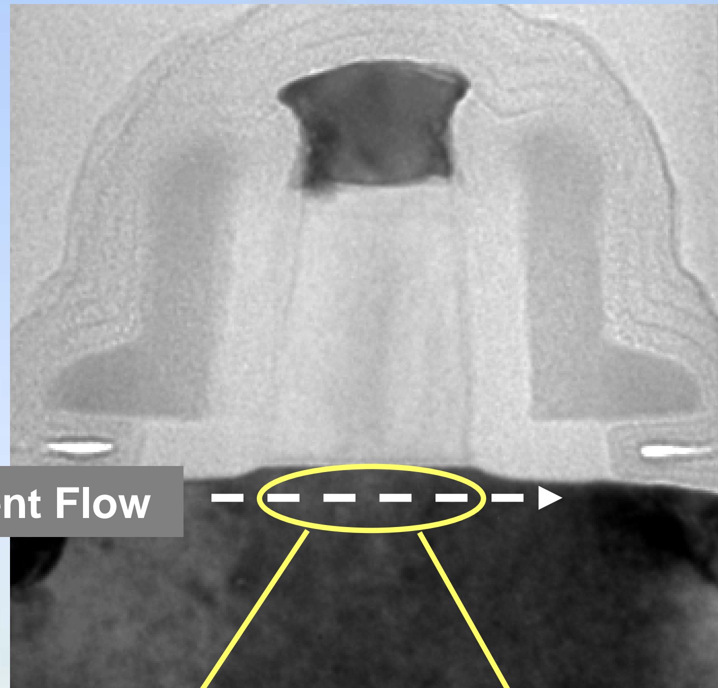
4x5 matrix



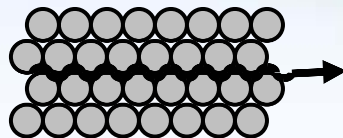
152 mm^2, 4X Reflective Mask

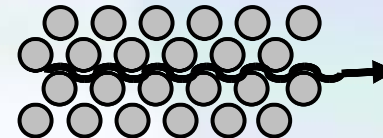
Printing 80 nm images at 0.1 NA is equivalent to printing 32 nm with 0.25 NA production system

Strained Silicon Transistors



Normal electron flow





Faster electron flow

Normal Silicon Lattice

Strained Silicon Lattice

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Source: Intel

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Strained Silicon Transistors

Strained silicon benefits

- Strained silicon lattice increases electron and hole mobility in transistor channels
- Greater mobility results in 10-20% increase in transistor current flow (drive current)
- Increased drive current = increased transistor performance
- Both NMOS and PMOS transistor performance improved

Strained silicon process

- Intel's strained silicon process is unique in the industry
- No detriments to transistor short channel behavior or junction leakage
- The added process steps increase total processing cost by only ~2%

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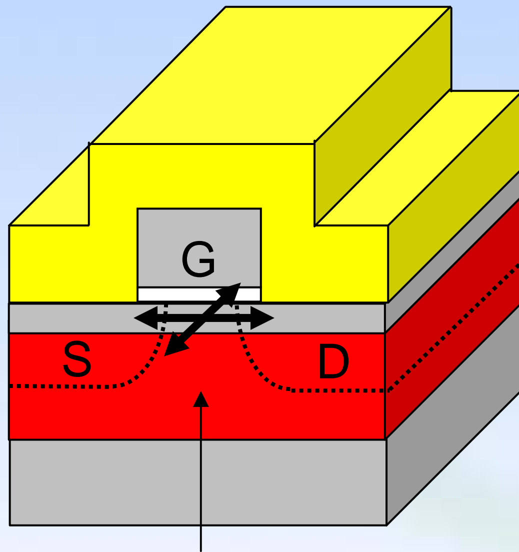
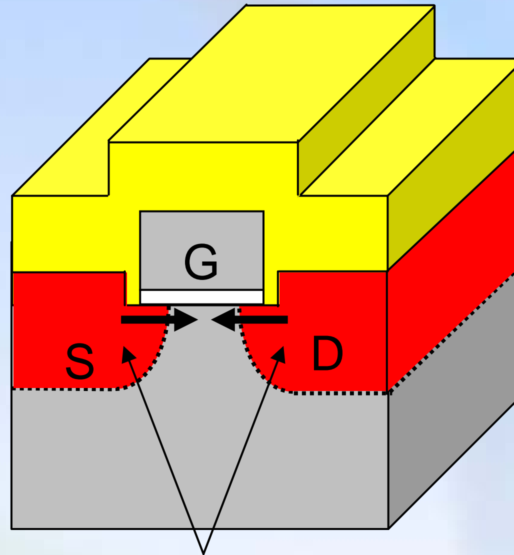
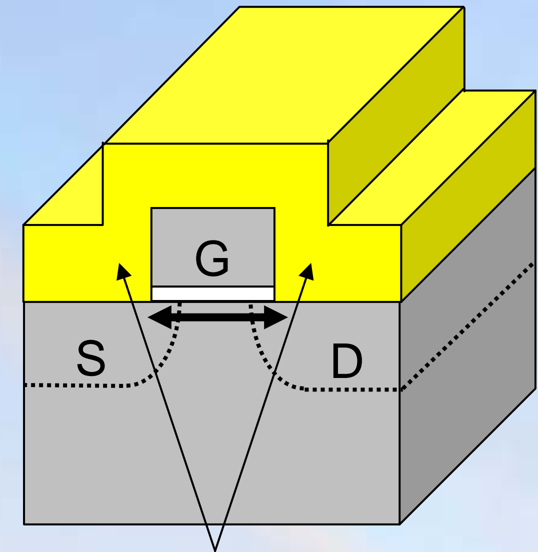
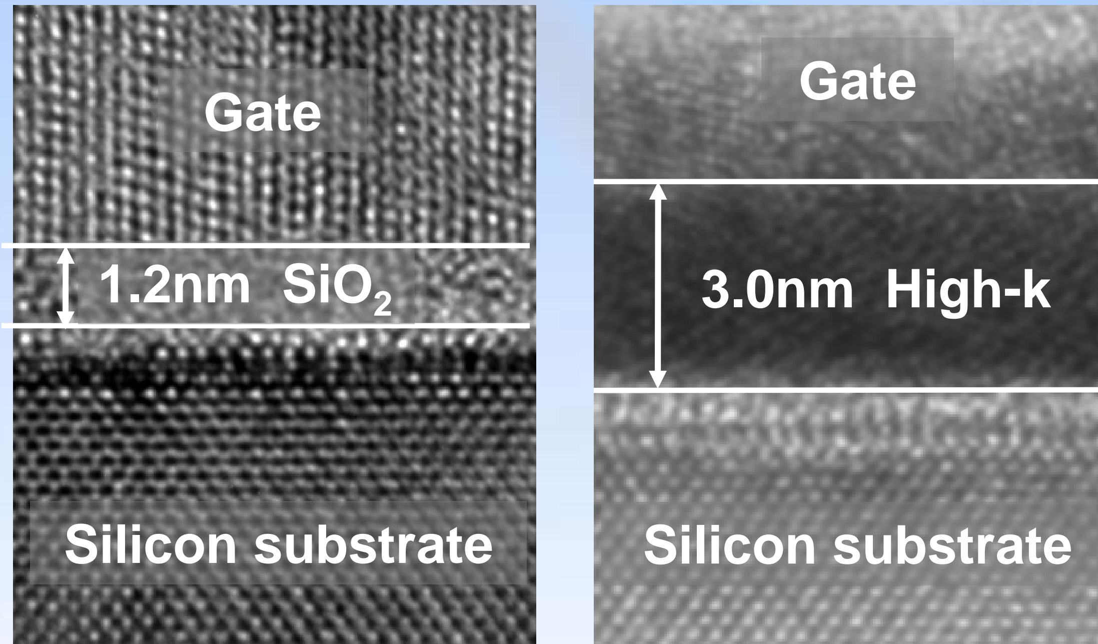
Transistor Strain Techniques

Traditional Approach	Intel's 90nm Technology	
		
Graded SiGe Layer	Selective SiGe S-D	Tensile Si_3N_4 Cap
Biaxial Tensile Strain	Uniaxial Compressive Strain for PMOS	Uniaxial Tensile Strain for NMOS

High-K Gate Dielectric

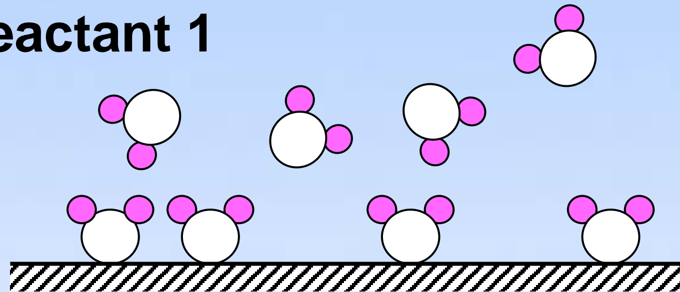


	90nm process	High-k
Capacitance:	1.0x	1.6x
Leakage:	1.0x	< 0.01x

Source: Intel

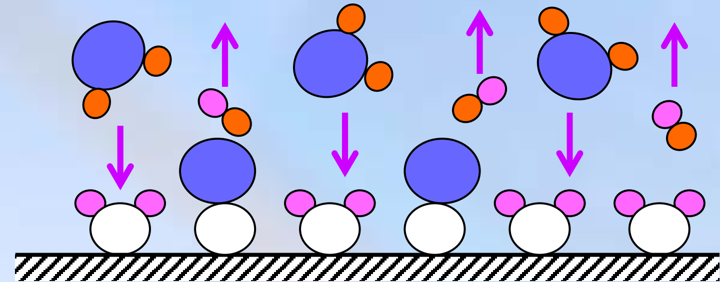
High-K Gate Dielectric Formed Using Atomic Layer Chemical Vapor Deposition

Reactant 1



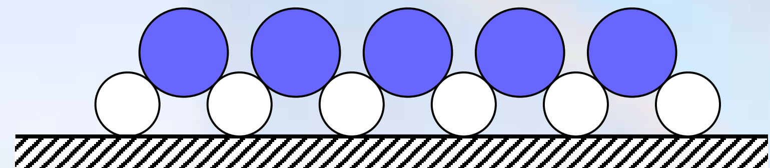
Step 1

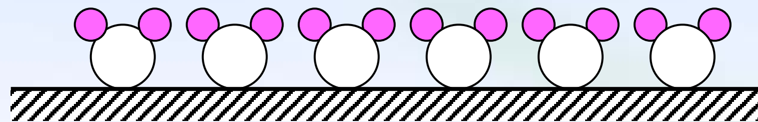
Introduce reactant 2



Step 3

Final film





Step 2

Step 4

- "Self-assembly process" ready for manufacturing
- Sequential introduction of precursors molecules
- Allows for precise building of the dielectric film

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Source: Intel

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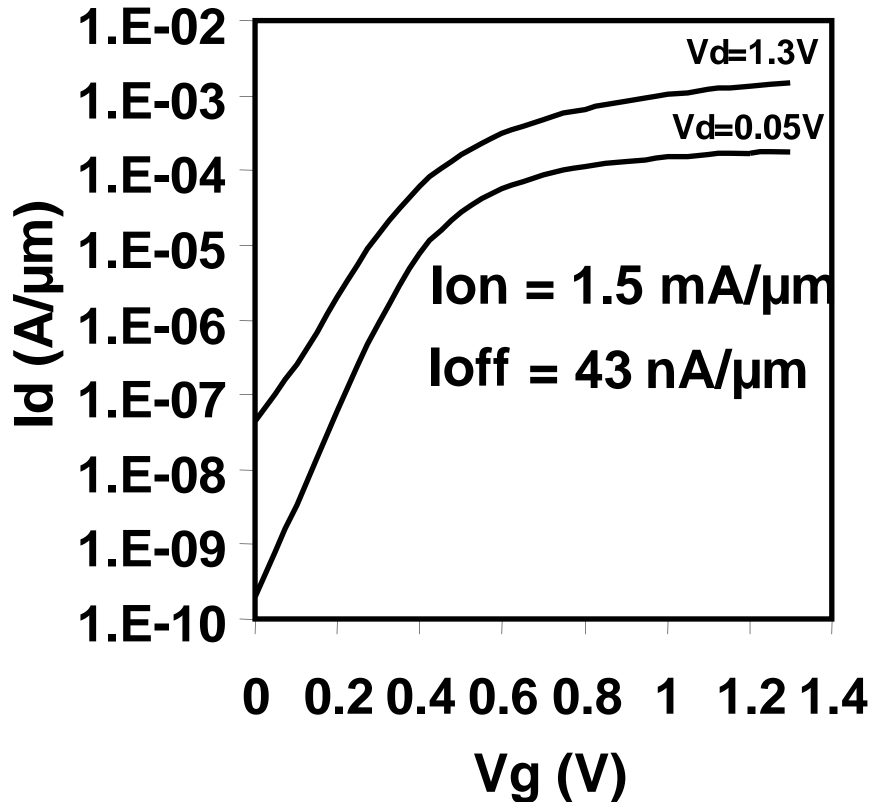
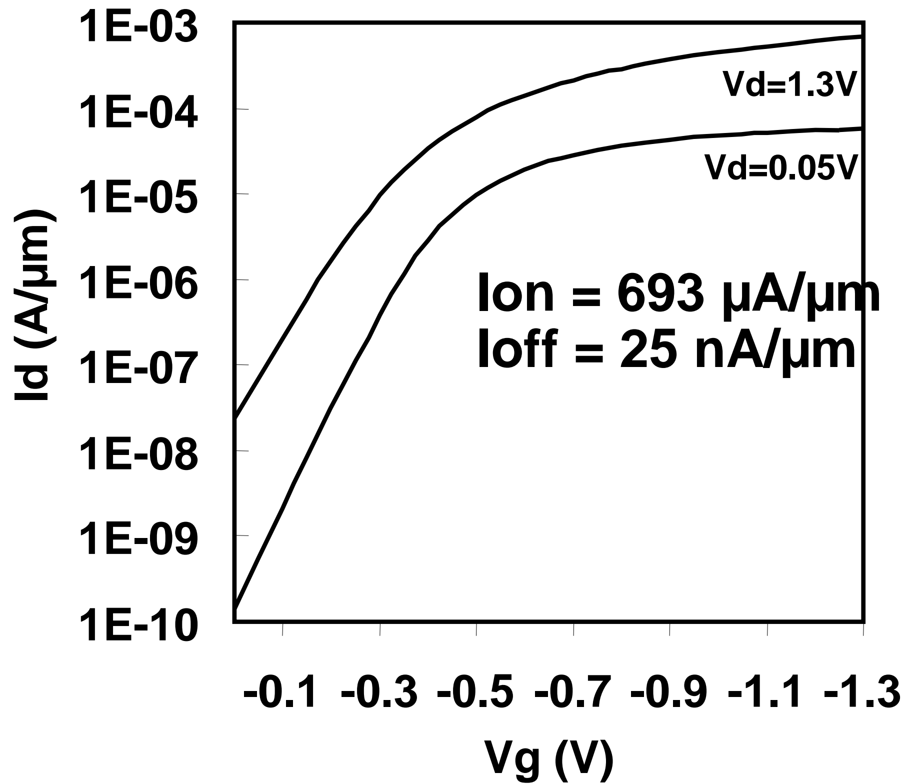
High-K/Metal-Gate Achieved Recording-Setting Performance



NMOS Transistor



PMOS Transistor

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Source: Intel

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Continuation of Moore's Law

Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268	P1270
1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25µm	0.18µm	0.13µm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/300	300	300	300	300	300
Inter-connect	Al	Al	Cu	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal	Metal

Source: Intel

Introduction targeted at this time

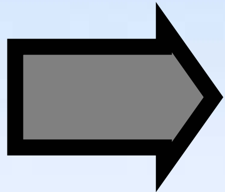
Subject to change

Intel found a solution for* High-k *and metal gate

Agenda

What is Silicon Nanotechnology?

Nanoscaling

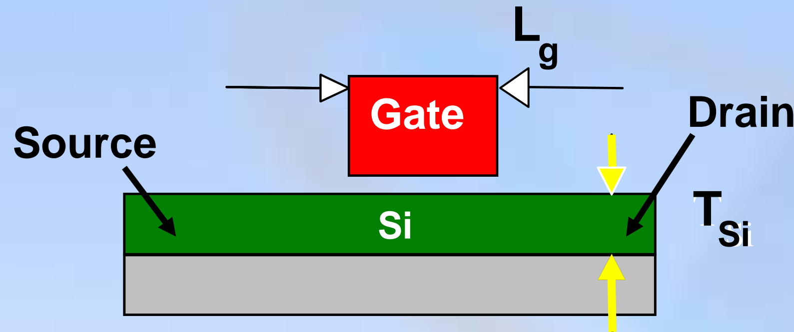


Nonclassical CMOS

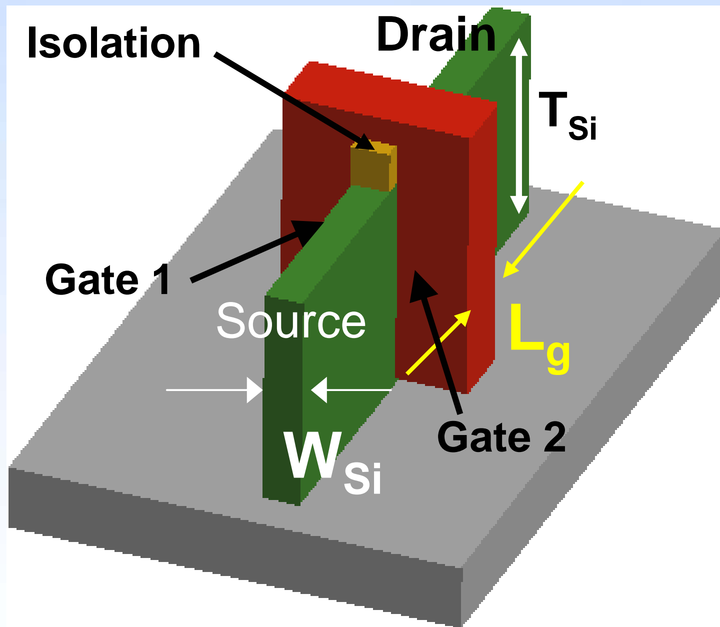
Novel Devices

Summary

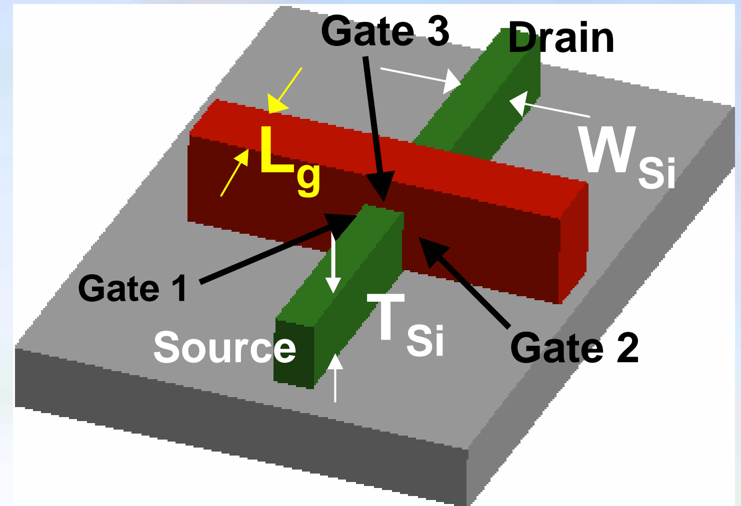
Transistor Architectures



(Planar)



Double-gate (e.g. FINFET)
(Non-Planar)



Tri-gate
(Non-Planar)

Source: Intel

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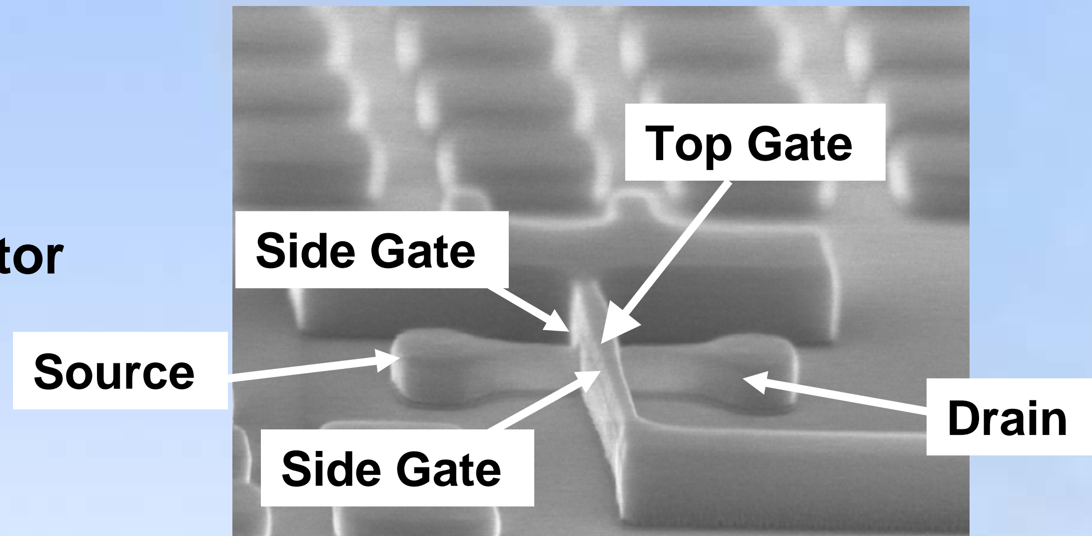
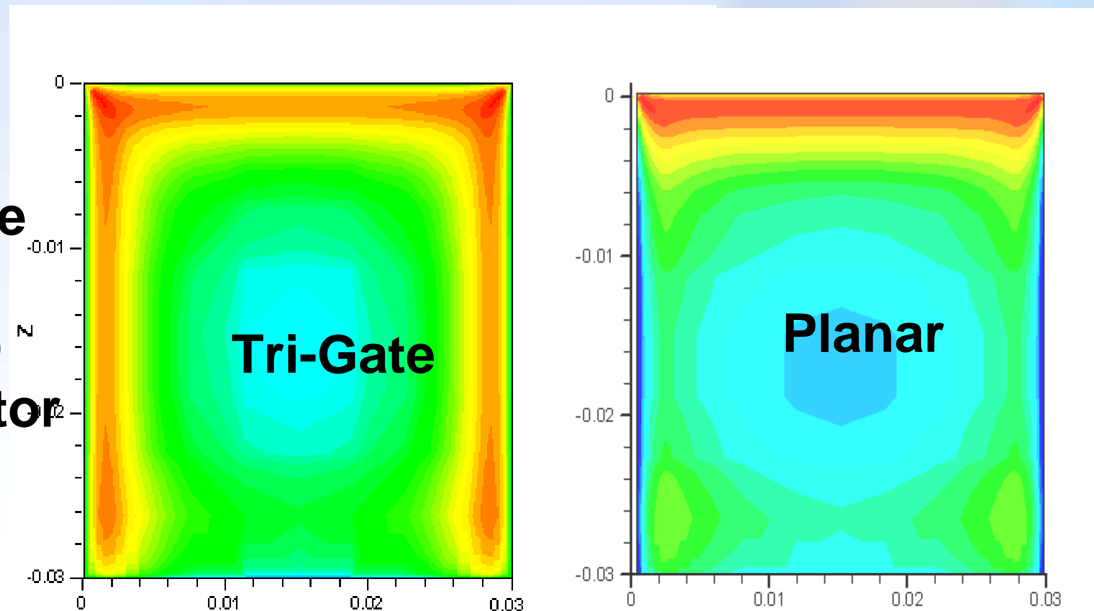
Tri-Gate Transistor

Actual photo
30nm tri-gate transistor



Simulation
Cross-section of silicon channel shows much more current flow (indicated by red) in tri-gate transistor than in planar transistor



Source: Intel

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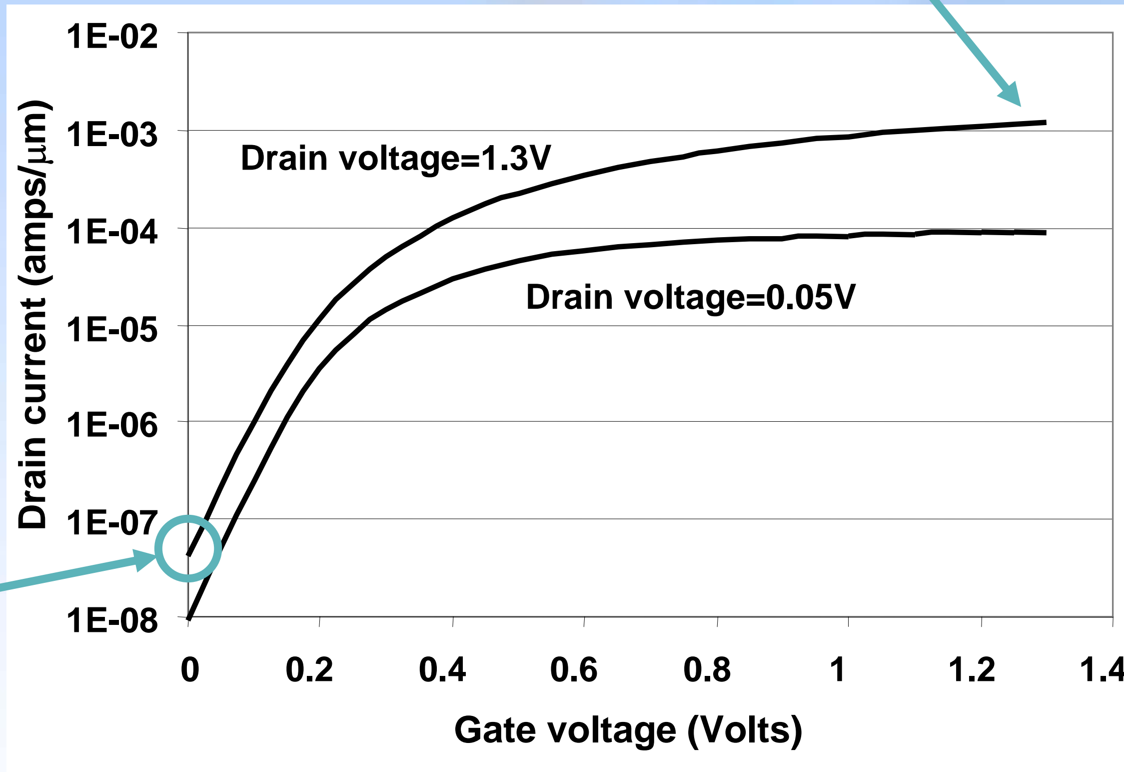
World Record Non-Planar Performance

Very high drive current at saturation, 1.23 mA/μm



Very low leakage, 40nA/μm

Tri-gate transistor exhibits excellent device characteristics

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Source: Intel

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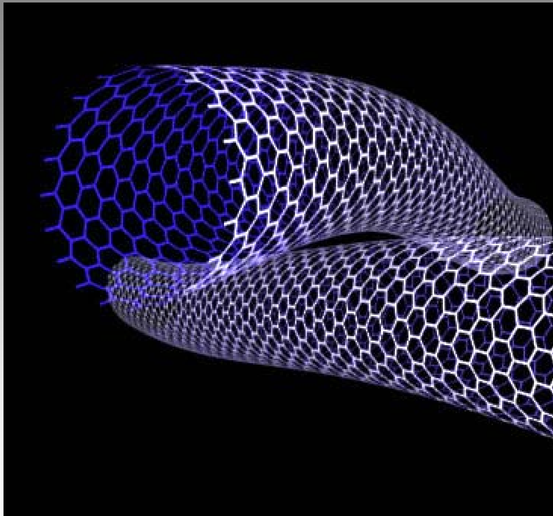
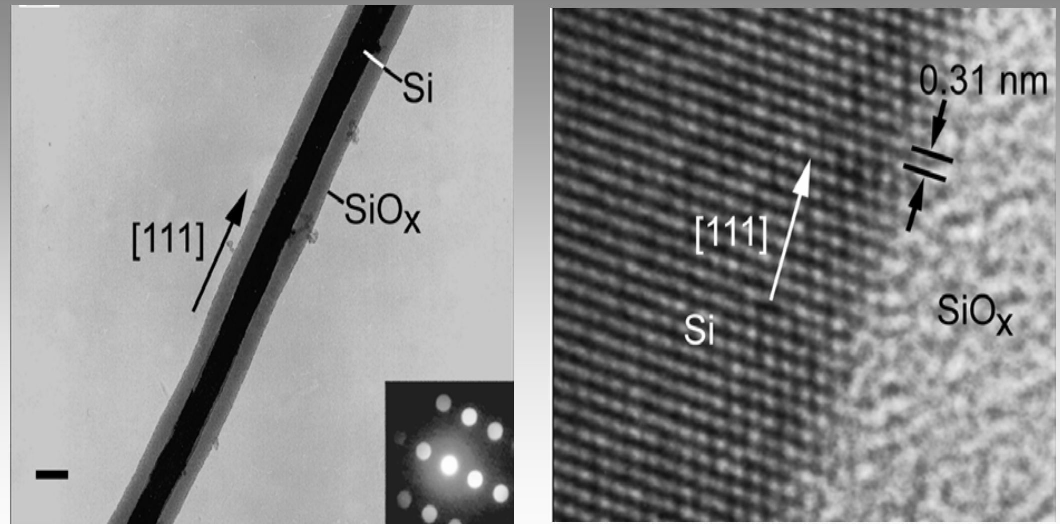
Non-Classical CMOS

- Many options including nanotubes/nanowires
- Collaborations with universities in progress

Carbon Nanotube



Silicon Nanowire



Source: Morales & Lieber, Science **279**, 208 (1998)

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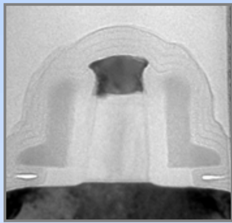
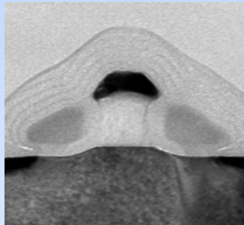
CMOS Device Scaling Demonstration

90nm Node
2003



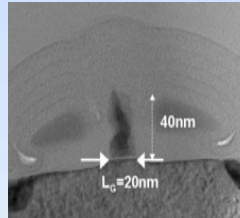
50nm Length
(IEDM2002)

65nm Node
2005



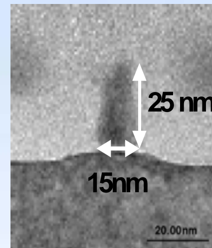
30nm
Prototype
(IEDM2000)

45nm Node
2007



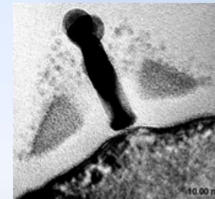
20nm Prototype
(VLSI2001)

32nm Node
2009



15nm Prototype
(IEDM2001)

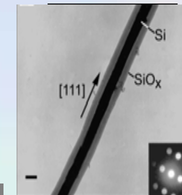
22nm Node
2011



10nm Prototype
(DRC 2003)

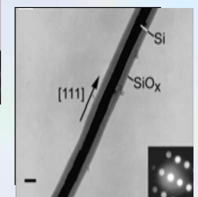
16 nm node
2013

11nm node
2015



TBD

8 nm node
2017



TBD

Si nanowires??

Integration of nanotubes, nanowires onto Si by end of this decade will extend device scaling well into next decade

Source: Intel; Morales and Lieber Science, **279**, 208, 1998

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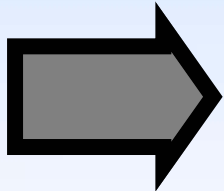
Agenda

What is silicon Nanotechnology?

Nano Scaling

Non classical CMOS



Novel Devices

Summary

Novel Devices

- Many device options….
- Compatibility with CMOS for evolutionary introduction
- Directed or self assembly of arrays???
  - Defect density or purity required….
- Self correcting architectures??
- Nanotechnology needs a richer suite of functionality…

Collaboration between industry, universities, and government is essential

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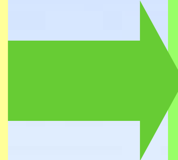
Novel Devices
What are we looking for?

- Required characteristics:
  - Scalability
  - Performance
  - Energy efficiency
  - Gain
  - Operational reliability
  - Room temp. operation
- Preferred approach:
  - CMOS process compatibility
  - CMOS architectural compatibility



Alternative state variables

- **Spin–electron, nuclear, photon**
- **Phase**
- **Quantum state**
- **Magnetic flux quanta**
- **Mechanical deformation**
- **Dipole orientation**
- **Molecular state**

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Intel Involved in University Research

Intel-supported Nanotechnology Research at Universities

Colorado
Illinois
Ohio
Ireland
New York
Oregon
Mass
Israel
California
Tennessee
Arizona
Texas
Florida

Intel engaged in >300 SRC* projects at 50 universities

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*Semiconductor Research Corp

Agenda

- What is Silicon Nanotechnology?
- Nano Scaling
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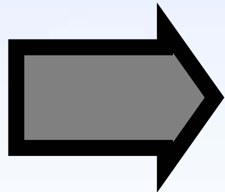

- Summary

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Summary

- **Nanotechnology is here today in "state of the art" high speed Si CMOS process technologies**
- **Si nanotechnology process scaling/convergence will continue indefinitely.**
- **New architectures will further extend silicon scaling.**
- **Novel technologies being investigated and may be integrated with silicon technology mid-next decade**
- **Compatability with CMOS (product development spectrum) will leverage existing learning and enable earlier production of novel devices**

Please fill out the Session Evaluation Form.

Thank You!

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