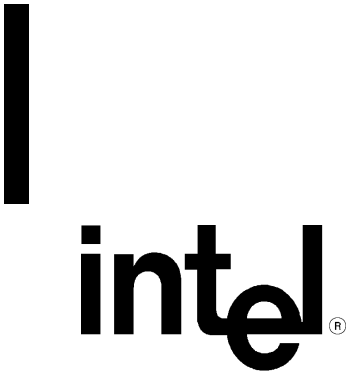

Enterprise Server Group

Intel NL440BX/T440BX UP Server
Technical Product Specification

Version 2.0
Order Number: 243716-002
June, 1999

The Intel NL440BX/T440BX UP Server baseboard may contain design defects or errors known as errata. Characterized errata that may cause the NL440BX/T440BX UP Server baseboard's behavior to deviate from published specifications are documented in the NL440BX/T440BX UP Server Specification Update.

Revision History

Revision	Revision History	Date
Rev 1.0	Initial release of the NL440BX Server Technical Product Specification.	6/98
Rev 2.0	Added Errata section, added T440BX, updated connector chart, added chassis intrusion pinout, corrected for trademark issues	6/99

*NOTE**: If printing this document from an electronic file, use a PostScript printer with the appropriate PostScript print driver to insure the drawings print clearly.***

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1. Introduction

This document describes the architecture of the NL440BX/T440BX UP Server baseboard. The Intel NL440BX/T440BX UP Server is an entry-level server platform based on the Intel® 440BX AGPset and featuring the Pentium® II/Pentium® III processor. It follows the "Extended ATX" form factor for baseboard design and is optimized for 100 MHz system bus operation. There is an extensive feature list for the NL440BX/T440BX UP Server baseboard including:

- Volume server, workstation, or desktop platform based on the Pentium II/ Pentium III processor. On the NL440BX/T440BX UP Server, this processor operates with a 100 MHz or 66 MHz system bus. The NL440BX/T440BX UP Server baseboard provides one 'SC242' connector.
- System design based on Intel® 440BX AGPset and PIIX4 devices.
- Main memory interface supporting up to 768 MB of PC/100-compliant or PC/66-compliant commodity SDRAM DIMMs in both ECC or non-ECC.
- PCI I/O system, compliant with revision 2.1 of the PCI specification. PCI interface is provided by the Intel 440BX host bridge
- A.G.P. connector
- PCI SCSI controller providing one Ultra wide SCSI channel.
- PCI 10/100 Mbit Ethernet controller with integrated physical layer.
- High performance 2D PCI video controller with 2 MB of video memory onboard.
- PCI IDE controller (in PIIX4) providing dual independent Ultra DMA/33 IDE interfaces, each able to support 2 IDE drives.
- 4 PCI expansion slots.
- 2 ISA expansion slots (1 shared with a PCI slot).
- Compatibility I/O device integrating floppy, dual serial and parallel ports.
- Integration of server management features, including thermal, voltage, fan, and chassis monitoring into one controller and the Emergency Management Port (EMP) feature.
- Universal Serial Bus (USB) support.
- Flash BIOS support for all of the above.

The following diagram shows the functional blocks of the NL440BX/T440BX UP Server baseboard and the plug-in modules that it supports.

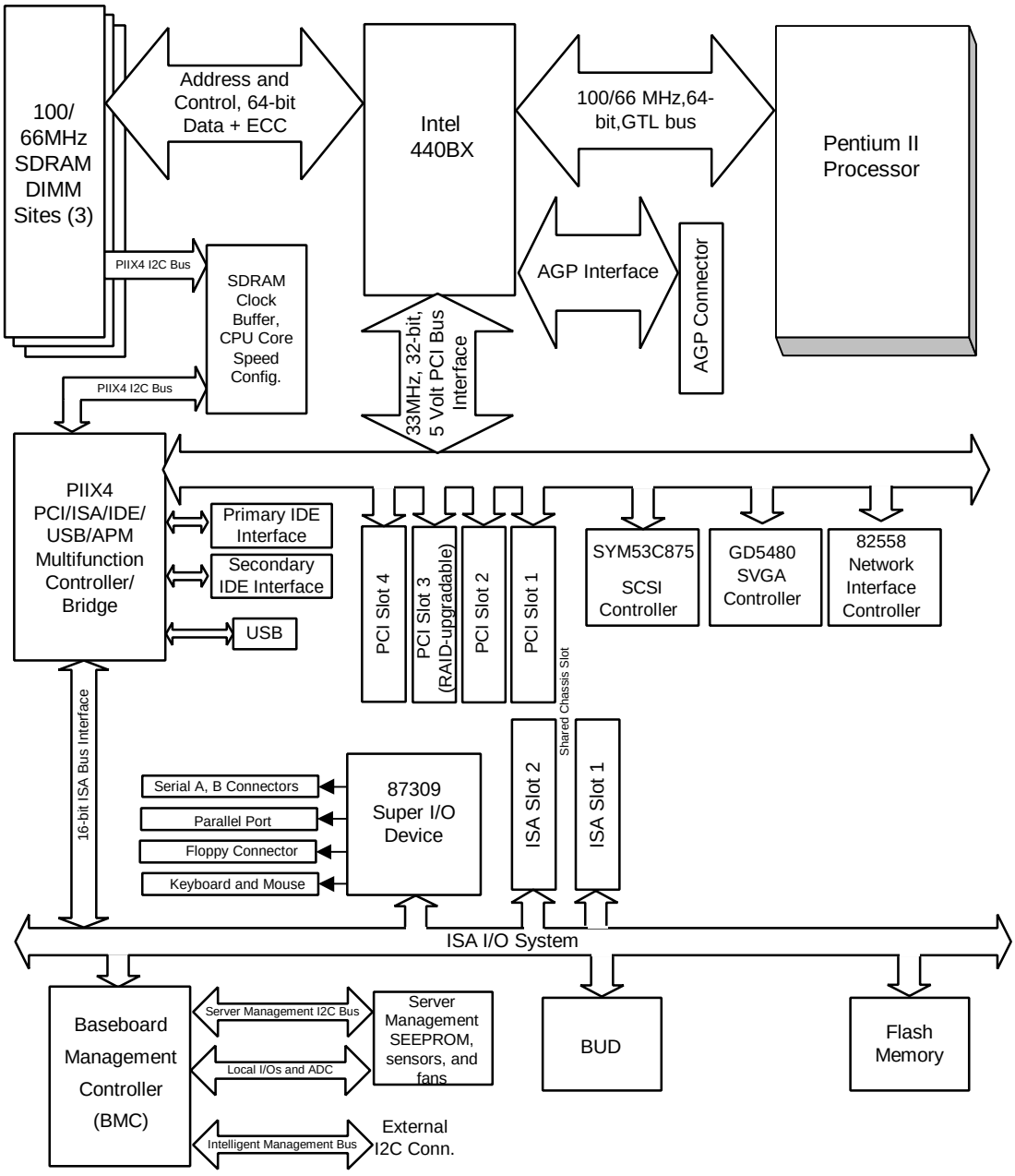


Figure 1. NL440BX/T440BX UP Server Block Diagram

1.1 Baseboard Architecture Overview

The NL440BX/T440BX UP Server baseboard architecture is based on a design supporting single processor operation using a Pentium® II processor SECC or SECC2 and Pentium ® III processor cartridges and the Intel 440BX PCIset. The NL440BX/T440BX UP Server provides a PCI-based I/O subsystem containing embedded devices for video, NIC, SCSI, and IDE, along with an ISA bridge to support compatibility devices. Additionally, the baseboard provides server management and monitoring hardware support, single processor, and PC/AT compatible operation. This section provides an overview of the NL440BX/T440BX UP Server subsystems:

Support for one Pentium II processor SECC or SECC2 and Pentium III processor cartridges.

- One "SC242" edge connector operating at 100 MHz or 66 MHz.
- One embedded VRM 8.1-compliant voltage regulator for the SEC cartridge.

Intel 440BX AGPset providing processor host interface, PCI bridge, and memory controller with 100 MHz or 66MHz pathway to memory.

3 DIMM sockets that support PC/100 and PC/66 compliant SDRAM devices.

A.G.P. connector:

- Complies with the A.G.P 1.0 specification
- Support for +3.3V A.G.P. 66/133 MHz devices
- Synchronous coupling to the host-bus frequency

33 MHz, 5V PCI segment with four expansion connectors and four embedded devices.

- PCI/ISA/IDE Accelerator (PIIX4) for PCI-to-ISA bridge, and PCI IDE interface, USB controller, and power management controller.
- PCI video controller - Cirrus Logic GD5480*.
- PCI SCSI controller - Symbios SYM53C875*, supporting wide SCSI interface onboard.
- "RAID-upgradeable" PCI slot with special interrupt capabilities supporting low cost 0 channel RAID cards by AMI and Mylex.
- PCI Network Interface Controller (NIC) with integrated physical layer - Intel 82558.

ISA bus segment with two expansion connectors and four embedded devices.

- National Semiconductor 87309 SuperI/O* controller providing all PC-compatible I/O (floppy, parallel, serial, keyboard, mouse).
- Flash memory for system BIOS.
- Server management host interface.
- BUD (Basic Utility Device) implemented using an Altera PLD.

Single server management microcontroller providing monitoring, alerting, and logging of critical system information from embedded sensors on baseboard. The NL440BX/T440BX UP Server includes the Emergency Management Port (EMP) interface for remote access to this information, along with reset and power control, via external modem.

Pentium® II/Pentium® III Processor

The NL440BX/T440BX UP Server is optimized to function with the Pentium® II processor SECC or Pentium® III processor cartridges. The Pentium II/ Pentium III processor core/L1 cache appears on one side of a preassembled printed circuit board, approximately 2.5" x 5" in size, with the L2 cache on the backside. The L2 cache and processor core/L1 cache connect using a private bus isolated from the processor host bus. This Pentium II/Pentium III processor L2 cache bus operates at half of the processor core frequency. To compensate for the cache bus speed, the L1 data and code caches are 16 KB.

The Pentium II/Pentium III processor package follows Single Edge Contact cartridge (SECC) form factor and provides a thermal plate for heatsink attachment with a plastic cover located opposite the thermal plate.

The Pentium II/Pentium III processor core internal frequencies supported include 66MHz (233, 266, 300, 333) and 100MHz (350, 400, 450, 500, 550). The initial baseboard design uses the 350 MHz version. The 512 KB secondary (L2) cache runs at half the core frequency.

VRM

The NL440BX/T440BX UP Server provides one embedded VRM 8.1-compliant voltage regulator (DC-to-DC converter) to provide VCC_P to the Pentium II/Pentium III processor. The VRM automatically determines the proper output voltage as required by the processor.

440BX Host Bridge / Memory Controller

The NL440BX/T440BX UP Server architecture is designed around the Intel 440BX AGPset. This device provides 100 MHz processor host bus interface support, DRAM controller, PCI bus interface, AGP interface, and power management functions. The host bus/memory interface in the Intel 440BX AGPset is optimized for 100 MHz operation, using 100 MHz SDRAM main memory. The PCI interface is PCI 2.1-compliant, providing a 33 MHz / 5V signaling environment for embedded controllers and slots in the single PCI segment on the NL440BX/T440BX UP Server. The Intel 440BX AGPset memory interface supports up to 1 GB of memory, however, the NL440BX/T440BX UP Server only supports up to 768 MB of ECC memory, using registered PC/100 compliant Synchronous DRAM (SDRAM) devices on DIMM plug-in modules. ECC can detect and correct single-bit errors, and detect multiple-bit errors.

Memory

Support for both 100 MHz PC/100-compliant and 66MHz PC/66-compliant SDRAM DIMMs is available on the NL440BX/T440BX UP server board. Two types of memory devices on the DIMMs are supported: registered or unbuffered. A list of NL440BX/T440BX qualified DIMMs will be available on the Intel World Wide Web site and Intel ServerBuilder website.

The baseboard provides three DIMM sites. Both ECC (72-bit) and Non-ECC (64-bit) DIMMs are specified for use in the NL440BX/T440BX UP Server system, however Intel recommends the use of ECC memory server environment.

The PIIX4 provides a local SM bus interface to SDRAM DIMM information, SDRAM clock buffer control, and processor core speed configuration. The BIOS code uses this interface during auto-configuration of the processor/memory subsystem, as part of the overall server management scheme.

A.G.P.

A.G.P. is a high-performance bus for graphics-intensive applications, such as 3D applications. A.G.P., while based on the *PCI Local Bus Specification, Rev. 2.1*, is independent of the PCI bus and is intended for exclusive use with graphical display devices. A.G.P. overcomes certain limitations of the PCI bus related to handling a large amount of graphics data with the following features:

- Pipeline memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for near 100 percent bus efficiency
- AC timing for 133 MHz data transfer rates allowing real data throughput in excess of 500 MB/sec

PCI I/O Subsystem

The primary I/O bus for the NL440BX/T440BX UP Server is PCI, compliant with revision 2.1 of the PCI specification. The PCI bus on the NL440BX/T440BX UP Server supports embedded SCSI, network control, video, and a multi-function device that provides a PCI-to-ISA bridge, bus master IDE controller, Universal Serial Bus (USB) controller, and power management controller. The PCI bus also supports four slots for full-length PCI add-in cards (one shared with an ISA slot).

PCI SCSI Subsystem

The embedded SCSI controller on the NL440BX/T440BX UP Server is the Symbios SYM53C875 controller. This device provides one Ultra wide SCSI interface. PCI slot 3 is RAID-upgradeable, providing additional support for a Zero channel low cost RAID adapter.

PCI Network Interface Subsystem

The network interface on the NL440BX/T440BX UP Server is implemented using an Intel 82558, which provides a 10/100 Mbit Ethernet interface supporting 10Base-T and 10Base-TX, integrated with an RJ45 physical interface. The Intel 82558 controller also provides Wake-On-LAN functionality if the power supply supports a minimum of 800mA of 5V standby current (configurable via the baseboard jumper).

PCI Video Subsystem

The embedded SVGA-compatible video controller on NL440BX/T440BX UP Server is a Cirrus Logic GD5480 SGRAM GUI Accelerator. The SVGA subsystem also contains 2 MB of SGRAM (synchronous graphics RAM).

PCI-to-ISA Bridge, IDE/USB/PM Controller

The PIIX4 is a multi-function PCI device, with four distinct PCI controllers onboard: PCI-to-ISA bridge, PCI bus master IDE interface, USB host controller, and enhanced power management. The PIIX4 also integrates a real-time clock (RTC), 82C54 Timer/Counter, two 82C59 interrupt controllers, and dual 82C37 DMA controllers on-chip that support "distributed DMA" transfers as well as compatibility operation. The PIIX4 also provides general-purpose chip select decoding for BIOS, external RTC, and keyboard controller. The integrated IDE controller supports up to four IDE devices in bus master mode at speeds up to 33 MB/s (Ultra DMA/33 operation). The USB controller is Universal Host Controller Interface (UHCI) compatible.

ISA I/O Subsystem

The NL440BX/T440BX UP Server contains a full-featured ISA I/O subsystem with two full length ISA slots (one shared with a PCI slot), and local ISA bus interface to embedded SuperI/O, Flash BIOS, Basic Utility Device (BUD), and server management features.

National 87309 SuperI/O Device

Compatibility I/O on the NL440BX/T440BX UP Server is implemented using a National PC87309VLJ component. This device integrates a floppy disk controller, keyboard and mouse controller, two enhanced UARTs, full IEEE 1284 parallel port, and support for power management. The controller provides separate configuration register sets for each supported function. Connectors are provided for all compatibility I/O devices.

Flash BIOS

The BIOS for the NL440BX/T440BX UP Server baseboard resides in an Intel 28F004S5 FlashFile Memory Family, 4 Mbit, symmetrically blocked (64 KB) flash device.

Server Management Subsystem

The NL440BX/T440BX UP Server incorporates a Dallas 82CH10 micro-controller as baseboard management controller (BMC). The BMC controls and monitors all server management features on the baseboard, and provides interface to two independent I^2C bus-based serial buses. This includes power supply on/off control, hard reset control, video blanking, watchdog timers and all temperature, voltage, fan and chassis intrusion monitoring. The BMC can be polled for current status, or configured to automatically send an alert message when an error condition is detected either manually or by software.

In addition, the NL440BX/T440BX UP Server baseboard provides a new server management feature: Emergency Management Port (EMP). When using an external modem or a direct connection, this allows remote reset, power up/down control, and access to the event log, or run-time information. This port also supports console redirection, and, with additional software support, the EMP can also be used to download firmware and BIOS upgrades.

Basic Utility Device

NL440BX/T440BX UP Server provides the Basic Utility Device (BUD) for SMI/NMI routing, and PCI arbitration expansion. The physical device is an Altera 7032 CPLD. Other features formerly handled by an external CPLD on previous servers, such as the host ISA interface to server management functions, now appear in the BMC.

1.2 Baseboard Placement Diagram

The following diagram shows the placement of major components and connector interfaces on the NL440BX/T440BX UP Server baseboard.

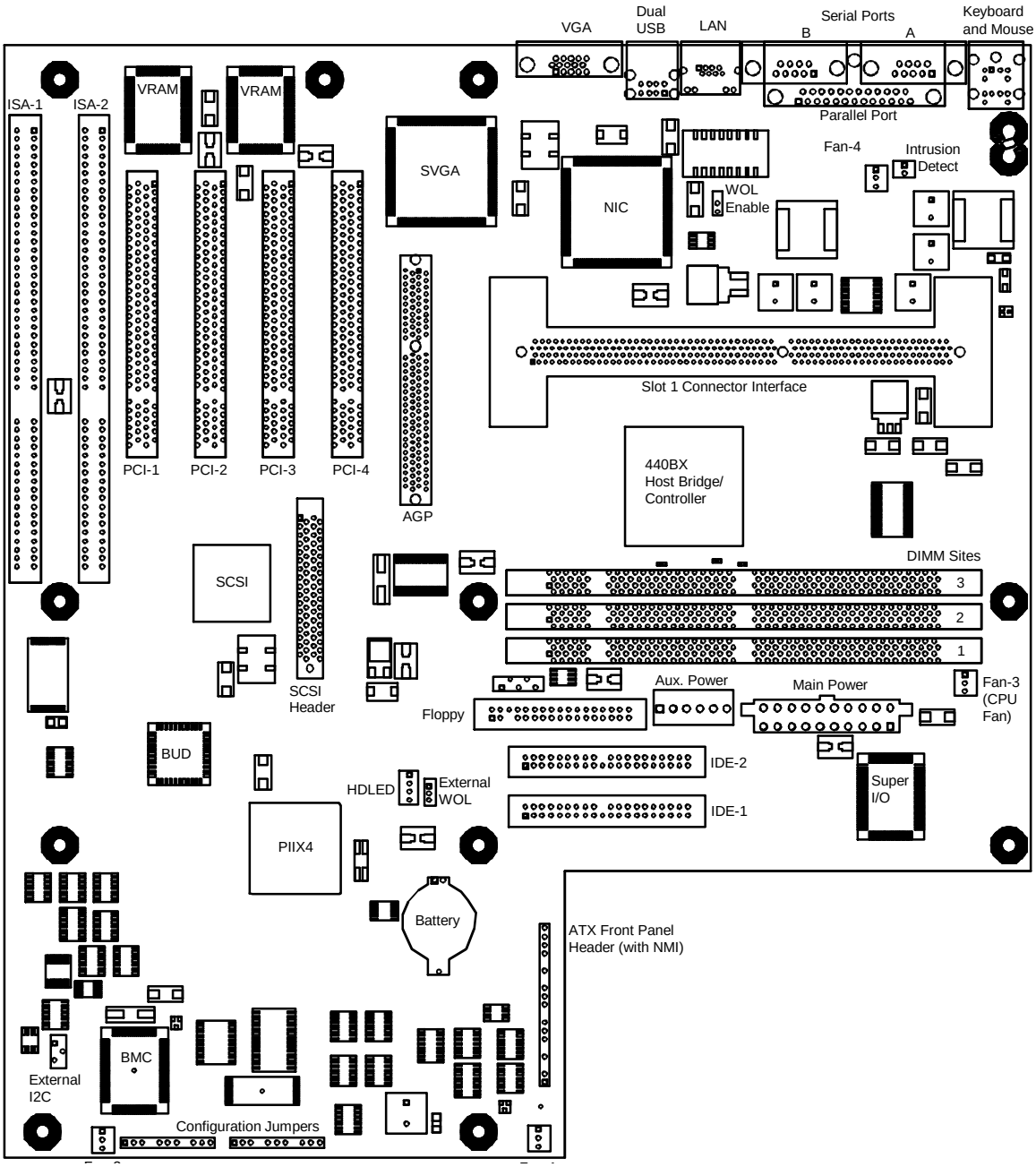


Figure 2. NL440BX/T440BX UP Server Baseboard Layout (FAB 4.0)

2. Functional Architecture

The following diagram illustrates the functional architecture of the NL440BX/T440BX UP Server baseboard, with lines showing the major functional blocks. This chapter describes the operation of each block and associated circuitry and specifies the pinouts of related connectors. Additionally, this chapter provides high-level descriptions of functionality distributed between functional blocks (e.g., interrupt structure, clocks, resets, and server management).

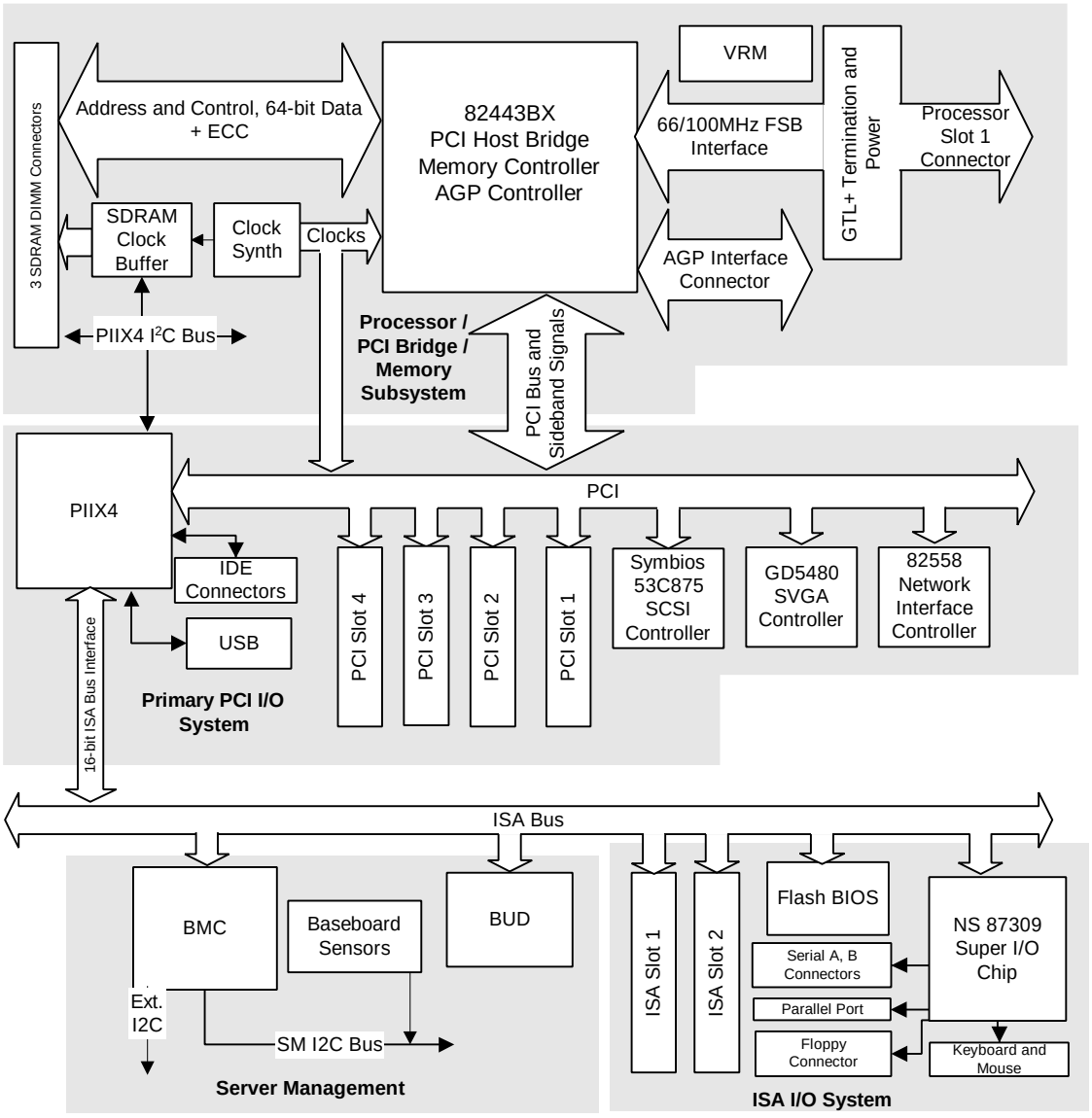


Figure 3. NL440BX/T440BX UP Server Baseboard Functional Blocks

2.1 Processor/PCI Host Bridge/Memory Subsystem

The processor/PCI bridge/memory subsystem consists of support for one SECC Pentium® II processor or one SECC2 Pentium® III processor, and up to 3 SDRAM DIMMs. The support circuitry on the baseboard consists of the following:

- Intel 440BX AGPset PCI host bridge, memory, and power management[1] controller.
- One processor bus SC242 edge connector that accepts a 100MHz or 66MHz Pentium II or 100MHz Pentium III processor.
- Three 168-pin DIMM connectors for interface to SDRAM memory.
- Processor host bus GTL+ support circuitry, including termination power supply.
- Embedded DC-to-DC voltage converter for processor power.
- Miscellaneous logic for reset configuration.

Intel 440BX AGPset Host Bridge

The Intel 440BX AGPset is a 492-pin BGA device with a 3.3V core and mixed 5V, 3.3V, and GTL+ signal interface pins. The PCI host bridge in the Intel 440BX AGPset provides the sole pathway between processor and I/O systems, performing control signal translations and managing the data path in transactions with PCI resources onboard. This includes translation of 64-bit operations in the GTL+ signaling environment at 100 MHz, to a 32-bit PCI Rev. 2.1 compliant, 5V signaling environment at 33 MHz. The Intel 440BX AGPset also handles arbitration for PCI bus master. The Intel 440BX AGPset is capable of being clocked to operate with multiple processor bus frequencies, the NL440BX/T440BX UP Server supports both 66 MHz and 100 MHz processor bus speeds. The device also features 32-bit addressing (not 36-bit), 4 or 1 deep in-order and request queue (IOQ), dynamic deferred transaction support, and Desktop Optimized (DTO) GTL bus driver support (gated transceivers for reduced power operation). The PCI interface provides greater than 100 MB/s data streamlining for PCI to SDRAM accesses (120 MB/s for writes), while supporting concurrent processor host bus and PCI transactions to main memory. This is accomplished using extensive data buffering, with processor-to-SDRAM and PCI-to-SDRAM write data buffering and write-combining support for processor-to-PCI burst writes.

Intel 440BX AGPset Memory Controller

The Intel 440BX AGPset performs the function of memory controller for NL440BX/T440BX UP Server. Total memory of 32 MB to 768 MB is supported.

The Intel 440BX AGPset provides ECC that can detect and correct single-bit errorsand detect all double-bit and some multiple-bit errors (DED). Parity checking and ECC can be configured under software control. At initial power-up, ECC and parity checking are enabled unless non-ECC memory is installed (then ECC is always disabled).

[1] Refer to “Power Management” later in this chapter, for information on how Intel 440BX AGPset and PIIX4 power management features are used on the NL440BX UP Server.

SDRAM Memory DIMM Sites

The NL440BX/T440BX UP Server provides three connectors that accept 168-pin JEDEC, 3.3V, 72-bit unbuffered or registered SDRAM DIMMs. You cannot use EDO DIMMs, only SDRAM DIMMs are allowed. You can mix various sizes of DIMMs, but cannot mix unbuffered and registered DIMMs. Best performance is obtained using unbuffered DIMMs. Registered DIMMs stack memory devices on each DIMM for greater memory capacity, but they require additional time (1 clock) for memory accesses.

SC242 Connector Interface

The Pentium® II/Pentium® III processor edge connector conforms to the SC242 specification, which can also accommodate future SECC2 cartridges. The NL440BX/T440BX UP Server provides one SC242 connector.

Processor Termination/Regulation/Power

The termination circuitry required by the Pentium II/Pentium III processor bus signaling environment (GTL+), and the circuitry to set the GTL+ reference voltage are implemented directly in the SECC/SECC2 processor. The baseboard provides 1.5V GTL+ termination power, and one VRM 8.1-compliant DC-to-DC converter to provide processor VCC_P power. VRM power is derived from the 12V supply, using an embedded DC-DC converter onboard. The VRM looks at the VID bits from the processor to automatically determine proper output voltage.

Miscellaneous Processor/Memory Subsystem Circuitry

In addition to the circuitry described above, the processor subsystem contains the following:

- Processor core frequency configuration circuitry
- DIMM presence detection and auto-configuration logic

Processor Core Frequency and Memory Configuration Logic

The PIIX4 provides an independent I^2C bus segment, the PIIX4 System Management Bus (PIIX4 SMB), supporting an I^2C bus EEMUX device (PCF8550) for configuration of processor core speed. The PIIX4 I^2C bus segment also provides access to information stored in I^2C bus ROMs on installed DIMMs, and control of the SDRAM clock buffer that generates synchronous clocks to each DIMM. BIOS code controls these features using I^2C bus operations performed by the PIIX4.

2.2 PCI I/O Subsystem

All I/O for the NL440BX/T440BX UP Server, including PCI and PC-compatible, is directed through the PCI interface. On NL440BX/T440BX UP Server, the PCI bus supports the following embedded devices and connectors:

- Four 120-pin, 32-bit, 5 Volt, PCI expansion slot connectors, one slot is RAID-upgradeable
- PIIX4 PCI-to-ISA bridge / IDE / USB / Power Management (and PIIX4 SMB) controller
- PCI video controller, Cirrus Logic CL-GD5480
- PCI Ultra SCSI Controller, Symbios Logic SYM53C875
- PCI Network Interface Controller, Intel 82558

Each device under the PCI host bridge has its IDSEL signal connected to one bit out of the PCI Address/Data lines AD[31::11], which acts as a device select on the PCI bus. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached, along with its corresponding device number

Table 1. PCI Configuration IDs

IDSEL Value	Device
22	PCI SC242
23	PCI Slot 2
24	SCSI
25	PCI Slot 3
26	NIC
27	PCI Slot 4
29	PIIX4
31	Video

PCI Arbitration

The NL440BX/T440BX UP Server PCI bus supports 8 PCI masters: NIC, PCI slots 1 through 4, SCSI, PIIX4, and Intel 440BX AGPset (video is always a slave). All PCI masters must arbitrate for PCI access, using resources supplied by the both Intel 440BX AGPset and custom arbitration logic. The Intel 440BX AGPset uses internal arbitration connections within its host interface, and the PCI interface on the Intel 440BX AGPset provides 5 REQ_L/GNT_L pairs for external devices or bridges. Logic in the BUD, which is attached to the REQ0_L/GNT0_L signals, provides support for an additional master on “Round Robin” basis.

The PIIX4 operates with a private arbitration scheme using the Intel 440BX AGPset P_PHOLD_L / P_PHOLDA_L signals, so that access time capability for ISA masters is guaranteed.

The following table defines the arbitration connections on the NL440BX/T440BX UP Server:

Table 2. PCI Arbitration Connections

Baseboard Signals	Device
P_PHOLD_L/P_PHLDA_L	PIIX4
P_REQ1_L/P_GNT1_L	PCI Slot 3
P_REQ2_L/P_GNT2_L	PCI Slot 2
P_REQ3_L/P_GNT3_L	PCI SC242
P_REQ4_L/P_GNT4_L	NIC
S_REQ0A_L/S_GNT0A_L	PCI Slot 4
S_REQ0B_L/S_GNT0B_L	SCSI

PCI Connectors

There are 4 32-bit PCI expansion connectors on the NL440BX/T440BX UP Server baseboard. One is in a shared ISA/PCI location.

RAID-upgradeable PCI Slot

NL440BX/T440BX UP Server provides support in PCI slot 3 for a zero channel RAID controller. This PCI add-in card leverages the onboard SCSI controller along with its own built-in intelligence to provide a complete RAID controller subsystem onboard. The NL440BX/T440BX UP Server interrupt structure is designed to allow the Zero channel RAID card to intercept PCI interrupts from the onboard SCSI controller when this card is installed in slot 3. If no RAID card is installed, the interrupts pass through the PCI interrupt swizzle on the NL440BX/T440BX UP Server.

PCI Bus Termination

Certain PCI signals on the NL440BX/T440BX UP Server have “passive” termination, i.e., either pull-up or pull-down resistors. In addition, certain PCI signals may have additional termination to meet signal quality requirements. These are driven through the board topology definition and simulation process, and are not discussed in this document.

PIIX4

The PIIX4 is a multi-function PCI device, providing four PCI functions in a single package: PCI-to-ISA bridge, PCI IDE interface, PCI USB controller, and power management controller. Each function within the PIIX4 has its own set of configuration registers and once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

The PIIX4 is packaged as a BGA device. On the NL440BX/T440BX UP Server, its primary role is to provide the gateway to all PC-compatible I/O devices and features. The NL440BX/T440BX UP Server uses the following PIIX4 features:

- PCI interface
- ISA bus interface
- Dual IDE interfaces
- System reset control
- ISA-compatible interrupt control
- PC-compatible timer/counters and DMA controllers
- Baseboard plug-n-play support
- General purpose I/O
- Real-time Clock and CMOS configuration RAM.

PIIX4 PCI Interface

The PIIX4 fully implements a 32-bit PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Rev. 2.1*. On NL440BX/T440BX UP Server, the PCI interface operates at 33 MHz, using the 5V signaling environment.

ISA Interface

Function 0 in the PIIX4 provides an ISA bus interface, operating at 8.33 MHz, that supports two ISA expansion connectors, Flash memory, server management interface, and the SuperI/O controller (PC87309VLJ).

PCI Bus Master IDE Interface

Function 1 in the PIIX4 provides a PCI bus master controller for dual IDE channels, each capable of programmed I/O (PIO) operation for transfer rates up to 14 MB/s, and Ultra DMA operation for transfer rates up to 33 MB/s. Each IDE channel supports two drives (0 and 1). Two IDE connectors, each featuring 40 pins (2 x 20), are provided.

Power Management Controller

One of the embedded functions in the PIIX4 is a power management controller. On the NL440BX/T440BX UP Server, power management features are obtained using ACPI-compatible software control.

Compatibility Interrupt Control

The PIIX4 provides the functionality of two 82C59 PIC devices, for ISA-compatible interrupt handling.

Real-time Clock

The PIIX4 contains an MC14681A compatible real-time clock with battery backup from an external battery. The device also contains 240 bytes of general-purpose battery backed CMOS system configuration RAM.

General Purpose Input and Output Pins

The PIIX4 provides a number of general purpose input and output pins. Some of the pins are multiplexed with specific signals and are unavailable as GPIOs, and some perform dedicated GPIO functions on the NL440BX/T440BX UP Server. These signals are not discussed in this document.

SCSI Subsystem

The NL440BX/T440BX UP Server provides an embedded PCI SCSI host adapter: Symbios Logic SYM53C875. The SYM53C875 contains a single PCI bus master interface packaged in a 169-pin BGA. The controller is capable of operations using either 8- or 16-bit SCSI providing 10 MB/s (Fast-10) or 20 MB/s (Fast-20) throughput, or 20 MB/s (Ultra) or 40 MB/s (Ultra-wide). In the NL440BX/T440BX UP Server implementation, only a 68-pin 16-bit (wide) SCSI connector interface is available on the baseboard. As a PCI 2.1 bus master, the SYM53C875 supports burst data transfers on PCI up to the maximum rate of 132 MB/sec using on-chip buffers.

Symbios Logic SYM53C875 PCI Signals

The SYM53C875 supports all of the required 32-bit PCI signals including the PERR_L and SERR_L functions. Full PCI parity is maintained on the entire data path through the controller. The device also takes advantage of PCI interrupt signaling capability, using PCI_ INT_C_Lon the NL440BX/T440BX UP Server baseboard. The figure below shows the PCI signals supported by the SYM53C875.

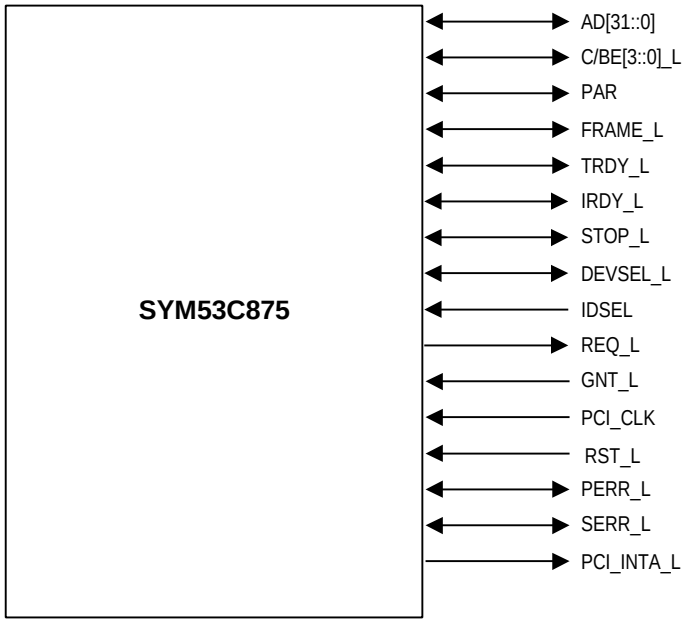


Figure 4. Embedded SCSI PCI Signals

SCSI Interfaces

The SYM53C875 contains a single Wide SCSI controller. This controller supports 8-bit or 16-bit Fast-10 and Fast-20 SCSI operation at data transfer rates of 10, 20, or 40 MB/s.

The SCSI interface on the NL440BX/T440BX UP Server offers active negation outputs, a disk activity output, and a SCSI terminator power-down control. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus, avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48 mA single-ended SCSI bus with no additional drivers (the SCSI segment can handle up to 15 devices).

SCSI Bus

The SCSI data bus is 8- or 16-bits wide with odd parity generated per byte. To accommodate 8-bit devices on the 16-bit Wide SCSI connector, the SYM53C875 assigns the highest arbitration priority to the low byte of the 16-bit word. This way, 16-bit targets can be mixed with 8-bit if the 8-bit devices are placed on the low data byte. For 8-bit mode, the unused high data byte is self-terminated and need not be connected. During chip power-down, all inputs are disabled to reduce power consumption.

PCI Video

The NL440BX/T440BX UP Server provides a Cirrus Logic CL-GD5480 video controller, along with video SGRAM and support circuitry for an embedded SVGA video subsystem. The CL-GD5480 64-bit VGA Graphics Accelerator controller contains an SVGA video controller, clock generator, BitBLT engine, and RAMDAC in a 208-pin PQFP. Two 256K x 32 SGRAM controller provides 2 MB of 10ns video memory. The SVGA subsystem supports a variety of modes: up to 1600 x 1200 resolution, or up to 16.7M colors. It also supports analog VGA monitors, single- and multi-frequency, interlaced and non-interlaced, up to 100 Hz vertical retrace frequency. The NL440BX/T440BX UP Server baseboard also provides a

standard 15-pin VGA connector, and external video blanking logic for server management console redirection support.

Video Chip PCI Signals

The CL-GD5480 supports a minimal set of 32-bit PCI signals since it never acts as a PCI master. As a PCI slave, the device requires no arbitration or interrupt connections.

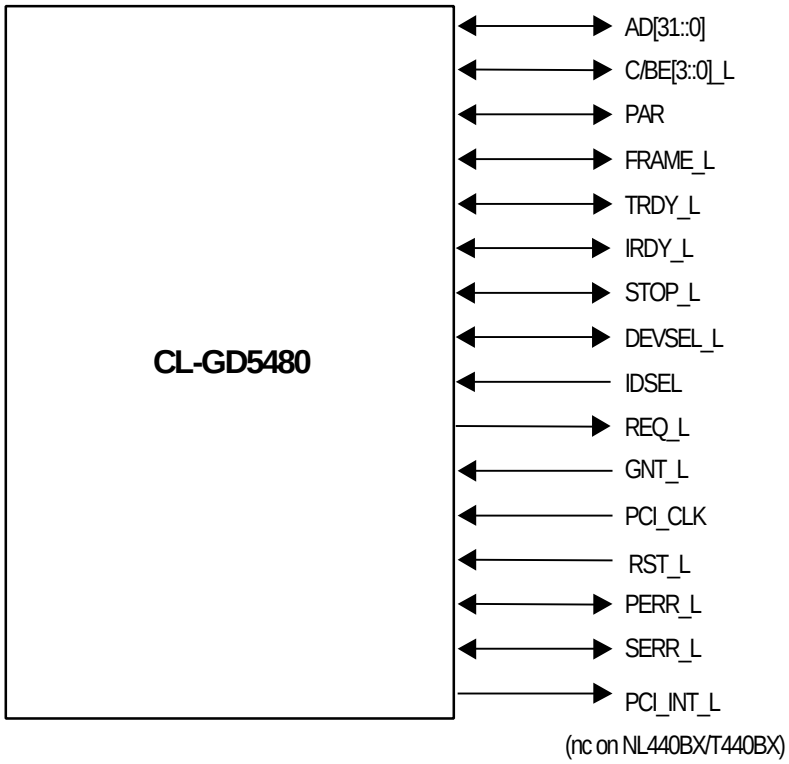


Figure 5. Video Controller PCI Signals

Video Modes

The CL-GD5480 supports all standard IBM VGA modes. Using 2 MB of SGRAM, the NL440BX/T440BX UP Server supports special Cirrus Logic extended modes. The following tables show the standard and extended modes that this implementation supports, including the number of colors and palette size (e.g., 16 colors out of 256 K colors), resolution, pixel frequency, and scan frequencies.

Table 3. Standard VGA Modes

Mode(s) in Hex	Colors (number /palette size)	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	16/256K	360 X 400	14	31.5	70
2, 3	16/256K	720 X 400	28	31.5	70
4, 5	4/256K	320 X 200	12.5	31.5	70
6	2/256K	640 X 200	25	31.5	70
7	Mono	720 X 400	28	31.5	70
D	16/256K	320 X 200	12.5	31.5	70
E	16/256K	640 X 200	25	31.5	70
F	Mono	640 X 350	25	31.5	70
10	16/256K	640 X 350	25	31.5	70
11	2/256K	640 X 480	25	31.5	60
12	16/256K	640 X 480	25	31.5	60
12+	16/256K	640 X 480	31.5	37.5	75
13	256/256K	320 X 200	12.5	31.5	70

Table 4. Extended VGA Modes

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)	Memory Option
58, 6A	16/256K	800 X 600	36	35.2	56	1 MB
58, 6A	16/256K	800 X 600	40	37.8	60	1 MB
58, 6A	16/256K	800 X 600	50	48.1	72	1 MB
58, 6A	16/256K	800 X 600	49.5	46.9	75	1 MB
5C	256/256K	800 X 600	36	35.2	56	1 MB
5C	256/256K	800 X 600	40	37.9	60	1 MB
5C	256/256K	800 X 600	50	48.1	72	1 MB
5C	256/256K	800 X 600	49.5	46.9	75	1 MB
5C	256/256K	800 X 600	56.25	53.7	85	1 MB
5C	256/256K	800 X 600	68.2	63.6	100	1 MB
5D	16/256K (interlaced)	1024 X 768	44.9	35.5	43	1 MB
5D	16/256K	1024 X 768	65	48.3	60	1 MB
5D	16/256K	1024 X 768	75	56	70	1 MB
5D	16/256K	1024 X 768	78.7	60	75	1 MB
5E	256/256K	640 X 400	25	31.5	70	1 MB
5F	256/256K	640 X 480	25	31.5	60	1 MB

5F	256/256K	640 X 480	31.5	37.9	72	1 MB
5F	256/256K	640 X 480	31.5	37.5	75	1 MB
5F	256/256K	640 X 480	36	43.3	85	1 MB
5F	256/256K	640 X 480	43.2	50.9	100	1 MB
60	256/256K (interlaced)	1024 X 768	44.9	35.5	43	1 MB
60	256/256K	1024 X 768	65	48.3	60	1 MB
60	256/256K	1024 X 768	75	56	70	1 MB
60	256/256K	1024 X 768	78.7	60	75	1 MB
60	256/256K	1024 X 768	94.5	68.3	85	1 MB
60	256/256K	1024 X 768	113.3	81.4	100	1 MB
64	64K	640 X 480	25	31.5	60	1 MB
64	64K	640 X 480	31.5	37.9	72	1 MB
64	64K	640 X 480	31.5	37.5	75	1 MB
64	64K	640 X 480	36	43.3	85	1 MB
64	64K	640 X 480	43.2	50.9	100	1 MB
65	64K	800 X 600	36	35.2	56	1 MB
65	64K	800 X 600	40	37.8	60	1 MB
65	64K	800 X 600	50	48.1	72	1 MB
65	64K	800 X 600	49.5	46.9	75	1 MB
65	64K	800 X 600	56.25	53.7	85	1 MB
65	64K	800 X 600	68.2	63.6	100	1 MB
66	32K	640 X 480	25	31.5	60	1 MB
66	32K	640 X 480	31.5	37.9	72	1 MB
66	32K	640 X 480	31.5	37.5	75	1 MB
66	32K	640 X 480	36	43.3	85	1 MB
66	32K	640 X 480	43.2	50.9	100	1 MB
67	32K	800 X 600	36	35.2	56	1 MB
67	32K	800 X 600	40	37.8	60	1 MB
67	32K	800 X 600	50	48.1	72	1 MB
67	32K	800 X 600	49.5	46.9	75	1 MB
67	32K	800 X 600	56.25	53.7	85	1 MB
67	32K	800 X 600	68.2	63.6	100	1 MB

Table 2-0. Extended VGA Modes (cont.)

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)	Memory Option
68	32K (interlaced)	1024 X 768	44.9	35.5		2MB
68	32K	1024 X 768	65	48.3		2MB
68	32K	1024 X 768	75	56		2MB
68	32K	1024 X 768	78.7	60		2MB
68	32K	1024 X 768	94.5	68.3		2MB
68	32K	1024 X 768	113.3	81.4		2MB
6C	16/256K (interlaced)	1280 X 1024	75	48	43	1 MB
6D	256/256K (interlaced)	1280 X 1024	75	48	43	2MB
6D	256/256K	1280 X 1024	108	65	60	2MB
6D	256/256K	1280 X 1024	135	80	75	2MB
6D	256/256K	1280 X 1024	157.5	91	85	2MB
6E	32K	1152 X 864	94.5	63.9	70	2MB
6E	32K	1152 X 864	108	67.5	75	2MB
6E	32K	1152 X 864	121.5	76.7	85	2MB
6E	32K	1152 X 864	143.5	91.5	100	2MB
71	16M	640 X 480	25	31.5	60	1 MB
71	16M	640 X 480	31.5	37.9	72	1 MB
71	16M	640 X 480	31.5	37.5	75	1 MB
71	16M	640 X 480	36	43.3	85	1 MB
71	16M	640 X 480	43.2	50.9	100	1 MB
74	64K (interlaced)	1024 X 768	44.9	35.5	43	2MB
74	64K	1024 X 768	65	48.3	60	2MB
74	64K	1024 X 768	75	56	70	2MB
74	64K	1024 X 768	78.7	60	75	2MB
74	64K	1024 X 768	94.5	68.3	85	2MB
74	64K	1024 X 768	113.3	81.4	100	2MB
78	32K	800 X 600	36	35.2	56	1 MB
78	16M	800 X 600	40	37.8	60	2MB
78	16M	800 X 600	50	48.1	72	2MB
78	16M	800 X 600	49.5	46.9	75	2MB
78	16M	800 X 600	56.25	53.7	85	2MB
78	16M	800 X 600	68.2	63.6	100	2MB

7B	256/256K (interlaced)	1600 X 1200	135	62.5	48	2MB
7B	256/256K	1600 X 1200	162	75	60	2MB
7C	256/256K	1152 X 864	94.5	63.9	70	1 MB
7C	256/256K	1152 X 864	108	67.5	75	1 MB
7C	256/256K	1152 X 864	121.5	76.7	85	1 MB
7C	256/256K	1152 X 864	143.5	91.5	100	1 MB
7D	64K	1152 X 864	94.5	63.9	70	2MB
7D	64K	1152 X 864	108	67.5	75	2MB
7D	64K	1152 X 864	121.5	76.7	85	2MB
7D	64K	1152 X 864	143.5	91.5	100	2MB

For more information refer to the *Cirrus Logic CL-GD5480 Technical Reference Manual*.

Network Interface Controller (NIC)

NL440BX/T440BX UP Server supports a 10BASE-T/100BASE-TX network subsystem based on the Intel 82558 Fast Ethernet PCI Bus Controller. This device is similar in architecture to its predecessor (Intel 82557), except with an integrated physical layer interface.

The 82558 is a highly integrated PCI LAN controller for 10 or 100 Mbps Fast Ethernet networks. As a PCI bus master, the 82558 can burst data at up to 132 MB/s. This high-performance bus master interface can eliminate the intermediate copy step in RX/TX frame copies, resulting in faster frame processing. The network OS communicates with the 82558 using a memory-mapped I/O interface, PCI interrupt, and two large receive and transmit FIFOs, which prevent data overruns or underruns while waiting for access to the PCI bus, as well as enabling back to back frame transmission within the minimum 960ns inter-frame spacing.

Supported Network Features

The 82558 contains an IEEE MII compliant interface to the components necessary to implement a IEEE 802.3 100Base-TX network connection. The NL440BX/T440BX UP Server supports the following features of the 82558 controller:

- Glueless 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with PCI Bus Specification, revision 2.1
- 82596-like chained memory structure, with improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- On-chip counters for network management
- Autodetect and autoswitching for 10 or 100 Mbps network speeds
- Support for both 10 Mbps and 100 Mbps Networks, full or half duplex-capable, with back-to-back transmit at 100 Mbps
- Integrated physical interface to TX magnetics.

The magnetics component terminates the 100Base-TX connector interface. A Flash device stores the network ID.

NIC Connector and Status LEDs

The 82558 drives LEDs on the network interface connector that indicate transmit/receive activity on the LAN, valid link to the LAN, and 10/100 Mbps operation. The location and function of each LED is shown in the following figure.

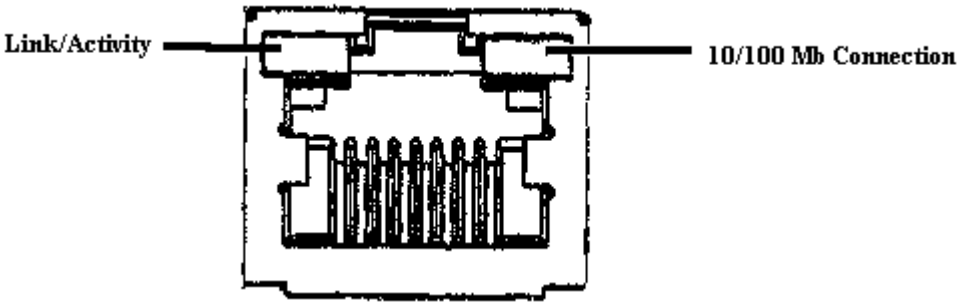


Figure 6. NIC Connector and Status LEDs

2.3 ISA I/O Subsystem

On the NL440BX/T440BX UP Server, the PIIX4 provides a bridge to an ISA I/O subsystem that provides the following connectors and devices:

- Two ISA slots, one physically shared with PCI slot 4
- Flash memory for BIOS ROM and extensions
- National Semiconductor PC87309VLJ SuperI/O controller, which provides the following:
  - ⇒ Two PC-compatible serial ports
  - ⇒ Enhanced parallel port
  - ⇒ Floppy controller
  - ⇒ Keyboard/Mouse ports

The ISA I/O subsystem also connects with the BMC. The BUD, a programmable logic device performs control of the management interrupts (NMI_L and SMI_L). Refer to “Interrupts” later in this chapter for more information on these devices and how they are used in the NL440BX/T440BX UP Server interrupt structure. The BMC controls server management features on the NL440BX/T440BX UP Server.

ISA Bus Termination

The following table describes the ISA signals on the NL440BX/T440BX UP Server that have termination, i.e. either pull-up or pull-down resistors. In addition, certain ISA signals may have additional termination to meet signal quality requirements. Those additional requirements are driven through the board topology definition and simulation process. All signals listed in the table are bussed and contain a single pull-up or pull-down resistor.

Table 5. ISA Signal Termination

Signal	Pull-up/Pull-down	Signal	Pull-up/Pull-down	Signal	Pull-up/Pull-down
DRQx	pull-down - 5.6 KΩ	IRQx	pull-up - 8.2 KΩ	REFRESH_L	pull-up - 300 Ω
IOCHK_L	pull-up - 4.7 KΩ	LA[23::17]	pull-up - 10 KΩ	SA[19::0]	pull-up - 10 KΩ
IOCHRDY	pull-up - 1 KΩ	MASTER16_L	pull-up - 300 Ω	SD[15::0]	pull-up - 8.2 KΩ
IOCS16_L	pull-up - 300 Ω	MEMCS16_L	pull-up - 300 Ω	SRDY_L	pull-up - 300 Ω
IOR_L	pull-up - 8.2 KΩ	MEMR_L	pull-up - 8.2 KΩ	SMEMW_L	pull-up - 8.2 KΩ
IOW_L	pull-up - 8.2 KΩ	MEMW_L	pull-up - 8.2 KΩ		

Compatibility I/O Controller Subsystem

The National PC87309VLJ SuperI/O device is a plug and play (PnP) compatible standard I/O subsystem controller. This device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. The NL440BX/T440BX UP Server provides the connector interface for each.

Note: Unlike it predecessor (87307), the PC87309VLJ provides no general-purpose I/O bits or programmable chip selects. All GPIOs required by NL440BX/T440BX UP Server subsystems are supplied by the PIIX4 as specified above.

Serial Ports

Two 9-pin D-sub connectors are provided. Both ports are compatible with 16550A and 16450 UARTs, supporting relocatable I/O addresses. Each serial port can be set to 1 of 4 different COM ports, and can be enabled separately. When disabled, serial port interrupts are available to add-in cards.

Parallel Port

The 87309 provides an IEEE 1284-compliant 25-pin bi-directional parallel port. BIOS programming of the SuperI/O registers enable the parallel port, and determine the port address and interrupt. When disabled, the interrupt and DMA is available to add-in cards.

Floppy Disk Controller

The FDC on the SuperI/O is functionally compatible with the PC8477, which contains a superset of the floppy disk controllers in the DP8473 and N82077. The baseboard provides the 24 MHz clock, termination resistors, and chip selects. All other FDC functions are integrated into the SuperI/O, including analog data separator and 16-byte FIFO.

Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single stacked housing. External to the board they appear as two connectors. The keyboard and the mouse controller are software compatible with the 8042AH and PC87911. The keyboard and mouse connectors are PS/2 compatible.

AT-style Front Panel Header

A header is provided for AT-style front panel connections, e.g., power, LED indicators, and reset. The connector has the following pinout:

Table 6. AT Front Panel Header Pinout

Pin	Signal
	Front panel power switch
1	Power switch
2	GND
3	(key)
	Hard disk activity LED
4	Current limited +5V
5	nc.
6	HD activity LED
7	Current limited +5V
	Speaker
8	GND
9	nc.
10	Internal Speaker Enable
11	Speaker Out
	Power LED
12	GND
13	nc.
14	Power LED
15	nc
	Front panel reset switch
16	GND
17	Reset switch
	Front panel NMI switch
18	GND
19	NMI switch

Flash ROM BIOS

An 4 Mbit flash memory (Intel 28F004S5) provides non-volatile storage space for BIOS and general purposes, packaged as a 40-lead TSOP. The device is byte wide, of the Smart 5 FlashFile family and symmetrically blocked. The Flash device is directly addressed as 8 64-kbyte blocks of 8-bit ISA memory.

Secure Flash Programming Mechanism

On NL440BX/T440BX UP Server, the BUD detects any write operation to Flash and asserts SMI_L. The SMI_L handler (part of BIOS) then looks for a signature from the BIOS Flash update utility (iFLASH) before allowing any writes to Flash. This prevents accidental loading of non-compatible BIOS code into Flash.

2.4 System Reset Control

Reset circuitry on the NL440BX/T440BX UP Server baseboard monitors reset from the front panel, PIIX4, I/O controller, and processor subsystem to determine proper reset sequencing for all types of reset. The reset logic is designed to accommodate a variety of ways to reset the system, which can be divided into the following categories:

- Power-up reset
- Hard reset
- Soft (programmed) reset

Power-up Reset

Power-up reset occurs on the initial application of power to the system. The power supply asserts its "power good" signal within 400 to 2000ms of its output voltages being stable. The BMC monitors this signal, and asserts its power good output 30 to 40ms after detecting the power supply's power good signal asserted.

Hard Reset

Hard reset may be initiated by software, or by the user resetting the system through the front panel. For software initiated hard reset, the PIIX4 Reset Control register should be used. The front panel reset is routed to the PIIX4 through the reset and power microcontroller. Both sources of hard reset cause the PIIX4 to assert ISA bus reset (RST_RSTDRV) and PCI reset (RST_P_RST_LB). RST_RSTDRV resets the ISA subsystem, while RST_P_RST_L resets the PCI bus. The Intel 440BX AGPset receives the PCI reset signal and propagates it to the processor subsystem

Soft Reset

Soft resets may be generated by the keyboard controller (RST_KB_L), or by the chipset in the processor subsection (RST_INIT_REQ_L). The two sources of soft reset are combined in the reset logic, and routed to the processor subsection via the RST_INIT_CPU_L signal. Soft reset causes the processor to begin execution in a known state without flushing caches or internal buffers.

A programmed reset may be initiated by software. Although reset control is provided by registers in the Intel 440BX AGPset, the documentation recommends that the PIIX4 Reset Control register be used instead for programmed resets.

Reset Diagram

Reset flows throughout the NL440BX/T440BX UP Server baseboard as shown in the following figure.

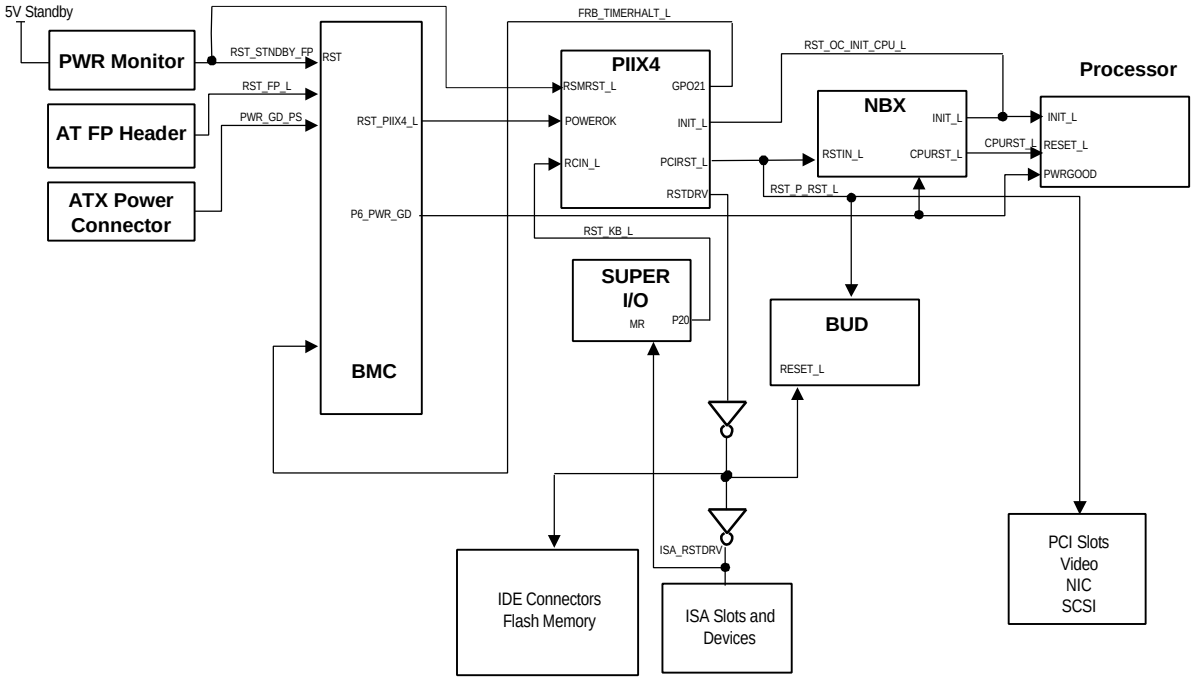


Figure 7. Reset Flow Diagram

2.5 Clock Generation and Distribution

All buses on the NL440BX/T440BX UP Server operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 100 MHz at 2.5V logic levels - SC242 connector, the Intel 440BX AGPset
- 100 MHz at 3.3V logic levels - SDRAM DIMMs
- 33.3 MHz at 3.3V logic levels - Reference clock for the PCI bus clock driver
- 14.31818 MHz at 2.5V logic levels - Processor bus clock

There are four main synchronous clock sources on the NL440BX/T440BX UP Server baseboard: 100 MHz host clock generator for the processor and SDRAM, 48 MHz clock for PIIX4 and SuperI/O controllers, 33.3 MHz PCI reference clock, and 14.318 MHz APIC and ISA clocks. In addition, the NL440BX/T440BX UP Server provides asynchronous clock generators: 40 MHz clock for the embedded SCSI controller, 32 KHz clock for the PIIX4 RTC, 22.1 MHz clock for the BMC, and a 25 MHz clock for the NIC. The following figure illustrates clock generation and distribution on the NL440BX/T440BX UP Server baseboard.

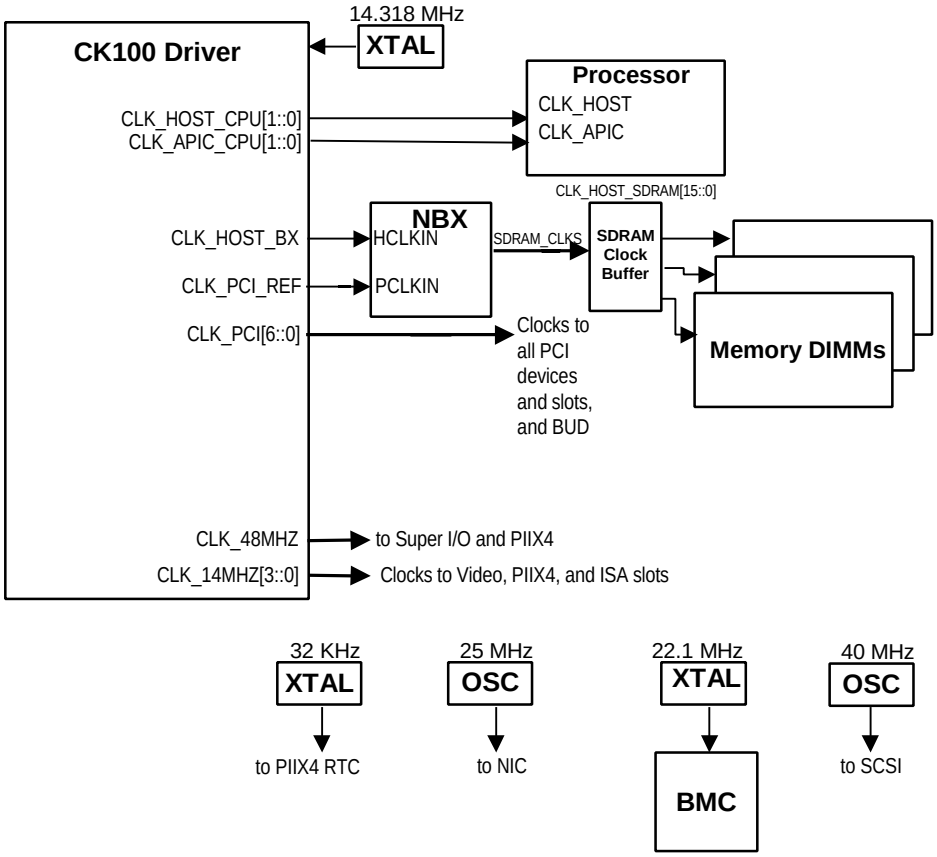


Figure 8. NL440BX/T440BX UP Server Baseboard Clock Generation and Distribution

2.6 Interrupts

The NL440BX/T440BX UP Server interrupt architecture is PC-compatible PIC mode.

PIIX4 Compatibility Interrupt Controller

For PC-compatible mode, the PIIX4 provides two 82C59-compatible interrupt controllers embedded in the device. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processor which will respond for servicing.

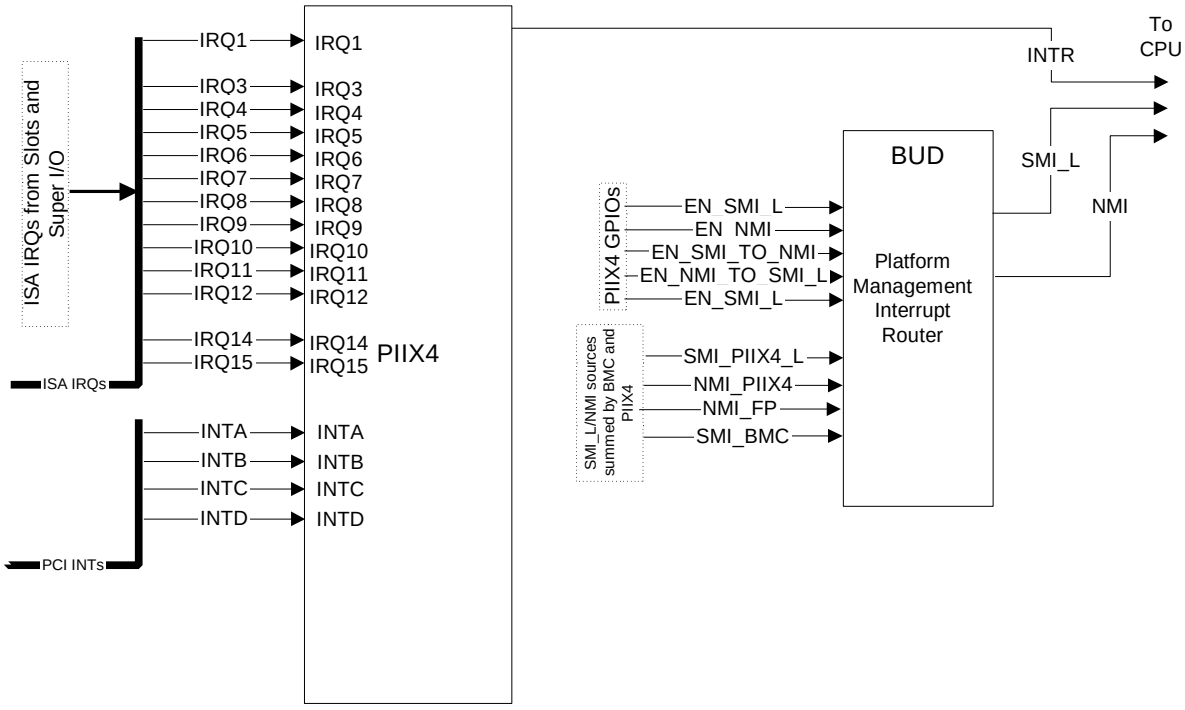


Figure 9. NL440BX/T440BX UP Server Interrupt Structure

Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on NL440BX/T440BX UP Server. The actual interrupt map is defined using configuration registers in the PIIX4 and the I/O controller.

Table 7. Interrupt Definitions

Interrupt	Description
INTR	Processor interrupt
NMI	NMI from BUD to processor
IRQ0	Timer interrupt from PIIX4
IRQ1	Keyboard interrupt
IRQ2	Interrupt signal from second 8259 internal to PIIX4
IRQ3	Serial port A or B interrupt from 87309VLJ device, user-configurable.
IRQ4	Serial port A or B interrupt from 87309VLJ device, user-configurable.
IRQ5	
IRQ6	Floppy disk
IRQ7	Parallel port
IRQ8_L	RTC interrupt
IRQ9	
IRQ10	
IRQ11	
IRQ12	Mouse interrupt
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	Secondary IDE interrupt
PCI_INTA_L	PCI Interrupt signal A
PCI_INTB_L	PCI Interrupt signal B
PCI_INTC_L	PCI Interrupt signal C
PCI_INTD_L	PCI Interrupt signal D
SMI_L	System Management Interrupt. General-purpose error indicator from various sources. Controlled by BUD.

PCI Add-in Card Slot Interrupt Sharing

The following figure shows how PCI interrupts that are shared between slots and embedded controllers are routed to the PIIX4. The arrows indicate the direction of interrupt flow from slot to slot, with final destination at the PIIX4 interrupt inputs.

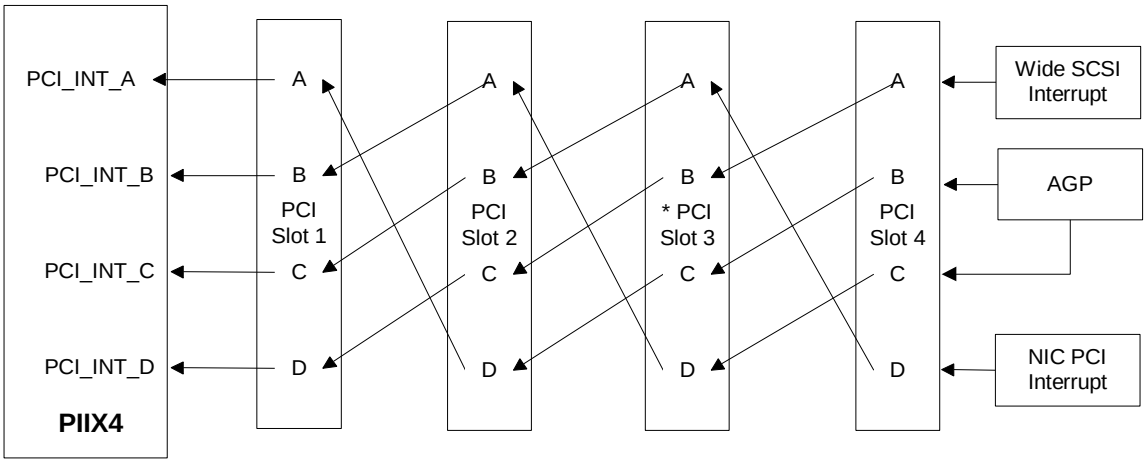


Figure 10. PCI Slot Interrupt Swizzle

PCI Interrupt Rerouting

The PIIX4 performs internal PCI to IRQ interrupt steering so that PCI interrupts can be delivered to the PIC.

System Management Interrupt Handling

NL440BX/T440BX UP Server is designed to report these types of system errors: ISA bus, PCI bus, ECC memory, and System limit. Errors are reported by the BMC and PIIX4 using SMI_L. SMI is used for server management and advanced error processing. All errors are intercepted and handled transparently by the BMC.

Basic Utility Device (BUD)

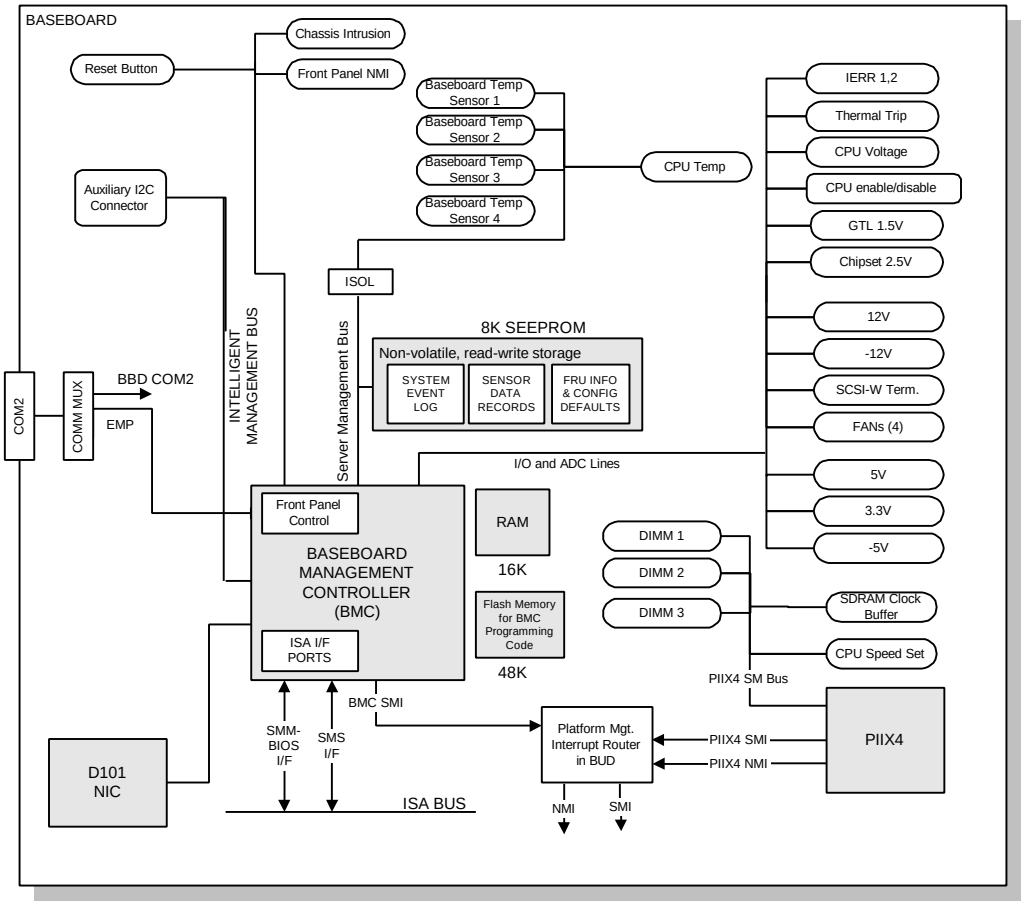
In addition to the PCI arbitration function described above, the BUD also gates and redirects SMI_L and NMI to generate SERR_L, and performs other miscellaneous logic functions. Functional specifications for BUD signal pins are not discussed in this document.

2.8 Server Management

On the NL440BX/T440BX UP Server, three serial data buses that follow I^2C bus protocol provide independent pathways for server management functions. The PIIX4 system management bus mentioned above (PIIX4 SMB) connects with each DIMM, and controls SDRAM clocks and processor speed configuration. A single microcontroller referred to as the Baseboard Management Controller (BMC) manages the other two I^2C bus segments:

- Server Management Bus supporting 8K SEEPROM and processor/baseboard temperature sensors.
- Intelligent Management Bus (IMB) supporting connectors to system-wide server management devices.

In addition, the BMC manages sensors directly using I/O and ADC lines, controls the Emergency Management Port (EMP) and detects and reports system fan failures. The BMC provides the Host ISA and IMB interfaces to server management features on NL440BX/T440BX UP Server. The following diagram illustrates server management architecture on the NL440BX/T440BX UP Server baseboard.



NL440BX/T440BX UP Server Management Block Diagram

Server Management Bus

The Server Management Bus (SMB) is a single master, open-drain, serial bus that is electrically and timing compatible with the 100 Kbps version of the I^2C bus specification. The SMB extends throughout the baseboard providing an independent pathway for the BMC to communicate with 1 baseboard and 1 processor slot temperature sensor. In addition, the SMB supports an 8K SEEPROM device for non-volatile storage of the System Event Log (SEL), Sensor Data Record Repository (SDRR), FRU information, and configuration defaults. The BMC controls access to this device and manages the data structures within (refer to BMC description below).

Buffers are provided to isolate the baseboard and processor temperature sensors from the rest of the SMB. This allows the BMC to communicate with its SEEPROM at all times.

Baseboard Management Controller (BMC)

On NL440BX/T440BX UP Server, all server management functionality is concentrated in the BMC. The BMC and associated circuitry are powered from 5V_Standby, which remains active when system power is switched off. The BMC is implemented using a Dallas Semiconductor DS82CL10 (or equivalent) microcontroller.

The primary function of the BMC is to autonomously monitor system platform management events, and log their occurrence in the non-volatile SEL. These include events such as over-temperature and over-voltage conditions, fan failure, or chassis intrusion. While monitoring, the BMC maintains the non-volatile SDRR, from which run-time information can be retrieved. The BMC provides an ISA host interface to SDRR information, so software running on the server can poll and retrieve the current status of the platform. A shared register interface is defined for this purpose. Refer to "Server Management Programming Interface" in Chapter 4 for more information.

SEL contents can be retrieved after system failure, for analysis by field service personnel using system management tools, such as Intel Server Control. Since the BMC is powered by 5V_Standby, SEL (and SDRR) information is also available via the IMB. NL440BX/T440BX UP Server includes the Emergency Management Port (EMP), which allows remote access to the SEL and other features using the COM2 port. During its watch, the BMC performs the following functions:

- Baseboard temperature and voltage monitoring
- Baseboard fan failure detection and indicator control
- SEL interface management
- SDR Repository interface management
- SDR/SEL time-stamp clock
- Baseboard Field Replaceable Unit (FRU) information interface
- System management watchdog timer
- Front panel NMI handling
- Event receiver
- ISA host and IMB interface management
- Secure mode control, video blank and floppy write protect monitoring and control, front panel lock/unlock initiation.
- Sensor event initialization agent
- Wake-on LAN (WOL) via Magic Packet* support
- ACPI Support

BMC Front Panel Control

The BMC performs all front panel controller functions on NL440BX/T440BX UP Server. These include control of system power, hard-resets, and the power failure LED. The BMC drives system power-on/off or hard reset from the following sources:

- Front panel push-button
- Transition of PIIX real-time clock alarm/suspend signal
- Magic Packet signal from NIC
- Command from EMP
- Command from ISA interface
- BMC watchdog timer

Secure Mode

The BMC monitors the SECURE_MODE signal from the baseboard keyboard controller. When the system is powered up, and SECURE_MODE asserted, the BMC prevents power off or reset via the front panel power and reset the push-buttons. A 'Secure Mode Violation Attempt' event is flagged by the BMC whenever a front panel push-button is pressed while in secure mode. Options are provided for blanking the onboard video, and write-protecting the onboard floppy interface when Secure Mode is active.

Emergency Management Port (EMP)

The COM2 serial port on the NL440BX/T440BX UP Server can be configured for use as an EMP. EMP provides a level of system management via RS-232 during powered-down, pre-boot, and post-boot situations. This allows system management software (SMS) interactions via point-to-point RS-232 connections, or external modem. EMP provides access to these basic management features:

- System power up
- System power-down (Not available in restricted mode).
- System Reset (Not available in restricted mode).
- NMI control (Not available in restricted mode).
- Access to the System Event Log, FRU, and Sensor Data Records.
- Access to BIOS Console Redirection.
- Password Protection

The EMP is intended for use in a secure environment. A simple password can be configured to provide a rudimentary level of security on the interface. System configuration options can be used to disable this interface.

The COM2 port can be used on NL440BX/T440BX UP Server for three different purposes: EMP, console redirection, or normal COM usage. If the BMC is using the port for EMP purposes, it is unavailable to the BIOS or SMS during this mode. If the System BIOS is using the port for console redirection, it is unavailable to the BMC or SMS (since the machine is still doing POST). Under normal usage COM2 appears to the OS as a normal serial port; in this case the BMC and System BIOS cannot use the port.

The NL440BX/T440BX UP Server EMP architecture supports several remote access modes, selectable using the F1 BIOS Setup Screen, as follows:

1. **Pre-boot only mode** - The EMP is only available while the machine is powered off and during POST. Just prior to booting the OS, the System BIOS disables the EMP by sending a command to the BMC. COM2 is then available as a normal serial port.
2. **Always active mode** - EMP and Console Redirect are available under the same conditions as listed in #1 above. However, the System BIOS leaves the port enabled for run-time EMP and SMS usage. The BIOS configures the hardware such that the O/S can not “see” the port.
3. **Always disabled mode** - EMP is not available under any conditions, Console redirection is a separate function and is not affected.
4. **Restricted mode -** This option can be selected in conjunction with either the ‘Pre-boot Only’ or ‘Always Active’ modes listed above, using the BIOS setup interface. When activated, Power Down control, Front Panel NMI, and Reset Control via the EMP are disabled. Power On control, System Event Log access, FRU Inventory, and Sensor Data Repository access remain enabled. Console redirection operation is unaffected by Restricted Mode.

EMP Password

The BMC implements a simple password mechanism for the EMP, activated by BIOS setup. If the password is active, a correct password must be received on the EMP before any other commands are accepted. The password must be entered every time COM2 is switched over to EMP operation. It must also be re-entered if the EMP has been inactive for more than 30 seconds. Only BIOS setup can set or clear the password, it cannot be changed remotely.

System Fan Interface

The NL440BX/T440BX UP Server provides four 3-pin, shrouded, and keyed fan connectors. One of these connectors, marked as “Fan 3(CPU)”, located next to the Pentium II/Pentium III processor SEC cartridge on the baseboard, is for a fansink. This fan can be equipped with a sensor that indicates whether the fan is operating. The remaining three connectors on the baseboard attach to chassis fans equipped with a sensor that indicates whether the fan is operating. These three fans can also be turned on and off from the BMC. The sensor pins for all of these fans are routed to the BMC for failure monitoring.

3. Configuration and Initialization

This chapter describes the initial programming environment including address maps for memory and I/O, techniques and considerations for programming ASIC registers, and hardware options configuration.

3.1 Memory Space

The NL440BX/T440BX server operates in PC-compatible memory space (below 1MB), as well as the entire range of installed memory, according to conventions defined for Pentium II/Pentium III processors using the 82443BX memory controller. For complete information regarding memory space for 82443BX-based systems, refer to the *Intel 440BX AGPset: 82443BX Host Bridge/Controller Data Sheet*.

3.2 I/O Map

The Intel 440BX AGPset allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including PIIX4, have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On the NL440BX/T440BX UP Server, the PIIX4 provides the bridge to ISA functions.

The I/O map in the following table shows the location in the NL440BX/T440BX UP Server I/O space of all directly I/O-accessible registers. PCI configuration space registers for each device control mapping in I/O and memory spaces, and other features that may affect the global I/O map.

Table 8. NL440BX/T440BX UP Server I/O Map

Address(es)	Resource	Notes
0000h - 000Fh	DMA Controller 1	
0010h - 001Fh	DMA Controller 1	aliased from 0000h - 000Fh
0020h - 0021h	Interrupt Controller 1	
0022h - 0023h		
0024h - 0025h	Interrupt Controller 1	aliased from 0020h - 0021h
0026h - 0027h		
0028h - 0029h	Interrupt Controller 1	aliased from 0020h - 0021h
002Ah - 002Bh		
002Ch - 002Dh	Interrupt Controller 1	aliased from 0020h - 0021h
002Eh - 002Fh	Super I/O Index and Data Ports	
0030h - 0031h	Interrupt Controller 1	aliased from 0020h - 0021h
0032h - 0033h		
0034h - 0035h	Interrupt Controller 1	aliased from 0020h - 0021h
0036h - 0037h		
0038h - 0039h	Interrupt Controller 1	aliased from 0020h - 0021h
003Ah - 003Bh		
003Ch - 003Dh	Interrupt Controller 1	aliased from 0020h - 0021h
003Eh - 003Fh		
0040h - 0043h	Programmable Timers	
0044h - 004Fh		
0050h - 0053h	Programmable Timers	aliased from 0040h - 0043h
0054h - 005Fh		
0060h, 0064h	Keyboard Controller	Keyboard chip select from 87309
0061h	NMI Status & Control Register	
0063h	NMI Status & Control Register	aliased
0065h	NMI Status & Control Register	aliased
0067h	NMI Status & Control Register	aliased
0070h	NMI Mask (bit 7) & RTC Address (bits 6::0)	
0072h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0074h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0076h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0071h	RTC Data	

0073h	RTC Data	aliased from 0071h
0075h	RTC Data	aliased from 0071h
0077h	RTC Data	aliased from 0071h
0080h - 0081h	BIOS Timer	
0080h - 008Fh	DMA Low Page Register	PIIX4
0090h - 0091h	DMA Low Page Register (aliased)	PIIX4
0092h	System Control Port A (PC-AT control Port) (this port not aliased in DMA range)	PIIX4
0093h - 009Fh	DMA Low Page Register (aliased)	PIIX4
0094h	Video Display Controller	
00A0h - 00A1h	Interrupt Controller 2	PIIX4
00A4h - 00A15	Interrupt Controller 2 (aliased)	PIIX4
00A8h - 00A19	Interrupt Controller 2 (aliased)	PIIX4
00ACh - 00ADh	Interrupt Controller 2 (aliased)	PIIX4
00B0h - 00B1h	Interrupt Controller 2 (aliased)	PIIX4
00B2h	Advanced Power Management Control	PIIX4
00B3h	Advanced Power Management Status	PIIX4
00B4h - 00B5h	Interrupt Controller 2 (aliased)	PIIX4
00B8h - 00B9h	Interrupt Controller 2 (aliased)	PIIX4
00BCh - 00BDh	Interrupt Controller 2 (aliased)	PIIX4
00C0h - 00DFh	DMA Controller 2	PIIX4
00F0h	Clear NPX error	Resets IRQ13
00F8h - 00FFh	x87 Numeric Coprocessor	
0102h	Video Display Controller	
0170h - 0177h	Secondary Fixed Disk Controller (IDE)	PIIX4 (not used)
01F0h - 01F7h	Primary Fixed Disk Controller (IDE)	PIIX4
0200h - 0207h	Game I/O Port	Not used
0220h - 022Fh	Serial Port A	
0238h - 023Fh	Serial Port B	
0278h - 027Fh	Parallel Port 3	
02E8h - 02EFh	Serial Port B	
02F8h - 02FFh	Serial Port B	
0338h - 033Fh	Serial Port B	
0370h - 0375h	Secondary Floppy	

0376h	Secondary IDE	
0377h	Secondary IDE/Floppy	
0378h - 037Fh	Parallel Port 2	
03B4h - 03BAh	Monochrome Display Port	
03BCh - 03BFh	Parallel Port 1 (Primary)	
03C0h - 03CFh	Video Display Controller	
03D4h - 03DAh	Color Graphics Controller	
03E8h - 03EFh	Serial Port A	
03F0h - 03F5h	Floppy Disk Controller	
03F6h - 03F7h	Primary IDE - Sec. Floppy	
03F8h - 03FFh	Serial Port A (Primary)	
0400h - 043Fh	DMA Controller 1, Extended Mode Registers.	PIIX4
0461h	Extended NMI / Reset Control	PIIX4
0462h	Software NMI	PIIX4
0480h - 048Fh	DMA High Page Register.	PIIX4
04C0h - 04CFh	DMA Controller 2, High Base Register.	
04D0h - 04D1h	Interrupt Controllers 1 and 2 Control Register.	
04D4h - 04D7h	DMA Controller 2, Extended Mode Register.	
04D8h - 04DFh	Reserved	
04E0h - 04FFh	DMA Channel Stop Registers	
0678h - 067Ah	Parallel Port (ECP)	
0778h - 077Ah	Parallel Port (ECP)	
07BCh - 07BEh	Parallel Port (ECP)	
0800h - 08FFh	NVRAM	
0C80h - 0C83h	EISA System Identifier Registers	PIIX4
0C84h	Board Revision Register	
0C85h - 0C86h	BIOS Function Control	
0CA9h	BMC Data Register	Server management mailbox registers.
0CAAh	BMC Command Register	
0CABh	BMC Status Register	
0CF8h	PCI CONFIG_ADDRESS Register	Located in NBX
0CF9h	NBX Turbo and Reset control	PIIX4
0CFCh	PCI CONFIG_DATA Register	Located in NBX
46E8h	Video Display Controller	

3.3 Accessing Configuration Space

All PCI devices contain PCI configuration space, accessed using mechanism #1 defined in the *PCI Local Bus Specification*. The PIIX4 is accessed as a multi-function PCI device, with 4 sets of configuration registers.

Two Dword I/O registers in the Intel 440BX AGPset are used for the configuration space register access:

- CONFIG_ADDRESS (I/O address 0CF8h)
- CONFIG_DATA (I/O address 0CFCh)

When CONFIG_ADDRESS is written to with a 32-bit value selecting the bus number, device on the bus, and specific configuration register in the device, a subsequent read or write of CONFIG_DATA initiates the data transfer to/from the selected configuration register. Byte enables are valid during accesses to CONFIG_DATA; they determine whether the configuration register is being accessed or not. Only full Dword reads and writes to CONFIG_ADDRESS are recognized as a configuration access by the Intel 440BX AGPset. All other I/O accesses to CONFIG_ADDRESS are treated as normal I/O transactions.

CONFIG_ADDRESS Register

CONFIG_ADDRESS is 32 bits wide and contains the field format shown in the following figure. Bits [23::16] choose a specific bus in the system. Bits [15::11] choose a specific device on the selected bus. Bits [10::8] choose a specific function in a multi-function device. Bits [7::2] select a specific register in the configuration space of the selected device or function on the bus.

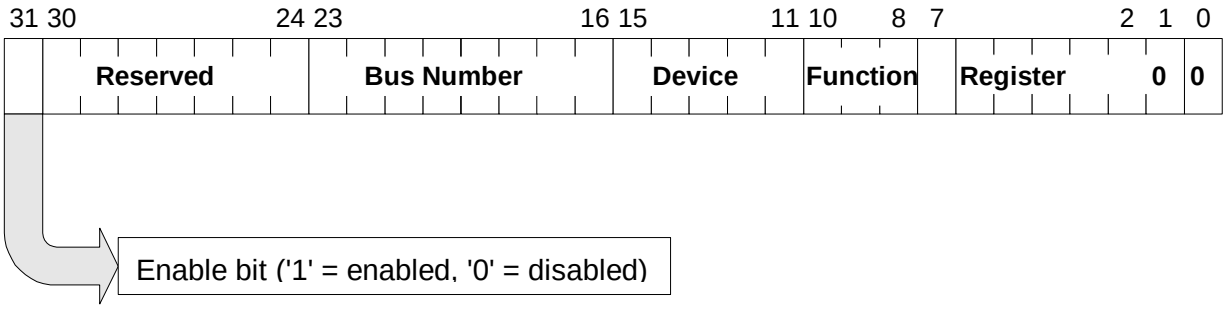


Figure 15. CONFIG_ADDRESS Register

Bus Number

PCI configuration space protocol requires that all PCI buses in a system be assigned a Bus Number. Furthermore, bus numbers must be assigned in ascending order within hierarchical buses. Each PCI bridge has registers containing its PCI Bus Number and Subordinate PCI Bus Number, which must be loaded by POST code. The Subordinate PCI Bus Number is the bus number of the last hierarchical PCI bus under the current bridge. The PCI Bus Number and the Subordinate PCI Bus Number are the same in the last hierarchical bridge.

Device Number and IDSEL Mapping

Each device under a PCI bridge has its IDSEL input connected to one bit out of the PCI bus address/data signals AD[31::11] for the PCI bus. Each IDSEL-mapped AD bit acts as a chip select for each device on PCI. The host bridge responds to a unique PCI device ID value, that along with the bus number, cause the assertion of IDSEL for a particular device during configuration cycles. The following table shows the correspondence between IDSEL values and PCI device numbers for the PCI bus. The lower 5-bits of the device number are used in CONFIG_ADDRESS bits [15::11].

Table 9. PCI Configuration IDs and Device Numbers

	PCI Bus	
IDSEL	**Device #**	**Device**
31	10100b	CL-GD5480 video chip
30	10011b	
29	10010b	PIIX4
28	10001b	
27	10000b	PCI Slot 4
26	01111b	82558 NIC
25	01110b	PCI Slot 3
24	01101b	SYM53C875
23	01100b	PCI Slot 2
22	01011b	PCI SC242
21	01010b	
20	01001b	
19	01000b	
18	00111b	
17	00110b	
16	00101b	
15	00100b	
14	00011b	
13	00010b	
12	00001b	
11	00000b	Hardwired to NBX host bridge

Translation Types

The following discussion of PCI configuration cycles and translations relate to the default PCI bus structure for NL440BX/T440BX UP Server. If a PCI-to-PCI bridge is present on an expansion card, the following principles apply.

When the host bridge sees a configuration access to CONFIG_DATA, it uses the data previously written into CONFIG_ADDRESS to determine the appropriate response. If the configuration cycle enable bit (bit 31) is set and the Bus Number in CONFIG_ADDRESS falls within the range of the host bridge Bus Number and Subordinate Bus Number, the HOST BRIDGE performs a configuration cycle translation of three types:

1? An internal access to host bridge configuration space is performed if the Bus Number and Device Number are 0. No PCI cycles are generated.

2? A Type 0 translation is performed if the PCI device being configured is on the primary PCI segment and the Device Number is less than or equal to 20.

3? A Type 1 translation is performed if the target device is on a secondary segment (only applies on NL440BX/T440BX UP Server if using an add-in board with a PCI-to-PCI bridge).

The following figure shows a Type 0 translation, in which the host bridge decodes the Device Number field (bits [15::11] in CONFIG_ADDRESS) to select one of the AD[31::16] lines to drive active, which provides the chip select (via IDSEL) to the specified device.

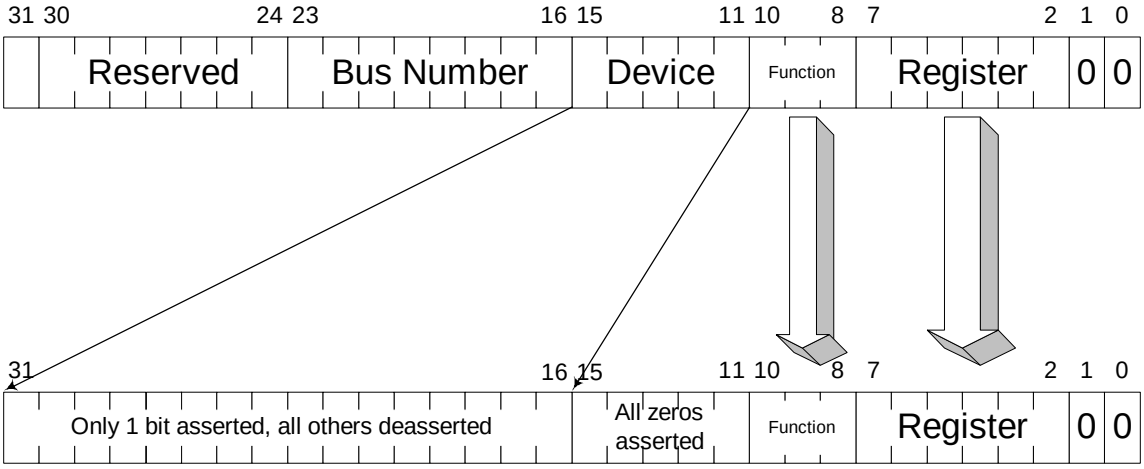


Figure 16. Type 0 Configuration Cycle Translation

If the bus number field of CONFIG_ADDRESS does not match the host bridge's PCI Bus Number, but matches the PCI-to-PCI bridge, the transaction is passed through the host bridge as a Type 1 configuration cycle. In a Type 1 configuration cycle translation, the contents of CONFIG_ADDRESS are driven onto AD[31::2], AD1 is 0 and AD0 is 1 which indicates to all PCI agents that the configuration cycle is a Type 1 translation that is targeting a secondary PCI segment.

Special Cycle Generation

When CONFIG_ADDRESS is written with a host bridge's PCI bus number, Device Number of all 1s, a Function Number of all 1s, and a Register Number of all 0s, that host bridge performs a PCI Special Cycle when CONFIG_DATA is written, using the contents of CONFIG_DATA as Special Cycle data. Reads of CONFIG_DATA when CONFIG_ADDRESS is set up to do a Special Cycle are treated like a normal configuration cycle.

3.4 Hardware Initialization and Configuration

This section describes the following:

- System initialization
- Programming considerations for various portions of the system

System Initialization Sequence

A Pentium® II/Pentium® III processor system based on the Intel 440BX AGPset is initialized and configured in the following manner.

1. System power is applied. The power-supply provides resets using the RST_PWR_GD_BB signal. PCI reset (RST_P_RST_L) is driven to tri-state the PCI bus in order to prevent PCI output buffers from short circuiting when the PCI power rails are not within the specified tolerances. The Intel 440BX AGPset asserts G_CPURST_L to reset the processor(s).
2. The Intel 440BX AGPset is initialized, with its internal registers set to default values.
3. Before G_CPURST_L is deasserted, the Intel 440BX AGPset asserts BREQ0_L
4. The processor begins by fetching the first instruction from the reset vector.
5. Intel 440BX AGPset registers are updated to reflect memory configuration. DRAM is sized and initialized.
6. All PCI and ISA I/O subsystems are initialized and prepared for booting.

Obtaining DIMM Information for Memory Configuration

Before any memory operations can begin, Intel 440BX AGPset DRAM-related registers must be initialized using information obtained from installed DIMMs via the PIIX4 SMB. The format of this information is defined by Serial Presence Detection mechanism in the JEDEC 168-pin DIMM standard. Each DIMM site provides a unique PIIX4 SMB address, which after a series of SM bus operations reveals the following information (this is only a subset; refer to the documentation for installed DIMMs for details):

Table 10. DIMM Information for Intel 440BX AGPset Register Initialization

Data Byte	Function
02h	Memory type (always SDRAM on NL440BX/T440BX UP Server)
03h	Number of row addresses, not counting bank addresses
04h	Number of column addresses
05h	Number of banks of DRAM on the DIMM (single- or double- sided)
0Bh	ECC support indication
0Ch	Refresh rate
11h	Number of banks on each SDRAM device
24h - 29h	Access time from clock for CAS_L latency 1 through 7
2Ah	Data width of SDRAM components

For example, to program the DRAM Row Boundary (DRB) registers (at 60h - 67h in Intel 440BX AGPset config. space), the size of each row must be determined. The number of row addresses (byte 03h), plus the number of column addresses (byte 04h), plus the number of banks on each DIMM (byte 05h) equals the total address depth for a DRAM row. Since each row is always 64 data bits wide, the row size is easily determined for DRB programming.

PCI Bus Master IDE Programming

The PIIX4 IDE controller provides two PCI bus master channels capable of PIO IDE transfers at 14 MB/s, or Ultra DMA/33 bus master IDE transfers at 33 MB/s. A device driver that performs IDE transactions as a PCI bus master offloads the processor(s), which improves performance in a multitasking (and multi-processor) environment. The physical memory region to be transferred is defined for the PIIX4 IDE master using the 64-bit Physical Region Descriptor (PRD) structure, with the following format:

Table 11. PCI Bus Master IDE Physical Region Descriptor Format

Bit(s)	Name	Description
64	End Of Table (EOT)	Indicates that this PRD is the last for this IDE transfer. The PRD table consists of a number of PRD entries as required by the transfer size. The total number of PRDs in the table must represent a block of memory equal to or greater than the actual transfer size.
63::48	Reserved	
47::33	Byte Count	Bits 15::1 of the byte transfer count. A value of 0 means 64 KB for this PRD. Each PRD entry describes no greater than a 64 KB block of memory.
32	Reserved	Always 0.
31::1	Memory Region Physical Base Address	Bits 31::0 of the physical memory region byte address. The region referenced must not cross a 64 KB boundary.
0	Reserved	Always 0.

Using the Physical Region Descriptor

Software uses the PRD as follows.

1. Prepare a PRD table in main memory, consisting of a number of entries as required by the total transfer size. The last PRD entry has the EOT bit set, indicating the table end.
2. Load the starting address for the first entry in the PRD table using the PRD Table Pointer register.
3. Issue the appropriate DMA transfer command to the disk device.
4. Set the Start bit in the Bus Master IDE Command register, which causes the PIIX4 to fetch the first PRD table entry. The IDE controller transfers data between memory and the IDE device, and signal an interrupt when the transfer is completed.
5. Clear the Start bit, and read the Bus Master IDE Status register.

Bus Master IDE Command Register

For the primary channel, this register resides at the base address, for the secondary channel, at offset 08h from the base address.

Table 12. Bus Master IDE Command Register Format

Bit(s)	Name	Description
7::4	Reserved	
3	Bus Master R/W Control	If 1, write command; if 0, read command. This bit must not be changed while the IDE bus master function (initiated by bit 0) is active.
2::1	Reserved	
0	Start/Stop Bus Master	When set, bus master operation begins. When clear, bus master operation stops.

Bus Master IDE Status Register

For the primary channel, this register resides at offset 02h from the base address, for the secondary channel, at offset 0Ah.

Table 13. Bus Master IDE Status Register Format

Bit(s)	Name	Description
7	Reserved	Always 0.
6	Drive 1 DMA Capable	If 1, indicates that slave drive is capable of DMA transfers. If 0, no DMA.
5	Drive 0 DMA Capable	If 1, indicates that master drive is capable of DMA transfers. If 0, no DMA.
4::3	Reserved	
2	IDE Interrupt Status	If 1, indicates that the IDE device has asserted its interrupt line. This bit is cleared by writing a 1. Bits 2 and 0 of this register indicate interrupt activity as shown in the following table.
1	IDE DMA Error	If 1, indicates that a target-abort or master-abort occurred during a data transfer on PCI. This bit is cleared by writing a 1.
0	Bus Master IDE Active	If 1, indicates bus master operation as determined by bit 0 of the Bus Master IDE Command register. This bit is cleared when the last transfer to a region is performed.

Table 14. IDE Interrupt Activity Status Encoding

Bit 2	Bit 0	Meaning
1	1	The IDE device generated an interrupt before exhaustion of the physical memory region. This is the normal indication of transfer completion when the transfer size is less than the target physical memory block size.
1	0	The IDE device generated an interrupt on exhaustion of the physical memory region. This is the normal indication of transfer completion when the transfer size equals the target physical memory block size.
0	1	DMA Transfer in progress; no interrupt has been generated.
0	0	Error indication. Either an error has occurred while transferring data to/from memory (bit 1 = 1), or the physical descriptor specified a smaller block than the IDE transfer (bit 1 = 0).

Bus Master PRD Table Pointer Register

Specifies the pointer to the PRD table. For the primary channel, this register resides at offset 04h from the base address, for the secondary channel, at offset 0Ch.

Server Management Programming Interface

BMC mailbox registers provide a mechanism for communications between SM bus server management bus agents, and SMS or SMI handler code running on the server. BMC mailbox register space, physically located in the device, is mapped to BMC external data memory and ISA I/O space. This shared register space consists of three byte-wide registers:

- Status Register - provides semaphores for use in various defined operations
- Command Register - accepts commands and returns completion codes
- Data Register - provides a port for transactions that exchange data

In addition to the ports described above, the BUD contains a port 070h snoop register. See the section titled "Port 70h Snoop Register" later in this chapter for further information.

SMS and SMI handler code interacts with the register interface using a variety of read and write commands encapsulated in messages. The origin of a message is specified during a particular transaction using Control Codes that are unique to the transaction, allowing the interface to allocate priority to various sources, and control SMI handler and SMS precedence (the SMI handler can always abort or temporarily interrupt any transaction).

Following are descriptions of the BMC mailbox registers.

BMC Status Register

Typically, BMC mailbox registers do not return data immediately during the processing of message transactions. The ISA bus side must always initiate the transaction because the BMC cannot act as an ISA bus master. The BMC must use semaphores in the Status register to arbitrate data transfers with the ISA side. The Status register is located at I/O address 0CABh. Bits 7::2 are read-only from the ISA bus and write-only from the BMC; these bits are used by the BMC as semaphores. Only bits 1::0 are readable and writeable from both sides of the interface. The following table defines the function of Flag register bits.

Table 15. BMC Status Register Format

Bit	Name	Description
7	DATA_READY	Indicates when data for the BMC is available in the Data register from the BMC. Occasional polling of this bit from the ISA bus is recommended. In the event that the SMI handler interrupts an SMS application, the BMC saves the prior state of bits 7::2, and restores them on exit from the SMI handler.
6	Reserved	
5	Reserved	
4	SMI	Indicates whether or not an SMI was generated by the BMC, PBC, or FPC.
3	SMI_I2C_READY	Indicates when an SM bus message response is pending to an SMI handler request.
2	SMS_I2C_READY	Indicates when an SM bus message response is pending to an SMS request.
1	Reserved	
0	BUSY	Provides the arbitration mechanism for BMC mailbox register access. This bit is settable only from the ISA side and clearable only by the BMC.

BMC Command Register

The Command register is the destination for Control Codes from the ISA bus, and Status codes returned by the BMC. Control codes determine the function of a particular command, and status codes indicate the completion status of the previously issued ISA command by the BMC. The Command register is located at I/O address 0CAAh.

Completion status codes returned in the Command register indicate BMC mailbox transaction status. For example, if several bytes of data were uploaded to a device on the SM bus from Server Management Software, the BMC acknowledges reception of each byte by writing a completion status code in the Command register before clearing the Busy bit. Completion codes are returned on every byte transfer through the BMC.

On the ISA side of the interface, two sources of messages are defined: SMI handler or SMS application. They can address SM bus messages to any device on the SM bus server management bus. Messages may include both command and data sequentially written to the Data register. Process control or framing codes are placed in the Command register. These codes, unique to each defined transaction, define the beginning, intermediate, and ending stages of a message transaction for BMC execution. Completion status (described above) is returned for each byte transferred in the transaction.

BMC Data Register

The Data register is the destination for all commands and data presented to the BMC from either side of the interface, and read/writeable from both ISA bus and BMC. The Data register is located at I/O address 0CA9h.

SM Bus Addresses

NL440BX/T440BX UP Server provides 3 independent SM bus segments for server management purposes: IMB, SMB, and PIIX4 SMB. The IMB supports connector interfaces to external SM bus devices; only the SMB and PIIX4 SMB connect with onboard devices. The following table defines the SM bus addresses for SM bus devices on the NL440BX/T440BX UP Server baseboard. All other sensors, fans, and switches related to server management connect directly with the BMC (not SM bus-accessible).

Table 16. SM Bus Addresses on NL440BX/T440BX UP Server

Address	SM Bus Segment	Device
9Ah	SMB	Processor temperature sensor
9Ch	PIIX4 SMB	Processor core speed control
A0h	PIIX4 SMB	DIMM SC242 information
A2h	PIIX4 SMB	DIMM slot 2 information
A4h	PIIX4 SMB	DIMM slot 3 information
AEh	SMB	SEEPROM containing SEL, SDR, and FRU info.
D2h	PIIX4 SMB	SDRAM clock buffer control

3.5 Hardware Jumper Configuration

This section describes how to configure hardware jumper options on the baseboard for the following:

- System configuration
- Internal/external speaker selection

Jumper locations and designations are marked on the baseboard, refer to the layout diagram in Chapter 1 for placement information.

System Configuration Jumpers

15-pin and 11-pin single inline headers provide seven 3-pin jumper blocks that control various configuration options, as shown in the figure below. The shaded areas show default jumper placement for each configurable option.

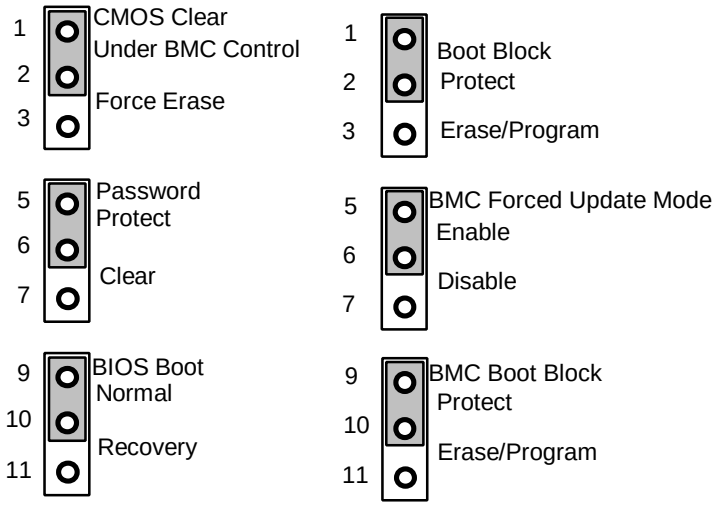


Figure 17. System Configuration Jumpers

The following table describes each jumperable option.

Table 17. System Configuration Jumper Options

Option	Description
CMOS Clear	If pins 1 and 2 are jumpered (default), preservation of configuration CMOS through system reset is controlled by the BMC. If pins 2 and 3 are jumpered, CMOS contents are set to manufacturing default during system reset.
Password Clear	If pins 5 and 6 are jumpered (default), the current system password is maintained during system reset. If pins 6 and 7 are jumpered, the password is cleared on reset.
Recovery Boot	If pins 9 and 10 are jumpered (default) the system will attempt to boot using the BIOS programmed in the Flash memory. If pins 10 and 11 are jumpered, the BIOS will attempt a recovery boot, loading BIOS code from a floppy disk into the Flash device. This is typically used when the BIOS code has been corrupted.
BIOS Boot Block Write Protect	If pins 13 and 14 are jumpered (default), the BIOS boot block is write-protected. If pins 14 and 15 are jumpered, the boot block is erasable and programmable. ***WARNING: Incorrect programming of the boot block will render the system unbootable.***
BMC Forced Update Mode	puts the BMC into firmware transfer mode. All normal operation is suspended allowing a clean boot. In this mode the BMC is operating out of the hardware protected BOOT block
BMC Boot Block Write	protects the BMC's boot block, it cannot be written to if the jumper is in the protect mode.

Speaker Circuit Jumper/Connector

A 4-pin single inline header provides a way to plug in an external speaker or, by jumper, a connection to the onboard speaker. The configuration is shown in the figure below.

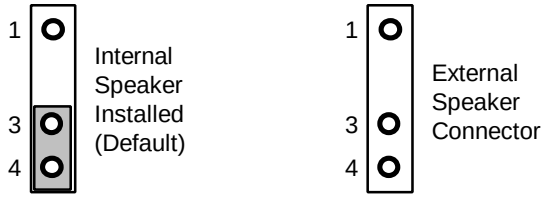


Figure 18. Speaker Circuit Jumper

4. Electrical, Environmental, and Mechanical Specifications

This chapter specifies the operational parameters and physical characteristics for NL440BX/T440BX UP Server . This is a board-level specification only. System specifications are beyond the scope of this document.

4.1 Absolute Maximum Ratings

Operation of the NL440BX/T440BX UP Server at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 18. Absolute Maximum Ratings

Operating Temperature	0°C to +55°C *
Storage Temperature	-40°C to +70°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V **
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V

Chassis design must provide proper airflow to avoid exceeding Pentium II/Pentium III processor maximum case temperature.

** V_{DD} means supply voltage for the device.

4.2 Electrical Specifications

DC specifications for the NL440BX/T440BX UP Server power connectors and module power budgets, are summarized here. Electrical characteristics for major connector interfaces (including DC and AC specifications), can be obtained from other documents:

- PCI Connectors -- *PCI Local Bus Specification Rev. 2.1*
- ISA slots -- *EISA Bus Specification*

Power Connection

Main power supply connection is obtained using the 20-pin ATX-style connector. A second connector is provided to supply additional if necessary. The following tables define the pinouts and wire gauge/color for each of these connectors.

Table 19. 20-pin ATX-style Main Power Connector Pinout

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	+3.3 VDC	Orange	11	+3.3 VDC 3.3 V sense	Orange Brown
2	+3.3 VDC	Orange	12	-12 VDC	Blue
3	COM	Black	13	COM	Black
4	+5 VDC	Red	14	PS-ON*	Green
5	COM	Black	15	COM	Black
6	+5 VDC	Red	16	COM	Black
7	COM	Black	17	COM	Black
8	PWR-OK	Gray	18	-5 VDC	White
9	5 V Standby	Purple	19	+5 VDC	Red
10	+12 VDC	Yellow	20	+5 VDC	Red

Table 20. 6-pin Auxiliary Power Connector Pinout

Pin	Signal	24 AWG Color
1	Ground	Black
2	Ground	Black
3	Ground	Black
4	3.3V	???
5	3.3V	???
6	5V	???

Power Consumption

The following table shows the power consumed on each supply line for a the NL440BX/T440BX UP Server baseboard with 3 DIMMs, 4 PCI slot loads (2A @ 5V per slot), and 1 ISA slot load (1A @ 12V).

NOTE: The following numbers are provided as an example. Actual power consumption will vary depending on the exact NL440BX/T440BX UP Server configuration. Refer to the appropriate system chassis document for more information.

Table 21. NL440BX/T440BX UP Server Power Consumption

Device(s)	**3.3V**	**+5V**	**+12V**	**-12V**	**5V Standby**	
Processors	1.5A		3.4A			
Memory DIMMs	7.8A					
GTL Termination	2.0A					
82443BX	1.8A					
Baseboard	2.2A	2.5A	.1A	.1A	.8A	
Fans			.5A			
Keyboard/Mouse		.5A				
PCI slots		8A				
ISA slot		.1A	1.0A			
AGP	7.6A					
Total Current	**22.9A**	**11.1 A**	**5.0A**	**.1A**	**.8A**	**Total**
Total Power	**75.6 W**	**55.5 W**	**60.0W**	**1.2W**	**4.0W**	**196.3W**

Power Supply Specifications

This section provides power supply design guidelines for a NL440BX/T440BX UP Server -based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 22. NL440BX/T440BX UP Server Power Supply Voltage Specification

Item	Min	Nom	Max	Units	Tolerance
VOLTAGE TOLERANCE:					
3.3 Volts	3.14	3.30	3.46	V	± 5%
5 Volts	4.80	5.00	5.25	V	± 5%
+12 Volts	11.40	12.00	12.60	V	± 5%
-12 Volts	-11.40	-12.00	-12.60	V	± 5%
-5 Volts	-4.75	-5.00	-5.25	V	± 5%
5 Volts Standby	+4.75	+5.00	+5.25	V	± 5%

Table 23. Transient and Remote Sense/Sink Currents

Item	Min	Nom	Max	Units
TRANSIENT CURRENTS				
di/dt:				
5 Volts			0.5	A/µs
3.3 Volts			1.0	A/µs
+12 Volts			1.0	A/µs
-12 Volts			0.3	A/µs
-5 Volts			0.3	A/µs
5 Volts Standby			0.5	A/µs
Amplitude:				
5 Volts			7.0	A
3.3 Volts			0.5	A
+12 Volts			3.0	A
-12 Volts			0.5	A
-5 Volts			0.5	A
5 Volts Standby			0.01	A

Table 24. Ramp Rate / Ramp Shape / Sequencing / Power Good & Power On Signals

Item	Min	Nom	Max	Units	Comments
Ramp Rate(On):					
5 Volts	5		1500	ms	From 10% to within regulation
3.3 Volts	5		1500	ms	From 10% to within regulation
+12 Volts	5		1500	ms	From 10% to within regulation
-12 Volts	5		1500	ms	From 10% to within regulation
-5 Volts	5		1500	ms	From 10% to within regulation
5 Volts Standby	5		1500	ms	From 10% to within regulation
Ramp "Shape" (On & Off):					Monotonic
Sequencing: **(with respect to 5 Volts)**					See Figure 6-1
3.3 Volts	-250		+250	ms	
+12 Volts	-250		+250	ms	
-12 Volts	-250		+250	ms	
-5 Volts	-250		+250	ms	
5 Volts Standby	-1500		-	ms	
Power Good Signal					See Figure 6-2
Vil			0.4	V	
Vih	3.5			V	
Iol	4.0			mA	
Ioh			0.2	mA	
Turn On Timing requirements	100		1500	ms	
Turn Off Timing requirements	1			ms	
Power On Signal					
Vol			0.4	V	
Voh	3.5			V	

Iil	4.0			mA	
Iih			0.2	mA	

*-5V must not ramp up before +12V

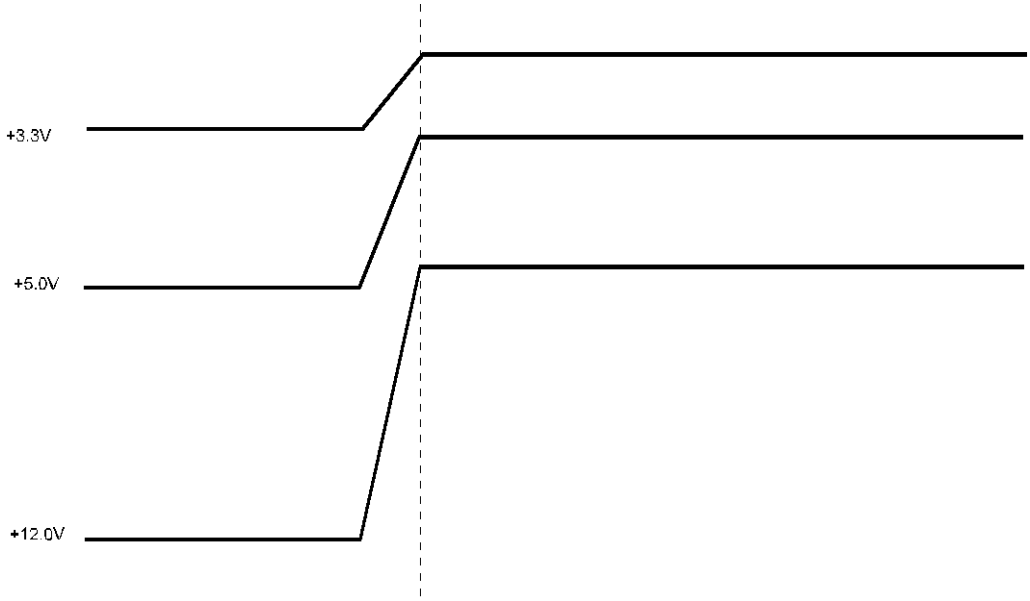
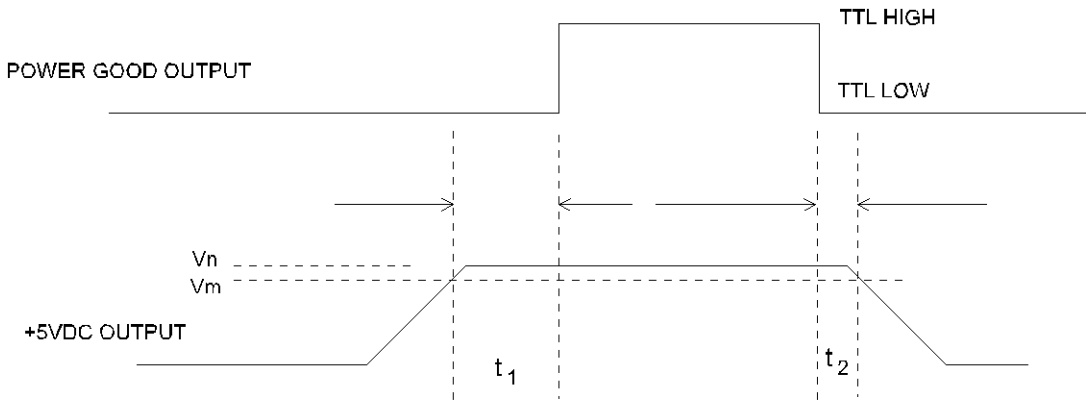


Figure 19. DC Voltage Sequencing



Vn: Nominal Output Voltage +5Vdc
Vm: Minimum Output Voltage +4.75Vdc
t1: Power Good turn on Delay (100-1500mSec)
t2: Power Good turn off time (1mSec minimum)

Figure 20. Power Good Signal Characteristics

4.3 Mechanical Specifications

The following diagrams show the mechanical specifications of the NL440BX/T440BX UP Server baseboard. All dimensions are given in inches, and are dimensioned per ANSI Y15.4M. Maximum primary-side component height is .550" unless otherwise noted. Connectors are dimensioned to pin 1. Refer to "Connector Specifications" after the diagram for more information.

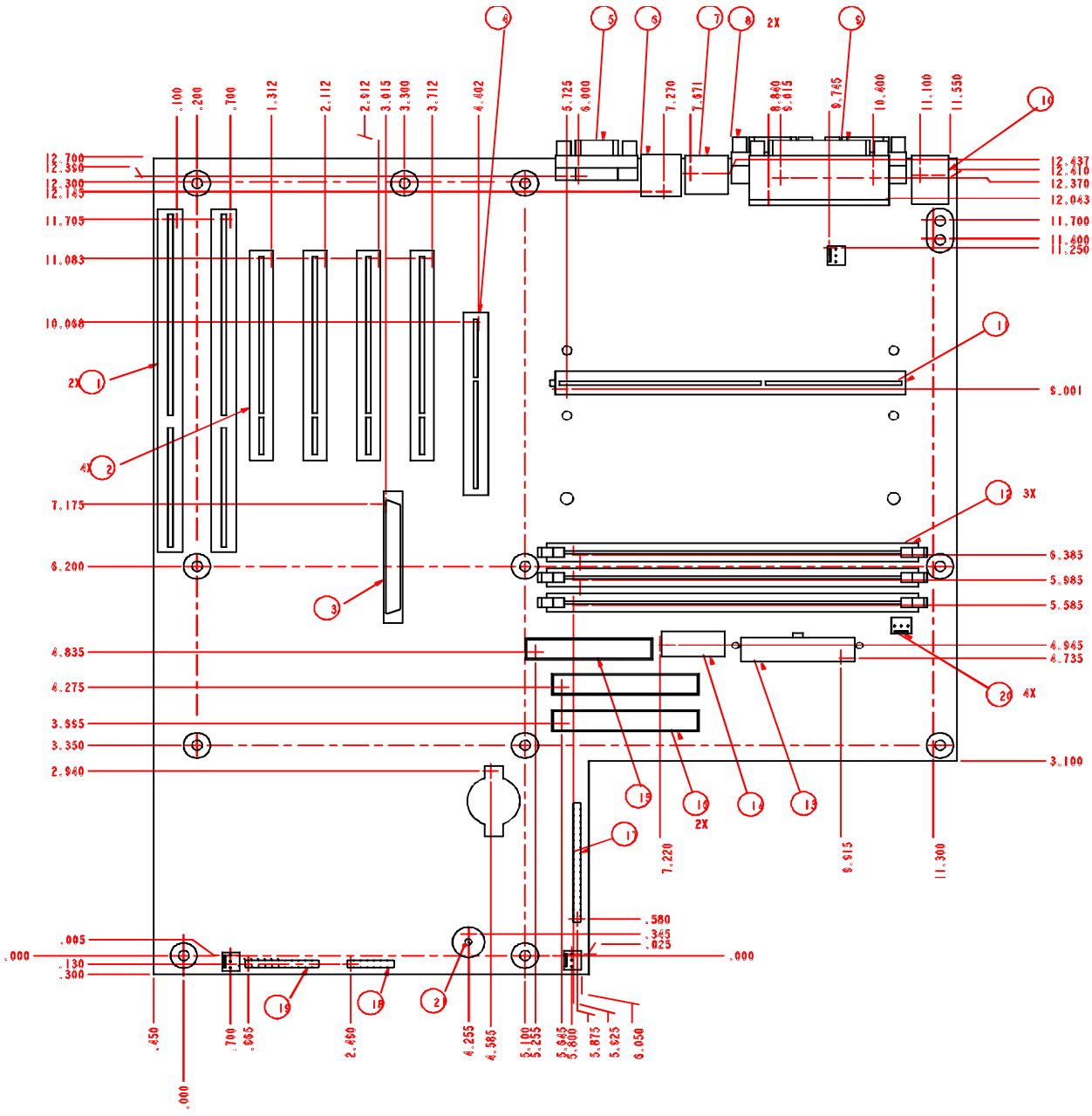


Figure 21. Baseboard Mechanical Diagram

Connector Specifications

The following table shows the quantity and manufacturer's part numbers for connectors on the baseboard. Item numbers reference the circled numbers on the mechanical drawing.

Table 25. Baseboard Connector Specifications

Item	Qty.	Mfr(s). and Part #	Description
1	2	AMP 176139-2	ISA add-in card connector
2	4	AMP 145154-4	PCI add-in card connector
3	1	FOXCONN QA01343-P4	68-pin SCSI connector
4	1	AMP 145263-1	AGP add-in card connector
5	1	FOXCONN DZ11A36-R9	15-pin VGA connector
6	1	FOXCONN UB1112C-D1	Dual USB connector
7	1	AMP 406549-4	Ethernet connector
8	2	AMP 787650-4	9-pin Serial port D-sub connector
9	1	AMP 787812-1	25-pin Parallel port connector
10	1	AMP 84376-1	Stacked keyboard and mouse connector
11	1	AMP 145251-2	242-contact slot 1 connector
12	3	Molex 71736-0004	Memory DIMM Connector
13	1	FOXCONN HM20100-P2	20-pin power connector, ATX style
14	1	FOXCONN HZ-50060-E3	6-pin auxiliary power connector
15	1	FOXCONN HL09177-P4	Floppy connector
16	2	FOXCONN HL09207-D2	IDE connector
20	4	FOXCONN HF08030-P1	3-pin System Fan Conn.
--	1	FOXCONN HF06021-P1	2-pin chassis intrusion connector
--	1	FOXCONN HF57030-C1	External Wake-On-LAN connector
--	1	AMP 640456-4	Hard drive LED input connector
--	1	Sony HL32-E2R	Battery Holder
--	1	Molex 22-44-7031	IMB connector

6. Not indicated on mechanical drawing; refer to board layout in Chapter 1.

PCI and ISA Connectors

The baseboard PCI and ISA connectors adhere to the requirements in the *PCI Local Bus Specification* and *ISA Specification*. Refer to these documents for connector specifications.

Chassis Intrusion Connector

The ATX / OPSD 2-pin standard chassis intrusion header has the following pinout. This signal is monitored by the BMC and will log an event in its event log if the chassis intrusion switch installed in the chassis generates a signal.

Table 26. Chassis Intrusion Pinout

Pin	Signal
1	Chassis Intrusion
2	GND

Connector I/O Panel

The following diagram shows the locations of serial, parallel, video, keyboard, and mouse connector interfaces on the system I/O panel, as viewed from the rear of the system.

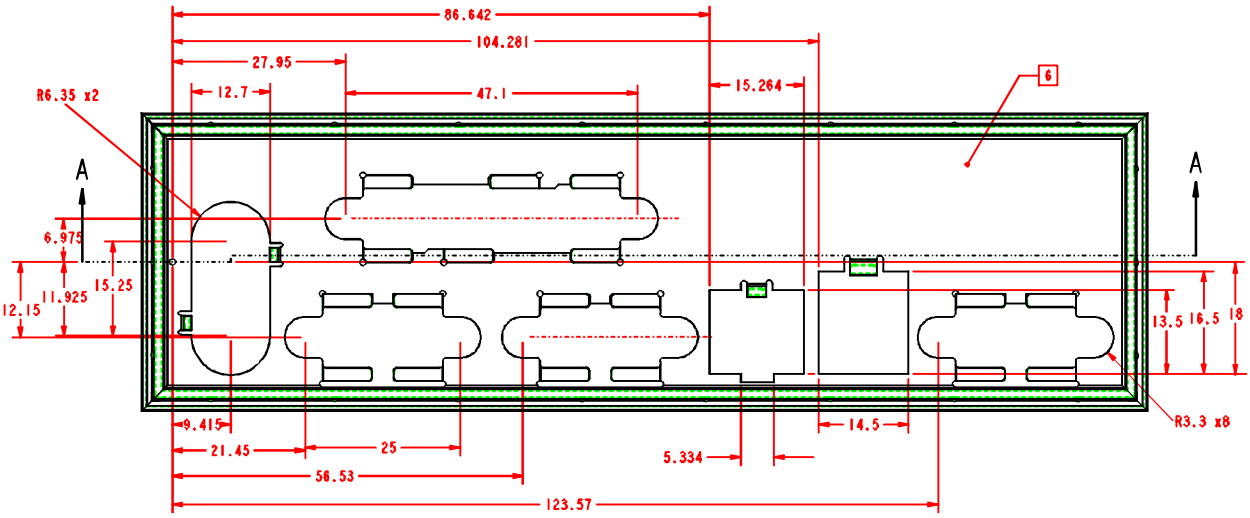


Figure 22. I/O Panel Connector Locations

7. Conventions and Terminology

Term	Definition
ACPI	Advanced Configuration Programming Interface. With respect to NL440BX/T440BX UP Server, ACPI provides the programming standard for power management features.
AGP	Accelerated Graphics Port.
AP	Application Processor. Processor not designated to boot the system in the multi-processor configuration
APIC	Intel Advanced Programmable Interrupt Controller for Symmetric Multi-processor (SMP) systems.
Asserted	Active-high (positive true) signals are asserted when in the high electrical state (near power potential). Active-low (negative true) signals are asserted when in the low electrical state (near ground potential).
Bridge	The circuitry that connects one computer bus to another, allowing an agent on one to access the other.
BSB	Back Side Bus. Pentium® II/Pentium® III processor internal interface to its second level cache operating at half core speed.
BSP	BootStrap Processor. Processor designated to boot the system in the multi-processor configuration.
BUD	Basic Utility Device. On NL440BX/T440BX UP Server, this refers to a custom ASIC for miscellaneous functions.
Byte	An 8-bit quantity.
Dword	Double word is a 32-bit quantity.
ECC	Error Checking and Correction. On NL440BX/T440BX UP Server, error correction is provided for single-bit memory errors, and error detection for multiple-bit errors.
EDO	Extended Data Out memory device
FSB	Front Side Bus. Pentium II/Pentium III processor interface to system memory and chipset operating at 100 MHz. Also referred to as the processor host bus.
GB	1024 MB
GTL	Gunning Transceiver Logic
Hard Reset	A reset event in the system that initializes all components and invalidates caches.
Kb	1024 bits
KB	1024 bytes
Mb	1024 Kb
MB	1024 KB
MB/s	Mega**bytes** per second.
Mbps	Mega**bits** per second.
Nc	Signal is not connected
Negated	A signal is negated when inactive. Active-low signal names have "_L" at the end of the name. Active-high signal names have no "_L" suffix. To reduce confusion when referring to active-high and active-low signals, the terms one/zero, high/low, and true/false are not used when describing signal states.
NIC	Network Interface Controller. On NL440BX/T440BX UP Server this function is performed by the Intel 82558 device.
NMI	Non-Maskable Interrupt. This signal is designed to be connected to a recessed push-button on the chassis Front Panel Board. Pressing this push-button causes the signal to become asserted and cause a system NMI. The signal is used as a 'diagnostic dump switch' for field diagnosis of hang problems with certain Operating Systems. These Operating Systems perform a 'core dump' on receipt of an unknown NMI. This information is used to help determine the reason for the hang.
P/d	Signal is grounded (pulled down)

p/u	Signal is pulled up or directly connected to VCC
PCI	Peripheral Component Interconnect. I/O bus for the NL440BX/T440BX UP Server baseboard.
PIIX4	PCI ISA bridge, IDE, USB, and power management controller, along with ISA interrupt, RTC, and DMA controllers.
Qword	Quad word is a 64-bit quantity.
RAID	Redundant Array of Inexpensive Disks
SDRAM	Synchronous Dynamic RAM device
SEC cartridge	Single Edge Contact cartridge packaging for Pentium® II processors.
SECC 2 cartridge	Single Edge Contact Cartridge packaging for Pentium® III Processors
SMP	Symmetric Multi-Processing
Soft Reset	A reset event in the system that forces processors to execute from the boot address, but does not change the state of any caches or peripheral devices.
Ultra SCSI	Small Computer Systems Interface (SCSI) interconnect operating at 20 MHz, providing 40 MB/s throughput with 16-bit data width.
Word	A 16-bit quantity.

6. Errata Listing

Summary Errata Table

The following tables indicate the Errata and the Document Changes that apply to the NL440BX/T440BX UP Server system. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Table

Doc:	Intel intends to update the appropriate documentation in a future revision.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	Plans	ERRATA
1	NoFix	Some mouse configurations are incompatible with NL440BX/T440BX Server.
2	Fixed	The ISA ESCD Plug-n-Play records incorrectly indicate compliance with V2.0 of the ESCD spec
3	Fix	HDD LED constantly lit if onboard SCSI disabled
4	NoFix	When selecting BIOS Boot Order, it is impossible to determine boot drive if models are identical.
5	NoFix	If PS/2 mouse is not connected Windows NT 4.0, install fails.
6	NoFix	Windows 95 fails to correctly automatically install onboard devices
7	Fixed	NL440BX/T440BX has error messages during boot of UnixWare
8	NoFix	Option ROM space is limited with NL440BX/T440BX UP Server.
9	Fix	Sensor data records cannot be read when NL440BX/T440BX Server is in +5V standby power mode.
10	Fix	FRB 3 errors are logged multiple times in the system event log.
11	Fix	Cannot clear system event log when in +5V standby power mode.
12	NoFix	Watch Dog timer Is inaccurate with timer values less than 1 second.
13	NoFix	Various vendors video cards do not operate correctly
14	NoFix	IBM 5576-B01 Kanji keyboard only works in one PS/2 port
15	Fix	Windows NT 4.0 will not boot with UPT 3334UW RAID controller installed
16	Fix	System Event Log time does not increment when system is off
17	Fix	SDR Repository information is not correct when system is powered down
18	NoFix	AMI RAID Express 762 doesn’t respond with correct PCI configuration data

NO.	Plans	DOCUMENT CHANGES
1	Doc.	The NL440BX/T440BX Server baseboard powers-on when a PCI card is inserted.
2	Doc.	Response to power button takes approximately four seconds before reaching video on boot-up using the front panel.
3	Doc.	Loading the field replaceable unit(FRU) clears the system event log and sensor data records

ERRATA

1. Some mouse configurations are incompatible with the NL440BX/T440BX UP Server

PROBLEM: The NL440BX/T440BX baseboard may not recognize some PS/2 mouse configurations. Specifically when a PS/2 mouse is attached to a 25' extension, the mouse often fails to be recognized by most operating systems. When using a switch box the user is limited to an extension cable that is no longer than 6'.

IMPLICATION: With certain operating systems, when using a long mouse extension cable the mouse will not be recognized and not be functional.

WORKAROUND: None identified.

STATUS: NoFix.

2. The ISA Extended System Configuration Data (ESCD) Plug-n-Play records incorrectly indicate compliance with V2.0 of the ESCD spec

PROBLEM: The Plug-n-Play ISA ESCD records incorrectly indicate compliance with v2.0 of the ESCD specification.

IMPLICATION: The Plug-n-Play ESCD records appear as not compliant with v2.0 or v2.1 of the ESCD specification.

WORKAROUND: Use BIOS 2.0.

STATUS: Fixed in BIOS Release 2.0, correctly indicates v2.1 compliance.

3. HDD LED constantly lit if onboard SCSI disabled

PROBLEM: In a system with an IDE only solution, where the onboard SCSI is disabled via the <Ctrl> C method and there are no SCSI devices present, the HDD LED will turn on and remain on.

IMPLICATION: Appears as if the HDD is constantly being accessed and does not represent true usage of the HDD.

WORKAROUND: Only use the BIOS F2 setup to disable the onboard SCSI.

STATUS: Fix.

4. When selecting BIOS boot order it is impossible to determine the boot drive if models are identical

PROBLEM: When using identical hard disk drives, some SCSI BIOS's present identical drive identifiers in the hard drive boot menu, making it virtually impossible to determine which drive corresponds to which logical unit number (LUN).

IMPLICATION: If two identical drives are installed, the user will not be able to determine which drive corresponds to which LUN in BIOS setup.

WORKAROUND: Some SCSI BIOS's operate differently, try a different SCSI device, or do not use identical HDD's.

STATUS: NoFix.

5. If PS/2 mouse is not connected, Windows NT 4.0 install fails

PROBLEM: When the Windows NT 4.0 install process tries to load the kernel and drivers it hangs after displaying OS version and kernel type if the PS/2 mouse is not connected.

IMPLICATION: Windows NT 4.0 cannot install without a pointing device on a NL440BX/T440BX UP Server.

WORKAROUND: None identified.

STATUS: NoFix.

6. Windows 95 fails to correctly automatically install onboard devices

PROBLEM: Windows 95 fails to correctly automatically install onboard devices, such as the NIC or SCSI. This is because the onboard devices are not listed as a know device inside Windows 95.

IMPLICATION: The onboard device might not correctly operate under Windows 95.

WORKAROUND: Windows 98 does correctly identify and automatically load the correct driver for the NL440BX/T440BX onboard devices. Windows 95 users may go to Device Manager and either delete all devices marked "Other Devices" and reboot providing driver diskette created off the NL440BX/T440BX CD-ROM disk, or select the "Other Device" and then select "Update Driver" using the driver diskette created off the NL440BX/T440BX CD-ROM disk.

STATUS: NoFix.

7. NL440BX/T440BX has error messages during boot of UnixWare

PROBLEM: Using a the onboard 83C875 SCSI controller, or a Symbios SCSI add-in card under UnixWare with the Symbios driver set version 4.2.1 may result in variations on the following error messages to be displayed to the screen during O/S boot up.

```
dstat=A0 on ha=1 has DS_BF, rp=C3BB200 dsp=2EDFC010 dcmd_dbc=00000000
dsa=00000000    Warning: running TimeToDie=X on ha=1 id=0 lun=0 tag=EC
```

Usually the system continues to boot, but occasionally the boot sequence will result in a kernel trap.

IMPLICATION: The NL440BX/T440BX appears as failing to boot UnixWare.

WORKAROUND: If the system continues to boot after these errors, it will be stable. If it does not continue to boot, a single reboot results in a stable system.

STATUS: Fixed with Symbios UnixWare driver version 4.3 (also contained in Symbios driver set family 4.3a).

8. Option ROM space limited on the NL440BX/T440BX UP Server

PROBLEM: When configuring a NL440BX/T440BX with multiple add-in cards using option ROMs, the system may skip an option ROM while scanning, if there is not enough space to load all option ROMs.

IMPLICATION: Every device requires a certain amount of option ROM space to function. The NL440BX/T440BX has C800 to E000h available for high memory. However, certain configurations will not fit inside of this space causing the system to leave out one or more add-in cards option ROMs.

WORKAROUND: Remove one or more add-in cards, or disable unnecessary options if possible.

STATUS: NoFix.

9. Sensor data records cannot be read when server is in +5V standby power mode

PROBLEM: With the power off and the NL440BX/T440BX Server system in +5V standby power mode, the sensor data records cannot be read using the emergency management console.

IMPLICATION: When querying the baseboard management controller for sensor data records, no error is given and zero SDR records are reported even when SDR records are present.

WORKAROUND: None identified.

STATUS: Fix - in a future maintenance release of the BMC firmware.

10. FRB3 errors are logged multiple times in the system event log

PROBLEM: Once the baseboard management controller has marked a processor as having a FRB 3 error, it is logged into the system event log on every power cycle boot sequence. The FRB 3 error should only be logged on the first boot-up. Using the reset button, or <Ctrl><Alt><Del>, does not log incorrect FRB 3 errors.

IMPLICATION: The number of errors in the system event log is artificially inflated.

WORKAROUND: None identified.

STATUS: Fix - in a future maintenance release of the BMC firmware.

11. Cannot clear the system event log in +5V standby power mode

PROBLEM: In +5V standby power mode with only the baseboard management controller and system event log buffer either full or partially filled, a user can, via EMP, issue the clear system event log command. It will appear to execute normally but a *Get System Event Log* information command indicates the same system event log entry count reported just before the clear. Powering the system up (booting the system) and re-sending the *Get System Event Log* command will correctly indicated the numbers of events currently logged. . Note that powering on the system will result in an event being logged (BIOS start log).

IMPLICATION: It will be necessary to power the system up and re-issue the *Get System Event Log* command to get the accurate system event log entry count.

WORKAROUND: None identified.

STATUS: Fix - in a future maintenance release of the BMC firmware.

12. Watch Dog Timer Is inaccurate with timer values less than 1 second

PROBLEM: If count down value is set to 12h or below, the timer counts down to zero very rapidly or instantaneously. On rare occasions it will count properly and count down to 08h in second intervals.

IMPLICATION: Processor test may fail which would cause the system to halt.

WORKAROUND: If it timer is set to 15h which is equivalent to 2 seconds it reliably counts down to 0 in 1 second intervals.

STATUS: NoFix.

13. Various vendors video cards do not operate correctly

PROBLEM: The NL440BX/T440BX server appears to not work correctly with the Intergraph Intense 3D100 card, the STB Velocity 128 AGP card, and the Diamond Fire GL 1000 Pro AGP card.

IMPLICATION: These video adapters do not work in the NL440BX/T440BX.

WORKAROUND: Use the onboard video or try a different video adapter card.

STATUS: NoFix.

14. IBM 5576-B01 Kanji keyboard only works in one PS/2 port

PROBLEM: The IBM 5576-B01 Kanji keyboard only works in one PS/2 port on the NL440BX/T440BX Server. This is the lower port, closest to the baseboard fiberglass,

IMPLICATION: The mouse and keyboard PS/2 ports are not interchangeable.

WORKAROUND: There are two other models of Kanji Keyboards that do function in both of the PS/2 ports. They are: "Mitac KBD-B106JP" and "Generic RT6676TJP".

STATUS: NoFix.

15. Windows NT 4.0 will not boot with UPT 3334UW RAID controller installed

PROBLEM: Windows NT returns an error initializing computer video with the UPT 3334UW installed. This happens when installing NT with the card and when adding the card to an existing configuration.

IMPLICATION: The UPT 3334UW RAID controller does not work in the NL440BX/T440BX Server.

WORKAROUND: None identified at this time.

STATUS: Fix.

16. System Event Log time does not increment when system is off

PROBLEM: When the system is powered off, but still connected to AC power, and the System Event Log is accessed via EMP or other means the time reads as the last known timestamp and it does not increment.

IMPLICATION: If there is an event (like chassis intrusion) logged to the event log while the system is powered down, that event's time stamp will read as the last known timestamp which may not reflect the time of the event.

WORKAROUND: None identified at this time.

STATUS: Fix - in a future maintenance release of the BMC firmware.

17. SDR Repository information is not correct when system is powered down

PROBLEM: When the system is powered off, but still connected to AC power, and the SDR Repository information is accessed via EMP or other means the data shown is incorrect.

IMPLICATION: The SDR repository data appears incorrect.

WORKAROUND: Do not attempt to read the SDR Repository info when the system is powered down.

STATUS: Fix - in a future maintenance release of the BMC firmware.

18. AMI RAID Express 762 doesn't respond with correct PCI configuration data

PROBLEM: AMI RAID Express 762 does not reliably respond with the correct PCI configuration information when queried by the SSU utility.

IMPLICATION: The AMI RAID Express 762 appears to be configured incorrectly, even though it is operating. It also causes the SSU conflict detection and resolution function to fail.

WORKAROUND: Inside the SSU, change the current setting of the AMI 762 from "Enabled" to "Free resources - reassign next boot".

STATUS: NoFix.

DOCUMENTATION CHANGES

1. The NL440BX/T440BX baseboard powers on when a PCI card is inserted

PROBLEM: The NL440BX/T440BX system without add-in cards installed may power on unexpectedly when a single PCI card supporting Wake-on-LAN is inserted.

IMPLICATION: PCI Power Management Specification has implemented a previously reserved pin for the PME_L signal. This is the pin used to tell the system to change power states. If the system is connected to AC power, and a card is inserted that uses this PME_L pin, yet does not conform to the specification for electrically isolating itself on that signal, may be misinterpreted as a signal to power on the system.

WORKAROUND: The power cord should be completely removed from the power supply when installing any add in cards to the system. The +5V standby voltage is still present on the baseboard even with the front panel power switch off.

STATUS: Fix - in a future release of the Product Guide.

2. Response to power button takes approximately four seconds before video display occurs on boot-up

PROBLEM: If the NL440BX/T440BX is turned off using the front panel switch before video is reached during POST there will be a four second delay in the system shutting down.

IMPLICATION: The BIOS SMI handler does not get initialized until shortly before POST 52 (video). If the power button is depressed before this time the baseboard management controller (BMC) senses the change in state and will wait for a message from the PIIX4 until its time-out period has reached about four seconds. If there is no message, the BMC will then force the system to power down.

WORKAROUND: None identified.

STATUS: Fix - in a future release of the Product Guide.

3. Loading the Field Replaceable Unit (FRU) clears the system event log and Sensor Data Records

PROBLEM: When updating the field replaceable unit, all system event log logs and sensor data records are cleared.

IMPLICATION: The system event log may be saved to a file before updating the FRU.

WORKAROUND: Always load the FRU image before loading the SDR. The SEL can be saved to disk.

STATUS: Fix - in a future release of the Product Guide.