Intel® AC450NX Server System

Technical Product Specification

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Revision History

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11/98	1.0	First external release

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Conventions and Terminology

This document uses the following terms and abbreviations:

Term	Definition
Ω	ohms
μA	0.000001 amperes
μf	microfarad
A	amperes (amps)
AC	alternating current
ACPI	advanced configuration power interface
ASCII	American Standard Code for Information Interchange
ASIC	application specific integrated circuit
BIOS	basic input output system
BMC	baseboard management controller
byte	8-bit quantity
C	centigrade
CD	compact disc
CD-ROM	compact disc read only memory
CE	Community European
cfm	cubic feet per minute
CPU	central processing unit
DC	direct current
DCD	data carrier detect
DEMKO	Danishe Elektriske Materiellkontroll (Danish Board of Testing and Approval of Electrical Equipment)
DIMM	dual inline memory module
DRAM	dynamic random access memory
ECC	error correction code
EDO	extended data out
EEPROM	electrically erasable programmable read only memory
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EMP	emergency management port
EN	European Standard (Norme Européenne or Europäische Norm)
ESD	electrostatic discharge
EU	European Union
F	Fahrenheit
FCC	Federal Communications Commission (USA)
FD	floppy disk
FET	field effect transistor
FP	front panel
FPC	front panel controller
FRB	fault resilient booting
FRU	field replaceable unit
GB	gigabyte (1024 MB)
HSC	hot-swap controller
Hz	hertz (cycles per second)
I/O	input/output

Term	Definition
I^2C	inter-integrated circuit
ICMB	Intelligent Chassis Management Bus
IDE	integrated drive electronics
IERR	processor internal error
IPMB	Intelligent Platform Management Bus
ISA	Industry Standard Architecture
ISP	in-system programmability
KB	kilobyte (1024 bytes)
kg	kilograms
kV	kilovolts (1000 volts)
LCD	liquid crystal display
LED	light emitting diode
LVDS	low-voltage differential SCSI
mA	milliamps
MB	megabytes (1024K)
mm	millimeters
MPS	multiprocessor specification
MPU	multiprocessor unit
ms	milliseconds (0.001 seconds)
MTBF	mean time between failure
NEMKO	Norges Elektriske Materiellkontroll (Norwegian Board of Testing and Approval of Electrical Equipment)
NMI	nonmaskable interrupt
NVM	nonvolatile memory
OCP	over-current protection
OEM	original equipment manufacturer
OS	operating system
OTP	over-temperature protection
OVP	over-voltage protection
PCI	peripheral component interconnect
pf	picofarad (10^{-12})
PFC	power factor correction
PHP	PCI hot plug
PIIX4	PCI-ISA IDE Xcelerator controller
PLD	programmable logic device
POST	power-on self test
RAID	redundant array of independent disks
RAM	random access memory
RPM	revolutions per minute
RxD	receive data
SAF-TE	SCSI Accessed Fault-Tolerant Enclosures
SCA	single connector attachment
SCL	serial clock
SCSI	small computer systems interface
SDA	serial data
SDR	sensor data record
SE	single ended

Term	Definition
SECC	single-edge connector cartridge
SEEPROM	serial electrically erasable programmable read only memory
SEL	system event log
SELV	safe extra low voltage
SEMKO	Sverge Elektriske Materiellkontroll (Swedish Board of Testing and Approval of Electrical Equipment)
SIO	Super I/O
SMC	Standard Microsystems Corp.
SMI	system management interrupt
SMM	server management module
SMP	symmetrical multiprocessing
SMS	server management software
TTL	transistor-transistor logic
TxD	transmit data
UART	universal asynchronous receiving/transmitting
UL	Underwriter's Laboratories
USB	Universal Serial Bus
V	volt
VA	volt amperes
Vac	volts alternating current
VCCI	Voluntary Control Council for Interference (by data processing and electronic office equipment)
Vdc	volts direct current
VGA	video graphics array
VID	voltage ID
Vin	volts in
VRM	voltage regulator module
Vrms	volts root-mean-square
W	watts
Wdc	Watts direct current

References

Refer to the following documents for additional information:

- *AC450NX OS and Adapters Priority List*
- *AC450NX Peripheral Validation Report*
- *AC450NX Server Management External Product Specification*
- *AC450NX Server system Peripheral Validation Summary*
- *Ak450NX MP Server Board Set Technical Product Specification*
- *Intel® Environmental Standards Handbook* (Doc. #662394-03)
- *Intel® Multiprocessor Specification, Ver. 1.1*
- *Intel® Multiprocessor Specification, Ver. 1.4*
- *PCI Hot-plug (PHP) Architecture and Usage Model White Paper*
- *Peripheral Component Interconnect (PCI) Local Bus Specification, Rev. 2.1 (PCI Spec., Rev. 2.1)*
- *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification*
- *SCSI Command Set for Enclosure Services Document Specification*
- *Small Form Factor-8046, Rev. 1.1*

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1. Introduction

This document describes the chassis and system level features of the AC450NX Server System. This system is a high performance server consisting of the AC450NX server system chassis and the Ak450NX board set. The features of the Ak450NX server board set are detailed in the *Ak450NX MP Server System Board Set Technical Product Specification*. The combination of these two documents provides a full overview of the AC450NX server ystem.

Features Summary

Table 1-1 provides a list and brief description of the major features of the AC450NX server system.

Table 1-1: AC450NX Server System Feature List

Feature	Description
Upgradeability	The system can be upgraded to the OCPRF100 eight-way board set.
4-way symmetric multiprocessing support	Four slot-2 connectors for the Pentium® II Xeon™ processor. The system may include 1-4 processors. Any unpopulated processor slot requires a front-side bus termination module. *Intel® Multiprocessor Specification (MPS), Ver 1.1* and *1.4* compliant with the appropriate Pentium® II Xeon™ processor.
8-GB error correction code (ECC) memory	Support of up to 8 GB of buffered EDO RAM using two memory modules.
Redundant power	The system supports three 750-W power supplies in a redundant (2 + 1) configuration, or two 750-W supplies in a nonredundant configuration. All power supplies are hot swappable.
Redundant cooling	Six system fans in a redundant (5 + 1) configuration cool the upper system (CPU and I/O). Three internal power supply fans cool the lower system (memory, peripheral bay and power supplies) in a redundant configuration when the power supply configuration is redundant (2 + 1). All fans are hot swappable.
Two hot-swap drives	Two bays, each holding 1.0” or 1.6”, 10K rpm, hot- swappable SCSI 2 hard drives. Drives can be swapped in or out of the system without being powered down.
Floppy drive	3.5-inch diskette drive bay.
CD-ROM	24x Intel® IDE CD-ROM (included, depending on configuration).
Front panel LCD	A two line LCD used to provide system status.
Add-in card support	Rail and back window support for up to 10 add-in cards.
System management ready	Intelligent Platform Management Bus (IPMB) for intrachassis communication. EMP/COM2 redirection for remote management.
ICMB support	Intelligent Chassis Management Bus (ICMB) for interchassis communication.
SCSI controller	Integrated 53C896* dual channel LVDS controller.

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2. AC450NX Server System

This chapter describes the features of the AC450NX server system chassis.

2.1 Introduction

The scalable architecture of the AC450NX server supports symmetrical multiprocessing (SMP) and a variety of operating systems. The server provides Peripheral Component Interconnect (PCI) and Industry Standard Architecture (ISA) buses.

The processor baseboard contains connectors for installing up to four Pentium® II Xeon™ processors packaged in single-edge contact cartridges (SECC). Each of the two memory boards supports up to 4 GB of error correction code (ECC) memory. The I/O baseboard contains nine PCI slots, one combination PCI/ISA slot, I/O ports and various controllers.

Figure 2-1 shows an isometric view of the chassis.

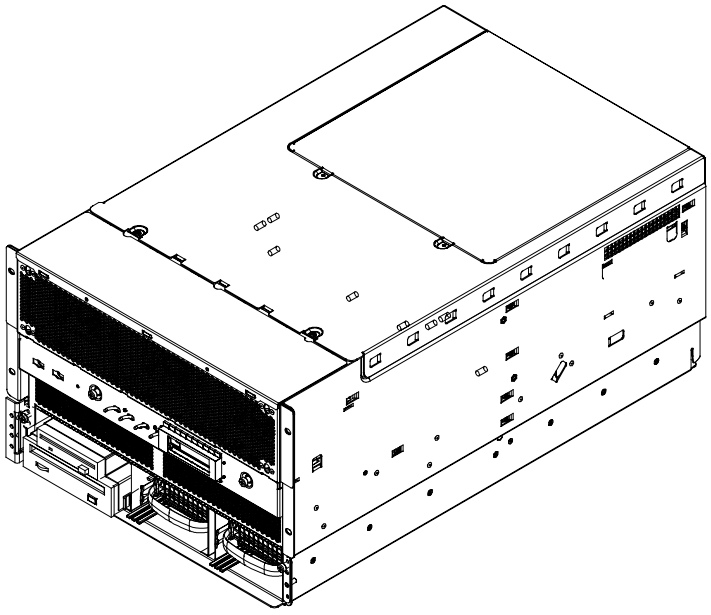

Figure 2-1: AC450NX Server System Chassis

Figure 2-2 displays the layout of the Ak450NX board set as oriented within the chassis. The processor and I/O baseboard are mounted horizontally, with the processor board toward the front of the chassis and the I/O board immediately behind at the rear of the chassis.

The midplane distributes power and signal connections to all boards except the front panel. The midplane resides between the processor and I/O board and connects these boards with the memory modules and system power supplies. The front panel resides in front of the processor board in the same plane and provides user interface, system management, and cooling system power and control.

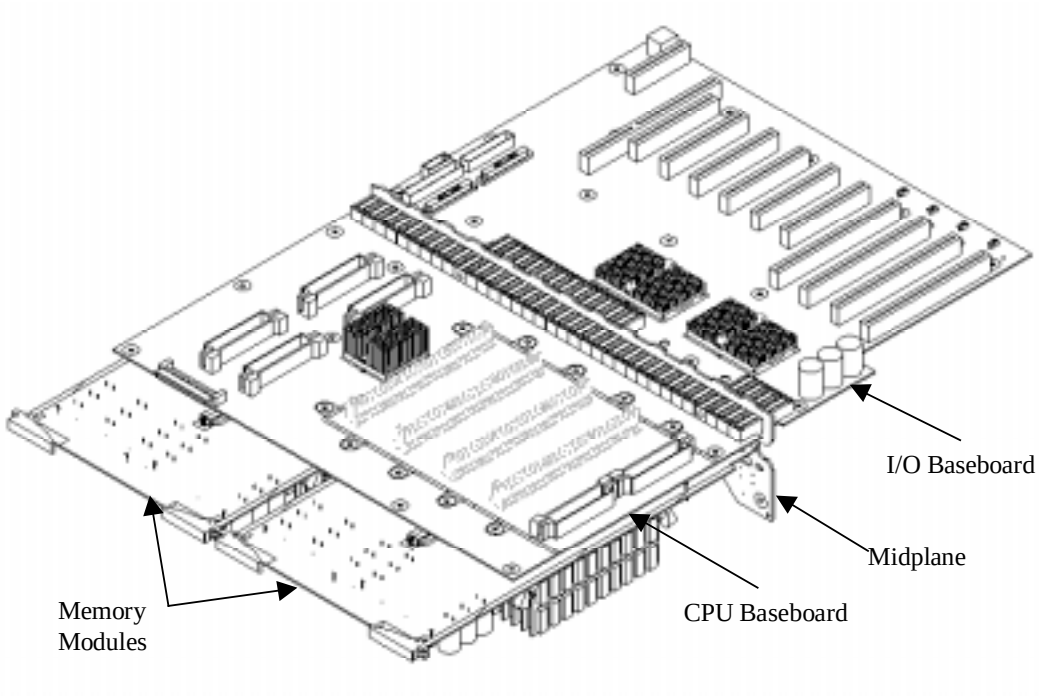

Figure 2-2: Ak450NX Board Set

The peripheral bay mounted at the lower front of the chassis supports a 3.5-inch floppy drive, a half-height 5.25-inch device (e.g., CD-ROM) and two 3.5-inch by 1.0- or 1.6-inch hot-swap hard drives. SCSI drives in the hot-swap hard drive bays can be hot swapped without shutting down the server.

The chassis supports up to three hot-swap, redundant power supplies in a 2 + 1 configuration. A cover plate for the missing supply location is supplied for systems without redundancy. These supplies provide redundant and hot swappable cooling to the memory boards and peripherals when the power supplies are in a redundant configuration.

The system design provides a hot-swap, redundant (5 + 1) cooling system for the processor and I/O baseboards. Basic controls and indicators are located on the front panel.

The front bezel can be customized for original equipment manufacturers (OEMs) to meet their industrial design requirements. It contains openings to provide adequate cooling for the chassis components, and to allow access to the peripherals.

Figure 2-3 shows a block diagram of the AC450NX server system with interconnections. PCI plug-in, redundant array of independent disks (RAID) support for the two hot-swap hard drives can be accommodated in either of the two left PCI slots (as viewed from the front of the chassis).

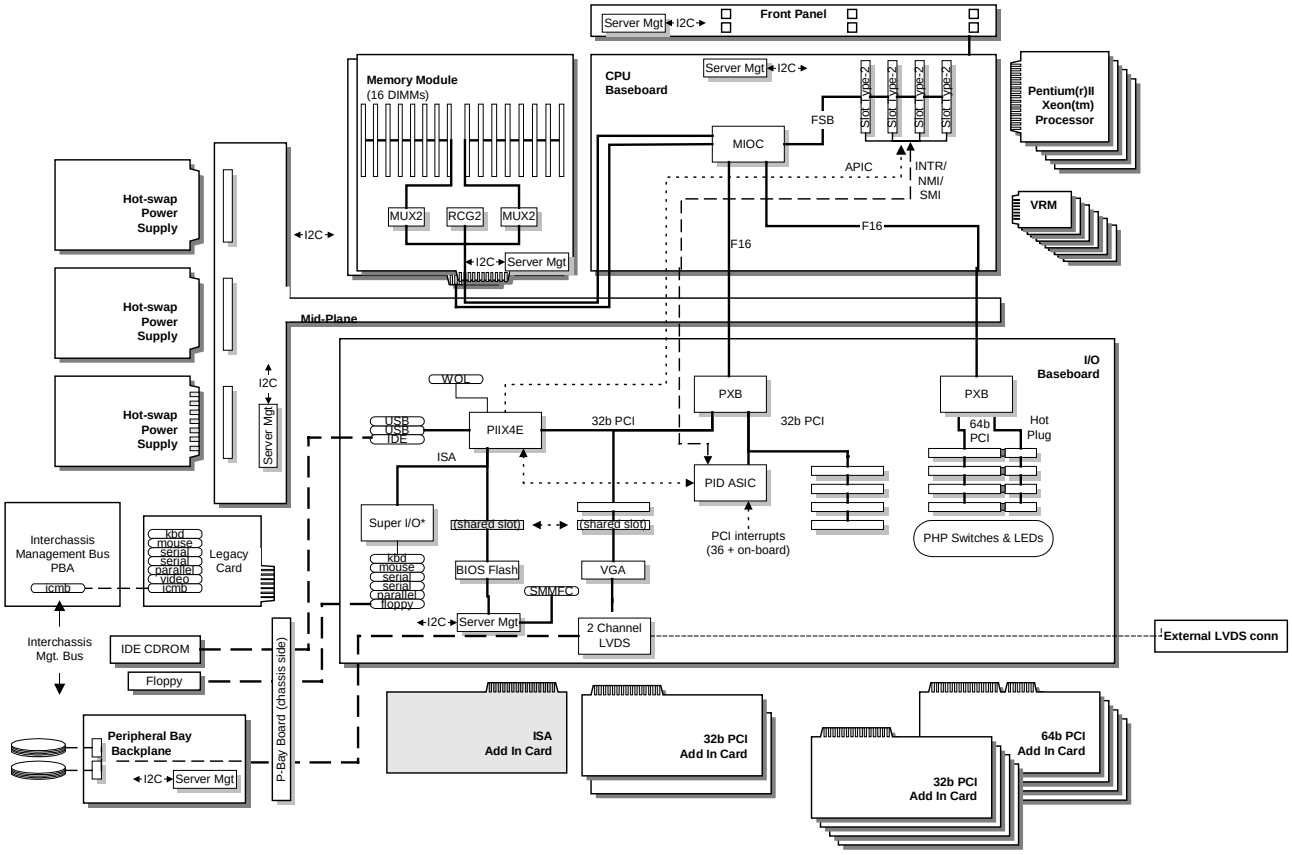

Figure 2-3: AC450NX Server System Chassis Block Diagram

2.2 External Chassis Features

2.2.1 Front View of Chassis

The front bezel of the server has two main user-accessible areas:

- Front panel liquid crystal display (LCD), switches and indicators.
- Replaceable media bays—floppy and 5.25-inch half-height bay.

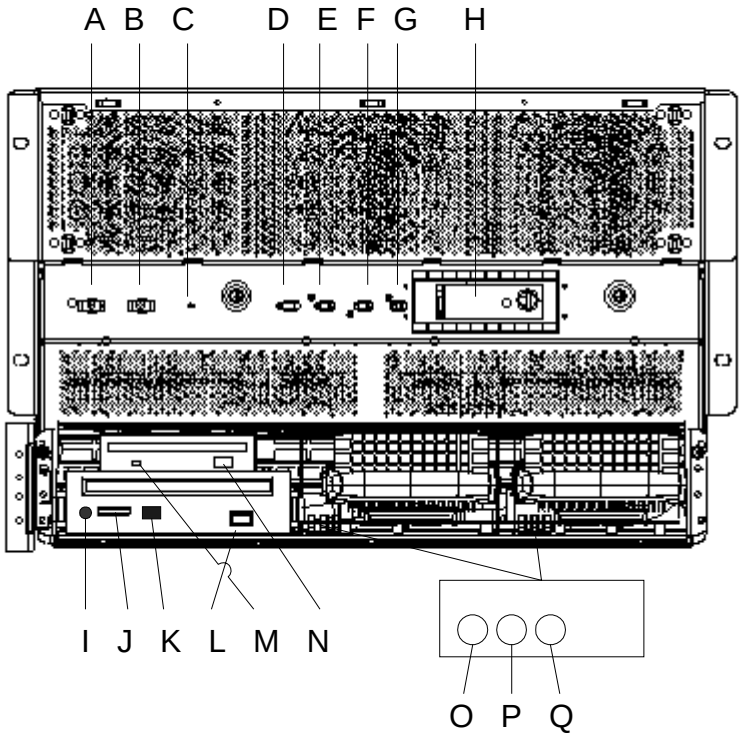

Figure 2-4: Front View of Chassis with No Bezel

Table 2-1: System Features – Front

Item	Feature	Description
Front Panel Controls and Indicators		
A	Power switch	When pressed, turns the DC power inside the server on or off.
B	Reset switch	When pressed, resets the server and causes the power-on self test (POST) to run.
C	NMI switch	When pressed, causes a nonmaskable interrupt (NMI). This switch is recessed behind the front panel to prevent inadvertent activation. (Activation requires a narrow tool.)
D	Power light emitting diode (LED) (green)	When continuously lit, indicates the presence of DC power in the server. The LED goes out when the power is turned off or the power source is disrupted. When flashing, it indicates the system is in advanced configuration power interface (ACPI) sleep mode.
E	Power fault LED (yellow)	When continuously lit, indicates a power supply failure. When flashing, indicates a 240 VA overload shutdown and power control failure.
F	Cooling fault LED (yellow)	When lit, indicates a fan failure has been detected in the server.
G	Drive fault LED (yellow)	When continuously lit, indicates an asserted fault status on one or more hard disk drives in the hot-swap bay. When flashing, indicates drive rebuild in progress.
H	Front panel LCD	Displays information about processor type and failure codes.

Item	Feature	Description
CD-ROM Drive		
I	Headphone jack	Provides a connection for headphones.
J	Volume control	Adjusts the volume of headphones or speakers.
K	Activity LED	When lit, indicates the drive is in use.
L	Open/close button	When pressed, opens or closes the compact disc (CD) tray.
3.5-inch Floppy (Diskette) Drive Descriptions		
M	Activity LED	When lit, indicates the drive is in use.
N	Ejector button	When pressed, ejects the diskette.
Status LEDs for SCSI Drives in Hot-swap Bays		
O	Drive power LED (green)	When continuously lit, indicates the presence of the drive and that drive is powered on.
P	Drive activity LED (green)	When flashing, indicates drive activity.
Q	Drive fault LED (yellow)	When continuously lit, indicates an asserted fault status on one or more hard disk drives in the hot-swap bay. When flashing, indicates that drive rebuild is in progress.

2.2.2 Rear View of Chassis

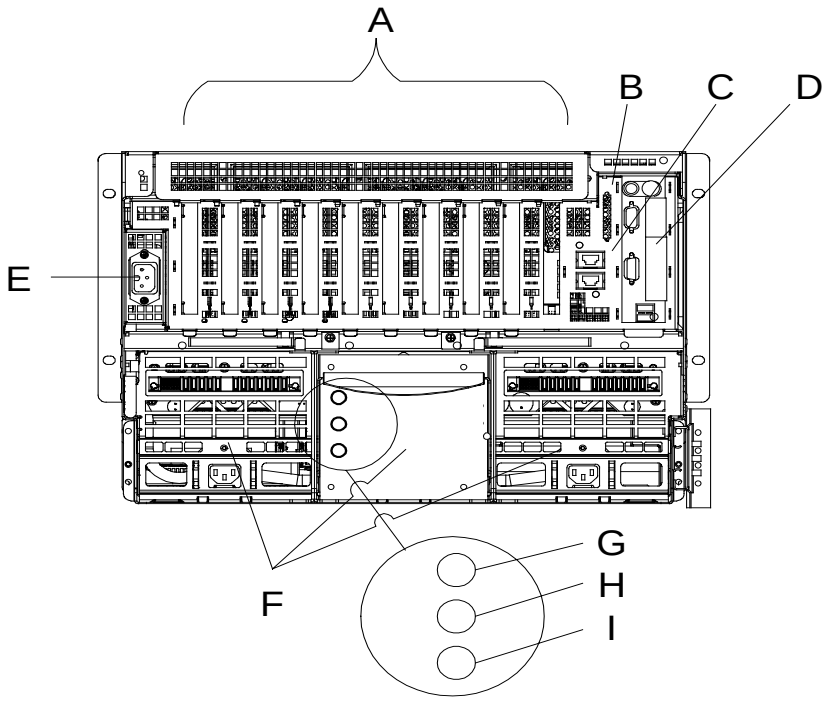

Figure 2-5: Rear View of Chassis

Table 2-2: System Features – Rear

Item	Description
A	PCI and ISA add-in board slots.
B	External low-voltage differential SCSI (LVDS) connector.
C	ICMB connectors in/out.
D	I/O riser card.
E	AC input power connector (220 V).
Power Supply Descriptions	
F	Three power supplies (one shown installed).
G	PWR LED (green) – power condition.
H	PR_FL LED (yellow) – power supply predictive failure.
I	FAIL LED (yellow) – failure condition.

2.2.3 Riser Card External I/O Connectors

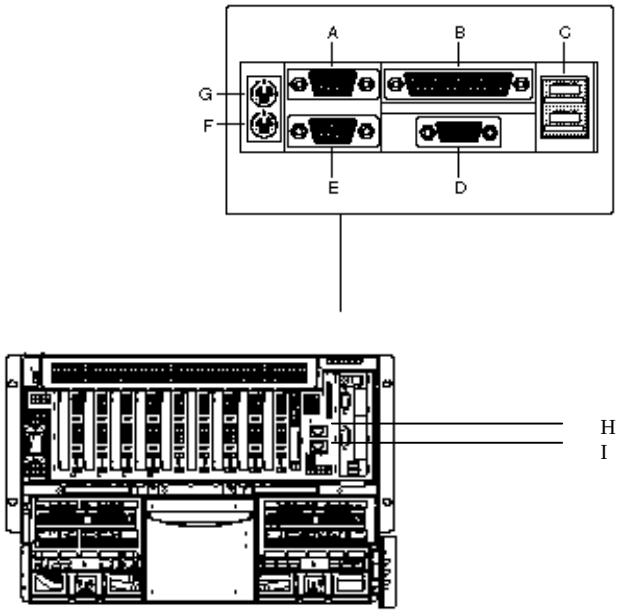

Figure 2-6: Riser Card External I/O Connectors

Table 2-3: Riser Card External I/O Connectors

Item	Descriptions
A	Serial port 1 (COM1), 9-pin RS-232 connector.
B	PS/2-compatible parallel port (LPT), 25-pin bidirectional subminiature D connector.
C	Universal Serial Bus (USB) ports 0 (upper) and 1 (lower), 4-pin connectors.
D	Super video graphics array (VGA) compatible, 15-pin video connector.
E	Serial port 2 (COM2), 9-pin RS-232 connector.

Item	Descriptions
F	PS/2-compatible keyboard port, 6-pin connector.
G	PS/2-compatible mouse port, 6-pin connector.
H	ICMB port 0, SEMCONN* 6-pin connector.
I	ICMB port 1, SEMCONN 6-pin connector.

2.3 Internal Chassis Features

2.3.1 Power System

The modular power system for the server is provided by up to three autoranging power supplies and a midplane. When connected to 100-120 Vac mains, each power supply is capable of delivering 650 Wdc. When connected to 200-240 Vac mains, each power supply is capable of delivering 750 Wdc. The power system may be configured with two power supplies (standard) or three power supplies (2 + 1, redundant). The power supplies are mounted in a 2 + 1 pattern in the back of the chassis along the bottom. Each power supply has an integrated fan for cooling. A single input connector provides power to the daisy-chained supplies.

When the server is configured with three power supplies, the user can hot swap a failed supply without affecting system functionality.

The Ak450NX midplane provides power distribution of the internal power system with minimal active circuitry. The power distribution circuitry reports quantity and location of the installed power supplies through the inter-integrated circuit (I^2C) server management. Refer to the *Ak450NX MP Server Board Set TPS* for more details on the Ak450NX midplane.

A jumper located on the midplane selects the input voltage at which the server will operate. The jumper also enables/disables the brown-out recovery feature that aids server startup during low AC input voltage conditions.

Enabling the brown-out feature ensures that all power supplies turn on when the AC input voltage reaches at least 180 Vac following an AC main brown-out condition.

Disabling the brown-out feature can cause power problems when the system tries to recover from a brown-out condition. The problems that can result depends on server AC input voltages:

- For 100-120 Vac input power after a brown-out: AC input voltage may slowly rise to its nominal level and, because of slight differences in power supply turn-on thresholds at 90 V, one power supply may turn on before the others. This power supply will most likely see too large a DC load and shut down (other power supplies may do the same), removing all DC voltages from the server.
- For 200-240 Vac input power after a brown-out: AC input voltage may slowly rise to its nominal level and the power supplies turn on at 90 V, doubling the current load on the AC main and causing them to trip.

Two supplies are capable of handling power requirements for the Ak450NX board set and peripherals with either a 100-120 Vac or 200-240 Vac nominal input. For the Ak450NX board set, this includes four Pentium II Xeon processors, 8 GB of memory, and two hard drives (typical worst case is 3.5-inch by 1.6-inch, 10,000 rpm drive).

The processor baseboard provides connectors for six voltage regulator modules (VRM). The converter input is +12 Vdc from the power supply. Each Pentium II Xeon processor core has its own converter. One converter is provided for a pair of Pentium II Xeon processor L2 caches.

The total power requirement for the Ak450NX board set exceeds the 240 VA energy hazard limit that defines an operator-accessible area. As a result, only qualified technical individuals should access the processor, memory, and non-hot-plug I/O baseboard areas while the system is energized.

Refer to *Chapter 6 System Power Supply* of this document for detailed power supply specifications.

2.3.2 DC Output Power Supply Voltages

The power supply voltages shown in Table 2-4 are distributed by the midplane to the rest of the system, with a 2 + 1 power supply redundant configuration.

Table 2-4: Available Power Supply Voltages

DC Voltage	Regulation	Ripple/Noise pk-pk	Maximum Continuous Load	OCP†† Limits	OVP†† Limits	Midplane†† Bulk Cap.
+3.3 V (VCC3)	3.25 V min. 3.35 V max.	1.5%	61.0 A	70.4 A min. 82.8 A max.	4.0 V min. 4.5 V max.	0 mF
+5 V (VCC5)	4.9 V min. 5.1 V max.	1%	68.0 A	79.2 A min. 93.6 A max.	6.2 V min. 6.5 V max.	40.8 mF ±20%
+12 V VCC12	11.76 V min. 12.24 V max.	1%	56.0 A (†) (67.0 A pk)	78 A min. 90 A max.	14.5 V min. 15.5 V max.	0 mF
-12 V (-12VCC) (1)	-12.6 V min. 11.4 V max.	1%	1.0 A	1.1 A min. 1.3 A max.	n/a	0
+5 V Standby VCC5STBY	4.75 V min. 5.25 V max.	2%	1.75 A	n/a	n/a	1 µF ±20%
+15 V Bias VBIAS	12 V min. 18 V max.	5%	200 mA	n/a	n/a	1 µF ±20%

† The regulation of –12 V to the front panel connector is +/- 10%.
†† Over-current protection (OCP); Over-voltage protection (OVP);

2.3.3 Cooling System

There are two independent cooling subsystems:

- The upper system encompassing the front panel, processor baseboard, and I/O baseboard.
- The lower system encompassing the memory boards, peripheral bay, and power supplies.

Air flows in through the bezel and exhausts out the rear of the chassis.

Cooling system redundancy to the upper system is provided by the 5 + 1 redundant fans at the front top of the system. All AC450NX server systems are redundant in factory configurations with six upper system fans. Each fan provides tachometer signal output to the front panel to indicate a fan failure. There may be time limit restrictions on service time for fan and hot-plug PCI card replacement.

Cooling system redundancy of the lower system is provided by fans integral to the system power supplies. When a redundant power supply is installed in the server, cooling of the hot-swap bay is also redundant. Each power supply fan provides tachometer signal output to the supply in which it is installed. A power supply fan failure is indicated at the front panel as a predictive power supply failure. There may be time restrictions on service time for power supply hot swap replacement.

The inlet air for the processor board, memory boards, and peripheral bay is not preheated. The I/O board receives preheated air from the processor board and the power supplies receive preheated air from the memory boards and peripheral bay.

2.3.3.1 Redundancy and Ambient Temperature Control

2.3.3.1.1 System Fans

The front panel provides either of two fan input voltages to the system fans. Under normal room ambient conditions (less than 30°C) the front panel supplies approximately 8.4 Vdc to the system fans. When either a system fan fails or the room ambient temperature exceeds 30°C, the fan input voltage is increased to approximately 12 Vdc. Following a room temperature excursion above 30°C, the fan voltage does not change back to 8.4 Vdc until the room temperature drops below 28°C and all system fans are operational.

2.3.3.1.2 Power Supply Fans

The power supply fans are controlled independently by each supply. The ambient temperature sensed at the inlet to each supply is used as the input to a control circuit which continuously varies the fan input voltage. At 28°C ambient temperature, the fan input voltage is approximately 9.0 Vdc and at 35°C the fan input voltage is approximately 13.5 Vdc.

2.3.3.2 Cooling Summary

The system fans are sized to provide cooling for up to eight Pentium II Xeon processors dissipating 65 W each. The power supply fans are sized to cool both memory modules and two 10K rpm 1.0" or 1.6" hot-swap hard drives, and for maintaining power supply function under a full load condition. See the *AC450NX Peripheral Validation Report* for information on validated hard drives. The cooling system is designed using a worst case analysis with no margin under a single fan failure (system or power supply fan) condition. The environmental conditions are summarized in *Chapter 10 Environmental Specification* of this document. Figure 2-7 summarizes the cooling provided to the system components when system and power supply fans are operating at maximum input voltage. The lower fan speed settings were chosen to meet acoustic and thermal requirements.

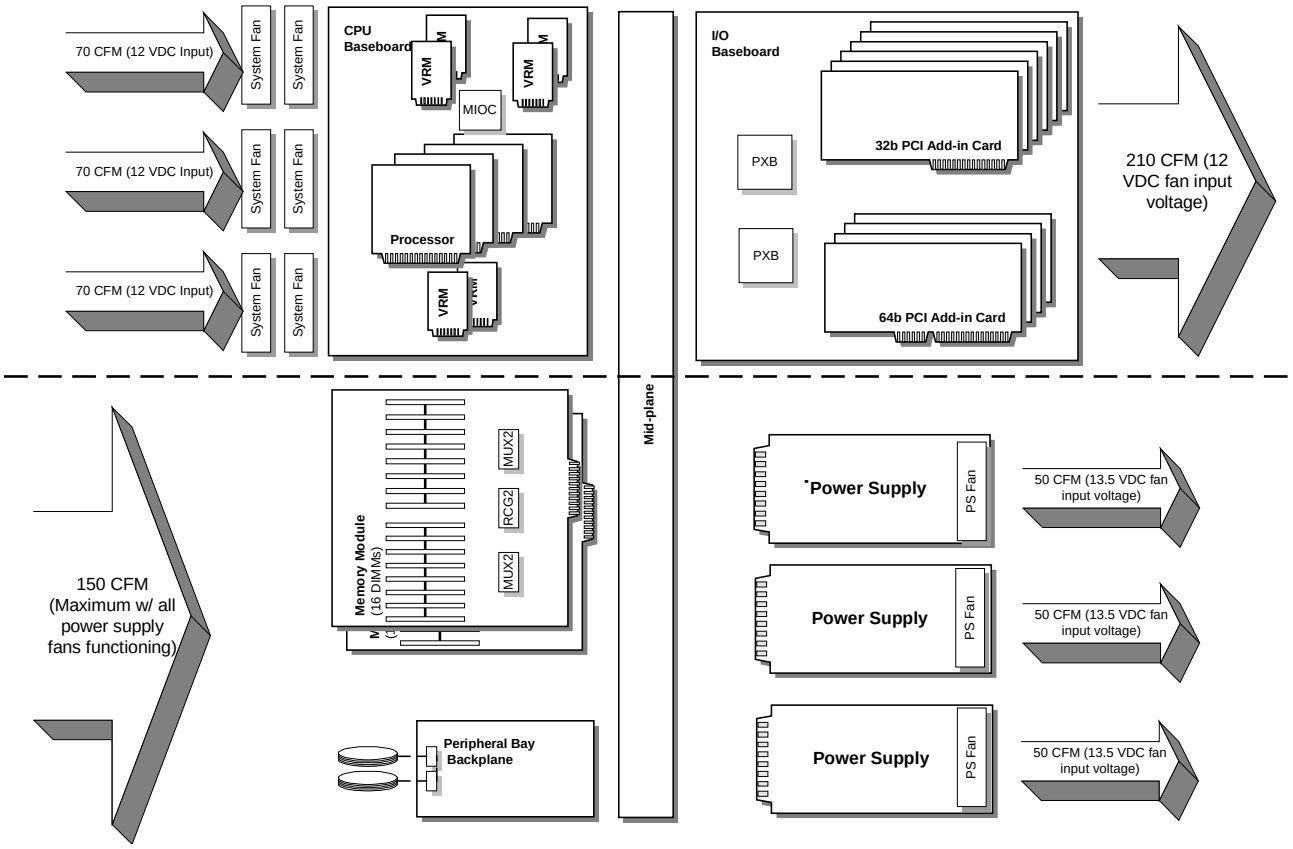

Figure 2-7: AC450NX Server System Cooling

2.3.4 PCI Hot-plug (PHP) Functionality

PCI hot-plug functionality provides a facility to replace, upgrade, or add PCI adapter cards without shutting down the server. The following is a description of the three PCI hot-plug scenarios.

- **Replace:** The user can replace a PCI card with an identical card. The replacement card will use the same PCI resources assigned to the previous card. Operating system (OS) driver will not be updated.
- **Upgrade:** The user can replace the existing card with a new version of the same card and driver software.
- **Add:** The user can add an adapter card to a previously unpopulated slot in the system.

A PHP operation requires support from the OS, the BIOS, and the PHP adapter card driver, apart from the hardware support to control the power and signals of each slot.

2.3.4.1 Goals

Replace functionality is available in the initial release of the AC450NX server system. The upgrade and add functionalities will be provided as the software elements mature.

2.3.4.2 Hardware Components

The AC450NX server system PHP implementation is based upon a discrete hot-plug controller application specific integrated circuit (ASIC). Additional components are also required. The basic components consist of:

- Power cycling and reset generation hardware that complies with the *Peripheral Component Interconnect (PCI) Local Bus Specification, Rev. 2.1 (PCI Spec., Rev. 2.1)*.
- Bus isolation switches to physically disconnect the PHP capable card from the PCI bus (these switches are located on the I/O board between each PHP PCI slot).
- LED indicators to provide service personnel with positive slot identification (these LEDs are visible when viewed from above the I/O board and from the rear of the system through holes in the chassis).
- Electromechanical hardware to prevent accidental insertion/removal from a slot while power is still present.
- Protection hardware to isolate the live components of the system from the card being inserted/removed (a mechanical barrier prevents access to I/O and CPU board components and between PCI cards; each PHP PCI connector is limited to 240 VA).
- A controller element that controls the above hardware and provides an interface for system software.

2.3.4.3 Software Components

The main software components for a PHP system are discussed below.

2.3.4.3.1 Hot-plug User Interface

- Provides user with access to the hot-plug control panel.
- Receives user input and sends a request to the hot-plug service layer.
- Displays the status of the PCI slot.
- Provides user with access to PHP functions through multiple interfaces.

2.3.4.3.2 Hot-plug Service

- Interfaces between the user interface and the hot-plug driver, and is responsible for configuring, loading, and unloading the driver component.
- Responsible for quiescing the adapter via system calls.
- Communicates to the hot-plug controller through hot-plug primitives.
- Reports adapter status to the hot-plug user interface.

2.3.4.3.3 Hot-plug Driver

- Executes request from the service layer.
- Drives the hot-plug controller.

2.3.4.3.4 BIOS

- Responsible for initialization of the hot-plug hardware components.

2.3.4.3.5 Adapter Drivers

- Allows the PHP capable card to interface with thehot-plug service.

An adapter card must be “qualified” by Intel to guarantee proper hot-plug functionality. A limited number of network and storage adapters will be qualified initially. For more information, see the *AC450NX OS and Adapters Priority List*.

For additional details on the PHP implementation, refer to the *PCI Hot-plug (PHP) Architecture and Usage Model White Paper*.

2.3.5 Drive Bays

The AC450NX server system chassis provides the following drive bays:

- One 3.5-inch floppy drive bay.
- One 5.25-inch user-accessible drive bay for removable media.
- Two 3.5-inch x 1.0" or 1.6" hot-swap bays for Ultra II* SCSI single connector attachment (SCA) hard disk drives.

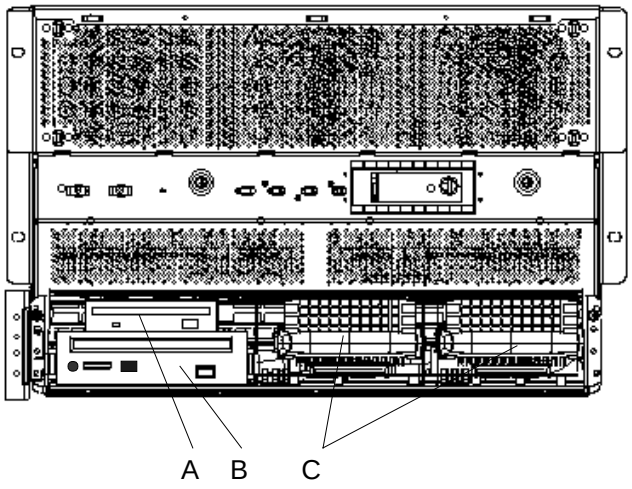

Figure 2-8: Chassis Drive Bays

Table 2-5: I/O External Connectors

Item	Bay	Description
A	3.5-inch bay	3.5 inch floppy drive
B	5.25-inch half-height bay	CD-ROM drive
C	3.5-inch x 1.0" or 1.6" bays	2 hot-swap hard drives

2.3.6 3.5-inch User-accessible Drive Bay

The system ships from the factory with a 3.5-inch floppy drive installed in this user-accessible bay.

2.3.7 5.25-inch User-accessible Drive Bay

Depending on the configuration, the system may or may not ship from Intel's factory with an integrated drive electronics (IDE) CD-ROM installed in this user-accessible bay.

Note: Installation of hard disk drives in the 5.25-inch user-accessible bays is not recommended due to cooling and electromagnetic interference (EMI) constraints.

2.3.8 3.5-inch SCSI Hot-swap Drive Bays

Two 3.5-inch hot-swap bays support either 1.0″ or 1.6″ high SCA SCSI hard disk drives. These bays are accessible following removal of the lower bezel section. The peripheral bay backplane provides industry standard 80-pin SCA-2 connectors for two drives. Two Ultra II, SCSI III SCA type hard disk drives can be installed in these bays. Extruded aluminum drive carriers with integral heat sinks that accommodate 3.5″ wide by either 1.0″ or 1.6″ height drives are required as part of the hot-swap implementation. The carrier is attached to the drive with four fasteners, and it is retained in the chassis by a locking handle.

The LEDs below each drive display individual drive status. There are three LEDs for each drive: a power (green) LED; an activity (green) LED; and a fault (yellow) LED. A fault LED on the front panel board also indicates a fault if either of these drives fail.

Note: Because all hard drives have different cooling, power, and vibrational characteristics, Intel will validate specific hard drive types in the AC450NX server system chassis. Refer to the *AC450NX Server System Peripheral Validation Summary* document for a list of these drives.

2.3.9 Server Management

The AC450NX server management architecture features several management controllers, which autonomously monitor server status and provide the interface to server management control functions. The controllers communicate via an I^2C-based serial bus referred to as the Intelligent Platform Management Bus (IPMB).

The functions of each controller are summarized in the following sections. The firmware of all the controllers is field upgradeable using the Server Management Firmware Update Utility. Refer to the *AC450NX Server Management EPS*, as well as the specifications for each of the microcontrollers for more details.

2.3.9.1 Front Panel Controller

The front panel controller (FPC) on the AC450NX server system chassis front panel board manages the front panel operations. Since this controller is responsible for system power control, it is powered from the +5 V standby output of the power supply. The FPC takes part in implementing the following system functions:

- Power and reset switch interfaces.
- Chassis field replaceable unit (FRU) inventory.
- System hard reset generation.
- System power fault indication.
- System cooling fault indication.
- Hard drive fault indication.
- Intelligent Chassis Management Bus (ICMB) bridge device.
- Emergency management port (EMP) (COM2 redirection).
- LCD interface.

2.3.9.2 Baseboard Management Controller (BMC)

The baseboard management controller (BMC) on the Ak450NX board set I/O baseboard provides server management monitoring capabilities. Associated with the BMC is a flash memory that holds the operation code. It also holds the BMC configuration defaults. The various server management functions provided by the BMC are listed below.

- Baseboard voltage monitoring
- System cooling failure detection
- Processor voltage monitoring
- Processor voltage ID (VID) monitoring
- Processor presence detection
- Processor internal error (IERR) and thermal trip monitoring
- Fault resilient booting (FRB)
- Processor disable control
- Watchdog timer
- Periodic system management interrupt (SMI) timer
- I^2C master controller
- Private management bus interface
- Server management software (SMS) and server monitor module (SMM) IPMB message receiver
- Event message receiver
- System event log management and access
- Sensor data record (SDR) repository management and access
- Processor NMI monitoring
- Processor SMI monitoring
- Time-stamp clock
- Power-on self test (POST) code log
- Secure mode, video blank, and floppy write protect
- Dual inline memory module (DIMM) ID monitoring and presence detection
- Front panel NMI monitoring
- Software front panel NMI generation

2.3.9.3 Hot-swap Controller

The hot-swap controller (HSC) on the peripheral bay backplane is connected to other system boards via the IPMB interface. The HSC provides server management information through both the IPMB and the *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification. SAF-TE* is an industry standard for communicating drive and slot status. The HSC does the following:

- Implements the *SAF-TE* command set accessed through SCSI
- Provides an IPMB path for drive presence, drive fault status, backplane temperature
- Controls the LED indicators and drive power on the AC450NX server system chassis peripheral bay backplane
- Controls drive power on and off, facilitating hot swapping of drives

2.3.10 Expansion Support

Table 2-6 summarizes the expansion support provided by the AC450NX server system.

Table 2-6: Expansion Support

Quantity	Type
6	32-bit PCI expansion bus slots.
4	64-bit PCI hot-plug expansion bus slots.
1	ISA expansion bus slot (shares a common chassis I/O expansion slot with a 32-bit PCI slot; either the ISA slot or the PCI slot can be used, but not both).
2	Single connector attachment (SCA) SCSI hard disk drive bays.
1	5.25-inch half-height drive bay. This bay contains an IDE CD-ROM drive in some factory configurations.
32	72-bit EDO DIMM module sockets (16 per memory module).

2.4 Specifications

2.4.1 Physical Specifications

Table 2-7 describes the physical specifications of the AC450NX server system.

Table 2-7: Dimensions and Weight

Height	12.25 in (311 mm).
Width	17.5 in (445 mm).
Depth	28 in (711 mm).
Weight	Approximately 132 pounds (approximately 60 kg) maximum configuration (without packing).

Notes: 1. The system weight listed above is only an approximation and can vary depending upon number of peripherals and add-in cards in the system. The above mentioned weight includes a floppy, CD-ROM, and one add-in card.

2. The system dimensions exclude the power supply handles for depth.

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3. Front Panel

This chapter describes the design and external interface of the AC450NX server system front panel. The front panel provides a user interface to the AC450NX server system via push buttons, indicator LEDs, an LCD panel, and a speaker. It also provides an interface to external systems via the ICMB. All of the front panel functions are controlled by a Philips* 80C652 microcontroller. LEDs used to indicate individual fan failure and a dual speed fan converter that controls the system fans are located on the front panel. System fan tachometer inputs are monitored by the front panel.

Features

- Philips 80C652* microcontroller
- Power, reset, and NMI push buttons
- Fan speed control, monitoring, and individual fan fail indication
- Power-off and reset security
- Power, power fail, hard drive fail, and fan fail indicator LEDs
- LCD panel, which provides boot status and other information
- Concurrent ICMB and COM2 EMP interface
- Speaker
- Operation from standby power
- Full authority power management

1.1 Introduction

This section provides an overview of the AC450NX server system front panel. It also discusses the primary components and their relationships, and provides diagrams of the physical board layout.

3.1.1 Board Overview

The AC450NX server system front panel provides a simple user interface to the AC450NX server system. Push buttons on the front panel allow for power-up and reset as well as NMI assertion. LEDs indicate when the system is powered on and when there has been a power supply failure, hard drive failure, fan or other system cooling failure. The LCD panel provides information about the system, including boot status, available number of processors, and other server management information.

The front panel also allows other systems to communicate with the server, even while power is down, via an ICMB. The ICMB is an extension of the internal IPMB. Although the control circuitry for ICMB is present on the front panel, the ICMB user interface connectors are located at the rear of the chassis.

All of the front panel's functions are controlled by a Philips 80C652 microcontroller and are available at all times when AC power is available. The connection from the front panel to the rest of the AC450NX server system is via the 80-pin connector to the Ak450NX CPU baseboard. All six system fans plug into the AC450NX server system front panel. Circuitry located on the front panel controls the fan speed, monitors individual fan tachometer signals, and indicates (via LEDs) whether an individual fan failed in the system.

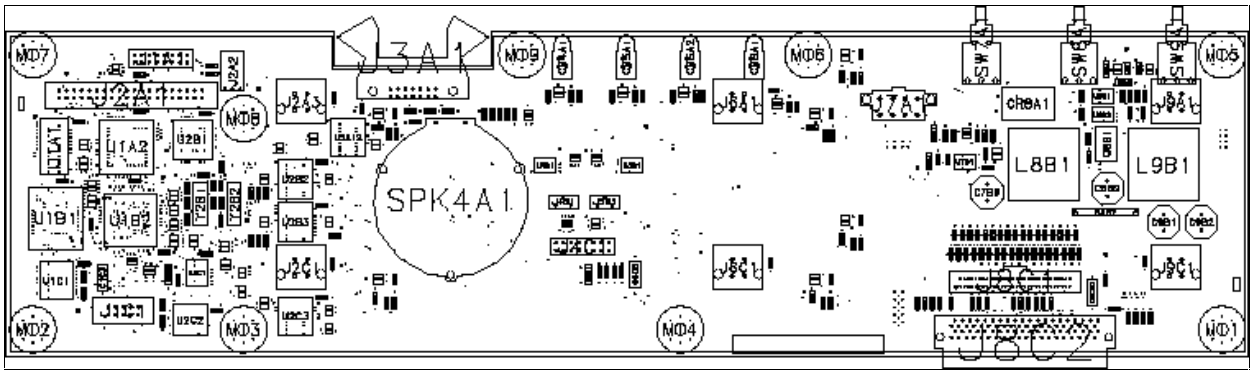

Figure 3-1: Cabot Front Panel Layout

3.2 Functional Description

This section provides a functional description of the front panel including the microcontroller, push buttons, indicator LEDs, LCD panel, ICMB, and RS-232 extension.

3.2.1 Microcontroller

All of the "intelligent" functions on the front panel are implemented with a Philips 80C652 microcontroller (also referred to in this document as the FPC. The FPC has 32KB of RAM, 7.5KB of which is accessible; and, 64KB of flash, 56KB of which is accessible. The flash contains all of the firmware the front panel needs, while the RAM is used to store the stack and local variables.

The microcontroller is always active as long as AC power is present. This power is also known as 5 V standby power, standby power, or always-alive power. The microcontroller records the current power state (on or off) in its nonvolatile memory (NVM); in the event of an AC power failure, the FPC can return the system's power status to the state it was in prior to the power failure.

The microcontroller constantly monitors the switches, the state of the power supplies (via its private I^2C bus, I2C_FPC_Sxx), and the ICMB, which is described below in further detail. While the system is powered on, the front panel also monitors the IPMB and responds to IPMB messages.

3.2.2 Memory Maps

This section contains a device maps subsection and an I/O memory maps subsection.

3.2.2.1 Device Maps

Table 3-1: Device Maps

Function	Address Range	Access	Width
Output Latch #1	FFF0 - FFFF	Write (Read RAM Shadow)	Byte
Output Latch #0	FFE0 - FFEF	Write (Read RAM Shadow)	Byte
RAM, Output Latch Shadow	FF00 - FFFF	Execute, Read, Write (Shadows Output Latches)	Byte

Function	Address Range	Access	Width
Input Latch #1	FFD0 - FFDF	Read	Byte
Input Latch #0	FFC0 - FFCF	Read	Byte
PLD	FE00 - FFFF	Read, Write	Byte
RAM # 0	E000 - FDFF	Execute, Read, Write	Byte
FLASH, OPS	1000 - DFFF	Execute, Read, Write	Byte
FLASH, BOOT	0000 - 0FFF	Execute, Read	Byte

3.2.2.2 I/O Memory Maps

Table 3-2 provides a cross reference between the I/O signals and the individual devices. These can be referenced against the device map section to resolve the absolute address.

Table 3-2: I/O Signals and Devices

Topic	Signal	Device	Address	Access	Offset	Bit
Not Applicable	Not Applicable (Muxed Address/Data BUS)	Micro Port 0	-	-	-	0 to 7
LCD	LCD_RW	Micro Port 1	-	RW	-	0
LCD	LCD_EN	Micro Port 1	-	RW	-	1
LCD	LCD_RS	Micro Port 1	-	RW	-	2
Miscellaneous	RESET_OUTPUTS_L	Micro Port 1	-	RW	-	3
ICMB/COM2	COM2_TO_SIO_EN	Micro Port 1	-	RW	-	4
ICMB/COM2	COM2_TO_FP_EN_L	Micro Port 1	-	RW	-	5
I^2C Interfaces	I2C_BACKUP_SCL	Micro Port 1	-	RW	-	6
I^2C Interfaces	I2C_BACKUP_SDA	Micro Port 1	-	RW	-	7
Not Applicable	Not Applicable (Upper Address Bus)	Micro Port 2	-	-	-	0 to 7
ICMB/COM2	MICRO_RXD	Micro Port 3	-	-	-	0
ICMB/COM2	MICRO_TXD	Micro Port 3	-	-	-	1
System Power	PWR_INTR_L	Micro Port 3	-	R	-	2
ICMB/COM2	MICRO_RXD_INTR_L	Micro Port 3	-	R	-	3
I^2C Interfaces	I2C_FPC_SCL	Micro Port 3	-	RW	-	4
I^2C Interfaces	I2C_FPC_SDA	Micro Port 3	-	RW	-	5
Processor	MICRO_WR_L	Micro Port 3	-	W	-	6
Processor	MICRO_RD_L	Micro Port 3	-	W	-	7
Reserved	Reserved	Input Latch #0	FFC0	R	-	0
Miscellaneous	SECURE_MODE_BMC	Input Latch #0	FFC0	R	-	1
ICMB/COM2	RI_TTL_FP	Input Latch #0	FFC0	R	-	2
Reserved	Reserved	Input Latch #0	FFC0	R	-	3
Reserved	Reserved	Input Latch #0	FFC0	R	-	4
System Power	PS_PWR_ON (input)	Input Latch #0	FFC0	R	-	5
ICMB/COM2	DCD_TTL_FP	Input Latch #0	FFC0	R	-	6
Reserved	Reserved	Input Latch #0	FFC0	R	-	7
Reserved	Reserved	Input Latch #1	FFD0	R	-	0
Fan Control	FAN_TACH1	Input Latch #1	FFD0	R	-	1
Fan Control	FAN_TACH2	Input Latch #1	FFD0	R	-	2
Fan Control	FAN_TACH3	Input Latch #1	FFD0	R	-	3
Fan Control	FAN_TACH4	Input Latch #1	FFD0	R	-	4

Topic	Signal	Device	Address	Access	Offset	Bit
Fan Control	FAN_TACH5	Input Latch #1	FFD0	R	-	5
Fan Control	FAN_TACH6	Input Latch #1	FFD0	R	-	6
Reserved	Reserved	Input Latch #1	FFD0	R	-	7
LCD	DB4	Output Latch # 0	FFE0	RW	-	0
LCD	DB5	Output Latch # 0	FFE0	RW	-	1
LCD	DB6	Output Latch # 0	FFE0	RW	-	2
LCD	DB7	Output Latch # 0	FFE0	RW	-	3
LED	POWER_FAIL_LED_CMD	Output Latch # 0	FFE0	RW	-	4
LED	DRIVE_FAIL_LED_CMD	Output Latch # 0	FFE0	RW	-	5
System Power	POWER_GOOD_LED_CMD	Output Latch # 0	FFE0	RW	-	6
Reset	HARD_RESET	Output Latch # 0	FFE0	RW	-	7
Fan Control	FAN_LED_CMD_1	Output Latch #1	FFF0	RW	-	0
Fan Control	FAN_LED_CMD_2	Output Latch #1	FFF0	RW	-	1
Fan Control	FAN_LED_CMD_3	Output Latch #1	FFF0	RW	-	2
Fan Control	FAN_LED_CMD_4	Output Latch #1	FFF0	RW	-	3
Fan Control	FAN_LED_CMD_5	Output Latch #1	FFF0	RW	-	4
Fan Control	FAN_LED_CMD_6	Output Latch #1	FFF0	RW	-	5
Reserved	Reserved	Output Latch #1	FFF0	RW	-	6
Reserved	Reserved	Output Latch #1	FFF0	RW	-	7
COM2	UART_ADDR	PLD	FFB0	R	27	0
Memory	FW_BOOT_PGM_EN	PLD	FFA0	R	26	0
Reset	RST_SWT_LATCH	PLD	FF90	R	25	0
System Power	PWR_CNTRL_RTC_L	PLD	FF80	R	24	0
Memory	FRC_UPDATE_L (was SPARE_JUMPER)	PLD	FF70	R	23	0
Power	POWER_CNTRL_SFC_L	PLD	FF60	R	22	0
Power	POWER_GOOD	PLD	FF50	R	21	0
COM2	UART_RESET	PLD	FF30	R	19	0
Memory	BOOT_PGM_EN_LATCH	PLD	FF20	RW	18	0
Reset	SYS_RESET_STATE_LATCH	PLD	FF10	RW	17	0
Power	PS_PWR_ON (output)	PLD	FF00	RW	16	0
FP_TO_PIIX4_PWRBTN	ACPI	PLD	FEF0	RW	15	0
COM2/ICMB	ICMB_ACTIVITY_LATCH	PLD	FEE0	RW	14	0
COM2/ICMB	COM2_ACTIVITY_LATCH	PLD	FED0	RW	13	0
Memory	I2C_CEL_CONNECT_FPC	PLD	FEC0	RW	12	0
Memory	I2C_CEL_CONNECT_BMC	PLD	FEB0	RW	11	0
System Power	PWR_GOOD_LATCH	PLD	FEA0	RW	10	0
COM2/ICMB	ICMB_EN_LATCH	PLD	FE90	RW	9	0
COM2/ICMB	FORCE_RXD_ICMB_LATCH	PLD	FE80	RW	8	0

Topic	Signal	Device	Address	Access	Offset	Bit
COM2/ICMB	FORCE_RXD_COM2_LATCH	PLD	FE70	RW	7	0
Reserved	Reserved	PLD	FE60	RW	6	0
SPEAKER	SPEAKER_LATCH	PLD	FE50	RW	5	0
System Power	PWR_RTC_TRANS_LATCH	PLD	FE40	RW	4	0
System Power	PWR_SFC_LATCH	PLD	FE30	RW	3	0
System Power	PWR_SWT_LATCH	PLD	FE20	RW	2	0
System Power	PWR_INTR_LATCH_L	PLD	FE10	RW	1	0
Memory Map	UART_INT	PLD	FE00	RW	0	0

NOTE: The programmable logic device (PLD) addresses are calculated using offset term and the following equation: ADDRESS = PLD_BASE + OFFSET * 80H

3.2.3 Memory

3.2.3.1 Program Memory, Flash

The front panel contains an ATMEL 29C512* for storing program memory and initialized variables. This device is nominally 64KB by 8 but is expandable to 128KB by 8. In order to use the 128KB by 8 devices, the memory model would need to be changed to provide enough address space, or a paging scheme would need to be incorporated.

FRU information is not stored in this device, but, rather, is stored in the serial EEPROM.

3.2.3.2 RAM

There is 32KB by 8 of RAM on the FPC. Note that only approximately 7.5KB of the RAM is accessible accordng to the memory map.

3.2.3.3 UART

A universal asynchronous receiver/transmitter (UART) is memory mapped to the microcontroller's bus to allow concurrent operation of the ICMB and EMP ports. The UART is used for the EMP interface.

3.2.3.4 Serial EEPROM/Temperature Sensor

The serial EEPROM is accessible on the FPC's private I^2C bus. A DS1621* temperature sensor is also on the private I^2C bus, which is used to sense the ambient temperature outside of the system.

Table 3-3: FRU Device Address

Device	Function	I^2C Address
24C02*	Front panel FRU information	A0h, A1h
DS1621*	Temperature sensor to detect ambient temperature	90h, 91h

The 24C02*, when accessed via the I^2C bus, provides the following FRU information. The FRU information is read by the Intel® LANDesk® Server Manager or similar management software and is available via the LANDesk Server Manager console.

The 24C02 SEEPROM has 256 bytes of programmable space, which is broken into four areas. Table 3-4 is a list of the areas, a brief description of the purpose of each area, and the space allocated to each area.

Table 3-4: SEEPROM Programming Areas

Area	Size	Description
Common header	8 Bytes	Programming offsets to the other areas below.
Internal use	80 Bytes	This area is reserved for general purpose use by Intel® server management firmware/controllers.
Chassis information	32 Bytes	Contains chassis information.
Board information	56 Bytes	Contains the board FRU information listed in Table 3-5.
Product information	80 Bytes	Available for OEM use.†

† A utility provided by Intel, called the *FRU & SDR Load Utility,* allows the OEM to program any of the FRU SEEPROM in the chassis.

Table 3-5 lists the board specific FRU information that is programmed into the board information area.

Table 3-5: FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Manufacturing date/time	Time and date of board manufacture (value programmed [in hex] is the number of minutes after 0:00 hrs 1/1/96).	000f593h (Date/time translation shown below.) f593h = 62867 min. = 43 Days & 947 min. = Feb 12, 1997, 3:47p.m.	2
Manufacturer	Board manufacturer.	Intel	1
Board product name	Board name/description.	AC450NX server system front panel	1
Board serial number	Intel board serial number.	N42385906	2
Board part number	Intel board part number.	703106-002	2

Notes: 1. Actual value programmed into the board.
2. Example value. Actual value varies with each board and/or fab revision.

Table 3-6 identifies the exact purpose for which bytes are allocated within the 24C02 SEEPROM. This information is useful for those who will be accessing the hardware directly (i.e., BIOS and server management software developers).

Table 3-6: I/O Signals and Devices SEEPROM Byte Map

Address	Length	Description	Default Value
0x00	1	Common header format version	0x01
0x01	1	Internal use area offset (8-byte multiples)	0x01
0x02	1	Chassis information area offset (8-byte multiples)	0x0B
0x03	1	Board information area offset (8-byte multiples)	0x0F
0x04	1	Product information area offset (8-byte multiples)	0x16
0x05	2	Zero padding	
0x07	1	Common header checksum	0xCE
0x08	80	Internal use area	
0x58	1	Chassis information area format version	0x01
0x59	1	Chassis information area length (8-byte	0x04

Address	Length	Description	Default Value
		multiples)	
0x5A	1	Chassis type	0x11
0x5B	1	Chassis part number type/length byte	0xCA
0x5C	10	Chassis part number	
0x66	1	Chassis serial number type/length byte	0xC9
0x67	9	Chassis serial number	
0x70	1	No more fields flag	0xC1
0x71	6	Zero padding	
0x77	1	Chassis information area checksum	0X2C
0x78	1	Board information area format version	0x01
0x79	1	Board Information area length (8-byte multiples)	0x0A
0x7A	1	Unicode country base	0x00
0x7B	3	Manufacturer date/time	
0x7E	1	Board manufacturer type/length byte	0xC5
0x7F	5	Board manufacturer (ASCII)	Intel
0x84	1	Product name type/length byte	0xDC
0x85	17	Product name	AC450NX front panel
0x96	1	Board serial number type/length byte	0xC9
0x97	9	Board serial number	
0xA0	1	Board part number type/length byte	0xCA
0xA1	10	Board part number	
0xAB	1	No more fields flag	0xC1
0xAC	3	Zero padding	
0xAF	1	Board information area checksum	0x7A
0xB0	80	Product information area	

3.2.3.5 System Event Log (SEL)

The system event log (SEL) serial EEPROM (which resides on the Ak450NX I/O baseboard on the BMC's private I^2C bus) can be accessed by the front panel's private bus under certain conditions. This feature has been added to allow access when main power is down.

When the I2C_CEL_CONNECT_FPC signal is asserted, the serial EEPROM is connected electrically to the FPC's private I^2C bus and is powered off of the 5 V standby supply.

When the I2C_CEL_CONNECT_BMC signal is asserted, the serial EEPROM is connected electrically to the I/O's private I^2C bus and is powered off of the +3.3 V supply.

When both the I2C_CEL_CONNECT_FPC and the I2C_CEL_CONNECT_BMC signals are asserted, the 5 V standby, +5 V, and the +3.3 V supplies are connected together. Firmware provisions prevent this scenario from happening.

An additional consideration is the BMC on power-up. A firmware mechanism is required to tell the BMC when this device is available.

It is required that the BMC's I^2C bus be static between 0 and 20 ms after the rising edge of the I2C_CEL_CONNECT_BMC signal.

Upon power-up, the I2C_CEL_CONNECT_BMC signal is asserted and the I2C_CEL_CONNECT_FPC is deasserted.

3.2.4 Front Panel Indicator LEDs

The POWER_FAIL LED is under the control of the FPC. When the FPC asserts (high) the POWER_FAIL_LED_CMD signal, the LED becomes illuminated. This LED is off when deasserted and during an FPC reset. This LED is powered off 5 V standby so it can be illuminated even when +5 V is invalid.

The DRIVE_FAIL_LED is an indication of hard drive failure. It is illuminated when the DRIVE_FAIL_LED_CMD signal is asserted (high). It is off when this signal is deasserted (low) and during an FPC reset.

The POWER_GOOD_LED is an indication of good DC power in the system. It is illuminated when the POWER_GOOD_LED_CMD signal is asserted (high). It is off when this signal is deasserted (low) and during an FPC reset.

The FAN_FAIL_LED is under the control of the BMC. The FPC queries the BMC for system fan fail status. It illuminates when the FAN_FAILED_L signal is asserted (low) from the BMC. It is an indication of system cooling failure. Additionally, there is an LED associated with each fan. These LEDs are located adjacent to each individual fan to provide an indication of which of the six system fans has failed. These LEDs are driven by the FPC.

3.2.5 Front Panel LCD

The front panel LCD is a Stanley GMD1620A*. The LCD and the LCD's LED backlighting unit are powered off of the main +5 V. Therefore, this capability is only available when the +5 V power is available.

In order to avoid loss of 5 V standby power and LCD latch-up, the firmware must comply with the following. When main power is OFF, all signals driving the LCD should be disabled or driven low. These include the D0 through D3, RW, EN, and RS signals. Also, when main power is removed the LCD signals should be brought to this safe state within 200 µs.

3.2.6 System Power

3.2.6.1 Power Supply Monitoring

Each of the three supplies has three signals that can be monitored. These are the PS_PRES, PS_FAULT and the PRED_FAIL signals. These are available via the private I^2C bus.

3.2.6.2 Power Interrupt Routing

There are three hardware signals that can initiate power cycling. They are the real time clock (RTC) (PWR_CNTRL_RTC_L), the Intel® SMM card (PWR_CNTRL_SFC_L), and main power going out (PWR_GOOD). These are accessed via the PWR_RTC_TRANS_LATCH, the PWR_SFC_LATCH, and the PWR_GOOD_LATCH signals per the memory map. Upon assertion, each of these signals is individually latched in the programmable logic device (PLD). The asserted state remains latched even if the signal becomes deasserted. The asserted state remains latched until the latch is read by the microcontroller. When read by the microcontroller, the latch becomes cleared.

The PWR_CNTRL_RTC_L transition latch (PWR_RTC_TRANS_LATCH) becomes set (asserted) on either transition of the PWR_CNTRL_RTC_L signal. When set, the latch remains set until read by the FPC. Note that by reading the PWR_RTC_TRANS_LATCH latch it is not possible to obtain the absolute state of the PWR_CNTRL_RTC_L signal. Therefore, the PWR_CNTRL_RTC_L signal can also be read by the FPC.

The PWR_CNTRL_SFC_L latch (PWR_SFC_LATCH) becomes set (asserted) on a high to low transition of the PWR_CNTRL_SFC_L signal. When set, the latch remains set until read by the FPC. When the latch is read, it

becomes cleared and remains cleared until the next high to low transition of the PWR_CNTRL_SFC_L signal. The state of the PWR_CNTRL_SFC_L signal can also be read directly.

The PWR_GOOD_LATCH becomes set (asserted) when the PWR_GOOD signal has a high to low transition. This occurs when main power goes bad. Once read, the latch is cleared and will not be set until the next high to low transition. The state of the POWER_GOOD signal can also be read directly. Each of these three latches is fed into a fourth latch (PWR_INTR_LATCH_L), which drives the PWR_INTR_L signal. The PWR_INTR_L signal drives the FPC's INT0 input. This latch is asserted (low) if **any** of the power cycle signals become asserted (high). This latch signal is deasserted (high) whenever it is read, as long as all three inputs are also deasserted.

All four latches may be read by the microcontroller. Reading by the microcontroller causes the latch to be deasserted (assuming that the asserting signal is also deasserted.)

With this interrupting scheme, it is suggested that the FPC use the power interrupt in level mode, not edge mode. This is because a reassertion of an interrupting source at the wrong time could prevent the interrupt pin from being toggled.

3.2.6.3 Front Panel Power Switch

The paramount design concern is the capture of an asserted switch with a microcontroller/firmware design that experiences starved threads, specifically the thread that polls the power switch. (In normal real time control, a starved thread is an indication of abnormal operation that would cause a fatal error and abortion of microcontroller operation.) This is addressed by latching the asserted state in hardware via the PWR_SWT_LATCH. This latch is set whenever the switch is asserted. Whenever the switch is read, the latch is cleared. Therefore, when the starved thread regains the FPC, it can read the latch. If the switch was asserted after the last polling, the latch will read a one.

3.2.6.4 Hardware Control of Power Supply ON Command

The following describes the hardware control over the PS_PWR_ON (output) signal. The FPC has only marginal control over this signal. The system-power-on command (PS_PWR_ON) is asserted by the FPC via the PS_PWR_ON (output) signal, **as long as** there is not a 240 volt-amp incident.

3.2.6.5 Default Power State

The default power state is OFF. This is the state that the front panel commands for the main power via the PS_PWR_ON (output) signal. During normal operation the firmware must assert the PS_PWR_ON (output) signal to turn the supplies on. This is controlled from the PLD. During a firmware-driven PLD download, the PLD's outputs become tristated. When tristated, the power supplies are commanded on via an external pull-up resistor.

3.2.6.6 Dual Speed Fan Power

The system cooling fans typically operate at low voltage to minimize acoustic noise. Under normal conditions, the fans run at this slower, quieter speed. When a fan failure is sensed, the fan speed is set to high. Also, if the ambient temperature sensor reads 31 degrees or higher, the fan speed will be set to high (there are 2 degrees of hysteresis built into this algorithm, so the ambient temperature must drop to 29 degrees before the fan speed is reduced to low again). The high/low decision is made by the FPC, via the FULL_FAN_SEL_L signal.

The fan voltage is derived via a buck converter from 12 V, and is current limited at 9 A. Maximum current during high speed operation is 5.04 A.

3.2.7 Reset

3.2.7.1 Resetting the System

The FPC has the capability to reset the entire system (processors, chip sets, etc.) by asserting the HARD_RESET signal. It must be asserted for a minimum of 500 ms. There is no maximum.

3.2.7.2 Reset Inputs

The state of the reset switch can be determined by reading the RST_SWT_LATCH signal within the PLD. If the reset switch has been asserted since the previous reading of this latch, then the latch will be asserted (high). Reading of this latch clears the latch. Therefore, there are no minimum polling requirements to detect an asserted switch. The latch is asynchronously set whenever the switch is pressed and remains set as long as the switch is pressed, whether or not the latch is read by the FPC.

3.2.7.3 Reset Switch During +5 V Power Cycle

While +5 V power is inactive, the RST_SWT_LATCH remains asserted. This is because the reset switch circuitry incorporates a pull-up to main +5 V, and when main power is off, the main +5 V power is at 0 V, making the switch appear asserted. This pull-up is tied to main +5 V to save power on +5 V standby.

The RST_SWT_LATCH might remain asserted up to and including the first read after the PWR_GOOD indicates that main +5 V power is valid. The first valid RST_SWT_LATCH read occurs on the SECOND READ after PWR_GOOD becomes asserted (high).

3.2.7.4 Resetting the FPC

The FPC is reset whenever the VCC_STDBY is invalid and 500 ms (typically) after VCC_STDBY becomes valid. The front panel has development support for a push button reset input. Removing the default RP1A1 and connecting a switch between J1A1 pins 3 and 4 activates this by controlling the PUSH_BTN_RST_L signal.

3.2.7.5 Determining the System Reset State

Signal PROC_RESET _LATCH provides firmware with an indication of the processor reset state. A latch is used because a processor reset assertion may last as short a period of time as 40 ns, and as long as many seconds. Therefore, an assertion of the PROC_RESET_L signal causes the PROC_RESET _LATCH to become set. When the signal is read by the FPC, the latch is cleared (assuming the PROC_RESET_L signal is no longer asserted).

To determine whether an assertion of the PROC_RESET_L signal has occured since the last reset **and** the current state, read the PROC_RESET_LATCH twice. If PROC_RESET_LATCH returns sequential ones, then the processors are currently in reset. If PROC_RESET_LATCH returns one, then zero, the processors have gone through reset since the last time the latch was read, but are not currently in reset. If PROC_RESET_L returns two zeroes, the processors have not gone through reset since the last time the latch was read.

Whenever the front panel goes through a hardware reset this latch is cleared.

3.2.7.6 Development and Test Reset

In development and board testing the PLD and microcontroller can be put into a reset state by asserting the PB_RST_L signal.

3.2.8 Speaker

The front panel contains a speaker that is controlled by either the FPC or the I/O board. The speaker is energized if either source commands the speaker on. The speaker impedance is approximately 8 ohms.

The FPC commands the speaker on by setting the PLD's SPEAKER_LATCH. This latch also can be read. The state of the I/O board's speaker command cannot be read by the FPC.

During reset the SPEAKER_LATCH is set to deasserted (off, low).

3.2.9 Fan Control

There are six fans which plug into the front panel board. Each fan is powered from the VCCFAN supply (see *Section 3.2.6.6, Dual Speed Fan Power*). Each fan also has a tachometer out signal, which is fed into Input Latch #1, to be monitored by the FPC. If a fan is determined to have failed, the FAN_FAILED_L signal turns on the yellow fan failed LED on the front panel. Also, an LED near the fan that has failed is illuminated by the FPC (via Output Latch #1).

3.2.10 ICMB and COM2 Redirection

The ICMB/COM2 redirection circuitry provides a number of capabilities. These capabilities are dealt with individually in the following subsections.

3.2.10.1 Receive Auto Switching

Both the COM2 RXD (received) and the ICMB RXD signals are routed to the front panel and are continuously available, regardless of the state of any other control signals. In certain conditions it is desirable to monitor both signals and to switch to whichever signal goes active first into the FPC's RXD input. This section covers such an auto-switch capability, implemented in the PLD.

The FP PLD supports auto-switching of the first-active incoming RXD signal into the incoming RXD signals. The auto-switch is enabled by deasserting both the FORCE_RXD_ICMB_LATCH and the FORCE_RXD_COM2_LATCH. When these are both deasserted by firmware, the PLD goes into auto-switch mode.

Upon RXD activity, the microcontroller can determine which RXD signal is routed to the microcontroller by reading the states of both FORCE bits within the PLD. Only the FORCE bit corresponding to the switched RXD (ICMB or COM2) signal becomes asserted. In no case will both FORCE bits become asserted.

3.2.10.2 Receive Forced Switching

In certain cases it is desirable to force a specific RXD (COM2 or ICMB) into the FPC's RXD input. This section covers this forced switch capability.

To force the ICMB's RXD signal into the FPC's RXD input, assert the FORCE_RXD_ICMB_LATCH and deassert the FORCE_RXD_COM2_LATCH.

To force the COM2's RXD signal into the FPC's RXD input, assert the FORCE_RXD_COM2_LATCH and deassert the FORCE_RXD_ICMB_LATCH.

The following (or equivalent) sequence occurs in firmware. **The deassertion must occur whether or not it had previously been asserted.**

1. Disable interrupts.

2. Assert desired FORCE bit.
3. Deassert undesired FORCE bit.
4. Enable interrupts.

There is no guarantee that incoming RXD streams will be coherently switched in the hardware. It is probably a good idea to discard any immediate UART receptions after a switch.

3.2.10.3 Receive Interrupt

The microcontroller interrupt number one is programmed in the PLD to be logically the same as the microcontroller's RXD input.

3.2.10.4 Receive Activity Detection

A completely independent circuit monitors activity on the ICMB and COM2 receive inputs. This allows bus activity monitoring regardless of the state of the auto-detect switch. Note that the receive (RXD) inputs from both COM2 and ICMB are always available to the front panel, regardless of the states of the COM2_TO_FP_EN_L and the COM2_TO_SIO_EN signals.

The ICMB_ACTIVITY_LATCH becomes set when the SIN_TTL_ICMB signal becomes asserted (low). This assertion corresponds to receive activity. The latch remains asserted (set) until read by the FPC at which time the latch is cleared. The latch remains cleared until the next activity on this line is detected.

The COM2_ACTIVITY_LATCH becomes set when the SIN_TTL_COM2 signal becomes asserted (low). This assertion corresponds to receive activity. The latch remains asserted (set) until read by the FPC at which time the latch is cleared. The latch remains cleared until the next activity on this line is detected.

3.2.10.5 ICMB Transmit Control

The FPC's TXD (transmitted) pin drives both the COM2's SOUT_TTL_COM2 signal and the ICMB's SOUT_TTL_ICMB signal. There is no interlock for preventing the FPC from simultaneously transmitting on both ICMB and COM2; in fact, this capability could be desirable.

The FPC drives the ICMB bus with the FPC's TXD output whenever the ICMB_EN_LATCH is asserted (high).

3.2.10.6 COM2 Transmit Control

The COM2 transmit signals are connected to either the FPC or the SMC Super I/O* (SIO) chip depending on the states of the COM2 signals. Note that this discussion is limited solely to the TXD signals since this is the only signal that the FPC can control.

The routing of COM2 to the SMC I/O chip or FPC and the routing of the ICMB to the FPC is controlled by two signals, COM2_TO_FP_EN_L and COM2_TO_SIO_EN. Note that if these two signals are not carefully controlled by firmware, the VCC_BACKUP can be shorted to ground. The VCC_BACKUP is shorted to ground via the SIO's power pins. In this case, the power supplies will cycle the entire system and component damage may occur. **When switching between enabling of these routings, it is important never to enable both these signals at the same time.**

Table 3-7 shows the allowed combination of states.

Table 3-7: Allowed Combination of States

Main Power	COM2_TO_FP_EN_L	COM2_TO_SIO_EN	Result
OFF	Deasserted (1)	Deasserted (0)	COM2 disconnected ICMB available†
ON	Deasserted (1)	Deasserted (0)	COM2 disconnected ICMB available†
OFF	Asserted (0)	Deasserted (0)	COM2 routed to front panel ICMB available†
ON	Asserted (0)	Deasserted (0)	COM2 routed to front panel ICMB available†
ON	Deasserted (1)	Asserted (1)	COM2 connected with SMC* ICMB available†
All Other States			Possible main power cycle Possible component damage

† ICMB available means that if the ICMB_SOUT_EN signal is asserted then the FPC will transmit to the ICMB bus. The data that is transmitted comes from the microcontroller's TXD output pin. Note that this capability is independent of the states of the COM2_TO_SIO_EN and COM2_TO_FPC_EN signals; it depends only on the state of the ICMB_SOUT_EN signal.

To switch between the SMC and FPC connection of COM2, both signals should be deasserted before either signal is asserted.

When main power is off, the COM2_TO_SIO_EN signal should never be asserted.

3.2.10.7 Transmit and SMC/Front Panel Connection Control

The FPC's interrupt 2 input is logically the same signal as the signal connected to the FPC's RXD pin. The description in this section, therefore, applies to both signals.

The FPC's TXD pin drives both the COM2's SOUT_TTL_COM2 signal and the ICMB's SOUT_TTL_ICMB signal.

3.2.10.8 COM2 Data Carrier Detect (DCD) Input Signal

The COM2's data carrier detect (DCD) input is availabe as signal name DCD_TTL_FP. This input is available to the firmware at all times, regardless of the states of any ICMB and COM2 control signals. This signal is a direct pass through from the COM2 port. The memory map location is described in *Section 3.2.2 Memory Maps*.

3.2.11 Front Panel Push Buttons

The AC450NX front panel has three momentary-contact push button switches: power, reset, and NMI. The power and reset switches are easily accessible by the user, whereas the NMI button is accessible only via a "pinhole" protective cover. The power switch controls main system power. If the system is powered off, pressing this button will always turn system power on. However, if the system is on, the microcontroller qualifies this button press with the current security state of the system, and decides whether the system is actually to be powered off.

The power switch is available to the FPC and is described in Section 3.2.6.3.

The reset switch is available to the FPC and is described in Section 3.2.7.4.

3.2.11.1 Switch Debounce

Table 3-8 describes the debounce characteristics and requirements for all push button switches.

Table 3-8: Debounce Characteristics and Requirements

Event	Mininum (milliseconds)	Typical	Maximum (milliseconds)
Switch Press Ramp (High-Low)	0	20	200
Switch Release Ramp (Low-High)	0	12	150
Required switch cycle duration detection by firmware	50†	20	Infinity
Potential Switch Cycle characteristics (Press to Release) [no firmware requirements derived from this row]	0	200	Infinity

† Note that although the keypad press-release cycle may be as short as zero, worst case, the firmware is only required to detect a cycle as short as 50 ms.

3.2.11.2 NMI Switch

The NMI push button is hidden behind the main front panel bezel, except for a small “pinhole” access hole. This is done to prevent inadvertent activation of the NMI switch. The NMI switch is routed directly to the BMC. There is no interface to the FPC.

3.2.12 I^2C Interfaces

The FPC interfaces to two I^2C buses; the FPC’s I^2C bus and the global I^2C bus. These are described in the following subsections.

3.2.12.1 The FPC Private I^2C Bus

The FPC’s private I^2C bus is used for the FPC to communicate with dumb I^2C devices that do not support multimaster mode. These are shown in Figure 3-2.

AC450NX
FPC Private I2C Bus Diagram

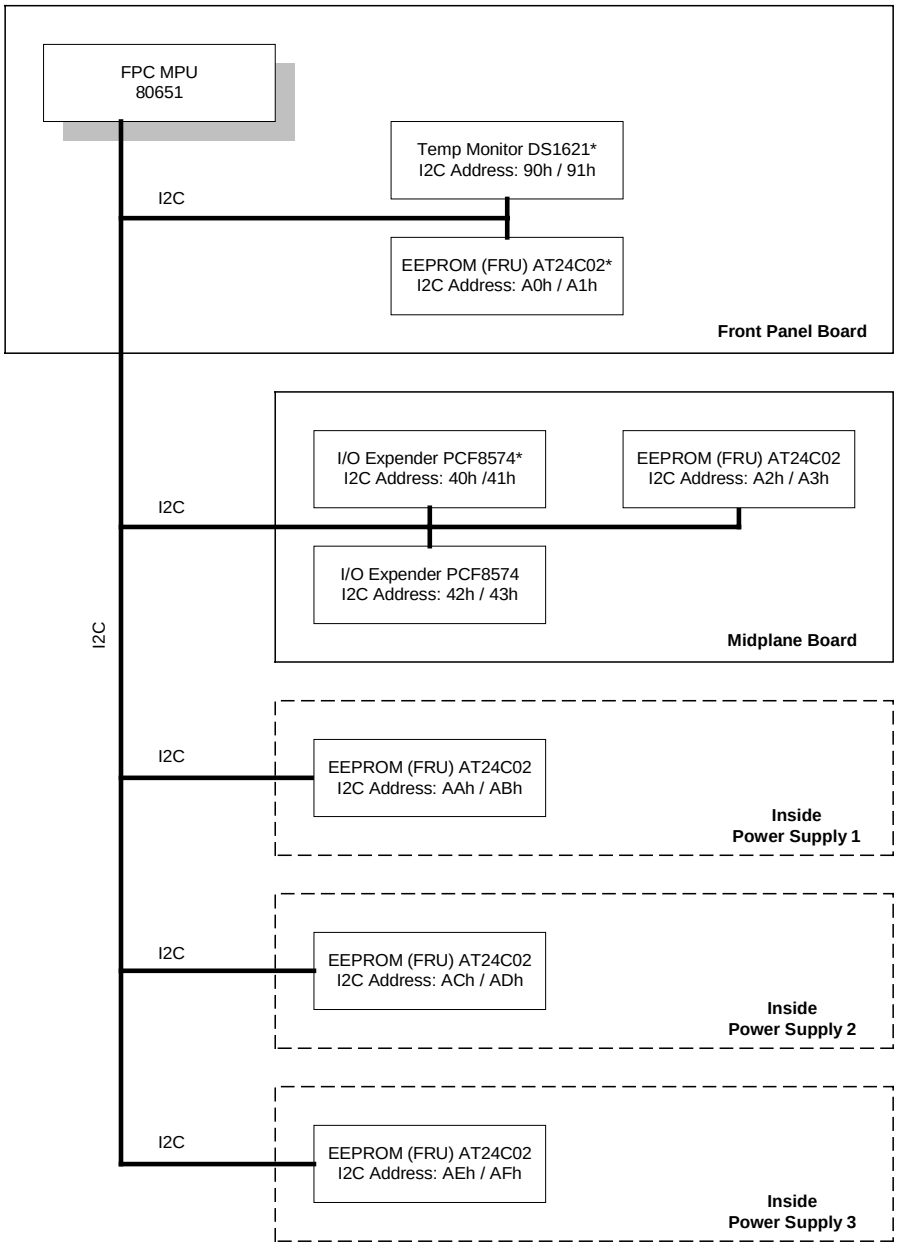

Figure 3-2: Devices Not Supporting Multimaster Mode

3.2.12.2 Global I^2C Bus

The global I^2C bus is connected automatically to the IPMB whenever power is valid. This bus is used to allow communication between smart I^2C devices that operate in multimaster mode. Specifically, this bus connects the FPC and BMC. Also, there may be an SMM based device on the bus and a cluster card connector based device.

On the FPC, this bus consists of the I2C_BACKUP_SCL and the I2C_BACKUP_SDA signals.

3.2.12.3 I^2C Development Support Jumpers

Development support jumpers on the I^2C buses are provided to isolate I^2C devices. These jumpers must first be enabled by removing Resistor Pack RP3A4 and RP3A5 and adding all J3 jumpers. Once enabled, specific I^2C devices/sections can be isolated by removing the jumpers.

In production, the jumper blocks are not stuffed.

3.2.13 Miscellaneous

3.2.13.1 Signal RESET_OUTPUTS_L

The RESET_OUTPUTS_L signal is used to enable the output latch. Immediately after the microcontroller comes out of a hard reset, this signal goes to the deasserted (high) state. In this state the output latch is output disabled, but retainsany states written to it. The microcontroller initializes the latch with proper values before the RESET_OUTPUTS_L signal is asserted (low).

4. Peripheral Bay Backplane Board

This chapter describes the features and functionality of the peripheral bay backplane board, which is also referred to as the backplane. The backplane is designed in compliance with the *SCSI Command Set For Enclosure Services Document Specification*, and the *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification.*

Features

The backplane supports the following features:

- Single channel maximum of two 1″ or 1.6″ LVDS SCSI (16-bit) drives and one 8-bit SCSI device
- Single connector attachment (SCA-2) connectors to simplify insertion and removal of hard disk drives
- Insertion and removal of hard drives with system powered on (hot swap)
- LED indicators for each drive
- Field effect transistor (FET) power control for each hard drive
- FET short protection
- Microcontroller to monitor enclosure services
- I^2C bus for management information
- Flash memory for upgrading firmware
- Temperature sensing
- PLD reprogrammability
- *SAF-TE*
- Tolerant of baseboard management controller (BMC) failure
- Supports SCSI-3 (LVDS SCSI) and SCSI-2
- LVD/SE multimode support
- onboard IDE/FD connections

4.1 Peripheral Bay Backplane Overview

The backplane is an LVDS SCSI design. The one-piece backplane has one SCSI channel with *SAF-TE* implemented. The backplane accomodates either 1.0″ or 1.6″ tall and 3.5″ wide.

The backplane incorporates indicator LEDs. These LEDs indicate drive power (green), drive activity (green), and drive fault (yellow). A light pipe transmits the LED indicators from the backplane to the front bezel.

4.1.1 Architectural Overview

The backplane is an integral part of the AC450NX server system. It is designed to provide a cost effective, easily hot-swappable drive replacement, easy RAID integration over a wide range of RAID controller products, and be vendor independent.

The single feature that simplifies RAID integration is the addition of an onboard SCSI target whose command set allows vendor independent controller management and monitoring for associated drive functions such as drive

insertion and removal, light indicators, and drive power control. Its use simplifies cable management and eliminates errors caused by the possibility of incorrect correlation of several cables.

The backplane performs the tasks associated with hot-swappable SCSI drives, and enclosure (chassis) monitoring and management, as specified in the *SAF-TE*. The tasks supported by the backplane include, but are not limited to, the following:

- Monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages include: activate a drive fault indicator, power down a drive which has failed, and report backplane temperature.
- *SAF-TE* intelligent agent, which acts as a proxy for "dumb" I^2C devices (that have no bus mastering capability), during intrachassis communications.

4.1.2 Placement Diagram

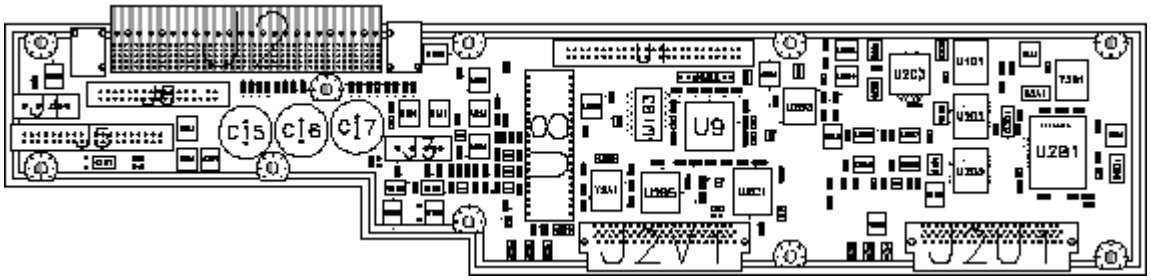

Figure 4-1: Placement Diagram Primary Side

4.1.3 Deviations from *SAF-TE* Specification

The *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification* specification requires the use of a PAIR signal. The intended use of this signal is to allow inter-backplane processor communication. This design is not intended to be connected to other backplanes; therefore, this signal is deemed unnecessary and is not implemented here.

4.2 Functional Description

This section defines the architecture of the backplane, including descriptions of functional blocks and how they operate. Figure 4-2 shows the functional blocks on the SCSI channel of the backplane. An overview of each block follows.

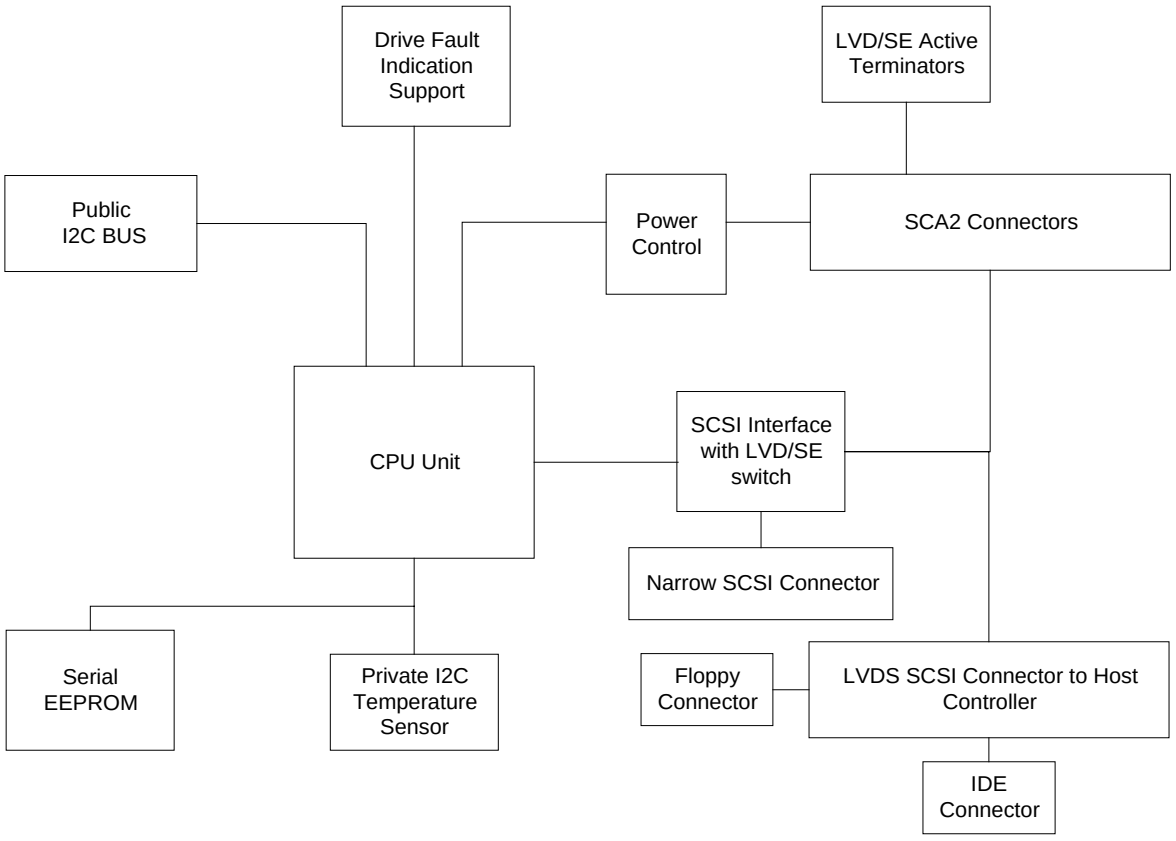

Figure 4-2: Functional Block Diagram

4.2.1 Hot-swap Connectors

The backplane provides two hot-swap SCA-2 right angle connectors, which provide power and SCSI signals using a single connector. Each SCSI drive attaches to the backplane using one of these connectors.

4.2.2 SCSI Interface

There is one LVDS SCSI channel on the backplane. The SCSI interface on the backplane provides the required additional circuitry between the SCSI bus and the microcontroller (containing the intelligence for the backplane), which allows the microcontroller to respond as a SCSI target. This is implemented using a Symbios Logic 53C80S* SCSI interface chip (or equivalent).

4.2.3 LVD/SE Active Termination

The low-voltage differential/single ended (LVD/SE) active terminators provide SCSI-3 compliant termination for the backplane end of the SCSI bus. It is assumed that the other end of the SCSI segment is properly terminated as required by the SCSI-3 specification.

4.2.3.1 LVDS Termination

The following is a list of the features of the LVDS SCSI termination.

- Multimode support with auto selection of single-ended or low voltage differential operation
- 2.7 V to 5.25 V operation
- Differential failsafe bias
- Thermal packaging for low junction temperature and better mean time between failure (MTBF)
- Master/slave inputs
- Supports active negation
- Standby (Disable Mode) 5 µA
- 3 pf channel capacitance

4.2.3.2 Single-ended Termination

The following is a list of the features of the single-ended SCSI termination.

- Fully compliant with SCSI, SCSI-2, and SCSI-3 standards
- Backward compatible to the DS2107* and DS2107A*
- Provides active termination for nine signal lines
- Laser-trimmed 110 ohm termination resistors have 2% tolerance
- Low dropout voltage regulator
- Power-down mode isolates termination resistors from the bus
- Fully supports actively negated SCSI signals
- Onboard thermal shutdown circuitry

4.2.4 Power Control

Power control on the backplane supports the following features.

- Spin-down of a drive when failure is detected and reported (using enclosure services messages) via the SCSI bus. An application or RAID controller detects a drive-related problem that indicates a data risk. In response, it takes the drive out of service and sends a spin down SCSI command to the drive. This decreases the likelihood that the drive is damaged during removal from the hot-swap drive bay. When a new drive is inserted, the power control waits a small amount of time for the drive to be fully seated, and then appiles power to the drive to prepare for operation.
- If system power is on, the backplane immediately powers off a drive slot when it detects a drive has been removed. This prevents possible damage to the drive when it is partially removed and reinserted while full power is available, and it also prevents disruption of the entire SCSI array from possible sags in supply voltage and resultant current spikes.

4.2.5 FET Short Protection

The FET short protection circuit protects both 12 V and 5 V power located on the backplane. This circuit prevents damage to the backplane in the event of a power fault on the drives plugged into the SCA connectors.

4.2.6 LED Arrangement

The three LEDs per drive are arranged as follows (viewed from the drive bay):

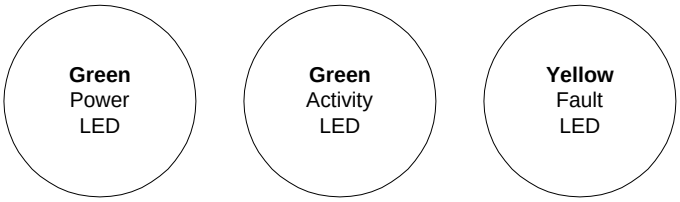

Figure 4-3: LED Arrangement

4.2.6.1 Power LEDs

Power LEDs are green and they indicate the drive is receiving power. Power LED control is driven by the FET switched +5 V applied to the drive.

4.2.6.2 Drive Activity LEDs

The activity LEDs are green and are driven by the drive, pin 77, and interface directly to the LED.

4.2.6.3 Fault LEDs

The hot-swap controller is responsible for turning the drive fault LEDs on or off according to the states specified via commands received through *SAF-TE* and the IPMB. The drive fault LEDs are yellow and serve to indicate failure status for each drive. The LEDs are physically located on the LVDS SCSI backplane, and are driven from the backplane.

During initialization, the microcontroller flashes the LEDs for 2 seconds to signal successful POST completion.

4.2.7 Temperature Sensor

A Dallas DS1621* temperature sensor device is connected to each microcontroller on a "private" I^2C bus. This device is used to monitor the drive bay temperature. The temperature may be read via *SAF-TE* and IPMB commands. In addition, settable temperature thresholds are provided via IPMB commands. The HSC can be configured to issue an event message on the IPMB when the temperature threshold is crossed.

Microcontroller programming implements the private I^2C connection by explicitly setting and clearing appropriate clock and data signals to emulate an I^2C-like interface to the sensor.

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5. Peripheral Bay Board (Chassis Side)

This chapter describes the design of the peripheral bay board (chassis side). This board, used in the AC450NX server system, is attached to the AC450NX server system chassis and provides power and signal distribution to the peripheral bay backplane and other system peripheral devices.

Features

The AC450NX server system peripheral bay board has the following features:

- Provides an interface which allows plugging of the peripheral bay into the system.
- Distributes power and signal connections from the midplane and I/O board to the floppy, IDE CD-ROM, and the peripheral bay backplane.
- Provides a common interface for OEM custom peripheral bay solutions.

5.1 Introduction

The peripheral bay board (chassis side) provides power and signal interconnection from the midplane and I/O boards to the peripheral devices and the peripheral bay backplane. This board allows the single point connection of all power and signals required by the peripheral bay backplane. The peripheral bay board (chassis side) contains no active components. Also, it does not provide or contain any field replaceable unit (FRU) information.

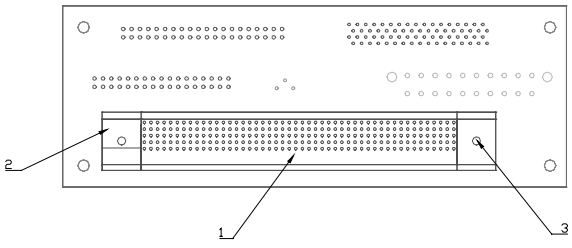
5.2 Mechanical Description

The blind mate is the junction of the peripheral bay board (chassis side) with the peripheral bay backplane. The peripheral bay backplane meets the peripheral bay board (chassis side) at a 90-degree angle.

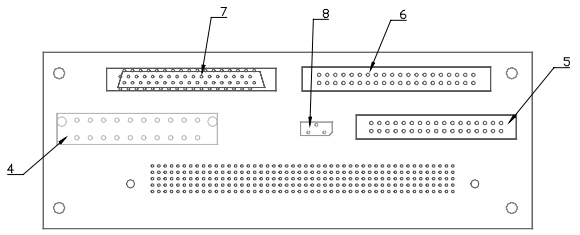
The blind mate consists of one 240-pin connector in between two long guide pins.

5.2.1 Board Layout

Figure 5-1 illustrates the layout of the peripheral bay board (chassis side) with the connectors.



1.) 89009-149 (BERG*) Blind Mate Connector Header
2.) 73475-101 (BERG) Guide Pin Housing
3.) 70295-001 (BERG) Guide Pin and Screw



4.) 39-29-9206 (Molex*) 20-position power Connector
5.) 39-26-7345 (Molex) 34-position Header (floppy)
6.) 39-26-7405 (Molex) 40-position Header IDE
7.) 15-87-0305 (Molex) Wide SCSI Connector
8.) 2204407031 (Molex) 3-position Header

Figure 5-1: Peripheral Bay Board (Chassis Side) Layout

Figure 5-2 shows the printed circuit board dimensions, mounting holes, and connector placements.

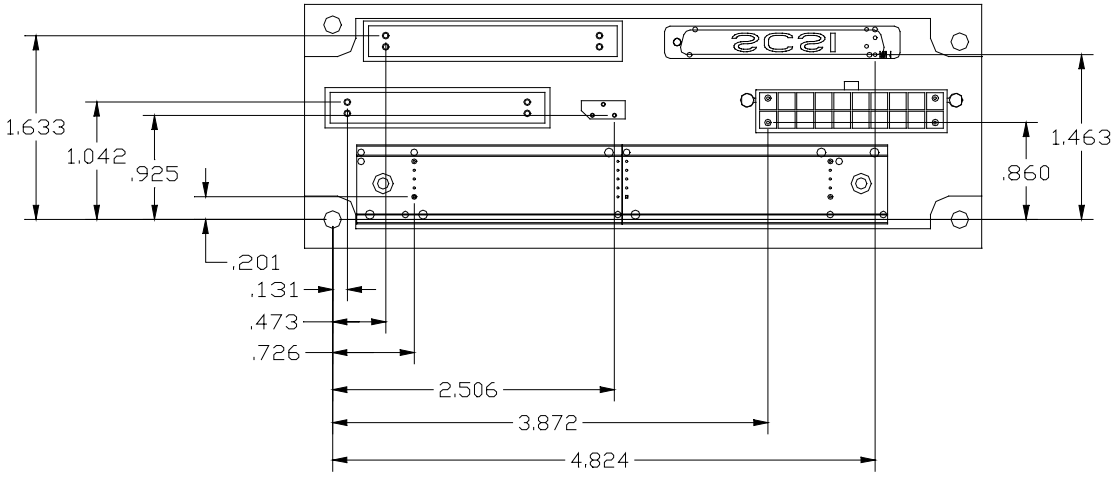


Figure 5-2: Peripheral Bay Board (Chassis Side) Connector Layout

6. System Power Supply

This chapter defines the features and functionality of the AC450NX server system power supply.

Features

- 750 W output capability at high line AC input
- 650 W output capability at low line AC input
- AC input auto-ranged
- Power, predictive fail, and power supply fail indicator LEDs
- Power factor correction (PFC) capability
- Blind mate and hot swap capability
- Integral cooling fan with multispeed capability
- Remote sense of 3.3 V, 5 V, and 12 Vdc outputs
- AC-OK circuitry for brown out protection
- Protection against over-temperature (OTP), over-voltage (OVP), over-current (OCP), and fan failure
- Load sharing capability
- Onboard FRU information
- I^2C interface for server management functions
- Integral handle for insertion/extraction

6.1 Introduction

The AC450NX server system uses universal input switching power supplies that provide 750 watts at high line AC input but are derated to 650 watts at low line AC input. The high line AC input is defined as the AC input between 200 Vac and 240 Vac. The low line AC input is defined as the AC input between 100 Vac and 120 Vac.

The power supply is power factor corrected at the AC input with forced current sharing and remote sense regulation at the DC outputs. The power supply may be used either singularly or with up to three identical power supplies, with DC outputs paralleled to form a redundant power system (2 + 1) that has system operating replacement capability (hot swap). All power supply connectors, including both the AC and DC connectors, accommodate "blind mating." The supply has four externally enabled outputs, one +5 V standby output, and one +15 V standby output. The +5 Vdc standby output and the +15 Vdc standby output are present whenever AC power is applied. The four externally enabled outputs, the +5 Vdc standby output, and the +15 Vdc standby output have the following ratings at high line AC input.

- +3.3 Vdc at 36 A
- +5 Vdc at 36 A
- +12 Vdc at 36 A with 42 A peak for no more than 12 seconds
- -12 Vdc at 1 A
- +5 V standby at 1 A
- +15 V Standby at 0.2 A

The power supply DC outputs have the following current rating at low line AC input.

- +3.3 Vdc at 31 A

- +5 Vdc at 31 A
- +12 Vdc at 31 A with 37 A peak for no more than 12 seconds
- -12 Vdc at 1 A
- +5 V standby at 1 A
- +15 V standby at 0.2 A

6.2 Mechanical Interface

6.2.1 Mechanical Outline

The mechanical outline and dimensions are shown in Figure 6-1. The unit of measure is inches. The following mechanical sketches should be used for preliminary reference only.

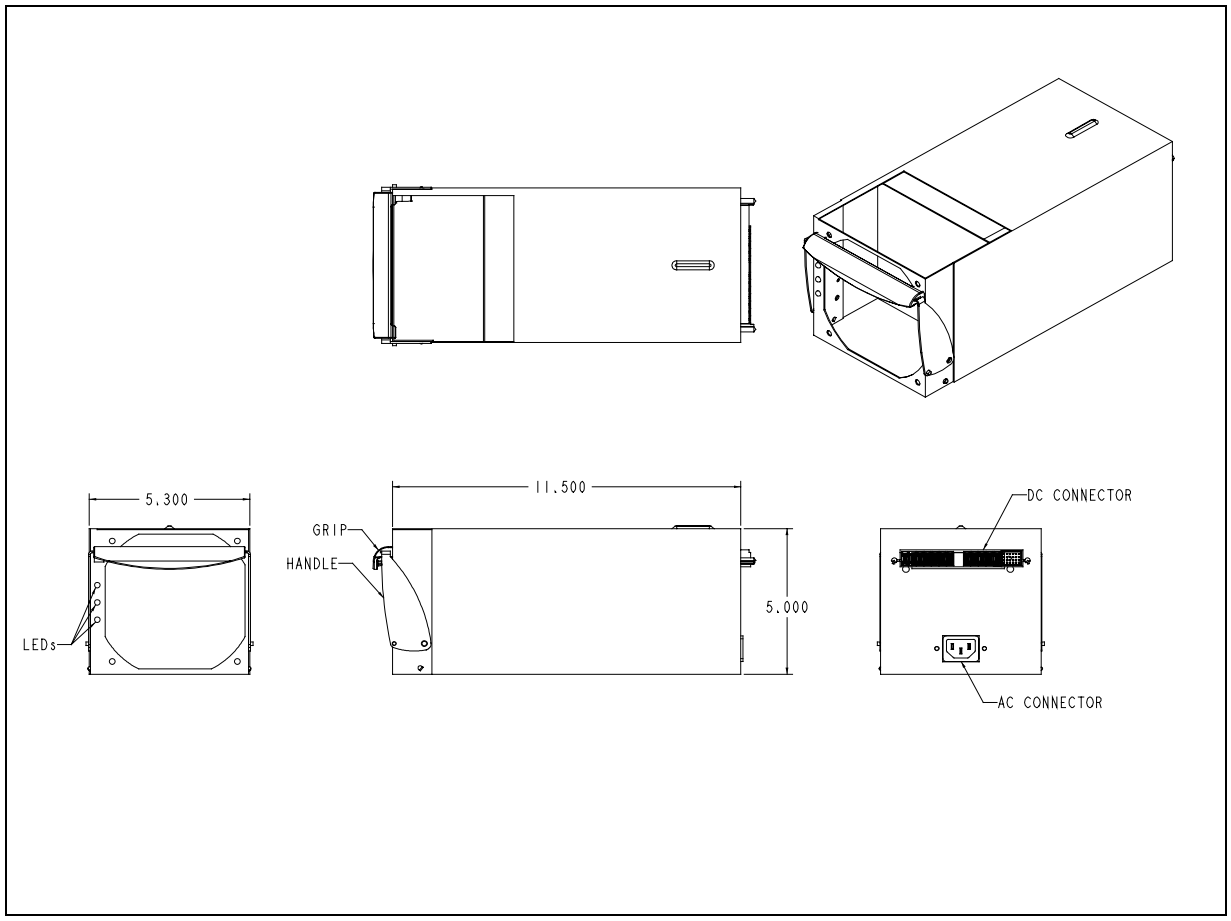


Figure 6-1: Outline Drawing for Power Supply Enclosure

The power supply dimensions are 5.0″ H by 5.3″ W by 11.5″ D.

6.2.2 Fan Requirements

6.2.2.1 Air Flow

The power supply contains a 120 mm fan for self-cooling. The temperature sensor which indirectly controls the fan speed is located close to the air inlet side within the power supply chassis.

6.2.2.2 Special Requirements for Fan

The power supply will shut down if the fan fails in any way including, but not limited to, fan open, fan short, or fan lock rotor.

6.2.2.3 Over-temperature Protection (OTP)

The power supply is protected against over-temperature conditions caused by loss of cooling air, fan slow down, cooling fan failure, or excessive ambient temperature. In an over-temperature protection (OTP) condition, the power supply will be in power-off mode with the exception of +5 V standby output and the +15 V standby output, but the power supply will not latch in the power-off mode. When the power supply temperature drops to the operating level, the power supply will restore power automatically by PSON reset. The OTP circuit has built-in hysteresis such that the power supply will not oscillate on and off due to a temperature recovering condition.

The power supply will alert the system of the OTP condition via the power supply fail signal on the DC connector, and the FAIL LED will illuminate to indicate such a condition.

6.2.3 Interface Requirements

6.2.3.1 AC Inlet

The AC power inlet receptacle, or pins and wiring, placed electrically before the protective fuse(s) has a peak current rating higher than the peak inrush current or maximum fault current drawn by the supply. The safety ground pin is the first pin to connect and the last to disconnect. The ground pin for each supply can pass twice the branch current under ground impedance test. With the intent of these servers being connected to 15 A branch services, the ground pin is required to pass a 30 A ground impedance test per safety standards. This power supply is hot swappable. It accommodates being inserted or removed from operating assemblies which have AC input and DC output voltages and signals present at the mating connectors, without disrupting operation of the assembly due to transients induced on AC or DC voltages or radiated EMI.

6.2.3.2 DC Output Connector(s)

DC power and control signals are interfaced to the system distribution and control subsystem via connectors that dock with mating connectors when the power supply is inserted into the system midplane. In addition to the +3.3 V, +5 V and +12 V DC outputs, the following signals and output pins are included as a minimum:

- +3.3 Vdc load share control
- +5 Vdc load share control
- +12 Vdc load share control
- +3.3 Vdc remote sense
- +5 Vdc remote sense

- +12 Vdc remote sense
- Remote sense return
- Power supply present
- Power supply on
- Power supply kill
- Power good
- AC OK
- Predictive failure
- Power supply failure
- FRU information SERIAL CLOCK (SCL)
- FRU information SERIAL DATA (SDA)
- EEPROM address line: A0
- EEPROM address line: A1
- +5 V standby
- +15 V standby
- – 12 Vdc output

6.2.3.3 LED Labeling

The power LED (green), the power supply failure LED (yellow), and the predictive failure LED (yellow) are marked or labeled near the LEDs with the following markings:

- **PWR** - power LED
- **FAIL -** power supply failure LED
- **PRFL** - predictive failure LED

The LEDs should be viewable on the outside when the power supply is installed in the system chassis. LEDs are located to meet all electrostatic discharge (ESD) requirements. The appearance of the LEDs external to the chassis is in the following order: power LED, predictive failure LED, and power supply failure LED. Refer to Figure 6-1 for the location of the LEDs in the chassis.

6.3 Electrical Interface

6.3.1 AC Input Voltage Specification

6.3.1.1 AC Input Voltage Ranges

The nominal input voltage ranges specified in AC volts rms are 100, 120, 208, 220, and 240 Vac. The power supply incorporates a universal power input with active power factor correction, which will reduce line harmonics in accordance with EN61000-3-2 and JEIDA MITI standards. The ratings will be marked on the supply labels.

Table 6-1: Input Voltage Requirements

Parameter	Minimum	Nominal	Maximum	Units
Vin (115)	90	100-120	132	Vrms
Vin (230)	180	200-240	264	Vrms
Vin frequency	47	50/60	63	Hz
Input current 115 Vac range		13		Amps
Input current 220 Vac range		7		Amps

6.3.1.2 AC Line Dropout

AC line dropout condition is a transient condition defined when the line voltage input to the power supply drops to 0 volts. This condition is tested at minimum nominal input voltage and at zero crossing of the sinusoid wave. AC line dropout will not damage the power supply under any load conditions. While operating at full load, an AC line dropout condition with a period equivalent to a complete cycle of AC input power frequency (i.e., 20 ms at 50 Hz) or less will not cause any out of regulation conditions such as overshoot or undershoot, nor will it cause any nuisance trips of any of the power supply protection circuits. The power good signal will not go to a low state under these conditions. AC dropout transients in excess of 20 milliseconds may cause a shutdown of the power supply or out of regulation conditions, but will not cause damage to the power supply.

6.3.1.3 AC Line Fuse

Both the LINE and NEUTRAL AC inputs are fused. AC line fusing must be acceptable for all safety agency requirements. AC inrush current will not cause the AC line fuses to blow under any conditions. Protection circuits in the power supply will not cause the AC fuses to blow unless a component in the power supply has failed. This includes DC output load short conditions. The DC load short circuit protection circuits will shut down or limit power supply without causing the AC line fuse to blow.

6.3.2 DC Output Specification

The power supply DC output specification is met by a single supply, by two supplies, or by three supplies operating with their outputs directly paralleled. When operated in parallel, the supplies share the total load currents equally within the limits specified, while meeting all performance requirements of individual supplies. Failure of a supply in a paralleled group, or removal of an operational or failed supply from a paralleled group will not cause DC output transients in excess of the limits specified. Adding an operational or failed supply to a paralleled group will not cause DC output transients in excess of the limits specified.

Steady state DC output voltages at the remote sense points remain within the limits of Table 6-2 for all combinations of operating line, load, load transient, and environment specified here. The combination of setpoint limits, line/load regulation and ripple/noise cannot exceed the DC output voltage limits of Table 6-2.

Table 6-2: DC Output Voltage Limits

Parameter	Min	Max	Units	Tolerance
+3.3 V	+3.25	+3.35	V	± 1.5%
+5 V	+4.90	+5.10	V	± 2%
+12 V	+11.76	+12.24	V	± 2%
-12 V	-11.16	-12.84	V	+9% and 5%
+5 V Standby	+4.85	+5.20	V	+ 4% and -3%
+15 V Standby	+13.5	+16.5	V	± 10%

6.3.2.1 DC Outputs Rating

At high line AC input, the steady state and peak DC output load currents are in the ranges shown in Table 6-3.

Table 6-3: Load Range for High Line AC Input

	Single Power Supply Maximum Load Condition at High Line		
Voltage	**Minimum Continuous**	**Maximum Continuous**	**Peak**
+3.3 V	1.1 A	36 A	
+5 V	0.7 A	36 A	
+12 V	0.7 A	36 A	42 A
-12 V	0 A	1.0 A	
+5 V Standby	0.05 A	2.0 A	
+15 Vbias	0 A	0.2 A	

At low line AC input, the steady state and peak DC output load currents are in the ranges shown in Table 6-4.

Table 6-4: Load Range for Low Line AC Input

	Single Power Supply Maximum Load Condition at Low Line		
Voltage	**Minimum Continuous**	**Maximum Continuous**	**Peak**
+3.3 V	1.1 A	31 A	
+5 V	0.7 A	31 A	
+12 V	0.7 A	31 A	37 A
-12 V	0 A	1.0 A	
+5 V Standby	0.05 A	1.0 A	
+15 Vbias	0 A	0.2 A	

6.3.2.2 Remote Sense

The power supply provides remote sense on the +3.3 Vdc, +5 Vdc, and +12 Vdc outputs and their common DC return to provide regulation at those remote points. The connector shown in *Section 6.2.3.2 DC Output Connector(s)* provides the +3.3 V, +5 V, and +12 V remote sense and a common remote sense return to the power supply. The local sense resistor between the power supply outputs and the remote sense input will not be less than 200 ohms. In the event of an open remote sense line, the power supply will maintain local sense regulation. In the event of an open DC power line or shorted remote sense line, the power supply will not be damaged. The remote sense is capable of regulating out the drops shown in Table 6-5 and still meeting regulation requirements.

Table 6-5: Remote Sense Drops

Output	Max Drops	Units
+3.3 Vdc	200	mV
+5 Vdc	250	mV
+12 Vdc	250	mV
Remote sense return	200	mV

6.3.2.3 Over-voltage Protection

The power supply over-voltage protection is sensed locally. The power supply shuts down in a latch off mode after an over-voltage condition. The latch is cleared by toggling the power supply on signal, or by an AC power interruption of greater than one second. This over-voltage limit applies over all specified AC input voltages and output load conditions. Table 6-6 contains the over-voltage limits. The values are measured at the output of the power supply DC connector.

Table 6-6: Over-voltage Protection

Output Voltage	Protection Point [V]
+3.3 V	3.8 – 4.3
+5 V	6.0 – 6.5
+12 V	13 – 14

6.3.2.4 Over-current Protection

The power supply has current limits to prevent the +3.3 Vdc, +5 Vdc, and +12 Vdc outputs from exceeding the values shown in Table 6-7. The current limiting is of the voltage fold-back type. The over-current limit level is maintained for a period of 1.6 seconds minimum and 2.0 seconds maximum. After this time, the power supply latches off. The latch is cleared by toggling the power supply on signal or by an AC power interruption of greater than one second. The power supply is not damaged from repeated power cycling in this condition.

Table 6-7: Over-current Protection

Voltage	Over Current Limit
+3.3 V	39.6 A minimum; 46.8 A maximum
+5 V	39.6 A minimum; 46.8 A maximum
+12 V	46 A minimum; 51 A maximum

6.3.2.5 Short Circuit Protection

The power supply will not be damaged by application of a short circuit to any DC output. Short circuits will not turn into the over-current protection process described in Section 6.3.2.4 Over-current Protection (OCP). A hard short circuit should turn off the power supply immediately. A hard short circuit is defined as the load level dropping to less than 10 milliohms.

6.3.2.6 Grounding Requirements

The power supply DC output ground is earth grounded and connected to the power supply case. Resistance from the DC return pins to the chassis will not exceed 1.0 milliohms. This path may be used to carry DC current.

6.3.2.7 Current Sharing Requirements

Equal power sharing of paralleled power supplies is required to prevent a life shortening stress concentration in individual power supplies. Power sharing is accomplished by actively matching the output currents on the high power outputs. The failure of a power supply does not affect the current sharing or output voltages of other power supplies still in operation. The current sharing load deviation is defined as follows:

Load_Deviation% = [(Actual_Load – Mean_ Load)/(Mean_Load)] * 100

Mean_Load = (Total Output)/ (# of PSU)

The +3.3 V, +5 V, and +12 V output currents of paralleled supplies maintain a maximum load deviation of ± 10% at rated current. At one-half of rated current, the maximum load deviation is ± 20%. At less than half the rated current, the maximum load deviation can be greater than ± 20%.

A maximum load deviation of ± 30% is achieved on the +5 V standby output. The load deviation on the +5 V standby may come from the droop sharing when paralleling more than one supply in the system.

The other DC outputs may share to any degree, as long as regulation, transient, and hot-swap limits are met.

Signals to control current share may consist of one wire connecting all paralleled power supplies for each output. One separate ground wire may be supplied for these signals if required.

6.3.3 Control Signals

6.3.3.1 Power Supply On (Input)

The power supply on circuit is a Safety Extra Low Voltage (SELV) circuit. Upon receiving a logic HIGH at this signal, along with a LOW signal on the PS_Kill pin, the power supply is turned on and power outputs and other signals are provided at the corresponding DC connector output pins.

A logic LOW on this pin at the DC connector should turn the power supply off regardless of the state of the PS_Kill signal. The normal turn off delay and shut down sequence will be followed when the power supply on signal is used to turn the power supply off.

The truth table for the logic of power supply on and power supply kill is shown below.

Table 6-8: Truth Table-Logic of Power Supply On/Power Supply Kill

Power Supply Kill	Power Supply On	Power Supply Conditions
Low	High	DC outputs are on
X	Low	DC outputs are off
High	X	DC outputs are off

The characteristics of the power supply on signal are shown in Table 6-9. The power supply on is an input signal to the power supply from the system.

Table 6-9: Power Supply On Specification

Power Supply On Signal	Voltage Level†	Current
HIGH, Power Supply Enabled	4 V min	0.5 mA max source current
LOW, Power Supply Disabled	1 V max or open circuit	

† Measured relative to the power supply DC common output ground pins.

6.3.3.2 AC OK Signal (Output)

Each power supply provides an AC_OK signal. A pin must be allocated for this signal on the DC connector. This signal is to be utilized by the system to synchronize the power on timing of multiple power supplies within the

system when the system is operated at high line input voltages. The AC_OK signal allows the system to turn on at 180 Vac with 10% THD. The AC_OK signal must have hysteresis such that the power system does not oscillate on/off due to normal AC source impedance (0.5 Ω). The power supply demonstrates thermal and current margin at 50°C with maximum DC load at minimum AC voltage when AC_OK is asserted. AC_OK may not be deasserted during any of the operating level tests in this specification, including the 20 ms dropout test.

The AC_OK signal is an active low signal with open collector at the output. The pull-up resistor is assembled on the system midplane. The electrical characteristic of the AC_OK signal is shown in Table 6-10.

Table 6-10: Electrical Characteristic of AC_OK Signal

AC OK Signal	Voltage Level†	Current
LOW:AC is up to high line minimum level.	0.4 V max	4 mA min sinking current
HIGH/Open Collector: AC is NOT up to the high line minimum level.	Open collector	

† Measured relative to the power supply DC common output ground pins.

6.3.3.3 Power Good (Output)

Each power supply provides a power good signal. A pin must be allocated for this signal. This signal indicates that all outputs have reached acceptable operating voltage. The power good signal levels and souring/sinking requirements are shown in Table 6-11. The power good signal is an output signal from the power supply to the system.

Table 6-11: Power Good Signal

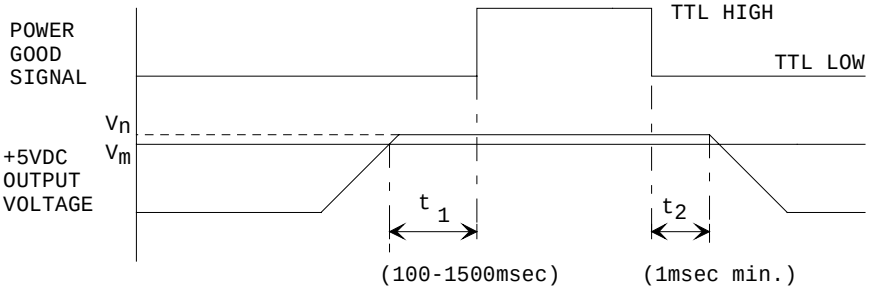
Power Good Signal	Voltage Level†	Current
LOW: Deasserted (Power Not Good)	0.4 V max	4 mA min sink current
HIGH: Asserted (Power Good)	4 V min	0.5 mA max source current

† Measured relative to the power supply DC common output ground pins.

The power good signal is held low until all outputs have reached at least 90% of their respective operating voltages. The turn on delay for the power good signal is between 100 and 1500 milliseconds.

The power good signal is low for a minimum of one millisecond before any of the output voltages fall below the regulation limits. Tests are conducted with a maximum load and minimum line voltage.

In Figure 6-2, +5 V output is used as an example.



Vn Nominal Output Voltage +5 VDC
Vm Minimum Output Voltage +4.75 VDC
t1 Delay Turn-on (100-1500msec)
t2 Delay Turn-off(1msec min)

Figure 6-2: Power Good Signal Characteristics

6.3.3.4 Power Supply Present Indicator (Output)

This signal is used to sense the number of power supplies in the system (operational or not). A pin on the output connector is allocated for this signal. Internal to the power supply, this signal pin is tied directly to ground potential. On the system side, the power supply present signal is pulled up through a pull-up resistor to +5 V standby on the midplane. The power supply present is an output signal from the power supply to the system.

6.3.3.5 Predictive Failure (PRFL) Signal (Output)

This signal is available on the power supply connector. A HIGH state in this signal indicates that the power supply is likely to fail in the near future due to a poorly performing fan. The predictive fan failure signal going HIGH does not cause the power supply to shut down, but it will cause the PRFL LED to latch onto flashing mode. The predictive failure is an output signal from the power supply to the system.

Table 6-12: Predictive Failure Signals

Predictive Failure Signal	Voltage Level†	Current
LOW: (power supply OK)	0.4 V max	4 mA min sink current
HIGH: (poorly performing fan)	4 V min	0.5 mA max source current

† Measured relative to the power supply DC common output ground pins.

6.3.3.6 Power Supply Failure Signal (Output)

This signal is available on the power supply connector. Upon receiving this signal, the system informs the operator that the appropriate power supply has failed, and therefore a replacement of that power supply is necessary.

The power supply failure is defined as OVP at any output, under-voltage (UV) at any output, and/or fan failure inside the power supply. The power supply failure is an output signal from the power supply to the system.

Table 6-13: Power Supply Failure

Power Supply Failure Signal	Voltage Level†
LOW: (power supply failure)	0.4 V max
HIGH: (power supply OK)	4 V min

† Measured relative to the power supply DC common output ground pins.

6.3.3.7 Power Supply Kill (Input)

The power supply kill signal is available on the power supply connector. The mating pin of this signal on the midplane should be tied to ground potential on the midplane. Internal to the power supply, the power supply kill pin is connected to the +5 V standby through a pull-up resistor.

Upon receiving a low state signal at the power supply kill pin, the power supply will be allowed to turn on. A logic low on this pin by itself does not turn on the power outputs. With the power supply kill signal in a low state, a logic high signal on the power-supply-on signal is able to turn on the power supply.

When the power supply kill signal pin is pulled up high (power supply is extracting from the midplane), the power supply should be shut down immediately without any delay, regardless of the condition of the PS_On signal.

Table 6-14 is the truth table for the logic of power supply kill and power supply on is shown below.

Table 6-14: Logic Table for Power Supply Kill and Power Supply On

Power Supply Kill	Power Supply On	Power Supply Conditions
Low	High	DC outputs are On
X	Low	DC outputs are Off
High	X	DC outputs are Off

The characteristics of the power supply kill signal are shown in Table 6-15. The power supply kill is an input signal to the power supply from the system.

Table 6-15: Power Supply Kill Specification

Power Supply Kill Signal	Voltage Level†
HIGH: Power Supply is Disabled	4.5 V minimum
LOW: Power Supply is Enabled	0.25 V maximum

† Measured relative to the power supply DC common output ground pins.

6.3.3.8 Power Supply Field Replacement Unit Signals

Four pins are allocated for the field replaceable unit (FRU) information on the power supply connector. One pin is for the Serial Clock (SCL). The second pin is used for Serial Data (SDA). Both pins are bidirectional and are used to form a serial bus. The third pin is address line A0 of the EEPROM, and the last pin is address line A1 of the EEPROM.

Inside the power supply, the highest address bit of the EEPROM A2 should be tied to +5 V standby on the cathode side of the OR'ing Diode.

The Vcc pin of the EEPROM should also be tied to the +5 V standby on the cathode side of the OR'ing Diode so that even during failure, the FRU information within the power supply can be accessed.

The write control (or write protect) pin should be tied to ground inside the power supply so that information can be written to the EEPROM.

6.3.3.9 LED Indicators

There is a green power LED (PWR) to indicate that AC is applied to the power supply and standby voltages are available when blinking. This same LED goes solid to indicate that all the power outputs are ready. There is a yellow power supply fail LED (FAIL) to indicate that the power supply has failed and a replacement of the unit is necessary. There is a yellow predictive failure LED (PR_FL) to indicate that the power supply is about to fail in the near future due to a poorly performing fan. This LED blinks to indicate the predictive failure condition and is latched into the blinking state once the condition has occurred. This latch can be cleared by toggling the power supply on signal or by an AC power interruption of greater than one second. Refer to Table 6-17 for conditions of the LEDs. The LEDs are marked as shown in Table 6-17.

Table 6-16: LED Indicators

	Power Supply LEDs		
Power Supply Condition	PWR (green)	PRFL (yellow)	FAIL (yellow)
No AC power	OFF	OFF	OFF
AC in/standby outputs on	Blinking	OFF	OFF
Power supply DC outputs on and OK	ON	OFF	OFF

Power Supply Condition	Power Supply LEDs		
	PWR (green)	PRFL (yellow)	FAIL (yellow)
Power supply failure	OFF	OFF	ON
Current limit	ON	OFF	Blinking/not latched
Predictive failure	ON	Blinking/latched	OFF
Power supply failure*	OFF	OFF	OFF

* Failures in the input side of the power supply shut down the 5 V Stbty circuit that powers the LED indicators.

The LEDs are visible on the power supply surface, which is opposite the docking end. The LED location meets ESD requirements. LEDs are securely mounted in such a way that incidental pressure on the LED will not cause it to become displaced. The appearance of the three LEDs should be in the following order: PWR, PRFL, and FAIL, top to bottom.

Table 6-17 shows the LED indicator and the control signals. It is presented here for reference only.

Table 6-17: Power Supply LED Indicators and Control Signal Logic

Conditions	Power Supply LEDs			Power Supply Output Signal States			Input to PS
	PWR (green)	FAIL (yellow)	PRFL (yellow)	P_Good H=power good	Pred. Failure H=predictive failure	PS Failure H=PS OK	PS On H=PS enable
No AC power	OFF	OFF	OFF	L	L	L	L
AC in/stdby on	Blinking	OFF	OFF	L	L	H	L
DC outputs OK	ON	OFF	OFF	H	L	H	H
Power supply failure	OFF	ON	OFF	L	L	L	H
Current limit	ON	Blinking Not Latched	OFF	L	L	H	H
Predictive failure	ON	OFF	Blinking /latched	H	H	H	H

6.3.4 Fan Speed Control

The fan circuitry will implement variable speed fan control and fan failure detection.

6.4 Regulatory Agency Certifications

The power supply will have UL recognition, CSA certification to level 3, Bauart and any NORDIC CENELEC certifier (such as SEMKO, NEMKO, or SETI) markings demonstrating compliance. The power supply must also meet FCC Class A, VDE 0871 Level A, and CISPR Class A requirements.

Note, refer to the *Conventions and Terminology* sections of this documents for definitions of the above certifications names.

7. Cable and Connector Specifications

This chapter describes the connectors that connect various components of the AC450NX server system. The discussion in this chapter includes an overview diagram of the AC450NX server system interconnections, as well as tables describing the signals and pinouts for the various connectors.

Figure 7-1 shows all of the system cable-to-board and board-to-board connections.

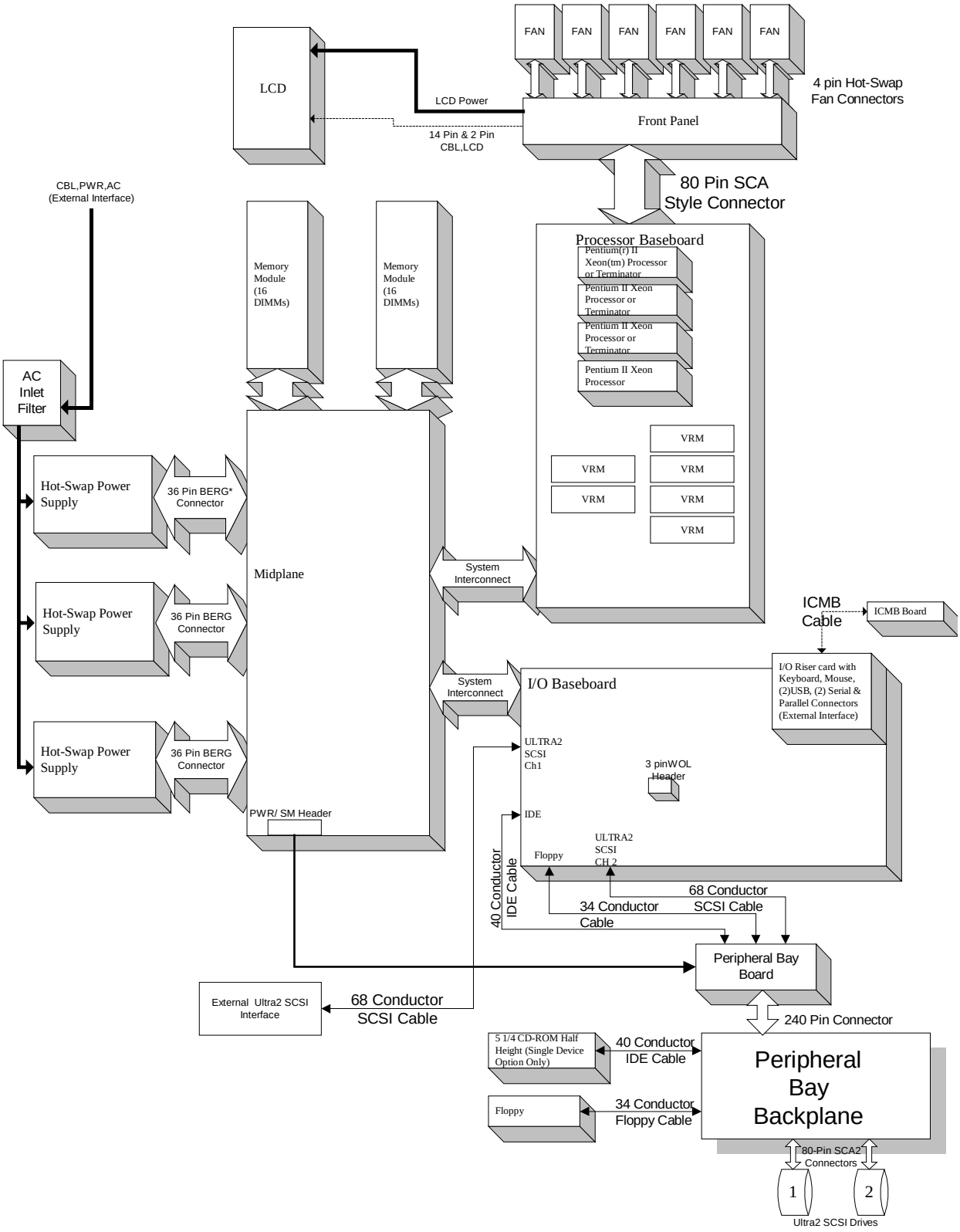


Figure 7-1: System Interconnect Drawing

7.1 CPU Board/Front Panel Interface Descriptions

Table 7-1 shows the interconnections of all of the boards used in the AC450NX server system.

Table 7-1: CPU to Front Panel Connector Pinout

Pin # on 80 Pin	Front Panel Signal		Pin # on 80 Pin	Front Panel Signal
1	GND		41	GND
2	12 volts		42	(-12 volts)
3	12 volts		43	12 volts
4	GND		44	GND
5	GND		45	GND
6	12 volts		46	12 volts
7	12 volts		47	12 volts
8	SPEAKER_DATA		48	GND
9	ISP_SCLK		49	GND
10	FAN_FAILED_L		50	5 volts
11	GND		51	ISP_SDI
12	ISP_FPC_EN_L		52	5 volts
13	FP_TO_PIIX4_PWRBRN		53	ISP_MODE
14	ISP_FPC_SDO		54	5 volts
15	NC		55	NC
16	COM2_TO_FP_EN		56	5 volts
17	COM2_TO_SIO_EN		57	PROC_RESET_L
18	GND		58	NC
19	SECURE_MODE_BMC		59	XIMB_SOUT_EN
20	HARD_RESET		60	GND
21	FP_NMI_SWT_L		61	NC
22	SIN_TTL_COM2		62	NC
23	SIN_TTL_XIMB		63	NC
24	GND		64	GND
25	SOUT_TTL_XIMB		65	PWR_CNRTL_SFC_L
26	PWR_CNRTL_RTC_L		66	SOUT_TTL_COM2
27	GND		67	GND
28	PS_PWR_ON		68	PWR_GOOD
29	DSR_TTL_FP		69	DCD_TTL_FP
30	I2C_CEL_CONNECT_FPC		70	GND
31	CTS_TTL_FP		71	NC
32	I2C_CEL_CONNECT_BMC		72	NC
33	I2C_FPC_SCL		73	RI_TTL_FP
34	I2C_FPC_SDA		74	NC
35	GND		75	RTS_TTL_FP
36	GND		76	DTR_TTL_FP
37	I2C_BACKUP_SDA		77	I2C_BACKUP_SCL
38	VCC_STDBY		78	VCC_STDBY
39	VCC_STDBY		79	VCC_STDBY
40	NC		80	GND

7.2 Fan Connector

Table 7-2 describes the pinouts for the six fan connectors (J2A3, J2C1, J6A1, J6C1, J9A1, and J9C1).

Table 7-2: Fan Connector Pinout

Pin	Signal
1	GROUND
2	VCC FAN
3	GROUND
4	FAN_TACH

7.3 Peripheral Bay Backplane Connector Assignments

7.3.1 Connectors

This section defines all the major connectors on the backplane. All the connectors on the backplane are keyed.

7.3.1.1 Connector Specifications

Table 7-3 shows the quantity, manufacturer, and Intel part number for connectors on the backplane. Refer to manufacturers' documentation for more information on connector mechanical specifications.

Table 7-3: Connector Specifications

Item	Quantity	Manufacturers and Part Number	Description
1	2	AMP* (787535-1)	80 pin right angle SCA-2 connector.
2	1	BERG* (73957-1002)	240 pin recp right angle 5X48.
3	1	FOXCONN* (HL03177-P4)	34 pin (2x17) BMC connector KY5.
4	2	Molex* (15-24-4342)	4 pin power connector.
5	1	Molex (87256-4043)	40 pin IDE cable.
6	1	FOXCONN (HL07256-D6)	50 pin SE SCSI connector.

7.3.1.2 SCSI SCA-2 Drive Connector

An SCA-2 connector is used on the primary side of the board. The pinout is the same as SCA-1. The connector pin assignment is for the current draft *Small Form Factor-8046 Rev. 1.1* document.

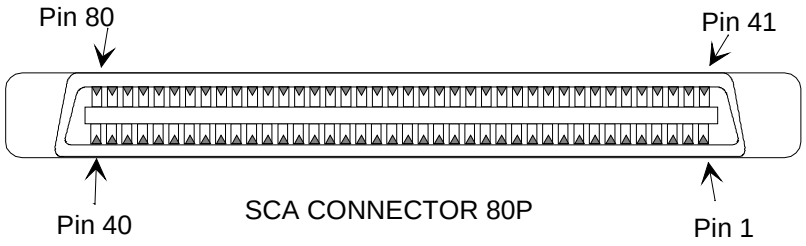


Figure 7-2: SCA-2 Connector 80P

Table 7-4: SCA-2 Connector

80-pin connector contact and signal name			Cable conductor numbers are not applicable	80-pin connector contact and signal name		
1	12 V Charge	(L)		(L)	12 V Ground	41
2	12 V	(S)		(L)	12 V Ground	42
3	12 V	(S)		(L)	12 V Ground	43
4	12 V	(S)		(S)	Mated 1	44
5	Reserved/ESI-1	(S)		(L)	-EFW	45
6	Reserved/ESI-2	(S)		(L)	DIFFSNS	46
7	-DB(11)	(S)		(S)	+DB(11)	47
8	-DB(10)	(S)		(S)	+DB(10)	48
9	-DB(9)	(S)		(S)	+DB(9)	49
10	-DB(8)	(S)		(S)	+DB(8)	50
11	-I/O	(S)		(S)	+I/O	51
12	-REQ	(S)		(S)	+REQ	52
13	-C/D	(S)		(S)	+C/D	53
14	-SEL	(S)		(S)	+SEL	54
15	-MSG	(S)		(S)	+MSG	55
16	-RST	(S)		(S)	+RST	56
17	-ACK	(S)		(S)	+ACK	57
18	-BSY	(S)		(S)	+BSY	58
19	-ATN	(S)		(S)	+ATN	59
20	-DB(P)	(S)		(S)	+DB(P)	60
21	-DB(7)	(S)		(S)	+DB(7)	61
22	-DB(6)	(S)		(S)	+DB(6)	62
23	-DB(5)	(S)		(S)	+DB(5)	63
24	-DB(4)	(S)		(S)	+DB(4)	64
25	-DB(3)	(S)		(S)	+DB(3)	65
26	-DB(2)	(S)		(S)	+DB(2)	66
27	-DB(1)	(S)		(S)	+DB(1)	67
28	-DB(0)	(S)		(S)	+DB(0)	68
29	-DB(P1)	(S)		(S)	+DB(P1)	69
30	-DB(15)	(S)		(S)	+DB(15)	70
31	-DB(14)	(S)		(S)	+DB(14)	71
32	-DB(13)	(S)		(S)	+DB(13)	72
33	-DB(12)	(S)		(S)	+DB(12)	73
34	5 V	(S)		(S)	Mated 2	74
35	5 V	(S)		(L)	5 V Ground	75
36	5 V Charge	(L)		(L)	5 V Ground	76
37	Spindle Sync	(L)		(L)	Active LED Out	77
38	MTRON	(L)		(L)	DLYD_START	78
39	SCSI ID (0)	(L)		(L)	SCSI ID (1)	79
40	SCSI ID (2)	(L)		(L)	SCSI ID (3)	80

7.3.1.3 Floppy Disk Port Connection

Table 7-5: Floppy Disk Connector

Pin	Name	Pin	Name
1	GND	2	FD_DENSEL
3	GND	4	n/c
5	Key	6	FD_DRATE0
7	GND	8	FD_INDEX_L
9	GND	10	FD_MTR0_L
11	GND	12	FD_DR1_L
13	GND	14	FD_DR0_L
15	GND	16	FD_MTR1_L
17	FD_MSEN1	18	FD_DIR_L
19	GND	20	FD_STEP_L
21	GND	22	FD_WDATA_L
23	GND	24	FD_WGATE_L
25	GND	26	FD_TRK0_L
27	FD_MSEN0	28	FD_WPROT_L
29	GND	30	FD_RDATA_L
31	GND	32	FD_HDSEL_L
33	GND	34	FD_DSKCHG_L

7.3.1.4 BERG* 240-pin Right Angle 5 X 48 Connector

Table 7-6: BERG 240-Pin Right Angle 5 X 48 Connector Pinout*

	ROW				
Column	**A**	**B**	**C**	**D**	**E**
1	RESET(1)	GND	DD8 (4)	GND	FD_DSKCHG_L
2	DD7 (3)	GND	DD9 (6)	GND	FD_HDSEL_L
3	DD6 (5)	GND	DD10 (8)	GND	FD_RDATA_L
4	DD5 (7)	GND	DD11 (10)	GND	FD_WPROT_L
5	DD4 (9)	GND	DD12 (12)	GND	FD_MSEN0
6	DD3 (11)	GND	DD13 (14)	GND	FD_TRK0_L
7	DD2 (13)	GND	DD14 (16)	GND	FD_WGATE_L
8	DD1 (15)	GND	DD15 (18)	GND	FD_WDATA_L
9	DD0 (17)	GND	GND	GND	FD_STEP_L
10	GND	GND	DIOW (23)	GND	FD_DIR_L
11	DMARQ (21)	GND	CSEL (28)	GND	FD_MSEN1
12	GND	GND	DIOR (25)	GND	FD_MTR1_L
13	IORDY (27)	GND	GND	GND	FD_DR0_L
14	DMACK (29)	GND	RESERVED (32)	GND	FD_DR1_L
15	GND	GND	PDIAG (34)	GND	FD_MTR0_L
16	INTRQ (31)	GND	DA2 (36)	GND	FD_INDEX_L
17	DA1 (33)	GND	CS0 (37)	GND	FD_DRATE0
18	DASP (39)	GND	DA0 (35)	GND	KEY
19	GND	GND	CS1 (38)	GND	N/C
20	GND	GND	GND	GND	FD_DENSEL
21	GND	GND	GND	GND	OEM 1
22	GND	GND	S68 (-DB 11)	GND	OEM 2
23	GND	GND	S34 (+DB 11)	GND	OEM 3
24	GND	GND	S65 (-DB8)	S32 (+DB 9)	S67 (-DB 10)
25	+12 V	+12 V	S31 (+DB 8)	S66 (-DB 9)	S33 (+DB 10)
26	+12 V	+12 V	S62 (-C/D)	S29 (+REQ)	S64 (-I/O)
27	+12 V	+12 V	S28 (+C/D)	S63 (-REQ)	S30 (+I/O)
28	+12 V	+12 V	S59 (-RST)	S26 (+MSG)	S61 (-SEL)
29	+12 V	+12 V	S25 (+RST)	S60 (-MSG)	S27 (+SEL)
30	+12 V	+12 V	S56	S23 (+BSY)	S58 (-ACK)
31	+12 V	+12 V	S22	S57 (-BSY)	S24 (+ACK)
32	+12 V	+12 V	S53 (RESERVED)	S20	S55 (-ATN)
33	+12 V	+12 V	S19 (RESERVED)	S54	S21 (+ATN)
34	+12 V	+12 V	S50	S17 (TERMPWR)	S52 (TERMPWR)
35	+12 V	+12 V	S16 (DIFFSENS)	S51 (TERMPWR)	S18 (TERMPWR)
36	+12 V	+12 V	S47 (-DB 7)	S14 (+DB P)	S49
37	+5 V	+5 V	S13 (+DB 7)	S48 (-DB P)	S15
38	+5 V	+5 V	S44 (-DB 4)	S11 (+DB5)	S46 (-DB 6)
39	+5 V	+5 V	S10 (+DB 4)	S45 (-DB 5)	S12 (+DB 6)
40	+5 V	+5 V	S41 (-DB 1)	S8 (+DB 2)	S43 (-DB 3)

	ROW				
Column	**A**	**B**	**C**	**D**	**E**
41	+5 V	+5 V	S7 (+DB 1)	S42 (-DB 2)	S9 (+DB 3)
42	+5 V	+5 V	S38 (-DB 15)	S5 (+DB P1)	S40 (-DB 0)
43	+5 V	+5 V	S4 (+DB 15)	S39 (-DB P1)	S6 (+DB 0)
44	+5 V	+5 V	S35 (-DB 12)	S2 (+DB 13)	S37 (-DB 14)
45	+5 V	+5 V	S1 (+DB 12)	S36 (-DB 13)	S3 (+DB 14)
46	+5 V	+5 V	GND	GND	GND
47	+5 V	+5 V	GND	SDA	Reser Ved
48	+5 V	+5 V	GND	PWR_GOOD	SCL

7.3.1.5 IDE Connector

Table 7-7: IDE Connector

Pin	Signal	Pin	Signal
1	RSTDRV	2	GROUND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD1
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GROUND	20	KEY PIN
21	DRQ	22	GROUND
23	DIOW	24	GROUND
25	DIOR	26	GROUND
27	IORDY	28	CSEL
29	DACK	30	GROUND
31	IRQ	32	No Connection
33	DA1	34	No Connection
35	DA0	36	DA2
37	CS1P_L	38	DS3P_L
39	DHACT_L	40	GROUND

7.3.1.6 Power Connectors

Table 7-8: Power Supply Connectors

Pin #	Signal:
1	VCC12
2	GND
3	GND
4	VCC5

7.3.2 Peripheral Bay Board(Chassis Side) Connector Assignments

Table 7-9: Blind Mate Connector

R3 Row	BERG* 240-Pin Connector (HEADER/RA FEMALE)				
Column	**A**	**B**	**C**	**D**	**E**
1	RESET(1)	GND	DD8 (4)	GND	FD_DSKCHG_L
2	DD7 (3)	GND	DD9 (6)	GND	FD_HDSEL_L
3	DD6 (5)	GND	DD10 (8)	GND	FD_RDATA_L
4	DD5 (7)	GND	DD11 (10)	GND	FD_WPROT_L
5	DD4 (9)	GND	DD12 (12)	GND	FD_MSEN0
6	DD3 (11)	GND	DD13 (14)	GND	FD_TRK0_L
7	DD2 (13)	GND	DD14 (16)	GND	FD_WGATE_L
8	DD1 (15)	GND	DD15 (18)	GND	FD_WDATA_L
9	DD0 (17)	GND	GND	GND	FD_STEP_L
10	GND	GND	DIOW (23)	GND	FD_DIR_L
11	DMARQ (21)	GND	CSEL (28)	GND	FD_MSEN1
12	GND	GND	DIOR (25)	GND	FD_MTR1_L
13	IORDY (27)	GND	GND	GND	FD_DR0_L
14	DMACK (29)	GND	RESERVED (32)	GND	FD_DR1_L
15	GND	GND	PDIAG (34)	GND	FD_MTR0_L
16	INTRQ (31)	GND	DA2 (36)	GND	FD_INDEX_L
17	DA1 (33)	GND	CS0 (37)	GND	FD_DRATE0
18	DASP (39)	GND	DA0 (35)	GND	KEY
19	GND	GND	CS1 (38)	GND	N/C
20	GND	GND	GND	GND	FD_DENSEL
21	GND	GND	GND	GND	OEM 1
22	GND	GND	S68 (-DB 11)	GND	OEM 2
23	GND	GND	S34 (+DB 11)	GND	OEM 3
24	GND	GND	S65 (-DB8)	S32 (+DB 9)	S67 (-DB 10)
25	+12 V	+12 V	S31 (+DB 8)	S66 (-DB 9)	S33 (+DB 10)
26	+12 V	+12 V	S62 (-C/D)	S29 (+REQ)	S64 (-I/O)
27	+12 V	+12 V	S28 (+C/D)	S63 (-REQ)	S30 (+I/O)
28	+12 V	+12 V	S59 (-RST)	S26 (+MSG)	S61 (-SEL)
29	+12 V	+12 V	S25 (+RST)	S60 (-MSG)	S27 (+SEL)
30	+12 V	+12 V	S56	S23 (+BSY)	S58 (-ACK)
31	+12 V	+12 V	S22	S57 (-BSY)	S24 (+ACK)
32	+12 V	+12 V	S53 (RESERVED)	S20	S55 (-ATN)
33	+12 V	+12 V	S19 (RESERVED)	S54	S21 (+ATN)
34	+12 V	+12 V	S50	S17 (TERMPWR)	S52 (TERMPWR)
35	+12 V	+12 V	S16 (DIFFSENS)	S51 (TERMPWR)	S18 (TERMPWR)
36	+12 V	+12 V	S47 (-DB 7)	S14 (+DB P)	S49
37	+5 V	+5 V	S13 (+DB 7)	S48 (-DB P)	S15
38	+5 V	+5 V	S44 (-DB 4)	S11 (+DB5)	S46 (-DB 6)

R3 Row	BERG* 240-Pin Connector (HEADER/RA FEMALE)				
Column	**A**	**B**	**C**	**D**	**E**
39	+5 V	+5 V	S10 (+DB 4)	S45 (-DB 5)	S12 (+DB 6)
40	+5 V	+5 V	S41 (-DB 1)	S8 (+DB 2)	S43 (-DB 3)
41	+5 V	+5 V	S7 (+DB 1)	S42 (-DB 2)	S9 (+DB 3)
42	+5 V	+5 V	S38 (-DB 15)	S5 (+DB P1)	S40 (-DB 0)
43	+5 V	+5 V	S4 (+DB 15)	S39 (-DB P1)	S6 (+DB 0)
44	+5 V	+5 V	S35 (-DB 12)	S2 (+DB 13)	S37 (-DB 14)
45	+5 V	+5 V	S1 (+DB 12)	S36 (-DB 13)	S3 (+DB 14)
46	+5 V	+5 V	GND	GND	GND
47	+5 V	+5 V	GND	SDA	Reser Ved
48	+5 V	+5 V	GND	PWR_GOOD	SCL

Table 7-10: Wide SCSI Connector

Wide SCSI Connector			
1	S1 (+DB 12)	S35 (-DB 12)	35
2	S2 (+DB 13)	S36 (-DB 13)	36
3	S3 (+DB 14)	S37 (-DB 14)	37
4	S4 (+DB 15)	S38 (-DB 15)	38
5	S5 (+DB P1)	S39 (-DB P1)	39
6	S6 (+DB 0)	S40 (-DB 0)	40
7	S7 (+DB 1)	S41 (-DB 1)	41
8	S8 (+DB 2)	S42 (-DB 2)	42
9	S9 (DB 3)	S43 (-DB 3)	43
10	S10 (+DB 4)	S44 (-DB 4)	44
11	S11 (+DB5)	S45 (-DB 5)	45
12	S12 (+DB 6)	S46 (-DB 6)	46
13	S13 (+DB 7)	S47 (-DB 7)	47
14	S14 (+DB P)	S48 (-DB P)	48
15	S15	S49	49
16	S16 (DIFFSENS)	S50	50
17	S17 (TERMPWR)	S51 (TERMPWR)	51
18	S18 (TERMPWR)	S52 (TERMPWR)	52
19	S19 (RESERVED)	S53 (RESERVED)	53
20	S20	S54	54
21	S21 (+ATN)	S55 (-ATN)	55
22	S22	S56	56
23	S23 (+BSY)	S57 (-BSY)	57
24	S24 (+ACK)	S58 (-ACK)	58
25	S25 (+RST)	S59 (-RST)	59
26	S26 (+MSG)	S60 (-MSG)	60
27	S27 (+SEL)	S61 (-SEL)	61
28	S28 (+C/D)	S62 (-C/D)	62
29	S29 (+REQ)	S63 (-REQ)	63
30	S30 (+I/O)	S64 (-I/O)	64
31	S31 (+DB 8)	S65 (-DB8)	65

Wide SCSI Connector			
32	S32 (+DB 9)	S66 (-DB 9)	66
33	S33 (DB +10)	S67 (-DB 10)	67
34	S34 (DB +11)	S68 (-DB 11)	68

Table 7-11: 40-position Header (IDE)

IDE 40 Pin Connector			
Pin			**Pin**
1	RESET	GND	2
3	DD7	DD8	4
5	DD6	DD9	6
7	DD5	DD10	8
9	DD4	DD11	10
11	DD3	DD12	12
13	DD2	DD13	14
15	DD1	DD14	16
17	DD0	DD15	18
19	GND	KEYPIN (NC)	20
21	DMARQ	GND	22
23	DIOW	GND	24
25	DIOR	GND	26
27	IORDY	CSEL	28
29	DMACK	GND	30
31	INTRQ	RESERVED	32
33	DA1	PDIAG	34
35	DA0	DA2	36
37	CS0	CS1	38
39	DASP	GND	40

Table 7-12: 34-position Header (Floppy)

Floppy Connector			
Pin			**Pin**
1	GND	FD_DENSEL	2
3	GND	N/C	4
5	KEY	FD_DRATE0	6
7	GND	FD_INDEX_L	8
9	GND	FD_MTR0_L	10
11	GND	FD_DR1_L	12
13	GND	FD_DR0_L	14
15	GND	FD_MTR1_L	16
17	FD_MSEN1	FD_DIR_L	18
19	GND	FD_STEP_L	20
21	GND	FD_WDATA_L	22
23	GND	FD_WGATE_L	24
25	GND	FD_TRK0_L	26
27	FD_MSEN0	FD_WPROT_L	28

Floppy Connector			
29	GND	FD_RDATA_L	30
31	GND	FD_HDSEL_L	32
33	GND	FD_DSKCHG_L	34

Table 7-13: 20-position Power Connector

20-position Power Connector			
PIN			**PIN**
1	+12 V	+12 V	11
2	GND	GND	12
3	+12 V	+12 V	13
4	+5 V	+5 V	14
5	GND	GND	15
6	+5 V	+5 V	16
7	GND	GND	17
8	SCL	SDA	18
9	GND	GND	19
10	PWR_GOOD	Reserved	20

Table 7-14: 3-position Header

	3 Pin Header (22-44-7031)
1	Reserved
2	Reserved
3	Reserved

7.3.3 System Power Supply Connector Assignments

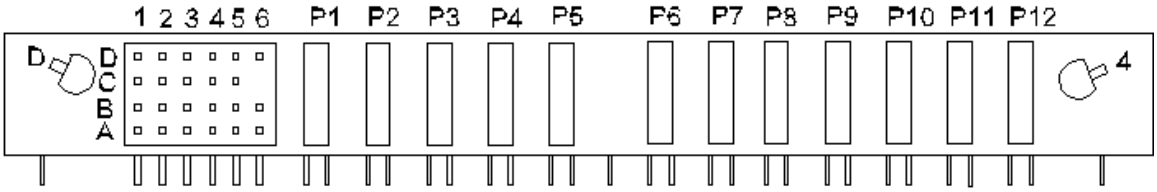
The pin assignment for the DC connector is shown in Table 7-15.

Table 7-15: DC Connector Pin Assignment

Signal Pins						
	1	**2**	**3**	**4**	**5**	**6**
D	+12 V LS	PG	AC_OK	+15 V Stdby	Remote SEN RTN	- 12 V
C	A0	SCL	FAULT	PRED FAIL	+12 V SENSE	KEY
B	A1	SDA	+3.3 V SENSE	+5 V SENSE	+5 V Stdby	+5 V Stdby
A	+3.3 V LS	Power Present	Spare	+5 V LS	PS_ON	PS_KILL

Power Blades											
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
+12 V	+12 V	GND	GND	GND	GND	GND	GND	+5 V	+5 V	3.3 V	3.3 V

Notes: PS_On and PS_Kill are 1.2 mm shorter in mating length compared to others in the connector.



Notes: Power blades (P1 – P12) are rated at 25 A each for operation.
Signal pins (A1 – D6) are rated at 1 A each for operation.

Figure 7-3: DC Connector Drawing

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8. Reliability

8.1 MTBF

Table 8-1 lists the calculated AC450NX server system hard mean time between failures (MTBF). A hard failure indicates a permanent or repeatable failure that can be readily remedied by replacing the faulty part with a good part. The MTBF calculations are derived using the procedures described in Intel's *Environmental Standards Handbook, (Doc. #662394-03).*

Table 8-1: AC450NX Server System MTBF at 35°C

Sub Assembly Description	Sub Assembly QTY	Total Sub Assembly MTBF (Hrs)	Total Sub Assembly Failure Rate (FITs)
CPU baseboard	1	146,883	5,694
VRM modules	6	213,709	9,359
CPU Pentium® II Xeon™ processor	1	312,534	6,254
Memory board	4	318,043	3,200
Peripheral bay backplane	2	NA	8,136
Front panel board	1	633,564	5,898
PHP-IO-BB	1	NA	1,159
IO RISER	1	1,248,711	796
MID-PLN	1	411,111	1,121
Processor slot termination board	1	NA	801
CD ROM Hitachi* IDE	1	500,000	3,845
PRO 100 B	1	580,540	2,000
Power supply 750 W	2	14,668	23,438
1.44 MB 3.5" FDU	1	405,000	2,469
FAN	0[1]	90,167	NA
MTBF in Hrs [2]		**13,481**	
Total Failure Rate (FITs)			**74,177**

Notes: **1.** System cooling fans are redundant in the factory default configuration. A single fan failure does not require an *immediate* shutdown of the system. The chance of a second fan failure during this time is considered very slight. However, as soon as a replacement fan becomes available, it should be replaced to minimize the risk for two system fan failures. Should a power supply fan fail, the power supply can only be replaced without shutting down the system in a 2+1 configuration (a total of three power supplies must be present).

2. The MTBF numbers are for a standard system with four Pentium® II Xeon™ processors and two memory modules with 0 MB memory.

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9. Regulatory Specifications

The AC450NX server system with the Ak450NX board set meets the specifications and regulations for safety and electromagnetic compatibility (EMC) defined in this chapter.

The AC450NX server system complies with *EMC Directive 89/336/EEC*, using standards *EN55022 Class A* and *EN50082-1*, and the *Low Voltage Directive 73/23/EEC*, using the *EN60 950* standard.

9.1 Safety Compliance

USA / Canada:	UL 1950, 3rd Edition / CSA950-95
Europe:	TUV/GS to EN60950 (A1+A2+A3+A4) Low Voltage Directive (73/23/EEC) (CE Mark)
International:	CB Certificate to IEC950 plus EMKO-TSE(74-SEC) 207/94

9.2 Electromagnetic Compatibility

USA:	FCC 47 CFR Parts 2 and 15, Class A.
Canada:	ICES-003 Class A.
Europe:	EN55022, Class A, Radiated & Conducted Emissions. EN50082-1 Generic Immunity Standard. EN61000-4-2 ESD Immunity (level 2 contact discharge, level 3 air discharge). EN61000-4-3 Radiated Immunity (level 2). EN61000-4-4 Electrical Fast Transient (level 2). EN61000-3-2; Harmonic Currents.
International:	CISPR 22, Class A.
Australia/New Zealand	AS/NZS 3548, Class A Limits (CISPR 22 Class A Limits).
Japan:	VCCI Class A ITE (CISPR 22 Class A Limits)

9.2.1 CE Mark

The CE marking on this product indicates that it is in compliance with the European community's *EMC Directive (89/336/EEC)* and *Low Voltage Directive (73/23/EEC).*

9.2.2 Electromagnetic Compatibility Notice (USA)

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio

frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at his own expense.

9.2.3 Electromagnetic Compatibility Notices (International)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:

This is a Class A product based on the standard of the Voluntary Control Council for Interference by Information Technology Equipment (VCCI). If this equipment is used in a domestic environment, radio disturbance may arise. When such trouble occurs, the user may be required to take corrective actions.

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: “Appareils Numériques,” NMB-003 édictée par le Ministre Canadian des Communications.

English translation of the notice above:

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled “Digital Apparatus,” ICES-003 of the Canadian Department of Communications.

10. Environmental Specification

The AC450NX server system was tested to the environmental specifications indicated in Table 10-1.

Table 10-1: Environmental Specifications Summary

Environmental Feature	Specification
Operating temperature	5° to 40°C (41° to 95°F). See Altitude exception.
Nonoperating temperature	-40°C to 70°C (-104° to 158°F).
Altitude	0 to 3048 m (0 to 10,000 ft). Note: Maximum ambient temperature is linearly derated between 1520 m (5000 ft) and 3048 m (10,000 ft) by 1°C per 305 m (1000 ft).
Operating humidity	85%, noncondensing at 40°C (104°F). <33°C (59.4°F) wet bulb at 40°C (104°F) without peripherals.
Nonoperating humidity	95%, noncondensing at +55°C (131°F).
Vibration	Random, nonoperating • 2.2 g RMS • 5 Hz @ 0.001 g^2/Hz to 20 Hz @ 0.01 g^2/Hz • 20 Hz to 500 Hz @ 0.01 g^2/Hz
Operating shock	• 2.0 g, half sine impulse • 11 ms duration
Nonoperating shock	• 30 g, trapezoidal • 170 in/s delta V
Safety	UL 1950 – CSA 950-95, 3rd Edition (USA/Canada). TUV/GS to EN60950, 2nd Edition (Europe – German GS Mark & CE Mark – complies with Directive 73/23/EEC). CB Certificate to IEC 950, 2nd Edition plus EMKO-TSE (74-SEC) 207/94 (International).
Emissions	FCC Class A tested to CISPR 22 Class A, EN 55022, Class A.
Immunity	EN50082-1.
Harmonic currents	EN61000-3-2.
Electrostatic discharge (ESD)	Tested to ESD levels up to 20 kilovolts (kV) air discharge without physical damage as per the *Intel® Environmental Standards Handbook* (Doc. #662394-03)
AC Voltage/frequency	90 to 132 volts and 180 to 264 volts / 47 to 63 Hz.
Source interrupt	No loss of data for power line dropout of one cycle.
Surge nonoperating and operating	2.0 kV unidirectional and 3.0 kV ring wave.
Acoustic	Sound pressure: <55 dBA at ambient temperatures <28°C measured at bystander positions in operating mode. Sound power: < 6.5 BA at ambient temperatures <28°C in operating mode.