Ak450NX Server Board Set

Technical Product Specification

Revision 1.1

November 1998

Enterprise Server Group

intel. ®

Revision History

Date	Rev	Modifications
10/98	1.00	Compilation of first release.
11/98	1.10	Updated memory board layout

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Conventions and Terminology

This document uses the following terms and abbreviations:

Term	Definition
Ω	ohm
μA	microamp (0.000001 amps)
μf	microfarad (0.000001 farads)
μs	microsecond (0.000001 seconds)
A	ampere (amp)
A/D	analog to digital
ABP	address bit permuting
AC	alternating current
ACPI	advanced configuration and power interface
AGTL+	assisted gunning transceiver logic plus
ANSI	American National Standards Institute
AP	application processor
APIC	Intel® advanced programmable interrupt controller
ASCII	American Standard Code for Information Interchange
ASIC	application specific integrated circuit
BAID	BIOS aware IPL device
BBS	BIOS Boot Specification, Version 1.01
BCV	boot connection vector
BEV	bootstrap entry vector
BGA	ball grid array
BIOS	basic input output system
BIST	built-in self test
Bitblt	bit-block transfer
BMC	baseboard management controller
BSP	bootstrap processor
byte	an 8-bit quantity
C	Celsius
C2C	card-to-card
CBR	CAS-before-RAS
CD-ROM	compact disk read only memory
CE Mark	indicates certification in the European Community
CISPR	Comite Int'l Special Des Perturbation Radioelectriques
CMOS	complementary metal-oxide semiconductor
CPU	central processing unit
CU	Configuration Utility
DEMKO	Danishe Elektriske Materiellkontroll (Danish Board of Testing and Approval of Electrical Equipment)
DIMM	dual inline memory module
DMA	direct memory access
DMI	desktop management interface
DOS	disk operating system
DRAM	dynamic random access memory
DWORD	double word -a 32-bit quantity
EBDA	extended BIOS data area
ECC	error correction code
ECP	extended capabilities port
EDO	extended data out (DRAM type)

Term	Definition
EEPROM	electrically erasable programmable read only memory
EMP	emergency management port
EN	European Standard (Norme Européenne or Europäische Norm)
EPP	enhanced parallel port
EPS	external product specification
ESCD	extended system configuration data
EU	European Union
FCC	Federal Communications Commission (USA)
FIFO	first-in first-out
FP	front panel
FPC	front panel controller
FRB	fault resilient boot
FRC	functional redundancy checking
FRU	field replaceable unit
FSB	front-side bus
GB	gigabyte - 1024 MB
GB/s	gigabytes per second
GPNV	general purpose nonvolatile
GUI	graphical user interface
HSC	hot-swap controller
Hz	hertz (cycles per second)
I/O	input/output
I^{2}C	inter integrated circuit
I$_2$O	intelligent I/O
ICMB	Intelligent Chassis Management Bus
ID	identification
IDE	integrated drive electronics
IERR	internal error
iFLASH	Flash Update Utility
IOAPIC	Intel® I/O Advanced Programmable Interrupt Controller
IOP	I/O processor
IPL	initial program load
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IRQ	interrupt request
ISA	industry standard architecture
ISC	Intel® Server Console
ISP	in-system programming
KB	kilobyte - 1,024 bytes
KBC	keyboard controller
LCD	liquid crystal display
LED	light emitting diode
LFM	linear feet per minute
LVDS	low-voltage differential SCSI
M	mega
m	milli
mA	milliamps
MB	megabyte - 1,024KB
MB/s	megabytes per second
MBE	multi-bit error

Term	Definition
MD	memory data
MHz	megahertz
MIF	management information format
MIOC	memory and I/O controller (450NX PCIset)
MP	multiprocessor
ms	milliseconds (0.001 seconds)
MTBF	mean time between failures
MTRR	memory type range register
MUX	multiplexor
mV	microvolt (0.000001 volts)
NEMKO	Norges Elektriske Materiellkontroll (Norwegian Board of Testing and Approval of Electrical Equipment)
NMI	nonmaskable interrupt
ns	nanosecond
NVRAM	nonvolatile random access memory
OEM	original equipment manufacturer
OPSM	operating system directed power management
OS	operating system
OS/AML	OS/ACPI machine language
P2P	PCI-to-PCI bridge
PAL	programmable array logic
PCC	power control circuitry
PCI	peripheral component interconnect
PCIset	450NX chip set
PD	presence detect
PDE	presence detect enable
PERR	parity error
pf	picofarad (10^{-12})
PHP	PCI hot plug
PIC	program interrupt control
PID	programmable interrupt device
PIIX4e	PCI ISA/IDE Xcelerator controller
PLD	programmable logic device
PME	power management event
PnP	Plug and Play
POST	power-on self test
PS	power supply
PXB	PCI eXpansion bridge
RAM	random access memory
RAS/CAS	row address select/column address select
RCCU	RAS/CAS control units
RCG	RAS/CAS generator (450NX PCIset)
ROM	read-only memory
RTC	real-time clock
SBE	single-bit error
SCA	single connector attachment
SCI	scalable coherent interconnect
SCSI	small computer systems interface
SDR	sensor data record
SDRAM	synchronous DRAM
SECC	single edge connector cartridge

Term	Definition
SEEPROM	serial electrically erasable programmable read only memory
SEL	system event log
SEMKO	Sverge Elektriske Materiellkontroll (Swedish Board of Testing and Approval of Electrical Equipment)
SERR	system error
SMBIOS	system management BIOS
SMC	Standard Microsystems Corp.
SMI	system management interrupt
SMIC	system management interface chip
SMM	server monitor module
SMP	symmetric multiprocessing
SMRAM	system management RAM
SMS	system management software
SPI	serial peripheral interface
SSU	System Setup Utility
STD	SaveToDisk
SVGA	super video graphics array
TBD	to be determined
TSOP	thin small outline package
TTL	transistor-transistor logic
TUV	Technischer Ügerwachungsverein (English: Technical Inspection Association)
UART	universal asynchronous receiver/transmitter
USB	Universal Serial Bus
USWC	uncacheable-speculative-write-combining
V	volt
VA	volt-ampere
Vac	alternating current (AC) voltage
VCCI	Voluntary Control Council for Interference (by data processing equipment and electronic office machines)
Vdc	volts of direct current
VGA	video graphics array
VID	voltage ID
VMC	voltage management control
VRM	voltage regulator module
Vstby	volts standby
Vtt	termination voltage
W	watt
Wdc	watts direct current
WE	write enable
WOL	Wake On LAN
WORD	a 16 bit quantity

References

Refer to the following documents for additional information:

- *AC450NX (Polar) Server Management External Product Specification*
- *AC450NX Server System Product Guide (Intel Part #678269-002)*
- *Ak450NX MP Server Board Set Specification Update*
- *BIOS Boot Specification, Ver. 1.01*
- *Extended System Configuration Data Specification, Rev. 1.02A*
- *FRU and SDR Load Utility External Product Specification*
- *Intel® Board Environmental Specification 112000, Rev. G*
- *Intel® Multiprocessor Specification (MPS), Ver. 1.1*
- *Intel® Multiprocessor Specification (MPS), Ver. 1.4*
- *Pentium® II Xeon™ Processor Datasheet*
- *Peripheral Component Interconnect (PCI) Local Bus Specification, Rev. 2.1 (PCI Spec., Rev. 2.1)*
- *Plug and Play ISA Specification, Rev. 1.0a*
- *Slot 2 Connector Specification*
- *System Management BIOS (SMBIOS) Specification, Ver. 2.1*
- *VRM 8.3 DC-DC Converter Design Guidelines*

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1. Introduction

This document describes the architecture, functionality and interfaces of the Ak450NX board set. The Ak450NX is a 1-4 processor server board set based on the Pentium® II Xeon™ processor and the Intel® 450NX PCIset. The Pentium II Xeon processor is the next generation Intel architecture processor beyond the current Pentium® II and Pentium® Pro processors. Both the Pentium II Xeon processor and the 450NX PCIset have been optimized for 4-way server applications. The boardset layout was designed specifically to maximize expandability, perfomance, and accessibility while maintaining a low profile appropriate for use in rack mountable chassis. Refer to the *Ak450NX MP Server Board Set Specification Update* for the most recent specification updates concerning the board set. The combination of this TPS and the specification update provide an updated overview of the Ak450NX multiprocessor (MP) server board set.

Features

- 1-4 Pentium® II Xeon™ processors
- Intel® 450NX PCIset
- Support for up to 8 GB of 3.3 V EDO DRAM (DIMMs)
- Low profile board set layout designed specifically for rack mountable system chassis
- Three peer PCI buses (two 32-bit and one 64-bit bus; all are 5 V and *Peripheral Component Interconnect (PCI) Local Bus Specification, Rev. 2.1,(PCI Spec., Rev. 2.1)* compliant)
- Eleven full length I/O expansion slots (four PCI hot plug 64-bit, six 32-bit, and one ISA [shared with one of the 32-bit PCI slots])
- Onboard dual channel low-voltage differential SCSI (LVDS) controller for peripheral devices (Symbios 53C896*)
- Single IDE connector
- PCI ISA/IDE Xcelerator controller (PIIX4E) PCI to ISA bridge
- Universal Serial Bus (USB)
- SMC Super I/O* component to handle all PC legacy functions (keyboard, mouse, serial, parallel, etc.)
- Programmable interrupt device (PID) - custom Intel® application specific integrated circuit (ASIC), which provides interrupt steering and I/O advanced programmable interrupt controller (APIC) capabilities
- Complete built-in server management capabilities
- Intelligent Platform Management Bus (IPMB) based on I^2C for communicating server management information between all Intelligent Platform Management Interface (IPMI) compliant boards on the chassis
- Field replaceable unit (FRU) information stored on all boards (P/N, S/N, board name, etc.), and temperature sensors located on all major boards.

Document Structure and Outline

The information contained in this document is organized into five chapters. Each board in the Ak450NX board set is described in detail in *Chapter 2 Board Set Details*. Additional chapters for added detail on server management and board set specifications are also provided. A description of each chapter is summarized below:

Chapter 1: Introduction
Provides an architectural overview of the Ak450NX board set

Chapter 2: Board Set Details
Provides the functional details of the board set

Chapter 3: BIOS Features
Describes the featues of the Ak450NX board set BIOS

Chapter 4: Server Management Implementation
> Describes the implementation details of the Ak450NX board set server management features

Chapter 5: Board Set Specifications
> Describes the electrical, mechanical, environmental, and regulatory specifications of the Ak450NX board set. It also provides specifications for the connectors and for the processor retention mechanism.

1.1   Architecture Overview

Figure 1-1 is a block diagram of the Ak450NX board set. The following sections briefly describe the various aspects of the Ak450NX board set architecture.
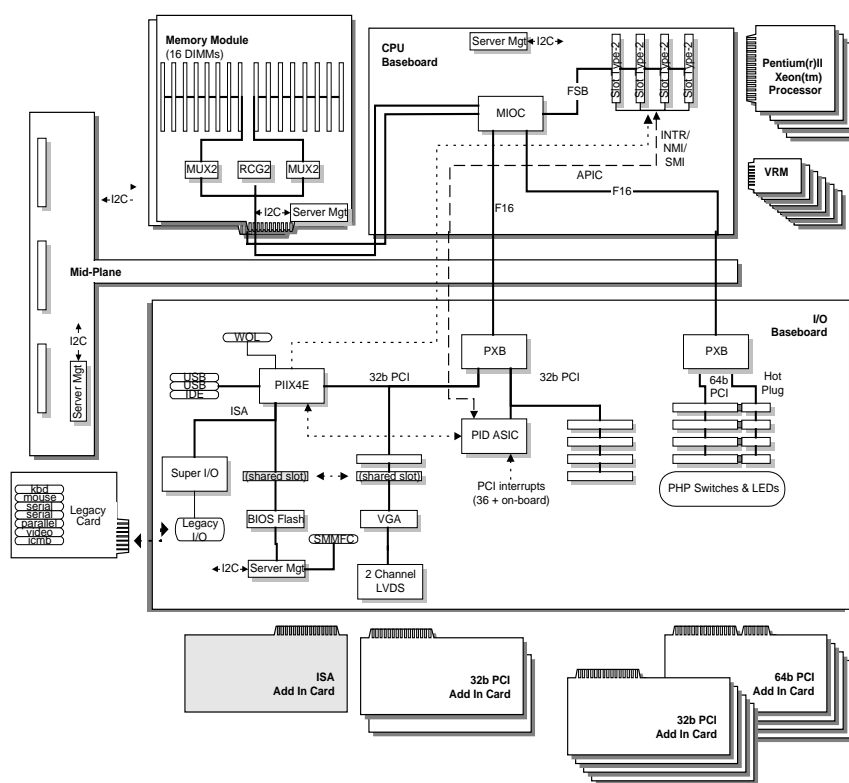
Figure 1-1: Ak450NX Board Set Block Diagram

1.2   Board Set Overview

The Ak450NX board set is a dual baseboard design that contains a total of seven individual boards.

- Central processing unit (CPU) baseboard (contains the processor and memory interface complexes)
- I/O baseboard (contains all I/O functions, including PCI and ISA slots)
- I/O riser card (plugs into the I/O baseboard and contains all legacy connectors (video connector, parallel port, 2 serial ports, keyboard and mouse connectors)
- Memory module (two memory modules are required for the operation of the complete board set)
- Interconnect midplane (provides connection between the I/O baseboard and CPU baseboard. Also provides the power distribution interfaces for the entire board set and system power supplies.)

- Front-side bus terminator module (used to terminate the processor bus when a processor is not installed into a processor slot)

The baseboards are connected to each other through the interconnect midplane and are laid horizontally to maintain a low profile suitable for a rack chassis. The two F16 buses of the 450NX PCIset electrically connect the two baseboards. Power to the board set is supplied through the interconnect midplane.
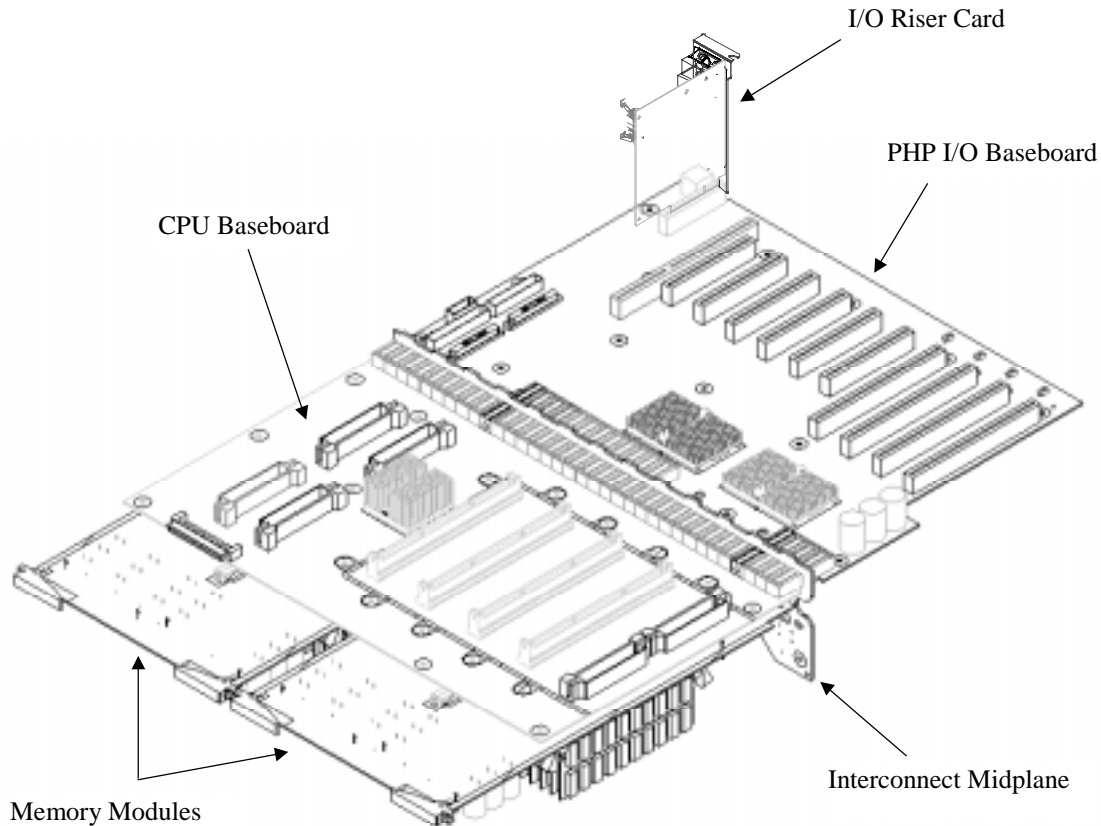
Figure 1-2: Ak450NX Board Set

1.2.1   CPU Baseboard

The Ak450NX CPU baseboard supports 1-4 Pentium II Xeon processors. Each processor, packaged in a single-edge connector cartridge (SECC), includes a 100 MHz front-side bus interface, a processor core operating at four or more times the front-side bus frequency (400+ MHz), and a back-side bus that operates at the full frequency of the processor core and supports 512K, 1 MB or 2 MB of L2 cache. Hardware support for processor fault resilient boot (FRB) is provided. A front-side bus (FSB) terminator module is required for any unoccupied processor slot.

Also connected to the front side bus and interfacing with the processors is the memory and I/O controller (MIOC) component of the 450NX PCIset. This component allows the processors to interface to the memory subsystem and I/O expansion (F16) buses, in addition to the other processors on the front-side bus. The memory subsystem interface allows connection to two Ak450NX memory modules through the interconnect midplane.

Power is supplied to the processors via plug-in voltage regulator modules (VRM). There are a total of six VRM sockets on the CPU baseboard which are connected to the four processors in the following manner: four VRMs supply the processor core voltage, and two VRMs supply the L2 cache core voltage, both of which are contained

within the Pentium II Xeon processor cartridge. VRMs may be installed incrementally as processors are added to the system or may be installed in advance of the processor to ease processor installations in the field.

In addition to the facilities described above, the CPU baseboard also supports the Ak450NX server management architecture by providing nonvolatile storage of baseboard and server management data, digital and analog data monitoring hardware, processor disabling controls and access to memory module management data. See *Chapter 2 Board Set Details* for more details on the CPU baseboard.

1.2.2   PCI Hot-plug I/O Baseboard

The Ak450NX PCI hot-plug (PHP) I/O baseboard provides the basis for a scalable, high performance, high-slot-count I/O subsystem. Three PCI bus segments are supported (all are peer buses), via two PXBs (the PXB is the PCI expander bridge component of the 450NX PCIset). Two 32-bit PCI segments are configured from the first PXB, while a single 64-bit PCI segment is configured from the second PXB. The 64-bit PCI segment hosts four PCI slots all of which are *PCI hot pluggable* when used with appropriate PCI hot plug adapters and operating systems (OS). There are a total of six 32-bit PCI slots on the two 32-bit bus segments (two slots on the primary (compatibility) 32-bit PCI bus, and four slots on the secondary 32-bit PCI bus).

The first of the two 32-bit PCI segments (known as the compatibility bus) hosts the PIIX4E ISA south bridge (with two IDE interfaces and two USB ports), a Cirrus Logic 5446* VGA controller (with 2 MB of video memory on the baseboard), a Symbios 53C896* LVDS controller for high performance mass strorage device support (i.e., boot drives, peripheral drive arrays, etc.), and two PCI slots. One of the PCI slots is shared with the single ISA slot (provided by the PIIX4E). Also provided by the PIIX4E is an SMC FDC37C937APM* Super I/O component (providing two serial ports, a parallel port, a keyboard controller and PS/2 keyboard and mouse ports, a floppy disk interface, and a real-time clock), and an X-bus with 2 MB of BIOS flash and an interface to the server management hardware. Note that the connectors for the serial ports, parallel port, video, and the PS/2 keyboard and mouse ports are provided on a separate I/O riser card (which is part of the Ak450NX board set). The I/O riser card plugs into the I/O baseboard vertically, next to the ISA slot.

The secondary 32-bit PCI segment hosts four PCI slots, and the PID ASIC. The PID provides interrupt steering functions (including support logic for use with the 8259A* interrupt controllers in the PIIX4E) and I/O APIC facilities. In addition to the standard IRQs, the PID supports a large number of PCI and onboard interrupt sources; a total of 64 interrupt routing table entries are available. A separate interrupt input will be provided for each of the four interrupts from every 64-bit PCI slot on the I/O baseboard. Separate INTA and INTB connections are provided from every 32-bit PCI slot, but INTC and INTD are bused (in a rotating pattern) from the slots on the 32-bit PCI segments; separate bused connections are provided for each 32-bit PCI segment.

In addition to the two 32-bit PCI bus segments, a third 64-bit PCI segment is included on the PHP I/O baseboard. The only components that reside on this bus are the four 64-bit PCI expansion connectors and the PCI hot-plug controller. Although all 32- and 64-bit PCI 2.1 compliant adapters are supported in these expansion slots. If the hot plug function of these expansion slots is to be used, then only adapters/drivers which are designed as hot pluggable devices should be installed.

In addition to the facilities described above, the I/O baseboard also implements the core of the Ak450NX server management architecture. See *Chapter 2 Board Set Details* for more details about the I/O baseboard.

1.2.3   I/O Riser Card

The I/O riser card plugs into the PHP I/O baseboard vertically and provides all of the necessary legacy connectors for video, parallel, serial, keyboard and mouse. The Intelligent Chassis Management Bus (ICMB) connects through the I/O riser card as well. All of the connectors are located on the riser card instead of on the PHP I/O baseboard because of real estate constraints on the PHP I/O baseboard.

The I/O riser card supports the Ak450NX server management architecture by providing nonvolatile storage of module and server management data. See *Chapter 2 Board Set Details* of this document for more details about the I/O riser card.

This card is common with the I/O riser card used in the Intel® A450NX MP server board set, which has features that are similar to those of the Ak450NX MP Server Board Set, except that it is designed in a different form factor suitable for a floor standing server chassis.

1.2.4   Memory Module

The Ak450NX memory module provides 16 sites for single high, 168-pin DIMMs, supporting up to 4 GB of 50 nanosecond (ns) or 60 ns 3.3 V buffered extended data out (EDO) DRAM; both 16-Mbit and 64-Mbit DRAMs may be used. To properly terminate the memory bus, both memory slots that are provided on the interconnect midplane must be populated by two memory modules, although only one module is required to be populated with memory (DIMMs). Each memory module is divided into four banks (4-DIMMs per bank) and always supports a 4:1 interleave. The minimum configuration is four 32-MB DIMMs (one full bank). The supported memory sizes range from 128 MB to 8 GB (4 GB per module). Supported memory configurations are:

- 32-, 64- and 256-MB DIMM modules
- 50 ns or 60 ns DRAM
- 4-, 8-, 16-, 24-, or 32-DIMMs (total number of DIMMs on both memory modules)
- Equal number of DIMMs in each module (except when only four DIMMs are used, then all four DIMMs must be in the primary module - Module 1)
- All DIMMs on a module must be identical in size and speed
- DIMM sizes may differ between memory modules

The memory module contains the RAS/CAS generator (RCG) and multiplexor (MUX) components of the 450NX PCIset. Each memory module (alone) can provide a peak bandwidth of 800 MB/s. In order to achieve the maximum memory bandwidth (1.067 GB/s peak), both memory modules must be installed and must contain at least two 4:1 interleaved, identically populated banks per module (i.e., 16 DIMMs).

The memory module also supports the Ak450NX server management architecture by providing nonvolatile storage of module and server management data and digital I/O hardware for determination of the installed DIMM types. See *Chapter 2 Board Set Details* for more details about the memory module.

1.2.5   Interconnect Midplane

The interconnect midplane is essentially a passive signal and power distribution interface to the other boards that make up Ak450NX board set. It directly links the two memory modules to the CPU baseboard, the CPU baseboard to the PHP I/O baseboard, and also provides three power supply input connectors for power distribution throughout the board set.

The interconnect midplane supports the Ak450NX server management architecture by providing nonvolatile storage of module and server management data. See *Chapter 2 Board Set Details* for more details about the midplane

1.2.6   Front-side Bus Terminator Module

The front-side bus (FSB) terminator module provides the necessary electrical termination for the processor's front-side advanced gunning transceiver logic plus (AGTL+) bus. The FSB terminator module is used if a processor is not installed into one of the processor slots. All processor slots must contain either a processor or an FSB terminator module for the bus to operate correctly.

The FSB terminator supports the Ak450NX server management architecture by providing nonvolatile storage of module and server management data. See *Chapter 2 Board Set Details* for more details about the FSB terminator module.

This card is common with the FSB terminator used in the Intel A450NX MP server board set, which has features similar to those of the Ak450NX MP server board set, except that it is designed in a different form factor suitable for a floor standing server chassis.

1.3   I/O Bus Support

1.3.1   PCI Bus

The Ak450NX board set provides three PCI peer buses; two 32-bit segments and one 64-bit segment. There are a total of six 32-bit PCI slots and five 64-bit slots. All three PCI buses are 5 V (with support for both 5 V and 3.3 V signaling), 33 MHz and compliant to the *PCI Spec., Rev. 2.1*. The PCI buses are operated synchronously with the processor bus, using the processor bus clock as a master clock. The input clock, received over the F16 interface, is divided by three to support the 33 MHz PCI bus. The board set will support PCI adapters that draw power from both 3.3 V and 5 V (signaling), although the power allocation from 3.3 V may be limited. Note that the 64-bit slots will accept both 32 and 64-bit adapters.

1.3.2   ISA Bus

The Intel® 82371AB PCI to ISA/IDE Accelerator (PIIX4E) component provides the bridge interconnect from the primary 32-bit PCI bus to an ISA bus. The PIIX4E also provides two IDE channels as well as the Universal Serial Bus (USB) interface. The ISA bus contains one slot, which is shared with the first PCI slot on the primary 32-bit PCI bus. Also on the ISA bus are the BIOS flash component, the SMC Super I/O component and the main Ak450NX board set server management controller. The SMC Super I/O component provides all legacy connections including keyboard, mouse, floppy disk controller, one parallel port and two serial ports. The server management interface chip (SMIC) and the baseboard management controller (BMC) are the heart of the Ak450NX board set's server management functionality. The SMIC is implemented with the programmable logic device (PLD), while the BMC is implemented with an 80C652* microcontroller. The SMIC actually resides on the ISA bus, while the BMC is located behind the SMIC.

1.4   Component Details

1.4.1   Microprocessor

The Ak450NX board set supports 1 to 4 Pentium II Xeon generation processors. The Pentium II Xeon processor is packaged in a 330-contact single edge connector cartridge (SECC), and contains a processor core, L2 cache components, and miscellaneous other components mounted to a fiberglass substrate. The substrate is then mounted to a cartridge, which includes a heat plate to which a heat sink is attached for heat dissipation.

The Pentium II Xeon processor is the next generation of Intel® architecture processors following the Pentium® II processor. The internal architecture of the Pentium II Xeon processor core is similar to that of the Pentium II processor (super scalar, super pipelined, speculative execution, 16KB L1 instruction cache, a 16KB data cache, and MMX™ technology).

Unlike the Pentium II processor, the Pentium II Xeon processor has a full speed (core frequency) interface between the processor core and the L2 cache. Not only is the cache interface performance higher with the Pentium II Xeon processor, it also supports larger cache sizes, either 512KB, 1 MB or 2 MB L2 caches. The Pentium II Xeon processor adds support for higher levels of scalability, and expanded 36-bit memory addressing support for memory capacities greater than 4 GB.

Initial processor core frequencies are targeted at 400 MHz and will increase in 50 MHz increments. The CPU baseboard has jumpers allowing the installation of processor frequencies ranging from 300 MHz to 650 MHz in 50 MHz increments. There will be limitations as to which processor frequencies will be supported. All processors in the system must be running at the same frequency and with the same size L2 cache. Also, mixed processor steppings will be supported on a limited basis.

Additionally, it is planned that the Ak450NX board set will support the next generation of the Pentium II Xeon processor.

1.4.2   450NX PCIset

The Ak450NX board set is based on the Intel 450NX PCIset. The 450NX is optimized for server platforms and offers the following features not found on previous Intel chip sets.

- Support for greater than 4 GB of memory addressing (36-bit addressing)
- Support for greater than two PCI peer buses
- 64-bit PCI bus support

In addition, the I/O performance of the 450NX has been increased from previous chip sets.

- 100 MHz front-side bus frequency with a peak bandwidth of 800 MB/s
- Dedicated 100 MHz memory bus with a peak bandwidth of 1.067 GB/s
- Two dedicated I/O buses (F16 buses) each with a peak bandwidth of 400 MB/s

The 450NX PCIset is comprised of four unique components; there are nine components over all.

- One memory and I/O component (MIOC), located on the CPU baseboard
- Two PCI eXpansion bus (PXB) components, both located on the I/O baseboard
- Two RAS/CAS generators (RCG), one located on each memory module
- Four data path multiplexors (MUX), two located on each memory module

1.4.2.1   MIOC

The memory & I/O component (MIOC) is packaged in a 540-pin ball grid array (BGA) package. The MIOC provides the interface between the processor bus, the memory bus and both of the F16 I/O buses. The MIOC dissipates 13-14 W and will be shipped with a heat sink.

1.4.2.2   PXB

The PCI eXpansion bridge (PXB) component is packaged in a 540-pin BGA package. It provides the interface between the F16 I/O bus and the PCI buses. The PXB can be configured to provide either two 32-bit PCI buses, or a single 64-bit PCI bus. Two PXBs are located on the I/O baseboard. One of them, PXB-0, is configured to provide the primary (compatibility) and secondary 32-bit PCI buses. The other, PXB-1, is configured to provide a single 64-bit PCI bus. Each PXB dissipates 7-8 W and will be shipped with a heat sink.

1.4.2.3   RCG

The RAS/CAS generator (RCG) is packaged in a 324-pin BGA package. It drives the RAS, CAS address and Write Enable signals to the DRAM array. One RCG component is located on each memory module. The RCG dissipates 2 W and does not need a heat sink.

1.4.2.4   MUX

The data path multiplexor (MUX) component is packaged in a 324-pin BGA package. It drives and receives the data to and from the DRAM array. Two MUX components are located on each memory module. The MUX dissipates 2.5 W and does not need a heat sink.

1.4.3   PID

The programmable interrupt device (PID) is an Enterprise Server Group/Intel® ASIC designed specifically for the Ak450NX board set. The PID provides interrupt steering functions (including support logic for use with the 8259A interrupt controllers in the PIIX4E) and I/O APIC facilities. In addition to the standard IRQs, the PID supports a large number of PCI and onboard interrupt sources; a total of 64 interrupt routing table entries are available. A separate interrupt input is provided for each of the four interrupts from every 64-bit PCI slot on the I/O baseboard. Separate INTA and INTB connections are provided from every 32-bit PCI slot, but INTC and INTD are bused (in a rotating pattern) from the slots on the 32-bit PCI segments; separate bused connections are provided for each 32-bit PCI segment. The PID is packaged in a 256-pin BGA package.

1.5   Performance

The core of the Ak450NX board set is the Pentium II Xeon processor and the Intel 450NX PCIset. Table 1-1 shows the capabilities of each of the major buses on Ak450NX. The values shown are peak bandwidth capable on the bus. Actual sustained bandwidth will be lower and will vary with the configuration of the server (i.e., adapter cards, operating system, etc.) and the application(s) being run.

Table 1-1:   Peak Bus Bandwidth

Bus	Frequency	Bus Width	Peak Band Width	Signaling Technology
Processor	100 MHz	72-bits	800 MB/s	AGTL+
Memory[1]	100 MHz	72-bits	1.067 MB/s[2]	AGTL+
F16 (each) [1]	100 MHz	16-bits	400 MB/s	AGTL+
PCI-64	33 MHz	64-bits	266 MB/s	TTL/LV-TTL
PCI-32 (each)	33 MHz	32-bits	133 MB/s	TTL/LV-TTL

Notes: 1. Bus drives data on both edges of the clock.

       2. 1.067 GB/s bandwidth is with two memory modules installed and populated with at least 8 DIMMs in each module. Maximum bandwidth with only one memory module populated is 800 MB/s.

2. Board Set Details

2.1 PCI Hot-plug (PHP) I/O Baseboard

This section describes the architecture of the Ak450NX PCI hot-plug (PHP) I/O baseboard. The PHP I/O baseboard interfaces with the CPU baseboard through the midplane board. The I/O baseboard contains all primary I/O interfaces for the Ak450NX board set.

Features

The I/O baseboard has the following features:

- Three functionally independent PCI buses
- Integrated 53C896* dual channel LVDS controller
- Integrated IDE controller supporting one IDE bus
- Onboard video, serial, parallel, universal serial bus (USB)
- Five 32-bit PCI slots (non-hot-plug)
- Four hot-plug 64-bit PCI slots
- One shared ISA/32-bit PCI slot (non-hot-plug)
- Intelligent Platform Management Bus (IPMB) server management interface

2.1.1   Block Diagram

Figure 2-1 illustrates the general architecture of the PHP Ak450NX I/O baseboard.
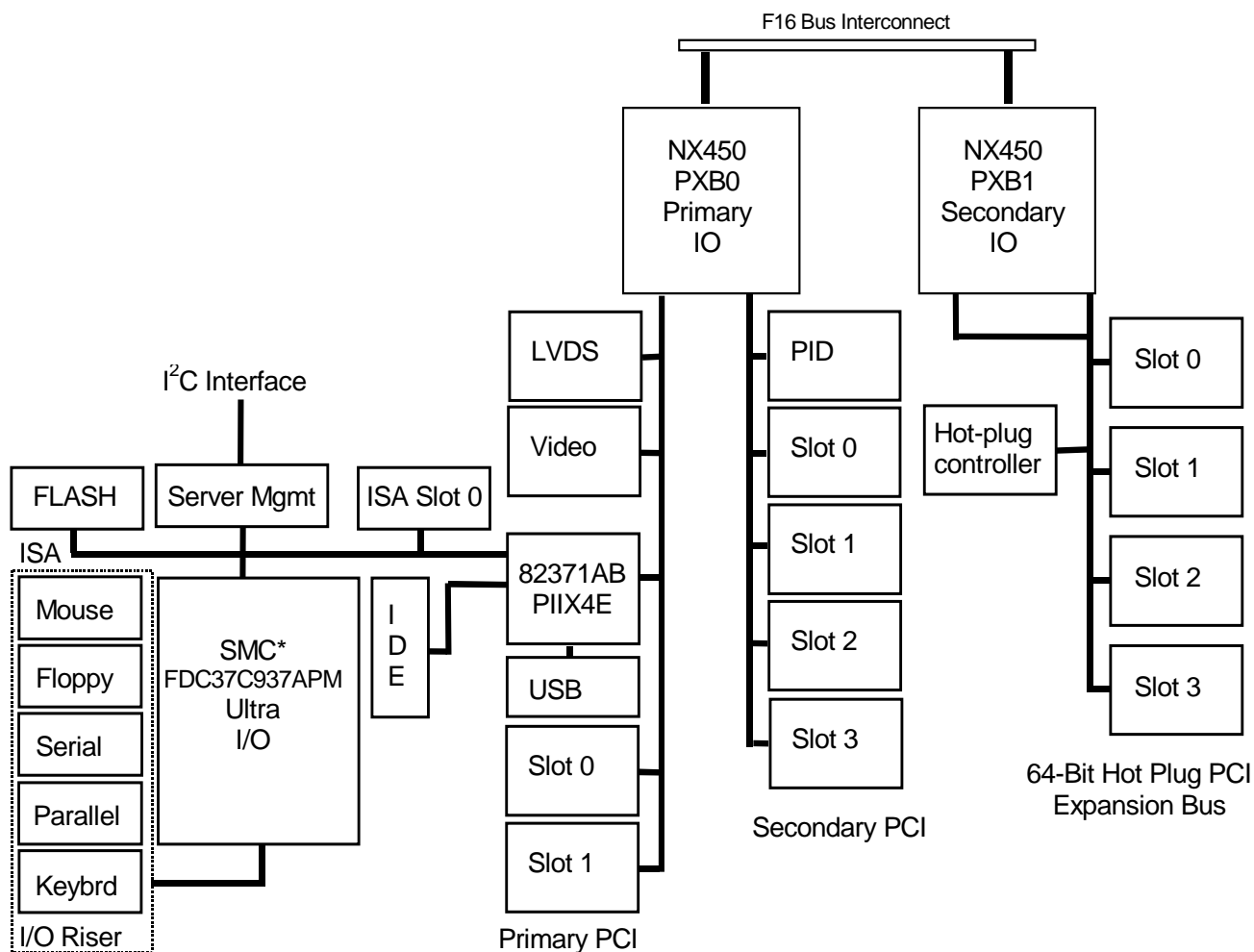
Figure 2-1: I/O Baseboard Block Diagram

2.1.1.1   I/O Riser Card

In order to conserve space on the I/O baseboard, many legacy connections have been moved to a riser card attached to the baseboard. Connections to video, keyboard, mouse, COM ports, parallel port, and ICMB interface are all provided through the I/O riser card. The I/O riser card is the same as the one found in the A450NX board set. Note that the USB connection is located directly on the I/O baseboard.

2.1.2   Placement Diagrams

The diagrams below were generated from the actual layout database and show the primary components of the I/O baseboard and I/O riser card, and the components' positions on the printed circuit board. The table following each diagram identifies the major components using the reference designators to locate the item in the plot.
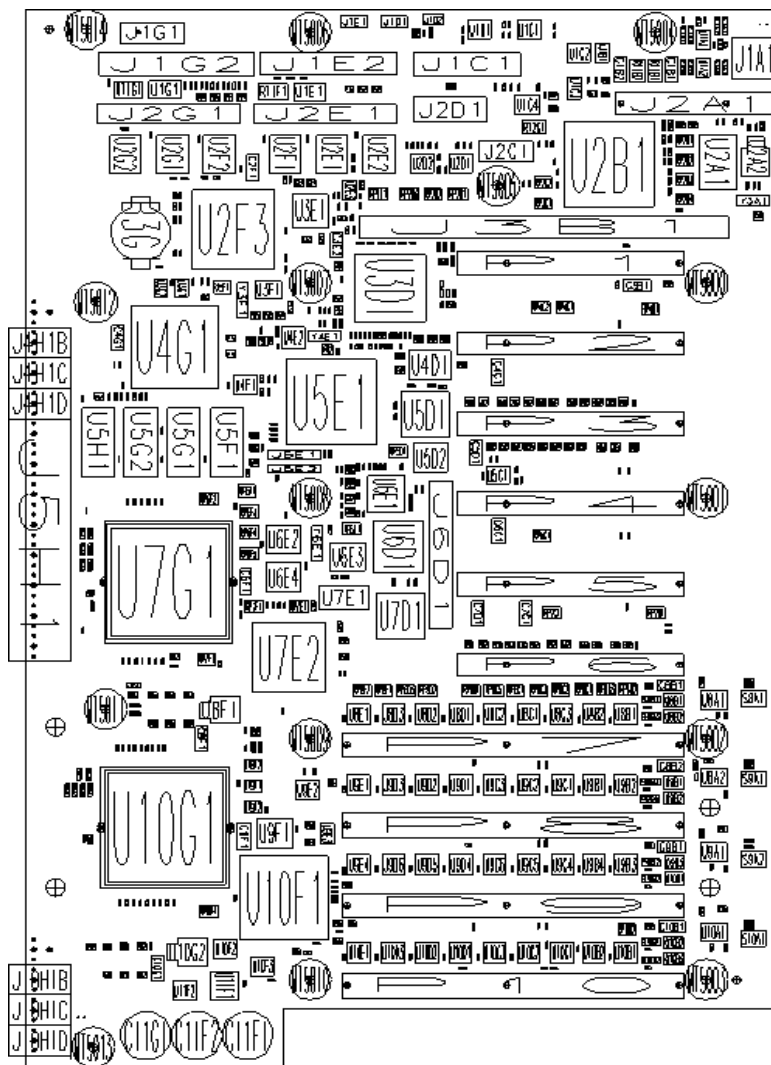
Figure 2-2: I/O Baseboard Placement Plot

Table 2-1:   Major Component Reference (I/O Baseboard)

Reference Designator	Name and Description
J1A1	USB connector
J3B1	ISA connector
J2A1	I/O riser card connector
P1–P2	Primary 32-bit PCI slots
P3–P6	Secondary 32-bit PCI slots
P7–P10	64-bit PCI slots (hot plug)
J3D1	In-system programming. (Used to program the SMIC and PCI error programmable array logic (PAL). Used by Intel for test purposes only. Will be removed on future board revisions.)
J1G2	IDE connector: primary channel
J1E2	Floppy disk drive connector
J2F1	Server management feature connector
J2G1,J2E1	SCSI connector (for peripheral devices)
J2H1–J2H2	Auxiliary I^2C connectors
J3H1	Configuration jumper block (see *Section 2.1.3.6*)
J7G2	In-system programming connector. (Used to program the BMC control PAL. Used by Intel for test purposes only. Will be removed on future board revisions.)
U2A1	2 MB BIOS flash device
U5F1,U5G1 U5G2,U5G3	2 MB video DRAM
U4G1	Cirrus Logic* GD5446 VGA controller
U2G3	Symbios* 53C896 LVDS
U2B1	SMC* Ultra I/O component
U3D1	PIIX4E, PCI to ISA bridge device
U5E1	Server management interface controller (SMIC)
U4F1	Baseboard management controller (BMC)
U5F2	Flash to hold the BMC code. 32Kx8 (or 64Kx8)
U4F4	32Kx8 RAM for BMC
U7E1	PID
U7G1	PXB-0 (PCI bus expander for the 32-bit PCI buses)
U10G1	PXB-1 (PCI bus expander for the 64-bit PCI bus)
U10E1	Hot-plug controller for 64-bit PCI card
B5000	Battery
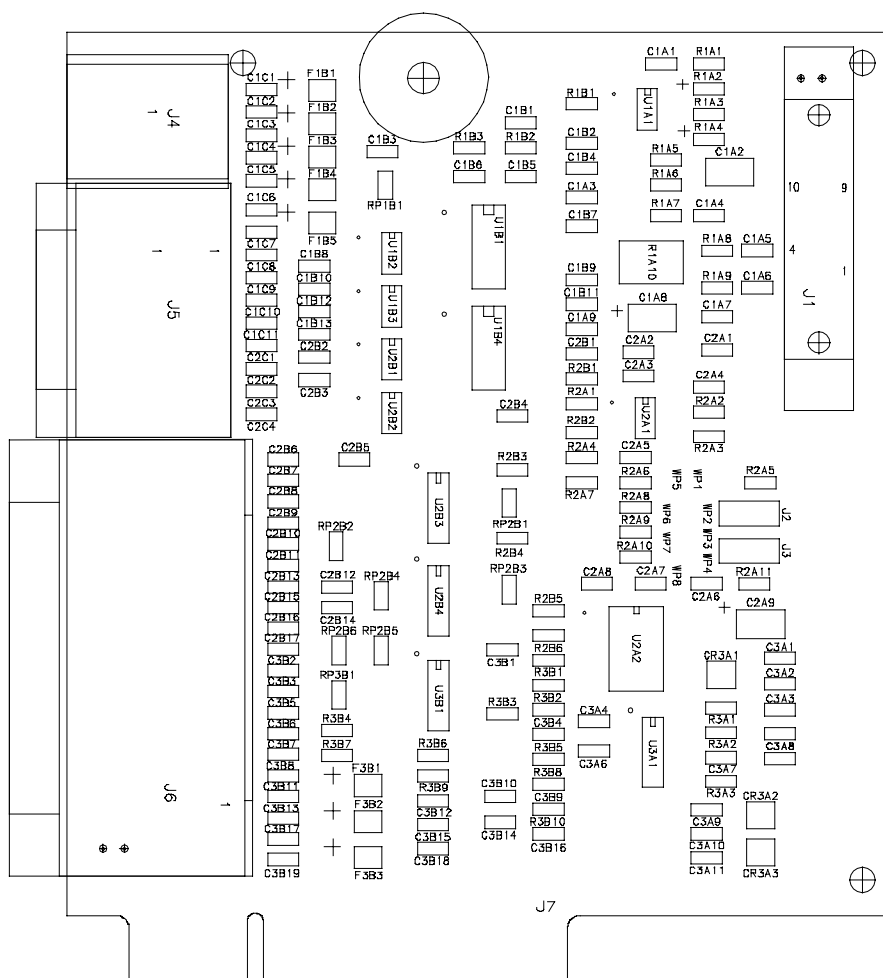
Figure 2-3: I/O Riser Card Placement Plot

Table 2-2: Major Component Reference (I/O Riser Card)

Reference Designator	Name and Description
J1	ICMB connector
J4	Combined mouse and serial connector
J5	COM 1 and COM 2 serial port connectors
J6	Combined parallel and video connector
J7	Edge connector. Plugs into connector J3 on the I/O baseboard

2.1.3   Architectural Overview

- F16 bus interface
- Primary 32-bit PCI bus
- Secondary 32-bit PCI bus
- 64-bit PCI hot-plug bus
- System management logic

The following subsections briefly describe each block.

2.1.3.1   F16 Bus Interface

The F16 bus, a proprietary, fast, 16-bit bus, connects each of the two PXBs on the Ak450NX I/O baseboard with the MIOC located on the CPU baseboard. Operating at 100 MHz, and transferring data on both the rising and falling clock edges, each F16 bus is capable of transfers at a peak data rate of 400 MB/s. The Ak450NX I/O baseboard implements two F16 bus interfaces, one to communicate to each of the 82450NX PCI bridges (PXBs).

The expander bus is bidirectional, synchronous, and uses a full split transaction protocol. Each transaction consists of a request and completion phase. To guarantee high bus efficiency, the expander bus protocol is a No Wait State protocol. The bus also is parity checked to provide superior data reliability.

2.1.3.2   Intel® 82450NX PCI Bridge (PXB)

Two PXB components reside on the I/O baseboard. Each PXB supports 5 V, 33 MHz, *PCI Spec., Rev. 2.1* compliant interfaces. One of the components is configured to drive two 32-bit PCI buses, while a second PXB component is configured to support a single, dedicated, 64-bit PCI interface.

The PCI buses are operated synchronously with the processor bus, using the processor bus clock as a master clock. The input clock, received over the F16 bus interface, is divided by three to support the 33-MHz PCI bus.

The PXB supports all transactions defined for the *PCI Spec., Rev. 2.1* bus, except that cache coherency is not supported, either between PCI devices or between the PCI and processor buses.

2.1.3.3   Primary 32-bit PCI Bus

Conforming to *PCI Spec., Rev. 2.1,* the primary 32-bit PCI bus is configured on the baseboard with the necessary devices to boot the operating system.

The Intel® 82371AB PIIX4E component provides the bridge for interconnect to ISA devices, as well as the USB interface. The boot flash ROM is directly connected to the ISA bus and is under the control of the PIIX4E.

A Symbios 53C896* LVDS controller provides a 16-bit, high speed, low voltage differential SCSI (LVDS) interface for mass storage and/or peripheral devices (CD-ROMs, tape drives, etc.). This high performance adapter is capable of providing data rates of up to 80 MB/s in 16-bit LVDS operation to ensure maximum data throughput while minimizing PCI bus overhead.

Onboard video is supplied by a Cirrus Logic GD5446* PCI video controller with 2 MB of onboard video DRAM. The CL-GD5446 VisualMedia accelerator is a 64-bit DRAM based SVGA controller with hardware-accelerated bitblt, video playback, and video capture to the frame buffer. It combines the Cirrus Logic V-Port* with a multiformat frame buffer for cost effective video playback. The onboard video also features a 64-bit GUI BitBLT engine with double-buffered, memory-mapped control registers.

The primary 32-bit PCI bus also provides two, full length, 32-bit expansion slots (identified as P1 and P2). One slot is shared with the ISA expansion slot.

Further details of the primary components connected to the primary 32-bit PCI bus are provided in the following sections.

2.1.3.3.1   Symbios 53C896* SCSI Controller

A single Symbios 53C896 LVDS controller provides embedded SCSI on the primary 32-bit PCI bus. The 53C896 supports two LVDS channels. Use of these SCSI I/O channels is defined by the peripheral device support provided by the system chassis. For example, one channel might be used for control of boot drives and/or other peripheral

devices (CD-ROM, tape backup, etc.), whereas the second channel might be used for connection to an external disk array.

The configuration registers define PCI-related parameters for the 53C896 device. The 53C896 supports all mandatory registers in the PCI configuration space header, including the vendor ID, device ID, class code, revision ID, header type, and command and status fields. Refer to the 53C896 datasheets for details.

2.1.3.3.2   Cirrus Logic GD5446* PCI Video Controller

The Cirrus Logic GD5446 PCI video controller is connected to the primary 32-bit PCI bus and is used to provide onboard VGA capability to the I/O baseboard. The CL-GD5446 includes a glueless 32-bit PCI bus interface. This interface features full PCI compliance, including optimized PCI burst write, which supports PCI writes to the frame buffer at greater than 55 MB/s.

The frame buffer is addressable through a 16-MB window consisting of three 4-MB byte-swapping apertures, and a special video aperture. The VGA control registers are relocatable anywhere in the 64KB space (allowing multiple devices in a single system).

Complete information for this device can be found in the vendor's data manual.

When external PCI video adapters are added, they should be added to the primary 32-bit PCI bus. The GD5446 is automatically disabled by BIOS if a video adapter is detected in any to the expansion slots on the primary 32-bit PCI bus.

2.1.3.3.3   Video Modes

The CL-GD5446 provides all standard IBM* VGA modes. Table 2-3 and Table 2-4 show all supported video modes.

Table 2-3:   Standard VGA Modes

Mode(s) in Hex	Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	16/256K	40 x 25	9 x 16	360 X 400	Text	14	31.5	70
2, 3	16/256K	80 x 25	9 x 16	720 X 400	Text	28	31.5	70
4, 5	4/256K	40 x 25	8 x 8	320 X 200	Graphics	12.5	31.5	70
6	2/256K	80 x 25	8 x 8	640 X 200	Graphics	25	31.5	70
7	Mono	80 x 25	9 x 16	720 X 400	Text	28	31.5	70
D	16/256K	40 x 25	8 x 8	320 X 200	Graphics	12.5	31.5	70
E	16/256K	80 x 25	8 x 14	640 X 200	Graphics	25	31.5	70
F	Mono	80 x 25	8 x 14	640 X 350	Graphics	25	31.5	70
10	16/256K	80 x 25	8 x 14	640 X 350	Graphics	25	31.5	70
11	2/256K	80 x 30	8 x 16	640 X 480	Graphics	25	31.5	60
11+	2/256K	80 x 30	8 x 16	640 X 480	Graphics	31.5	37.9	72
11+	2/256K	80 x 30	8 x 16	640 X 480	Graphics	31.5	37.5	75
12	16/256K	80 x 30	8 x 16	640 X 480	Graphics	25	31.5	60
12+	16/256K	80 x 30	8 x 16	640 X 480	Graphics	31.5	37.9	72
12+	16/256K	80 x 30	8 x 16	640 X 480	Graphics	31.5	37.5	75
12+	16/256K	80 x 30	8 x 16	640 X 480	Graphics	35.8	43.3	85
13	256/256K	40 x 25	8 x 8	320 X 200	Graphics	12.5	31.5	70

Table 2-4:   Extended VGA Modes

Mode(s) in Hex	Colors	Char. x Row	Char. Cell	Screen Format	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
58, 6A	16/256K	100 x 37		800 X 600	36	35.2	56
58, 6A	16/256K	100 x 37		800 X 600	40	37.8	60
58, 6A	16/256K	100 x 37		800 X 600	50	48.1	72
58, 6A	16/256K	100 x 37		800 X 600	49.5	46.9	75
5C	256/256K	100 x 37		800 X 600	36	35.2	56
5C	256/256K	100 x 37		800 X 600	40	37.9	60
5C	256/256K	100 x 37		800 X 600	50	48.1	72
5C	256/256K	100 x 37		800 X 600	49.5	46.9	75
5C	256/256K	100 x 37		800 X 600	56.25	53.7	85
5D[†]	16/256K	128 x 48		1024 X 768	44.9	35.5	43
5D	16/256K	128 x 48		1024 X 768	65	48.3	60
5D	16/256K	128 x 48		1024 X 768	75	56	70
5D[†]	16/256K	128 x 48		1024 X 768	77	58	72
5D	16/256K	128 x 48		1024 X 768	78.5	60	75
5E	256K/256K	80 x 25		640 X 400	25	31.5	70
5F	256/256K	80 x 30		640 X 480	25	31.5	60
5F	256/256K	80 x 30		640 X 480	31.5	37.9	72
5F	256/256K	80 x 30		640 X 480	31.5	37.5	75
5F	256/256K	80 x 30		640 X 480	36	43.3	85
65	64K	-	-	800 X 600	36	35.2	56
65	64K	-	-	800 X 600	40	37.8	60
65	64K	-	-	800 X 600	50	48.1	72
65	64K	-	-	800 X 600	49.5	46.9	75
65	64K	-	-	800 X 600	56.25	53.7	85
66	32K[‡]	-	-	640 X 480	25	31.5	60
66	32K[‡]	-	-	640 X 480	31.5	37.9	72
66	32K[‡]	-	-	640 X 480	31.5	37.5	75
66	32K[‡]	-	-	640 X 480	36	43.3	85
67	32K[‡]	-	-	800 X 600	36	35.2	56
67	32K[‡]	-	-	800 X 600	40	37.8	60
67	32K[‡]	-	-	800 X 600	50	48.1	72
67	32K[‡]	-	-	800 X 600	49.5	46.9	75
67	32K[‡]	-	-	800 X 600	56.25	53.7	85
68	32K[‡]	-	-	1024 X 768	44.9	35.5	43
68	32K[‡]	-	-	1024 X 768	65	48.3	60
68	32K[‡]	-	-	1024 X 768	75	56	70
68	32K[‡]	-	-	1024 X 768	78.7	60	75
68	32K[‡]	-	-	1024 X 768	94.5	68.3	85
69[†]	32K[‡]	-	-	1280 X 1024	75	48	43
69[†]	32K[‡]	-	-	1280 X 1024	108	65	60
6C[†]	16/256K	160 x 64	8 x 16	1280 X 1024	75	48	43
6D[†]	256/256K	160 x 64	8 x 16	1280 X 1024	75	48	43
6D	256/256K	160 x 64	8 x 16	1280 X 1024	108	65	60
6D	256/256K	160 x 64	8 x 16	1280 X 1024	126	76	71.2
6D	256/256K	160 x 64	8 x 16	1280 X 1024	135	80	75
71	16M	-	-	640 X 480	25	31.5	60
71	16M	-	-	640 X 480	31.5	37.9	72

Mode(s) in Hex	Colors	Char. x Row	Char. Cell	Screen Format	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
71	16M	-	-	640 X 480	31.5	37.5	75
71	16M	-	-	640 X 480	36	43.3	85
74[†]	64K[†]	-	-	1024 X 768	44.9	35.5	43
74	64K	-	-	1024 X 768	65	48.3	60
74	64K	-	-	1024 X 768	75	56	70
74	64K	-	-	1024 X 768	78.7	60	75
74	64K	-	-	1024 X 768	94.5	68.3	85
75[†]	64K[†]	-	-	1280 X 1024	75	48	43
78	16M	-	-	800 X 600	36	35.2	56
78	16M	-	-	800 X 600	40	37.8	60
78	16M	-	-	800 X 600	50	48.1	72
78	16M	-	-	800 X 600	49.5	46.9	75
78	16M	-	-	800 X 600	56.25	53.7	85
79	16M	-	-	800 X 600	44.9	35.5	43
79	16M	-	-	1024 X 768	65	483	60
79	16M	-	-	1024 X 768	75	56	70
79	16M	-	-	1024 X 768	78.7	60	75
79	16M	-	-	1024 X 768	94.5	68.3	85
7C	256K/256K	144 x 54	8 x 16	1152 X 864	94.5	63.9	70
7C	256K/256K	144 x 54	8 x 16	1152 X 864	108	67.5	75
7D	64K	-	-	1152 X 864	94.5	63.9	70
7D	64K	-	-	1152 X 864	94.5	67.5	75

[†] Indicates interlaced mode
[‡] Indicates 32KB direct-color/256-color mixed mode

2.1.3.3.4   Expansion Slots

Two standard 32-bit PCI expansion slots are user accessible on the primary PCI bus. These slots compete for access to the bus along with the other components mounted to the bus.

2.1.3.3.5   Intel® 82371AB PCI to ISA/IDE Accelerator

The Intel 82371AB PIIX4E component provides the bridge for interconnecting to ISA, two IDE channels, and the USB interface.

2.1.3.3.6   ISA Bus

The ISA bus provides a single ISA slot, which is physically shared with the first PCI slot on the primary 32-bit PCI bus (P1). The BIOS flash device, SMC* Ultra I/O controller and the SMIC are also located on the ISA bus.

2.1.3.3.6.1   SMC FDC37C937APM* Ultra I/O Controller

The FDC37C935APM incorporates the following features:

- keyboard interface
- real-time clock
- SMC's true CMOS 765B* floppy disk controller
- advanced digital data separator
- 16-byte data FIFO
- two 16C550* compatible UARTs
- one Multimode* parallel port, which includes ChiProtect* circuitry plus enhanced parallel port (EPP) and extended capabilities port (ECP) support

- on-chip 24 mA AT bus drivers
- game port chip select
- two-floppy direct drive support
- ACCESS bus
- soft power management and system management interrupt (SMI) support

The true CMOS 765B core provides 100% compatibility with both the IBM* PC/XT and PC/AT architecture in addition to providing data overflow and underflow protection. The SMC advanced digital data separator incorporates SMC's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with the NS16C550*. The parallel port, the IDE interface, and the game port select logic are compatible with IBM PC/AT architecture, as well as EPP and ECP. The FDC37C937APM incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C937APM provides features for compliance with the advanced configuration and power interface (ACPI). These features include support of both legacy and ACPI power management models through the selection of SMI or SCI. It implements a 24-bit power management timer, power button override event (4 second button hold to turn off the system) and either edge triggered interrupts.

The FDC37C937APM provides support for the *Plug-and-Play ISA Standard Version 1.0a*. The FDC37C937APM has multiple logical devices, each of which has an I/O address, a DMA and an IRQ setting that may be programmed through internal configuration registers. There are 480 I/O address location options, 13 IRQ options, and three DMA channel options for each logical device. The FDC37C937PM does not require any external filter components and is, therefore, easy to use and offers lower system cost and reduced board area. The FDC37C937APM is software and register compatible with SMC's proprietary 82077AA* core.

2.1.3.3.6.2   BIOS Flash Device

The onboard BIOS is located in an onboard 2 MB flash device attached directly to the ISA bus. The device is enabled under the control of the PIIX4E. The device is accessed in byte wide mode. The BIOS can be updated by means of an update utility at boot time by inserting a bootable floppy into the drive that contains the updated BIOS image as well as the update utility software. The BIOS contains a recovery boot option, by positioning jumper J30 to cover pins 2 and 4. See *Section 2.1.3.6* of this chapter for more details. This jumper configuration forces the BIOS to update without user intervention. A series of beeps indicates the beginning and end of the programming process.

2.1.3.4   Secondary 32-Bit PCI Bus

The secondary 32-bit PCI bus is also *PCI Spec., Rev. 2.1*, compliant. The programmable interrupt device (PID), an Intel designed ASIC, resides on the secondary 32-bit PCI bus for system interrupt handling. The PID is an interrupt controller that provides the interrupt steering. The PID contains the logic required to provide 8259A mode, advanced programmable interrupt controller (APIC) mode, and ACPI functionality. The PID includes a PCI, APIC, and PIIX4E interface. The secondary 32-bit PCI bus also contains four, full length, 32-bit user accessible expansion slots (identified as P3, P4, P5 and P6).

Further details of the components connected to the secondary 32-bit bus are provided in the following sections.

Note: Due to architectural limitations of the 450NX PCIset, all expansion video cards must be placed on the primary 32-bit PCI bus.

2.1.3.4.1   Programmable Interrupt Device

The I/O baseboard incorporates an ASIC referred to as the programmable interrupt device, or PID. The PID is an Intel designed interrupt controller ASIC that provides interrupt steering functions including ISA 8259A, and I/O APIC mode controller operations. The PID provides up to 15 IRQs and 48 PCI interrupt inputs.

The PID contains logic that is used to direct system critical error interrupts to the SMI and NMI signals to the processors. The following critical interrupts can be routed to SMI:

- PIIX NMIs (these include ISA parity, IOCHK, and Port 92h software NMIs)
- PCI SERR and PERR
- Correctable ECC errors
- Uncorrectable ECC errors
- PIIX SMI

So that fatal NMIs can be produced even when the SMI handler is disabled, the PID allows the following to generate an NMI via an SMI-to-NMI mapping option:

- PCI SERR and PERR
- Uncorrectable ECC errors
- BMC SMI

The SMI handler has an option to generate a fatal NMI after it has logged an event, whereupon the operating system (OS) will typically execute an NMI handler that will display an error status and halt the system. This is an appropriate action to avoid continuing OS operation with a potential unlocated data corruption.

To minimize the possibility of interrupt conflicts, especially with increased use of multiported adapter cards, the PID provides at least two dedicated interrupts per 32-bit PCI slot and four dedicated interrupts per 64-bit PCI slot. Table 2-5 summarizes the interrupt mappings.

Table 2-5:   Interrupt Mappings

PID Interrupt	PCI Interrupt	Component/PCI Slot Number	PCI Bus
0	Not Used	---	---
1	Not Used	---	---
2	B	Onboard SCSI B	Primary PCI-32
3	---	PHP Controller	PCI-64 (PHP)
4	A	P7	PCI-64 (PHP)
5	B	P7	PCI-64 (PHP)
6	C	P7	PCI-64 (PHP)
7	D	P7	PCI-64 (PHP)
8	A	P8	PCI-64 (PHP)
9	B	P8	PCI-64 (PHP)
10	C	P8	PCI-64 (PHP)
11	D	P8	PCI-64 (PHP)
12	A	P9	PCI-64 (PHP)
13	B	P9	PCI-64 (PHP)
14	C	P9	PCI-64 (PHP)
15	D	P9	PCI-64 (PHP)
16	A	P10	PCI-64 (PHP)
17	B	P10	PCI-64 (PHP)
18	C	P10	PCI-64 (PHP)
19	D	P10	PCI-64 (PHP)
20	A	PXB-1	PCI-64 (PHP)
21	B	P3	Secondary PCI-32
22	A	P3	Secondary PCI-32

PID Interrupt	PCI Interrupt	Component/PCI Slot Number	PCI Bus
23	B	P4	Secondary PCI-32
24	A	P4	Secondary PCI-32
25	B	P5	Secondary PCI-32
26	A	P5	Secondary PCI-32
27	B	P6	Secondary PCI-32
28	A	P6	Secondary PCI-32
29	C/D/C/D	P3/P4/P5/P6[†]	Secondary PCI-32
30	D/C/D/C	P3/P4/P5/P6[†]	Secondary PCI-32
31	Not Used	---	---
32	A	Video	Primary PCI-32
33	D	PIIX4E	Primary PCI-32
34	---	PXB-0	Secondary PCI-32
35	---	PXB-0	Primary PCI-32
36	D/C	P1/P2[†]	Primary PCI-32
37	C/D	P1/P2[†]	Primary PCI-32
38	B	P1	Primary PCI-32
39	A	P1	Primary PCI-32
40	B	P2	Primary PCI-32
41	A	P2	Primary PCI-32
42	A	Onboard SCSI A	Primary PCI-32
43	Not Used	---	---
44	---	MIOC	---
45	Not Used	---	---
46	NMI	PIIX4E	---
47	Not Used	---	---

[†] Shared interrupt

2.1.3.5   64-Bit PCI Bus

The 64-bit PCI bus provides the user with four full length, *PCI Spec., Rev. 2.1* compliant hot-plug expansion slots on a dedicated high performance bus.

Notes: 1. Both 32-bit and 64-bit PCI adapters may be plugged into the 64-bit slots. The 32-bit adapters, however, will not take advantage of the extra bandwidth provided by the 64-bit bus.

2. Due to architectural limitations of the 450NX PCIset, all expansion video cards must be placed on the primary 32-bit PCI bus.

2.1.3.5.1   PCI Hot-plug Controller

The PCI hot-plug controller is connected on the 64-bit PCI bus and is used to provide the ability for software to connect or disconnect any of the four 64 bit PCI slots from the 64-bit PCI bus. This enables add-in cards to be installed or removed safely without removing power from the server. The PCI hot-plug controller includes a glueless PCI bus interface to the 64-bit PCI bus. The controller enables/disables bus switches which connect/disconnect the entire 64-bit PCI bus to/from each 64-bit PCI slot. The controller also enables/disables clock buffers and the PCI hot-plug voltage controller, which switches on and off the +3.3 V, +5 V,+12 V and –12 V to each 64-bit PCI slot.

For each PCI slot, there is a yellow status LED controlled by OS level software which can be illuminated to designate a failed adapter/slot. There is also a green power LED controlled by both the PCI hot-plug controller and

OS level software, which tells the user whether or not power is applied to the PCI card. If this LED is illuminated, the card cannot be removed from the slot.

2.1.3.6   Board Configuration Jumpers

Configuration jumpers exist on the I/O baseboard to enable the user to recover a BIOS, clear a CMOS password, or clear all CMOS settings. Positioning of the jumpers as shown in Figure 2-4 provides the default system configuration. Reserved jumpers may not be populated in shipping configurations. Minimum configuration default configurations are identified in Table 2-6. The configuration jumper block is located near PXB-0 and in line with the 32-bit PCI slots (P3 and P4).

J2C1   A   B   C

1   Update Server Mgmt
2   Recovery Boot
3   Reserved
4   BIOS update
5   CMOS Clear
6   Password Clear
7   PHP switch override
8   Enable ISP chain
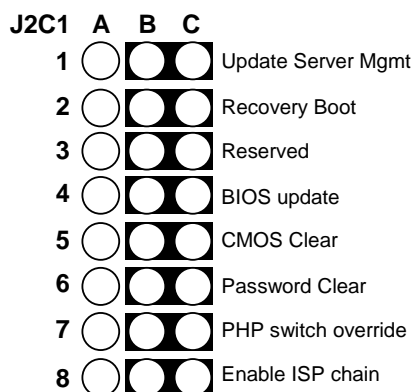
Figure 2-4: Configuration Jumpers

Table 2-6:   Board Configuration Jumpers

Jumper	Function
1(B–C)	Permits server management to program onboard programmable devices (baseboard management controller (BMC), front panel controller (FPC), hot-swap controller (HSC)).
1(A–B)	Do not allow server management to program onboard programmable devices.[†]
2(B–C)	Normal boot.[†]
2(A–B)	Recovery boot.
3(B–C)	Reserved.[†]
3(A–B)	Reserved.
4(B–C)	Allow BIOS flash update.[†]
4(A–B)	No BIOS flash update.
5(B–C)	Do not clear CMOS.[†]
5(A–B)	Clear CMOS.
6(B–C)	Do not clear CMOS password.[†]
6(A–B)	Clear CMOS password.
7(B–C)	Normal operation.[†]
7(A–B)	Override power-disable switch.
8(B–C)	Reserved.[†]
8(A–B)	I/O serial peripheral interface (SPI) chain enable (enable programming of onboard parts).

[†] Indicates the default jumper position.

2.1.3.7 Boot Order

The I/O baseboard provides the system with a variety of methods for detecting and booting an operating system. The BIOS scans devices and user configurable option slots in a specific sequence. Knowing the precise sequence in which the BIOS will detect, setup, and boot, will greatly assist in system definition. The default boot order is listed below although there are many factors, including user changes to the BIOS setup, which may affect the actual boot order of a particular configuration. The exact IDSEL numbers are shown in Table 2-7 to help in determining the actual boot order.

Default Boot Order
- Floppy
- ISA
- IDE (primary)
- Primary 32-bit PCI bus
  - P1. PCI connector 1 (P1)
  - Onboard LVDS (primary)
  - Onboard LVDS (secondary)
  - P2. PCI connector 2 (P2)
- Secondary 32-bit PCI bus
  - P3. PCI connector 3 (P3)
  - P4. PCI connector 4 (P4)
  - P5. PCI connector 5 (P5)
  - P6. PCI connector 6 (P6)
- 64-bit PCI bus
  - P7. PCI connector 7 (P7)
  - P8. PCI connector 8 (P8)
  - P9. PCI connector 9 (P9)
  - P10. PCI connector 10 (P10)

Table 2-7:   Device Configuration Order

Location	Bus	IDSEL	Comment
J1E2	ISA	None	Floppy Drive
J3B1	ISA	None	Compatability (Legacy) Boot Slot 1 (1)
J1G2	IDE	None	Primary IDE
P1	Primary PCI	25	Expansion Slot (Note 1)
J2G1	Primary PCI	26	Onboard SCSI
P2	Primary PCI	27	Expansion Slot (Note 1)
U4G1	Primary PCI	28	Onboard Video
U3D1	Primary PCI	31	PIIX4E Component
P3	Secondary PCI	20	Expansion Slot
P4	Secondary PCI	21	Expansion Slot
P5	Secondary PCI	22	Expansion Slot
P6	Secondary PCI	23	Expansion Slot
U7E2	Secondary PCI	25	PID Component
P7	64 Bit PCI	20	Expansion Slot
P8	64 Bit PCI	21	Expansion Slot
P9	64 Bit PCI	22	Expansion Slot
P10	64 Bit PCI	23	Expansion Slot

Note: User supplied video adapters may be installed only in slots P1 or P2.

2.1.3.8 Server Management

The heart of server management is the BMC. External communication can be established with the BMC through the SMIC. The server management logic maintains a system event log (SEL) to store server management event

messages. The server management logic also provides monitoring and/or control of system devices including power status, chassis fan status/speed, security, and other system status information. For more information on server management implementation on the Ak450NX board set, see *Chapter 4 Server Management Implementation* of this document.

2.1.3.8.1   Memory Map

This section contains a server management device map and an I/O memory map.

Table 2-8:   Server Management Device Maps

Function	Address Range	Access	Width
I/O board A/D[†] converter	SPI Bus		
CPU board A/D converter	SPI Bus		
SMIC	FC00 - FFFF	See SMIC section	Byte
Output Latch #1	F800 - FBFF	Write (Read RAM Shadow)	Byte
Output Latch #0	F400 - F7FF	Write (Read RAM Shadow)	Byte
RAM, Output Latch Shadow	F400 - FBFF	Execute, Read, Write (Shadows Output Latches)	Byte
Input Latch	F000 - F3FF	Read	Byte
RAM # 1	Not assigned	Not defined	Byte
RAM # 0	8000 - EFFF	Execute, Read, Write	Byte
FLASH, OPS	1000 - 7FFF	Execute, Read, Write	Byte
FLASH, BOOT	0000 - 1000	Execute, Read	Byte

[†] analog to digital

Table 2-9:   Server Management

Topic	Signal	Device	Access	Offset	Bit
Not Applicable	Not Applicable	Micro Port 0	-	-	0 to 7
	(Muxed Address/Data BUS)				
SPI Bus	SPI_CLK - Bit 0	Micro Port 1	RW	-	0
SPI Bus	SPI_MISO - Bit 6	Micro Port 1	RW	-	1
SPI Bus	SPI_MOSI - Bit 5	Micro Port 1	RW	-	2
SPI Bus	SPI_SEL_2_L -Bit 3	Micro Port 1	RW	-	3
SPI Bus	SPI_SEL_3_L - Bit 4	Micro Port 1	RW	-	4
Memory	BMC_OP_CLR_L	Micro Port 1	RW	-	5
Global I^{2}C Bus	I2C_GLOBAL_SCL	Micro Port 1	RW	-	6
Global I^{2}C Bus	I2C_GLOBAL_SDA	Micro Port 1	RW	-	7
Not Applicable	Not Applicable	Micro Port 2	-	-	0–7
	(Upper Address Bus)				
BMC's Private I^{2}C Bus	I2C_BMC_SCL	Micro Port 3	-	-	0
BMC's Private I^{2}C Bus	I2C_BMC_SDA	Micro Port 3	-	-	1
Processor to BMC Interrupt	INTR0_SMIC_L	Micro Port 3	R	-	2
Secure Mode	SECURE_MODE_KB_L	Micro Port 3	R	-	3
BMC's Private I^{2}C Bus	I2C_BMC_SCL	Micro Port 3	RW	-	4
BMC's Private I^{2}C Bus	I2C_BMC_SDA	Micro Port 3	RW	-	5
BMC_RD_L	Reserved	Micro Port 3	-	-	6
BMC_WR_L	Reserved	Micro Port 3	-	-	7
Interrupts	FP_NMI_SWT_L	Input Latch	R	-	0
In Circuit Logic Programming	ISP_HSBP_SDO	Input Latch	R	-	1
Not Used	Not Used	Input Latch	R	-	2

Topic	Signal	Device	Access	Offset	Bit
In Circuit Logic Programming	ISP_FPC_SDO	Input Latch	R	-	3
Memory	BMC_FRC_UPDATE_L	Input Latch	R	-	4
Keylock	KEYLOCK_FROM_SFC_L	Input Latch	R	-	5
Bios Flash	FLASH_WP_L	Input Latch	R	-	6
Not Used	Not Used	Input Latch	R	-	7
Keylock	KEYLOCK_SFC_L	Output Latch # 0	RW	--	0
Fans	FAN_FAILED_L	Output Latch # 0	RW	-	1
Interrupts	PX4_EXTSMI_L	Output Latch # 0	RW	-	2
Secure Mode	SECURE_MODE_BMC	Output Latch # 0	RW	-	3
Floppy Drive	FD_READ_ONLY_L	Output Latch # 0	RW	-	4
Video	BLANK_VID	Output Latch # 0	RW	-	5
Interrupts	BMC_FP_NMI_L	Output Latch # 0	RW	-	6
Output Latches	LATCH_2_EN_L	Output Latch # 0	RW	-	7
In Circuit Logic Programming	ISP_SCLK	Output Latch # 1	RW	--	0
In Circuit Logic Programming	ISP_MODE	Output Latch # 1	RW	-	1
In Circuit Logic Programming	ISP_EN_L	Output Latch # 1	RW	-	2
In Circuit Logic Programming	ISP_EN2_L	Output Latch # 1	RW	-	3
In Circuit Logic Programming	ISP_IO_EN_L	Output Latch # 1	RW	-	4
In Circuit Logic Programming	ISP_FPC_EN_L	Output Latch # 1	RW	-	5
In Circuit Logic Programming	SPI_SEL_0	Output Latch # 1	RW	-	6
In Circuit Logic Programming	SPI_SEL_1	Output Latch # 1	RW	-	7
ISA to BMC Bridge	ISA_BMC_DATA_REG	PLD	-	0xFF01	7..0
ISA to BMC Bridge	ISA_BMC_CTRL_REG	PLD	-	0xFF02	7..0
ISA to BMC Bridge	ISA_BMC_FLAG_REG	PLD	-	0xFF03	7..0
Reset	PROC_RESET_NOW	PLD	R	0xFF04	7
Reset	PROC_RESET_HI_LO	PLD	RW	0xFF04	6
Reset	PROC_RESET_LO_HI	PLD	RW	0xFF04	5
Reset	PWR_GOOD_LAST_RESET	PLD	RW	0xFF04	4
Memory	BMC_A16_PAGE	PLD	RW	0xFF04	3
Reset	FW_FORCE_RST_LATCH	PLD		0xFF04	2
Reset	RESET_HSBP_L	PLD	RW	0xFF04	1
Reset/Interrupt	BMC_SERR_L	PLD	RW	0xFF04	0
Not Used	Not Used	PLD		0xFF05	7
Not Used	Not Used [Was; PWR_CNTRL_SFC_L]	PLD		0xFF05	6
Not Used	Not Used [Was: SFC_RST_L]	PLD	R	0xFF05	5
Not Used	Not Used [Was: FP_NMI_SWT_L]	PLD	R	0xFF05	4
Memory	FW_BOOT_BLOCK_PGM_EN (from jumper block)	PLD	R	0xFF05	3
Memory	FW_BOOT_BLOCK_PGM_EN_L (from processors)	PLD	R	0xFF05	2
Watchdog	SW_WATCHDOG_EN	PLD	R	0xFF05	1
Watchdog	WDO_307_L	PLD	R	0xFF05	0
Not Used	Not Used [REAL_TIME_CLOCK_SYNCH]	PLD	RW	0xFF06	7..0

2.1.3.8.2   System Event Log (Serial EEPROM)

The system event log is implemented with a 128KB serial EEPROM device, Atmel AT24C128W*. In addition to the SEL, the serial EEPROM is used to store the board FRU information and contains additional storage for chassis FRU information (must be programmed by the system integrator).

2.1.3.8.3   I^{2}C Accessed Features

The I/O baseboard and I/O riser card contain the following I^{2}C accessible devices, which contain FRU information:

- AT24C128*–I/O baseboard FRU information
- AT24C02*–256-byte SEEPROM containing I/O riser card FRU information

FRU information for both the I/O baseboard and I/O riser card are stored in SEEPROM devices located on each board. The devices are accessed via the BMC. The SEEPROM devices are accessible at the following addresses:

Table 2-10: I/O Baseboard and I/O Riser Card I^{2}C Address Map (FRU Data)

Device	Function	I^{2}C Address
AT24C128*	I/O baseboard FRU information	A6h,A7h
AT24C02*	I/O riser card FRU information	AEh,AFh

Both the AT24C128 and AT24C02 will provide board FRU information. The FRU information is read by server manager software such as the Intel® LANDesk® Server Manager and is available via the Intel® Server Console (ISC).

2.1.3.8.4   FRU Information

2.1.3.8.4.1   I/O Baseboard FRU Information

There are 256 bytes of the 128KB SEEPROM on the I/O baseboard dedicated to storage of FRU information. The 256 bytes of programmable space is broken into four areas. Table 2-11 lists the areas, a description, and the space allocated to each area.

Table 2-11: SEEPROM Programming Areas (I/O Baseboard)

Area	Size	Description
Common Header	8 Bytes	Programming offsets to the other areas below.
Internal Use	48 Bytes	This area is reserved for general purpose use by Intel®'s server management firmware/controllers.
Board Information	80 Bytes	Contains the board FRU information listed in Table 2-12.
Product Information	120 Bytes	Programmed as shown below when the I/O baseboard is installed into the AC450NX chassis. Otherwise this area is not programmed by Intel and is available for OEM use.†

† Documentation on this area is available in the *FRU and SDR Load Utility EPS*.

Table 2-12 list the board specific FRU information that will be programmed into the board information area.

Table 2-12: Board FRU Information (I/O Baseboard)

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. Date/Time	Time and date of board manufacture. Value programmed (in hex) is the number of minutes after 0:00 hrs. 1/1/96.	000f593h (Date/time translation shown below.) f593h = 62867min. Feb 12, 1996 3:47 p.m.	2
Manufacturer	Board Manufacturer	Intel	1
Board Product Name	Board Name/Description	Ak450NX I/O baseboard	1
Board Serial Number	Intel Board Serial Number	N42385906	2
Board Part Number	Intel Board Part Number	662379-001	2

Notes: 1. Actual value programmed into the board.
         2. Example value. Actual value will vary with each board and/or fab revision.

Table 2-13 lists the system specific FRU information that will be programmed into the system chassis information area. Note the following information is an example of how the area is programmed when used in the AC450NX server system. This area will be left blank if the I/O baseboard is purchased as a board level product.

Table 2-13: Product FRU Information (I/O Baseboard)

Product Information			
Information	**Description**	**Example**	**Notes**
Manufacturer Name	System Manufacturer Name	Intel	1
Product Name	System Name/Description	AC450NX Server System	1
Part Number/Model Number	Intel System Top Assembly Part Number	670305-101	1
Product Version	Not Used. 0 Bytes allocated.	---	1
Product Serial Number	Intel System Serial Number	N42385906	1
Asset Tag	Not used. 0 Bytes allocated.	---	1

Note: 1. Example as used in the AC450NX server system.

2.1.3.8.4.2   I/O Riser Card FRU Information

The AT24C02 SEEPROM has 256 bytes of programmable space, which is broken into four areas. Table 2-14 shows a list of the areas, a description, and the space allocated to each area.

Table 2-14: SEEPROM Programming Areas (I/O Riser Card)

Area	Size	Description
Common Header	8 Bytes	Programming offsets to the other areas below.
Internal Use	48 Bytes	This area is reserved for general purpose use by Intel server management firmware/controllers.
Board Information	80 Bytes	Contains the board FRU information listed in Table 2-15.
Product Information	120 Bytes	Available for OEM use[†]

[†] Documentation on how to program this area will be available at a later date.

Table 2-15 lists the board specific FRU information that will be programmed into the board information area.

Table 2-15: FRU Information (I/O Riser Card)

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. Date/Time	Time and date of board manufacture. Value programmed (in hex) is the number of minutes after 0:00 hrs. 1/1/96.	000f593h (Date/time translation shown below.) f593h = 62867 min. = 43 days and 947 min. = Feb 12, 1996, 3:47 p.m.)	2
Manufacturer	Board Manufacturer	Intel	1
Board Product Name	Board Name/Description	A450NX I/O Riser Card	1
Board Serial Number	Intel Board Serial Number	N42385906	2
Board Part Number	Intel Board Part Number	679267-001	2

Notes: 1.   Actual value programmed into the board.
            2.   Example value. Actual value will vary with each board and/or fab revision.

2.2   CPU Baseboard

This section describes the architecture of the Ak450NX CPU baseboard.   The CPU baseboard plugs into the 960-pin CPU board connector on the midplane. This board provides the main processor memory and I/O interfaces for the Ak450NX board set. It allows scalable installation of 1-4 Pentium II Xeon processors and provides a memory bus for a total memory capacity of up to 8 GB.

Features

The Ak450NX CPU baseboard provides the following features:

- Four Slot 2 connectors to accommodate 1-4 Intel® Pentium® II Xeon™ processors
- MIOC component of the 82450NX PCIset
- Interface buses to the Ak450NX I/O baseboard (F16 bus) and memory modules (through midplane)
- Clock generation for most of the Ak450NX board set components
- Onboard DC-DC converter for the CPU baseboard and memory module V_{TT} power
- Four sockets for voltage regulator module (VRM) 8.3 converters to supply power to the processor core component of the four Pentium II Xeon processors
- Two sockets for VRM 8.3 converters for the L2 cache voltage for the Pentium II Xeon processors
- IPMI, SPI, and In-system Programming (ISP) server management interfaces

2.2.1   Block Diagram

Figure 2-5 illustrates the general architecture of the CPU baseboard.
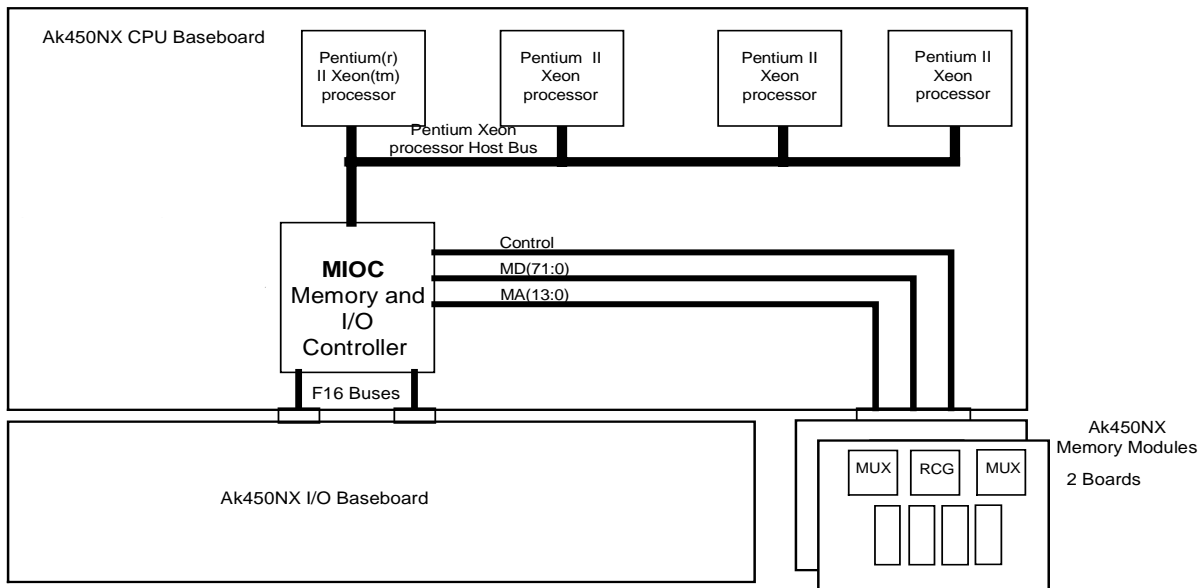
Figure 2-5: CPU Baseboard Block Diagram

2.2.2   Placement Diagram

Figure 2-6 shows the placement of the major components and connectors on the CPU baseboard.
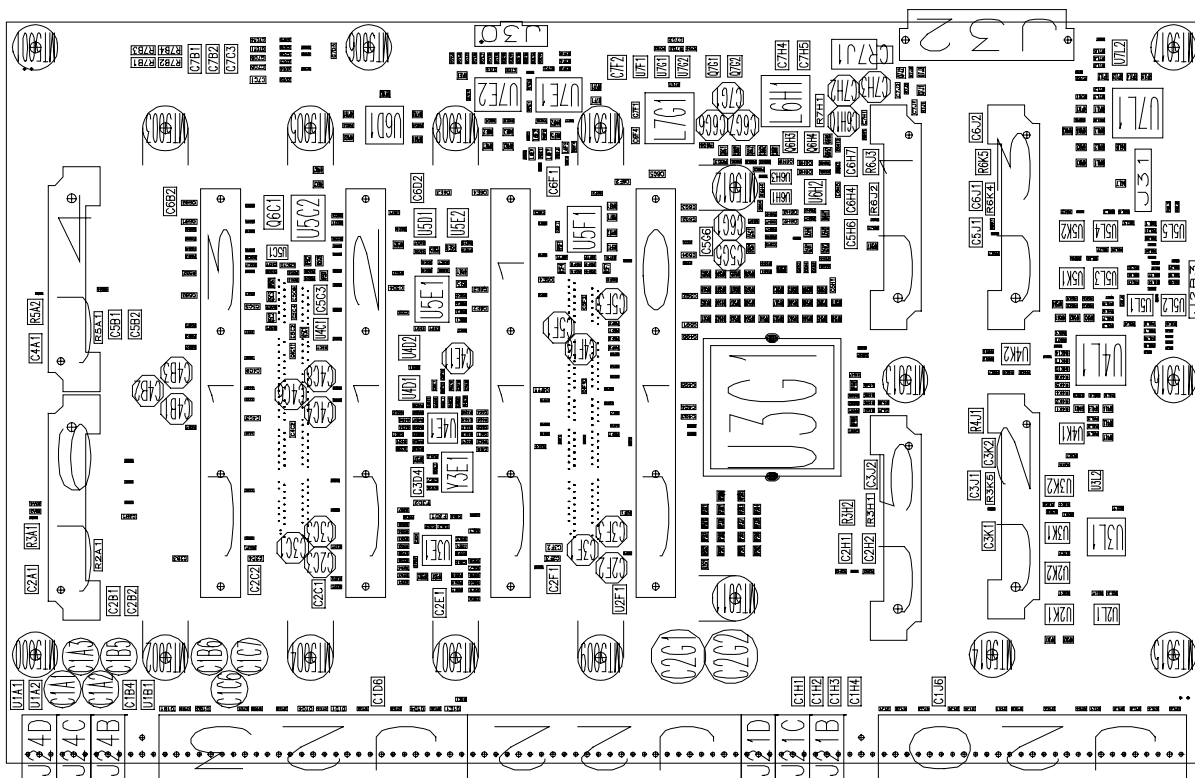
Figure 2-6: CPU Baseboard Layout

Refer to *Chapter 5 Board Specifications* for a detailed mechanical drawing. The connectors are as follows:

Table 2-16: Connectors on the CPU Baseboard

Jumper	Connector Name	Description
J1	VRM socket	Provides power for processor slot #1 (processor core power only)
J2	VRM socket	Provides power for processor slots #1 and #2 (L2 cache power only)
J3	VRM socket	Provides power for processor slot #2 (processor core power only)
J4	VRM socket	Provides power for processor slot #3 (processor core power only)
J5	VRM socket	Provides power for processor slots #3 and #4 (L2 cache power only)
J6	VRM socket	Provides power for processor slot #4 (processor core power only)
J10	Slot 2 connector	Processor slot #1
J11	Slot 2 connector	Processor slot #2
J12	Slot 2 connector	Processor slot #3
J13	Slot 2 connector	Processor slot #4
J2B3	ISP connector	
J30	ITP connector	
J31	Board configuration jumper block	
J24	Power connector	

Jumper	Connector Name	Description
J23	Memory connector #1	
J22	I/O connector	
J21	Power connector	
J20	Memory connector #2	
J32	Front panel connector	

2.2.3   Functional Architecture

This section provides a more detailed architectural description of the main functional blocks of the CPU baseboard.

2.2.3.1   Front-side Bus

This 64-bit bus uses AGTL+ technology and runs at 100 MHz. The FSB requires special AGTL+ buffers employing active termination through a pull-up device at each output buffer. 1-4 Pentium II Xeon processors can be installed into the Ak450NX CPU baseboard. These processors are connected together and to the MIOC of the 82450NX PCIset through the front-side bus for superior data reliability. The front-side bus is ECC protected.

The AGTL+ signaling technology requires that each stub of the FSB must be terminated. Therefore, the FSB requires termination modules to be installed in each unused processor slot. For example, in a dual processor system, slot #1 and slot #2 will contain processors while slot #3 and slot #4 will contain termination modules. Processors must always be inserted starting with processor slot #1 and continue successively into the #2, #3, and #4 slots.

2.2.3.2   Memory Interface Bus

The Ak450NX memory interface bus consists of two memory modules that connect to the CPU baseboard through the midplane. Each contains sixteen 72-bit wide DIMM sockets. With the largest DIMM size (256 MB) installed in each socket, each memory module can provide up to 4 GB of EDO memory per module. The memory interface is extensible to potential future versions of the Ak450NX memory module.

Like the processor bus, the memory bus also uses AGTL+ signaling technology. However, a source synchronous scheme is used on this bus enabling data transfers at up to twice the bus frequency. This is achieved by sending two strobes, offset by 180 degrees, together with data, both running at 100 MHz, and using them to capture the data at the destination. The strobes are single ended. Like the processor bus, any open connector on the memory bus (not the DIMM sockets) has to be terminated; thus both memory connectors on the Ak450NX midplane must always be populated with memory modules. One common address/data/control bus is routed from the MIOC component on the CPU baseboard to the interface connectors at the midplane, and continues on to the two memory module connectors on the midplane. In addition, there are dedicated control signals for each of the memory module connectors.

2.2.3.3   I/O Interface (F16 Bus)

There are two F16 16-bit, parity checked, high-speed, bidirectional, point-to-point links between the CPU baseboard and the I/O baseboard. Like the memory bus, the F16 uses a source-synchronous scheme but the strobes are differential. Each F16 bus can transfer data on both the rising and falling edges of the 100 MHz clock. This results in 400 MB/s of bandwidth available to each and has enough bandwidth to support the two 32-bit, 33-MHz PCI buses or one 64-bit, 33-MHz PCI bus. Like the FSB and memory interfaces, the F16 buses use AGTL+ signaling technology.

2.2.3.4   Clock Generation

Figure 2-7 shows the clock distribution architecture for the Ak450NX CPU baseboard. The clock frequency of the onboard clock oscillator is 100 MHz and is distributed through clock buffers to several remote components on the other boards of the Ak450NX board set.

Ak450NX CPU Baseboard Clock Distribution
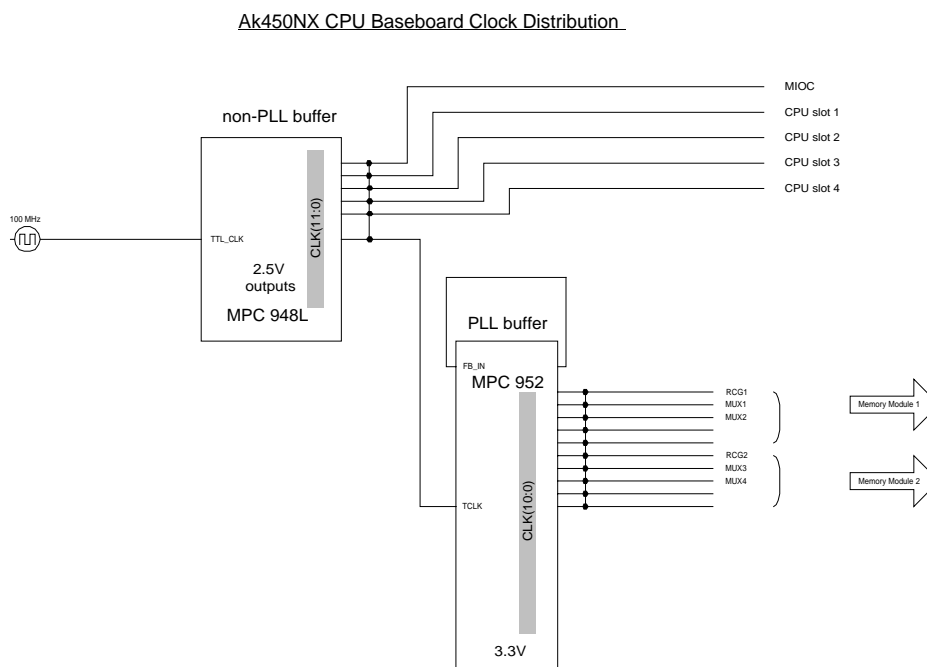
Figure 2-7: CPU Baseboard Clock Distribution

2.2.3.5   Voltage Regulators

The voltage supply for each of the four processor cores is supplied independently by one VRM 8.3 converter, for a total of four VRMs. Two additional VRM 8.3 converters provide the voltage supply for the L2 caches; one VRM is shared between two processors. This arrangement requires that the L2 voltages within a processor pair be identical. A PAL on the CPU baseboard called the VMC compares the VID bits from the two L2s and, if different, the VMC disables the VRM. See the *VRM 8.3 DC-DC Converter Design Guidelines* for details on these converters. Note that the VRM 8.3 has remote sensing.

For all processors installed into the CPU baseboard, the VRM supplying current for both the core and L2 cache of that processor must be populated. If a processor is not installed, the corresponding VRM(s) may be installed either in the socket, or the socket may be left empty. If the VRM is installed even though its corresponding processor is not, circuitry on the CPU baseboard disables the VRM.

All converters for the processor voltages convert off of the +12 V supply rail. The CPU baseboard also has one large switching regulator for the AGTL+ termination voltage (1.5 V) required on the CPU baseboard, memory modules, and processors, and a small +2.5 V linear regulator for the 2.5 V logic (clock buffers and voltage shifters). Both of these regulators convert off of the +5 V supply rail.

2.2.4 Configuring Baseboard Jumpers

The J31 jumper block serves three functions (refer to Figure 2-8):

- Controls the VRMs and server management outputs (see Table 2-17)
- Determines core to bus ratio (see Table 2-18)
- Provides parking space for unused jumper pegs
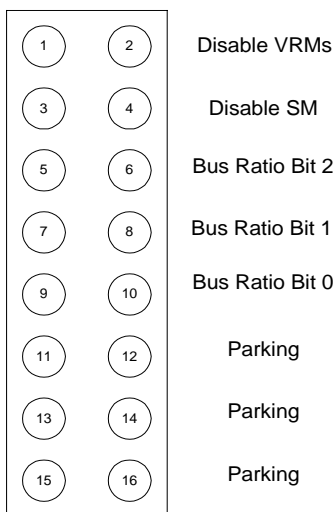
Figure 2-8: J31 Jumper Block Pinout

Table 2-17: Board Configuration Jumper Block (VRMs, Server Management)

Pins 1-2	Pins 3-4	Status
1	1	Disables VRMs
1	0	Reserved
0	1	Disable Server Management
0	0	Default/Normal Operation

Notes: 1. 0=open, 1=closed.

2. Jumpers across pins 1-2 and 3-4 are for Intel's validation and manufacturing test purposes only. In normal operation these jumpers should be open.

Jumpers across pins 5-6, 7-8, and 9-10 determine the processor core to the front side bus frequency ratio. The bus frequency (supplied by the onboard TTL oscillator) is 100 MHz. Core frequencies shown in Table 2-18 are based on 100 MHz bus frequency.

Table 2-18: Board Configuration Jumper Block (Bus Ratio)

Pins 5-6	Pins 7-8	Pins 9-10	Bus Ratio	Core Freq. (MHz)
1	1	1	11:2	550
1	1	0	9:2	450
1	0	1	7:2	350
1	0	0	Reserved	

Pins 5-6	Pins 7-8	Pins 9-10	Bus Ratio	Core Freq. (MHz)
0	1	1	5:1	500
0	1	0	4:1	400
0	0	1	3:1	300
0	0	0	Reserved	

Notes: 0=open, 1=closed.

There are three parking positions available for the safekeeping of the jumper pegs. These jumper pegs can be parked across pins 11-12, 13-14, and 15-16.

2.2.5 Populating Processors

Processors must be populated starting at the first Slot 2 connector (J10), then at the second Slot 2 connector (J11), and so on. All empty processor slots must be populated with FSB termination modules.

2.2.6 Mixing Processors of Different Frequency and Stepping

Processors are validated to operate within a minimum and maximum frequency window. For instance, a processor rated as 350 MHz is not guaranteed to operate beyond 350 MHz, but may be guaranteed to operate down to 300 MHz. Refer to the *Pentium® II Xeon™ Processor Datasheet* for supported valid ranges. Consequently, processors of different frequency ratings may have different valid ranges. **The common range among the different processors determines the overall valid frequency range within which the core-to-bus ratio jumper (J31) needs to be set.** This means the lowest rated processor would determine the overall core-to-bus ratio, compromising the performance achievable with the higher rated processors in the system.

Though Intel recommends using identical processor steppings in multiprocessor systems (as this is the only configuration that receives full validation across all of Intel's testing), Intel does not actively prevent using various steppings of the Pentium II Xeon processor together in MP systems. However, since Intel cannot validate every possible combination of devices, each stepping of a device is fully validated only against the latest steppings of other processors and chip set components. Refer to the *Pentium® II Xeon™ Processor Datasheet* for further details on issues related to mixed processor steppings in an MP system.

2.2.7 Server Management Features

The private I^{2}C buses provide access to basic temperature, configuration, and inventory information. The CPU baseboard contains the following I^{2}C accessible devices:

- Baseboard FRU information and temperature sensor (Dallas* DS1624)
- Processor temperature sensors in Pentium II Xeon processors
- Processor FRU information SEEPROM

These server management features are accessed via the BMC on the Ak450NX I/O baseboard. Details on how to access information on this bus are described in the *AC450NX (Polar) Server Management EPS*. The I^{2}C devices are accessible at the addresses show in Table 2-19.

Table 2-19: CPU Baseboard I²C Address Map

Device and Bus Name	I²C Address
Devices on Pentium® II Xeon™ processor SMBus:	
Processor #1: OEM_EEPROM	Intel_EEPROM	A2D converter	A0h,A1h	A2h,A3h	30h,31h
Processor #2: OEM_EEPROM	Intel_EEPROM	A2D converter	A4h,A5h	A6h,A7h	52h,53h
Processor #3: OEM_EEPROM	Intel_EEPROM	A2D converter	A8h,A9h	AAh,ABh	34h,35h
Processor #4: OEM_EEPROM	Intel_EEPROM	A2D converter	ACh,ADh	AEh,AFh	56h,57h
Terminator card (if present) at 1st processor slot OEM_EEPROM	A0h,A1h
Terminator card (if present) at 2nd processor slot OEM_EEPROM	A4h,A5h
Terminator card (if present) at 3rd processor slot OEM_EEPROM	A8h,A9h
Terminator card (if present) at 4th processor slot OEM_EEPROM	Ach,Adh
Devices on BMC's Private I²C Bus:	
CPU baseboard temperature and FRU information	98h,99h

2.2.7.1   DS1624* SEEPROM

The DS1624, when accessed via the BMC's private I²C bus, provides the temperature of the baseboard, as measured at the DS1624, as well as the FRU information shown in Table 2-21. The FRU information is read by the Intel LANDesk Server Manager or similar software, and is available via the Intel® Server Control (ISC).

The DS1624 SEEPROM has 256 bytes of programmable space, which is broken into four areas. Table 2-20 is a list of the areas, with a description and the amount of space allocated to each.

Table 2-20: DS1624 SEEPROM Programming Areas

Area	Size	Description
Common Header	8 bytes	Programming offsets to the other areas below.
Internal Use	48 bytes	This area is reserved for general-purpose use by the Intel® Server Management Firmware/Controllers.
Board Information	80 bytes	Contains the board FRU information listed in Table 2-21.
Product Information	120 bytes	Available for OEM use[†]

[†]The Intel-provided FRU and SDR Load Utility allows OEMs to program this area. Refer to the *FRU and SDR Load Utility EPS* for more details.

Table 2-21 lists the board specific FRU information that will be programmed into the board information area.

Table 2-21: FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. Date/Time	Time and date of board manufacture (value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/96).	000f593h (Date/time translation shown below.) f593h = 62867 min. = 43 days and 947 min. = Feb 12, 1996, 3:47 p.m.	2
Manufacturer	Board Manufacturer	Intel	1
Board Product Name	Board Name/Description	Ak450NX CPU Baseboard	1
Board Serial Number	Intel Board Serial Number	INBR85906000	2
Board Part Number	Intel Board Part Number	702545-301	2

Notes: 1.   Actual value programmed into the board.

2.   Example value. Actual value will vary with each board and fab revision.

Table 2-22 identifies exactly how bytes are allocated within the DS1624 SEEPROM. This information is useful for those who will be accessing the hardware directly for information (i.e., BIOS and server management software developers).

Table 2-22: SEEPROM Byte Map

Address	Length	Description	Default Value
0x00	1	Common Header Format Version	0x01
0x01	1	Internal Use Area Offset (8-byte multiples)	0x01
0x02	1	Chassis Information Area Offset (8-byte multiples)	0x00 (area not present)
0x03	1	Board Information Area Offset (8-byte multiples)	0x07
0x04	1	Product Information Area Offset (8-byte multiples)	0x11
0x05	2	Zero Padding	
0x07	1	Common Header Checksum	0xE6
0x08	48	Internal Use Area	
0x38	1	Board Information Area Format Version	0x01
0x39	1	Board Information Area Length (8-byte multiples)	0x0A
0x3A	1	Unicode Country Base	0x00
0x3B	3	Manufacture Date/Time	
0x3E	1	Board Manufacturer Type/Length Byte	0xC5
0x3F	5	Board Manufacturer (ASCII)	'Intel'
0x44	1	Product Name Type/Length Byte	0xD5
0x45	31	Product Name	'Ak450NX CPU Baseboard'
0x64	1	Board Serial Number Type/Length Byte	0xCC
0x65	12	Board Serial Number	…………
0x71	1	Board Part Number Type/Length Byte	0xCA
0x72	10	Board Part Number	………
0x7C	1	No More Fields Flag	0xC1
0x7D	10	Zero Padding	
0x87	1	Board Information Area Checksum	0x7E
0x88	120	Product Information Area	

Temperature and SEEPROM data may be accessed via I^{2}C commands to the DS1624 device. Table 2-23 is taken from the DS1624 data sheet.

Table 2-23: SEEPROM Command Set

Instruction	Description	Protocol	2-Wire Bus Data After Issuing Protocol
Temperature Conversion Commands			
Read Temperature	Read last converted temperature value from temperature register.	Aah	<read 2 bytes data>
Start Convert T	Initiates temperature conversion.	Eeh	Idle
Stop Convert T	Halts temperature conversion.	22h	Idle
Memory Commands			
Access Memory	Reads or writes to 256-byte EEPROM memory.	17h	<write data>
Access Config.	Reads or writes configuration data to configuration register.	Ach	<write data>

2.2.8   Front Panel

The AC450NX server system chassis front panel connects to the Ak450NX CPU baseboard through an 80-pin SCA-type connector. Almost all of the front panel signals interfacing through that connector are sourced or destined to the Ak450NX I/O baseboard through the I/O connector on the CPU baseboard. The CPU baseboard just acts as a passive transport for these signals between the front panel, midplane, and I/O baseboard. For connector numbering conventions and mechanical specifications, refer to *Chapter 5 Board Specifications.*

2.3 Front-side Bus Terminator Module

This section describes the features of the front-side bus (FSB) terminator module. The FSB terminator module was designed to be used with the CPU baseboard component of the Ak450NX MP server board set. This card is common with the FSB terminator module used in the Intel® A450NX MP server board set, which has features that are similar to those of the Ak450NX MP server board set, except that it is designed in a different form factor suitable for a floor standing server chassis

2.3.1 Architectural Overview

The signaling technology (AGTL+) used for the front-side bus of the Ak450NX CPU baseboard require that each stub of the front-side bus be properly terminated. The FSB terminator module contains the appropriate signal trace layout and resistors to provide this electrical termination. The Pentium II Xeon processor also can provide the required FSB termination. Therefore, each of the four FSB slot-2 connectors must be populated with either a processor or termination module. For example, if only one processor were to be installed on the Ak450NX CPU baseboard, then three additional FSB terminator modules would be needed to populate the remaining three slot-2 connectors.

Features

- Terminates the processors front-side bus AGTL+ signals
- FRU information (P/N, S/N, board ID, etc.) via I^{2}C

2.3.1.1 Placement Diagram

Figure 2-9 shows the primary components of the FSB terminator module and their positions on the printed circuit board. Table 2-24 maps reference designators to device names.
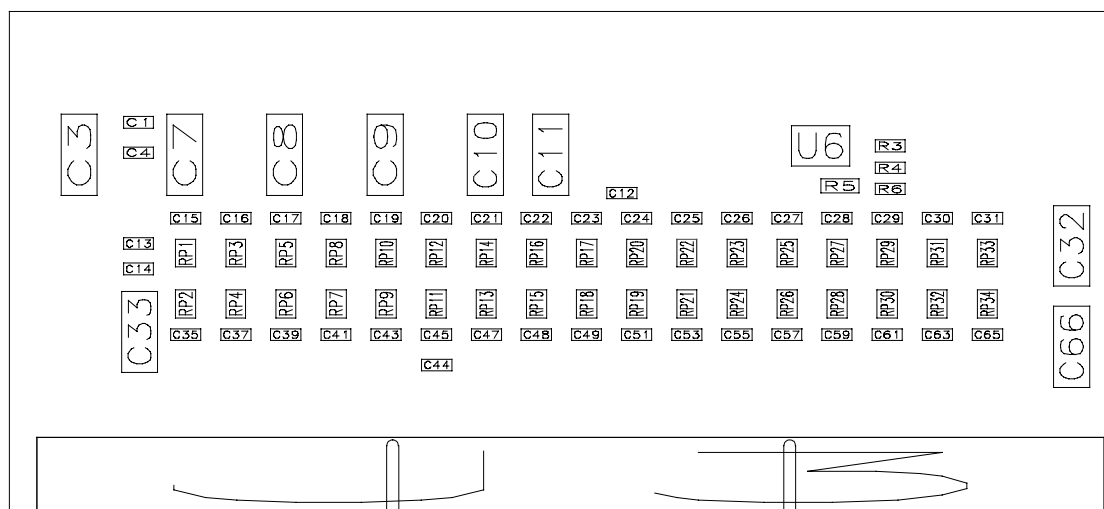
Figure 2-9: FSB Terminator Module Placement Diagram

Table 2-24: Reference Designator Decoder

Reference Designator	Description
U6	AT24C02* SEEPROM
J3	FSB interface connector

2.3.2   Server Management Features

The FSB terminator module contains the following I^2C accessible device:

- Atmel AT24C02* - SEEPROM containing FRU information

The FRU device information is accessible at the addresses shown in Table 2-25.

Table 2-25: FSB Terminator Module Address Map

Device	Function	Bus Name	Slot	Address
AT24C02*	FSB Term. Module FRU Information	Processor SMBus[†]	Processor Slot #1	A0h,A1h
AT24C02	FSB Term. Module FRU Information	Processor SMBus[†]	Processor Slot #2	A4h,A5h
AT24C02	FSB Term. Module FRU Information	Processor SMBus[†]	Processor Slot #3	A8h,A9h
AT24C02	FSB Term. Module FRU Information	Processor SMBus[†]	Processor Slot #4	ACh,ADh

[†] The AT24C02* device can be accessed through the Pentium® II Xeon™ slot-2 processor SMBus only via the BMC.

The AT24C02, when accessed, will provide FRU information for the board. The FRU information is read and made available by the ISC.

The AT24C02 SEEPROM has 256 bytes of programmable nonvolatile memory, which is broken into four areas. Table 2-26 provides a list of the areas, a description each area, and the space allocated to each.

Table 2-26: AT24C02 SEEPROM Programming Areas

Area	Size	Description
Common Header	8 bytes	Programming offsets to the other areas below.
Internal Use	48 bytes	This area is reserved for general purpose use by Intel® server management firmware/controllers.
Board Info	80 bytes	Contains the board FRU information listed in Table 2-27.
Product Info	120 bytes	Available for OEM use[†]

[†] An FRU & SDR Load Utility is provided by Intel that allows OEMs to program that area. Please refer to the *FRU & SDR Load Utility* documentation for details.

Table 2-27 lists the specific board FRU information that is programmed into the board information area during manufacturing assembly.

Table 2-27: FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. Date/Time	Time & Date of board manufacture (Value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/96)	0x00f593h (Date/time translation shown below) f593h = 62867 min = 43 Days & 947 min = Feb 12, 1996, 3:47pm	2
Manufacturer	Board Manufacturer	Intel	1
Board Product Name	Board Name/Description	A450NX FSB Terminator Module	1
Board Serial Number	Intel Board Serial Number	INBR42385906	2
Board Part Number	Intel Board Part Number	663077-001	2

Notes: **1.** Actual value programmed into the board.
           2. Example value. Actual value will vary with each board and fab revision.

Table 2-28 identifies exactly how bytes are allocated within the AT24C02 SEEPROM. This information is useful for those who will be accessing the hardware directly for information (e.g., BIOS and server management software developers).

Table 2-28: SEEPROM Content Location

Address	Length	Description	Default Value
0x00	1	Common Header Format Version	0x01
0x01	1	Internal Use Area Offset (8-byte multiples)	0x01
0x02	1	Chassis Information Area Offset (8-byte multiples)	0x00 (area not present)
0x03	1	Board Information Area Offset (8-byte multiples)	0x07
0x04	1	Product Information Area Offset (8-byte multiples)	0x11
0x05	2	Zero Padding	
0x07	1	Common Header Checksum	0xE6
0x08	48	Internal Use Area	
0x38	1	Board Information Area Format Version	0x01
0x39	1	Board Information Area Length (8-byte multiples)	0x0A
0x3A	1	Unicode Country Base	0x00
0x3B	3	Manufacture Date/Time	
0x3E	1	Board Manufacturer Type/Length Byte	0xC5
0x3F	5	Board Manufacturer (ASCII)	'Intel'
0x44	1	Product Name Type/Length Byte	0xDC
0x45	28	Product Name	'A450NX FSB Terminator Module'
0x61	1	Board Serial Number Type/Length Byte	0xCC
0x62	12	Board Serial Number	....
0x6E	1	Board Part Number Type/Length Byte	0xCA
0x6F	10	Board Part Number	....
0x79	1	No More Fields Flag	0xC1
0x7A	13	Zero Padding	
0x87	1	Board Information Area Checksum	0xC7
0x88	120	Product Information Area	

2.4   Memory Module

This section describes the architecture and external interfaces of the Ak450NX memory module. The Ak450NX memory module is a high-capacity DRAM memory board based on the Intel® 82450NX PCIset. The memory module has been designed for use with the Ak450NX CPU baseboard and midplane.

The midplane has two memory module connectors. Both midplane memory interface connectors must be filled in order to terminate the AGTL+ memory bus properly. Two memory modules must be installed in the midplane in order to properly terminate the AGTL+ memory bus, however, only one of the modules needs to be populated with dual inline memory modules (DIMMs).

Features

- Up to 4 GB of error correction code (ECC) memory per module using 16 72-bit DIMMs, for a total of 8 GB using two modules.
- 60 ns and 50 ns 3.3 V buffered EDO DRAM.
- Four-way interleaving.
- Minimum configuration of 128 MB using four 32-MB DIMMs.
- Supports buffered DIMMs with capacity of 32 MB, 64 MB, and 256 MB. Other DRAM sizes may function correctly but will not be validated.
- Provides server management data, including thermal monitoring, field replaceable unit (FRU) information, and presence detect bit access.
- High-reliability Futurebus* right-angle mating connector for interfacing with the Ak450NX midplane.

1.1.1   Introduction

This section provides an overview of the memory module, showing primary components and their relationships, and physical board layout diagrams.

2.4.2   Block Diagram

Figure 2-10 shows the main architectural features of the memory module.
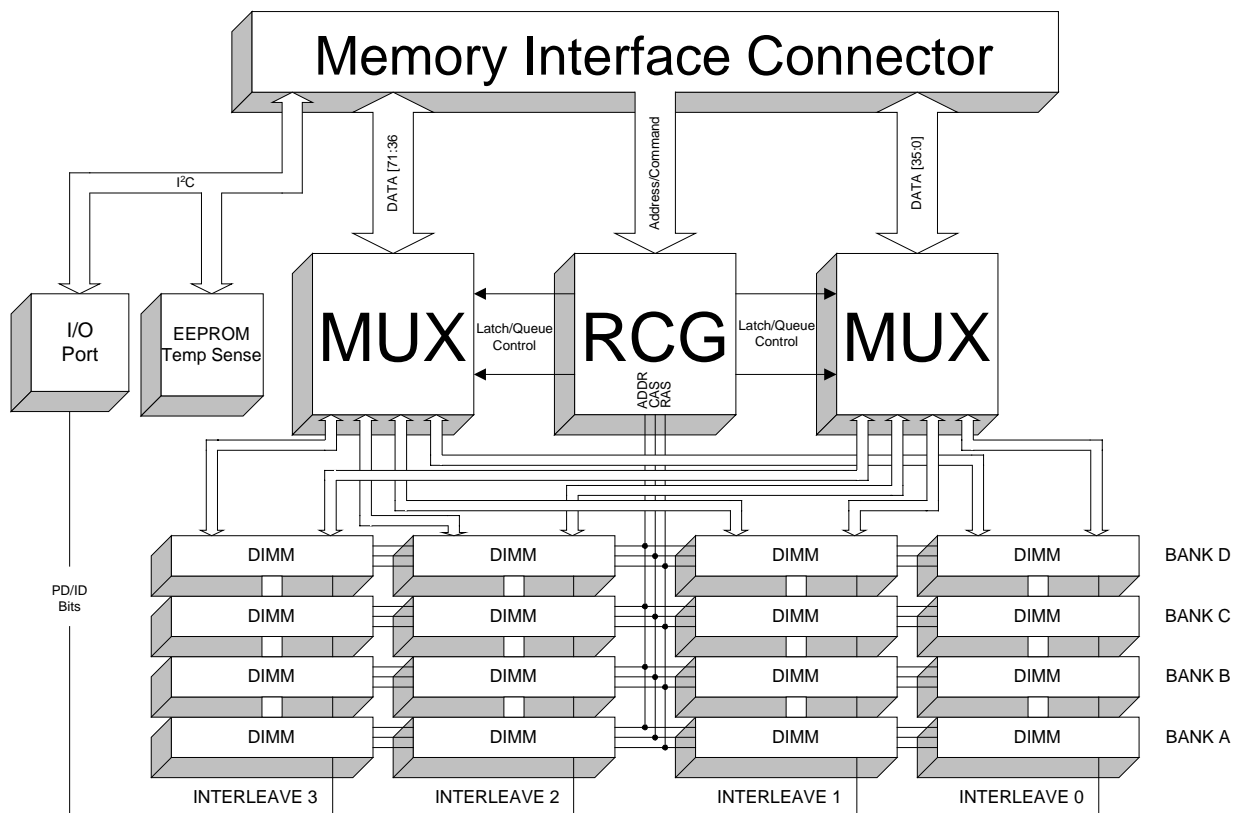
Figure 2-10:Memory Module Block Diagram

2.4.3　Placement Diagram

The diagram in Figure 2-11 was generated from the actual layout database and shows the primary components of the memory module, and their position on the printed circuit board. Table 2-29 maps reference designators to device names.
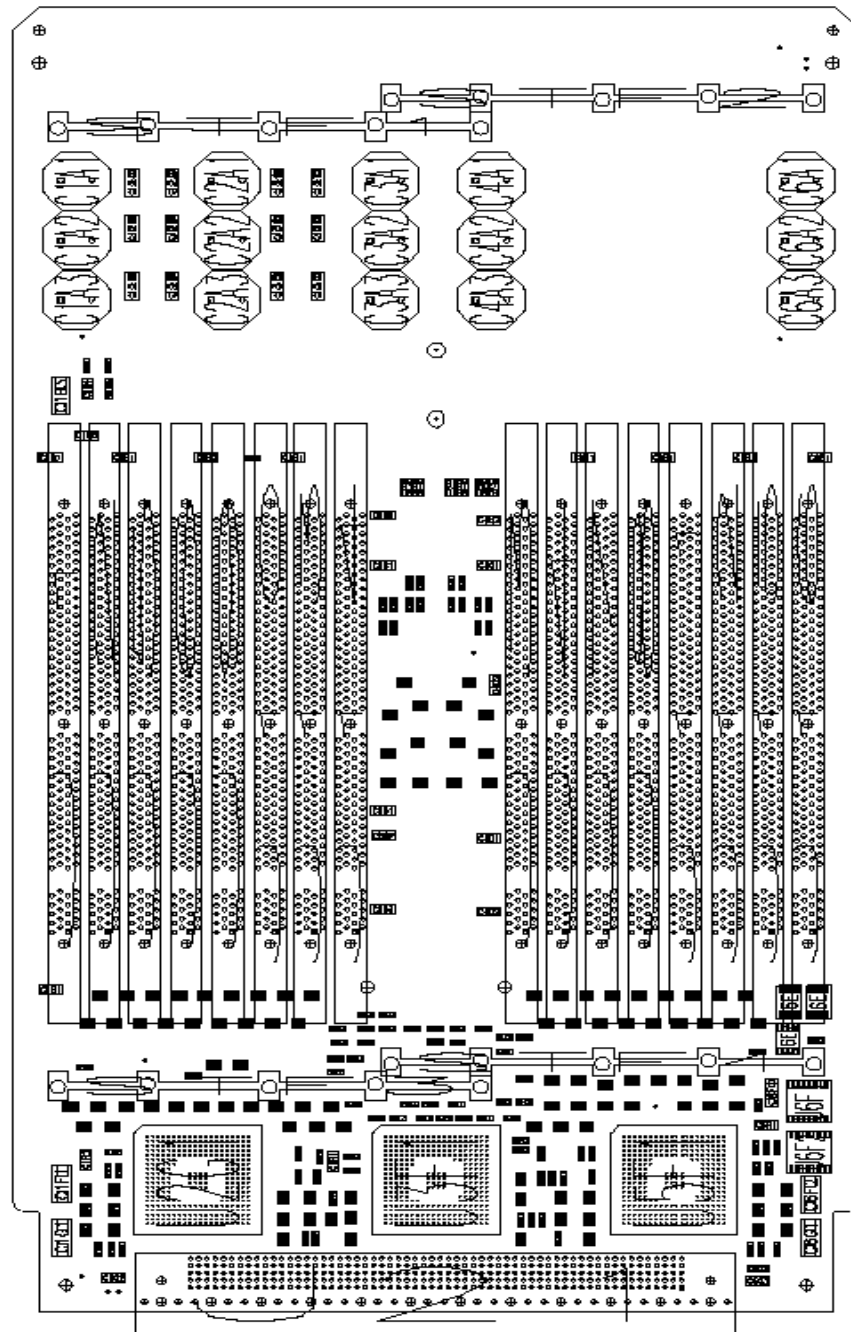
Figure 2-11:Board Layout

Table 2-29: Placement Diagram Reference Designators

Reference Designator	Description
U2F1	MUX0, data path multiplexor for data bits 0-35, 324-ball BGA
U3F1	MUX1, data path multiplexor for data bits 36-71, 324-ball BGA
U5F1	RCG, RAS/CAS generator for banks A-D, 324-ball BGA
U6E2	DS1624, I^{2}C EEPROM and temperature sensor [package].
U6F1, U6F2	PCF8574A, I^{2}C 8-bit I/O ports [package].
U6E1, U6E3	74LVC138, 3-8 decoders [package].
J1-J4	168-pin DIMM sockets, Bank A.
J5-J8	168-pin DIMM sockets, Bank B.
J9-J12	168-pin DIMM sockets, Bank C.
J13-J16	168-pin DIMM sockets, Bank D.
J21	Memory interface connector (Futurebus* connector).
C1A1-C1A3	Capacitors for 3.3 V current transients (each are 1" tall 6800uF electrolytic capacitors).
C2A1-C2A3	Capacitors for 3.3 V current transients (each are 1" tall 6800uF electrolytic capacitors).
C3A1-C3A3	Capacitors for 3.3 V current transients (each are 1" tall 6800uF electrolytic capacitors).
C4A1-C4A3	Capacitors for 3.3 V current transients (each are 1" tall 6800uF electrolytic capacitors).
C6A1-C6A3	Capacitors for 3.3 V current transients (each are 1" tall 6800uF electrolytic capacitors).

2.4.4 Functional Architecture

This section provides a more detailed description of the memory module's main components.

The memory module is based on the Intel® 82450NX chip set. The module's main components are as follows:

- DRAM array consisting of 16 DIMM sockets which accept 3.3 V buffered ECC DIMMs
- One 82450NX RAS-CAS Generator (RCG) which drives RAS, CAS, address, and write enable to the DRAM array
- Two 82450NX data path multiplexors (MUXs) which drive and receive data to and from the DRAM array
- Server management support with onboard EEPROM and temperature sensor plus accessibility of all presence detect (PD) bits from all DIMMs

2.4.4.1   EDO DRAM Array

The memory array on the memory module consists of 16 72-bit (64-bit data plus 8 ECC bits) DIMM sockets. These sockets are divided into four banks of four sockets each (labeled A through D). These banks support only 4:1 interleaving. With 4:1 interleaving, all four DIMMs in the bank are populated and a single DRAM transaction is required to retrieve a full cache line. The four DIMMs are organized as follows, using the reference designators for Bank A as an example:

- J1   Interleave 0
- J2   Interleave 1
- J3   Interleave 2
- J4   Interleave 3

Each interleave provides access to 72 bits of data, thus 4:1 interleaving yields 288-bits (32 bytes) per transaction, which is one cache line for the Pentium II Xeon processor. With two memory modules in a system, the modules can complete DRAM transactions at a maximum rate of once every 30 ns (when consecutive transactions hit in different memory modules) for a maximum data rate of 1.067 GB/s.

Note that to achieve the maximum sustainable bandwidth, the memory modules must be configured so that

1. memory accesses can alternate back and forth between boards and,

2. it is possible to get a continuous stream of row misses.

Condition 2 can be achieved only if a minimum of four banks of memory are populated. To meet both conditions 1 and 2, a minimum of four banks must be populated, two on each memory module.

There are several types of DIMM components available. Table 2-30 shows which combinations of DIMM components can be functionally used in the memory module. As a result of the numerous possible combinations of DIMM size, speed, vendor, and location within the memory module, not all combinations will be validated by Intel.

Table 2-30: Memory Module DIMM Support

Category	Supported DIMM Variety
Speed	50 ns, 60 ns
Capacity/ Organization/ Refresh	16 MB: 16 Mbit, 2 M x 8 DRAM; 2K Refresh[1,2]
	32 MB: 16 Mbit, 4 M x 4 DRAM; 2K or 4K Refresh[1]
	64 MB: 64 Mbit, 8 M x 8 DRAM; 4K Refresh[1]
	128 MB: 64 Mbit, 16 M x 4 DRAM; 4K or 8K Refresh[1,2]
	256 MB: Double-high; 64 Mbit, 16 M x 4 DRAM; 4K or 8K Refresh[1]
Voltage	3.3 V
Data Width	x 72 (ECC)
Page Mode	EDO
Buffered/Non	Buffered
Maximum Height	2.1 inches
DRAM Package	TSOP

Notes: 1.   The memory module supports CAS-before-RAS refresh only. When selecting a module, make sure that the target refresh number corresponds to CAS-before-RAS (CBR) refresh.

2.   Should function correctly, but will not be validated.

The memory module will not work with any interleave scheme other than 4:1 interleaving. As a result, there are basic population requirements. the following bullets outline the configurations expected to function in the Ak450NX board set. However, only a limited subset of the possible combinations from these parameters will be validated and supported by Intel. The requirements which will result in an Intel validated and supported configuration are discussed in the paragraph below.

- All banks used must be fully populated with four DIMMs
- 16 MB, 32MB, 64 MB, 128 MB, and 256 MB capacity DIMMs
- 4, 8, 12, 16, 20, 24, 28, 32 DIMMs (total number of DIMMs on both memory modules; see Figure 2-12 through Figure 2-15).
- 50 ns or 60 ns DIMM speeds (DIMMs may be mixed from bank to bank, but all DIMMs will run at the speed of the slowest installed DIMM)
- Banks are to be populated in consecutive order from the first (Bank A) to the last (Bank D) in each module
- All DIMMs in a given bank must be of uniform size. DIMM sizes may change from bank to bank.

The following configurations will be validated and fully supported by Intel.

Note: Only the following configuration rules should be used to populate the memory module. If other configurations are desired (as discussed in the previous configuration rules), they need to be validated by the OEM.

- All banks used must be fully populated with four DIMMs
- 32 MB, 64 MB, and 256 MB DIMMs
- 50 ns or 60 ns DIMM speeds (all DIMMs installed must be of identical speed)
- 4, 8, 16, 24, or 32 DIMMs (total number of DIMMs installed in both memory modules)
- Equal number of DIMMs in each memory module (except when only four DIMMs are used. In this case, the four DIMMs must be installed in Bank A of the primary memory module)
- All DIMMs on a module must be of identical size and speed
- DIMM sizes may differ between memory modules

To take advantage of address bit permuting (ABP), which increases memory access performance across sequential cache line accesses, the following rules must be followed:

- All rules listed above.
- All banks that are used must be populated with four DIMMs.
- There must be a power of two banks populated (two, four, or eight banks).
- All banks in an ABP group (eight DIMMs in two-bank permuting, 16 DIMMs in four-bank permuting, or 32 DIMMs in eight-bank permuting) must be the same size.
- All populated banks must be adjacent and must start at bank 0.
- Both memory modules must be configured to allow equivalent ABP settings. For example, the chip set cannot support two-bank permuting on one board and four-bank permuting on the other.

To take advantage of card-to-card interleaving (C2C), which provides maximum performance across sequential cache line accesses, the following rules must be followed:

- All ABP rules above must be followed.
- Corresponding banks of the first memory module must be populated identically with DIMMs of the same size and type as those populating banks in the second memory module.

Figure 2-12 through Figure 2-15 are given as a graphical representation of the supported configuration requirements discussed above. These figures describe the population order only and do not specify the DIMM capacity/speed combination requirements (refer back to the supported capacity/speed requirements given above). Also, refer to the ABP and C2C restrictions discussed above to maximize memory data transfer performance.
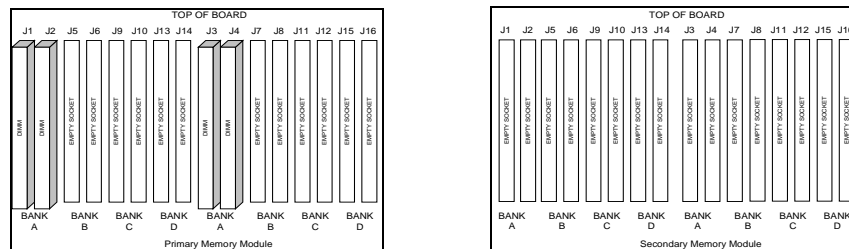
Figure 2-12:Interleave with Four DIMMs
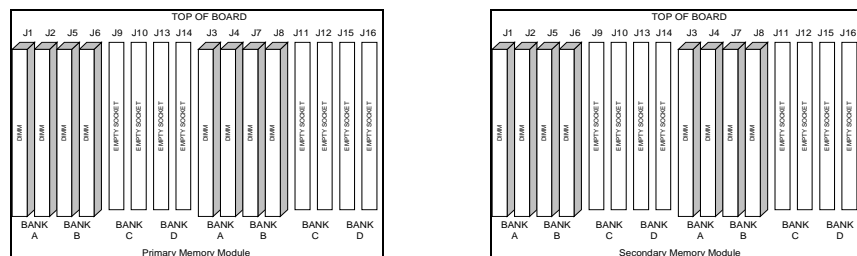
Figure 2-13:Interleave with 16 DIMMs (Two Memory Modules)
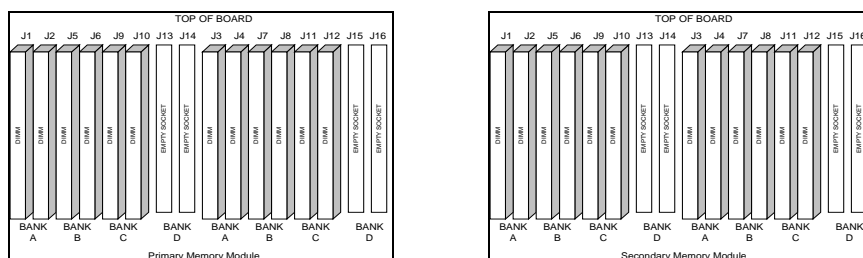
Figure 2-14:Interleave with 24 DIMMs (Two Memory Modules)
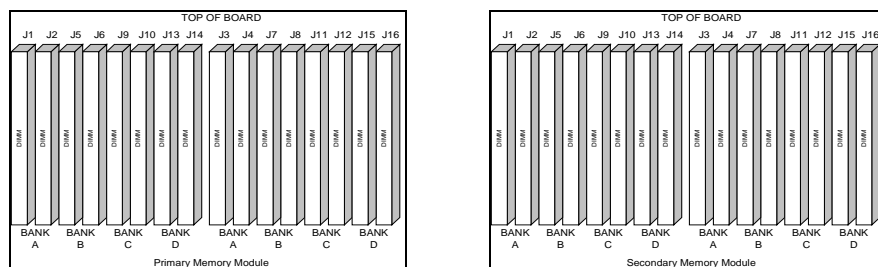
Figure 2-15:Interleave with 32 DIMMs (Two Memory Modules)

The server management firmware scans for the speed of all DIMMs during the power-on self test (POST). If all DIMMs are found to be 50 ns devices, then server management sets DIMM speed at 50 ns. If any single installed DIMM is found to not be 50 ns, then server management sets DIMM speed at 60 ns.

2.4.4.2   Intel® 450NX PCIset

2.4.4.2.1   MUX

The purpose of the MUX is to provide the data path from the DRAM array to the MIOC. The MUX takes no action by itself but is controlled either by the MIOC or RCG. Each MUX contains four 36-bit data I/O paths (quad words) to the DRAM array and a single 36-bit data I/O path to the MIOC. The respective quad words from each MUX are combined for the full 72-bits required for the memory data (MD) bus.

2.4.4.2.2   RCG

The RCG's primary purpose is to generate the signals to control accesses to the DRAM array. The RCG is responsible for driving the data to the MIOC by means of getting the data out on the MD bus. The RCG responds to

three types of requests from the MIOC: read, write, and refresh. Once one of these three commands has been received from the MIOC, the RCG will assert the appropriate DRAM control signals (RAS#, CAS#, address and WE#) to carry out that transaction. Each RCG contains four RAS/CAS control units (RCCUs); each one is dedicated to one bank of DRAM.

2.4.4.2.3   Error Detection and Correction

The 450NX chip set provides automatic correction of single bit errors and detection of double bit errors. All failures can be reported by the BIOS and recorded into the system event log. Single-bit errors will be reported down to the exact bit within a DIMM. Multi-bit errors will be reported down to an interleave, which corresponds to a single DIMM.

2.4.4.3   Server Management Features

The memory module server management features provide information about board operating temperature and DIMM configuration, in addition to FRU information about the memory module itself.

This data comes from three devices that reside on the BMC's private I^2C bus. Temperature and FRU data are provided by a Dallas DS1624* EEPROM, while DIMM configuration data (presence, organization, size, speed, etc.) can be accessed via two Philips PCF8574A* 8-bit I/O ports. The I^2C addresses of the three devices are listed in Table 2-31. Note that the address of a device depends on which of the two memory connectors (primary vs seconday) the memory module is plugged into on the midplane.

2.4.4.3.1 I^2C Accessed Features

The memory module contains the following I^2C accessible devices:

- DS1624 - temperature sensor and SEEPROM containing FRU information
- PCF8574A - 8-bit I/O ports, which contain DIMM configuration information

These devices are accessed via the BMC on the I/O baseboard.   The I^2C devices are accessible at the following addresses:

Table 2-31: Memory Module I^2C Address Map

		I^2C Address	
Device	Function	Mem. Slot #1 (Primary)	Mem. Slot #2 (Secondary)
DS1624*	Memory module temperature sensor and FRU information	9Ah	9Eh
PCF8574A*	I/O port 0	70h	74h
PCF8574A*	I/O port 1	72h	76h

Note: The device addresses are different depending into which slot the memory module is plugged. The I^2C addresses are hard coded by the CPU baseboard.

2.4.4.3.1.1   DS1624* SEEPROM

The DS1624, when accessed via the I^2C bus, will provide the temperature of the module, as measured at the location of this device. The FRU information listed in Table 2-33 is read by the server management software, such as the Intel LANDesk Server Manager, and is available via the ISC.

Table 2-32: FRU Information Memory Module

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. Date/Time	Time and date of board manufacture (value programmed (in hex) is the number of minutes after 0:00 hrs. 1/1/96).	000f593h (Date/time translation shown below) f593h = 62867 min. = 43 days and 947 min. = Feb 12, 1996, 3:47 p.m.	2
Manufacturer	Board manufacturer	Intel	1
Board Product Name	Board name/description	Ak450NX 16-DIMM memory module	1
Board Serial Number	Intel board serial number	N42385906	2
Board Part Number	Intel board part number	667829-201	2

Notes: 1. Actual value programmed into the board.
2. Example value. Actual value will vary with each board and/or fab revision.

The DS1624 SEEPROM has 256 bytes of programmable space which is broken into four areas. Table 2-33 is a list of the areas with a description and the space allocated to each area.

Table 2-33: DS1624 SEEPROM Programming Areas

Area	**Size**	**Description**
Common Header	8 bytes	Programming offsets to the other areas below
Internal Use	48 bytes	Reserved for general purpose use by Intel server management firmware/controllers
Board Information	80 bytes	Contains the board FRU information listed in Table 2-32
Product Information	120 bytes	Available for OEM use[†]

[†] Documentation on how to program this area will be available at a later date.

Table 2-32 lists the board-specific FRU information that will be programmed into the board information area of the memory module EEPROMs.

Table 2-34 identifies exactly how bytes are allocated within the DS1624 SEEPROM. This information is useful for those who will be accessing the hardware directly for information (i.e., BIOS developers and server management software developers).

Table 2-34: SEEPROM EEPROM Byte Map: Memory Module

Address	**Length**	**Description**	**Default Value**
0x00	1	Common Header Format Version	0x01
0x01	1	Internal Use Area Offset (8-byte multiples)	0x01
0x02	1	Chassis Information Area Offset (8-byte multiples)	0x00 (area not present)
0x03	1	Board Information Area Offset (8-byte multiples)	0x05
0x04	1	Product Information Area Offset (8-byte multiples)	0x11
0x05	2	Zero Padding	
0x07	1	Common Header Checksum	0xE8

Address	Length	Description	Default Value
0x08	72	Internal Use Area	
0x38	1	Board Information Area Format Version	0x01
0x39	1	Board Information Area Length (8-byte multiples)	0x0A
0x3A	1	Unicode Country Base	0x00
0x3B	3	Manufacture Date/Time	
0x3E	1	Board Manufacturer Type/Length Byte	0xC5
0x3F	5	Board Manufacturer (ASCII)	'Intel'
0x44	1	Product Name Type/Length Byte	0xDC
0x45	28	Product Name	'Ak450NX 16-DIMM memory module'
0x61	1	Board Serial Number Type/Length Byte	0xCC
0x62	12	Board Serial Number	
0x6E	1	Board Part Number Type/Length Byte	0xCA
0x6F	10	Board Part Number	
0x79	1	No More Fields Flag	0xC1
0x7A	13	Zero Padding	
0x87	1	Board Information Area Checksum	
0x88	120	Product Information Area	

Temperature and EEPROM data may be accessed via I^2C commands to the DS1624 device. Table 2-35 is taken from the DS1624 data sheet.

Table 2-35: EEPROM Command Set

Instruction	Description	Command	2-Wire Bus Data After Issuing Command	Notes
Temperature Conversion Commands				
Read Temperature	Read last converted temperature value from temperature register.	AAh	<read 2 bytes data>	
Start Convert T	Initiates temperature conversion.	EEh	Idle	
Stop Convert T	Halts temperature conversion.	22h	Idle	
Memory Commands				
Access Memory	Reads or writes to 256-byte EEPROM memory.	17h	<write data>	
Access Config	Reads or writes configuration data to configuration register.	ACh	<write data>	

2.4.4.3.1.2   PCF8574A – 8 bit I/O Ports

The DRAM configuration data is provided by two Philips PCF8574A 8-bit I/O ports, also on the I^2C bus. These ports allow for the reading of the presence detect bits and ID bits of each DIMM, which contain information on module speed. This information is generally only useful to the BIOS. The individual bits of this port are defined as follows:

Table 2-36: I²C I/O Port Pin Definition

Port	Bit	Description
Port 0	P0	PDE (presence detect enable) address bit 0 (output only)
Port 0	P1	PDE address bit 1 (output only)
Port 0	P2	PDE address bit 2 (output only)
Port 0	P3	PDE address bit 3 (output only)
Port 0	P4	Reserved
Port 0	P5	DR50H pin on RCG (input only)
Port 0	P6	DIMM ID bit 0 (input only)
Port 0	P7	DIMM ID bit 1 (input only)
Port 1	P0	DIMM PD bit 1 (input only)
Port 1	P1	DIMM PD bit 2 (input only)
Port 1	P2	DIMM PD bit 3 (input only)
Port 1	P3	DIMM PD bit 4 (input only)
Port 1	P4	DIMM PD bit 5 (input only)
Port 1	P5	DIMM PD bit 6 (input only)
Port 1	P6	DIMM PD bit 7 (input only)
Port 1	P7	DIMM PD bit 8 (input only)

To read a particular DIMM's ID and PD bits, software must first write a 4-bit address to bits P0–P3 of Port 0. Once the write has taken place, software may read the ID bits from P6–P7 of Port 0 and P0–P7 of Port 1. Table 2-37 shows the mapping of PDE addresses to individual DIMMs.

Table 2-37: PDE Address Map

DIMM	Address	DIMM	Address
Bank A, Interleaves 0 (J1)	0x0	Bank A, Interleaves 2 (J3)	0x8
Bank A, Interleaves 1 (J2)	0x1	Bank A, Interleaves 3 (J4)	0x9
Bank B, Interleaves 0 (J5)	0x2	Bank B, Interleaves 2 (J7)	0xA
Bank B, Interleaves 1 (J6)	0x3	Bank B, Interleaves 3 (J8)	0xB
Bank C, Interleaves 0 (J9)	0x4	Bank C, Interleaves 2 (J11)	0xC
Bank C, Interleaves 1 (J10)	0x5	Bank C, Interleaves 3 (J12)	0xD
Bank D, Interleaves 0 (J13)	0x6	Bank D, Interleaves 2 (J15)	0xE
Bank D, Interleaves 1 (J14)	0x7	Bank D, Interleaves 3 (J16)	0xF

Table 2-38: PD and ID Bit Definition

PD Bits 5 4 3 2 1	Module Configuration	DRAM Organization	RAS/CAS Addressing	Normal/Slow Refresh Period (ms)
1 1 1 1 1	NO MODULE			
0 0 0 0 0	256Kx64/72,72	256Kx16/18	9/9	8/64
0 0 0 0 1	512Kx64/72,72	256Kx16/18	9/9	8/64
0 0 0 1 0	512Kx64/72, 72/80	512Kx8/9	10/9	16/128
0 0 0 1 1	1Mx64/72, 72/80	512Kx8/9	10/9	16/128
0 0 1 0 0	1Mx64/72, 72/80	1Mx1/4/16/18	10/10	16/128
0 0 1 0 1	2Mx64/72, 72/80	1Mx1/4/16/18	10/10	16/128

PD Bits 5 4 3 2 1	Module Configuration	DRAM Organization	RAS/CAS Addressing	Normal/Slow Refresh Period (ms)
0 0 1 1 0	1Mx64/72, 72	1Mx16/18	12/8	64/256
0 1 0 0 0	2Mx64/72, 72	1Mx16/18	12/8	64/256
0 1 0 0 1	2Mx64/72, 72/80	2Mx8/9	11/10	32/256
0 1 0 1 0	4Mx64/72, 72/80	2Mx8/9	11/10	32/256
0 1 0 1 1	4Mx72	4Mx1/4/8	$12^2/11^2$	64/256
0 1 0 1 1	4Mx64, 72/80	4Mx4/16	12/10	64/256
0 1 1 0 0	8Mx64/72, 72	4Mx16/18	12/10	64/256
0 1 1 0 1	8Mx64/72, 72/80	8Mx8/9	12/11	64/256
0 1 1 1 0	16Mx64/72, 72/80	8Mx8/9	12/11	64/256
0 1 1 1 1	16Mx64/72, 72/80	16Mx4	13/11	128/512
1 0 0 0 0	16Mx72, 72	16Mx16/18	TBD[1]/TBD[1]	TBD[1]/TBD[1]
1 0 0 0 1	32Mx72, 72	16Mx16/18	TBD[1]/TBD[1]	TBD[1]/TBD[1]
1 0 0 1 0	32Mx64/72, 72/80	32Mx8/9	TBD[1]/TBD[1]	TBD[1]/TBD[1]
1 0 0 1 1	64Mx64/72, 72/80	32Mx8/9	TBD[1]/TBD[1]	TBD[1]/TBD[1]
1 0 1 0 0	64Mx64, 72/80	64Mx4	TBD[1]/TBD[1]	TBD[1]/TBD[1]
X 0 1 1 1	EXPANSION			

Notes: 1. These modules using 256 MB devices are for reference only and will be further defined in the future.

         2. This addressing includes a redundant address to allow mixing of 12/10(x4) and 11/11(x1) DRAMs.

Table 2-39: DIMM Speed Definition

Speed	PD7	PD6		Config	PD8	ID0		Refresh Mode	ID1
80 ns	0	1		x64	1	0		Normal	0
70 ns	1	0		x72 Parity	1	1		Self-refresh	1
60 ns	1	1		x72 ECC	0	0			
50 ns	0	0		x80 ECC	0	1			

2.5　Midplane

This section describes the features of the Ak450NX midplane board. The midplane is used to provide distribution of 2-3 power supplies, and to perform data/control signal distribution among the board's that make up the Ak450NX board set.

Features

Power Distribution Subsystem:

- Power supply (PS) connectors (for 2 + 1 power supply, hot swap)
- Power distribution from power supplies to the memory module, CPU, and PHP I/O baseboards
- Bulk decoupling capacitors for 5 Vdc loads
- 3.3 Vdc and 5 Vdc margining circuit
- Peripheral power connector
- Alternating current (AC) input power checking
- Power supply on/off switching as controlled by front panel controller (FPC)

Non-power Subsystem Features:

- Data and control signal interconnects between the memory module, CPU, and PHP I/O baseboard
- I^2C server management bus for PS_Fault, Predictive_Fail, and PS_Present indicators
- Peripheral bay board I^2C server management interface

2.5.1　Placement Diagrams

The following diagrams were generated from the actual layout database and show the primary and secondary side components/connectors of the interconnect midplane. The diagrams also show the positions on the printed circuit board of the components/connectors. The table following each diagram identifies the major components using the reference designators to locate an item in the plot.
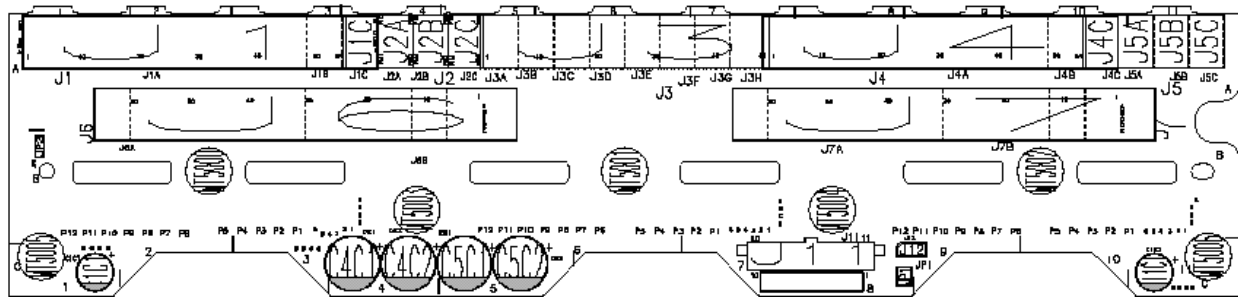
Figure 2-16:Placement Diagram (secondary side)

Table 2-40: Reference Designators (secondary side)

Reference Designator	Name and Description
J1	Grand connector for memory board 2
J2	Power from midplane to CPU and I/O baseboards
J3	F16 and server management connections for CPU, I/O, and midplane
J4	Grand connector for memory board 1
J5	Power from midplane to CPU and I/O baseboards
J6	Memory board 1 connector
J7	Memory board 1 connector
J11	Peripheral bay power and signal connector
J12	I^2C test connector
JP1	Force AC Okay jumper header
JP2	PS_PWR_ON test jumper header (not stuffed)

Note: The connectors divided by dashed lines can be assembled using standard submodules, or monoblock parts. The monoblock parts are preferred.
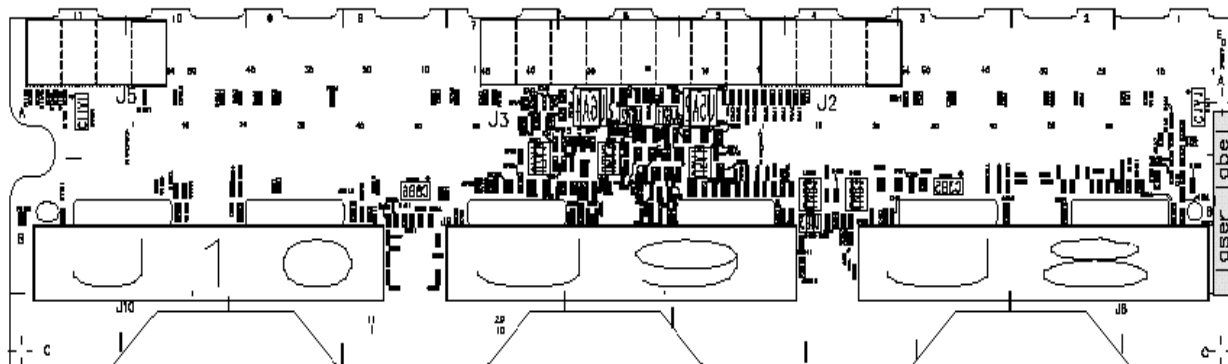
Figure 2-17:Placement Diagram (primary side)

Table 2-41: Reference Designators (primary side)

Reference Designator	Name and Description
J2	Power from midplane to CPU and I/O baseboards
J3	F16 and server management connections for CPU, I/O, and midplane
J5	Power from midplane to CPU and I/O baseboards
J8	Power supply 1 connector
J9	Power supply 2 connector
J10	Power supply 3 connector

2.5.2 Power Distribution Functions

The Ak450NX midplane has three power supply connectors which allow connection of up to three system power supplies. The midplane uses these power supply connections to distribute power to the remaining boards of the Ak450NX board set. The midplane also implements some active power control/status communication circuits that are used during power-up and by server management components of the board set. These power distribution functions are discussed in more detail in the the following sections.

2.5.2.1 Load Sharing

The Ak450NX midplane was designed with the expectations that any active forced load sharing functions would be implemented in the system power supplies. The midplane functions only to distribute the power to the loads and provide some additional decoupling capacitance to aid the power supply step load dynamic response. If the systen power supplies are designed to be hot swappable (the mating midplane connector is specified as such), then the power supply design must ensure that load redistribution and output voltage remain within regulation during a hot removal/insertion of a power supply. The power supply design should also be done such that remaining supplies are not subjected to loading beyond their rated capacity should a supply fail or be disconnected. The power supply output voltage and current requirements of the board set must always be met in order to guarantee proper operation of the Ak450NX board set. Output current is to be redistributed among remaining two supplies and must meet system requirements.

2.5.2.2 Power Distribution – Signal and Control Circuits

2.5.2.2.1 5 V Standby (VCC5STBY)

The power supplies provide a 5 V standby power source, pin #s B5 and B6 (P5V_STANDBY). VCC5STBY is a low power 5 Vdc supply that is active whenever the system is plugged into AC power. VCC5STBY is used in several places on the midplane, as follows: 5 V quick discharge circuit, I/O connector header J46 pin#A31/B32, power good circuit, and I²C bus circuits.

2.5.2.2.2 Power Supply Enable/Disable (PS_ON)

Also called Power_ON or PWR_ON_Supplies, this is a control signal which originates on the midplane and is connected directly to pin A5 of the power supply connectors (J8, J9, J10).

PS_ON is asserted (logic high) when signal PS_PWR_On (pin 13 of U7A1) coming from pin D15 of connector J3 (grand connector) is asserted (logic high), **and** at least two supplies have AC_OK_L asserted (logic low).   A special case is if the AC_OK test bypass jumper is installed, in which case PS_ON directly follows PS_PWR_ON.

PS_ON is deasserted (logic low) when signal PS_PWR_On (pin 13 of U7A1) coming from pin D15 of connector J3 (grand connector) is deasserted (logic low), **and/or** fewer than two supplies have AC_OK_L asserted.   As stated above, if the AC_OK bypass jumper is installed, PS_ON directly follows PS_PWR_ON.

Table 2-42: PS_ON Signal Logic Levels (PS Connector Pin 44)

PS_ON Signal	Voltage	Current
Asserted, Logic High, Power Supply Enabled	4 V min.	1.5 mA min. source to the power supplies
Deasserted, Logic Low, Power Supply Disabled	1 V max. or open circuit	0 mA

2.5.2.2.3   Remote Sense Circuit Connections

To maintain the power supply load regulation, voltage remote sensing is provided for the +3.3 Vdc, +5.0 Vdc, +12 Vdc and common ground return. Remote 12 V and 3.3 V sense points, as listed below, are located on the midplane in close proximity to the power section of the grand connector. The 5 V remote sense point is located on the I/O baseboard near the PCI slots. A secondary 5 V sense line is connected through a 100 Ω resistor and is located on the midplane. This is done to allow safe power regulation in the event that an I/O baseboard is not installed.

Table 2-43: Remote Sense Connections

Voltage	Remote Sense Resistor	Remote Sense Connection	PS Connector Pin (PS Signal)	Midplane Signal
3.3 V	R5B2	Buffered, individual for each PS	B3 (P3_3VSENSE)	PS1RS3, PS2RS3, PS3RS3
5 V	I/O	Buffered, individual for each PS	B4 (P5V_SENSE)	PS1RS5, PS2RS5, PS3RS5
12 V	R5A2	Direct, common for all three PS	C5 (P12V_SENSE)	12V_SENSE
GND	R5A4	Direct, common for all three PS	D5 (GS)	GND_SENSE

2.5.2.2.4   Power Good Circuit (PWR_GOOD) (Pin D2)

The PWR_GOOD, or power good signal functions originates on the midplane. The PGOOD signal of each power supply connector (J8, J9, J10) are OR'ed together and that signal inputs a control circuit, which generates a PWR_GOOD signal after a fixed delay of approximately 500 ms. This delay is provided to ensure a secure PWR_GOOD, even in case of a quick turn off/on of the front panel power on/off switch. The PWR_GOOD is asserted when at least one power supply's PGOOD is asserted, VCC5VSTBY is asserted, and 5V standby power is present. The delay for deassertion is less than 1 ms. The logic levels for the system PWR_GOOD signal are shown in Table 2-44.

Table 2-44: System PWR_GOOD Logic Levels

PWR_GOOD SIGNAL	VOLTAGE	CURRENT
Low state, deasserted	0.4 V max.	4 mA min. sink current.
High state, asserted	3.5 V min.	200 µA max. source current.

The PWR_GOOD will be deasserted when no power supply's PGOOD is asserted, and/or VCC5VSTBY is not present, and/or VCC5 is not present.

2.5.2.2.5   AC OK Circuit

This circuit is used as a brown-out protection function, where the midplane uses a signal, AC_OKAY, from the power supply connector, which indicates the power supply has valid AC input power and that it is safe to turn on that power supply. Without this signal, it is possible under a slow AC input voltage ramp (brown-out condition) that a single supply might attempt to turn on before other installed supplies. The logic of the AC_OKAY circuit requires that at least two supplies have indicated valid AC power and are both ready to turn on. The midplane AC OK circuit will disable system power according system and power supply designs that do not choose to implement this feature may disable it by jumpering the jumper block located at JP1. The power enable override conditions are listed in Table 2-45.

Table 2-45: Power Enable Override by AC OK Circuit

Number of Supplies Present	Number of AC_OK Asserted	POWER_ON_SUPPLIES
1	0	FORCED LOW
1	1	FORCED LOW
2	1	FORCED LOW
2	2	Unaffected
3	1	FORCED LOW
3	2	Unaffected
3	3	Unaffected

2.5.2.2.6   5 V Quick Discharge Circuit

The 5 V quick discharge circuit is provided to speed the discharge time of the +5 V supply voltage on power off. The main reason this circuit is implemented is because the 5 V power bus contains a large amount of decoupling caps which would otherwise take too long to discharge in case of a quick turn off and on. The quick discharge circuit intrudes a 5 Ω resistor to discharge the capacitance when power is turned off. During normal operation, the 5 Ω resistor is removed from the 5 V power bus.

2.5.2.2.7   PS Present (POWER_PRESENT, PSx_PRESENT)

Each power supply connector contains an input signal (Pin A2) that can be used by server management software to determine how many power supplies are installed. The midplane implements a pull up resistor on each of these signals. Should a system/power supply be designed to implement this feature, the power supply design should connect this pin internally to ground. This will allow server management to detect presence/absence of a power supply by reading the signal HIGH (supply not present) or LOW (supply is present).

2.5.2.2.8   PS Predictive Failure (PRED_FAIL_PSx)

Each PS connector implements a power supply predictive fail signal, PRED_FAIL_PSx (Pin C4), used to alert server management software in the event the PS is likely to fail (e.g., a poorly performing fan). If any of these signals is asserted, the midplane will not cause the PS to shut down, but it will communicate the alert via the server management I^2C bus.

2.5.2.2.9   Power Supply FAULT (PS_Fault)

A power supply fault indicator signal, PS_Fault, is available on each power supply connector (Pin C3). This signal is used to communicate power supply fault conditions to server management software. PS_FAULT is an output signal from each PS (connector pin C3). When asserted, logic HIGH, this signal indicates that the power supply is communicating its status as functional. When negated, logic LOW, the signal is communicating a failure of the supply. This signal is communicated to server management through the I^2C bus.

2.5.2.2.10   Power Supply Turn On Conditions

The logical relationship between signals PWR_GOOD, PRED_FAIL_PS, PS_FAULT, and POWER_ON is outlined in Table 2-46. The table shows the relationship between the previously described signals and the midplane's logic, which is used to turn on the supplies (assert PS_ON).

Table 2-46: PWR_GOOD, PRED_FAIL_PS, PS_FAULT, and POWER_ON Relationship

CONDITIONS	PWR_GOOD Output H = power good	PRED_FAIL_PSx Output H = pred. failure	PSx_FAULT Output H = PS OK	PS_ON PS Input (pin#A5) H = PS enabled
No AC power	L	L	L	L or H
AC in/stdby on	L	L	H	L
DC outputs OK	H	L	H	H
PS failure	L	L	L	H
Current limit	L	L	H	H
Predictive failure	H	H	H	H

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3. BIOS Features

This chapter describes the basic input output system (BIOS) embedded software, which is part of the Ak450NX server board set. The BIOS contains standard PC-compatible basic I/O services, plus Ak450NX system-specific hardware configuration routines and register defaults, embedded in flash ROM. The BIOS is implemented as firmware that resides in the flash ROM located on the PHP I/O baseboard. Support for I/O baseboard peripheral devices (SCSI or video adapters), which are also loaded into the baseboard flash ROM, are not specified here. Hooks are provided to support the addition of BIOS code for these adapters; the binaries must be obtained from the peripheral device manufacturers and loaded into the appropriate locations.

The BIOS features are grouped into several categories and are described in the following sections.

3.1   Ease-of-use Features

The following sections discuss the ease-of-use features of the Ak450NX BIOS.

3.1.1   Plug and Play

The Ak450NX BIOS supports the following industry standards for full Plug and Play (PnP) compatibility:

- *Plug and Play ISA Specification, Rev. 1.0a*
- *System Management BIOS (SMBIOS) Specification, Ver. 2.1*
- *Extended System Configuration Data Specification, Rev. 1.02A*
- *Peripheral Component Interconnect (PCI) Local Bus Specification, Rev. 2.1 (PCI Spec., Rev 2.1)*

Note: The Ak450NX BIOS does not support auto-detection of floppy-drive type, but IDE drives and floppy media are automatically detected.

3.1.2   Resource Allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Intel® servers. The BIOS scans for the following in the order listed:

1. **ISA devices.** If an ISA device is found, it is initialized and given resource priority over other devices of the same type, which are plugged into the system.
2. **Add-in PCI devices (e.g., PCI adapter cards).** If found, the BIOS initializes and allocates resources to these devices.
3. **Onboard video, IDE, and SCSI devices.** If equivalent functionality is not found offboard, the BIOS will allocate resources according to the parameters set up by the System Setup Utility (SSU). The add-in video adapter in the ISA bus or PCI bus 0 takes precedence over the onboard video controller.

3.1.3   PCI Auto-configuration

The Ak450NX BIOS supports the INT 1Ah, AH = B1h functions, in conformance with the *PCI Spec., Rev. 2.1*. System POST performs auto-detection and auto-configuration of ISA, ISA PnP, and PCI devices. This process maps each device into memory and/or I/O space, and assigns IRQs and DMA channels as required, so that there are no conflicts prior to booting the system. Drivers and operating system (OS) programs can determine the installed

devices and their assigned resources using the BIOS interface functions. In general, the PCI devices are scanned and initialized from low device number to high device number (and also low to high bus number) as shown below. However, scan and boot order may be affected by the implementation of the *BIOS Boot Specification, Ver. 1.01*. See *Section 3.5.1 Boot Device Selection and Ordering* in this chapter for further details.

Devices on the PCI bus are initialized in the following order:

1. On the primary 32-bit PCI bus [PXB0-A]:
    SLOT0 -> onboard SCSI -> SLOT1 -> onboard VIDEO
2. On the secondary 32-bit PCI bus [PXB0-B]:
    SLOT0 -> SLOT1 -> SLOT2 -> SLOT3
3. On the 64 bit PCI bus (third bus) [PXB1-A]
    SLOT0 -> SLOT1 -> SLOT2 -> SLOT3 -> SLOT4

Note the naming/numbering convention of the PCI buses attached to the host bus. The BIOS may enumerate the buses differently based on the type and number of PCI cards installed in the system. For example, if there are a number of cards with PCI-to-PCI bridges installed in the slots, it will affect the bus numbering, including the host PCI bus numbers. So, for clarity, we will refer to bus PXB0-A, bus PXB0-B, and bus PXB1-A when referring to the host PCI buses. An example of PCI bus enumeration follows.

Example 1:

If there were no PCI devices in any of the slots that had PCI-to-PCI bridges on them, the buses would be enumerated as follows:

Physical PCI Bus	Enumerated PCI Bus
0-A	0
0-B	1
1-A	2

Example 2:

If there were PCI devices in bus 0A and bus 0B that had PCI-to-PCI (P2P) bridges on them, the buses would be enumerated as follows:

Physical PCI Bus	Enumerated PCI Bus
0-A	0
P2P bridge on 0-A	1
0-B	2
P2P bridge on 0-B	3
1-A	4

The PCI interrupts are routed to ISA IRQs or IOAPIC through the PID ASIC. The PID supports IRQ map registers that are used to map PCI IRQ to ISA IRQ.

3.1.4   Legacy ISA Configuration

The SSU is provided to help the user configure the legacy ISA devices. The SSU allows the end user to reserve the legacy ISA system resource and save the information into extended system configuration data (ESCD) nonvolatile random access memory (NVRAM). The POST resource management will not allocate the resources that are reserved for legacy ISA cards to PnP devices.

3.1.4.1 Onboard Device Auto-configuration

The Ak450NX BIOS detects all onboard devices and assigns appropriate resources. The BIOS dispatches the option ROM code for the onboard devices to the DOS compatibility region (C0000h to DFFFFh) and transfers control to the entry point, if enabled by the user.

3.1.5 Automatic Detection of Video Adapters

The Ak450NX BIOS looks for video adapters in the following order:

1. ISA
2. PCI
3. Onboard, I/O baseboard

The onboard (or offboard) video BIOS is shadowed starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to add-in devices. Some video adapters request resources in the compatibility range. Only adapters on PCI bus 0-A, which are requesting compatibility resources, will be given the resources. Adapters that require compatibility resources cannot be placed on PCI bus 0-B or bus 1-A. Adapters behind a PCI-to-PCI bridge cannot request compatibility resources. Refer to *PCI Spec., Rev. 2.1* for the limitations.

A special VGA devnode option is provided in the BIOS setup to support PCI legacy VGA cards, which are not PCI 2.x compliant. When this option is enabled, the BIOS reserves up to 0x9000h address of I/O for Bus 0-A. This should be used for debug purposes only. By enabling this option, the user should be aware of the limitations of accommodating large I/O configurations on Bus 0-B and Bus 1-A.

3.1.6 Auto-detection of Processor Type and Speed

The Ak450NX BIOS automatically detects the processor stepping(s) installed in the system and configures the system accordingly. The BIOS detects the processor speed for all processors based on a jumper setting on the Ak450NX CPU baseboard. The BIOS displays the number of processors, and their speed prior to booting the operating system. It is preferred that all processors installed in a system be the same speed and same stepping; however, the BIOS allows the mixing of stepping under certain conditions. See *Section 3.2.2.1 Multiple Processor Speed Support* in this chapter for more details.

3.1.7 Mouse and Keyboard Port Swapping

The Ak450NX BIOS allows users to plug the keyboard or PS/2 mouse connectors into either PS/2 port on the I/O riser card. It detects and initializes the keyboard and mouse accordingly.

3.1.8 Memory Sizing

During POST the BIOS:

- Tests and sizes memory
- Configures the memory controller

The memory-sizing algorithm determines the size of each row of DIMMs. The BIOS always initializes ECC memory. The BIOS is capable of detecting, sizing, and testing any amount of RAM, up to the physical maximum of 8 GB. The BIOS is capable of reporting up to 64 MB using INT 15h, AX = 88h. It can report up to 4 GB using INT 15h, function E801h. Using INT 15h, function E820h, the BIOS can report system memory regions up to the physical maximum of 8 GB.

The Ak450NX BIOS reclaims all the memory lost due to PCI allocation, APIC and BIOS flash region, if there is more than 4 GB of system memory. The BIOS supports full remapping and 2/4 way ABP. The BIOS also provides a setup option to select memory testing every DWORD, a DWORD every KB or a DWORD every MB. Selecting memory testing a DWORD every MB increases the boot speed. The ABP feature can be disabled using the BIOS Setup.

3.1.9   LCD Display

The Ak450NX BIOS supports a front panel LCD for the display of informative messages. During POST the BIOS displays memory sizing information, BIOS revision information, cache size, keyboard and mouse presence, and POST error codes.

3.1.10 Boot Delay

The boot delay feature can be selected from setup through the advanced options menus. It provides a five second delay towards the end of POST. Its purpose is to allow the user to view all messages displayed by the BIOS during POST.

3.1.11 I$_2$O Support

Intelligent I/O (I$_2$O) defines a standard architecture for intelligent I/O, an approach to I/O in which low level interrupts are off loaded from the CPU to I/O processors (IOP). IOPs are designed specifically to handle I/O with support for message passing between multiple independent processors. The Ak450NX BIOS supports run-time services for I$_2$O devices.

3.1.12 ACPI Support

The advanced configuration and power interface (ACPI) specification is the key element in Operating System Directed Power Management (OSPM). The OSPM provides support for an orderly transition from existing (legacy) hardware to ACPI hardware. The ACPI interface gives the OS direct control over the power management and plug and play functions of the computer.

Ak450NX BIOS supports S1 Sleeping State & S4 Sleeping State. The power button and Power Management Event (PME) WakeOnLan (WOL) can wake from S1. Until an OS sends a command to SWITCH TO ACPI Mode, the power button acts as a power switch. While entering ACPI mode, the BIOS communicates with the front panel controller to switch into ACPI mode. In this mode, the power button acts as both a sleep button and a power button. If the power button is pressed momentarily (less than 4 sec) the PIIX4E treats it as a sleep button and informs the OS/AML (ACPI machine language) to switch to S1 state. If the power button is pressed for more than 4 seconds, it is treated as a power cycle and the system is powered down. The power button can also be configured via the OS to enter hibernation.

3.1.12.1   Implementation Details Of S1 Sleep State

S1 sleep state can be entered by pressing the power button or by direction from the OS. In this state no system context is lost, including CPU, caches, memory and all chip set I/O. Momentarily pressing the power button wakes the system from S1 state. The PME WOL feature of the Ak450NX is implemented only for S1 state.

3.1.12.2   Implementation Details Of S4 Sleep State

The S4 sleeping state is the lowest power, longest wakeup latency sleeping state supported by ACPI. State S4 is also called SaveToDisk (STD). This state can be entered either by pressing the power button, if the power button is configured for hibernation under the OS, or from the hibernate option in OS shut-down menu. If this state is invoked, the OS will store to the hard drive the context of all processes such as applications, memory, chip set, and processor, and then it will power down the system. When system power is reinitiated, the OS restores all the processes from the disk including the launching of all of the applications.

3.2   Performance Features

For enhanced performance, the Ak450NX BIOS supports the features discussed in the following section.

3.2.1   Symmetric Multiprocessor Support

The Ak450NX BIOS complies with all requirements of the *Intel*® *Multiprocessor Specification (MPS), Version 1.4*, for symmetric multiprocessing support, as well as *Intel*® *Multiprocessor Specification (MPS), Version 1.1*, for backward compatibility. The version number can be configured using the Configuration Utility (CU).

3.2.2   Multiple Processor Support

On reset, all the processors compete to become the bootstrap processor (BSP). If a serious error is detected on a processor during built-in-self-tests (BIST), that processor does not participate in the initialization protocol. The first processor (typically with the highest APIC ID) that successfully passes BIST is automatically selected by the hardware as the BSP and starts executing from the reset vector (F000:FFF0h). A processor that does not perform the role of BSP is referred to as an application processor (AP).

The BSP is responsible for executing the POST and preparing the machine to boot the OS. The Ak450NX BIOS performs several other tasks in addition to those required for MPS support, as described in the *Intel*® *Multiprocessor Specification (MPS), Version* 1.4. These tasks are part of the fault resilient booting algorithm. At the time of booting, the system is in virtual wire mode and the BSP alone is programmed to accept local interrupts (INTR driven by the programmable interrupt controller (PIC) and the nonmaskable interrupt). As a part of the boot process, the BSP wakes up the application processors (Aps). When awakened, the APs program their memory type range registers (MTRR) to be identical to those of the BSP. All APs execute a halt instruction with their local interrupts disabled.

3.2.2.1   Multiple Processor Speed Support

The Ak450NX BIOS supports processors with various clock frequencies without changes to the BIOS, but only across different system configurations. All installed processors in any one system must run at the same frequency (i.e., the bus and core frequencies of all processors must be the same). This is guaranteed by a jumper setting on the CPU baseboard, which programs the core to bus frequency ratio for all processors in the system.

Though Intel recommends using identical stepping of processor silicon in multiprocessor systems whenever possible (as this is the only configuration that receives full validation across all of Intel's testing), the BIOS does support mixing processor stepping. However, the support of mixed stepping will be limited to those steppings that do not have known incompatibilities. Typically, each new stepping of a device is fully validated only against the latest stepping of other processors and chip set components.

The Ak450NX BIOS does not support mixing processor cache sizes. The BIOS reports and logs an error for mixed stepping.

3.2.3   Cache

By default, the Ak450NX BIOS enables the L1 and L2 caches to write-back mode for all main system memory. The system shadow memory is initialized to be cached but write protected. In this case, it will not generate memory write cycles, which may destroy the shadow memory or cause a bad cycle.

Some video memory buffers can be initialized with uncacheable-speculative-write-combining (USWC) memory attribute, which combines the line memory cycle into a burst memory cycle to speed up video buffer performance. All other memory outside of the main system memory is initialized as not cacheable.

3.2.4   Memory Speed Optimization

The memory DIMM speed is obtained from server management via the BMC private management bus. The default memory DIMM speed is 60 nanoseconds (ns). Therefore, if memory DIMM speeds are mixed, or if the speed of all the DIMMs is 60 ns, the speed setting remains at the slower default value of 60 ns. If, however, the memory speed of **all** DIMMs is found to be 50 ns, the Ak450NX BMC program resets the DIMM speed to 50 ns.

3.2.5   Option ROM Shadowing

All onboard adapter ROMs and PCI adapter ROMs are shadowed into RAM in the ISA-compatible ROM adapter memory space between C0000h to DFFFFh. Cacheable BIOS ROMs found on ISA devices are shadowed into adapter memory space in the same range after initialization. PCI BIOS ROMs are always shadowed. The memory hole from 15 MB-16 MB will not be supported by the BIOS.

3.3   Security Features

The Ak450NX BIOS provides a number of security features. This section describes the security features and operating model. Some of these events, such as entering secure mode via a hot key, cannot take place unless the keyboard is connected to the keyboard controller (KBC), and will not be supported when the keyboard is connected to a USB port.

3.3.1   Operating Model

Table 3-1 summarizes the operation of security features supported by the Ak450NX BIOS.

Table 3-1:   Security Features Operating Model

Mode	Entry Method/Event	Entry Criteria/Qualifier	Behavior	Exit Criteria	After Exit
Secure mode	Keyboard inactivity timer; programming of KBC hot key	User password/ KBC inactivity timer (set by CU)	• Screen goes blank (if enabled in Setup) • Floppy writes are disabled (if selected in Setup) • Power and reset switches on front panel are disabled • No mouse or keyboard input is accepted	User password	• Video is restored • Floppy writes are enabled • Power and reset switches are enabled • Keyboard and mouse inputs are accepted
Secure boot	Power On/Reset	User password/ secure boot enabled in CU	• Boots drive C: if drive A is empty • Prompts for password, if drive A is not empty • Video is blanked (if enabled in Setup) • Floppy writes are disabled (if selected in Setup) • Power and reset switches on the front panel are disabled • No mouse or keyboard input is accepted	User password	• Floppy writes are enabled • Power and reset switches are enabled • Keyboard and mouse inputs are accepted • System attempts to boot from drive A
User password boot (AT style)	Power On/Reset	User password/ secure boot disabled in CU	• System halts for user password before booting • Video is blanked (if enabled in Setup) • Floppy writes are disabled (if selected by Setup) • Power and reset switches on the front panel are disabled • No mouse or keyboard input is accepted.	User password	• Power and reset-switches are enabled • Keyboard and mouse inputs are accepted • Boot sequence is determined by Setup options
Power and reset switch lockout	Same as secure mode above	User-programmed option (using Setup)	Power and reset buttons are disabled on front panel	User clears option	Power and reset switches enabled

3.3.2   Password Protection

Through the use of passwords, BIOS prevents unauthorized tampering with the system. Once secure mode is enabled, access to the system is allowed only after the correct password(s) is entered. Each of two passwords, for user and supervisor, can be created during system configuration using the ROM based Setup Utility.

If only a user password is set (no supervisor password), this password is the only one required to boot the machine or run Setup. If both passwords are enabled, either password can be used to boot the machine or enable the keyboard and/or mouse, but only the supervisor password allows the system configuration to be changed using Setup.

The supervisor password is provided as a means to control access to the basic system configuration independently of other access controls. For example, the system hardware configuration can be controlled by a supervisor while others control access to the machine's file system.

Once set, a password can be disabled by deleting it in Setup or by setting the Clear Password jumper on the I/O baseboard.

3.3.3   Inactivity Timer

If the inactivity timer function is enabled, and no keyboard or mouse actions have occurred for the specified time-out period, the following occurs until the user password is entered:

- Keyboard and mouse input is inhibited
- Video is blanked (if programmed in CU)
- Floppy drive is write protected (if enabled)
- Front panel buttons locked out (if enabled)

Using the CU, the user may specify a time-out period of 1 to 120 minutes.

3.3.4   Hot Key Activation

A hot key can activate secure mode immediately, rather than having to wait for the inactivity time-out to expire. The hot key combination is set using the CU.

3.3.5   Password Clear Switch

The BIOS reads the password clear switch (located on the I/O baseboard) to determine if it is set. If set, both user and administrator passwords are cleared from CMOS and password protection is disabled.

3.3.6   Boot Without Keyboard

The system can boot with or without a keyboard. The BIOS displays whether it detected a keyboard or not before booting. There is no entry in the CU for keyboard enable/disable. The presence of the keyboard is detected automatically during POST, and the keyboard is tested if present.

3.3.7   Floppy Write Protection

If enabled in Setup, floppy disk writes are disabled when the system is in secure mode. Floppy write protection is only in effect while the system is in secure mode. Otherwise, write protection is disabled.

3.3.8   Front Panel Lock

If front panel lock is enabled in Setup, the front panel, power switch and reset button, are disabled when in secure mode.

3.3.9 Secure Boot Mode

Secure boot mode lets the system boot and run the OS, but no mouse or keyboard input is accepted until the user password is entered. Setup is used to enable the secure boot mode feature. In secure boot mode, if the BIOS detects a floppy disk in the A drive at boot time, it prompts the user for a password. When the password is entered, the system can boot from the floppy and secure mode is disabled. Any one of the secure mode triggers, as described in Table 3-1 will cause the system to go back into secure mode. If there is no disk in drive A, the system boots from the C: drive and is placed in secure mode automatically. All of those secure mode features which are enabled go into effect at boot time.

3.3.10 Video Blanking

If enabled in Setup, the video display will be off when the system is in secure mode. Exiting secure mode will enable the video display. While the video is blank, the user must enter the password to exit secure mode.

3.4 Reliability Features

The Ak450NX BIOS supports several features to create a robust computing environment. These features are described in the following sections.

3.4.1 Defective DIMM Detection and Remapping

The ECC memory subsystem on the Ak450NX board set is able to detect single-bit errors (SBE) and multi-bit errors (MBE) during reads from and writes to system DRAM. SBEs can be detected and corrected, whereas MBEs can be detected but cannot be corrected.

During POST memory testing, detection of single-bit and multi-bit errors in DRAM banks is enabled. If an error is detected during POST, the bad location is avoided by reducing the usable memory in that bank so that the byte containing the hard error is no longer accessible.

Depending on where exactly the error is, BIOS divides down the bank size by 2, thereby lowering the top of the bank until the failing location is above the newly lowered top of bank. This continues until a worst case bank size of 0 is reached. With a max of 1 GB supported per bank, the minimum loss per bank will be 512 MB and the maximum will be 1 GB per bank.

The defective DIMM detection and memory remapping is done automatically by the BIOS during the POST and does not require any user intervention. The BIOS logs the errors in the nonvolatile system event log.

DIMM speed is programmed by the BMC firmware.

3.4.2 Memory Configuration Algorithm

BIOS requires at least 64 MB of good memory to start up. If there is no DIMM population or all DIMMs are bad, the BIOS sounds a beep code error (1-3-3-1) and POST is terminated.

It should be noted that during this memory size detection process, the BIOS does not distinguish between absent DIMMs and bad DIMMs. Although single-bit errors are correctable errors, they are considered serious enough to remove the entire bank altogether. This bank removal process continues iteratively for all banks until the BIOS finds at least 64 MB of memory good in one bank, or if all banks have been removed, it emits the 1-3-3-1 beep code and

halts the system. A bank is removed if any of the four DIMMs that make up the bank have any error, single or multiple bit.

In the event that the BIOS disables or resizes a bank during POST, an error message displays with the DIMM and board numbers of the failing memory. Elimination of hard errors in this way during POST is done as a precaution to prevent an SBE from becoming an MBE after the system has booted and to prevent SBEs from being detected and logged each time the failed location(s) are accessed.

DIMM resizing during POST comes with a restriction. If ABP and/or C2C interleaving have been turned on, resizing is not possible. However, error messages are still displayed at the end of POST, and errors are still logged.

After POST memory testing, automatic scrubbing of SBEs is enabled in the MIOC. If an error is a single-bit error, the 450NX automatically corrects the data before it is returned. If the error is an MBE, the condition is considered fatal and, after the error is logged, an NMI is generated telling the OS to handle this fatal error.

3.4.3   Logging Critical Events

If enabled by the CU, the Ak450NX BIOS has the ability to log critical and informational events to nonvolatile memory. The event log area is managed by the BMC and can be accessed by sending IPMB commands to the BMC. A critical event is one that may result in the system being shut down to prevent catastrophic side effects from propagating to other parts of the system. Multi-bit and parity errors in the memory subsystem are considered critical errors, as are bus errors, and most errors that generate a nonmaskable interrupt (NMI), which may subsequently generate an SMI. These errors include I/O channel check, software generated NMI, and PCI system error (SERR) and parity error (PERR) events.

3.4.4   CMOS Default Override

The BIOS detects the state of the CMOS default switch (configuration jumper on the I/O baseboard). If set to **CMOS Clear** prior to power on or hard reset, the BIOS changes CMOS and NVRAM settings to a default state with no exceptions, which guarantees the system's ability to boot from floppy. Password settings are unaffected by CMOS clear.

The BIOS does not clear the ESCD parameter block.

If the CMOS clear jumper is not set, ISA NVRAM still may be cleared if:

- the ISA NVRAM does not checksum to zero; or
- setting the Reset System Configuration Data field to "Yes" in Setup clears the ESCD.

3.4.5   BIOS Recovery Mode

In the case of a corrupt BIOS or an unsuccessful update of the system BIOS, the Ak450NX can boot in recovery mode. It requires that drive A: be setup to support a 3.5" 1.44 MB floppy drive. This is the mode of last resort, used only when the main system BIOS will not come up. In recovery mode operation, iFLASH (in noninteractive mode only) automatically updates only the main system BIOS. iFLASH senses that the system is in recovery mode and automatically attempts to update the system BIOS.

Before powering up the system, move the BIOS recovery jumper to the recovery state. Moving the recovery jumper causes the recovery BIOS (also known as boot block) to be executed instead of the normal BIOS. The recovery BIOS is a self-contained image that exists solely as a fail-safe mechanism to flash in a new BIOS image. Obtain a bootable DOS-compatible diskette that contains a copy of the BIOS release. Boot the system from the A: drive using

this diskette, which executes a special AUTOEXEC.BAT file from the BIOS release. The batch file invokes iFLASH, which updates the flash ROM with the BIOS found on the diskette.

NOTE: **During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes between two and four minutes. A successful update ends with two high-pitched beeps. A failure is indicated by a long series of short beeps.**

If a failure occurs, it is most likely that one or more of the system BIOS iFLASH files is corrupt or missing. After a successful update, power down the system and move the recovery jumpers to the default position. Power up the system and verify that the BIOS version number matches the version of the entire BIOS that you originally attempted to update.

CMOS is not cleared when the system BIOS is updated. Remember that any additional or different languages that were present before updating will need to be reloaded to flash.

3.5   Boot Features

The Ak450NX BIOS identifies all initial program load (IPL) devices in the system and attempts to boot from them in the order specified in Setup. IPL devices include the BIOS Aware IPL Device (BAID) as well as PnP cards containing an option ROM. The Ak450NX BIOS supports the *BIOS Boot Specification, 1.01* (BBS).

3.5.1   Boot Device Selection and Ordering

By adhering to the *BIOS Boot Specification, 1.01.* the Ak450NX BIOS gives the user the ability to order the list of boot devices, via the boot menu in the flash-resident setup utility. All boot devices are detected and listed. The user can choose the order of the devices from which the machine attempts to boot. This list is maintained until the user changes it again in setup or, overrides it during POST by pressing the <ESC> key and selecting a new boot device from the list of available devices.

By pressing <ESC> during POST, users have the option of overriding the boot sequence specified in setup by selecting a different primary boot device. This override is valid only for that specific boot. Subsequent boots will revert back to the order specified in setup. If the chosen device fails to load the operating system, the BIOS reverts to the previous boot sequence. The <ESC> hot key is valid while the "Press <F2> key to enter Setup" message is displayed at the bottom of the screen. At the end of POST, if the <ESC> key was pressed, a popup boot menu is displayed to allow the user to change the boot device choice, or to enter Setup and permanently change the boot order.

The system boots in the order chosen by the user, with the exception of legacy devices. Legacy devices are those devices that tend to take control of the boot process altogether by hooking the boot vector (interrupt 19h). Further, they provide no means for identifying themselves as an IPL device. Therefore, the BIOS cannot selectively boot from one of several legacy IPL devices in a system. The current implementation of the BBS supports up to eight devices. If greater than eight devices are present in the system configuration, the user should disable the multiboot option in Setup. If a BBS compliant adapter controls a number of drives that cause the eight-device limit to be exceeded, the multiboot option must be disabled.

3.5.2   PnP Option ROM Support

Bootable PnP cards containing an option ROM are supported. There are two varieties of PnP cards. One variety is the boot connection vector (BCV) devices such as SCSI hard drives. The other variety is the bootstrap entry vector (BEV) devices such as a PnP ISA Ethernet controller. BCVs generally install themselves into the INT 13h services by hooking INT 13h, while BEVs do not. The BIOS supports both BCVs and BEVs.

3.6 Console Redirection

The BIOS supports redirection of both video and keyboard via a serial link (COM1 or COM2). When console redirection is enabled, local (host server) keyboard input and video output is passed both to the local keyboard and video connections, and to the remote console via the serial link. Keyboard inputs from both sources are considered valid and video is displayed to both outputs. Optionally, the system can be operated without a host keyboard or monitor attached to the system and run entirely via the remote console. Only text-based programs such as flash-resident Setup can be accessed via console redirection.

3.6.1 Operation

When redirecting through a modem (as opposed to a null modem cable), the modem needs to be configured with:

- auto-answer (e.g., ATS0=2 to answer after 2 rings)
- modem reaction to DTR set to return to command state (e.g., AT&D1)

Failure to provide the second configuration above causes the modem either to drop the link when the server reboots (as in AT&D0), or make the modem unresponsive to server baud rate changes (as in AT&D2).

The setup option for handshaking must be set to CTS/RTS + CD. CD refers to carrier detect. In selecting this form of handshaking, the server is prevented from sending video updates to a modem that is not connected to a remote modem. If this is not selected, video update data being sent to the modem will inhibit many modems from answering an incoming call.

When console redirection is selected via the setup, redirection is loaded into memory and activated during POST. While redirection cannot be removed without rebooting, it can be inhibited and restarted. When inhibited, the serial port is released by redirection and may be used by another application. Restarting will reclaim the serial port and continue redirection. Inhibiting/restarting is accomplished through the following INT 16h mechanism. The standard INT 16h (keyboard handler) function ah=05h places a keystroke in the key buffer, just as if an actual key had been pressed. Keystrokes so buffered are examined by redirection, and if a valid command string has been sent, it is executed. The following commands are supported in this fashion:

- Esc-CDZ0 - Inhibit Console Redirection.
- Esc-CDZ1 - Restart Console Redirection.

In order to inhibit redirection, the software must call INT 16h, function ah=05h five times to place the five keys in the key buffer. Keystrokes sent to the INT 16h buffers for purposes of invoking a command <u>are</u> buffered, and should be removed via the normal INT 16h calls to prevent these keystrokes from being passed on to another application.

3.6.2 Keystroke Mappings

During console redirection, the **remote** terminal (which may be a dumb terminal or a system with a modem running a communication program) sends keystrokes to the **local** server. The **local** server passes video back over this same link.

For keys that have an ASCII mapping, such as A and Ctrl-A, the remote simply sends the ASCII character. For keys that do not have an ASCII mapping, such as F1 and Alt-A, the remote must send a string of characters as defined in Table 3-2. The strings are based on the American National Standards Institute (ANSI) terminal standard. Since the ANSI terminal standard does not define all the keys on the standard 101 key U.S. keyboard, mappings for these keys (e.g., F5 - F12, Page Up, and Page Down) were created.

Alt key combinations are created by sending the combination **^[}** followed by the character to be alt modified. Once this alt key combination is sent (^[}), the next keystroke sent will be translated into its alt key mapping (i.e., if ^[} is mapped to Shift-F1, then pressing Shift-F1 followed by 'a' would send an Alt-a to the server).

The remote terminal can force a refresh of its video by sending **^[{**.

Presently, unusual combinations outside of the ANSI mapping and not in Table 3-2 are not supported (e.g., Ctrl-F1).

Table 3-2:   Non-ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
ESC	^[	NS	NS	NS
F1	^[OP	NS	NS	NS
F2	^[OQ	NS	NS	NS
F3	^[OR	NS	NS	NS
F4	^[OS	NS	NS	NS
F5	^[OT	NS	NS	NS
F6	^[OU	NS	NS	NS
F7	^[OV	NS	NS	NS
F8	^[OW	NS	NS	NS
F9	^[OX	NS	NS	NS
F10	^[OY	NS	NS	NS
F11	^[OZ	NS	NS	NS
F12	^[O1	NS	NS	NS
Print Screen	NS	NS	NS	NS
Scroll Lock	NS	NS	NS	NS
Pause	NS	NS	NS	NS
Insert	^[[L	NS	NS	NS
Delete	(7Fh)	NS	NS	NS
Home	^[[H	NS	NS	NS
End	^[[K	NS	NS	NS
Pg Up	^[[M	NS	NS	NS
Pg Down	^[[2J	NS	NS	NS
Up Arrow	^[[A	NS	NS	NS
Down Arrow	^[[B	NS	NS	NS
Right Arrow	^[[C	NS	NS	NS
Left Arrow	^[[D	NS	NS	NS
Tab	(09h)	NS	NS	NS

NS = Not supported, (xxh) = ASCII character xx

Table 3-3:   ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
backspace	(08h)	(08h)	(7Fh)	^[}(08h)
(accent) '	'	(tilda) ~	NS	^[}'
1	1	!	NS	^[}1
2	2	@	NS	^[}2
3	3	#	NS	^[}3

Key	Normal	Shift	Ctrl	Alt
4	4	$	NS	^[}4
5	5	%	NS	^[}5
6	6	^	NS	^[}6
7	7	&	NS	^[}7
8	8	*	NS	^[}8
9	9	(	NS	^[}9
0	0	)	NS	^[}0
(dash) -	-	(under) _	(1Fh)	^[}-
=	=	+	NS	^[}=
a to z	a to z	A to Z	(01h) to (1Ah)	^[}a to ^[}z
[	[	{	(1Bh)	^[}[
]	]	}	(1Dh)	^[}]
\	\	|	(1Ch)	^[}\
(semi-colon) ;	;	(colon) :	NS	^[};
(apostrophe) '	'	(quote) "	NS	^[}'
(comma) ,	,	<	NS	^[},
(period) .	.	>	NS	^[}.
/	/	?	NS	^[}/
(space)	(20h)	(20h)	(20h)	^[}(20h)

NS = not supported, (xxh) = ASCII character xx

3.6.3   Limitations

Console redirection is a real mode BIOS extension and does not operate outside of real mode. Console redirection will not work once the operating system or a driver like EMM386 takes the processor into protected mode. If an application takes the processor in and out of protected mode, it should inhibit redirection before entering protected mode and restart it once back into real mode. Video is redirected by scanning and sending changes in text video memory. Thus, console redirection is unable to redirect video in graphics mode. Keyboard redirection functions via the BIOS INT 16h handler. Software bypassing this handler will not receive redirected keystrokes.

3.7   DMI Support

The main component of the desktop management interface (DMI) is the management information format (MIF) database. This database contains all of the information about the computing system and its components. Using DMI, a system administrator can obtain the types, capabilities, operational status, installation date, and other information about the system components.

The Ak450NX BIOS complies with *System Management BIOS (SMBIOS) Specification, 2.1,* and implements all mandatory function calls. The SMBIOS follows the System Device Node model used by PnP, and uses PnP BIOS functions to access SMBIOS information. PnP functions 50h-5Fh are assigned for SMBIOS interface. Each of the SMBIOS PnP functions is available in both real mode and 16-bit protected mode. General purpose nonvolatile (GPNV) storage as defined in the *System Management BIOS (SMBIOS) Specification, 2.1,* will be provided. The total size of the GPNV storage area is at least 128 bytes. The exact size depends upon availability of nonvolatile memory. A handle parameter is passed into GPNV function calls to specify which GPNV area is to be accessed.

The BIOS also constructs a table containing DMI information in shadow memory so that it is available to the drivers that require this information without performing BIOS calls.

The SMBIOS structure table is broken into two parts:

- SMBIOS entry point header structure
- SMBIOS structure table

The SMBIOS entry point header structure can be found in the 0F0000h to 0FFFFFh physical address area of memory and is paragraph (16 byte) aligned.

Table 3-4:   SMBIOS Header Structure

ELEMENT	LENGTH	DESCRIPTION
Header	5 Bytes	_DMI_
Checksum	1 Byte	Checksum of SMBIOS header structure
Length	2 Bytes	Total length of SMBIOS structure table
BIOS Structure Table Address	4 Bytes	32-bit physical address of beginning of byte aligned DMI structure table
NumStructures	1 Byte	Total number of structures within the DMI structure table
DmiBIOSRevision	1 Byte	Revision of the SMBIOS extensions

The SMBIOS structure table contains all of the SMBIOS structures fully packed together. The structures in this table can be parsed out and would be in the exact format returned by the SMBIOS extension function 51h, *GetDmiStructure*. This table is static. The BIOS will create this table before passing control to the OS, but it does not update the table while the OS is running, even if there are configuration changes. The *System Management BIOS (SMBIOS) Specification, 2.1,* describes the format of the SMBIOS structure table. Additionally, the Ak450NX BIOS supports GPNV areas as required by the manufacturing process.

The following are SMBIOS types supported by the Ak450NX BIOS.

Type 0: 1 for the system BIOS, 1 for video BIOS and 1 for SCSI BIOS
Type 1, Type 2, Type 3, Type 4, Type 5, Type 6, Type 7, Type 8, Type 9, Type 10, Type 11, Type 12, Type 13, Type 16 and Type 17.

3.8   USB Support

A USB-aware OS will enable the USB functionality and can make use of USB devices. The Ak450NX BIOS does not provide legacy support for the USB keyboard and mouse.

USB devices can resume the system from an ACPI S1 state. USB devices cannot wakeup a system from an S4 state.

3.9   PCI Hot-plug Support

The Ak450NX BIOS supports like-for-like replacement of PCI add-in cards on its four 64-bit PCI slots, power to which is controlled by the PHP controller. During POST, power to these four slots is turned on by writing appropriate commands to the PHP controller. Bus enumeration and resource allocation proceed normally, and the hot-plug slots appear to be ordinary 64-bit PCI slots to any software component that is hot-plug unaware. However, replacement of a failed card with an exactly identical card is done by a software stack that is aware of the hot-plug functionality. The system BIOS plays no part in this operation. *At the time of this publication, hot-add or hot-upgrade functionality are not supported on the Ak450NX board set.*

Each hot-plug PCI slot on the Ak450NX I/O board has a switch beside it which is closed (making contact) when a PCI plug-in card is in the corresponding PCI slot. During POST, the PCI hot-plug controller is programmed to turn on power to all hot-plug slots. However, only those slots whose switches are closed are powered up. The BIOS may override this, depending upon the user's choice in the CMOS setup, by means of the GPIO22 pin of the SMC Super I/O controller on the I/O board, which causes all slots to power up unconditionally.

3.10 Configuration Utility (CU)

The Configuration Utility (CU) provide the means to configure onboard resources and add-in cards. The utilities are provided in two forms: the System Setup Utility (SSU) and the Flash-resident Setup Utility.

Configuration of onboard devices is done using the Setup Utility embedded in flash ROM. Setup provides enough configuration functionality to boot a system diskette or other media such as a CD-ROM, which are shipped with the hardware that contains the SSU. The SSU is required for configuration of PCI and ISA add-in cards. The SSU is released on diskette or CD-ROM. Setup is always provided in flash memory for basic system configurations.

SSU is PCI-aware and conforms to the *Plug and Play ISA Specification,Ver. 1.0a*. The SSU works with any compliant **.**CFG or **.**OVL files supplied by the peripheral device manufacturer. Intel supplies only the **.**OVL and **.**CFG files for the system baseboard.

The configuration utilities modify the CMOS RAM and NVRAM, under direction of the user. The actual hardware configuration is accomplished by the BIOS POST routines and the PnP Auto-configuration Manager. The configuration utilities always update a checksum for both areas, so that any potential data corruption is detectable by the BIOS before hardware configuration takes place. If the data is corrupted, the BIOS requests that the system be reconfigured before it is rebooted.

If the disk-based SSU is used, a logo is automatically displayed before the SSU is executed. The logo can be customized by an OEM.

Refer to the *AC450NX Server System Product Guide (Intel Part #678269-002)* for details on when to use the configuration utilities and the options available to the user for system configuration.

3.11 Flash Update Utility

iFLASH loads a fresh copy of the system software, including system BIOS, into flash ROM. The loaded code and data include the following:

- Onboard video BIOS and SCSI BIOS
- Setup Utility
- User Binary Area

When running iFLASH in interactive mode, the user may choose to save, update, or verify a particular flash area. Saving a flash area takes a mirror image of the specified flash area and copies it to a file or series of files on hard or floppy disk. Updating a flash area takes a file or series of files from hard or floppy disk, and loads it in the specified area of flash ROM. Verifying a flash area compares an existing flash area against a file or series of files on hard or floppy disk. The primary purpose of iFLASH is to reprogram the flash area. Future versions may not support verification and save operations. In interactive mode, iFLASH can display the header information of selected files.

NOTES: The flash-resident setup field in System Management Mode is located on the Server Menu. This field must be **enabled** for iFLASH to run properly. This field is enabled by default.

The utility iFLASH must be run without the presence of a 386 Protected Mode control program, such as Windows or EMM386. iFLASH uses the processor's flat addressing mode to update the flash area.

Following is a typical example of how the areas of flash ROM are defined in the Flash Table (Table 3-5). The Block Base Address field contains the base address of each block, as located at the top of the address space.

Table 3-5:   Flash Table

Base Address	Length	Usage
0FFF80000h	10000h	ESCD,VPD and SCSI NVRAM
0FFF90000h	8000h	SMM Binary
0FFF98000h	4000h	User Binary
0FFF9C000h	4000h	BIOS Block
0FFFA0000h	12000h	Language Block
0FFFB2000h	D000h	BIOS Block
0FFFC0000h	4000h	Console Redirection Binary
0FFFC4000h	C000h	BIOS Block
0FFFD0000h	10000h	BIOS Block
0FFFE0000h	C000h	Reserved Block
0FFFEC000h	4000h	Recovery Block
0FFFFF000h	10000h	BIOS Block

3.12 Loading the System BIOS

A new Ak450NX BIOS is contained in the .BIx files. The number of .BIx files is determined by the size of the Ak450NX BIOS area in flash ROM (see Table 3-5 for further information on logical area 1 - System BIOS). As of this writing, the system BIOS area contains eight files (512KB). The files are named as follows:

        xxxxxxxx.BIO
        xxxxxxxx.BI1
        xxxxxxxx.BI2

The first eight letters of each file name on the release diskette can be of any value, but cannot be renamed. Each file contains a link to the next file in the sequence. iFLASH does a link check before updating to ensure that the process is successful. However, the first file in the list can be renamed, but all subsequent file names must remain unchanged. When an update of the system BIOS is complete, the system is automatically rebooted. The user binary area is also updated during a system BIOS update.

3.13 User Binary Area

The Ak450NX includes a 16KB area in flash for implementation-specific OEM add-ons. The user binary area can be saved and updated exactly as described above in Section 3.12 Loading the System BIOS. Only one file is needed. The valid extension for user files is **.**USR.

A user binary may be a run-time binary or a POST-time-only binary. In the Ak450NX BIOS, which was released when this specification was written, a run-time user binary is loaded at the physical address 000D8000h - 000DBFFFh, a size of 16KB. The load location, however, may change in future BIOS releases. This makes it important that user binaries be location independent.

A POST-time user binary may be loaded anywhere in the conventional (0 - 640KB) memory area and discarded at the time of OS boot.

3.14 System Resources

3.14.1 Memory Map

Table 3-6: System Memory Map

Address Range	Amount	Function
00000000 – 0009FFFF	640KB	Base (conventional) system memory
000A0000 – 000AFFFF	128KB	ISA video buffer
000C0000 – 000D7FFF	96KB	Add-in option ROMs (video, SCSI…)
000C0000 – 000D7FFF	96KB	Add-in option ROMs
000D8000 – 000DBFFF	16KB	Allocated to run-time user binary, if enabled/programmed, otherwise can be used for option ROMs
000DC000 – 000DFFFF	16KB	Allocated to console redirection, if enabled, otherwise can be used for option ROMs
000E0000 – 000FFFFF	128KB	System BIOS shadowed
00100000 - PCI memory allocated to first PCI device		Typically it can go up to 3 GB
FEC00000 – FEC0FFFF	64KB	Reserved. Unused on this platform Reclaimed. If main memory exceeds this region
FEC10000 – FEC1FFFF	64KB	IOAPIC allocated to the PID Reclaimed. If main memory exceeds this region
FEC20000 – FECFFFFF	896KB	Reserved Reclaimed. If main memory exceeds this region
FEE00000 - FEF00000	1 MB	LOCAL APIC Reclaimed. If main memory exceeds this region
FF000000 – FFDFFFFF	14 MB	Unused Reclaimed. If main memory exceeds this region
FFE00000 – FFFFFFFF	2 MB	Main system BIOS
100000000 – 1FFFFFFFF	4 GB	If memory exists

Note: The term main memory in the above table refers to the added physical memory.

3.14.2 I/O Map

Table 3-7: System I/O Address Map

I/O Address	Resource
0000 – 001F	DMA Controller
0020 – 0021	Interrupt Controller 1
0022 – 0040	Unused/Reserved
0040 – 005F	Programmable Timer
0060 & 0064	Keyboard Controller
0061	NMI Status & Control Register
0070	NMI Mask Bit and RTC Index Address
0071	Real-time Clock
0072	Real-time Clock extended index register
0073	Real-time Clock extended data register
0080 – 008F	DMA Low Page Register
0092	Port 92 Register
00A0 – 00A1	Interrupt Controller 2
00B2	Advanced Power Management Control

I/O Address	Resource
00B3	Advanced Power Management Status
00C0 – 00DF	DMA Controller
00F0	Coprocessor Error
0170 – 0177	Secondary IDE Controller
01F0 – 01F7	Primary IDE Controller
0278 – 027F	Parallel Port 2 (relocatable)
02E8 – 02EF	Serial Port 4 (relocatable)
02F8 – 02FF	Serial Port 2 (relocatable)
0370 – 0377	Secondary Floppy
0378 – 037F	Parallel Port 1 (relocatable)
03BC – 03BF	Parallel Port 3
03E8 – 03EF	Serial Port 2 (relocatable)
03F8 – 03FF	Serial Port 1 (relocatable)
0CF8	PCI Configuration Address Register
0CFC	PCI Data Address Register
0CF9	Reset Control
04D0 – 04D1	INTC Edge/Level Register
0C00 – 0C7F	Power Management Base Address
0CA8 – 0CAF	SMIC Decoder
0CC0 – 0CCF	SM Base Address
2000 – FFFF	Allocated to the PCI devices

3.14.3 PCI Configuration Space Map

Table 3-8: PCI Configuration Space Map

Host Bus Number	Device Number (Hex)	Description
0	48	Slot 1
0	50	Onboard 7880*
0	58	Slot 2
0	60	On board video
0	78	PIIX4
0	80	MIOC
0	90	PXB-0A
0	98	PXB-0B
0	A0	PXB-1A
1	20	Slot 3
1	28	Slot 4
1	30	Slot 5
1	38	Slot 6
1	48	PID
2	20	Slot 7
2	20	Slot 8
2	20	Slot 9
2	20	Slot 10
2	20	Slot 11

3.14.4 Interrupts Map

Table 3-9:   System Interrupts Map

IRQ	Device
NMI	Parity error
0	Interval timer
1	Keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	Onboard serial port B (COM2) or add-in board
4	Onboard serial port A (COM1) or add-in board
5	Parallel port LPT2 or add-in board
6	Onboard diskette (floppy) controller
7	Parallel port LPT1 or add-in board
8	Real-time clock (RTC)
9	Reserved/Used for ACPI
10	(add-in board)
11	(add-in board)
12	Onboard PS/2 mouse port or add-in board
13	Math coprocessor error
14	Primary IDE hard drive controller, if enabled
15	Secondary IDE hard drive controller, if enabled

Note: Add-in board can be PCI or ISA

3.14.5 DMA Channels

Table 3-10: DMA Channel Map

Channel	Device
0	(add-in board)
1	(add-in board)
2	Floppy drive
3	PCI IDE (selectable)
4	PCI IDE (selectable)
5	(add-in board)
6	(add-in board)
7	(add-in board)

3.15 Error Messages and Error Codes

The system BIOS displays error messages on the video screen. Prior to video initialization, beep codes inform the user of errors. POST error codes are logged in the system event log, as well as the extended BIOS data area (EBDA).

The BIOS displays POST error codes on the video monitor.

Table 3-11 and Table 3-12 define POST Port-80h codes, POST beep codes, POST error codes, and system error messages.

3.15.1 POST Port-80h Codes

The BIOS indicates the current testing phase during POST after the video adapter has been successfully initialized by writing a 2-digit hex code to I/O location 80h. If a Port-80h card is installed, it displays this 2-digit code on a pair of hex display LEDs.

Table 3-11: Port-80h Code Definition

Code	Meaning
CP	Phoenix check point (Port-80) code

Table 3-12 contains the Port-80 codes displayed during the boot process. A beep code is a series of individual beeps on the system speaker, each of equal length. Table 3-12 describes the error conditions associated with each beep code and the corresponding POST checkpoint code as seen by a Port 80h card (e.g., if an error occurs at checkpoint 20h, a beep code of 1-3-1-1 is generated).

Table 3-12: Standard BIOS Port-80 Codes

CP	Beeps	Reason
02		Verify real mode
04		Get processor type
06		Initialize system hardware
08		Initialize chip set registers with initial POST values
09		Set in POST flag
0A		Initialize processor registers
0B		Enable processor cache
0C		Initialize caches to initial POST values
0E		Initialize I/O
0F		Initialize the local bus IDE
10		Initialize power management
11		Load alternate registers with initial POST values
12		Restore processor control word during warm boot
14		Initialize keyboard controller
16	1-2-2-3	BIOS ROM checksum
18		8254 timer initialization
1A		8237 DMA controller initialization
1C		Reset programmable interrupt controller
20	1-3-1-1	Test DRAM refresh
22	1-3-1-3	Test 8742 keyboard controller
24		Set ES segment register to 4 GB
28	1-3-3-1	Autosize DRAM. Beep code indicates not enough RAM available
2A		Clear 512KB base RAM
2C		Reserved
2E	1-3-4-3	Base RAM failure, not enough memory to continue POST
30		Reserved
32		Test processor bus-clock frequency
34		Test CMOS

CP	Beeps	Reason
35		RAMInitialize alternate chip set registers
36		Warm start shutdown
37		Reinitialize the chip set (MB only)
38		Shadow system BIOS ROM
39		Reinitialize the cache (MB only)
3A		Autosize cache
3C		Configure advanced chip set registers
3D		Load alternate registers with CMOS values
40		Set initial processor speed new
42		Initialize interrupt vectors
44		Initialize BIOS interrupts
46	2-1-2-3	Check ROM copyright notice
47		Initialize manager for PCI Option ROMs
48		Check video configuration against CMOS
49		Initialize PCI bus and devices
4A		Initialize all video adapters in system
4B		Display QuietBoot screen
4C		Shadow video BIOS ROM
4E		Display copyright notice
50		Display processor type and speed
52		Test keyboard
54		Set key click, if enabled
56		Enable keyboard
58	2-2-3-1	Test for unexpected interrupts
5A		Display prompt **Press F2 to enter SETUP**
5C		Test RAM between 512KB and 640KB
60		Test extended memory
62		Test extended memory address lines
64		Jump to UserPatch1
66		Configure advanced cache registers
68		Enable external and processor caches
6A		Display external cache size
6C		Display shadow message
6E		Display nondisposable segments
70		Display error messages
72		Check for configuration errors
74		Test real-time clock
76		Check for keyboard errors
7A		Test for key lock on
7C		Set up hardware interrupt vectors
7E		Test coprocessor, if present
80		Detect and install external RS232 ports
82		Detect and install external parallel ports
85		Initialize PC-compatible PnP ISA devices
86		Reinitialize onboard I/O ports
88		Initialize BIOS data area
8A		Initialize extended BIOS data area

CP	Beeps	Reason
8C		Initialize floppy controller
90		Initialize hard-disk controller
91		Initialize local-bus hard-disk controller
92		Jump to UserPatch2
93		Build MPTABLE for multiprocessor system
94		Disable A20 address line
95		Install CD ROM for boot
96		Clear huge ES segment register
98	1-2	Search for option ROMs. One long, two short beeps on checksum failure
9A		Shadow option ROMs
9C		Set up power management
9E		Enable hardware interrupts
A0		Set time of day
A2		Check key lock
A4		Initialize typematic rate
A8		Erase F2 prompt
AA		Scan for F2 key stroke
AC		Enter SETUP
AE		Clear in-POST flag
B0		Check for errors
B2		POST done – prepare to boot operating system
B4	1	One short beep before boot
B5		Display Multiboot menu
B6		Check password (optional)
B8		Clear global descriptor table
BC		Clear parity checkers
BE		Clear screen (optional)
BF		Check virus and backup reminders
C0		Try to boot with INT 19
DO		Interrupt handler error
D2		Unknown interrupt error
D4		Pending interrupt error
D6		Initialize option ROM error
D8		Shutdown error
DA		Extended block move
DC		Shutdown 10 error
FB		FRB in progress
FC		5 sec wait for BMC to initialize
FD		FRB 2 watchdog timer failed, reset will occur in 5 seconds

3.15.2 POST Error Codes and Messages

Table 3-13 defines POST error codes and associated messages. These codes may change in the future as the Phoenix* BIOS matures and includes the support for POST error code display.

Table 3-13: POST Error Messages and Codes

Code	Error Message
0002	Primary Boot Device Not Found
0010	Cache Memory Failure, Do Not Enable Cache
0015	Primary Output Device Not Found
0016	Primary Input Device Not Found
0042	ISA Config contains invalid info
0050	PnP Memory Conflict:
0051	PnP 32-bit Memory Conflict:
0052	PnP IRQ Conflict:
0053	PnP DMA Conflict:
0054	PnP Error Log Is Full
0055	Bad PnP Serial ID Checksum:
0056	Bad PnP Resource Data Checksum:
0060	Keyboard Is Locked ... Please Unlock It
0070	CMOS Time & Date Not Set
0080	Option ROM has bad checksum
0083	Shadow Of PCI ROM Failed
0085	Shadow Of ISA ROM Failed
0131	Floppy Drive A:
0132	Floppy Drive B:
0135	Floppy Disk Controller Failure
0140	Shadow Of System BIOS Failed
0170	Disabled CPU slot #
0171	CPU Failure – CPU # 1
0172	CPU Failure – CPU # 2
0173	CPU Failure – CPU # 3
0174	CPU Failure – CPU # 4
0175	CPU modules are incompatible or one is not present.
0176	Previous CPU Failure – CPU # 1
0177	Previous CPU Failure – CPU # 2
0178	Previous CPU Failure – CPU # 3
0179	Previous CPU Failure – CPU # 4
0180	Attempting to boot with failed CPU
0181	BSP switched, system may be in uniprocessor mode
0191	CMOS Battery Failed
0195	CMOS System Options Not Set
0198	CMOS Checksum Invalid
0200	Failure Fixed Disk
0210	Stuck Key
0211	Keyboard error
0212	Keyboard Controller Failed
0213	Keyboard locked - Unlock key switch
0220	Monitor type does not match CMOS - Run SETUP
0230	System RAM Failed at offset
0231	Shadow RAM Failed at offset
0232	Extended RAM Failed at address line

Code	Error Message
0232	Extended RAM Failed at offset
0250	System battery is dead - Replace and run SETUP
0251	System CMOS checksum bad - Default configuration used
0260	System timer error
0270	Real time clock error
0271	Check date and time settings
0280	Previous boot incomplete - Default configuration used
0289	System Memory Size Mismatch
0295	Address Line Short Detected
0297	Base Or Extended Memory Error: Board #, DIMM #
0299	ECC Error Correction Failure
02B0	Diskette drive A error
02B1	Diskette drive B error
02B2	Incorrect Drive A type - run SETUP
02B3	Incorrect Drive B type - run SETUP
02D0	System cache error - Cache disabled
02F0	CPU ID
02F5	DMA Test Failed
02F6	Software NMI Failed
02F7	Fail-safe Timer NMI Failed
0370	Keyboard Controller Error
0373	Keyboard Stuck Key Detected
0375	Keyboard and Mouse Swapped
0430	Timer Channel 2 Failure
0440	Gate-A20 Failure
0441	Unexpected Interrupt in Protected Mode
0445	Master Interrupt Controller Error
0446	Slave Interrupt Controller Error
0450	Master DMA Controller Error
0451	Slave DMA Controller Error
0452	DMA Controller Error
0460	Fail-safe Timer NMI Failure
0461	Software Port NMI Failure
0465	Bus Timeout NMI in Slot
0467	Expansion Board NMI in Slot
0510	PCI Parity Error
0611	IDE configuration changed
0612	IDE configuration error - device disabled
0613	Com A configuration changed
0614	Com A configuration error - device disabled
0615	Com B configuration changed
0616	Com B configuration error - device disabled
0617	Floppy configuration changed
0618	Floppy configuration error - device disabled
0619	Parallel port configuration changed
061A	Parallel port configuration error - device disabled
0710	System Board Device Resource Conflict

Code	Error Message
0711	Static Device Resource Conflict
0780	PCI Segment 1 memory request exceeds 998 MB
0781	PCI Segment 1 I/O requests exceeds 12KB
0782	PCI I/O request exceeds amount available
0783	PCI memory request exceeds amount available
0784	Illegal bus for memory request below 1 MB
0785	Memory request below 1 MB exceeds 1 MB
0800	PCI I/O Port Conflict
0801	PCI Memory Conflict
0802	PCI IRQ Conflict
0804	PCI ROM not found, May Be OK For This Card:
0805	Insufficient Memory to Shadow PCI ROM:
0806	Memory Allocation Failure for Second PCI Segment
0810	Floppy Disk Controller Resource Conflict
0811	Primary IDE Controller Resource Conflict
0812	Secondary IDE Controller Resource Conflict
0815	Parallel Port Resource Conflict
0816	Serial Port 1 Resource Conflict
0817	Serial Port 2 Resource Conflict
0820	Expansion Board Disabled in Slot
0900	NVRAM Checksum Error, NVRAM Cleared
0903	NVRAM Data Invalid, NVRAM Cleared
0982	I/O Expansion Board NMI in Slot
0984	Expansion Board Disabled in Slot
0985	Fail-safe Timer NMI
0986	System Reset caused by Watchdog Timer
0987	Bus Timeout NMI in Slot
8100	Processor 0 failed BIST
8101	Processor 1 failed BIST
8102	Processor 2 failed BIST
8103	Processor 3 failed BIST
8104	Processor 0 Internal error (IERR)
8105	Processor 1 Internal error (IERR)
8106	Processor 0 Thermal Trip error
8107	Processor 1 Thermal Trip error
8108	Watchdog timer failed on last boot
810B	Processor 0 failed initialization
810C	Processor 0 disabled
810D	Processor 1 disabled
810E	Processor 0 failed FRB-3 timer
810F	Processor 1 failed FRB-3 timer
8110	Server Management Interface failed to function
8128	Processor 2 Internal error (IERR)
8129	Processor 3 Internal error (IERR)
8130	Processor 2 Thermal Trip error
8131	Processor 3 Thermal Trip error
8138	Processor 2 failed FRB-3 timer

Code	Error Message
8139	Processor 3 failed FRB-3 timer
8140	Processor 2 disabled
8141	Processor 3 disabled
8148	Processor 1 failed initialization
8149	Processor 2 failed initialization
814A	Processor 3 failed initialization
814B	BMC in Update Mode
8150	NVRAM Cleared by Jumper
8152	ESCD Data Cleared
8153	Password Cleared by Jumper
8160	Unable to apply BIOS update for Processor 1
8161	Unable to apply BIOS update for Processor 2
8162	Unable to apply BIOS update for Processor 3
8163	Unable to apply BIOS update for Processor 4
8168	Processor 1 L2 cache failed
8169	Processor 2 L2 cache failed
816A	Processor 3 L2 cache failed
816B	Processor 4 L2 cache failed
8170	BIOS does not support current stepping for Processor 1
8171	BIOS does not support current stepping for Processor 2
8172	BIOS does not support current stepping for Processor 3
8173	BIOS does not support current stepping for Processor 4
8180	PXB1 failed to respond
8181	Mismatch Among Processors Detected
8182	L2 cache size mismatch
8200	Baseboard Management Controller failed to function
8201	Front Panel Controller failed to function
8203	Primary Hot-swap Controller failed to function
8204	Secondary Hot-swap Controller failed to function

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4. Server Management Implementation

This chapter provides the server management architecture of the Ak450NX board set. The server management features are listed below.

Features

- Voltage monitoring
- Temperature monitoring
- Processor voltage ID (VID) monitoring and processor presence detection
- DIMM ID monitoring and presence detection
- Chassis fan failure detection
- System power control
- Watchdog timer
- BMC private management bus interface
- System management software (SMS) and system management mode (SMM) Intelligent Platform Management Bus (IPMB) message receiver
- Event message receiver
- System event log (SEL) management and access
- Sensor data record (SDR) repository management and access
- Processor nonmaskable interrupt (NMI) monitoring
- Front panel NMI monitoring and NMI generation
- Processor system management interrupt (SMI) monitoring
- Timestamp clock
- Power-on self test (POST) code log
- Secure mode support
- Fault resilient booting (FRB) support

4.1 Server Management Overview

The Ak450NX server management architecture revolves around a microcontroller and a parallel I/O-mapped interface for control of server management functions. Both components are located on the Ak450NX I/O baseboard. The onboard microcontroller provides a centralized interface for other microcontrollers, which an OEM may choose to integrate into their own custom chassis boards (e.g., front panel, hard disk backplane, power distribution backplane).

Figure 4-1 shows the Ak450NX board set integrated into the Intel® AC450NX Rack Mount Server System chassis, and is an example of the server management possibilities available to the designer.
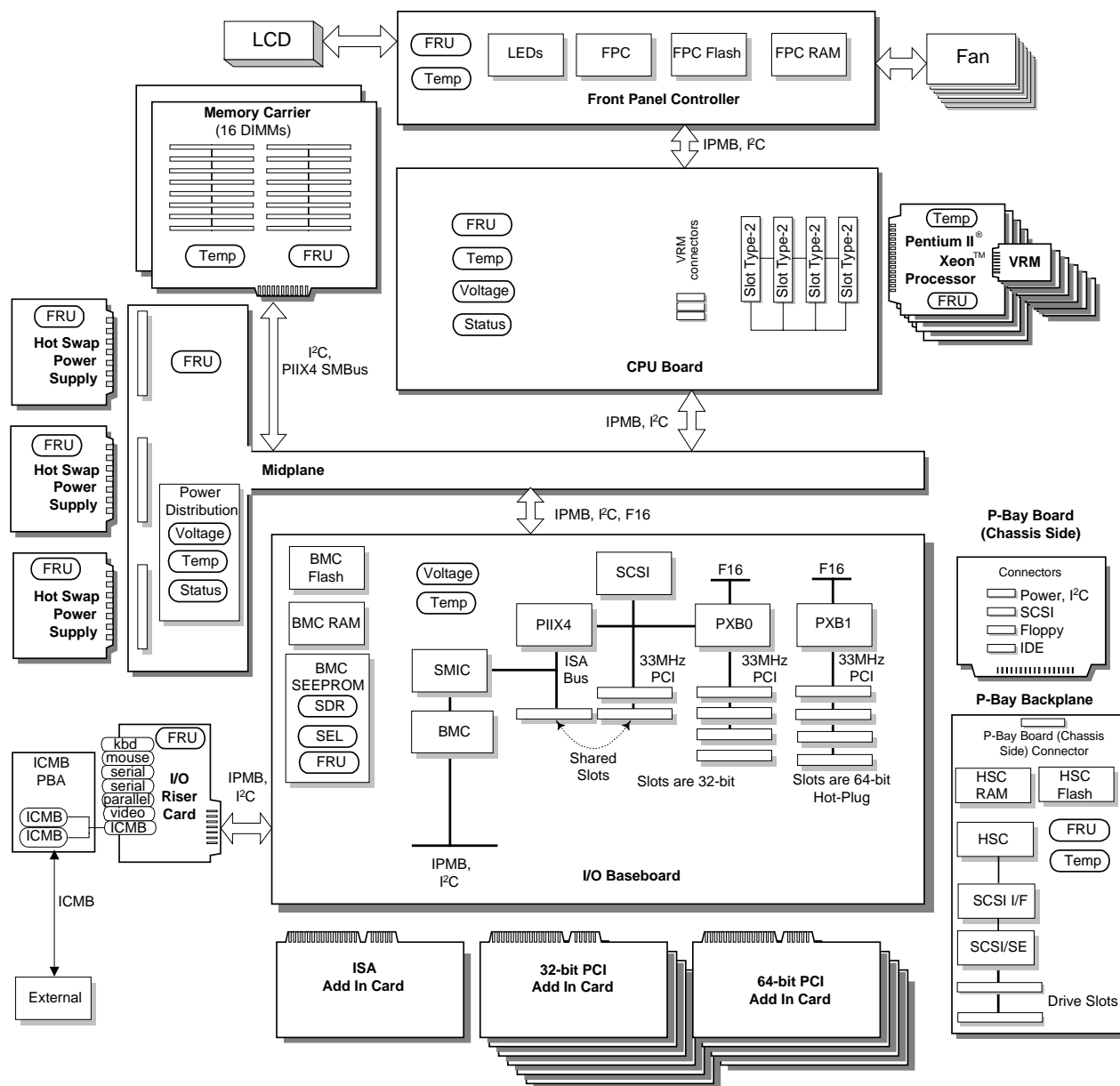
Figure 4-1: Ak450NX Server Management Architecture Diagram

4.2 Platform Management Hardware

The Ak450NX board set server management features are implemented using a BMC and an ISA/BMC interface device called the system management interface chip (SMIC).

Other key server management hardware components are:

- Buses, such as the IPMB, the microcontroller private I^2C buses, and the ISA bus
- Nonintelligent devices, such as serial EEPROMs (SEEPROMs)

- Nonvolatile storage to hold the FRU inventory and default configurations, the sensor data record (SDR), and the system event log (SEL)
- Connectors between the various boards and components

4.2.1   Baseboard Management Controller (BMC)

The heart of Ak450NX server management is the baseboard management controller (BMC). The BMC is located on the Ak450NX I/O baseboard. This controller provides primary server management monitoring capabilities. Associated with the BMC is a nonvolatile storage that holds the SEL, the SDR repository, the operational code, and the configuration defaults for the BMC itself.

The BMC supports the IPMI and the I^{2}C interface. The BMC uses IPMI protocol to communicate with other intelligent management controllers on the chassis boards via the IPMB.

The BMC also uses the I^{2}C interface to communicate with nonintelligent devices on its private management bus. The BMC can be accessed from the ISA bus via the SMIC.

4.2.1.1   BMC Features

The BMC provides various server management functions, some of which are discussed in the following sections.

4.2.1.1.1   Voltage Monitoring

The BMC scans voltages using the serial parallel interface (SPI) bus connected to the analog-to-digital (A/D) converter. The SPI bus is local to the I/O baseboard and CPU baseboard. It is isolated from the IPMB by the BMC.

Each time a channel is scanned, the BMC compares the current reading to assigned thresholds stored in the SDR, sets the appropriate status and, if a threshold has been crossed and BIOS has been enabled, generates an event message in the system event log. The BMC scans each voltage sensor once every 5 seconds in a sequential, revolving fashion, with the polling rate dependent on the number of voltage sensors.

Both the upper critical threshold and the lower critical threshold may be set.

The thresholds and event message configuration are programmable via the ISA/BMC interface. The voltage readings, thresholds, sensor configuration, and failure status can be read via the same interface.

4.2.1.1.2   Baseboard Voltage Monitoring

The A/D converter, manufactured by National Semiconductor as part number ADC0819*, is located on the I/O baseboard (see Figure 4-1). This device monitors all voltages on the I/O baseboard and provides the data to the BMC. The following I/O baseboard voltages are monitored:

- I/O baseboard +5 V
- I/O baseboard +12 V
- I/O baseboard +3.3 V
- I/O baseboard -12 V
- I/O baseboard -5 V
- Vcc standby
- Wide SCSI bus termination (3 channels)

Table 4-1 shows the default voltage threshold values.

Table 4-1:   Voltage Thresholds

Voltage	Upper Critical	Lower Critical
3.3 V	3.645 V	3.077 V
12 V	13.098 V	10.738 V
5 V	5.527 V	4.390 V
5 V Standby	5.527 V	4.390 V
-12 V	-10.720 V	-13.420 V
-5 V	-4.240 V	-5.860 V
SCSI Termination	3.136 V	2.508 V

4.2.1.1.3   Processor Voltage Monitoring

The BMC is responsible for monitoring the voltage for each Pentium II Xeon slot-2 processor supply and for the termination voltage and support logic supplies. The following voltages are monitored: 1.5 V, 2.5 V, 3.3 V, 5 V, 12 V, CPU core voltages and processor cache voltages. The BMC interfaces to an external multichannel A/D converter. Four of the A/D channels are used for these voltage scanning functions. The BMC maintains internal thresholds against which the A/D readings are compared. The BMC generates an event message on the IPMB when the thresholds are crossed. The following processor voltages are monitored:

- Processor 1 core voltage
- Processor 2 core voltage
- Processor 3 core voltage
- Processor 4 core voltage
- CPU +2.5 V
- CPU +1.5 V (front-side bus termination voltage)
- CPU +3.3 V
- CPU +5 V
- CPU +12 V
- Processor 1&2 cache voltage
- Processor 3&4 cache voltage

Table 4-2 shows the default processor voltage threshold values.

Table 4-2:   Processor Voltage Thresholds

Voltage	Upper Critical	Lower Critical
Core Voltage	2.175 V	1.666 V
CPU 2.5 V	2.744 V	2.254 V
CPU 3.3 V	3.645 V	3.077 V
CPU 5 V	5.527 V	4.390 V
CPU 12 V	13.932 V	10.062 V
Processor Cache	3.724 V	1.666 V
Processor Bus Termination	1.724 V	1.274 V

4.2.1.1.4   Temperature Monitoring

The BMC polls eight temperature sensor devices, which are accessed as nonintelligent devices on the BMC private I^2C bus. One sensor is located on the I/O baseboard, one is on the CPU baseboard, four are in the processor cartridges, and two are on the memory modules (see Figure 4-1). The current temperature readings, thresholds, sensor configuration, and failure status can be read via the ISA or IPMB interfaces to the BMC.

The BMC monitors the temperature sensors via its private management bus. This bus is isolated from the IPMB by the BMC. The BMC obtains the reading from the sensor, compares the readings to a set of thresholds and, if enabled in BIOS, generates an event message in the system event log when a threshold is crossed.

The BMC scans the temperature sensors in a sequential, revolving fashion. Two thresholds are supported for the temperature sensor: the upper critical threshold and the lower critical threshold. Critical indicates a situation that demands immediate attention to prevent or reduce damage.

Table 4-3 displays the temperature sensor devices, the device types, and the manner by which they are accessed by the BMC. Table 4-4 displays the default temperature thresholds.

Table 4-3:   Temperature Sensors Monitored by the BMC

Temperature Sensor	Device	Access
I/O Baseboard Temperature	DS1621*	BMC Private I^{2}C Bus
CPU Baseboard Temperature	DS1624*	BMC Private I^{2}C Bus
Processor 1 Temperature	DS1617*	Processor SMBus
Processor 2 Temperature	DS1617	Processor SMBus
Processor 3 Temperature	DS1617	Processor SMBus
Processor 4 Temperature	DS1617	Processor SMBus
Memory Module 1 Temp.	DS1624	BMC Private I^{2}C Bus
Memory Module 2 Temp.	DS1624	BMC Private I^{2}C Bus

Table 4-4:   Default Temperature Thresholds

Threshold	Upper Critical	Lower Critical
I/O Baseboard (PXB)	45 °C/113 °F	-10 °C/14 °F
CPU Baseboard	50 °C/122 °F	-10 °C/14 °F
Processor	70 °C/158 °F	0 °C/32 °F
Memory Module 1	50 °C/122 °F	-10 °C/14 °F
Memory Module 2 [†]	45 °C/113 °F	-10 °C/14 °F

[†] Different air flow in vicinity of this module allows different critical value.

4.2.1.1.5   Processor Voltage ID (VID) Monitoring and Processor Presence Detection

The voltage ID (VID) signals from the processors are used to configure the onboard processor voltage regulator circuits on the CPU baseboard using an IPMI command via the BMC. The BMC sensors read the processor status to determine presence and VID. The VID information read from the processor overrides any thresholds that were provided in the SDR. However, the override of the SDR values is only in effect while the system is powered on; it does not alter the default values of the SDR.

4.2.1.2   DIMM ID Monitoring and Presence Detection

The BMC supplies the interface to the identification (ID) information provided by the DIMMs . The DIMMs contribute the main DRAM memory for the system. This information includes the size, speed, and type of DIMM installed. The information also indicates presence, (whether a DIMM is physically inserted into the socket).

The BMC provides commands for reading the DIMM ID information. These commands are executable from ISA and from the IPMB. The memory modules make this information available to the BMC via the BMC private bus.

4.2.1.3   Fault Resilient Booting (FRB) Support

The BMC works in conjunction with the BIOS to implement fault resilient booting (FRB). The BMC specifically implements FRB-2 and FRB-3. The FRB feature allows a multiprocessor system to detect certain types of bootstrap processor failures. If a failure is detected, it asserts a signal to disable the errant processor/processor socket, resets the system and then restarts the system with one of the remaining processors serving as the boot-strap processor (BSP). The BMC does not disable the processor if it is the last remaining processor in the system, nor does it allow all processors to be disabled simultaneously.

4.2.1.3.1   FRB-3

FRB-3 refers to the level of FRB at which a watchdog timer is started on power-up or which hard resets in a MP system. The watchdog timer must be stopped by BIOS, which requires the BSP to actually run BIOS code. If the timer is not stopped, the BSP is disabled, the system is reset, and another processor becomes the BSP. Thus, FRB-3 provides verification on power-up of a functional BSP (which was assigned the BSP role by the hardware) that can actually run code. If so configured in BIOS, the BMC also generates an internal event message for the FRB-3 failure event.

FRB requires multiple processors. The BMC uses the VID bits to verify that there are at least two processors installed in the system. If only one processor is present, the FRB-3 timer is not started.

BSP assignment is deterministic (i.e., when multiple processors are present, the BSP selection occurs in a known sequence).

If an FRB-3 timeout occurs during the boot sequence, the current BSP is disabled and the system is reset. This process repeats until the system boots without an FRB-3 timeout or until all processors except the last one are disabled. The BMC will not disable the last remaining processor.

4.2.1.3.2   FRB-2

FRB-2 is a level of FRB at which the BIOS uses the BMC watchdog timer to back up its operation during POST. The BIOS sets a bit in the BMC indicating that the BIOS is in the FRB-2 phase of operation.

The BIOS sets this bit after it has determined which processor is the BSP, and has saved this information. At this time, BIOS can set the FRB-2 bit, load the BMC watchdog timer with the new timeout interval, and disable FRB-3. This sequence ensures that there is no gap in watchdog timer coverage between FRB-3 and FRB-2. If the timer expires while the FRB-2 function is selected in the timer use flags, the BMC generates an FRB-2 timeout event message. The BMC then hard resets the system. The BIOS is responsible for disabling FRB-2 timeout prior to exiting POST.

4.2.1.3.3   FRB-1

FRB-1 is implemented mostly by the BIOS. The BIOS detects the failure of the BSP by examining the processor's BIST results. If a BIST failure is indicated, the BIOS takes its own steps to record the event so that it can be logged later. The BIOS then disables the processor by allowing the FRB-3 timeout to occur.

4.2.2   SEEPROM Information

The BMC SEEPROM is used for holding the following information:

- **System Event Log (SEL).** This is a 7.75KB area of the SEEPROM that is used to hold the SEL.
- **Sensor Data Record (SDR) Repository.** This is an 8KB area of SEEPROM that is used to hold the sensor data records.

- **FRU Inventory Information.** The BMC implements a logical FRU inventory device. The SEEPROM device provides a 256 byte area of nonvolatile storage for this information.
- **BMC Configuration Defaults.** A portion of the FRU inventory area, referred to as the *internal use area* is used for holding configuration defaults for the BMC itself.

4.2.3   System Management Interface Chip (SMIC)

The SMIC ASIC provides a parallel I/O-mapped interface between the ISA bus and the BMC. This interface is used for communication between the BMC and system management software (SMS) running under the OS.

4.2.4   System Event Log (SEL)

The SEL is a repository for the system's critical event information. The SEL is maintained in the I/O baseboard's SEEPROM by the BMC. Commands for accessing the SEL can be delivered to the BMC via the ISA SMIC interface or via the IPMB. This makes system event information accessible *in-band* by the BIOS routines and SMS such as LANDesk Server Manager, and *out-of-band* via the server monitor module (SMM) card or other intelligent management device connected to the IPMB.

4.2.5   Sensor Data Record (SDR) Repository

The BMC maintains a special region of the I/O baseboard's SEEPROM for the SDRs. This area is used for storing sensor data records for all the sensor devices located on the Ak450NX board set, as well for sensor devices located on any additional system/chassis boards.

Sensor data records contain information that identifies which device holds a sensor, the number of that sensor and its type, the kinds of events it can generate, and the initial threshold values of the sensor. Sensor data records also hold information offsets and constants for converting the raw sensor readings to standard units (e.g., mA, volts, rpm, etc.). The system management software uses this information to get the sensor locations and conversion factors that it uses when polling the sensors.

The FRU & SDR Load Utility can be used to read the SDR repository.

4.2.6   System Management Buses

The Ak450NX board set implements the following buses for use in system management:

4.2.6.1   Intelligent Platform Management Bus (IPMB)

The IPMB is a multimaster, open-drain, serial bus that is routed between the major system boards. The bus is both electrical and timing compatible with the I^2C bus specification, and it supports both intelligent management controllers and nonintelligent devices (e.g., SEEPROM). Intelligent management controllers communicate with each other via the IPMB. An example of this is the AC450NX Rack Mount Server System, in which the BMC communicates with management microcontrollers on the front panel and the SCSI hot-swap backplane via the IPMB.

The BMC communicates with other management controllers, over the IPMB, using IPMI commands. The IPMB can also support devices that do not adhere to the IPMI protocol; including nonintelligent devices such as I^2C serial EEPROMs.

4.2.6.1.1   IPMB Electrical Isolation

The IPMB electrical isolation circuitry on the I/O baseboard allows the FPC, the SMM card feature connector, the SMM card IPMB connector and the auxiliary IPMB connector to be accessed when the rest of the system is powered down. These isolated, always alive parts are powered by 5 V Standby Power. This isolation ensures that the FPC can be accessed when 5 V powered IPMB devices on other segments of the IPMB 'ground out' the bus when power is removed.

This functionality is labeled as "isolator" on the I/O baseboard in Figure 4-1.

4.2.6.2   BMC Private Management Bus

A number of the devices that the BMC monitors, or to which it provides access, are connected to the BMC private management bus. The BMC private management bus is a single-master I^{2}C bus that is solely driven by the BMC. The BMC is considered to be the owner of the devices on its private management bus.

The BMC private management bus is local to the CPU baseboard and the I/O baseboard. The private management bus is isolated from the IPMB by the BMC. This provides several benefits, including faster polling accesses (since there is no IPMB arbitration) and a reduction of IPMB traffic and address space.

Table 4-5 displays the devices that are managed by the BMC and the boards on which those devices are located.

Table 4-5:   BMC Managed Devices

Name	Device	Board
FRU/SEL Serial EEPROM	AT24C128*	I/O Baseboard
Temp Sensor PXB	DS1621*	I/O Baseboard
Serial EEPROM	AT24C02*	I/O Riser Card
Serial EEPROM	AT24C02	Interconnect Backplane
I/O Port A	PCF8574*	Memory Module 1
I/O Port B	PCF8574	Memory Module 1
Serial EEPROM/Temp Sensor	DS1624*	Memory Module 1
IO Port A	PCF8574*	Memory Module 2
IO Port B	PCF8574	Memory Module 2
Serial EEPROM/Temp Sensor	DS1624	Memory Module 2
Serial EEPROM/Temp Sensor	DS1624	CPU Baseboard
Temp Sensor	DS1617*	Processor 1
Serial EEPROM	AT24C02[†]	Processor 1
Temp Sensor	DS1617	Processor 2
Serial EEPROM	AT24C02[†]	Processor 2
Temp Sensor	DS1617	Processor 3
Serial EEPROM	AT24C02[†]	Processor 3
Temp Sensor	DS1617	Processor 4
Serial EEPROM	AT24C02[†]	Processor 4

[†] There are two AT24C02* devices on this component, the processor FRU and the OEM FRU.

4.2.6.3   Serial Peripheral Interface (SPI) Bus

The serial peripheral interface (SPI) bus provides information about the processor slots, the processors installed in those slots and the A/D converters on the CPU baseboard. The SPI bus is accessed through the BMC. Capabilities of the SPI bus include:

- Error and status inputs – including processor ID bits and control outputs

- 16-channel A/D converter for monitoring CPU baseboard voltages

The SPI bus is composed of four separate scan chains to minimize the length of each chain, thus keeping the access latency short. The first chain provides access to the error and status information (e.g., processor internal errors and DIMM memory errors from the MIOC). The second chain provides access to the A/D converters (e.g., processor core voltage and the 2.5 V, 3.3 V and 5 V supplies). The third SPI chain provides error and status information such as VID for processors 1 and 2 and their L2 cache VID. The fourth SPI chain provides error and status information for processors 3 and 4.

4.2.6.4　Processor SMBus

The SMBus provides BMC access to temperature sensors on the processor cartridge. The bus also provides access to two FRU information areas that are available from each individual processor. The first FRU area is read only and provides data such as part number, core and L2 stepping, core frequency, and voltages for the processor and L2. The second FRU area is available for OEM use. Once OEM information is written to this FRU, it can be write-protected so that the data cannot be easily overwritten.

4.2.6.5　Intelligent Chassis Management Bus (ICMB)

The Intelligent Chassis Management Bus (ICMB), along with the ICMB bridge, provides a mechanism for interchassis management communications. Multiple systems and peripheral chassis can be connected to the same ICMB. Through the ICMB, intelligent devices local to a server (e.g., the BMC) can access the local server management functions of external servers, allowing server management across multiple servers.

4.2.6.5.1　IPMB-ICMB Bridging

A separate chassis microcontroller can be used to act as a bridge between the IPMB and the ICMB. The bridging controller provides a messaging connection between the IPMB and the ICMB. It also responds to ICMB discovery messages, and other bridge request messages, such as providing ICMB protocol version information.

Note:　The Ak450NX board set does not contain the IPMB-ICMB bridge. This functionality must be added on an OEM designed microcontroller such as a front panel board. However, the front panel board for the Intel AC450NX Rack Mount Server System does include the IPMB-ICMB bridge.

4.2.7　FRU Inventory Information

Every board in the Ak450NX board set holds a nonvolatile storage device that contains FRU inventory information. All FRU inventory devices on the Ak450NX board set reside on the BMC private management bus and can be accessed only via the BMC.

The FRU inventory information includes board serial number, part number, and revision information. It can also contain asset tag, product name, chassis, and OEM specific information. The information is provided to aid in system servicing, inventory, and asset tracking. The I^2C address, the content, and the format of FRU information about individual boards are described in *Chapter 2 Board Set Details* of this document. The following boards contain FRU information.

- PHP I/O baseboard
- CPU baseboard
- Interconnect midplane
- Memory module
- FSB terminator module
- I/O riser card

4.2.7.1   FRU & SDR Load Utility

The FRU & SDR Load Utility allows FRU information for each individual board in the Ak450NX board set to be loaded, read, and displayed.

4.2.8   Platform Management Connectors

The Ak450NX board set provides several connectors for the interconnections of the server management signals across the board set. Connections are also provided to extend the IPMB to additional boards in the chassis like the front panel board, SCSI hot-swap backplane and the power distribution backplane.

The connections provided by the Ak450NX board set to allow OEM designed components to integrate into the server management architecture are as follows:

4.2.8.1   Front Panel Connector

The front panel connector on the CPU baseboard provides system control and management interconnections, including IPMB, ICMB, emergency management port (EMP), and other system management signals. The front panel connector signals are described in *Chapter 5 Board Specifications* of this document.

4.2.8.2   SMM Card Feature Connector

The feature connector is provided for use by the Intel® Server Monitor Module (SMM) card, also known as the emergency management card. The signals provided by this connector allow the SMM card to take full control of the system. The feature connector, when attached to an SMM card, provides the following functionality:

- Monitors additional voltages and sends out voltage alerts
- Monitors additional temperatures and sends out temperature alerts
- Allows the administrator to power-up/down the server from a remote location
- Provides the ability to redirect the console to a remote location

For pinout information for this connector, see *Chapter 2 Board Set Details* of this document.

4.2.8.3   IPMB Connectors

There are two IPMB connectors on the I/O baseboard.

- SMM card IPMB connector
- Auxiliary IPMB connector

The SMM card IPMB connector and the auxiliary connector are located on the portion of the IPMB that is powered by the +5 V standby. Therefore, these connections allow communication with the FPC while the system is powered down. This makes it possible to control system power via IPMI commands to the FPC.

4.2.8.3.1   SMM Card IPMB Connector

The SMM card IPMB connector is a 3-pin shrouded connector. This connector provides IPMB access for future SMM cards, which may not rely on the SMM card feature connector. The SMM card IPMB connector is located near the SMM card feature connector.

4.2.8.3.2   Auxiliary IPMB Connector

The auxiliary IPMB connector is also a 3-pin shrouded connector located on the I/O baseboard. The connector is provided for SMM-type cards, which might be used by an OEM or a system integrator. For auxiliary IPMB connector specifications, see *Chapter 2 Board Set Details* of this document.

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5. Board Specifications

5.1 Electrical Specification

Table 5-1 describes the tolerances and minimum/maximum currents for +3.3 V, +5 V, +12 V, and -12 V for the complete Ak450NX board set; the CPU and PHP I/O baseboards, the memory modules, the FSB termination modules, the interconnect midplane, and the I/O riser card. The power supply system must meet these requirements at the inputs to the interconnect midplane to ensure proper board set functionality. All the values are specified at the remote sense points on the interconnect backplane. For further details on each board's individual requirements, see *Sections 5.1.1 – 5.1.5* below.

Off voltage is the maximum voltage allowed on each domain during a power-off condition. In the case of the AC450NX server system chassis, this voltage is present any time AC power is present and is a result of the power supplies used in that system. The Ak450NX board set will draw a certain amount of current at these voltages. The Ak450NX board set does not use -5 V. 5 V standby must be present at any time AC power is present.

Table 5-1:   Ak450NX Board Set Voltage and Current Requirements Summary

Voltage Domain	Static[1] Tolerance	Dynamic[2] Tolerance	Min[3] Current	Max[4] Current	Max[4] Current Step	Test Load[5] Step di/dt	Capacitive[6] Load (Min)
3.3 V	+5%/-1.5%	+5%/-3.5%	8.8 A	56.61 A	23.15A	2.5 A/µs	204,000 µF
5.0 V	NA	+5/-3%	1.5 A	46.21 A	13.83 A	2.5 A/µs	61,100 µF
12 V	NA	+5%/-4%	0.20 A	36.6 A	24.0 A	0.15 A/µs	19,800 µF
+5.0 V Stby	NA	+5%/-3%	0.02 A	1.5 A	0.14 A	0.1 A/µs	1 µF
VBIAS[7]	+/-10%	+/-10%	0 A	200 mA	NA	NA	1 uF
-12.0 V	NA	+ 9%/-5%	0 A	1 A	0.25 A	0.1 A/µs	0.2 µF
Ripple/Noise	80 mV of noise in the range of 1kHz to 1 MHz is allowed on the 3.3 V plane. This voltage is measured at the CPU Baseboard, and is required in addition to set-point accuracy and line/load regulation (see note 1).						
Max Allowable Off Voltage (V$_{off\text{-}max}$)	5% of nominal value for +3.3 V, +5.0 V, +12.0 V, -12.0 V.						

Notes:

1. Tolerance includes set-point accuracy and line/load regulation. This value is based on a recovery time of 500 microseconds to return to static tolerance requirements after the specified maximum dynamic load occurs. Since the dynamic tolerance cannot be widened beyond the static tolerance requirements, only the dynamic requirements are specified for the +5 V and +12 V lines.

2. Tolerance includes set point accuracy, line/load regulation, and transient loading.

3. Minimum system configuration is as follows: 1 idle processor, 2 VRMs, 3 FSB termination modules, two memory cards with 128 MB of RAM, no I/O adapter cards, no front panel, no keyboard, no mouse, no video, no parallel-port connections, no bus activity.

4. Maximum system configuration is as follows: 4x65 W processors and their associated VRMs operating at 80% efficiency, keyboard, mouse, video, parallel-port connected, two memory modules (8 GB of RAM total), no front panel connector load (on CPU baseboard), no peripheral power connector load (on Interconnect Midplane), and all I/O adapter slots sinking maximum allowable current (40 A @ +5 V, 23 A @ +3.3 V, 3 A @ +12 V, 1 A @ -12 V).

5. This is the slew rate at which the power supply should be tested to meet the board requirements.

6. The power supply must meet the requirements with this amount of low ESR bulk capacitance on each output.

7. VBIAS is used only on the midplane, as a bias voltage. It's nominal value is specified at 15 V.

5.1.1.1   Individual Board Minimum/Maximum Current Ratings

Table 5-2 shows the minimum and maximum currents for +3.3 V, +5 V, +12 V, -12 V, and +5 Vstby for each board of the Ak450NX board set: the CPU baseboard, PHP I/O baseboard (with I/O riser), memory modules, midplane, and termination modules. These are the requirements that the power supply system must meet at the input to the midplane to ensure complete board set functionality.

Table 5-2:   Minimum/Maximum Current Ratings

Ak450NX Power Budget		Units	+3.3V	+5V	+12V	-12 V	+5 Vstby	Power
Board	Spec	Units	+3.3V	+5V	+12V	-12 V	+5Vstby	Power
PCI Hot Plug I/O Baseboard (includes I/O Riser)	Min Load	Adc	0.20	0.70	0.00	0.00	0.01	**4.21**
	Max Load[1]	Adc	28.0	40.0	8.00	0.99	Note[3]	**407.9**
	Max Step Load[2]	Adc	3.00	12.00	0.50	0.25	0.10	
	Max Slew Rate	A/uS	1	1	0.1	0.1	0.05	
CPU Baseboard[4]	Min Load	Adc	4.60	0.80	0.20	0.000	0.00	**21.58**
	Max Load	Adc	4.60	6.20	28.5	0.000	0.00	**388.18**
	Max Step Load	Adc	0.15	0.75	18.00	0.00	0.00	
	Max Slew Rate	A/uS	0.00	0.50	0.15	0.00	0.00	
Mem. Bd.1	Min Load	Adc	2.00	0.00	0.00	0.000	0.00	**6.6**
	Max Load	Adc	16.0	0.00	0.00	0.000	0.00	**52.8**
	Max Step Load	Adc	14.9	0.00	0.00	0.000	0.00	
	Max Slew Rate	A/uS	290[5]	0.00	0.00	0.000	0.00	
Mem. Bd.2	Min Load	Adc	2.00	0.00	0.00	0.000	0.00	**6.6**
	Max Load[6]	Adc	8.00	0.00	0.00	0.000	0.00	**26.4**
	Max Step Load	Adc	5.1	0.00	0.00	0.000	0.00	
	Max Slew Rate	A/uS	290[5]	0.00	0.00	0.000	0.00	
Midplane[7]	Min Load	Adc	0	0	0	0	0.01	**0.05**
	Max Load	Adc	0.01	0.01	0.10	0	0.02	**1.383**
Total Board Set	Tot Min Load	Adc	8.8	1.5	0.20	0	0.02	**39.18**
	Tot Max Step Load	Adc	23.15	13.83	24.0	0.25	0.14	
	Total Max Load	Adc	56.61	46.21	36.6	1	1.5	
	Total Max Power	W	186.813	231.05	439.2	12	7.5	**876.66**

Notes: There is no 240 VA protection circuit in the Ak450NX board set, except for current limiting on PHP slots (12, 5, 3 V rails).

1. 3.3 V current per PCI slot not to exceed 5 amps or 23 amps total for all PCI slots, 5 V current per PCI slot not to exceed 5 amps or 40 amps total for all PCI slots, 12 V current per PCI slot not to exceed 0.3 amps or 3 amps total for all PCI slots.

2. 3 amps maximum step load allowed total for PCI slots on 3.3 V, 12 amps maximum step load allowed total allowed for PCI slots on 5 V.

3. The current will depend on whether WOL is connected to the front panel or I/O baseboard. The cumulative 5 V standby current must not exceed 1.50 amps. The absolute maximum load on the front panel connector is 1.0 amp; maximum load on the I/O baseboard is 0.75 amp.

4. Numbers shown for CPU baseboard do not include power consumed by a front panel board connected throught the front panel board connector (J32). The max current that can be passed through this connector is 2 amps @ 5 V, 5.5 amps @ 12 V, 0.01 amp @ -12v, and 1 amp @ 5v stndby. No pins are provided for 3.3 V.

5. The extremely high slew rate of the memory boards is handled by a combination of ceramic, tantalum, and electrolytic capacitors. The duration of the steep slew rate is very short.

6. The cumulative maximum memory load is 24.0 amps, with the cumulative max step load at 20.0 amps

7. Numbers shown for midplane do not include power consumed through the peripheral power connector (J11). The max current that can be passed through this connector is 4.5 amps @ 5V, and 5.65 amps @ 12 V. No pins are provided for other voltages through this connector.

5.1.2   Absolute Maximum Ratings

Operation of the board set at conditions beyond those shown in Table 5-3 may cause permanent damage to the system. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5-3:   Absolute Maximum Ratings

Storage temperature	-55°C to +70°C
Voltage of any signal with respect to ground	-0.3 V to Vdd[†] + 0.3 V
+3.3 V supply with respect to ground	-0.3 V to +4.3 V
+5 V supply with respect to ground	-0.3 V to +6.5 V
+12 V supply with respect to ground	-0.3 V to 14 V

[†] Vdd means supply voltage for the device.

5.1.3   Voltage Timing and Sequencing

Table 5-4 describes the power up and power down timing requirements for the board set.

Table 5-4:   Ak450NX Board Set Voltage Timing and Sequencing Requirements

Parameter	Description	Specification
Trise-min	The fastest the voltages are allowed to rise. Measured from when the voltages begin to rise to when they begin to settle at the setpoint.	10 ms
Trise-max	Voltage Rise Time. The time it takes for all voltages (+3.3 V, +5 V, +12 V, -12 V) to be within their specified values from the time the voltages begin their rise from $V_{off\text{-}max}$.	350 ms. Must be monotonic starting 10 ms before power good assertion.
Toff	Minimum Voltage Off Time. The time the power supplies must be powered down before being powered back up again.	100 ms
Tsequence-on	Voltage sequencing during power on and off	None. All voltages can come up or down in any order as long as they meet the above timing requirements and reach specified values within 100 ms of each other.

All parameters measured at the sense points of the system. The above parameters apply to the main voltages only.

5.1.3.1   Standby Voltage Timing and Sequencing

The standby voltages are VCC5STBY and VBIAS; both must be at the setpoint at least 100 ms before the main voltages begin to rise. The standby voltages must remain at their setpoint at least 100 ms after the main voltages go down, regardless of the method of power loss, and even in situations of loss of AC power to the supplies.

5.1.4   Interfacing Requirements

In addition to the power supplies' maximum and minimum currents, voltages, etc., there are also requirements for the logic-level control signals, which interface interconnect midplane.

The PWR_GOOD signal originates on the interconnect midplane. It is the culmination of all signals from each power supply indicating that each has valid and stable power. This signal is delayed from the power good signals coming from each supply. When this signal is low, the system is either receiving some sort of (invalid) power from the power supplies AND is being held in the reset state, or the power supplies are off. The midplane requires only one supply indicating power good to assert system power good. The PWR_GOOD signal must meet the requirements found in Table 5-5.

Table 5-5:   Power Good (from Power Supply) Electrical Requirements

Parameter	Description	Value
V_{oh} minimum	Minimum digital output high voltage	+4.0 V into high speed CMOS inputs at 0.75 mA
V_{ol} maximum	Maximum digital output low voltage	+0.7 V into high speed CMOS inputs at 3.5 mA
$T_{rise\ min}$	PWR_GOOD rise time from V_{ol} to V_{oh}	2 µs into 2000 pf

5.1.5   Power Subsystem Timing Specifications

Figure 5-1 shows the power up sequence. The sequence is initiated by assertion of PS_ON or AC applied. PWR_GOOD is the OR'ing of the power good signals from each supply. PWR_GOOD is a delayed version of the power supply power good (PGOOD) signals. This signal is the power good indication to the system.

5.1.5.1   Turn On Timing Specifications

Table 5-6:   Turn On Timing Specifications

Turn-on	+3.3 Vdc	+5 Vdc	+12 Vdc
T_{CMD_ON} (ms)	1500 max	1500 max	1500 max
T_{RISE} (ms)	10 - 350	10 -350	10 – 350
$T_{ON\text{-}GD}$ (ms)	100-1500	100-1500	100-1500
T_{OFF_MIN} (ms)	350-500	350-500	350-500
Overshoot (Vdc)	None	None	None

Note: All times are in milliseconds

TURN-ON TIMING
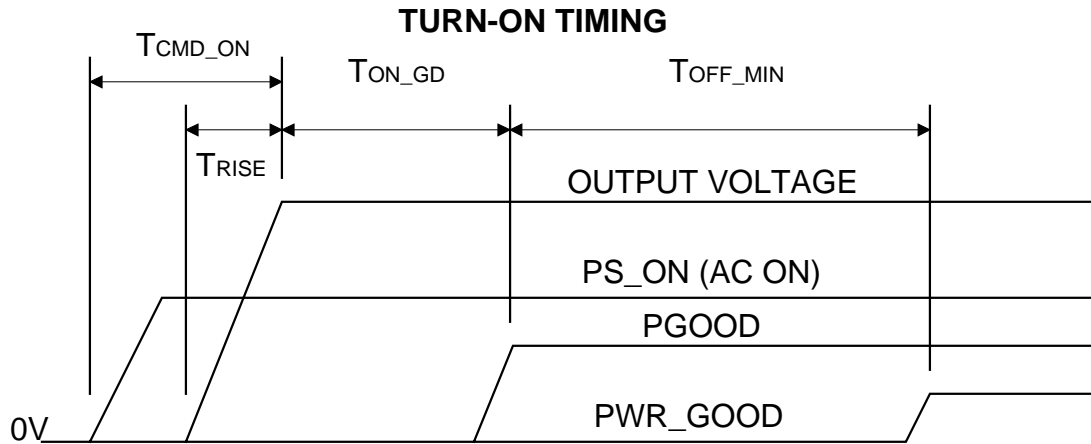
Note: t(PS_ON to PGOOD) must be greater than Trise.

Figure 5-1: Power Up Sequence

Figure 5-2 shows the power down sequence. The sequence is initiated by the front panel or other source such as interlock deasserting PS_ON, or loss of AC. At time T_{CMD_NGD} later PWR_GOOD is deasserted. This is followed at T_{NGD_DROP} time by power supplies going out of specification.

Table 5-7: Turn-off Timing Specifications

Turn-off Time	+3.3 Vdc	+5 Vdc	+12 Vdc
TCMD_NGD(ms)	0-13.5	0-13.5	0-13.5
TNGD_DROP(ms)	1 (min)	1 (min)	1 (min)
TCMD_DROP(sec)	10 (max)	10 (max)	10 (max)

TURN-OFF TIMING
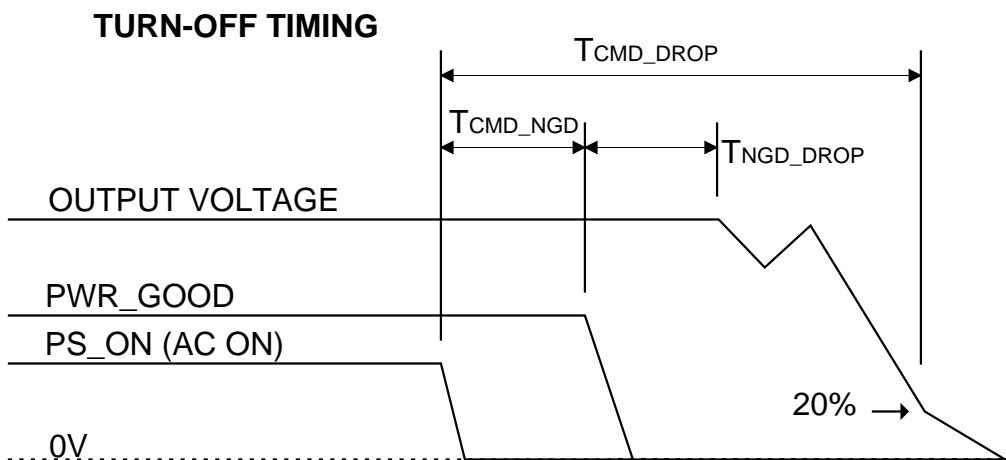
Figure 5-2: Power Down Sequence

5.2 Mechanical Specifications

This section describes the mechanical specifications of each board that make up the Ak450NX board set. The mechanical specifications are described by presentation of the specification drawing for each board.

5.2.1 PHP I/O Baseboard

The following diagrams show the mechanical specifications for the I/O baseboard and I/O riser card. All dimensions are given in inches. Connectors are dimensioned to pin 1.
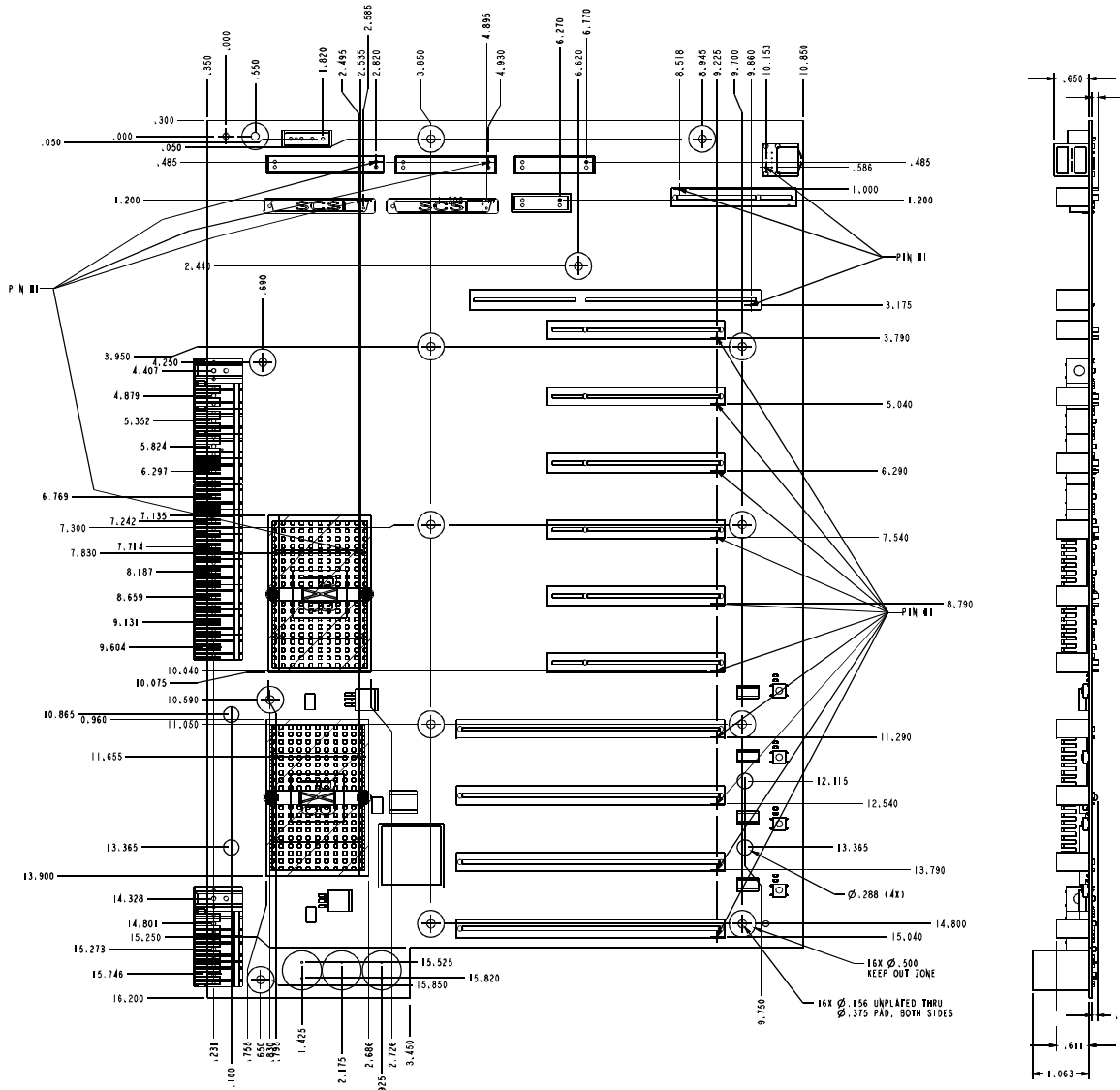
Figure 5-3: PHP I/O Baseboard Mechanical Diagram
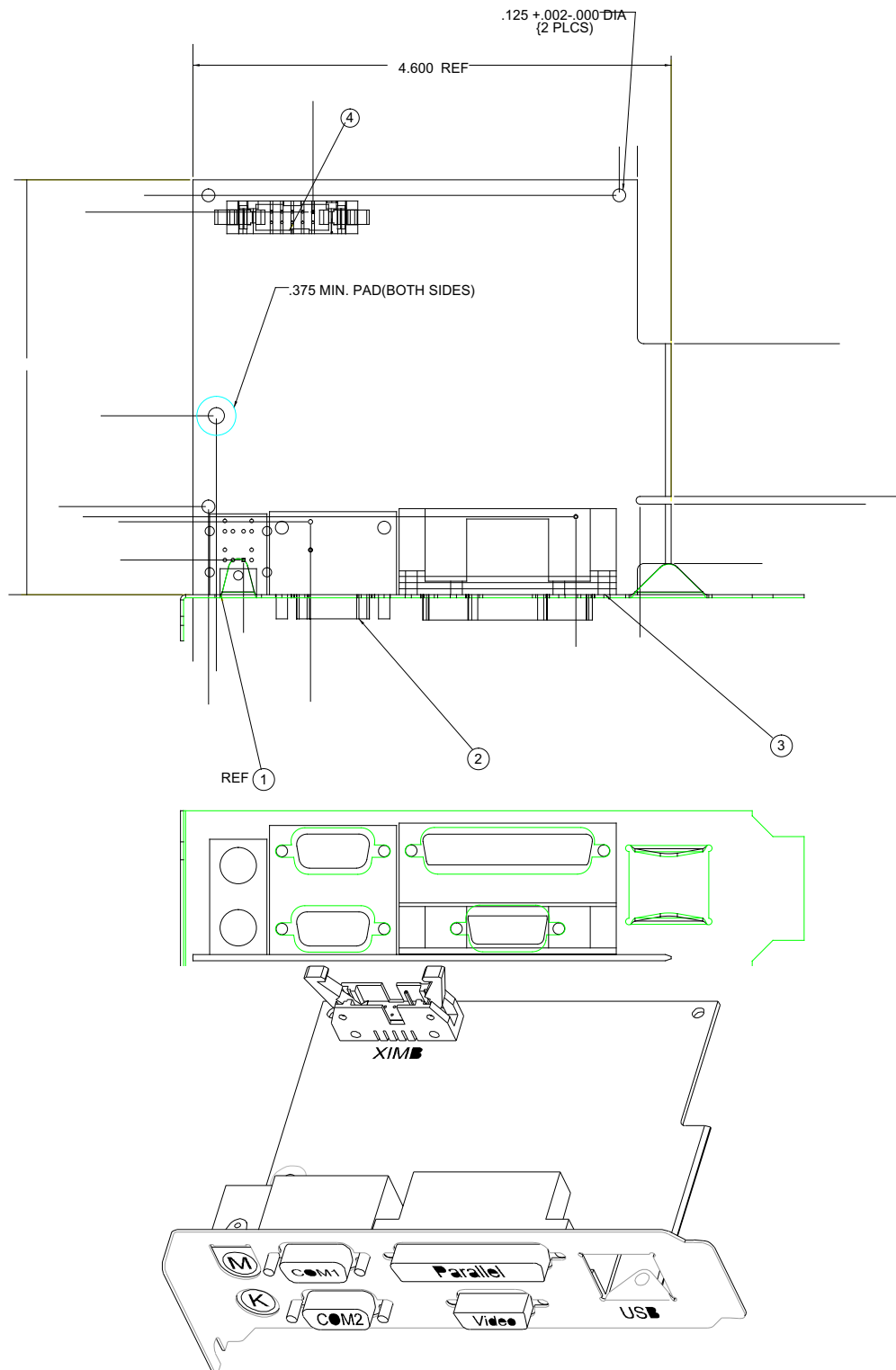
Figure 5-4: I/O Riser Card Mechanical Diagram

5.2.1.1   PXB Heat Sink

Both PXB components on the PHP I/O baseboard will have a heat sink attached as they are shipped from the manufacturing plant. The heat sink will be attached to the I/O baseboard via a retention clip and has the following dimensions: 2.74" X 1.785" X 0.39" tall. Figure 5-5 is a reference diagram for the PXB heat sink.
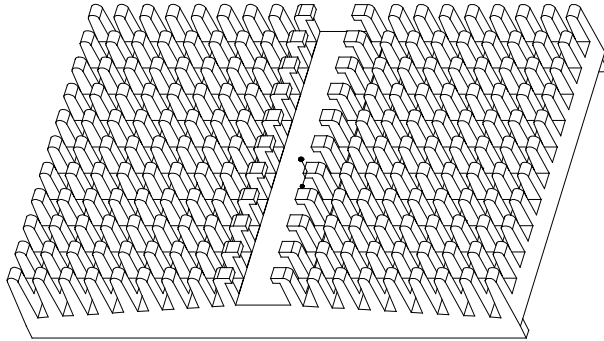
Figure 5-5: PXB Heat Sink

5.2.2 CPU Baseboard

Figure 5-6 diagrams the mechanical specifications and the connector positions for the CPU baseboard. The board outline dimensions are 16.5" x 10.25". All dimensions are given in inches.
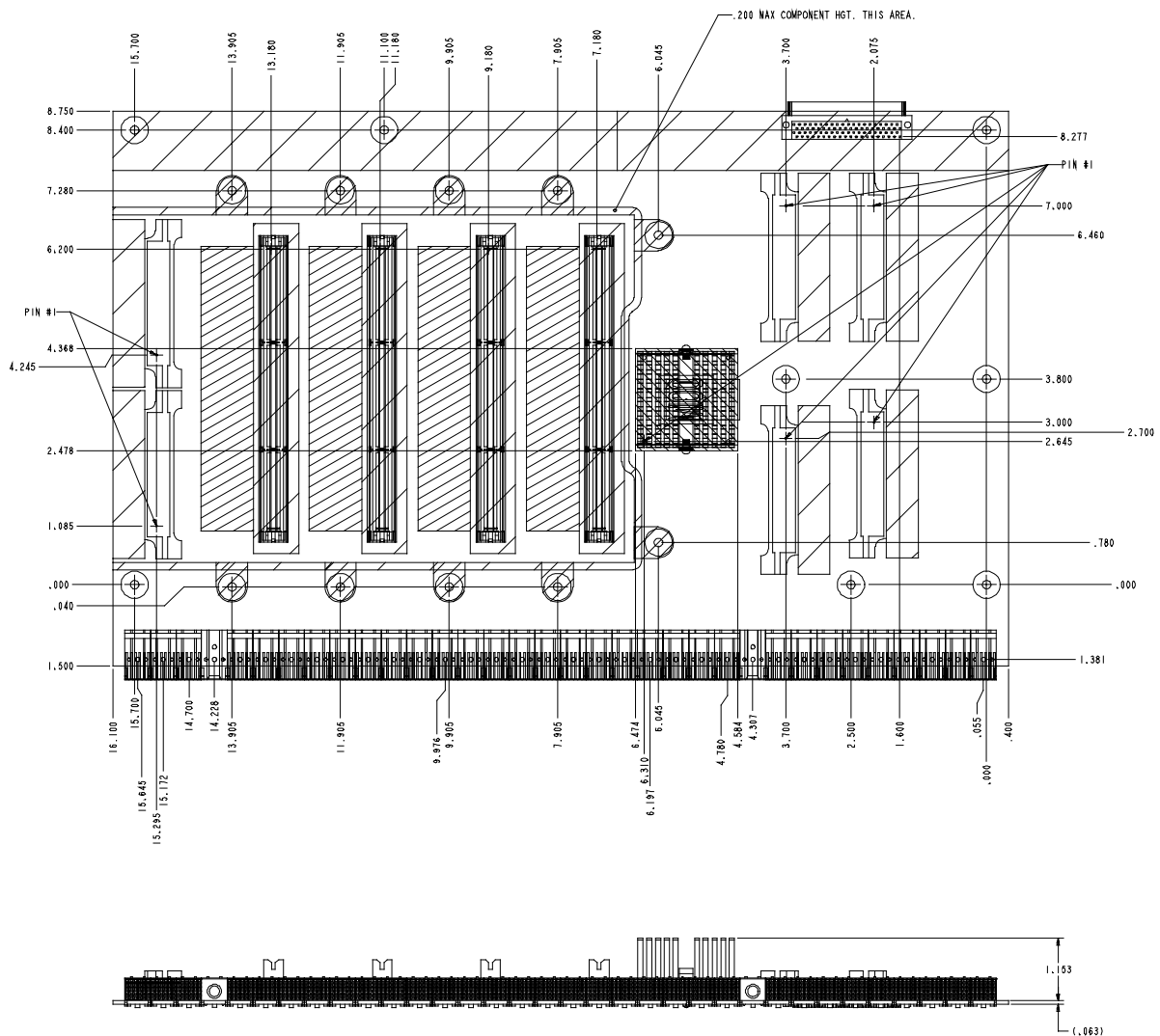
Figure 5-6: CPU Baseboard Mechanical Drawing

5.2.2.1   Processor Heat Sink

The suggested processor heat sink to be used with the Ak450NX board set and CPU baseboard is 5.20" x 4.24" x 1.00" and is attached to the processor heat plate with five screws. The heat sink will be manufactured with a pre-applied thermal interface material. The processor heat sink (with interface material) may be purchased from Intel or directly from Intel's vendor.
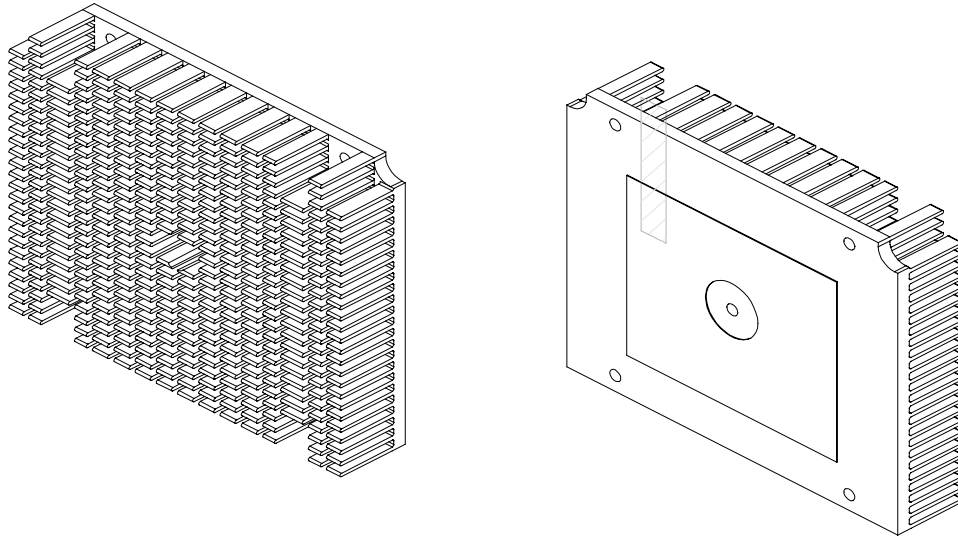
Figure 5-7: Processor Heat Sink

5.2.2.2   MIOC Heat Sink

The CPU baseboard's MIOC component will come from Intel's factory with a 1.75" x 1.75" x 1.0" heat sink with a pre-applied thermal interface material. The heat sink is attached with a clip, which is retained by the CPU baseboard. Figure 5-8 is a reference diagram for this heat sink.
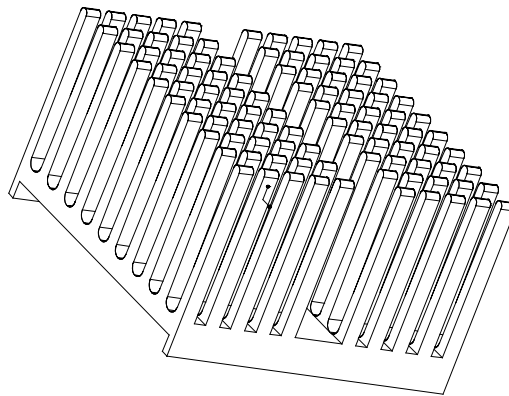
Figure 5-8: MIOC Heat Sink

5.2.3 Memory Module

Figure 5-9 shows the mechanical specifications of the memory module. All dimensions are given in inches.
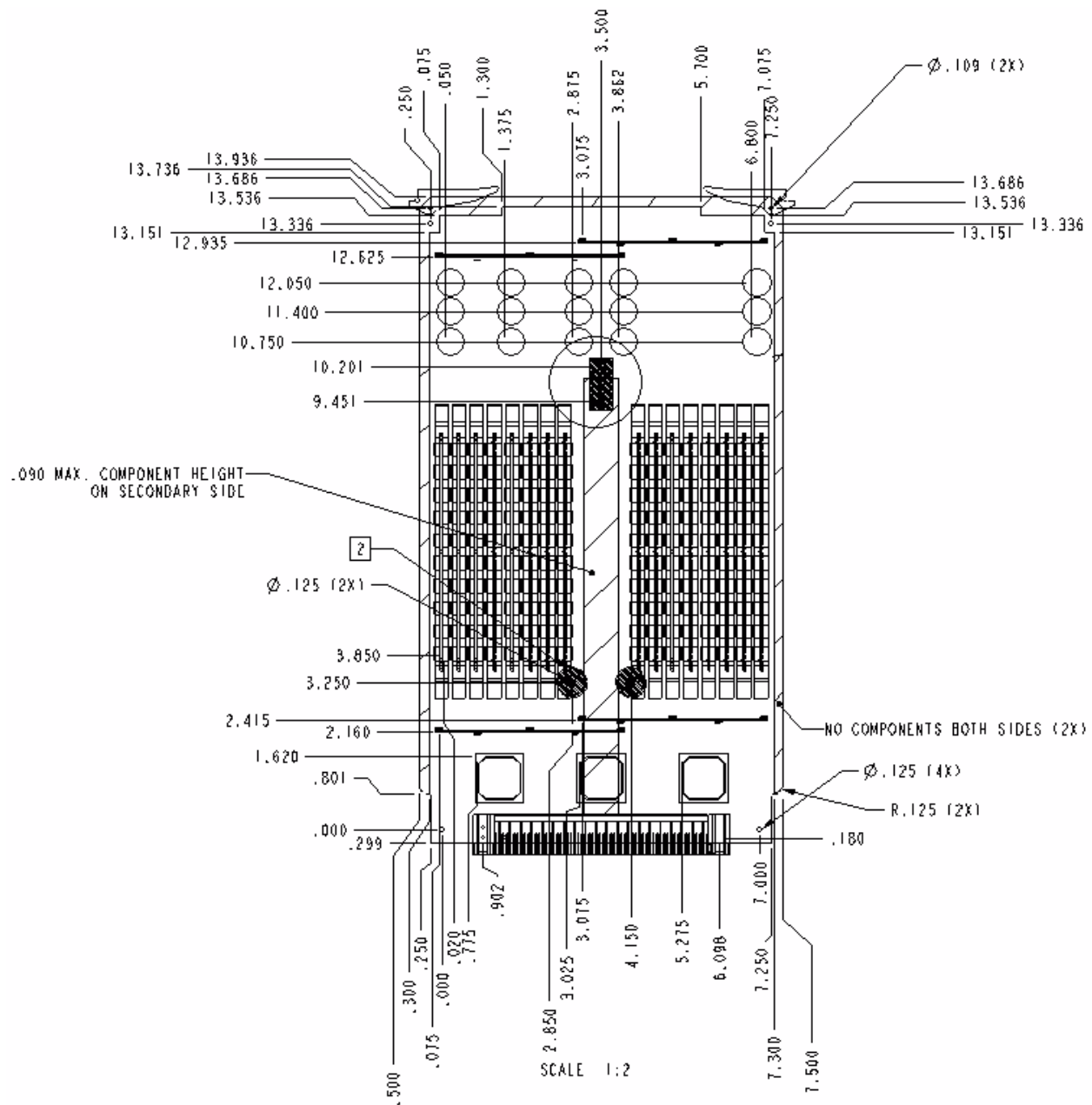
Figure 5-9: Memory Module Mechanical Specification

5.2.4   Interconnect Midplane

Figure 5-10 shows the mechanical specifications of the interconnect midplane. All dimensions are given in inches.
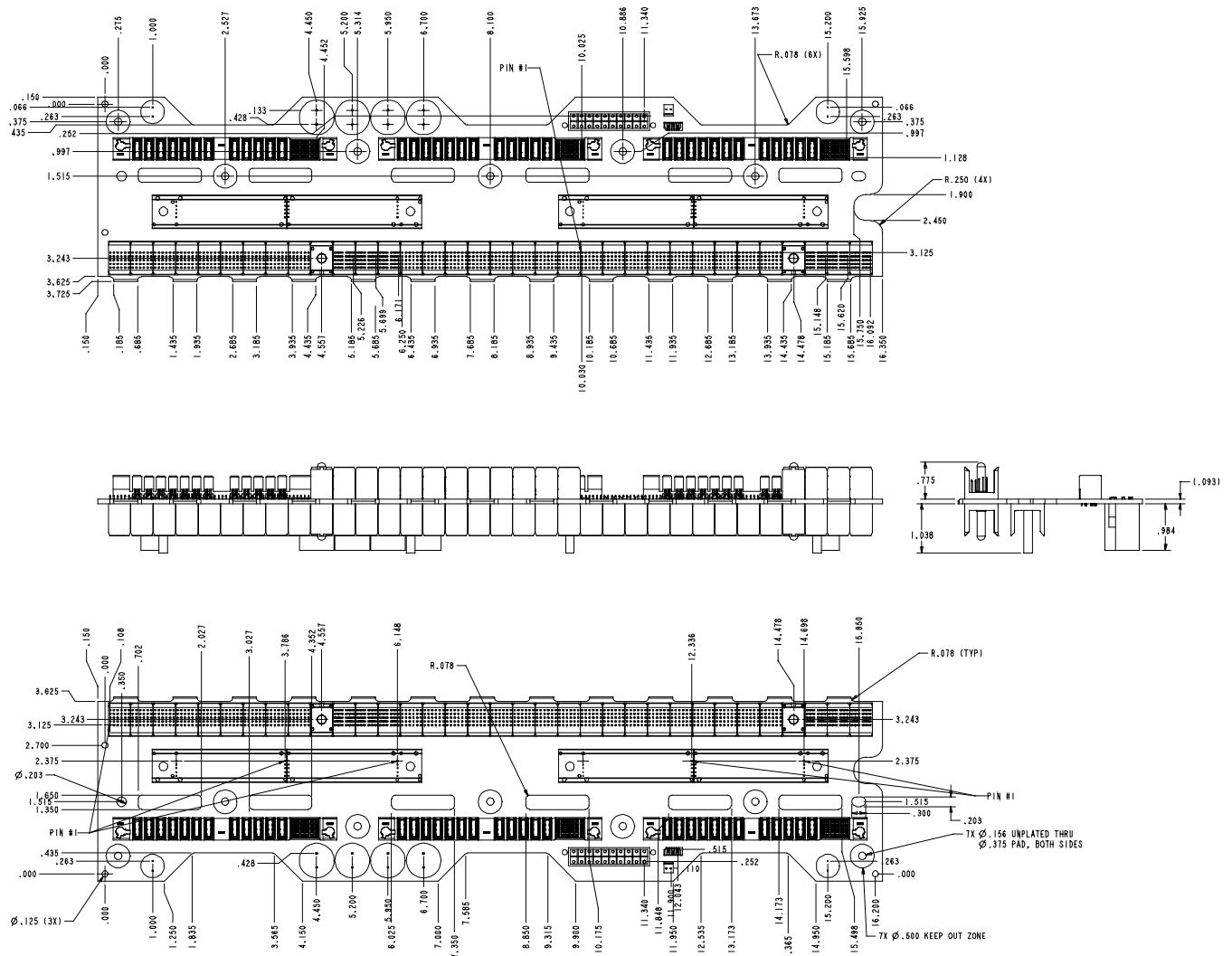
Figure 5-10:Interconnect Midplane Mechanical Diagram

5.2.5 Front-side Bus (FSB) Terminator Module

Figure 5-11 shows the mechanical specifications of the front side bus (FSB) terminator module. All dimensions are given in inches.
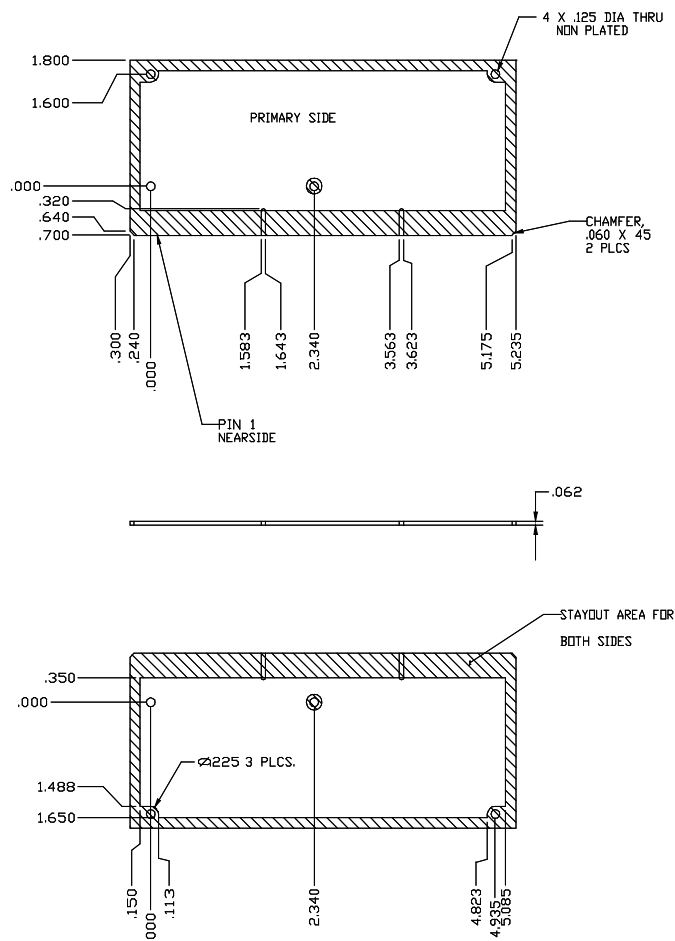
Figure 5-11:FSB Terminator Mechanical Drawing

5.3   Connector Specfication

5.3.1   PHP I/O Baseboard Connectors

Table 5-8 and Table 5-9 show the reference designators, quantity, manufacturer, and part number for each of the connectors used on the PHP I/O baseboard and I/O riser card. All remaining tables in this section describe the actual pinout of each connector.

Table 5-8:   PHP I/O Baseboard Connector Definitions

Item	Description	Connector Type [†]	Quantity	Locations
1	PCI connectors (64-bit)	AMP* 145034-1	4	P7-P10
2	PCI connectors (32-bit)	AMP 646255-1	6	P1–P6
3	ISA connector	AMP 176139-2	1	J3B1
4	Legacy connections	AMP 650090-3	1	J2A11
5				
6	SCSI connector	FOXCONN*/Hon Hai* QA01343-P4	2	J2G1,J2E1
7	Floppy disk port connection	AMP 111944-7	1	J1E2
8	IDE connector	AMP 111945-8	1	J1G2
9	Monoblock bus connector	BERG* 73956-9003	1	J5H1
10	Monoblock power module	BERG 73956-9004	6	J4H1B,J4H2C,J4H3D,J10H1B,J10H2C,J10H3D
11	USB connector	FOXCONN/Hon Hai UB1112C-D1	1	J1A1

† Representative manufacturer and part number.

Table 5-9:   I/O Risor Card Connector Definitions

Item	Description	Connector Type	Quantity	Locations
1	Multifunction Mouse Connector/Keyboard Connector	FOXCONN/Hon Hai* MH11063-D0	1	J4
2	Multifunction Dual Serial Port Connector	FOXCONN/Hon Hai DM10156-73	1	J5
3	Multifunction VGA Connector/Parallel Port Connection	AMP* 750433-2	1	J6
4	ICMB Cable Interface Connector	AMP 111988-1	1	J1

5.3.1.1   Monoblock Bus Connector Pinout

Table 5-10: F16 Connector Pinout

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
COM2_TO_FP_EN	A1	GND	B1	GND	C1	COM2_SIO_EN_A_	D1	PIC_CLK	E1
IO_TCK	A2	ICMB _SOUT_EN	B2	SIN_TTL_COM2	C2	STP_CLK_L	D2	GND	E2
IO_TDO	A3	GND	B3	IO_TMS	C3	IO_TRST_L	D3	PICD(1)	E3
BMC_SPI_BUS(1)	A4	IO_TDI	B4	PWRGDB	C4	PICD(0)	D4	GND	E4
BMC_SPI_BUS(6)	A5	GND	B5	A20M_L	C5	INIT_L	D5	RESET_PWR_DIST_L	E5
BMC_SPI_BUS(0)	A6	CPU_SPI_RESET_L	B6	PROC_RESET_L	C6	GND	D6	GND	E6

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
I2C_BMC_SCL	A7	GND	B7	GND	C7	BMC_SPI_BUS(2)	D7	BMC_SPI_BUS(4)	E7
I2C_BMC_SDA	A8	BMC_SPI_BUS(3)	B8	BMC_SPI_BUS(5)	C8	GND	D8	GND	E8
NMI_5V	A9	GND	B9	SMI_L	C9	X0IB_L	D9	CIB_INT0	E9
GND	A10	IGNNE_L	B10	I2C_GLOBAL_SDA	C10	IO_PWRGD	D10	GND	E10
X0D_L(0)	A11	GND	B11	GND	C11	I2C_GLOBAL_SCL	D11	INTR	E11
X0D_L(1)	A12	X0XRTS_L	B12	X0HRTS_L	C12	GND	D12	GND	E12
X0D_L(3)	A13	GND	B13	GND	C13	DSEL0_L	D13	FERR_L	E13
X0D_L(4)	A14	X0D_L(2)	B14	X0BE_L(0)	C14	GND	D14	GND	E14
GND	A15	GND	B15	GND	C15	DCMPLTA_L	D15	X0BLK_L	E15
X0D_L(6)	A16	X0D_L(5)	B16	X0PAR_L	C16	GND	D16	GND	E16
X0D_L(8)	A17	GND	B17	GND	C17	SIN_TTL_ICMB	D17	X0RST_L	E17
X0D_L(9)	A18	X0D_L(7)	B18	X0ADS_L	C18	GND	D18	GND	E18
GND	A19	GND	B19	X0D_L(11)	C19	SOUT_TTL_COM2	D19	SOUT_TTL_ICMB	E19
X0D_L(12)	A20	X0D_L(10)	B20	X0BE_L(1)	C20	GND	D20	DCD_TTL_FP	E20
X0D_L(14)	A21	GND	B21	X0XSTBN_L	C21	X0XSTBP_L	D21	GND	E21
X0D_L(15)	A22	X0D_L(13)	B22	GND	C22	GND	D22	WDEVT_L	E22
GND	A23	GND	B23	DOFF0_L	C23	X0HSTBP_L	D23	GND	E23
X0CLK	A24	GND	B24	GND	C24	X0HSTBN_L	D24	DCMPLTB_L	E24
GND	A25	DVALIDA_L	B25	DSR_TTL_FP	C25	ISP_MODE	D25	ISP_EN_L	E25
CTS_TTL_FP	A26	DOFF1_L	B26	GND	C26	ISP_CLK	D26	GND	E26
RI_TTL_FP	A27	GND	B27	ISP_FPC_SDO	C27	ISP_FPC_EN_L	D27	(-12V)	E27
ISP_SDO	A28	RTS_TTL_FP	B28	GND	C28	(-12V)	D28	GND	E28
INTRUSION_L	A29	GND	B29	DTR_TTL_FP	C29	DVALIDB_L	D29	CPU_SLP_L	E29
ISP_SDI	A30	FAN_FAILED	B30	SPEAKER_DATA	C30	GND	D30	GND	E30
VCC_STDBY	A31	GND	B31	GND	C31	FP_T0_PIIX4_PWRBTN	D31	SECURE_MODE_BMC	E31
I2C_FPC_SCL	A32	VCC_STDBY	B32	HARD_RESET	C32	DSEL1_L	D32	GND	E32
I2C_FPC_SDA	A33	GND	B33	GND	C33	X1IB_L	D33	PWR_GOOD	E33
GND	A34	I2C_DS2P_SDA	B34	I2C_DS2P_SCL	C34	PS_PWR_ON	D34	GND	E34
X1D_L(0)	A35	GND	B35	GND	C35	FP_NMI_SWT_L	D35	PWR_CNTR_SFC	E35
X1D_L(1)	A36	X1XRTS_L	B36	X1HRTS_L	C36	GND	D36	GND	E36
X1D_L(3)	A37	GND	B37	GND	C37	PWR_CNTR_RTC_L	D37	I2C_CEL_CONNECT_FPC	E37
X1D_L(4)	A38	X1D_L(2)	B38	X1BE_L(0)	C38	GND	D38	GND	E38
GND	A39	GND	B39	GND	C39	I2C_CEL CONNECT_BMC	D39	X1BLK_L	E39
X1D_L(6)	A40	X1D_L(5)	B40	X1PAR_L	C40	GND	D40	GND	E40
X1D_L(8)	A41	GND	B41	GND	C41	I2C_BACKUP_SCL	D41	X1RST_L	E41
X1D_L(9)	A42	X1D_L(7)	B42	X1ADS_L	C42	GND	D42	GND	E42
GND	A43	GND	B43	X1D_L(11)	C43	I2C_BACKUP_SDA	D43	MIOC_INTREQ_L	E43
X1D_L(12)	A44	X1D_L(10)	B44	X1BE_L(1)	C44	GND	D44	GND	E44
X1D_L(14)	A45	GND	B45	X1XSTBN_L	C45	X1XSTBP_L	D45	GND	E45
X1D_L(15)	A46	X1D_L(13)	B46	GND	C46	GND	D46	GND	E46
GND	A47	GND	B47	5V_SENSE	C47	X1HSTBP_L	D47	GND	E47
X1CLK	A48	5V_RET_SENSE	B48	GND	C48	X1HSTBN_L	D48	GND	E48

5.3.1.2   PCI Connectors (32-Bit) Pinout

Table 5-11: PCI Connectors (32-bit)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TRST_L	A32	AD16	B1	-12V	B32	AD17
A2	+12V	A33	+3.3V	B2	TCK	B33	C/BE2_L
A3	TMS	A34	FRAME_L	B3	GND	B34	GND
A4	TDI	A35	GND	B4	TDO	B35	IRDY_L
A5	+5V	A36	TRDY_L	B5	+5V	B36	+3.3V
A6	INTA_L	A37	GND	B6	+5V	B37	DEVSEL_L
A7	INTC_L	A38	STOP_L	B7	INTB_L	B38	GND
A8	+5V	A39	+3.3V	B8	INTD_L	B39	LOCK_L
A9	RESERVED	A40	SDONE	B9	PRSNT1_L	B40	PERR_L
A10	+5V	A41	SB0_L	B10	RESERVED	B41	+3.3V
A11	RESERVED	A42	GND	B11	PRSNT2_L	B42	SERR_L
A12	GND[†]	A43	PAR	B12	GND[†]	B43	+3.3V
A13	GND[†]	A44	AD15	B13	GND[†]	B44	C/BE1_L

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A14	RESERVED	A45	+3.3V	B14	RESERVED	B45	AD14
A15	RESET_L	A46	AD13	B15	GND	B46	GND
A16	+5V	A47	AD11	B16	CLK	B47	AD12
A17	GRANT_L	A48	GND	B17	GND	B48	AD10
A18	GND	A49	AD9	B18	REQ_L	B49	GND
A19	RESERVED	A50		B19	+5V	B50	
A20	AD30	A51		B20	AD31	B51	
A21	+3.3V	A52	C/BE0_L	B21	AD29	B52	AD8
A22	AD28	A53	+3.3V	B22	GND	B53	AD7
A23	AD26	A54	AD6	B23	AD27	B54	+3.3V
A24	GND	A55	AD4	B24	AD25	B55	AD5
A25	AD24	A56	GND	B25	+3.3V	B56	AD3
A26	IDSEL	A57	AD2	B26	C/BE3_L	B57	GND
A27	+3.3V	A58	AD0	B27	AD23	B58	AD1
A28	AD22	A59	+5V	B28	GND	B59	+5V
A29	AD20	A60	REQ64_L	B29	AD21	B60	ACK64_L
A30	GND	A61	+5V	B30	AD19	B61	+5V
A31	AD18	A62	+5V	B31	+3.3V	B62	+5V

† Indicates slot serves +5 V compliant devices only.

5.3.1.3　　PCI Connector (64-Bit) Pinout

The 64-bit PCI connector is identical to a 32-bit PCI connector for pins A1-A62 and B1-B62. Table 5-12 indicates the extension pins necessary for PCI-64 compliance.

Table 5-12: PCI Connectors (64-bit)

Pin	Signal	Pin	Signal
A63	GND	B63	RESERVED
A64	C/BE7_L	B64	GND
A65	C/BE5_L	B65	C/BE6_L
A66	+5V	B66	C/BE4_L
A67	PAR64	B67	GND
A68	AD62	B68	AD63
A69	GND	B69	AD61
A70	AD60	B70	+5V
A71	AD58	B71	AD59
A72	GND	B72	AD57
A73	AD56	B73	GND
A74	AD54	B74	AD55
A75	+5V	B75	AD53
A76	AD52	B76	GND
A77	AD50	B77	AD51
A78	GND	B78	AD49
A79	AD48	B79	+5V
A80	AD46	B80	AD47
A81	GND	B81	AD45
A82	AD44	B82	GND
A83	AD42	B83	AD43
A84	+5V	B84	AD41
A85	AD40	B85	+5V
A86	AD38	B86	AD39
A87	GND	B87	AD37
A88	AD36	B88	+5V
A89	AD34	B89	AD35
A90	GND	B90	AD33

Pin	Signal	Pin	Signal
A91	AD32	B91	GND
A92	RESERVED	B92	RESERVED
A93	GND	B93	RESERVED
A94	RESERVED	B94	GND

5.3.1.4   SCSI Connector Pinout

Table 5-13: SCSI Connector

Signal Name	Conn. Pin	Cable Pin	Cable Pin	Conn. Pin	Signal Name
GROUND	1	1	2	35	-DB(12)
GROUND	2	3	4	36	-DB(13)
GROUND	3	5	6	37	-DB(14)
GROUND	4	7	8	38	-DB(15)
GROUND	5	9	10	39	-DB(P1)
GROUND	6	11	12	40	-DB(0)
GROUND	7	13	14	41	-DB(1)
GROUND	8	15	16	42	-DB(2)
GROUND	9	17	18	43	-DB(3)
GROUND	10	19	20	44	-DB(4)
GROUND	11	21	22	45	-DB(5)
GROUND	12	23	24	46	-DB(6)
GROUND	13	25	26	47	-DB(7)
GROUND	14	27	28	48	-DB(P)
GROUND	15	29	30	49	GROUND
GROUND	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED (NC)	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
GROUND	21	41	42	55	-ATN
GROUND	22	43	44	56	GROUND
GROUND	23	45	46	57	-BSY
GROUND	24	47	48	58	-ACK
GROUND	25	49	50	59	-RST
GROUND	26	51	52	60	-MSG
GROUND	27	53	54	61	-SEL
GROUND	28	55	56	62	-C/D
GROUND	29	57	58	63	-REQ
GROUND	30	59	60	64	-I/O
GROUND	31	61	62	65	-DB(8)
GROUND	32	63	64	66	-DB(9)
GROUND	33	65	66	67	-DB(10)
GROUND	34	67	68	68	-DB(11)

5.3.1.5   ISA Connector Pinout

Table 5-14: ISA Connector

Pin	Signal	Pin	Signal
B1	GND	A1	IOCHK_L
B2	RESET	A2	SD7
B3	+5V	A3	SD6
B4	IRQ9	A4	SD5

Pin	Signal	Pin	Signal
B5	-5V	A5	SD4
B6	DRQ2	A6	SD3
B7	-12V	A7	SD2
B8	SRDY_L	A8	SD1
B9	+12V	A9	SD0
B10	GND	A10	IOCHRDY
B11	SMEMW_L	A11	AEN
B12	SMEMR_L	A12	SA19
B13	IOW_L	A13	SA18
B14	IOR_L	A14	SA17
B15	DACK#_3	A15	SA16
B16	DRQ3	A16	SA15
B17	DACK1_L	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH	A19	SA12
B20	BCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DACK2_L	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	+5V	A29	SA2
B30	14Mhz	A30	SA1
B31	GND	A31	SA0
D1	MEMCS16_L	C1	SGHE_I
D2	IOCS16_L	C2	LA23
D3	IRQ10	C3	LA22
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14D	C7	LA18
D8	ACK0_L	C8	LA17
D9	DRQ0	C9	MEMR_L
D10	DACK5_L	C10	MEMW_L
D11	DRQ5	C11	SD8
D12	DACK6_L	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7_L	C14	SD11
D15	DRQ7	C15	SD12
D16	+5v	C16	SD13
D17	MASTER16_L	C17	SD14
D18	GND	C18	SD15

5.3.1.6   IDE Connector Pinout

Table 5-15: IDE Connector

Pin	Signal	Pin	Signal
1	RSTDRV	2	GROUND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD1

Pin	Signal	Pin	Signal
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GROUND	20	KEY PIN
21	DRQ	22	GROUND
23	DIOW	24	GROUND
25	DIOR	26	GROUND
27	IORDY	28	CSEL
29	DACK	30	GROUND
31	IRQ	32	No Connection
33	DA1	34	No Connection
35	DA0	36	DA2
37	CS1P_L	38	DS3P_L
39	DHACT_L	40	GROUND

5.3.1.7   Floppy Disk Port Connector Pinout

Table 5-16: Floppy Disk Connector

Pin	Name	Pin	Name
1	GND	2	FD_DENSEL
3	GND	4	n/c
5	Key	6	FD_DRATE0
7	GND	8	FD_INDEX_L
9	GND	10	FD_MTR0_L
11	GND	12	FD_DR1_L
13	GND	14	FD_DR0_L
15	GND	16	FD_MTR1_L
17	FD_MSEN1	18	FD_DIR_L
19	GND	20	FD_STEP_L
21	GND	22	FD_WDATA_L
23	GND	24	FD_WGATE_L
25	GND	26	FD_TRK0_L
27	FD_MSEN0	28	FD_WPROT_L
29	GND	30	FD_RDATA_L
31	GND	32	FD_HDSEL_L
33	GND	34	FD_DSKCHG_L

5.3.1.8   USB Connector Pinout

Table 5-17: USB Connector

Pin	Signal	Description
A1	VCC	Over Current Monitor Line Port 0
A2	DATAL0	Differential Data Line Paired with DATAH0
A3	DATAH0	Differential Data Line Paired with DATAL0
A4	GND	Ground Potential
B1	VCC	Over Current Monitor Line Port 1
B2	DATAL1	Differential Data Line Paired with DATAH1
B3	DATAH1	Differential Data Line Paired with DATAL1
B4	GND	Ground Potential

5.3.1.9   I²C Feature Connector Pinout

Table 5-18: I²C Feature Connector Pin Assignments

Pin	Name	Pin	Name
1	SMI#	2	I2CCLK
3	CONP	4	key
5	PWROFF#	6	I2CDATA
7	LPOK	8	KEYUNLK
9	NMI	10	HostAUX
11	RESET#	12	GND
13	GND	14	key
15	SECURE	16	GND
17	INTRUD#	18	NMI_L
19	INIT_L	20	GND
21	KB_DATA	22	MS_DATA
23	KB_CLK	24	MS_CLK
25	Key	26	RESET_BMC_L

5.3.1.10   I²C Connector Pinout

Table 5-19: I²C Connector

Name	Pin
CLK	1
GND	2
DATA	3

5.3.1.11   Legacy Connections – Via I/O Riser Card

The I/O baseboard provides connection to VGA, serial, parallel, mouse, and keyboard functions by means of an I/O riser card mounted to the baseboard. The I/O riser card provides the direct user interface. The following sections provide the pinout of the user level interfaces of the I/O riser card.

Table 5-20: Legacy Connections

Pin	Signal	Pin	Signal
A1	VCC_STDBY	B1	+5V
A2	KB_DATA	B2	MS_DATA
A3	KB_CLK	B3	MS_CLK
A4	+5V	B4	SIN_TTL_XIMB
A5	SOUT_TTL_XIMB	B5	SIN_TTL_COM2
A6	PP_SLCT	B6	SP0_DCD_L
A7	PP_PE	B7	SP1_DCD_L
A8	PP_BUSY	B8	SP0_SIN
A9	PP_ACK_L	B9	Ground
A10	Ground	B10	SP1_SIN
A11	PP_DR7	B11	SP0_RI_L
A12	PP_DR6	B12	SP1_RI_L
A13	PP_DR5	B13	Ground
A14	PP_DR4	B14	SP0_DTR_L
A15	Ground	B15	SP1_DTR_L
A16	PP_DR3	B16	SP0_SOUT
A17	PP_DR2	B17	SP1_SOUT

Pin	Signal	Pin	Signal
A18	PP_DR1	B18	No Connection
A19	PP_DR0	B19	SP0_DSR_L
A20	Ground	B20	SP1_DSR_L
A21	PP_STB_L	B21	SP0_RTS_L
A22	PP_SLIN_L	B22	Ground
A23	PP_INIT_L	B23	SP1_RTS_L
A24	PP_ERR_L	B24	SP0_CTS_L
A25	PP_AFD_L	B25	SP1_CTS_L
A26	I2C_BMC_SCL	B26	RTL_TTL_FP_L
A27	DSR_TTL_FP	B27	DTR_TTL_FP_L
A28	CTS_TTL_FP	B28	DCD_TTL_FP_L
A29	RT_TTL_FP	B29	I2C_BMC_SDA
A30	COM2_TO_STD_EN	B30	XIMB_SOUT_EN
A31	COM2_TO_FP_EN	B31	SOUT_TTL_COM2
A32	Ground	B32	PWR_GOOD
A33	Ground	B33	Ground
A34	Ground	B34	Ground
A35	V_BLUE	B35	V_VSYNC
A36	Ground	B36	Ground
A37	V_GREEN	B37	V_HSYNC
A38	Ground	B38	Ground
A39	V_RED	B39	VR_DDCDAT
A40	Ground	B40	VR_DDCCLK

The "B" signals listed above are located on the primary side of the I/O riser card (USB connector side if looking at the I/O baseboard). The "A" signals are located on the secondary side of the I/O riser card (ISA slot side if looking at the I/O baseboard). Pin 1 is located nearest toward the front of the card (away from the connectors on the I/O riser card and toward the PXB heatsinks). Pin 40 is located nearest the connectors.

5.3.1.11.1   VGA Connector Pinout (I/O Riser Card)

Table 5-21: Video Port Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	RED	Analog color signal R	2	GREEN	Analog color signal G
3	BLUE	Analog color signal B	4	n/c	No connect
5	GND	Video ground (shield)	6	GND	Video ground (shield)
7	GND	Video ground (shield)	8	GND	Video ground (shield)
9	n/c	No connect	10	GND	Video ground
11	n/c	No connect	12	n/c	No connect
13	HSYNC	Horizontal sync	14	VSYNC	Vertical sync
15	n/c	No connect			

5.3.1.11.2   Serial Port Connector Pinout (I/O Riser Card)

Table 5-22: Serial Port Connector

Pin	Name	Description	Pin	Name	Description
1	DCD	Data Carrier Detected	2	RXD	Receive Data
3	TXD	Transmit Data	4	DTR	Data Terminal Ready
5	GND	Ground	6	DSR	Data Set Ready
7	RTS	Return to Send	8	CTS	Clear to Send
9	RIA	Ring Indication Active			

The I/O baseboard uses a connector equivalent to a FOXCONN/Hon Hai DM10156-73* connector to interface with each serial port.

5.3.1.11.3   Parallel Port Connection Pinout (I/O Riser Card)

Table 5-23: Parallel Port Connection

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

5.3.1.11.4   Mouse Connector Pinout (I/O Riser Card)

Table 5-24: Mouse Connector

Pin	Signal	Description
7	MSEDAT	Mouse Data
8	(NC)	
9	GND	
10	FUSED_VCC	
11	MSECLK	Mouse Clock
12	(NC)	

5.3.1.11.5   Keyboard Connector Pinout (I/O Riser Card)

Table 5-25: Keyboard Connector

Pin	Signal	Description
1	KEYDAT	Keyboard Data
2	(NC)	

Pin	Signal	Description
3	GND	
4	FUSED_VCC	
5	KEYCLK	Keyboard Clock
6	(NC)	

5.3.2 CPU Baseboard Connectors

Table 5-26 shows the reference designators, quantity, manufacturer, and part number for connectors on the CPU baseboard. All remaining tables in this section describe the actual pinout of each connector.

Table 5-26: Baseboard Connector Specifications

Item	Reference Designator(s)	Quantity	Manufacturer and Part Number	Description
1	J10, J11, J12, J13	4	MOLEX* 71109-5005	Slot 2 connector 330-pin.
2	J1, J2, J3, J4, J5, J6	6	BERG* 95798-202	VRM 8 socket 40-pin.
4	J20, J23	2	BERG 73945-1002	Memory connector 270-pin (5x54) Futurebus+.
5	J22	1	BERG 89095-102	I/O connector 240-pin (5x48) Futurebus+.
6	J21, J24	2	BERG 73951-1007	Power connector 90-pin (5x18) + guide receptacle Futurebus+.
7	J32	1	AMP* 2-557101-1	Front panel connector 80-pin.
8	J31	1	MOLEX 90367-7015	Jumper block.

The CPU baseboard interfaces to the midplane through one large, 960-pin Berg Futurebus+* style connector. This connector, termed the grand connector, consists of one 240-pin signal module (I/O connector), two 270-pin signal modules (memory connector), and two 90-pin power modules. A 1:1 signal/ground ratio for all high-speed signals is maintained while lower speed signals use a 2:1 signal/ground ratio.

5.3.2.1 Memory Connector Pinout

The CPU baseboard memory bus connects to the midplane mostly through the memory connectors, the two 270-pin signal modules of the grand connector. Each of the two memory modules interfaces through one of these connectors. To achieve a 1:1 signal/ground ratio, half of the signal pins of each connector are connected to ground. Table 5-27 gives the pinout for these connectors. Each pin is rated at 1 A. Nine additional memory bus control signals connect to the midplane through the I/O connector (DOFF0_L, DOFF1_L, DVALIDA_L, DVALIDB_L, DCMPLTA_L, DCMPLTB_L, DSEL0_L, DSEL1_L, and WDEVT_L). Refer to the I/O connector pinout in Table 5-28. Note that in Table 5-27, signals marked with parentheses and *no* comma indicate one signal of a bus, for example ADDRESS(1). Signals marked with square brackets and *one* comma indicate a single signal which is differentiated between the two memory connectors (first connector 1, then connector 2); for example, EXAMPLE_SIGNAL[A,B]_L would refer to two similar signals that appear on the same pin at each connector, one of which is EXAMPLE_SIGNALA_L and the other of which is EXAMPLE_SIGNALB_L.

Table 5-27: CPU Baseboard Memory Connector Pinout

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
MD_L(35)	A1	GND	B1	MD_L(34)	C1	GND	D1	MD_L(33)	E1
GND	A2	MD_L(32)	B2	GND	C2	MD_L(31)	D2	+1.5V	E2
MD_L(30)	A3	GND	B3	DSTBN_L(1)	C3	GND	D3	MD_L(29)	E3
GND	A4	MD_L(28)	B4	GND	C4	MD_L(27)	D4	GND	E4
MD_L(26)	A5	GND	B5	DSTBP_L(1)	C5	GND	D5	MD_L(25)	E5
GND	A6	MD_L(24)	B6	GND	C6	MD_L(23)	D6	+1.5V	E6

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
MD_L(22)	A7	GND	B7	MD_L(21)	C7	GND	D7	MD_L(20)	E7
GND	A8	GND	B8	GND	C8	MD_L(19)	D8	GND	E8
MUXCLK0[A,B]	A9	GND	B9	MD_L(17)	C9	GND	D9	MD_L(18)	E9
GND	A10	GND	B10	GND	C10	Reserved	D10	GND	E10
MRESET_L	A11	GND	B11	Reserved	C11	GND	D11	Reserved	E11
GND	A12	MD_L(16)	B12	GND	C12	MD_L(15)	D12	+1.5V	E12
MD_L(14)	A13	GND	B13	MD_L(13)	C13	GND	D13	MD_L(12)	E13
GND	A14	MD_L(11)	B14	GND	C14	MD_L(10)	D14	GND	E14
MD_L(9)	A15	GND	B15	DSTBP_L(0)	C15	GND	D15	MD_L(8)	E15
GND	A16	MD_L(7)	B16	GND	C16	MD_L(6)	D16	+1.5V	E16
MD_L(5)	A17	GND	B17	DSTBN_L(0)	C17	GND	D17	MD_L(4)	E17
GND	A18	MD_L(3)	B18	GND	C18	GND	D18	GND	E18
MD_L(2)	A19	GND	B19	MD_L(1)	C19	GND	D19	RCGCLK1[A,B]	E19
GND	A20	MD_L(0)	B20	GND	C20	GND	D20	GND	E20
MEM[A,B]_TCK	A21	GND	B21	MEMA_TDI	C21	GND	D21	MEM[A,B]_TMS	E21
GND	A22	MEM[A,B]_TRST_L	B22	GND	C22	GND	D22	MA_L(13)	E22
MA_(12)	A23	GND	B23	MA_L(11)	C23	GND	D23	MA_L(10)	E23
GND	A24	MA_L(9)	B24	GND	C24	MA_L(8)	D24	+1.5V	E24
MA_L(7)	A25	GND	B25	MA_L(6)	C25	GND	D25	MA_L(5)	E25
GND	A26	MA_L(4)	B26	GND	C26	GND	D26	GND	E26
MA_L(3)	A27	GND	B27	MA_L(2)	C27	GND	D27	RCGCLK0 [A,B]	E27
GND	A28	MA_L(1)	B28	GND	C28	GND	D28	GND	E28
MA_L(0)	A29	GND	B29	CSTB_L	C29	GND	D29	ROW_L	E29
GND	A30	CMND1_L	B30	GND	C30	BANK0_L	D30	+1.5V	E30
BANK1_L	A31	GND	B31	BANK2_L	C31	GND	D31	CMND0_L	E31
GND	A32	CARD[0,1]_L	B32	GND	C32	GND	D32	GND	E32
PHIT[A,B]_L	A33	GND	B33	RCMPLT[A,B]_L	C33	GND	D33	SDRAM[A,B]_CLK	E33
GND	A34	RHIT[A,B]_L	B34	GND	C34	GND	D34	GND	E34
Reserved	A35	GND	B35	Reserved	C35	GND	D35	Reserved	E35
GND	A36	MD_L(71)	B36	GND	C36	MD_L(70)	D36	Reserved	E36
MD_L(69)	A37	GND	B37	MD_L(68)	C37	GND	D37	MD_L(67)	E37
GND	A38	MD_L(66)	B38	GND	C38	MD_L(65)	D38	+1.5V	E38
MD_L(64)	A39	GND	B39	DSTBN_L(3)	C39	GND	D39	MD_L(63)	E39
GND	A40	MD_L(62)	B40	GND	C40	MD_L(61)	D40	GND	E40
MD_L(60)	A41	GND	B41	DSTBP_L(3)	C41	GND	D41	MD_L(59)	E41
GND	A42	GND	B42	GND	C42	MD_L(58)	D42	GND	E42
MUXCLK1[A,B]	A43	GND	B43	MD_L(56)	C43	GND	D43	MD_L(57)	E43
GND	A44	GND	B44	GND	C44	MD_L(55)	D44	GND	E44
MD_L(54)	A45	GND	B45	Reserved	C45	GND	D45	Reserved	E45
GND	A46	Reserved	B46	GND	C46	Reserved	D46	+1.5V	E46
MD_L(53)	A47	GND	B47	MD_L(52)	C47	GND	D47	MD_L(51)	E47
GND	A48	MD_L(50)	B48	GND	C48	MD_L(49)	D48	GND	E48
MD_L(48)	A49	GND	B49	DSTBP_L(2)	C49	GND	D49	MD_L(47)	E49
GND	A50	MD_L(46)	B50	GND	C50	MD_L(45)	D50	+1.5V	E50
MD_L(44)	A51	GND	B51	DSTBN_L(2)	C51	GND	D51	MD_L(43)	E51
GND	A52	MD_L(42)	B52	GND	C52	MD_L(41)	D52	GND	E52
MD_L(40)	A53	GND	B53	MD_L(39)	C53	GND	D53	MD_L(38)	E53
GND	A54	MD_L(37)	B54	GND	C54	MD_L(36)	D54	+1.5V	E54

5.3.2.2   I/O Connector Pinout

The CPU baseboard connects to the midplane to interface with the I/O baseboard through the I/O connector, the 240-pin signal module of the grand connector. A 1:1 signal/ground ratio for all high-speed signals is maintained while lower speed signals use a 2:1 signal/ground ratio. Table 5-28 gives the pinout for this connector. Each pin is rated at 1 A.

Table 5-28: CPU Baseboard I/O Connector Pinout

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
X1CLK	A1	5V_RET_ SENSE	B1	GND	C1	X1HSTBN_L	D1	GND	E1
GND	A2	GND	B2	5V_SENSE	C2	X1HSTBP_L	D2	GND	E2
X1D_L(15)	A3	X1D_L(13)	B3	GND	C3	GND	D3	GND	E3
X1D_L(14)	A4	GND	B4	X1XSTBN_L	C4	X1XSTBP_L	D4	GND	E4
X1D_L(12)	A5	X1D_L(10)	B5	X1BE_L(1)	C5	GND	D5	GND	E5
GND	A6	GND	B6	X1D_L(11)	C6	I2C_BACKUP_SDA	D6	MIOC_INTREQ_L	E6

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
X1D_L(9)	A7	X1D_L(7)	B7	X1ADS_L	C7	GND	D7	GND	E7
X1D_L(8)	A8	GND	B8	GND	C8	I2C_BACKUP_SCL	D8	X1RST_L	E8
X1D_L(6)	A9	X1D_L(5)	B9	X1PAR_L	C9	GND	D9	GND	E9
GND	A10	GND	B10	GND	C10	I2C_CEL_ CONNECT_ BMC_A	D10	X1BLK_L	E10
X1D_L(4)	A11	X1D_L(2)	B11	X1BE_L(0)	C11	GND	D11	GND	E11
X1D_L(3)	A12	GND	B12	GND	C12	PWR_CNTRL_RTC_L	D12	I2C_CEL_ CONNECT_FPC	E12
X1D_L(1)	A13	X1XRTS_L	B13	X1HRTS_L	C13	GND	D13	GND	E13
X1D_L(0)	A14	GND	B14	GND	C14	FP_NMI_SWT_L	D14	PWR_CNTRL_ SFC_L	E14
GND	A15	I2C_DS2P_SDA	B15	I2C_DS2P_ SCL	C15	PS_PWR_ON	D15	GND	E15
I2C_FPC_SDA	A16	GND	B16	X1B_L	C16	X1B_L	D16	PWR_GOOD	E16
I2C_FPC_SCL	A17	VCC_ STDBY	B17	HARD_ RESET	C17	DSEL1_L	D17	GND	E17
VCC_ STDBY	A18	GND	B18	GND	C18	FP_TO_PIIX_PWR BTN	D18	SECURE_MODE_ BMC	E18
ISP_SDI	A19	FAN_ FAILED_L	B19	SPEAKER_ DATA	C19	GND	D19	GND	E19
Reserved	A20	GND	B20	DTR_TTL_FP	C20	DVALIDB_L	D20	CPU_SLP_L	E20
ISP_SDO	A21	RTS_TTL_FP	B21	GND	C21	-12V	D21	GND	E21
RI_TTL_ FP	A22	GND	B22	ISP_FPC_ SDO	C22	ISP_FPC_EN_L	D22	-12V	E22
CTS_TTL_FP	A23	DOFF1_L	B23	GND	C23	ISP_SCLK	D23	GND	E23
GND	A24	DVALIDA_L	B24	DSR_TTL_ FP	C24	ISP_MODE	D24	ISP_EN_L	E24
X0CLK	A25	GND	B25	GND	C25	X0HSTBN_L	D25	DCMPLTB_L	E25
GND	A26	GND	B26	DOFF0_L	C26	X0HSTBP_L	D26	GND	E26
X0D_L(15)	A27	X0D_L(13)	B27	GND	C27	GND	D27	WDEVT_L	E27
X0D_L(14)	A28	GND	B28	X0XSTBN_L	C28	X0XSTBP_L	D28	GND	E28
X0D_L(12)	A29	X0D_L(10)	B29	X0BE_L(1)	C29	GND	D29	DCD_TTL_FP	E29
GND	A30	GND	B30	X0D_L(11)	C30	SOUT_TTL_ COM2	D30	SOUT_TTL_XIMB	E30
X0D_L(9)	A31	X0D_L(7)	B31	X0ADS_L	C31	GND	D31	GND	E31
X0D_L(8)	A32	GND	B32	GND	C32	SIN_TTL_ XIMB	D32	X0RST_L	E32
X0D_L(6)	A33	X0D_L(5)	B33	X0PAR_L	C33	GND	D33	GND	E33
GND	A34	GND	B34	GND	C34	DCMPLTA_L	D34	X0BLK_L	E34
X0D_L(4)	A35	X0D_L(2)	B35	X0BE_L(0)	C35	GND	D35	GND	E35
X0D_L(3)	A36	GND	B36	GND	C36	DSEL0_L	D36	FERR_L	E36
X0D_L(1)	A37	X0XRTS_L	B37	X0HRTS_L	C37	GND	D37	GND	E37
X0D_L(0)	A38	GND	B38	Reserved	C38	Reserved	D38	INTR_3V	E38
GND	A39	IGNNE_3V_L	B39	Reserved	C39	IO_PWRGD	D39	GND	E39
NMI_5V	A40	GND	B40	SMI_3V_L	C40	X0IB_L	D40	CIB_INT(0)	E40
I2C_BMC_SDA	A41	BMC_SPI_BUS(3)	B41	BMC_SPI_BUS(5)	C41	GND	D41	GND	E41
I2C_BMC_SCL	A42	GND	B42	GND	C42	BMC_SPI_ BUS(2)	D42	BMC_SPI_BUS(4)	E42
BMC_SPI_BUS(0)	A43	CPU_CPI_RESET_L	B43	PROC_ RESET_L	C43	GND	D43	GND	E43
BMC_SPI_BUS(6)	A44	GND	B44	A20M_3V_L	C44	INIT_3V_L	D44	Reserved	E44
BMC_SPI_BUS(1)	A45	Reserved	B45	PWRGDB	C45	PICD(0)	D45	GND	E45
IO_TDO	A46	GND	B46	IO_TMS	C46	IO_TRST_L	D46	PICD(1)	E46
IO_TCK	A47	XIMB_ SOUT_EN	B47	SIN_TTL_ COM2	C47	STPCLK_L	D47	GND	E47
COM2_TO_FP_ EN	A48	GND	B48	GND	C48	COM2_TO_ SIO_EN_A	D48	PIC_CLK	E48

5.3.2.3 Power Connector Pinout

The CPU baseboard draws power from the midplane through the power connectors, the two 90-pin power modules of the grand connector. Table 5-29 gives the pinout for these connectors. Each pin is rated at 1 A.

Table 5-29: CPU Baseboard Power Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
J24D									
P1A1	GND	P1B1	GND	P1C1	+12V	P1D1	+5V	P1E1	+5V
P1A2	GND	P1B2	GND	P1C2	+12V	P1D2	+5V	P1E2	+5V
P1A3	GND	P1B3	GND	P1C3	+12V	P1D3	+5V	P1E3	+5V

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
P2A1	GND	P2B1	GND	P2C1	+12V	P2D1	+5V	P2E1	+5V
P2A2	GND	P2B2	GND	P2C2	+12V	P2D2	+5V	P2E2	+5V
P2A3	GND	P2B3	GND	P2C3	+12V	P2D3	+5V	P2E3	+5V
J24C									
P1A1	GND	P1B1	GND	P1C1	+12V	P1D1	+5V	P1E1	+5V
P1A2	GND	P1B2	GND	P1C2	+12V	P1D2	+5V	P1E2	+5V
P1A3	GND	P1B3	GND	P1C3	+12V	P1D3	+5V	P1E3	+5V
P2A1	GND	P2B1	GND	P2C1	+12V	P2D1	+5V	P2E1	+5V
P2A2	GND	P2B2	GND	P2C2	+12V	P2D2	+5V	P2E2	+5V
P2A3	GND	P2B3	GND	P2C3	+12V	P2D3	+5V	P2E3	+5V
J24B									
P1A1	GND	P1B1	GND	P1C1	+12V	P1D1	+5V	P1E1	+3.3V
P1A2	GND	P1B2	GND	P1C2	+12V	P1D2	+5V	P1E2	+3.3V
P1A3	GND	P1B3	GND	P1C3	+12V	P1D3	+5V	P1E3	+3.3V
P2A1	GND	P2B1	GND	P2C1	+12V	P2D1	+5V	P2E1	+3.3V
P2A2	GND	P2B2	GND	P2C2	+12V	P2D2	+5V	P2E2	+3.3V
P2A3	GND	P2B3	GND	P2C3	+12V	P2D3	+5V	P2E3	+3.3V
J21D									
P1A1	GND	P1B1	GND	P1C1	+12V	P1D1	+5V	P1E1	+3.3V
P1A2	GND	P1B2	GND	P1C2	+12V	P1D2	+5V	P1E2	+3.3V
P1A3	GND	P1B3	GND	P1C3	+12V	P1D3	+5V	P1E3	+3.3V
P2A1	GND	P2B1	GND	P2C1	+12V	P2D1	+5V	P2E1	+3.3V
P2A2	GND	P2B2	GND	P2C2	+12V	P2D2	+5V	P2E2	+3.3V
P2A3	GND	P2B3	GND	P2C3	+12V	P2D3	+5V	P2E3	+3.3V
J21C									
P1A1	GND	P1B1	GND	P1C1	+12V	P1D1	+5V	P1E1	+3.3V
P1A2	GND	P1B2	GND	P1C2	+12V	P1D2	+5V	P1E2	+3.3V
P1A3	GND	P1B3	GND	P1C3	+12V	P1D3	+5V	P1E3	+3.3V
P2A1	GND	P2B1	GND	P2C1	+12V	P2D1	+5V	P2E1	+3.3V
P2A2	GND	P2B2	GND	P2C2	+12V	P2D2	+5V	P2E2	+3.3V
P2A3	GND	P2B3	GND	P2C3	+12V	P2D3	+5V	P2E3	+3.3V
J21B									
P1A1	GND	P1B1	GND	P1C1	+12V	P1D1	+12V	P1E1	+3.3V
P1A2	GND	P1B2	GND	P1C2	+12V	P1D2	+12V	P1E2	+3.3V
P1A3	GND	P1B3	GND	P1C3	+12V	P1D3	+12V	P1E3	+3.3V
P2A1	GND	P2B1	GND	P2C1	+12V	P2D1	+12V	P2E1	+3.3V
P2A2	GND	P2B2	GND	P2C2	+12V	P2D2	+12V	P2E2	+3.3V
P2A3	GND	P2B3	GND	P2C3	+12V	P2D3	+12V	P2E3	+3.3V

5.3.2.4   Processor Connector Pinout

Table 5-30 lists the pinout for the Slot 2 connectors on the CPU baseboard. The processor-unique signals on the Ak450NX board set are indicated with a † next to them. The connector pin numbers and signal names as described in the *Slot 2 Connector Specification* are also listed in Table 5-30 for reference. For more details, refer to the *Pentium® II Xeon™ Processor Datasheet*.

Table 5-30: Slot 2 Connector Pinout

Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name		Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name	
A1	1	Reserved	Reserved	RESERVED_ A1		A165	329	POW_ENABLE	Power Enable	POWOUT2#	†
A2	3	VCC_TAP	2.5V Supply	VCC_TAP		A165	329	POW_ENABLE	Power Enable	POWOUT3#	†
A3	5	Reserved	Reserved	RESERVED_ A3		A165	329	POW_ENABLE	Power Enable	POWOUT4#	†
A4	7	GND	Vss	GND		B1	2	POW_ENABLE	Power Enable	POW_ENABLE	
A5	9	Vcc_1.5	AGTL+ Vtt Supply	Vtt		B2	4	VCC_CORE	CPU Core Vcc	VCC_CORE	
A6	11	Vcc_1.5	AGTL+ Vtt Supply	Vtt		B3	6	Reserved	Reserved	RESERVED_B3	

Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name		Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name	
A7	13	SELFSB1	Frequency select 1	Frequency select 1		B4	8	XOR0	CMOS Test Input	TEST_25_B4	
A8	15	GND	Vss	GND		B5	10	VCC_CORE	CPU Core Vcc	VCC_CORE	
A9	17	SELFSB0	Frequency select 0	Frequency select 1		B6	12	Vcc_1.5	AGTL+ Vtt Supply	Vtt	
A10	19	GND	Vss	GND		B7	14	Vcc_1.5	AGTL+ Vtt Supply	Vtt	
A11	21	YYBYPASS	CMOS L2 Test Input	TEST_25_A11		B8	16	VCC_CORE	CPU Core Vcc	VCC_CORE	
A12	23	XXIERR#	CMOS Output	IERR1#	†	B9	18	Reserved	Reserved	RESERVED_B9	
A12	23	XXIERR#	CMOS Output	IERR2#	†	B10	20	XXFLUSH#	CMOS Input	P6_1_FLSH#	†
A12	23	XXIERR#	CMOS Output	IERR3#	†	B10	20	XXFLUSH#	CMOS Input	P6_2_FLSH#	†
A12	23	XXIERR#	CMOS Output	IERR4#	†	B10	20	XXFLUSH#	CMOS Input	P6_3_FLSH#	†
A13	25	GND	Vss	GND		B10	20	XXFLUSH#	CMOS Input	P6_4_FLSH#	†
A14	27	XXA20M#	CMOS Input	A20M#		B11	22	VCC_CORE	CPU Core Vcc	VCC_CORE	
A15	29	XXFERR#	CMOS Output	FERR1#	†	B12	24	XXSMI#	CMOS Input	SMI1#	†
A15	29	XXFERR#	CMOS Output	FERR2#	†	B12	24	XXSMI#	CMOS Input	SMI1#	†
A15	29	XXFERR#	CMOS Output	FERR3#	†	B12	24	XXSMI#	CMOS Input	SMI2#	†
A15	29	XXFERR#	CMOS Output	FERR4#	†	B12	24	XXSMI#	CMOS Input	SMI2#	†
A16	31	GND	Vss	GND		B13	26	XXINIT#	CMOS Input	P6_INIT1#	†
A17	33	XXIGNNE#	CMOS Input	IGNNE#		B13	26	XXINIT#	CMOS Input	P6_INIT1#	†
A18	35	XXTDI	JTAG Input	CPU1_TDI	†	B13	26	XXINIT#	CMOS Input	P6_INIT2#	†
A18	35	XXTDI	JTAG Input	CPU2_TDI	†	B13	26	XXINIT#	CMOS Input	P6_INIT2#	†
A18	35	XXTDI	JTAG Input	CPU3_TDI	†	B14	28	VCC_CORE	CPU Core Vcc	VCC_CORE	
A18	35	XXTDI	JTAG Input	CPU4_TDI	†	B15	30	XXSTPCLK#	CMOS Input	P6_1_STOP#	†
A19	37	GND	Vss	GND		B15	30	XXSTPCLK#	CMOS Input	P6_2_STOP#	†
A20	39	XXTDO	JTAG Output	CPU2_TDI	†	B15	30	XXSTPCLK#	CMOS Input	P6_3_STOP#	†
A20	39	XXTDO	JTAG Output	CPU3_TDI	†	B15	30	XXSTPCLK#	CMOS Input	P6_4_STOP#	†
A20	39	XXTDO	JTAG Output	CPU4_TDI	†	B16	32	XXTCK	JTAG Input	CPU1_TCK	†
A20	39	XXTDO	JTAG Output	MIOC_TDI	†	B16	32	XXTCK	JTAG Input	CPU2_TCK	†
A21	41	XXPWRGOOD	CMOS Input	PWRGOOD1	†	B16	32	XXTCK	JTAG Input	CPU3_TCK	†
A21	41	XXPWRGOOD	CMOS Input	PWRGOOD2	†	B16	32	XXTCK	JTAG Input	CPU4_TCK	†
A21	41	XXPWRGOOD	CMOS Input	PWRGOOD3	†	B17	34	VCC_CORE	CPU Core Vcc	VCC_CORE	
A21	41	XXPWRGOOD	CMOS Input	PWRGOOD4	†	B18	36	XXSLP#	CMOS Input	SLP1#	†
A22	43	GND	Vss	GND		B18	36	XXSLP#	CMOS Input	SLP2#	†
A23	45	XXBYPASS#	CMOS Test Input	BYPASS1#	†	B18	36	XXSLP#	CMOS Input	SLP3#	†
A23	45	XXBYPASS#	CMOS Test Input	BYPASS2#	†	B18	36	XXSLP#	CMOS Input	SLP4#	†
A23	45	XXBYPASS#	CMOS Test Input	BYPASS3#	†	B19	38	XXTMS	JTAG Input	CPU1_TMS	†
A23	45	XXBYPASS#	CMOS Test Input	BYPASS4#	†	B19	38	XXTMS	JTAG Input	CPU2_TMS	†
A24	47	XXTHERMTRIP#	CMOS Output	THERMTRIP1#	†	B19	38	XXTMS	JTAG Input	CPU3_TMS	†
A24	47	XXTHERMTRIP#	CMOS Output	THERMTRIP2#	†	B19	38	XXTMS	JTAG Input	CPU4_TMS	†
A24	47	XXTHERMTRIP#	CMOS Output	THERMTRIP3#	†	B20	40	VCC_CORE	CPU Core Vcc	VCC_CORE	
A24	47	XXTHERMTRIP#	CMOS Output	THERMTRIP4#	†	B21	42	XXTRST#	JTAG Input	CPU1_TRST#	†
A25	49	GND	Vss	GND		B21	42	XXTRST#	JTAG Input	CPU2_TRST#	†
A26	51	Reserved	Reserved	RESERVED_A26		B21	42	XXTRST#	JTAG Input	CPU3_TRST#	†
A27	53	XXLINT[0]	CMOS Input	LINT[0]		B21	42	XXTRST#	JTAG Input	CPU4_TRST#	†
A28	55	GND	Vss	GND		B22	44	Reserved	Reserved	RESERVED_B22	
A29	57	XXPICD[0]	CMOS Input	PICD[0]		B23	46	VCC_CORE	CPU Core Vcc	VCC_CORE	
A30	59	XXPREQ#	CMOS Input	CPU1_PREQ#	†	B24	48	XXTHRMDA	Thermal Diode	RESERVED_B24	
A30	59	XXPREQ#	CMOS Input	CPU2_PREQ#	†	B25	50	XXTHRMDC	Thermal Diode	RESERVED_B25	
A30	59	XXPREQ#	CMOS Input	CPU3_PREQ#	†	B26	52	VCC_CORE	CPU Core Vcc	VCC_CORE	
A30	59	XXPREQ#	CMOS Input	CPU4_PREQ#	†	B27	54	XXSQHITI#	Debug CMOS Output	SQHITI1#	†
A31	61	GND	Vss	GND		B27	54	XXSQHITI#	Debug CMOS Output	SQHITI2#	†
A32	63	XXBP#[3]	AGTL+ I/O	BP1#[3]	†	B27	54	XXSQHITI#	Debug CMOS Output	SQHITI3#	†
A32	63	XXBP#[3]	AGTL+ I/O	BP2#[3]	†	B27	54	XXSQHITI#	Debug CMOS Output	SQHITI4#	†
A32	63	XXBP#[3]	AGTL+ I/O	BP3#[3]	†	B28	56	XXLINT[1]	CMOS Input	LINT[1]	
A32	63	XXBP#[3]	AGTL+ I/O	BP4#[3]	†	B29	58	VCC_CORE	CPU Core Vcc	VCC_CORE	
A33	65	XXBPM#[0]	AGTL+ I/O	BPM1#[0]	†	B30	60	XXPICCLK	APIC Clock Input	PICCLK1	†
A33	65	XXBPM#[0]	AGTL+ I/O	BPM2#[0]	†	B30	60	XXPICCLK	APIC Clock Input	PICCLK2	†
A33	65	XXBPM#[0]	AGTL+ I/O	BPM3#[0]	†	B30	60	XXPICCLK	APIC Clock Input	PICCLK3	†

Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name		Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name	
A33	65	XXBPM#[0]	AGTL+ I/O	BPM4#[0]	†	B30	60	XXPICCLK	APIC Clock Input	PICCLK4	†
A34	67	GND	Vss	GND		B31	62	XXPICD[1]	CMOS Input	PICD[1]	
A35	69	XXBINIT#	AGTL+ I/O	BINIT#		B32	64	VCC_CORE	CPU Core Vcc	VCC_CORE	
A36	71	XXDEP#[0]	AGTL+ Data	DEP#[0]		B33	66	XXBP#[2]	AGTL+ I/O	BP1#[2]	†
A37	73	GND	Vss	GND		B33	66	XXBP#[2]	AGTL+ I/O	BP2#[2]	†
A38	75	XXDEP#[1]	AGTL+ Data	DEP#[1]		B33	66	XXBP#[2]	AGTL+ I/O	BP3#[2]	†
A39	77	XXDEP#[3]	AGTL+ Data	DEP#[3]		B33	66	XXBP#[2]	AGTL+ I/O	BP4#[2]	†
A40	79	GND	Vss	GND		B34	68	XXUCSIG#	AGTL+ Input	RESERVED_B34	
A41	81	XXDEP#[5]	AGTL+ Data	DEP#[5]		B35	70	VCC_CORE	CPU Core Vcc	VCC_CORE	
A42	83	XXDEP#[6]	AGTL+ Data	DEP#[6]		B36	72	XXPRDY#	AGTL+ Output	CPU1_PRDY#	†
A43	85	GND	Vss	GND		B36	72	XXPRDY#	AGTL+ Output	CPU2_PRDY#	†
A44	87	XXD#[61]	AGTL+ Data	D#[61]		B36	72	XXPRDY#	AGTL+ Output	CPU3_PRDY#	†
A45	89	XXD#[55]	AGTL+ Data	D#[55]		B36	72	XXPRDY#	AGTL+ Output	CPU4_PRDY#	†
A46	91	GND	Vss	GND		B37	74	XXBPM#[1]	AGTL+ I/O	BPM1#[1]	†
A47	93	XXD#[60]	AGTL+ Data	D#[60]		B37	74	XXBPM#[1]	AGTL+ I/O	BPM2#[1]	†
A48	95	XXD#[53]	AGTL+ Data	D#[53]		B37	74	XXBPM#[1]	AGTL+ I/O	BPM3#[1]	†
A49	97	GND	Vss	GND		B37	74	XXBPM#[1]	AGTL+ I/O	BPM4#[1]	†
A50	99	XXD#[57]	AGTL+ Data	D#[57]		B38	76	VCC_CORE	CPU Core Vcc	VCC_CORE	
A51	101	XXD#[46]	AGTL+ Data	D#[46]		B39	78	XXDEP#[2]	AGTL+ Data	DEP#[2]	
A52	103	GND	Vss	GND		B40	80	XXDEP#[4]	AGTL+ Data	DEP#[4]	
A53	105	XXD#[49]	AGTL+ Data	D#[49]		B41	82	VCC_CORE	CPU Core Vcc	VCC_CORE	
A54	107	XXD#[51]	AGTL+ Data	D#[51]		B42	84	XXDEP#[7]	AGTL+ Data	DEP#[7]	
A55	109	GND	Vss	GND		B43	86	XXD#[62]	AGTL+ Data	D#[62]	
A56	111	CPU_SENSE	Voltage Sense	CPU1_DS2P_SENSE	†	B44	88	VCC_CORE	CPU Core Vcc	VCC_CORE	
A56	111	CPU_SENSE	Voltage Sense	CPU2_DS2P_SENSE	†	B45	90	XXD#[58]	AGTL+ Data	D#[58]	
A56	111	CPU_SENSE	Voltage Sense	CPU3_DS2P_SENSE	†	B46	92	XXD#[63]	AGTL+ Data	D#[63]	
A56	111	CPU_SENSE	Voltage Sense	CPU4_DS2P_SENSE	†	B47	94	VCC_CORE	CPU Core Vcc	VCC_CORE	
A57	113	GND	Vss	GND		B48	96	XXD#[56]	AGTL+ Data	D#[56]	
A58	115	XXD#[42]	AGTL+ Data	D#[42]		B49	98	XXD#[50]	AGTL+ Data	D#[50]	
A59	117	XXD#[45]	AGTL+ Data	D#[45]		B50	100	VCC_CORE	CPU Core Vcc	VCC_CORE	
A60	119	GND	Vss	GND		B51	102	XXD#[54]	AGTL+ Data	D#[54]	
A61	121	XXD#[39]	AGTL+ Data	D#[39]		B52	104	XXD#[59]	AGTL+ Data	D#[59]	
A62	123	XXDCHITI#	Debug CMOS Output	DCHITI1#	†	B53	106	VCC_CORE	CPU Core Vcc	VCC_CORE	
A62	123	XXDCHITI#	Debug CMOS Output	DCHITI2#	†	B54	108	XXD#[48]	AGTL+ Data	D#[48]	
A62	123	XXDCHITI#	Debug CMOS Output	DCHITI3#	†	B55	110	XXD#[52]	AGTL+ Data	D#[52]	
A62	123	XXDCHITI#	Debug CMOS Output	DCHITI4#	†	B56	112	VCC_CORE	CPU Core Vcc	VCC_CORE	
A63	125	GND	Vss	GND		B57	114	L2_SENSE	Voltage Sense	L2_A_DS2P_SENSE	†
A64	127	XXD#[43]	AGTL+ Data	D#[43]		B57	114	L2_SENSE	Voltage Sense	L2_A_DS2P_SENSE	†
A65	129	XXD#[37]	Reserved	D#[37]		B57	114	L2_SENSE	Voltage Sense	L2_B_DS2P_SENSE	†
A66	131	GND	Vss	GND		B57	114	L2_SENSE	Voltage Sense	L2_B_DS2P_SENSE	†
A67	133	XXD#[33]	AGTL+ Data	D#[33]		B58	116	VCC_CORE	CPU Core Vcc	VCC_CORE	
A68	135	XXD#[35]	AGTL+ Data	D#[35]		B59	118	XXD#[41]	AGTL+ Data	D#[41]	
A69	137	GND	Vss	GND		B60	120	XXD#[47]	AGTL+ Data	D#[47]	
A70	139	XXD#[31]	AGTL+ Data	D#[31]		B61	122	VCC_CORE	CPU Core Vcc	VCC_CORE	
A71	141	XXD#[30]	AGTL+ Data	D#[30]		B62	124	XXD#[44]	AGTL+ Data	D#[44]	
A72	143	GND	Vss	GND		B63	126	XXD#[36]	AGTL+ Data	D#[36]	
A73	145	XXD#[27]	AGTL+ Data	D#[27]		B64	128	VCC_CORE	CPU Core Vcc	VCC_CORE	
A74	147	XXD#[24]	AGTL+ Data	D#[24]		B65	130	XXD#[40]	AGTL+ Data	D#[40]	
A75	149	GND	Vss	GND		B66	132	XXD#[34]	AGTL+ Data	D#[34]	
A76	151	XXD#[23]	AGTL+ Data	D#[23]		B67	134	VCC_CORE	CPU Core Vcc	VCC_CORE	
A77	153	XXD#[21]	AGTL+ Data	D#[21]		B68	136	XXD#[38]	AGTL+ Data	D#[38]	
A78	155	GND	Vss	GND		B69	138	XXD#[32]	AGTL+ Data	D#[32]	
A79	157	XXD#[16]	AGTL+ Data	D#[16]		B70	140	VCC_CORE	CPU Core Vcc	VCC_CORE	
A80	159	XXD#[13]	AGTL+ Data	D#[13]		B71	142	XXD#[28]	AGTL+ Data	D#[28]	
A81	161	GND	Vss	GND		B72	144	XXD#[29]	AGTL+ Data	D#[29]	
A82	163	XXSBK##	AGTL+ Data	TEST_VTT_A82		B73	146	VCC_CORE	CPU Core Vcc	VCC_CORE	
A83	165	Reserved	Reserved	RESERVED_A83		B74	148	XXD#[26]	AGTL+ Data	D#[26]	
A84	167	GND	Vss	GND		B75	150	XXD#[25]	AGTL+ Data	D#[25]	

Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name		Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name	
A85	169	XXD#[11]	AGTL+ Data	D#[11]		B76	152	VCC_CORE	CPU Core Vcc	VCC_CORE	
A86	171	XXD#[10]	AGTL+ Data	D#[10]		B77	154	XXD#[22]	AGTL+ Data	D#[22]	
A87	173	GND	Vss	GND		B78	156	XXD#[19]	AGTL+ Data	D#[19]	
A88	175	XXD#[14]	AGTL+ Data	D#[14]		B79	158	VCC_CORE	CPU Core Vcc	VCC_CORE	
A89	177	XXD#[9]	AGTL+ Data	D#[9]		B80	160	XXD#[18]	AGTL+ Data	D#[18]	
A90	179	GND	Vss	GND		B81	162	XXD#[20]	AGTL+ Data	D#[20]	
A91	181	XXD#[8]	AGTL+ Data	D#[8]		B82	164	VCC_CORE	CPU Core Vcc	VCC_CORE	
A92	183	XXD#[5]	AGTL+ Data	D#[5]		B83	166	Reserved	Reserved	RESERVED_B83	
A93	185	GND	Vss	GND		B84	168	Reserved	Reserved	RESERVED_B84	
A94	187	XXD#[3]	AGTL+ Data	D#[3]		B85	170	VCC_CORE	CPU Core Vcc	VCC_CORE	
A95	189	XXD#[1]	AGTL+ Data	D#[1]		B86	172	XXD#[17]	AGTL+ Data	D#[17]	
A96	191	GND	Vss	GND		B87	174	XXD#[15]	AGTL+ Data	D#[15]	
A97	193	XXBCLK	CPU Clock	CLK1	†	B88	176	VCC_CORE	CPU Core Vcc	VCC_CORE	
A97	193	XXBCLK	CPU Clock	CLK2	†	B89	178	XXD#[12]	AGTL+ Data	D#[12]	
A97	193	XXBCLK	CPU Clock	CLK3	†	B90	180	XXD#[7]	AGTL+ Data	D#[7]	
A97	193	XXBCLK	CPU Clock	CLK4	†	B91	182	VCC_CORE	CPU Core Vcc	VCC_CORE	
A98	195	PLL_CLK	Bypass Clock	PLLCLK1	†	B92	184	XXD#[6]	AGTL+ Data	D#[6]	
A98	195	PLL_CLK	Bypass Clock	PLLCLK2	†	B93	186	XXD#[4]	AGTL+ Data	D#[4]	
A98	195	PLL_CLK	Bypass Clock	PLLCLK3	†	B94	188	VCC_CORE	CPU Core Vcc	VCC_CORE	
A98	195	PLL_CLK	Bypass Clock	PLLCLK4	†	B95	190	XXD#[2]	AGTL+ Data	D#[2]	
A99	197	GND	Vss	GND		B96	192	XXD#[0]	AGTL+ Data	D#[0]	
A100	199	XXBERR#	AGTL+ I/O	BERR#		B97	194	VCC_CORE	CPU Core Vcc	VCC_CORE	
A101	201	XXA#[33]	AGTL+ Addresses	A#[33]		B98	196	XXRESET#	AGTL+ Input	RESET#	
A102	203	GND	Vss	GND		B99	198	XXFRCERR#	AGTL+ I/O	FRCERR1#	
A103	205	XXA#[34]	AGTL+ Addresses	A#[34]		B99	198	XXFRCERR#	AGTL+ I/O	FRCERR1#	
A104	207	XXA#[30]	AGTL+ Addresses	A#[30]		B99	198	XXFRCERR#	AGTL+ I/O	FRCERR2#	
A105	209	GND	Vss	GND		B99	198	XXFRCERR#	AGTL+ I/O	FRCERR42	
A106	211	XXA#[31]	AGTL+ Addresses	A#[31]		B100	200	VCC_CORE	CPU Core Vcc	VCC_CORE	
A107	213	XXA#[27]	AGTL+ Addresses	A#[27]		B101	202	XXA#[35]	AGTL+ Addresses	A#[35]	
A108	215	GND	Vss	GND		B102	204	XXA#[32]	AGTL+ Addresses	A#[32]	
A109	217	XXA#[22]	AGTL+ Addresses	A#[22]		B103	206	VCC_CORE	CPU Core Vcc	VCC_CORE	
A110	219	XXA#[23]	AGTL+ Addresses	A#[23]		B104	208	XXA#[29]	AGTL+ Addresses	A#[29]	
A111	221	GND	Vss	GND		B105	210	XXA#[26]	AGTL+ Addresses	A#[26]	
A112	223	XXA#[19]	AGTL+ Addresses	A#[19]		B106	212	VCC_L2	L2 Vcc	VCC_L2	
A113	225	XXA#[18]	AGTL+ Addresses	A#[18]		B107	214	XXA#[24]	AGTL+ Addresses	A#[24]	
A114	227	GND	Vss	GND		B108	216	XXA#[28]	AGTL+ Addresses	A#[28]	
A115	229	XXA#[16]	AGTL+ Addresses	A#[16]		B109	218	VCC_L2	L2 Vcc	VCC_L2	
A116	231	XXA#[13]	AGTL+ Addresses	A#[13]		B110	220	XXA#[20]	AGTL+ Addresses	A#[20]	
A117	233	GND	Vss	GND		B111	222	XXA#[21]	AGTL+ Addresses	A#[21]	
A118	235	XXA#[14]	AGTL+ Addresses	A#[14]		B112	224	VCC_L2	L2 Vcc	VCC_L2	
A119	237	GND	Vss	GND		B113	226	XXA#[25]	AGTL+ Addresses	A#[25]	
A120	239	XXA#[10]	AGTL+ Addresses	A#[10]		B114	228	XXA#[15]	AGTL+ Addresses	A#[15]	
A121	241	XXA#[5]	AGTL+ Addresses	A#[5]		B115	230	VCC_L2	L2 Vcc	VCC_L2	
A122	243	GND	Vss	GND		B116	232	XXA#[17]	AGTL+ Addresses	A#[17]	
A123	245	XXA#[9]	AGTL+ Addresses	A#[9]		B117	234	XXA#[11]	AGTL+ Addresses	A#[11]	
A124	247	XXA#[4]	AGTL+ Addresses	A#[4]		B118	236	VCC_L2	L2 Vcc	VCC_L2	
A125	249	GND	Vss	GND		B119	238	XXA#[12]	AGTL+ Addresses	A#[12]	
A126	251	Reserved	Reserved	RESERVED_A126		B120	240	VCC_L2	L2 Vcc	VCC_L2	

Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name		Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name	
A127	253	XXBNR#	AGTL+ I/O	BNR#		B121	242	XXA#[8]	AGTL+ Addresses	A#[8]	
A128	255	GND	Vss	GND		B122	244	XXA#[7]	AGTL+ Addresses	A#[7]	
A129	257	XXBPRI#	AGTL+ Input	BPRI#		B123	246	VCC_L2	L2 Vcc	VCC_L2	
A130	259	XXTRDY#	AGTL+ Input	TRDY#		B124	248	XXA#[3]	AGTL+ Addresses	A#[3]	
A131	261	GND	Vss	GND		B125	250	XXA#[6]	AGTL+ Addresses	A#[6]	
A132	263	XXDEFER#	AGTL+ Input	DEFER#		B126	252	VCC_L2	L2 Vcc	VCC_L2	
A133	265	XXREQ#[2]	AGTL+ I/O	REQ#[2]		B127	254	XXAERR#	AGTL+ I/O	AERR#	
A134	267	GND	Vss	GND		B128	256	XXREQ#[0]	AGTL+ I/O	REQ#[0]	
A135	269	XXREQ#[3]	AGTL+ I/O	REQ#[3]		B129	258	VCC_L2	L2 Vcc	VCC_L2	
A136	271	XXHITM#	AGTL+ I/O	HITM#		B130	260	XXREQ#[1]	AGTL+ I/O	REQ#[1]	
A137	273	GND	Vss	GND		B131	262	XXREQ#[4]	AGTL+ I/O	REQ#[4]	
A138	275	XXDBSY#	AGTL+ I/O	DBSY#		B132	264	VCC_L2	L2 Vcc	VCC_L2	
A139	277	XXRS#[1]	AGTL+ Input	RS#[1]		B133	266	XXLOCK#	AGTL+ I/O	LOCK#	
A140	279	GND	Vss	GND		B134	268	XXDRDY#	AGTL+ I/O	DRDY#	
A141	281	XXBREQ2#	AGTL+ Input	BREQ2#		B135	270	VCC_L2	L2 Vcc	VCC_L2	
A142	283	XXBREQ0#	AGTL+ Input	BREQ0#		B136	272	XXRS#[0]	AGTL+ Input	RS#[0]	
A143	285	GND	Vss	GND		B137	274	XXHIT#	AGTL+ I/O	HIT#	
A144	287	XXADS#	AGTL+ I/O	ADS#		B138	276	VCC_L2	L2 Vcc	VCC_L2	
A145	289	XXAP#[0]	AGTL+ I/O	AP#[0]		B139	278	XXRS#[2]	AGTL+ Input	RS#[2]	
A146	291	GND	Vss	GND		B140	280	XXRP#	AGTL+ I/O	RP#	
A147	293	VID[2]	CPU Voltage ID	SLOT1_VID[2]	†	B141	282	VCC_L2	L2 Vcc	VCC_L2	
A147	293	VID[2]	CPU Voltage ID	SLOT2_VID[2]	†	B142	284	XXBREQ3#	AGTL+ Input	BREQ3#	
A147	293	VID[2]	CPU Voltage ID	SLOT3_VID[2]	†	B143	286	XXBREQ1#	AGTL+ Input	BREQ1#	
A147	293	VID[2]	CPU Voltage ID	SLOT4_VID[2]	†	B144	288	VCC_L2	L2 Vcc	VCC_L2	
A148	295	VID[1]	CPU Voltage ID	SLOT1_VID[1]	†	B145	290	XXRSP#	AGTL+ Input	RSP#	
A148	295	VID[1]	CPU Voltage ID	SLOT2_VID[1]	†	B146	292	XXAP#[1]	AGTL+ I/O	AP#[1]	
A148	295	VID[1]	CPU Voltage ID	SLOT3_VID[1]	†	B147	294	VCC_L2	L2 Vcc	VCC_L2	
A148	295	VID[1]	CPU Voltage ID	SLOT4_VID[1]	†	B148	296	WP	WP	UN-DEF.	
A149	297	GND	Vss	GND		B149	298	VID[3]	CPU Voltage ID	SLOT1_VID[3]	†
A150	299	VID[4]	CPU Voltage ID	SLOT1_VID[4]	†	B149	298	VID[3]	CPU Voltage ID	SLOT2_VID[3]	†
A150	299	VID[4]	CPU Voltage ID	SLOT2_VID[4]	†	B149	298	VID[3]	CPU Voltage ID	SLOT3_VID[3]	†
A150	299	VID[4]	CPU Voltage ID	SLOT3_VID[4]	†	B149	298	VID[3]	CPU Voltage ID	SLOT4_VID[3]	†
A150	299	VID[4]	CPU Voltage ID	SLOT4_VID[4]	†	B150	300	VCC_L2	L2 Vcc	VCC_L2	
A151	301	Reserved	Reserved	RESERVED_A151		B151	302	VID[0]	CPU Voltage ID	SLOT1_VID[0]	†
A152	303	GND	Vss	GND		B151	302	VID[0]	CPU Voltage ID	SLOT2_VID[0]	†
A153	305	L2_VID[2]	L2 Voltage ID	L2_1_VID[2]	†	B151	302	VID[0]	CPU Voltage ID	SLOT3_VID[0]	†
A153	305	L2_VID[2]	L2 Voltage ID	L2_2_VID[2]	†	B151	302	VID[0]	CPU Voltage ID	SLOT4_VID[0]	†
A153	305	L2_VID[2]	L2 Voltage ID	L2_3_VID[2]	†	B152	304	L2_VID[0]	L2 Voltage ID	L2_1_VID[0]	†
A153	305	L2_VID[2]	L2 Voltage ID	L2_4_VID[2]	†	B152	304	L2_VID[0]	L2 Voltage ID	L2_2_VID[0]	†
A154	307	L2_VID[1]	L2 Voltage ID	L2_1_VID[1]	†	B152	304	L2_VID[0]	L2 Voltage ID	L2_3_VID[0]	†
A154	307	L2_VID[1]	L2 Voltage ID	L2_2_VID[1]	†	B152	304	L2_VID[0]	L2 Voltage ID	L2_4_VID[0]	†
A154	307	L2_VID[1]	L2 Voltage ID	L2_3_VID[1]	†	B153	306	VCC_L2	L2 Vcc	VCC_L2	
A154	307	L2_VID[1]	L2 Voltage ID	L2_4_VID[1]	†	B154	308	L2_VID[4]	L2 Voltage ID	L2_1_VID[4]	†
A155	309	GND	Vss	GND		B154	308	L2_VID[4]	L2 Voltage ID	L2_2_VID[4]	†
A156	311	VCC_1.5	AGTL+ Vtt Supply	VTT		B154	308	L2_VID[4]	L2 Voltage ID	L2_3_VID[4]	†
A157	313	VCC_1.5	AGTL+ Vtt Supply	VTT		B154	308	L2_VID[4]	L2 Voltage ID	L2_4_VID[4]	†
A158	315	GND	Vss	GND		B155	310	L2_VID[3]	L2 Voltage ID	L2_1_VID[3]	†
A159	317	SA2	Serial Bus Address	SA2		B155	310	L2_VID[3]	L2 Voltage ID	L2_2_VID[3]	†
A160	319	VCC_SMB	3.3V Supply	VCC_SM		B155	310	L2_VID[3]	L2 Voltage ID	L2_3_VID[3]	†
A161	321	GND	Vss	GND		B155	310	L2_VID[3]	L2 Voltage ID	L2_4_VID[3]	†
A162	323	SA1	Serial Bus Address	SA1[1]	†	B156	312	VCC_L2	L2 Vcc	VCC_L2	
A162	323	SA1	Serial Bus Address	SA2[1]	†	B157	314	VCC_1.5	AGTL+ Vtt Supply	VTT	
A162	323	SA1	Serial Bus Address	SA3[1]	†	B158	316	VCC_1.5	AGTL+ Vtt Supply	VTT	
A162	323	SA1	Serial Bus Address	SA4[1]	†	B159	318	VCC_L2	L2 Vcc	VCC_L2	
A163	325	SA0	Serial Bus Address	SA1[0]	†	B160	320	SCLK	Serial Bus Clock	SCLK	
A163	325	SA0	Serial Bus Address	SA2[0]	†	B161	322	SDAT	Serial Bus Data	SDAT	
A163	325	SA0	Serial Bus Address	SA3[0]	†	B162	324	VCC_L2	L2 Vcc	VCC_L2	

Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name		Spec. Pin#	Ak450NX Pin#	Spec. Name	Description	Ak450NX Name	
A163	325	SA0	Serial Bus Address	SA4[0]	†	B163	326	Reserved	Reserved	RESERVED_B163	
A164	327	GND	Vss	GND		B164	328	Reserved	Reserved	RESERVED_B164	
A165	329	POW_ENABLE	Power Enable	POWOUT1#	†	B165	330	Reserved	Reserved	RESERVED_B165	

† Processor-unique signals on the Ak450NX board set.

5.3.2.5 Front Panel Connector Pinout

A chassis front panel board may be added to the Ak450NX board set through the front panel connector on the CPU baseboard. This connector is a 80-pin SCA-type connector. Table 5-31 gives the pinout for this connector. Each pin is rated at 1 A.

Table 5-31: CPU Baseboard Front Panel Connector Pinout

Signal	Pin	Signal	Pin
GND	1	GND	41
+12V	2	-12V	42
+12V	3	+12V	43
GND	4	GND	44
GND	5	GND	45
+12V	6	+12V	46
+12V	7	+12V	47
SPEAKER_DATA	8	GND	48
ISP_SCLK	9	GND	49
FAN_FAILED_L	10	+5V	50
GND	11	ISP_SDI	51
ISP_FPC_EN_L	12	+5V	52
FP_TO_PIIX_PWRBTN	13	ISP_MODE	53
ISP_FPC_SDO	14	+5V	54
Reserved	15	Reserved	55
COM2_TO_FP_EN	16	+5V	56
COM2_TO_SIO_EN_A	17	PROC_RESET_L	57
GND	18	Reserved	58
SECURE_MODE_BMC	19	XIMB_SOUT_EN	59
HARD_RESET	20	GND	60
FP_NMI_SWT_L	21	Reserved	61
SIN_TTL_COM2	22	Reserved	62
SIN_TTL_XIMB	23	Reserved	63
GND	24	GND	64
SOUT_TTL_XIMB	25	PWR_CNTRL_SFC_L	65
PWR_CNTRL_RTC_L	26	SOUT_TTL_COM2	66
GND	27	GND	67
PS_PWR_ON	28	PWR_GOOD	68
DSR_TTL_FP	29	DCD_TTL_FP	69
I2C_CEL_CONNECT_FPC	30	GND	70
CTS_TTL_FP	31	Reserved	71
I2C_CEL_CONNECT_BMC_A	32	Reserved	72
I2C_FPC_SCL	33	RI_TTL_FP	73
I2C_FPC_SDA	34	Reserved	74
GND	35	RTS_TTL_FP	75
GND	36	DTR_TTL_FP	76
I2C_BACKUP_SDA	37	I2C_BACKUP_SCL	77
VCC_STDBY	38	VCC_STDBY	78
VCC_STDBY	39	VCC_STDBY	79
Reserved	40	GND	80

5.3.3   Memory Module Interface Connector

Each memory module uses a 300-pin Futurebus pin-and-socket connector for interfacing with the CPU baseboard (through the interconnect midplane). Both power and signals are routed on the pins. To achieve a 1:1 signal/ground ratio, over half of the pins on the signal module are connected to either ground or power. Table 5-32 gives the pinouts for the memory interface connector. Note that no special power modules are used; all power needed by the board is delivered on signal pins. Each signal pin is rated at 1A.

5.3.3.1   Memory Interface Connector Pinout

Table 5-32: Memory Interface Connector Pinout

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GND	A1	MD36_L	B1	GND	C1	MD37_L	D1	VCC	E1
GDCMPLT_L	A2	VCC	B2	DSTBN2_L	C2	GND	D2	MD38_L	E2
GND	A3	MD39_L	B3	GND	C3	MD40_L	D3	VCC	E3
MD41_L	A4	VCC	B4	DSTBP2_L	C4	GND	D4	MD42_L	E4
GND	A5	MD43_L	B5	GND	C5	MD44_L	D5	VCC	E5
MD45_L	A6	VCC	B6	MD46_L	C6	GND	D6	MD47_L	E6
GND	A7	MD48_L	B7	GND	C7	MD49_L	D7	VCC	E7
MD50_L	A8	VCC	B8	MD51_L	C8	GND	D8	MD52_L	E8
GND	A9	MD53_L	B9	GND	C9	TDO	D9	VCC	E9
VTT	A10	VCC	B10	MD54_L	C10	GND	D10	VCC	E10
GND	A11	GND	B11	VTT	C11	MD55_L	D11	VCC	E11
MUXCLK1	A12	GND	B12	MD56_L	C12	GND	D12	MD57_L	E12
GND	A13	GND	B13	VTT	C13	MD58_L	D13	VCC	E13
MD59_L	A14	VCC	B14	DSTBP3_L	C14	GND	D14	MD60_L	E14
GND	A15	MD61_L	B15	GND	C15	MD62_L	D15	VCC	E15
MD63_L	A16	VCC	B16	DSTBN3_L	C16	GND	D16	MD64_L	E16
GND	A17	MD65_L	B17	GND	C17	MD66_L	D17	VCC	E17
VTT	A18	VCC	B18	MD67_L	C18	GND	D18	MD68_L	E18
GND	A19	MD69_L	B19	GND	C19	MD70_L	D19	VCC	E19
MD71_L	A20	VCC	B20	VTT	C20	GND	D20	VCC	E20
GND	A21	NC	B21	GND	C21	NC	D21	VCC	E21
VTT	A22	VCC	B22	CARD_NUM	C22	GND	D22	I2C_BMC_SCL	E22
GND	A23	GND	B23	VTT	C23	PWRGD	D23	VCC	E23
SPAREKCLK1	A24	GND	B24	PHIT_L	C24	GND	D24	I2C_BMC_SDA	E24
GND	A25	GND	B25	VTT	C25	RHIT_L	D25	VCC	E25
WDEVT_L	A26	VCC	B26	RCMPLT_L	C26	GND	D26	GRCMPLT_L	E26
GND	A27	CMND0_L	B27	GND	C27	CARD_L	D27	VCC	E27
DCMPLT_L	A28	VCC	B28	BANK0_L	C28	GND	D28	BANK1_L	E28
GND	A29	BANK2_L	B29	GND	C29	CMND1_L	D29	VCC	E29
DVALID_L	A30	VCC	B30	ROW_L	C30	GND	D30	CSTB_L	E30
GND	A31	MA0_L	B31	VTT	C31	MA1_L	D31	VCC	E31
DOFF0_L	A32	GND	B32	MA2_L	C32	GND	D32	MA3_L	E32
GND	A33	MA4_L	B33	VTT	C33	MA5_L	D33	VCC	E33
DOFF1_L	A34	VCC	B34	MA6_L	C34	GND	D34	MA7_L	E34
GND	A35	MA8_L	B35	GND	C35	MA9_L	D35	VCC	E35
DSEL_L	A36	VCC	B36	MA10_L	C36	GND	D36	MA11_L	E36
GND	A37	GND	B37	GND	C37	MA12_L	D37	VCC	E37
RCGCLK	A38	GND	B38	MA13_L	C38	GND	D38	VCC	E38
GND	A39	GND	B39	VTT	C39	VCC	D39	VCC	E39
SPARECLK0	A40	GND	B40	NC	C40	GND	D40	TCK	E40
GND	A41	GND	B41	VTT	C41	VCC	D41	VCC	E41
MD0_L	A42	VCC	B42	MD1_L	C42	GND	D42	MD2_L	E42
GND	A43	MD3_L	B43	GND	C43	MD4_L	D43	VCC	E43

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
MD5_L	A44	VCC	B44	DSTBN0_L	C44	GND	D44	MD6_L	E44
GND	A45	MD7_L	B45	GND	C45	MD8_L	D45	VCC	E45
MD9_L	A46	VCC	B46	DSTBP0_L	C46	GND	D46	MD10_L	E46
GND	A47	MD11_L	B47	GND	C47	MD12_L	D47	VCC	E47
MD13_L	A48	VCC	B48	MD14_L	C48	GND	D48	MD15_L	E48
GND	A49	TDI	B49	GND	C49	TMS	D49	VCC	E49
MD16_L	A50	VCC	B50	TRST_L	C50	GND	D50	MRESET_L	E50
GND	A51	GND	B51	VTT	C51	MD17_L	D51	VCC	E51
MUXCLK0	A52	GND	B52	MD18_L	C52	GND	D52	MD19_L	E52
GND	A53	GND	B53	VTT	C53	MD20_L	D53	VCC	E53
MD21_L	A54	VCC	B54	MD22_L	C54	GND	D54	MD23_L	E54
GND	A55	MD24_L	B55	GND	C55	MD25_L	D55	VCC	E55
MD26_L	A56	VCC	B56	DSTBP1_L	C56	GND	D56	MD27_L	E56
GND	A57	MD28_L	B57	GND	C57	MD29_L	D57	VCC	E57
GDCMPLT_L	A58	VCC	B58	DSTBN1_L	C58	GND	D58	MD30_L	E58
GND	A59	MD31_L	B59	GND	C59	MD32_L	D59	VCC	E59
MD33_L	A60	VCC	B60	MD34_L	C60	GND	D60	MD35_L	E60

5.3.4   Interconnect Midplane Connectors

The interconnect midplane is mainly a passive interconnect board that serves as a cental interconnect board for the PHP I/O baseboard, CPU baseboard, and memory modules. The grand connector is the largest interface connector and is used to connect the midplane to the CPU baseboard. Two smaller connectors provide the interface of the midplane to the two memory modules. There is also a split connector across the top edge of the primary side of the midplane that allows connection to the PHP I/O baseboard.

Additional functions of the interconnect midplane are to provide power and server management distribution to the boards in the board set. This is done through 3 additional power supply interface connectors, a peripheral device power connector, and an I^2C server management bus connector. The pinouts for each of these connectors are listed in the following tables.

5.3.4.1   Grand Connector Pinout

The midplane interfaces to the CPU baseboard through one large, 960-pin Futurebus+ style connector. This connector, termed the grand connector, consists of one 240-pin signal module, two 270-pin signal modules (see *Section 2.2.2* of this document), and two 90-pin power modules. A 1:1 signal/ground ratio for all high-speed signals is maintained while lower speed signals use a 2:1 signal/ground ratio.

Table 5-33: Grand Connector - I/O Section (J3)

	A	B	C	D	E
1	COM2_TO_FP_EN	GROUND	GROUND	COM2_TO_SIO_EN	PIC_CLK
2	IO_TCK	XIMB_SOUT_EN	SIN_TTL_COM2	STPCLK_L	GROUND
3	IO_TDO	GROUND	IO_TMS	IO_TRST_L	PICD(1)
4	BMC_SPI_BUS(1)	IO_TDI	PWRGDB	PICD(0)	GROUND
5	BMC_SPI_BUS(6)	GROUND	A20M_L	INIT_L	Unused
6	BMC_SPI_BUS(0)	CPU_SPI_RESET_L	PROC_RESET_L	GROUND	GROUND
7	I2C_BMC_SCL	GROUND	GROUND	BMC_SPI_BUS(2)	BMC_SPI_BUS(4)
8	I2C_BMC_SDA	BMC_SPI_BUS(3)	BMC_SPI_BUS(5)	GROUND	GROUND
9	NMI_5V	GROUND	SMI_L	X0IB_L	CIB_INT(0)
10	GROUND	IGNNE_L	I2C_GLOBAL_SDA	IO_PWRGD	GROUND

	A	B	C	D	E
11	X0D_L(0)	GROUND	GROUND	I2C_GLOBAL_SCL	INTR
12	X0D_L(1)	X0XRTS_L	X0HRTS_L	GROUND	GROUND
13	X0D_L(3)	GROUND	GROUND	DSEL0_L	FERR_L
14	X0D_L(4)	X0D_L(2)	X0BE_L(0)	GROUND	GROUND
15	GROUND	GROUND	GROUND	DCMPLTA_L	X0BLK_L
16	X0D_L(6)	X0D_L(5)	X0PAR_L	GROUND	GROUND
17	X0D_L(8)	GROUND	GROUND	SIN_TTL_XIMB	X0RST_L
18	X0D_L(9)	X0D_L(7)	X0ADS_L	GROUND	GROUND
19	GROUND	GROUND	X0D_L(11)	SOUT_TTL_COM2	SOUT_TTL_XIMB
20	X0D_L(12)	X0D_L(10)	X0BE_L(1)	GROUND	DCD_TTL_FP
21	X0D_L(14)	GROUND	X0XSTBN_L	X0XSTBP_L	GROUND
22	X0D_L(15)	X0D_L(13)	GROUND	GROUND	WDEVT_L
23	GROUND	GROUND	DOFF0_L	X0HSTBP_L	GROUND
24	X0CLK	GROUND	GROUND	X0HSTBN_L	DCMPLTB_L
25	GROUND	DVALIDA_L	DSR_TTL_FP	ISP_MODE	ISP_EN_L
26	CTS_TTL_FP	DOFF1_L	GROUND	ISP_SCLK	GROUND
27	RI_TTL_FP	GROUND	ISP_FPC_SDO	ISP_FPC_EN_L	-12V
28	ISP_SDO	RTS_TTL_FP	GROUND	-12V	GROUND
29	INTRUSION_L	GROUND	DTR_TTL_FP	DVALIDB_L	CPU_SLP_L
30	ISP_SDI	FAN_FAILED_L	SPEAKER_DATA	GROUND	GROUND
31	VCC_STDBY	GROUND	GROUND	FP_TO_PIIX4_PWRBTN	SECURE_MODE_BMC
32	I2C_FPC_SCL	VCC_STDBY	HARD_RESET	DSEL1_L	GROUND
33	I2C_FPC_SDA	GROUND	GROUND	X1IB_L	PWR_GOOD
34	GROUND	DS2P_I2C_SDA	DS2P_I2C_SCL	PS_PWR_ON	GROUND
35	X1D_L(0)	GROUND	GROUND	FP_NMI_SWT_L	PWR_CNTRL_SFC_L
36	X1D_L(1)	X1XRTS_L	X1HRTS_L	GROUND	GROUND
37	X1D_L(3)	GROUND	GROUND	PWR_CNTRL_RTC_L	I2C_CEL_CONNECT_FPC
38	X1D_L(4)	X1D_L(2)	X1BE_L(0)	GROUND	GROUND
39	GROUND	GROUND	GROUND	I2C_CEL_CONNECT_BMC	X1BLK_L
40	X1D_L(6)	X1D_L(5)	X1PAR_L	GROUND	GROUND
41	X1D_L(8)	GROUND	GROUND	I2C_BACKUP_SCL	X1RST_L
42	X1D_L(9)	X1D_L(7)	X1ADS_L	GROUND	GROUND
43	GROUND	GROUND	X1D_L(11)	I2C_BACKUP_SDA	MIOC_INTREQ_L
44	X1D_L(12)	X1D_L(10)	X1BE_L(1)	GROUND	GROUND
45	X1D_L(14)	GROUND	X1XSTBN_L	X1XSTBP_L	GROUND
46	X1D_L(15)	X1D_L(13)	GROUND	GROUND	GROUND
47	GROUND	GROUND	5V_SENSE	X1HSTBP_L	GROUND
48	X1CLK	5V_RET_SENSE	GROUND	X1HSTBN_L	GROUND

Table 5-34: Memory Section – Primary Memory Module (J4)

	A	B	C	D	E
1	MD#(35)	GND	MD#(34)	GND	MD#(33)
2	GND	MD#(32)	GND	MD#(31)	+1.5V

	A	B	C	D	E
3	MD#(30)	GND	DSTBN1#	GND	MD#(29)
4	GND	MD#(28)	GND	MD#(27)	GND
5	MD#(26)	GND	DSTBP1#	GND	MD#(25)
6	GND	MD#(24)	GND	MD#(23)	+1.5V
7	MD#(22)	GND	MD#(21)	GND	MD#(20)
8	GND	GND	GND	MD#(19)	GND
9	MUXCLK0	GND	MD#(17)	GND	MD#(18)
10	GND	GND	GND	Was DSEL#	GND
11	MRESET#	GND	Was DOFF0_L	GND	Was DOFF1_L
12	GND	MD#(16)	GND	MD#(15)	+1.5V
13	MD#(14)	GND	MD#(13)	GND	MD#(12)
14	GND	MD#(11)	GND	MD#(10)	GND
15	MD#(9)	GND	DSTBP0#	GND	MD#(8)
16	GND	MD#(7)	GND	MD#(6)	+1.5V
17	MD#(5)	GND	DSTBN0#	GND	MD#(4)
18	GND	MD#(3)	GND	GND	GND
19	MD#(2)	GND	MD#(1)	GND	SPARECLK0
20	GND	MD#(0)	GND	GND	GND
21	TCK	GND	TDI	GND	TMS
22	GND	TRST#	GND	MA#(13)	GND
23	MA#(12)	GND	MA#(11)	GND	MA#(10)
24	GND	MA#(9)	GND	MA#(8)	+1.5V
25	MA#(7)	GND	MA#(6)	GND	MA#(5)
26	GND	MA#(4)	GND	GND	GND
27	MA#(3)	GND	MA#(2)	GND	RCGCLK
28	GND	MA#(1)	GND	GND	GND
29	MA#(0)	GND	CSTB#	GND	ROW#
30	GND	CMND1#	GND	BANK0#	+1.5V
31	BANK1#	GND	BANK2#	GND	CMND0#
32	GND	CARD#	GND	GND	GND
33	PHIT#	GND	RCMPLT#	GND	SPARECLK1
34	GND	RHIT#	GND	GND	GND
35	Unused	GND	Unused	GND	Unused
36	GND	MD#(71)	GND	MD#(70)	GND
37	MD#(69)	GND	MD#(68)	GND	MD#(67)
38	GND	MD#(66)	GND	MD#(65)	+1.5V
39	MD#(64)	GND	DSTBN3#	GND	MD#(63)
40	GND	MD#(62)	GND	MD#(61)	GND
41	MD#(60)	GND	DSTBP3#	GND	MD#(59)
42	GND	GND	GND	MD#(58)	GND
43	MUXCLK1	GND	MD#(56)	GND	MD#(57)
44	GND	GND	GND	MD#(55)	GND
45	MD#(54)	GND	Unused	GND	Was DCMPLT#

	A	B	C	D	E
46	GND	Was DVALID#	GND	Was WDEVT#	+1.5V
47	MD#(53)	GND	MD#(52)	GND	MD#(51)
48	GND	MD#(50)	GND	MD#(49)	GND
49	MD#(48)	GND	DSTBP2#	GND	MD#(47)
50	GND	MD#(46)	GND	MD#(45)	+1.5V
51	MD#(44)	GND	DSTBN2#	GND	MD#(43)
52	GND	MD#(42)	GND	MD#(41)	GND
53	MD#(40)	GND	MD#(39)	GND	MD#(38)
54	GND	MD#(37)	GND	MD#(36)	+1.5V

Table 5-35: Grand Connector – Secondary Memory Module (J1)

	A	B	C	D	E
1	MD#(35)	GND	MD#(34)	GND	MD#(33)
2	GND	MD#(32)	GND	MD#(31)	+1.5V
3	MD#(30)	GND	DSTBN1#	GND	MD#(29)
4	GND	MD#(28)	GND	MD#(27)	GND
5	MD#(26)	GND	DSTBP1#	GND	MD#(25)
6	GND	MD#(24)	GND	MD#(23)	+1.5V
7	MD#(22)	GND	MD#(21)	GND	MD#(20)
8	GND	GND	GND	MD#(19)	GND
9	MUXCLK0	GND	MD#(17)	GND	MD#(18)
10	GND	GND	GND	Was DSEL#	GND
11	MRESET#	GND	Was DOFF0_L	GND	Was DOFF1_L
12	GND	MD#(16)	GND	MD#(15)	+1.5V
13	MD#(14)	GND	MD#(13)	GND	MD#(12)
14	GND	MD#(11)	GND	MD#(10)	GND
15	MD#(9)	GND	DSTBP0#	GND	MD#(8)
16	GND	MD#(7)	GND	MD#(6)	+1.5V
17	MD#(5)	GND	DSTBN0#	GND	MD#(4)
18	GND	MD#(3)	GND	GND	GND
19	MD#(2)	GND	MD#(1)	GND	SPARECLK0
20	GND	MD#(0)	GND	GND	GND
21	TCK	GND	TDI	GND	TMS
22	GND	TRST#	GND	MA#(13)	GND
23	MA#(12)	GND	MA#(11)	GND	MA#(10)
24	GND	MA#(9)	GND	MA#(8)	+1.5V
25	MA#(7)	GND	MA#(6)	GND	MA#(5)
26	GND	MA#(4)	GND	GND	GND
27	MA#(3)	GND	MA#(2)	GND	RCGCLK
28	GND	MA#(1)	GND	GND	GND
29	MA#(0)	GND	CSTB#	GND	ROW#
30	GND	CMND1#	GND	BANK0#	+1.5V

	A	B	C	D	E
31	BANK1#	GND	BANK2#	GND	CMND0#
32	GND	CARD#	GND	GND	GND
33	PHIT#	GND	RCMPLT#	GND	SPARECLK1
34	GND	RHIT#	GND	GND	GND
35	Unused	GND	Unused	GND	Unused
36	GND	MD#(71)	GND	MD#(70)	GND
37	MD#(69)	GND	MD#(68)	GND	MD#(67)
38	GND	MD#(66)	GND	MD#(65)	+1.5V
39	MD#(64)	GND	DSTBN3#	GND	MD#(63)
40	GND	MD#(62)	GND	MD#(61)	GND
41	MD#(60)	GND	DSTBP3#	GND	MD#(59)
42	GND	GND	GND	MD#(58)	GND
43	MUXCLK1	GND	MD#(56)	GND	MD#(57)
44	GND	GND	GND	MD#(55)	GND
45	MD#(54)	GND	Unused	GND	Was DCMPLT#
46	GND	Was DVALID#	GND	Was WDEVT#	+1.5V
47	MD#(53)	GND	MD#(52)	GND	MD#(51)
48	GND	MD#(50)	GND	MD#(49)	GND
49	MD#(48)	GND	DSTBP2#	GND	MD#(47)
50	GND	MD#(46)	GND	MD#(45)	+1.5V
51	MD#(44)	GND	DSTBN2#	GND	MD#(43)
52	GND	MD#(42)	GND	MD#(41)	GND
53	MD#(40)	GND	MD#(39)	GND	MD#(38)
54	GND	MD#(37)	GND	MD#(36)	+1.5V

Table 5-36: Grand Connector - Powe   r Module 1 (J2)

	A	B	C	D	E
P1X1	GND	GND	12V	12V	3.3V
P1X2	GND	GND	12V	12V	3.3V
P1X3	GND	GND	12V	12V	3.3V
P2X1	GND	GND	12V	12V	3.3V
P2X2	GND	GND	12V	12V	3.3V
P2X3	GND	GND	12V	12V	3.3V
P1X1	GND	GND	12V	5V	3.3V
P1X2	GND	GND	12V	5V	3.3V
P1X3	GND	GND	12V	5V	3.3V
P2X1	GND	GND	12V	5V	3.3V
P2X2	GND	GND	12V	5V	3.3V
P2X3	GND	GND	12V	5V	3.3V
P1X1	GND	GND	12V	5V	3.3V

	A	B	C	D	E
P1X2	GND	GND	12V	5V	3.3V
P1X3	GND	GND	12V	5V	3.3V
P2X1	GND	GND	12V	5V	3.3V
P2X2	GND	GND	12V	5V	3.3V
P2X3	GND	GND	12V	5V	3.3V

Table 5-37: Grand Connector Power Module 2 (J5):

	A	B	C	D	E
P1X1	GND	GND	12V	5V	3.3V
P1X2	GND	GND	12V	5V	3.3V
P1X3	GND	GND	12V	5V	3.3V
P2X1	GND	GND	12V	5V	3.3V
P2X2	GND	GND	12V	5V	3.3V
P2X3	GND	GND	12V	5V	3.3V
P1X1	GND	GND	12V	5V	5V
P1X2	GND	GND	12V	5V	5V
P1X3	GND	GND	12V	5V	5V
P2X1	GND	GND	12V	5V	5V
P2X2	GND	GND	12V	5V	5V
P2X3	GND	GND	12V	5V	5V
P1X1	GND	GND	12V	5V	5V
P1X2	GND	GND	12V	5V	5V
P1X3	GND	GND	12V	5V	5V
P2X1	GND	GND	12V	5V	5V
P2X2	GND	GND	12V	5V	5V
P2X3	GND	GND	12V	5V	5V

5.3.4.2   Memory Module Connector Pinout (J6, J7)

The midplane interfaces to the two memory modules through two separate 300 pin connectors. Both power and signals are routed on the pins on the pins of this connector. To achieve a 1:1 signal/ground ratio, over half of the pins on the signal module are connected to either ground or power. Note that no special power modules are used. All power needed by the board is delivered on signal pins. Each signal pin is rated at 1 A.

Table 5-38: Primary Memory Module Interface Connector (J7)

	A	B	C	D	E
1	GND	MD#(36)	GND	MD#(37)	+3.3V
2	GDCMPLT#	+3.3V	DSTBN2#	GND	MD#(38)
3	GND	MD#(39)	GND	MD#(40)	+3.3V
4	MD#(41)	+3.3V	DSTBP2#	GND	MD#(42)

	A	B	C	D	E
5	GND	MD#(43)	GND	MD#(44)	+3.3V
6	MD#(45)	+3.3V	MD#(46)	GND	MD#(47)
7	GND	MD#(48)	GND	MD#(49)	+3.3V
8	MD#(50)	+3.3V	MD#(51)	GND	MD#(52)
9	GND	MD#(53)	GND	WDEVT#	+3.3V
10	DCMPLT#	+3.3V	MD#(54)	GND	DVALID#
11	GND	GND	+1.5V	MD#(55)	+3.3V
12	MUXCLK1	GND	MD#(56)	GND	MD#(57)
13	GND	GND	+1.5V	MD#(58)	+3.3V
14	MD#(59)	+3.3V	DSTBP3#	GND	MD#(60)
15	GND	MD#(61)	GND	MD#(62)	+3.3V
16	MD#(63)	+3.3V	DSTBN3#	GND	MD#(64)
17	GND	MD#(65)	GND	MD#(66)	+3.3V
18	+1.5V	+3.3V	MD#(67)	GND	MD#(68)
19	GND	MD#(69)	GND	MD#(70)	+3.3V
20	MD#(71)	+3.3V	+3.3V	GND	+3.3V
21	GND		GND		+3.3V
22	+3.3V	+3.3V	CARD_NUM	GND	I2C_BMC_SCL
23	GND	GND	+1.5V	PWRGD	+3.3V
24	SPARECLK1	GND	PHIT#	GND	I2C_BMC_SDA
25	GND	GND	+1.5V	RHIT#	+3.3V
26	+1.5V	+3.3V	RCMPLT#	GND	+3.3V
27	GND	CARD#	GND	GRCMPLT#	+3.3V
28	CMND0#	+3.3V	BANK0#	GND	BANK1#
29	GND	BANK2#	GND	CMND1#	+3.3V
30	+1.5V	+3.3V	ROW#	GND	CSTB#
31	GND	GND	+1.5V	MA#(0)	+3.3V
32	RCGCLK	GND	MA#(1)	GND	MA#(2)
33	GND	GND	+1.5V	MA#(3)	+3.3V
34	MA#(4)	+3.3V	MA#(5)	GND	MA#(6)
35	GND	MA#(7)	GND	MA#(8)	+3.3V
36	MA#(9)	+3.3V	MA#(10)	GND	MA#(11)
37	GND	MA#(12)	GND	MA#(13)	+3.3V
38	+1.5V	+3.3V	TMS	GND	+3.3V
39	GND	GND	+1.5V	TRST#	+3.3V
40	SPARECLK0	GND	TDI	GND	TDO
41	GND	GND	+1.5V	TCK	+3.3V
42	MD#(0)	+3.3V	MD#(1)	GND	MD#(2)
43	GND	MD#(3)	GND	MD#(4)	+3.3V
44	MD#(5)	+3.3V	DSTBN0#	GND	MD#(6)
45	GND	MD#(7)	GND	MD#(8)	+3.3V
46	MD#(9)	+3.3V	DSTBP0#	GND	MD#(10)
47	GND	MD#(11)	GND	MD#(12)	+3.3V
48	MD#(13)	+3.3V	MD#(14)	GND	MD#(15)
49	GND	DOFF1#	GND	DOFF0#	+3.3V

	A	B	C	D	E
50	MD#(16)	+3.3V	DSEL#	GND	MRESET#
51	GND	GND	+1.5V	MD#(17)	+3.3V
52	MUXCLK0	GND	MD#(18)	GND	MD#(19)
53	GND	GND	+1.5V	MD#(20)	+3.3V
54	MD#(21)	+3.3V	MD#(22)	GND	MD#(23)
55	GND	MD#(24)	GND	MD#(25)	+3.3V
56	MD#(26)	+3.3V	DSTBP1#	GND	MD#(27)
57	GND	MD#(28)	GND	MD#(29)	+3.3V
58	GDCMPLT#	+3.3V	DSTBN1#	GND	MD#(30)
59	GND	MD#(31)	GND	MD#(32)	+3.3V
60	MD#(33)	+3.3V	MD#(34)	GND	MD#(35)

Table 5-39: Secondary Memory Module Interface Connector (J6)

	A	B	C	D	E
1	GND	MD#(36)	GND	MD#(37)	+3.3V
2	GDCMPLT#	+3.3V	DSTBN2#	GND	MD#(38)
3	GND	MD#(39)	GND	MD#(40)	+3.3V
4	MD#(41)	+3.3V	DSTBP2#	GND	MD#(42)
5	GND	MD#(43)	GND	MD#(44)	+3.3V
6	MD#(45)	+3.3V	MD#(46)	GND	MD#(47)
7	GND	MD#(48)	GND	MD#(49)	+3.3V
8	MD#(50)	+3.3V	MD#(51)	GND	MD#(52)
9	GND	MD#(53)	GND	WDEVT#	+3.3V
10	DCMPLT#	+3.3V	MD#(54)	GND	DVALID#
11	GND	GND	+1.5V	MD#(55)	+3.3V
12	MUXCLK1	GND	MD#(56)	GND	MD#(57)
13	GND	GND	+1.5V	MD#(58)	+3.3V
14	MD#(59)	+3.3V	DSTBP3#	GND	MD#(60)
15	GND	MD#(61)	GND	MD#(62)	+3.3V
16	MD#(63)	+3.3V	DSTBN3#	GND	MD#(64)
17	GND	MD#(65)	GND	MD#(66)	+3.3V
18	+1.5V	+3.3V	MD#(67)	GND	MD#(68)
19	GND	MD#(69)	GND	MD#(70)	+3.3V
20	MD#(71)	+3.3V	+3.3V	GND	+3.3V
21	GND		GND		+3.3V
22	+3.3V	+3.3V	CARD_NUM	GND	I2C_BMC_SCL
23	GND	GND	+1.5V	PWRGD	+3.3V
24	SPARECLK1	GND	PHIT#	GND	I2C_BMC_SDA
25	GND	GND	+1.5V	RHIT#	+3.3V
26	+1.5V	+3.3V	RCMPLT#	GND	+3.3V
27	GND	CARD#	GND	GRCMPLT#	+3.3V
28	CMND0#	+3.3V	BANK0#	GND	BANK1#
29	GND	BANK2#	GND	CMND1#	+3.3V
30	+1.5V	+3.3V	ROW#	GND	CSTB#

	A	B	C	D	E
31	GND	GND	+1.5V	MA#(0)	+3.3V
32	RCGCLK	GND	MA#(1)	GND	MA#(2)
33	GND	GND	+1.5V	MA#(3)	+3.3V
34	MA#(4)	+3.3V	MA#(5)	GND	MA#(6)
35	GND	MA#(7)	GND	MA#(8)	+3.3V
36	MA#(9)	+3.3V	MA#(10)	GND	MA#(11)
37	GND	MA#(12)	GND	MA#(13)	+3.3V
38	+1.5V	+3.3V	TMS	GND	+3.3V
39	GND	GND	+1.5V	TRST#	+3.3V
40	SPARECLK0	GND	TDI	GND	TDO
41	GND	GND	+1.5V	TCK	+3.3V
42	MD#(0)	+3.3V	MD#(1)	GND	MD#(2)
43	GND	MD#(3)	GND	MD#(4)	+3.3V
44	MD#(5)	+3.3V	DSTBN0#	GND	MD#(6)
45	GND	MD#(7)	GND	MD#(8)	+3.3V
46	MD#(9)	+3.3V	DSTBP0#	GND	MD#(10)
47	GND	MD#(11)	GND	MD#(12)	+3.3V
48	MD#(13)	+3.3V	MD#(14)	GND	MD#(15)
49	GND	DOFF1#	GND	DOFF0#	+3.3V
50	MD#(16)	+3.3V	DSEL#	GND	MRESET#
51	GND	GND	+1.5V	MD#(17)	+3.3V
52	MUXCLK0	GND	MD#(18)	GND	MD#(19)
53	GND	GND	+1.5V	MD#(20)	+3.3V
54	MD#(21)	+3.3V	MD#(22)	GND	MD#(23)
55	GND	MD#(24)	GND	MD#(25)	+3.3V
56	MD#(26)	+3.3V	DSTBP1#	GND	MD#(27)
57	GND	MD#(28)	GND	MD#(29)	+3.3V
58	GDCMPLT#	+3.3V	DSTBN1#	GND	MD#(30)
59	GND	MD#(31)	GND	MD#(32)	+3.3V
60	MD#(33)	+3.3V	MD#(34)	GND	MD#(35)

5.3.4.3 Power Supply Connector Pinout (J8, J9, J10)

Table 5-40: BERG* Power Supply Connector Pinout

Pin	Signal (Description)	Pin	Signal (Description)	Pin	Signal (Description)
A1	3V_LS	C1	PSx_A0	P1	VCC12
A2	PS_x_PRESENT_L	C2	PS_SCL	P2	VCC12
A3	spare	C3	PSx_FAULT	P3	GND
A4	5V_LS	C4	PRED_FAIL_PSx	P4	GND
A5	POWER_ON_SUPPLIES	C5	12V_RS	P5	GND
A6	PS_KILL	C6	Removed for key	P6	GND
B1	PSx_A1	D1	12V_LS	P7	GND
B2	PS_SDA	D2	PSx_GOOD	P8	GND
B3	PS1RS3	D3	AC_OK_PSx	P9	VCC5
B4	PS1RS5	D4	VBIAS	P10	VCC5
B5	VCC5STBY	D5	GND_SENSE	P11	VCC3
B6	VCC5STBY	D6	-12VCC	P12	VCC3

5.3.4.4   Peripheral Power Connector Pinout (J11)

Table 5-41: 20-pin Peripheral Power Connector J11 Pinout

Pin #	Signal:	Pin #	Signal:
1	VCC12	11	VCC12
2	GND	12	GND
3	VCC12	13	VCC12
4	VCC5	14	VCC5
5	GND	15	GND
6	VCC5	16	VCC5
7	GND	17	GND
8	I2C_GLOBAL_SCL	18	I2C_GLOBAL_SDA
9	GND	19	GND
10	PWR_GOOD	20	VCC12

5.3.4.5   I^{2}C Connector Pinout

Table 5-42: I^{2}C Connector

Name	Pin
CLK	1
GND	2
DATA	3

5.4   Board Level Environmental Specifications

The Ak450NX board set meets the Intel® *Board Environmental Specification 112000, Rev. G,* with the following exception:

The minimum operating temperature is specified at +5° C (instead of 0° C).

Table 5-43: Board Level Environmental Specifications

Temperature	49
Operating	+5° C to +55° C **†**
Non-operating	-40° C to +70° C
Temperature, thermal map	Must not exceed maximum integrated circuit (IC) junction temperature as specified in the component data sheets
Thermal Shock	
Non-operating	-40° to 70° C (-40° to 158° F)
Shock	
Unpackaged	Trapezoidal, 50 g, 170 in/sec.

Packaged	Half sine, 2 msec Simulated Free Fall
	Product Weight Height
	 < 20-lbs. 42”
	   21-40 36”
	   41-80 30”
	   81-100 24”

Vibration	
Unpackaged	5 Hz to 500 Hz, Sine sweep 0.5 G, 15 minutes at each of 3 resonant points
	5 Hz to 500 Hz, 3.1 gRMS random
Packaged	10 Hz to 500 Hz, 1.0 gRMS random
Humidity	
Operating	85% relative humidity (noncondensing) at 55° C (131° F)
Non-operating	92% relative humidity (noncondensing) at 55° C (131° F)
Altitude	
Operating	To 10,000 ft (3,048 m)
Non-operating	To 50,000 ft (15,240 m)
Electrostatic Discharge (ESD)	
Operating	Tested as part of system to 25kV; no component damage
EMI	
Operating	Tested as part of system; required to meet EMI emission regulatory requirements

† Chassis design must provide proper air flow.

5.5 Thermal Requirements

The recommended air flow for the Ak450NX CPU baseboard is a minimum of 300 linear feet per minute (LFM) at 40° C, as measured at the right edge of the processor heat sink (closest to the F16 connector). Intel recommends that air flow be linear with the plane in which the processors reside and direction be from front to back (i.e., from the front panel connector of the board toward the interconnect midplane connector).

To operate within specifications, the Ak450NX PHP I/O baseboard and memory modules require a minimum air flow of 150 LFM at a maximum ambient temperature of 40° C.

These specifications are given as an aid to custom chassis designers. All chassis and cooling designs should be verified to ensure that all board level components are kept within their respective thermal requirements.

5.6 Regulatory Compliance

Safety:

U.S. & Canada	UL1950-CSA 950-95, 3rd Edition (UL,cUL)
Europe	EN 60950, 2nd Edition IEC 950, 2nd Edition CE Mark (Declaration of Conformity to European Directive 73/23/EEC)

EMC:

When configured in a compatible host system:

U.S. & Canada	Verified to FCC, CFR Part 15, Class B & IEC-003
Europe	Verified to EN55022 & EN50082-1 CE Mark (Declaration of Conformity to European Directive 89/336/EEC)
Japan	Verified to VCCI (CISPR 22, Class B)
Australia / New Zealand	Verified to AS/NZS 3548, Class B