Intel® AD450NX Server System

Technical Product Specification

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Enterprise Server Group

Revision History

Date	Rev	Modifications
07/06/98	0.1	Initial draft compiled.
07/16/98	0.2	Preliminary release revision
08/98	1.0	First external release

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Conventions and Terminology

This document uses the following terms and abbreviations:

Term	Definition
Ω	ohms
µA	0.000001 amperes
µf	microfarad
A	amperes (amps)
AC	alternating current
ACPI	advanced configuration power interface
AIC	A450NX Interconnect (board)
ANSI	American National Standards Institute
APIC	Intel® Advanced Programmable Interrupt Controller
ASCII	American Standard Code for Information Interchange
ASIC	application specific integrated circuit
asserted	Active-high (pos. true) signals are asserted when in high electrical state (near power potential). Active-low (neg. true) signals are asserted when in low electrical state (near ground potential).
BMC	baseboard management controller
bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other.
byte	8-bit quantity
C	centigrade
CD	compact disc
CD-ROM	compact disc read only memory
CE	Community European
DC	direct current
deasserted	A signal is deasserted when inactive.
DEMKO	Danishe Elektriske Materiellkontroll (Danish Board of Testing and Approval of Electrical Equipment)
DIMM	dual inline memory module
DRAM	dynamic random access memory
ECC	error correction code
EDO	extended data out
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EMP	emergency management port
EN	European Standard (Norme Européenne or Europäische Norm)
ESD	electrostatic discharge
EU	European Union
F	Fahrenheit
FCC	Federal Communications Commission (USA)
FET	field effect transistor
FP	front panel
FPC	front panel controller
FRB	fault resilient booting
FRU	field replaceable unit
GB	gigabyte (1024 MB)
hard reset	A reset event in the system that initializes all components and invalidates caches.
HSBP	hot-swap backplane

Term	Definition
HSC	hot-swap controller
Hz	hertz (cycles per second)
I/O	input/output
I^2C	inter-integrated circuit
I^2C bus	Two wire bi-directional serial bus, used as the carrier for I^2C communication.
IC	integrated circuit
ICMB	Intelligent Chassis Management Bus
IDE	integrated drive electronics
IEEE	Institute of Electrical and Electronics Engineers
IERR	processor internal error
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
ISA	Industry Standard Architecture
ISP	in-system programmability
JTAG	Joint Test Action Group
KB	kilobyte (1024 bytes)
KB/s	kilobytes per second
kg	kilograms
KHz	kilohertz (1000 Hz)
kV	kilovolts (1000 volts)
LCD	liquid crystal display
LED	light emitting diode
mA	milliamps
MB	megabytes (1024K)
MB/s	megabytes per second
mm	millimeters
ms	milliseconds (0.001 seconds)
n/c	signal not connected
negated	A signal is negated when inactive. Active-low signal names have "_L" appended to the end of the signal mnemonic. Active-high signal names have no "_L" suffix.
NEMKO	Norges Elektriske Materiellkontroll (Norwegian Board of Testing and Approval of Electrical Equipment)
NMI	nonmaskable interrupt
NOM	nominal
OEM	original equipment manufacturer
OS	operating system
OVP	over-voltage protection
PCI	peripheral component interconnect
PDBP	power distribution backplane
PID	programmable interrupt device
PIIX4E	PCI-ISA IDE Xcelerator controller
PLD	programmable logic device
PON	power enable/disable
POST	power-on self test
RAID	redundant array of independent disks
RMS	root-mean-square
RxD	receive data
SAF-TE	SCSI Accessed Fault-Tolerant Enclosures
SCA	single connector attachment

Term	Definition
SCSI	small computer systems interface
SDR	sensor data record
SECC	single-edge connector cartridge
SELV	safe extra low voltage
SEMKO	Sverge Elektriske Materiellkontroll (Swedish Board of Testing and Approval of Electrical Equipment)
SEP	safety enclosure processor
SIO	Super I/O
SMI	system management interrupt
SMC	Standard Microsystems Corp.
SMIC	server management interface chip
SMM	server management module
SMP	symmetrical multiprocessing
SMS	server management software
soft reset	A reset event in the system that forces processors to execute from the boot address, but does not change the state of any caches or peripheral devices.
TCK	test port clock
TDI	test data in
TDO	test data out
TTL	transistor-transistor logic
TxD	transmit data
UART	universal asynchronous receiving/transmitting
UL	Underwriter's Laboratories
USB	Universal Serial Bus
V	volt
VA	volt amperes
Vac	volts alternating current
VCCI	Voluntary Control Council for Interference (by data processing equipment and electronic office machines)
Vdc	volts direct current
VID	voltage ID
Vin	volts in
Vrms	volts root-mean-square
Vstby	volts standby
W	watts

References

Refer to the following documents for additional information:

- *A450NX MP Server Board Set Technical Product Specification*
- *A450NX MP Server Board Set Specification Update*
- *AD450NX Server System Specification Update*
- *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification*
- *AD450NX Server System Product Guide (Order Number 678269-002)*
- *Intel® Server Control, Ver. 1.6 Technical Product Specification*

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1. Introduction

This document describes the chassis and system level features of the AD450NX Server System. This system is a high performance server consisting of the AD450NX server system chassis and the A450NX board set. The features of the A450NX server board set are detailed in the *A450NX Board Set Technical Product Specification*. The combination of these two documents provides a full overview of the AD450NX Server System.

Features Summary

Table 1-1 provides a list and brief description of the major features of the AD450NX server system.

Table 1-1. AD450NX Server System Feature List

Feature	Description
4-way symmetric multiprocessing support	Four slot-2 connectors for the Pentium® II Xeon™ processor. The system may include 1-4 processors. Any unpopulated processor slot requires a front-side bus termination module. MPS 1.1 and 1.4 compliant with the appropriate Pentium II Xeon processor.
8-GB ECC memory	Support of up to 8 GB of buffered EDO RAM using two memory modules.
Redundant power	Three or four 420 W, auto-ranging power supplies. In a four-supply system, the fourth supply is redundant and any supply may be hot-swapped for replacement.
Redundant cooling	Six fans for processor baseboard area and three fans for I/O baseboard area
Twelve hot-swap drives	Two bays, each holding six 3.5-inch hot swappable SCSI 2 hard drives (for a total of 12 SCSI drives). Drives can be swapped in or out of the system without being powered down. The array of drives allows easy setup of redundant array of independent disks (RAID) applications.
Four 5.25-inch peripheral bays	Four 5.25-inch half-height bays for diskette, CD-ROM, and/or tape drives
One IDE boot drive bay	A 3.5-inch internal bay is provided for optional IDE boot drive.
Floppy drive	3.5-inch diskette drive bay externally accessible at upper right front (system ships with drive installed)
CD-ROM	24x IDE CR-ROM (included, depending on configuration)
Front panel LCD	A two line LCD used to provide system status.
Add-in card support	Rail and back window support for up to 10 add-in cards.
Hard drive security	Mechanical security lock for front bezel
System management ready	Intelligent Platform Management Bus (IPMB) for intrachassis communication. EMP/COM2 redirection for remote management.
ICMB support	Intelligent Chassis Management Bus (ICMB) for interchassis communication.
Intrusion switches	Security switches to monitor hard drive bays, doors, and top cover for unwanted intrusion into the system.
SCSI controller	Integrated AIC-7880* Wide SCSI controller for peripheral bay.

Document Structure and Outline

This document is organized into 10 chapters. Each chapter has a modular format, with numbered headings for each major topic and subtopic. Pages are numbered by chapter and page within that chapter (e.g., 1-1). Figures and tables are numbered by chapter and sequence within that chapter.

The content of each chapter is summarized below.

Chapter 1: Introduction
Provides a high level description of the AD450NX Server System. The Introduction also outlines the structure of this document.

Chapter 2: System Chassis Features
Describes the features of the AD450NX Server System chassis.

Chapter 3: A450NX Board Set
Describes the major features of the A450NX Server System board set.

Chapter 4: Chassis Board Set
Describes the features of the supporting chassis boards that are part of the AD450NX Server System.

Chapter 5: System Power Supply
Describes the features of the AD450NX Server System power supplies.

Chapter 6: Server Management Features
Describes the server management architecture of the AD450NX Server System.

Chapter 7: Connector Specifications
Describes the connectors that connect various components of the AD450NX Server System.

Chapter 8: Regulatory Certifications and Compliance
Describes the specifications and regulations for safety and electromagnetic compatibility that are met by the AD450NX Server System.

Chapter 9: Environmental Specifications
Provides the environmental specifications to which the AD450NX Server System is tested.

Chapter 10: Reliability, Availability, and Serviceability
Provides system mean-time-between failure (MTBF) and mean-time-to-repair (MTTR) data.

2. System Chassis Features

This chapter describes the features of the AD450NX server system chassis.

2.1 System Overview

The modular, scaleable architecture of the high performance AD450NX server (AD450NX server system chassis and A450NX server board set) supports symmetrical multiprocessing (SMP) and a variety of operating systems (OS). The server comes with Peripheral Component Interconnect (PCI) and Industry Standard Architecture (ISA) buses. The A450NX server board set consists of an input/output (I/O) baseboard and a CPU baseboard; the baseboards are electrically connected by the A450NX server board set interconnect backplane.

The I/O baseboard contains expansion slots, I/O ports, and various controllers. The CPU baseboard contains four connectors for installing up to four Pentium® II Xeon™ processors packaged in single edge contact cartridges (SECC) and two connectors for installing memory modules. Each memory module supports up to 4 GB of error correction code (ECC) memory.

The CPU and I/O baseboards are mounted vertically, back to back, in the chassis. Add-in boards, memory modules, and Pentium II Xeon processors are installed horizontally into these baseboards. Access to the baseboards is from the sides of the chassis via the removable top and side covers.

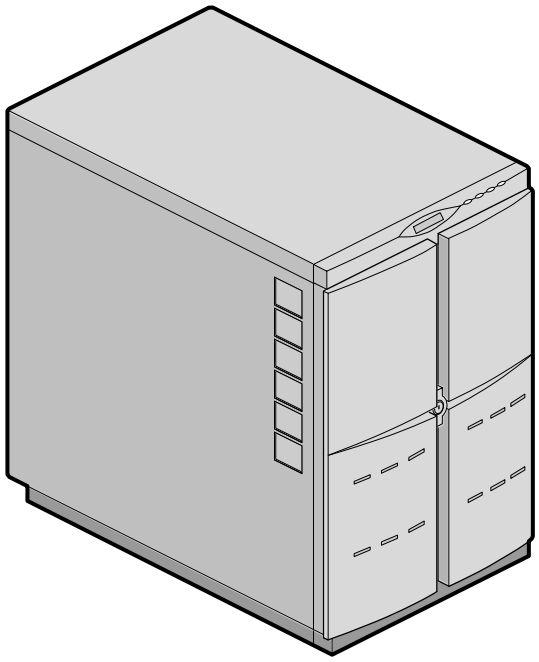

Figure 2-1. AD450NX Server System Chassis

The easy-to-integrate server chassis contains a 3.5-inch floppy (diskette) drive in the 3.5-inch bay. Certain system configurations may also contain a CD-ROM drive in the top 5.25-inch bay. The remaining 5.25-inch bays can house tape drives, CD-ROM drives, and other removable media devices. Any two adjacent 5.25-inch bays can be

converted into a single full-height bay. The chassis provides room for a redundant hot-swap power supply. The system is shipped with three 420-watt, auto-ranging power supplies. A fourth power supply can be added for redundancy. All four power supplies are hot swappable.

The hot-swap bays allow hot swapping of small computer system interface (SCSI) single connector attachment (SCA) hard disk drives without shutting down the server.

The system provides a redundant cooling solution for the CPU and I/O baseboards. The basic controls and indicators are located on the front panel (FP).

The front bezel contains several openings to allow for adequate cooling of the processor and I/O areas of the chassis. The vented door covering of the 5.25-inch drive bays allow airflow to also be provided for devices installed in these bays. Additional ventilation is also provided for CPU and I/O baseboard areas through side covers.

Figure 2-2 shows a block diagram of all of the major components of the AD450NX server system.

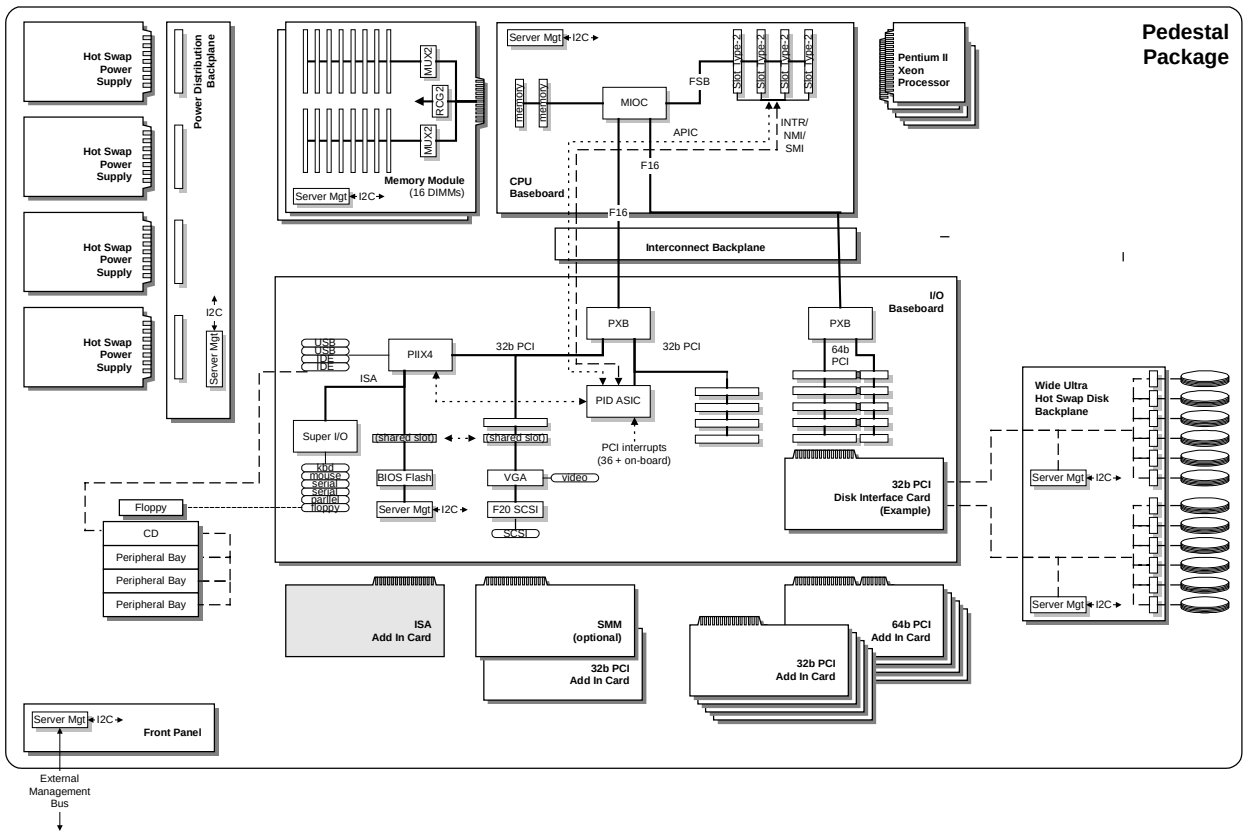

Figure 2-2. AD450NX Server System Block Diagram

2.2 External Chassis Features

2.2.1 System Color

The primary exterior color of the system matches Intel® Color Standard WH8145 (Eileen gray).

2.2.2 Front View of Chassis

The front bezel of the server is composed of four major sections.

- 5.25-inch drive bay door
- plastic snap-on cover for 5.25-inch drive bay
- left and right hot-swap hard drive bay doors on lower half of bezel
- bezel frame

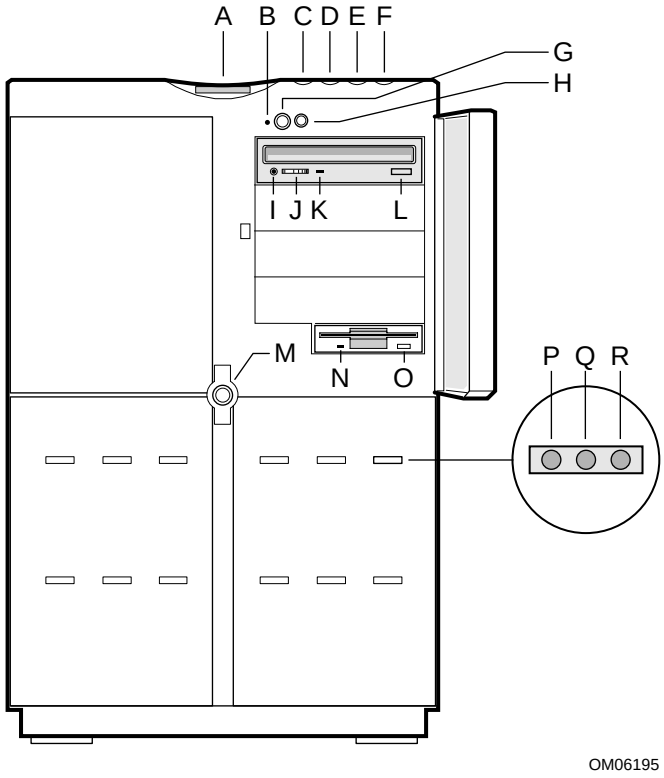

Figure 2-3. Front View of Chassis

Table 2-1. Chassis Features (front)

Item	Feature	Description
Front Panel Controls and Indicators		
A	Front panel LCD	Displays information about system status, including various failure codes.
B	NMI switch	When pressed, causes a nonmaskable interrupt (NMI). This switch is recessed behind the front panel to prevent inadvertent activation. (It must be pressed with a narrow tool.).
C	Power LED (green)	When continuously lit, indicates the presence of DC power in the server. The LED goes out when the power is turned off or the power source is disrupted. When flashing indicates system is in advanced configuration power interface (ACPI) sleep mode.
D	Power fault LED (yellow)	When continuously lit, indicates a power supply failure. When flashing, indicates a 240 volt amp (VA) overload shutdown and power control failure.
E	Cooling fault LED (yellow)	When lit, indicates a system fan whose speed has fallen below a failure threshold has been detected in the server.
F	Drive fault LED (yellow)	When continuously lit, indicates an asserted fault status on one or more hard disk drive in the hot-swap bay. When flashing, indicates drive rebuild in progress.
G	Power switch	When pressed, turns the DC power inside the server on or off.
H	Reset switch	When pressed, resets the server and causes the power-on self test (POST) to run.
CD-ROM Drive		
I	Headphone jack	Provides a connection for headphones.
J	Volume control	Adjusts the volume of headphones or speakers.
K	Activity LED	When lit, indicates the drive is in use.
L	Open/close button	When pressed, opens or closes the compact disk (CD) tray.
Security Key Lock		
M	Two-position lock	Secures the front doors of the bezel.
3.5-inch Floppy (Diskette) Drive Descriptions		
N	Activity LED	When lit, indicates the drive is in use.
O	Ejector button	When pressed, ejects the diskette.
Status LEDs for SCSI Drives in Hot-swap Bays		
P	Drive power LED (green)	When continuously lit, indicates the presence of the drive and that drive is powered on.
Q	Drive activity LED (green)	When flashing, indicates drive activity.
R	Drive fault LED (yellow)	When continuously lit, indicates an asserted fault status on one or more hard disk drives in the hot-swap bay. When flashing, indicates that drive rebuild is in progress.

Note: Some systems may not contain a front bezel and CD-ROM as part of the standard factory configuration.

2.2.3 Rear View of Chassis

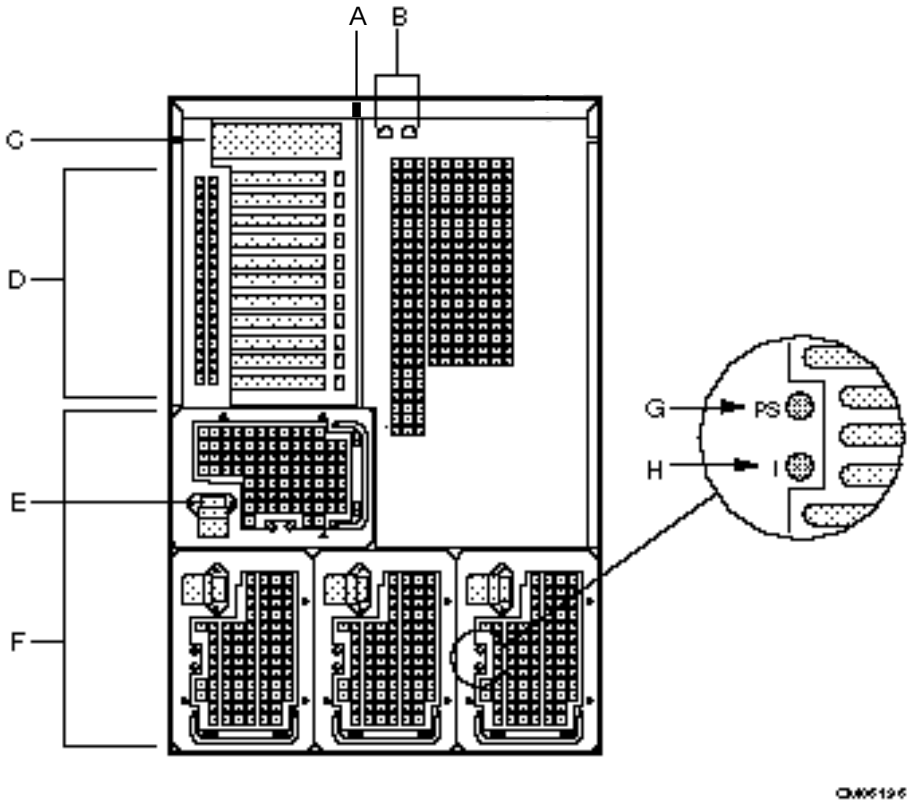

Figure 2-4. Rear View of Chassis

Table 2-2. Chassis Features (rear)

Item	Description
A	Padlock loop for the top and side covers
B	Intelligent Chassis Management Bus (ICMB) connectors in/out (see next page for details)
C	I/O riser card (see next page for details)
D	PCI and ISA add-in board slots
E	AC input power connector
F	Four power supplies
G	PS LED (green) power supply OK. When lit, indicates the power supply is on and working. When off, it may indicate: • the power supply has failed, **or** • that system loading on the power supply is too low to detect failure, **or** • that the supply is not properly plugged in
H	I LED (green) power supply current okay. When lit, indicates power supply is on and working. When off, indicates the power supply has shut down due to an overcurrent condition **or** that the power supply itself has failed.

2.2.4 Riser Card External I/O Connectors

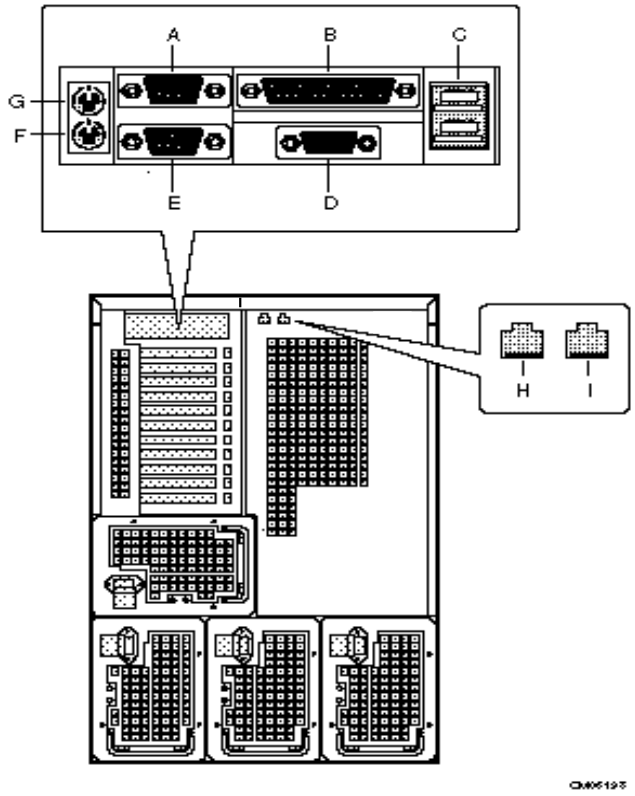

Figure 2-5. Riser Card External I/O Connectors

Table 2-3. Riser Card External I/O Connectors

Item	Descriptions
A	Serial port 1 (COM1), 9-pin RS-232 connector
B	Parallel port (LPT), 25-pin bidirectional subminiature D connector
C	Universal Serial Bus (USB) ports 1 (upper) and 2 (lower), 4-pin connectors
D	Super video graphics array (SVGA) compatible, 15-pin video connector
E	Serial port 2 (COM2), 9-pin RS-232 connector
F	PS/2-compatible keyboard port, 6-pin connector
G	PS/2-compatible mouse port, 6-pin connector
H	ICMB port 1, SEMCONN 6-pin connector
I	ICMB port 2, SEMCONN 6-pin connector

2.2.5 Security

The AD450NX server system chassis provides a variety of mechanical and electronic security options.

- Mechanical two-position key lock for the front bezel doors covering the power and reset switches, 5.25-inch drive bays, and SCSI hot-swap drive bays
- Intrusion sensors for the hot-swap drive bay access doors

- Intrusion sensor for the chassis top cover
- Padlock loop for top and side covers (at rear of chassis)
- BIOS and server management functions provide additional security options

2.2.5.1 Front Bezel Lock

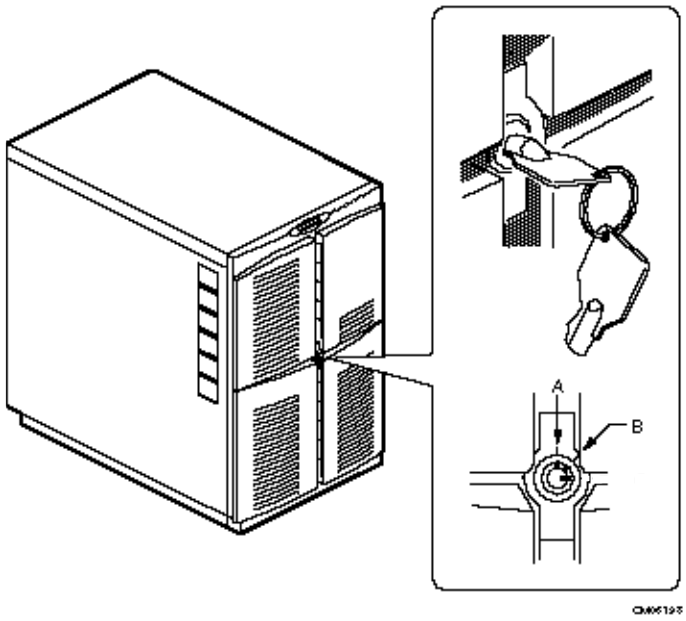

Figure 2-6. Front Bezel Security Key Lock

Table 2-4. Front Bezel Key Lock Features

Position	Action
A	Unlocked position. (Unlocks all doors on front of the chassis.)
B	Locked position. (Locks all doors on front of the chassis.)

2.2.6 Back of Chassis Lock

The processor and I/O baseboard areas can be secured with a padlock (not provided) through a loop on the back of the chassis. The mechanical design of the top and side access covers allows one padlock to secure all three covers.

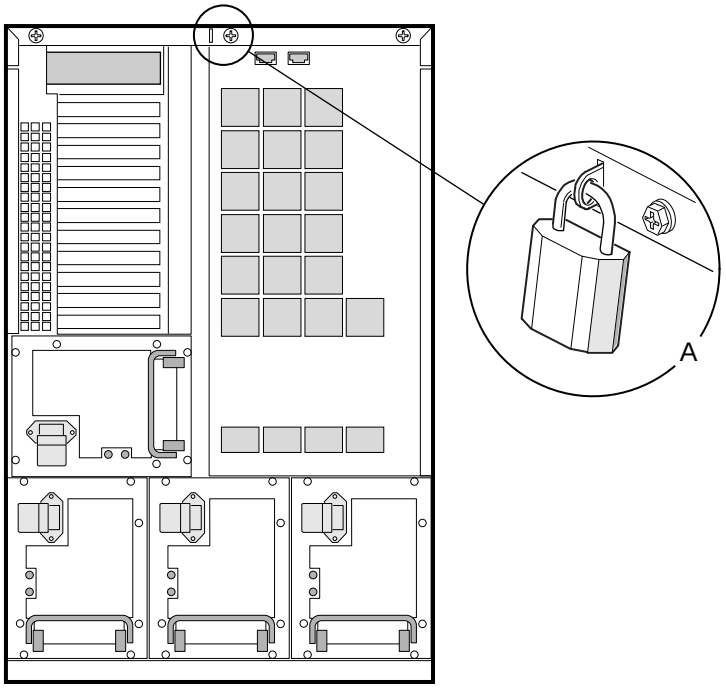

Figure 2-7. Top and Side Covers Security Padlock Loop

2.2.7 Chassis Rollers

The plastic base of the chassis includes four rollers. The rollers allow free movement of the chassis when rolling into or out of a location.

The rollers at the front side of the chassis are equipped with a locking mechanism. Each roller has its own locking latch. Flipping out the small latch on the outer side of the roller will release the lock mechanism, as shown in the following diagram. With the latches pushed in, flush with the frame, the front rollers are locked.

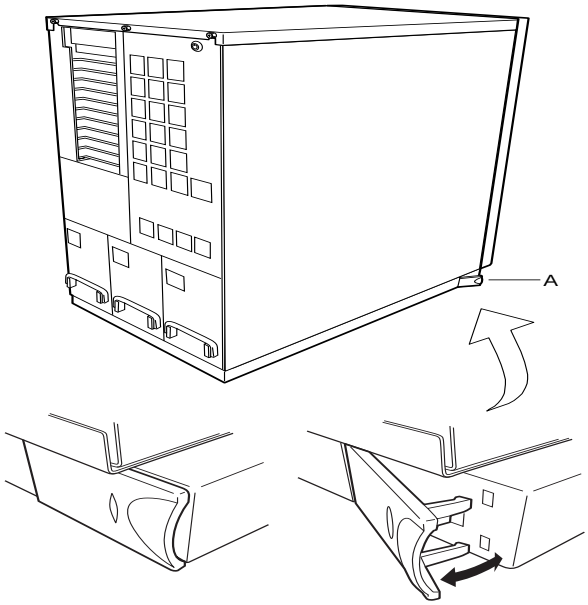

Figure 2-8. Chassis Rollers Locking Mechanism

2.2.8 Physical Specifications

Table 2-5 describes the physical specifications of the AD450NX system.

Table 2-5. Dimensions and Weight

Height[2]	27.5 inches (700 mm)
Width	17 inches (430 mm)
Depth[2]	28 inches (710 mm)
Weight[1]	~160 pounds (~73 kg) without packing ~185 pounds (~84 kg) with packing
Front clearance	12 inches (305 mm)
Side clearance	3 inches (76 mm) additional side clearance required for service
Rear clearance	5 inches (127 mm)

Notes: **1.** System that does not contain CD-ROM and front bezel in factory default configuration will be slightly less than the specified weight.
2. System dimensions include the rollers for height and exclude the power supply handles for depth.

2.3 Internal Chassis Features

2.3.1 Power System

Three 420W, auto-ranging power supplies in a standard configuration provide the modular power system for the AD450NX server. The power system may be configured with four power supplies (3 + 1) for power redundancy. The power supplies are mounted in a 3 + 1 pattern in the bottom of the chassis. Each power supply has its own power cord.

When the server is configured with four power supplies, the user can hot swap a failed supply without affecting the system functionality. The AC line cord must be removed from the failed power supply before it can be removed and replaced.

The power distribution backplane implements power distribution of the internal power system with minimal active circuitry. The power distribution circuitry reports quantity and location of the installed power supplies through an I^2C communications bus to server management. If a single output from the power distribution backplane exceeds 240 volt amp (VA) to areas that are user accessible (hot-swap drive bays, 5.25-inch drive bays and 3.5-inch floppy drive bays) while the system is energized, a current sensing protection circuit shuts down the entire power system.

The three 420 W, auto-ranging power supplies are capable of handling up to 12 hard drives at 24 W per drive (typical 3.5-inch by 1.6-inch, 7200 RPM drive) and four Pentium II Xeon processors at a maximum of 50 W per processor.

The processor baseboard provides connectors for six Voltage Regulator Module (VRM) 8.3 compatible voltage converters. The converter input is +12 volts (V) from the power supply. The VRMs are used to power the processor and L2 cache core components of each Pentium II Xeon processor in the following manner. Each Pentium II Xeon processor core has its own converter, whereas one converter is provided per pair of Pentium II Xeon processor L2 cache cores. This VRM power distribution scheme will accomidate processors consuming a maximum of 65W of power.

The total power requirement for the A450NX server board set exceeds the 240 VA energy hazard limit that defines an operator accessible area. As a result, only qualified technical individuals should access the processor and I/O baseboard areas and should ensure that AC power has been removed from the system before doing so.

The 240 VA protection circuits for the hot-swap drive bay area protect the user from a 240 VA energy hazard while installing or removing a hard drive. Refer to the *System Power Supply* chapter of this document for power specifications.

Table 2-6. Power Supply Output Ratings

Power Supply Outputs	Individual Supply	3 Supplies† Non-redundant	4 Supplies† Redundant
5 V	32 A	90 A	90 A
12 V	16 A	45 A	45 A
3.3 V	15 A	42 A	42 A
-12 V	1 A	1 A	1 A
5 V standby	100 mA	360 mA	360 mA

† Forced load sharing for 5, 3.3, and 12 volts only. The +5 V standby load sharing is a passive load sharing technique.

2.3.2 Cooling System

The chassis cooling system is designed around a maximum power dissipation of 65 W per Pentium II Xeon processor. The cooling design for the hard drives in the hot-swap bays is 24 W per drive with three power supplies. Air flows into and through the chassis via inlets in the bezel, and exhausts out the rear of the chassis.

There are three independent cooling areas throughout the chassis: a CPU baseboard area, an I/O baseboard area, and the hot-swap bay area. The fan arrays for the I/O and CPU baseboard areas are designed for N + 1 redundancy. The standard factory configuration of the AD450NX system is redundant, with three fans in the I/O baseboard area and six fans in the CPU baseboard area. Redundancy is provided with respect to only the first fan failure on either side. Each fan provides tachometer signal output to indicate a fan failure. The power supply fans provide cooling in the hot-swap bay area. When a fourth redundant power supply is installed in the server, cooling of the hot-swap bay is also redundant. Refer to the *System Cooling Fans* section in the *Chassis Board Set* chapter for further details on fans redundancy.

The inlet air for the CPU and I/O baseboards is not preheated. However, the inlet air for the power supplies is preheated because the hot-swap drive bays are in the front of the power supply fans.

2.3.3 Drive Bays

The AD450NX server system chassis provides the following drive bays:

- One 3.5-inch floppy drive bay
- Four 5.25-inch user-accessible drive bays for removable media
- One internal 3.5-inch bay for an IDE boot drive
- Twelve 3.5-inch hot-swap bays for 1” or 1.6” high SCSI SCA hard disk drives

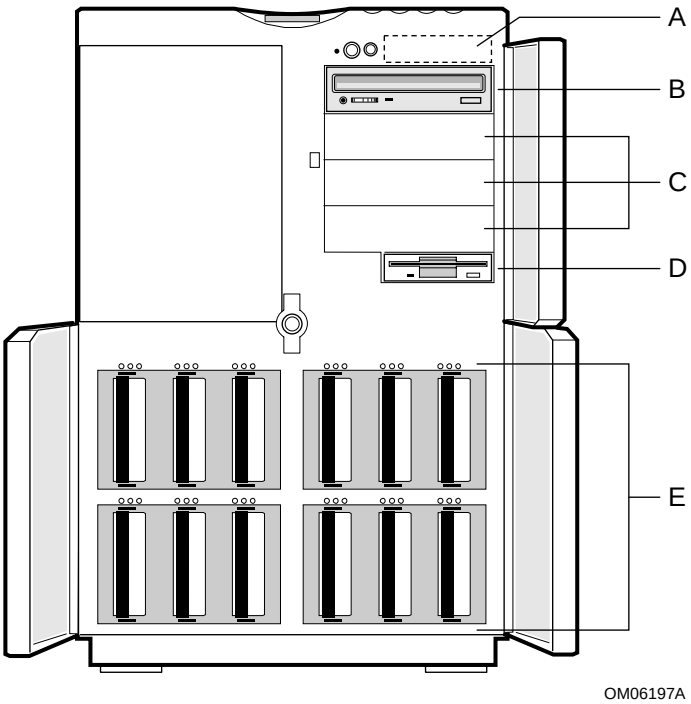

Figure 2-9. Chassis Drive Bays

Table 2-7. I/O External Connectors

Item	Bay	Description
A	3.5-inch bay	IDE boot drive (internal)
B	5.25-inch bay	CD-ROM drive†
C	5.25-inch bay	three empty bays
D	3.5-inch bay	3.5-inch floppy drive
E	3.5-inch bay	12 hot-swap bays

† Some systems will contain a CD-ROM drive as part of the standard factory configuration.

2.3.4 3.5-inch Internal IDE Drive Bay

The server contains an internal 3.5-inch bay for an optional IDE boot drive. The top and left side covers must be removed to gain access to this bay.

2.3.5 5.25-inch User-accessible Drive Bays

The system includes four 5.25-inch half-height drive bays. These bays are designed for devices with removable media; for example, floppy disks, CD-ROMs, tape drives. Any two adjacent 5.25-inch bays can be converted into a single full-height bay.

The 5.25-inch drives can be removed directly from the front of the chassis after removing the 5.25-inch drive bezel. The drive bezel is retained by snap features that are accessible when the side access cover is removed. Cosmetic cover panels, installed by the factory, cover all unused 5.25-inch bays.

Note: Installation of hard disk drives in the 5.25-inch user accessible bays is not recommended. This is due to excessive electromagnetic interference (EMI) radiation and susceptibility to electrostatic discharge (ESD) associated with drives operating in this area.

2.3.6 3.5-inch User-accessible Drive Bay

The system ships from the factory with a 3.5-inch 3-mode floppy drive installed in the user accessible drive bay.

2.3.7 SCSI Hot-swap Drive Bays

Twelve 3.5-inch hot-swap bays provide space for 3.5-inch wide by 1.0 or 1.6-inch high, SCA SCSI hard disk drives. The Wide Ultra SCSI hot-swap backplane provides industry standard 80-pin SCA-2 connectors arranged in two rows (top and bottom); each row is on a separate SCSI channel. Up to 12 industry standard Wide/Fast-20 SCA-type SCSI III hard disk drives can be installed in these bays. The Wide Ultra SCSI hot-swap backplane is designed to accept drives that consume up to 28 W of power and run at a maximum ambient temperature of 50°C (112°F). However, three or four 420 W, auto-ranging power supplies are capable of handling up to 12 hard drives at only 24 W per drive.

Aluminum drive carriers that accommodate the 3.5-inch wide drives are required as part of the hot-swap, cooling and EMI design implementation. The carrier is attached to the drive with four fasteners and is retained in the chassis by a locking handle. Due to its role in containing EMI emmissions, these carriers must be installed even when not used with a hard drive.

The bank of LEDs above each row of drives displays individual drive status. There are three LEDs for each drive: a power on LED (green); an activity LED (green); and a fault LED (yellow). A fault LED on the front panel board also indicates a fault on these drives.

Note: Because all hard drives have different cooling, power, and vibrational characteristics, Intel is validating certain types of hard drives in the AD450NX server system chassis. Consult your Intel representative for a list of validated drives.

2.3.8 Expansion Support

Table 2-8 summarizes the expansion support provided by the AD450NX server system.

Table 2-8. Expansion Support

Quantity	Type
6	32-bit PCI expansion bus slots (some factory configurations will contain a two-channel SCSI controller in one of the 32-bit PCI expansion bus slots)
5	64-bit PCI expansion bus slots
1	ISA expansion bus slot (shares a common chassis I/O expansion slot with a 32-bit PCI slot; either the ISA slot or the PCI slot can be used, but not both)
12	Single connector attachment (SCA) SCSI hard disk drive bays
4	5.25-inch half-height drive bays. Some systems will contain an IDE CD-ROM drive in the top bay as part of the factory standard configuration.
32	72-bit EDO DIMM module sockets (16 per memory module).

2.3.9 A450NX Server Board Set Insertion Mechanism

Approximately 100 pounds of force are required to fully insert the FutureBus* (male) connectors on the I/O interconnect backplane into the connectors on the processor and I/O baseboards. Since the baseboards are stationary inside the chassis, a mechanical system is used to insert and remove the interconnect backplane connectors into and out of the baseboard connectors. This inertion and extraction mechanical system is know as the A450NX Interconnect (AIC) Mechanism and is shown in Figure 2-10 below.

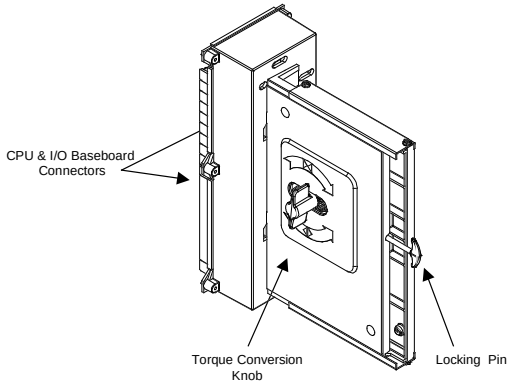

Figure 2-10.A450NX Interconnect Mechanism

The AIC Mechanism includes the addition of a Locking Pin at the back of the mechanism to reduce the chance that the AIC connectors could back apart from the I/O or CPU baseboard during shock and vibration associated with the transportation of the server system. This locking pin needs to be pulled rearward (opposite CPU and I/O baseboard) to allow the movement of the Torque Conversion Knob which backs apart the two boards. Without proper disengagement of this pin, use of the AIC mechanism will seem inordinately difficult and may damage the mechanism. Access to the locking pin can be gained by removing the system EPAC material and CPU baseboard fan arrays.

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3. A450NX Board Set

The A450NX server board set is a 1-4 processor board set based on the Pentium II Xeon processor and the Intel® 450NX PCIset. The Pentium II Xeon processor is the next generation Intel® architecture processor beyond the current Pentium II processor. Both the Pentium II Xeon and the 450NX PCIset have been optimized for 4-way server applications.

Features

- Pentium II Xeon processor support
- Intel 450NX PCIset
- Support for up to 8 GB of 3.3 V EDO DRAM (DIMMs)
- Three peer PCI buses (two 32-bit and one 64-bit bus, all 5 V, *PCI Spec. Rev 2.1* compliant)
- Full length I/O slots: five 64-bit, six 32-bit, and one ISA (shared with one of the 32-bit PCI slots)
- Onboard Ultra or Fast/Wide SCSI controller for peripheral devices (Adaptec 7880*)
- Two IDE controllers
- PCI to ISA bus accelerator/bridge (PIIX4E)
- Universal Serial Bus (USB)
- SMC Super I/O* component to handle all PC legacy functions (keyboard, mouse, serial, parallel, etc.)
- Programmable interrupt device (PID) - custom Intel® Application Specific Integrated Circuit (ASIC), which provides interrupt steering and I/O Advanced Programmable Interrupt Controller (APIC) facilities
- Complete built-in server management capabilities
- Internal Intelligent Platform Management Bus (IPMB) based on I^2C for communicating information between all boards in the chassis
- Field replaceable unit (FRU) information stored on all boards (P/N, S/N, board name, etc.)
- Temperature sensors on all major boards for temperature monitoring

3.1 Board Set Overview

The A450NX server board set is a dual baseboard design that contains a total of six individual boards.

- CPU baseboard (contains the processor and memory complexes)
- I/O baseboard (contains all I/O functions including PCI and ISA slots)
- I/O riser card (plugs into the I/O baseboard and contains all legacy connectors [video connector, parallel port, 2 serial ports, keyboard, and mouse connectors])
- Memory module with 16-DIMM connectors (two memory modules or one memory module and one termination module are needed)
- Interconnect backplane (provides connection between the I/O baseboard and processor baseboard. Also provides the power interface for the whole board set. This is essentially a passive backplane.)
- Front-side bus terminator module (terminates the processor bus. This module is used when a processor is not installed into a processor slot.)

The baseboards, when installed into a chassis, are physically placed back to back, connected to each other by the interconnect backplane. The two F16 buses of the 450NX PCIset electrically connect the two baseboards together. Power to the board set is supplied through the interconnect backplane.

For more details, refer to the A450NX MP Server Board Set Technical Product Specification.

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4. Chassis Board Set

This chapter describes the features chassis boards that are part of the AD450NX server system. The AD450NX server system contains the A450NX board set and three chassis boards: the front panel board, the hot-swap SCSI backplane, and the power distribution backplane.

4.1 Front Panel Board

The front panel board provides a simple user interface to the AD450NX server system. Push-button switches allow for power up and reset as well as NMI assertion. LEDs indicate when the server is powered on and when there has been a power supply failure, hard drive failure, or a fan failure. The LCD panel provides information about the server, including boot status, available number of processors, and other server management information.

The front panel board also allows other servers to communicate with the AD450NX server system, even while power is down, via an ICMB. The ICMB is an extension of the IPMB. All functions of the front panel are controlled by a Phillips 80C652* microcontroller.

All functions are available at all times when the main power is available. The front panel board connects to the rest of the AD450NX server system through a 60-pin ribbon cable. This cable then attaches to the front panel connector, which is located on the I/O baseboard of the A450NX board set.

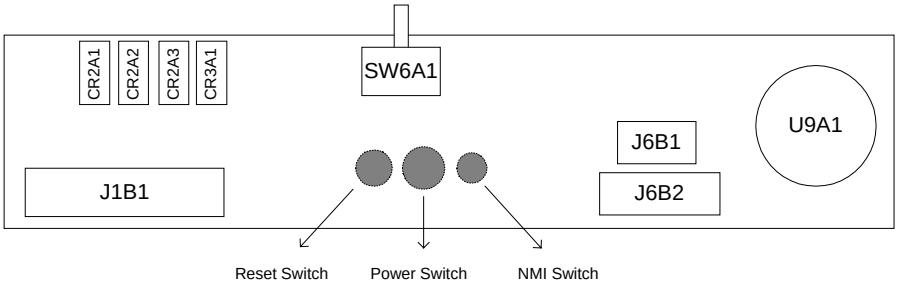


Figure 4-1. Front Panel Board Placement Diagram

Note: All connectors are located on the primary side of the front panel board whereas the NMI, Reset and Power push buttons are located on the secondary side on the board.

Table 4-1. Front Panel Board Reference Designators

Connector	Description
J1B1	Front panel connector
J6B1	LCD backside area light
J6B2	LCD power and data connector
SW6A1	Chassis intrusion switch for top cover
U9A1	Speaker
CR2A1	Drive fault LED
CR2A2	Cooling fault LED
CR2A3	Power fault LED
CR3A1	Power LED

4.1.1 Microcontroller

All of the **intelligent** functions on the front panel are implemented with a Phillips 80C652 microcontroller, which has 32KB of RAM and 64KB of FLASH for both code and data. The FLASH contains the firmware required by front panel microcontroller and is field upgradeable using the Intel provided firmware update utility. The RAM is used to execute the code and to store the stack and local variables.

The microcontroller is powered from the 5 V standby, which is always active as long as AC power is present. The microcontroller records the current power state (on or off) in its nonvolatile memory. In the event of an AC power failure, the front panel controller (FPC) can return the power status of the server to its status prior to the power failure.

The microcontroller constantly monitors the switches, the state of the power supplies (via its private I^2C bus), and the ICMB. While the server is powered on, the front panel also monitors the IPMB and responds to IPMB messages.

4.1.2 Drive Fault LED

The Drive Fault LED is used to indicate a hard drive failure. As with the Power Fault LED, this LED is also off during normal hard drive operations. The Drive Fault LED blinks when a drive is being rebuilt. The Drive Fault LED is controlled by the FPC upon receiving a command via the IPMB.

4.1.3 Cooling Fault LED

The Cooling Fault LED lights up only when the BMC receives a message from the HSC reporting a fan failure in the disk subsystem. Since the Cooling Fault LED is under the direct control of the BMC, there is no FPC interface with this LED. There is a direct connection between the BMC and the LED.

4.1.4 Power On LED

The Power ON LED is illuminated whenever +5 V is active (>~3 V). There is no microcontroller interface for this signal. It is directly driven by the power subsystem. The Power ON LED goes off when the power is turned off or the power source is disrupted. The blinking Power ON LED indicates that the system is in ACPI sleep mode

4.1.5 Power Fault LED

The Power Fault LED is controlled by the FPC and is used to indicate the status of a system power fault. The Power Fault LED is lit only when there is a fault detected in the system power, causing a signal to be asserted to the FPC. This LED is off during an FPC reset.

The Power Fault LED blinks if a system power control failure is detected. For example, if a 240 V overload condition occurs, the LED begins blinking. Since the LED is powered by a +5 V standby, it can be illuminated even when the main +5 V switched power is invalid.

Table 4-2. Power Fault Light States

Power State	5 V Standby	PWR_GD	PS-ON	Power on LED	Power Fault LED	Condition
ON	ON	ON	High	ON	OFF	Power ON and OK
ON	ON	OFF	High	OFF	ON	Supply failed
ON	ON	OFF	Low[1]	OFF	BLINK	240 VA overload
ON	OFF	ON[3]	High	OFF	OFF[2]	5 V standby failure[3]
ON	OFF	OFF	High	OFF	OFF[2]	AC power failed[3]
OFF	ON	ON	n/a	ON	BLINK	Power control failure[4]
OFF	OFF	ON[3]	Low	OFF	OFF[2]	5 V standby failure[3]
OFF	ON	OFF	Low	OFF	OFF[2]	Normal power OFF
OFF	OFF	OFF	n/a	OFF	OFF[2]	Normal OFF & unplugged

Notes:
1. The power subsystem forces PS-ON to be LOW when a 240 VA overload occurs. Thus, PS-ON is both an input and output signal.
2. No power fault light when there is no AC power!
3. If 5 V standby fails while 5 V is up, the power supplies automatically turn off. A different operation would require having circuitry that would direct 5 V to the microcontroller and LED, when 5 V standby fails. Note that with this model, it would still be the case that once the system was powered off, it couldn't be powered up again until 5 V standby was provided.
4. An unlikely circumstance. However, a blinking power fault indication is used to indicate that the condition may not be a supply failure.

4.1.6 Front Panel LCD

The front panel LCD is a Stanley GMD1620A*. The LCD and its corresponding LED backlighting unit are powered by the main +5 V power. Therefore, front panel LCD information is available only when the main +5 V of power is available. The LCD is used by the BIOS to display messages during POST. The LCD can also be used by the system management software as a status display during run-time. The display unit is controlled by the FPC and is accessed by the BIOS by sending IPMI commands to the FPC.

4.1.7 Power Supply Monitoring

Each of the four power supplies has two signals that can be monitored. They are the PWR_SUP_PRESENT and the PWR_SUP_FAULT signals. The state of these signals is monitored by the FPC via the private I^2C bus.

4.1.8 Chassis Intrusion Signal

The chassis cover intrusion switch is located on the front panel board. When the chassis top cover is removed, the intrusion switch enables the chassis intrusion signal, indicating that the chassis is being accessed. The FPC monitors the state of the chassis intrusion signal from the front panel. The FPC debounces the signal and makes the status of the signal available via an IPMI command. If the event logging is enabled in the BIOS, the FPC also generates an event message when the chassis intrusion goes from 'Secure' to 'Not Secure.' These event messages are limited to ~1/second to avoid multiple messages due to jostling that may occur when a cover is being removed.

4.1.9 Speaker

The system speaker resides on the front panel board. The impedance of the front panel speaker is approximately 8 ohms. Either the FPC or the I/O baseboard can control the impedance. The speaker is energized if either source commands the speaker ON.

4.1.10 ICMB and EMP/COM2 Redirection

The ICMB and the EMP/COM2 port are electrically connected to the I/O baseboard. However, both are controlled by the FPC. Also, both the COM2 receive data (RxD) and the ICMB RxD signals are routed to the FPC and are continuously available, regardless of the state of any other control signals.

4.1.10.1 ICMB

The ICMB provides a means by which an intelligent device on the IPMB in one chassis communicates with the intelligent device on the IPMB in another chassis. The ICMB protocol is used for interchassis communications. This is possible because the server provides two SEMCONN 6-pin connectors which enable multiple servers to be daisy chained together.

The ICMB is used to provide remote control and status information on servers that cannot be obtained through in-band channels, either because the information is not provided through those channels or because the in-band channels are not available (e.g., when the chassis is powered down). The ICMB has been targeted to support up to 42 chassis and 300 feet of cable. The ICMB, as with other instrumentation described in this document, is accessed by the system management software.

ICMB provides the ability to communicate information such as:

- Chassis FRU information
- Chassis power control
- Front Panel Board FRU information

4.1.10.2 EMP/COM2

The emergency management port (EMP) is a system feature that allows the COM2 connectors to provide a level of systems management when the server is powered down or in a preboot or OS-down state. This is done through a point-to-point RS-232 connection or with an external modem. The AD450NX server system ships with EMP console software. This software provides the interface to connect from a workstation console to the EMP on the server system.

The EMP provides feature access to system power up/down control, system reset, and chassis FRU inventory information.

The EMP interface is intended for use in a secure environment. A password can be configured to provide security on the interface and system configuration options can be used to disable the interface entirely. The EMP password and other EMP configuration options are available in BIOS setup.

The EMP consists of a management microcontroller device, known as the EMP controller, and additional EMP mux circuitry that allows a system serial port connector to be shared between the EMP controller's serial controller and the system serial controller. The EMP controller functions are incorporated within the FPC.

Special hardware allows the transmit data (TxD) and receive data (RxD) signals for the COM2 port connector to be connected either to the EMP controller or the baseboard serial port controller under control of the EMP controller.

The port transceivers are powered by 5 V standby power, so they can be used by the EMP controller when the system is powered down.

4.1.11 Power Button

As long as electrical power is available, the power button on the front panel always powers up the system. However, configurable security options determine whether this button may be used to power down the system.

The board set can be configured to support ACPI or legacy mode. Legacy mode is the traditional way of controlling power. It is in effect both when the system is powered down and on initial power up. For those operating systems that do not support ACPI mode, the BIOS has a setup option that locks the system into legacy mode. In legacy mode, the power is either on or off. If the power is on, depressing the button powers off the system. If the system is off, depressing the button powers on the system.

In ACPI mode, the power can be on, off, or in sleep mode. The system can be switched to ACPI mode by the OS during OS startup. APCI can be selected only in operating systems which support it, such as Windows NT 5.0.

In ACPI mode, a brief press and an extended press of the power button have different consequences. If the power is on and the button is depressed continuously for more than four seconds, a Power Button Override takes effect and the system is powered down. The results of a brief press of the power button (less than four seconds) results in one of three responses, as discussed in Table 4-3.

Table 4-3. Effect of Brief Press on Power Button

System power state when a brief press occurs	ACPI Effect	Legacy Effect
power is down	turn on power	turn on power
power is up	generate a sleep request to OS	turn off power
system is in sleep mode	resume power state that was in effect before system went to sleep	n/a

4.1.12 Reset Button

During normal operation, when secure mode is inactive, pressing the reset button causes the system to perform a hard reset. If secure mode is active, a hard reset is blocked by the FPC, which also issues a Secure Mode Violation event message via the IPMB.

4.1.13 NMI Button

A nonmaskable interrupt (NMI) is used to notify the operating system of a fatal system hardware condition, such as a uncorrectablr parity error or an unrecoverable bus error. The NMI button is included on the front panel to generate a memory dump in the event of such a fatal system condition. The NMI button is intended as a troubleshooting device and should be used with caution; pressing this button causes a system halt. To prevent inadvertent activation of the NMI button, the button is hidden behind the main front panel bezel, with only a small pinhole-sized opening in the bezel for access. A small tool is required to activate the button.

4.1.14 I^2C Interfaces

The FPC interfaces to two I^2C buses: the FPC private I^2C bus and the global I^2C bus (IPMB).

4.1.14.1 Private I²C Bus on the FPC

The FPC's private I²C bus is used to communicate with nonintelligent I²C devices that do not support multimaster mode. These devices are listed in Table 4-4.

Table 4-4. Nonintelligent I²C Devices

Device	Address
Front panel board 1/4KB by 8 serial EEPROM (Front panel & chassis FRU information)	A0H to A1H
Power distribution backplane 1/4KB by 8 SEEPROM (power distribution backplane FRU information)	A2 H to A3H
Power distribution board I/O port 1 (power supplies fault/presence signals)	40H to 41H
Power distribution board I/O port 2 (F16 cable sense and misc. signals)	42H to 43H

4.1.14.2 Global I²C Bus

The global I²C bus on the front panel is automatically connected to the IPMB whenever power is valid. Electrical isolation circuity on the I/O baseboard disconnects the IPMB from the front panel global I²C bus when the system power is not valid. This bus allows communication between intelligent I²C devices that operate in multimaster mode; specifically, this bus connects the FPC, the BMC, and both HSCs.

4.1.14.3 I²C Accessed Feature

The 256-byte FRU SEEPROM device resides on the FPC private I²C bus. This device, an Atmel 24C02*, is accessed via the front panel controller on the AD450NX server system front panel board. The FPC and BMC are interconnected via the IPMB. The 24C02 device is accessible at the addresses show in Table 4-5.

Table 4-5. Front Panel Board I²C Address Map

Device	Function	I²C Address
24C02*	Front panel FRU info	A0h, A1h

The 24C02, when accessed via the I²C bus, provides the FRU information shown in Table 4-7. This information is read and made available by Intel® Server Control.

The 24C02 SEEPROM has 256 bytes of programmable space, which is broken into four areas. Table 4-6 is a list of the areas, a brief description of their purpose, and the space allocated to each area.

Table 4-6. SEEPROM Programming Areas

Area	Size	Description
Common header	8 Bytes	Programming offsets to the other areas below.
Internal use	80 Bytes	This area is reserved for general purpose use by Intel® server management firmware/controllers.
Chassis info	32 Bytes	Contains chassis information.
Board info	64 Bytes	Contains the board FRU information listed in Table 4-7.
Product Info	72 Bytes	Available for OEM use†

† An Intel provided utility, called the *FRU & SDR Load Utility,* allows the OEM to program any FRU SEEPROM in the chassis.

Table 4-7 lists the board specific FRU information that will be programmed into the board information area.

Table 4-7. FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. date/time	Time & date of board manufacture (value programmed [in hex] is the number of minutes after 0:00 hrs 1/1/96)	000f593h (Translation to date & time shown below) f593h = 62867 min = 43 Days & 947 min = Feb 12, 1997, 3:47pm	2
Manufacturer	Board manufacturer	Intel	1
Board product name	Board name/description	Drake front panel	1
Board serial number	Intel board serial number	N42385906	2
Board part number	Intel board part number	6650049-002	2

Notes: 1. Actual value programmed into the board.
2. Example value. Actual value will vary with each board.

Table 4-8 identifies the exact purpose for which bytes are allocated within the 24C02 SEEPROM. This information is useful for those who will be accessing the hardware directly for information (i.e., BIOS developers and server management software developers).

Table 4-8. Front Panel Board FRU SEEPROM Byte Map

Address	Length	Description	Default Value
0x00	1	Common header format version	0x01
0x01	1	Internal use area offset (8-byte multiples)	0x01
0x02	1	Chassis information area offset (8-byte multiples)	0x0B
0x03	1	Board information area offset (8-byte multiples)	0x0F
0x04	1	Product information area offset (8-byte multiples)	0x17
0x05	2	Zero padding	
0x07	1	Common header checksum	0xCD
0x08	80	Internal use area	
0x58	32	Chassis information area	
0x78	1	Board information area format version	0x01
0x79	1	Board Information area length (8-byte multiples)	0x08
0x7A	1	Unicode country base	0x00
0x7B	3	Manufacturer date/time	
0x7E	1	Board manufacturer type/length byte	0xC5
0x7F	5	Board manufacturer (ASCII)	‘Intel’
0x84	1	Product name type/length byte	0xD1
0x85	17	Product name	‘Drake Front Panel’
0x96	1	Board serial number type/length byte	0xCC
0x97	12	Board serial number	
0xA3	1	Board part number type/length byte	0xCA
0xA4	10	Board part number	
0xAE	1	No more fields flag	0xC1
0xAF	8	Zero padding	
0xB7	1	Board information area checksum	
0xB8	72	Product information area	

4.2 Power Distribution Backplane

The AD450NX power distribution backplane serves as an interface between the individual power supplies, the A450NX interconnect backplane, and the Wide Ultra SCSI hot-swap backplane. Power supply monitoring and margin control, as well as the signal interface between the interconnect backplane and the hot-swap backplane, are handled on the power distribution backplane. The power distribution backplane provides the following features:

- 240 volt amps (VA) protection for the SCSI hot-swap backplane
- Normal and high voltage settings for cooling fans
- Supply present and fault monitoring per supply
- Power good indication
- A450NX interconnect cable detect
- Cable detect for fourth power supply
- Voltage margin circuits for +5 V and +3.3 V
- Redundant power supply for fault tolerance

Figure 4-2 presents a generalized power supply distribution layout. Three supplies connect directly with the power distribution backplane, while the fourth supply is connected through the redundant supply board cable assembly.

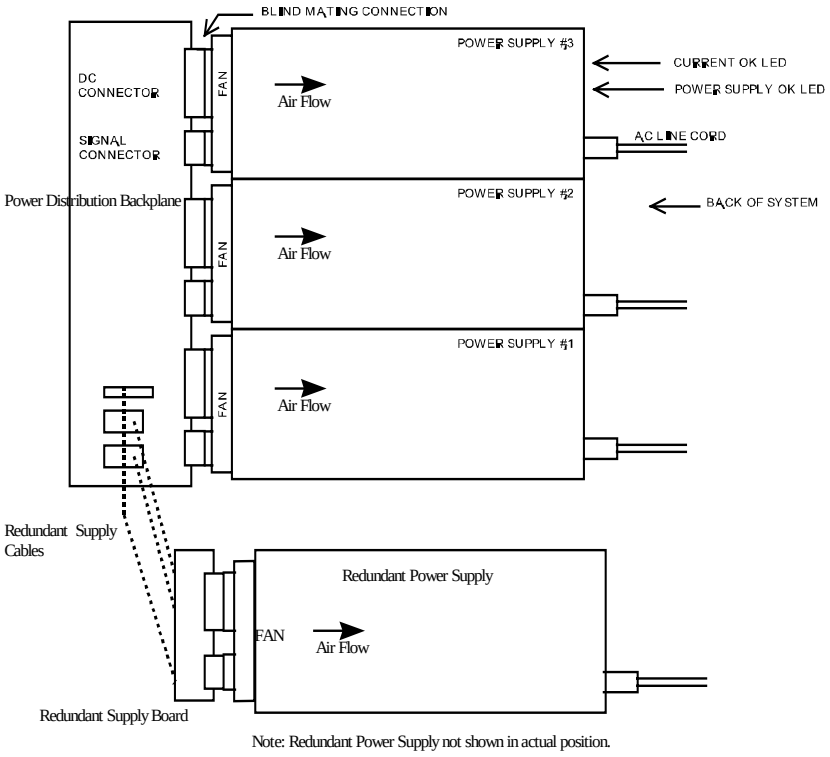


Figure 4-2. Power Supply Setup

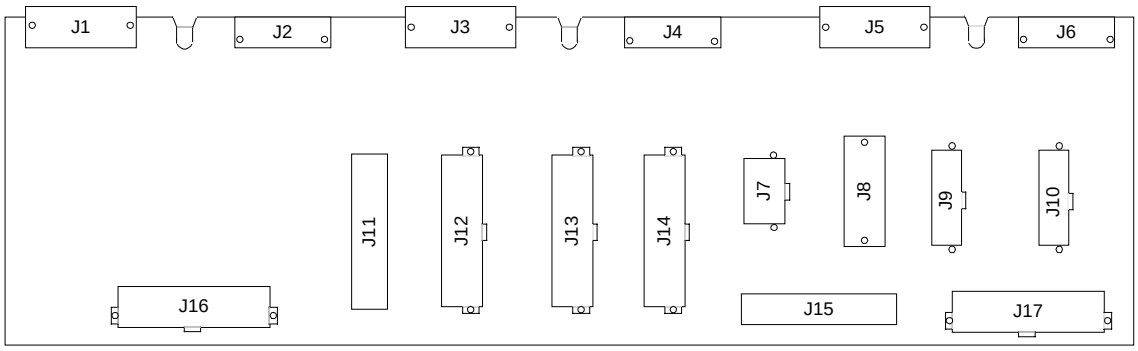


Figure 4-3. Power Distribution Backplane Layout Diagram

Table 4-9. Power Distribution Backplane Connector Description

Connector	Description
J1	Power Supply #1 Power Connector
J2	Power Supply #1 Signal Connector
J3	Power Supply #2 Power Connector
J4	Power Supply #2 Signal Connector
J5	Power Supply #3 Power Connector
J6	Power Supply #3 Signal Connector
J7	Peripheral Bay Power Connector
J8	Power Supply #4 Signal Connector
J9	Power Supply #4 Power Connector #1
J10	Power Supply #4 Power Connector #2
J11	A450NX Interconnect Signal Connector
J12	A450NX Interconnect Power Connector #1
J13	A450NX Interconnect Power Connector #2
J14	A450NX Interconnect Power Connector #3
J15	Hot-Swap SCSI Backplane Signal Connector
J16	Hot-Swap SCSI Backplane 5 Volt Power Connector
J17	Hot-Swap SCSI Backplane 12 Volt, Fan Power Connector

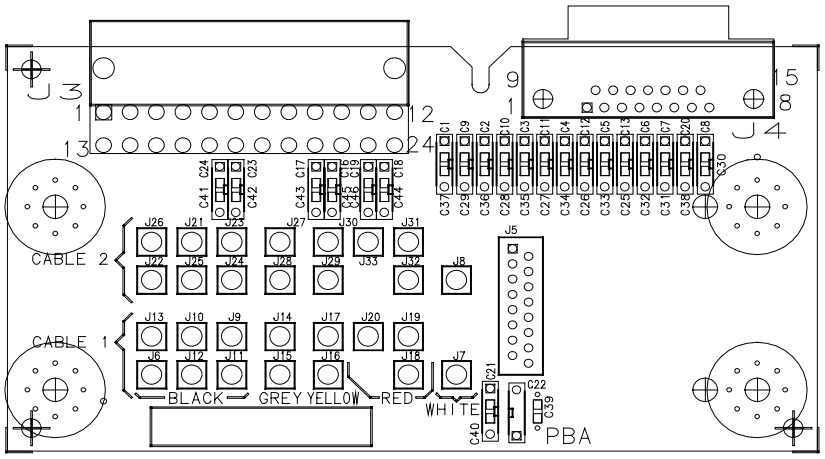


Figure 4-4. Redundant Power Distribution Board Layout Diagram

Table 4-10. Redundant Power Distribution Board Connector Description

Connector	Description
J3	Redundant Power Supply Power Connector
J4	Redundant Power Supply Signal Connector
J5	Redundant Power Dist to Power Dist Board Signal Connector
J6-J7, J9-J20	Wire to board connectors for cable set 1/P1
J8, J21-J33	Wire to board connectors for cable set 2/P2
Cable1/P1†	Redundant Power Dist to Power Dist Backplane Power Connector #1
Cable2/P2†	Redundant Power Dist to Power Dist Backplane Power Connector #2

† Cable sets 1 and 2 have one end soldered onto the redundant power distribution board via wire to board connectors. The other end of cable sets 1 and 2 form connectors P1 and P2 respectively. Connectors P1 and P2 are not shown in Figure 4-4.

4.2.1 Voltages Provided

The power distribution backplane is designed to deliver maximum current for all supplied voltages as described in the *System Power Supply* chapter of this document. However, current to the hot-swap bay user-access area is limited as shown in Table 4-11.

Table 4-11. 240 VA Maximum Load and Voltages

Voltage	Destination	Maximum Current
+12 240 VA	AD450NX hot-swap backplane	34.5 amps
+5 240 VA	AD450NX hot-swap backplane	22 amps

4.2.2 Redundant Power Supply

The AD450NX server system is designed to operate with a **minimum** of three power supplies. A fourth supply may be added as a redundant option. If any one supply fails, it will shut down and the other three will continue to operate. The system can continue operating normally while a failed supply is being replaced.

A system operating with only three power supplies is not considered to be redundant, and may fail if one power supply fails. The redundant power supply is also hot swappable.

4.2.3 240 VA Protection

For safety reasons, exposed power circuits must be limited to 240 VA. Because drive power is exposed on the hot-swap backplane, sources of 240 VA limited +5 V and +12 V are required. 240 VA protection is provided by sensing the current and shutting off the system power, if the 240 VA setpoint is exeeded. In the case of 240 VA shutdown, all DC voltages except the 5 V standby and VBIAS are shut down. They remain down until AC power is removed from and then reapplied to the system.

4.2.4 Two Speed Fan Voltage

To minimize acoustic noise, the fan voltage for all system fans has a low setting (10.2 V) during normal operational conditions. When a fan failure is sensed, the fan speed will be set to high (13 V) to increase fan speed to accomidate for the failed fan. Fan failure is not simply determined by if the fan is rotating or not, rather it is determined by monitoring the actual rotational fan speed. The microcontrollors on the SCSI hot-swap backplane monitor each fan's tachometer in order to determine if it is operating below the predetermined speed threshold. If any single system fan is determined to be operating below this threshold, a fan failure signal is asserted and the fan voltage will be set to high.

The fan voltage is derived via a boost converter from the 240 VA limited 5 V.

4.2.5 A450NX Interconnect Cable Detect

In order to prevent operating the system with interconnect power cables disconnected, a circuit is included that senses the -12 V on two of the cables. The third cable supplies -12 V to the A450NX I/O interconnect backplane. On the interconnect backplane, the -12 V is simply looped back to the other two cables. If one cable sense is high, that cable is missing. If both are high, at least two of the three A450NX interconnect power cables are missing. If both cable sense lines are asserted low, all three cables are installed. The cables can be sensed only after power is applied. Cable detects are monitored through the private I^2C bus by server management firmware.

4.2.6 Fourth Power Supply Cables Good Detect

The fourth power supply connects to the redundant power supply board. The main power distribution backplane and the redundant power supply board are connected to each other through two power cables and one signal cable. If the system was powered up missing a cable, the other cables, the backplane, or the power supply could be damaged. If all three cables are not correctly connected, the detect circuit prevents power on of the fourth power supply.

A cable detect signal is daisy chained through the fourth power supply cable; any missing cable will break the chain, causing the cable detect signal to be deasserted. The cable detect signal is monitored through the front panel controller's private I^2C bus.

The fourth power supply does not have to be present for cable detect circuitry to work. In systems with no redundant power distribution assembly, the cable detect will always be deasserted.

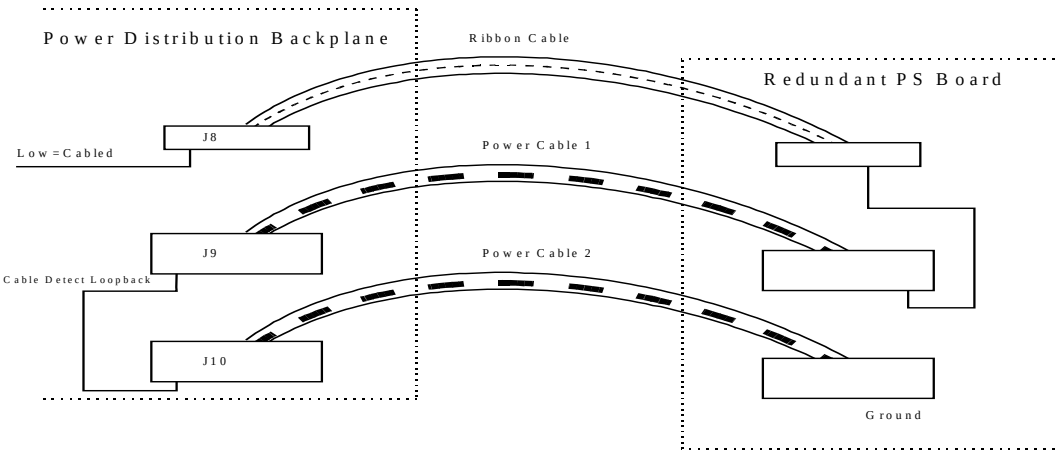


Figure 4-5. Redundant Power Supply Cable Detect Daisy Chain

4.2.7 Power Supply Revision Detect

Future processor upgrades and higher speed disk drives could exceed the power capabilities of the 420 W power supplies. Power supply revision detect circuitry determines the presence or absence of any 420 W power supply. This signal is monitored with server management firmware via I^2C.

4.2.8 Power Good

This signal provides an indication to the FPC that the system has successfully powered up and the system power is stable. System Reset is also based on Power Good.

4.2.9 Power On

The power supplies are powered on if power_on is asserted from the front panel, and there is no 240 VA shutdown condition. The fourth supply will power up only if all three cables that interconnect the power distribution backplane and the redunant power supply board are detected.

4.2.10 I^2C Accessed Features

The I^2C bus on the power distribution backplane is part of the front panel controller's private I^2C bus and is used for monitoring failures. Table 4-12 lists the I^2C inputs and outputs.

Table 4-12. I^2C Inputs and Outputs

I^2C Signal	Base Address	Port Offset	Description
SUP1_Fault	0x40/41	0	HIGH=Supply 1 Faulted
SUP1_Present_L	0x40/41	1	LOW=Supply 1 Present
SUP2_Fault	0x40/41	2	HIGH=Supply 2 Faulted
SUP2_Present_L	0x40/41	3	LOW=Supply 2 Present
SUP3_Fault	0x40/41	4	HIGH=Supply 3 Faulted

I²C Signal	Base Address	Port Offset	Description
SUP3_Present_L	0x40/41	5	LOW=Supply 3 Present
SUP4_Fault	0x40/41	6	HIGH=Supply 4 Faulted
SUP4_Present_L	0x40/41	7	LOW=Supply 4 Present
F16 Cable1_Sense_L	0x42/43	0	LOW=At least 2 cabled
F16 Cable2_Sense_L	0x42/43	1	LOW=At least 2 cabled
Supply4_Cabled_L	0x42/43	2	LOW=Supply 4 fully cabled
SPARE	0x42/43	3	Not Used
SPARE	0x42/43	4	Not Used
PS_REV	0x42/43	5	LOW=420 Watt Supplies
Margin_En_L	0x42/43	6	LOW=Enable Voltage Margin
High_Low_Sel	0x42/43	7	HIGH=High Margin, LOW=Low Margin
FRU EEPROM	0xA2/A3	0-7	256KBx1 Serial EEPROM

The FPC private I^2C bus is powered by standby voltage. It is, therefore, available even when the system power is off.

The power distribution backplane holds a 256-byte FRU SEEPROM device that resides on the private I^2C bus of the FPC. This device, an Atmel 24C02, is accessed by the front panel controller. The 24C02 device is accessible at the addresses shown in Table 4-13.

Table 4-13. Power Distribution Backplane I^2C Address Map

Device	Function	I^2C Address
24C02	Power Distribution Backplane FRU Information	A2h, A3h

The 24C02, when accessed via the I^2C bus, will provide the FRU information found in Table 4-15. The FRU information is read and made available by Intel Server Control.

The 24C02 SEEPROM has 256 bytes of programmable space that is broken into four areas. Table 4-14 presents the programmable areas, a description of each area, and the space allocated to each area.

Table 4-14. 24C02 SEEPROM Programming Areas

Area	Size	Description
Common Header	8 Bytes	Programming offsets to the other areas below.
Internal Use	48 Bytes	This area is reserved for general purpose use by the Intel® Server Management Firmware/Controllers.
Board Info	80 Bytes	Contains the board FRU information listed in Table 4-15.
Product Info	120 Bytes	Available for OEM use†

† The *FRU & SDR Load Utility* can read and modify the contents of the SEEPROM.

Table 4-15 lists the board specific FRU information that will be programmed into the board information area.

Table 4-15. FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. Date/Time	Time & date of board manufacture (value programmed [in hex] is the number of minutes after 0:00 hrs 1/1/96)	000f593h (date & time translation is shown below) f593h = 62867 min = 43 Days & 947 min = Sep 12, 1997, 3:47pm	2
Manufacturer	Board Manufacturer	Intel	1
Board Product Name	Board Name/Description	AD450NX Power Dist Backplane	1
Board Serial Number	Intel Board Serial Number	N42385906	2
Board Part Number	Intel Board Part Number	6650049-002	2

Notes: **1.** Actual value programmed into the board.
2. Example value. Actual value will vary with each board and/or fab revision.

Table 4-16 identifies the exact purpose for which bytes are allocated within the 24C02 SEEPROM. This information is useful for those who will be directly accessing the hardware for information (i.e., BIOS developers and server management software developers).

Table 4-16. Power Distribution Backplane FRU SEEPROM Byte Map

Address	Length	Description	Default Value
0x00	1	Common Header Format Version	0x01
0x01	1	Internal Use Area Offset (8-byte multiples)	0x01
0x02	1	Chassis Information Area Offset (8-byte multiples)	0x00 (area not present)
0x03	1	Board Information Area Offset (8-byte multiples)	0x07
0x04	1	Product Information Area Offset (8-byte multiples)	0x11
0x05	2	Zero Padding	
0x07	1	Common Header Checksum	0xE6
0x08	48	Internal Use Area	
0x38	1	Board Information Area Format Version	0x01
0x39	1	Board Information Area Length (8-byte multiples)	0x0A
0x3A	1	Unicode Country Base	0x00
0x3B	3	Manufacture Date/Time	
0x3E	1	Board Manufacturer Type/Length Byte	0xC5
0x3F	5	Board Manufacturer (ASCII)	‘Intel’
0x44	1	Product Name Type/Length Byte	0xDC
0x45	28	Product Name	‘AD450NX POWER DIST BACKPLANE’
0x61	1	Board Serial Number Type/Length Byte	0xCC
0x62	12	Board Serial Number	
0x6E	1	Board Part Number Type/Length Byte	0xCA
0x6F	10	Board Part Number	
0x79	1	No More Fields Flag	0xC1
0x7A	13	Zero Padding	
0x87	1	Board Information Area Checksum	
0x88	120	Product Information Area	

4.3 Wide Ultra SCSI Hot-swap Backplane

The Wide Ultra SCSI hot-swap backplane is an integral part of the AD450NX chassis system. It provides an easy, cost effective power on (hot swap) drive replacement.

The SCSI hot-swap backplane has a capacity for 12 hard disk drives arranged in two rows of six. Each row is on a separate SCSI channel, and has space for either six 1" or 1.6" high by 3.5-inch wide SCA SCSI hard disk drives. The connectors on the backplane are SCA-2 PressFit* connectors. The backplane supports hot swapping of SCA style drives in and out of the hot-swap bays, when the drives are mounted in hot-swap drive carriers. The LEDs on the backplane indicate drive present (power), drive activity, and drive fault. Light pipes transmit the light from the LEDs to the front bezel.

The backplane also provides easy RAID integration over a wide range of RAID controller products. The single feature that simplifies RAID integration is the addition of an onboard SCSI target whose command set allows vendor independent controller management and monitoring for associated drive functions such as drive insertion and removal, light indicators, and drive power control. Its use simplifies cable management and eliminates errors caused by the possibility of incorrect correlation of several cables.

Since operator accessibility to each power bus is required with the system energized, a 240 VA protection scheme is implemented for each power bus in the backplane.

The SCSI hot-swap backplane performs the tasks associated with hot-swapping SCSI drives and enclosure (chassis) monitoring and management as specified in the *SAF-TE Specification*. The hot-swap backplane supports the following capabilities:

- Dual channels (six drives on each channel) twelve 1-inch or 1.6-inch Wide Ultra SCSI (16 bit) drives
- Single connector attachment (SCA-2) connectors to simplify insertion and removal of hard disk drives
- Insertion and removal of hard drives during power ON (hot swap)
- Hard wired SCSI IDs for each SCA connector
- LED indicators for each drive
- Switched field effect transistor (FET) power control for each hard drive
- FET short circuit protection
- Microcontroller to monitor enclosure services
- I^2C bus for management information
- Ease of RAID integration
- Flash memory for upgrading firmware
- Temperature sensing
- Hard drive bay intrusion warning
- SCSI Accessed Fault Tolerant Enclosures (SAF-TE)
- SCSI-3 (Ultra SCSI) and SCSI-2 support
- Fan speed monitoring and control

Figure 4-6 and Figure 4-7 show the component placement on the primary and secondary sides of the Wide Ultra SCSI hot-swap backplane. The SCA connectors for the hard disk drives are on the secondary side (hot-swap drive bay side) of the SCSI hot-swap backplane. The SCSI backplane has many cutouts (holes) to allow increased airflow and cooling of the hard drives.

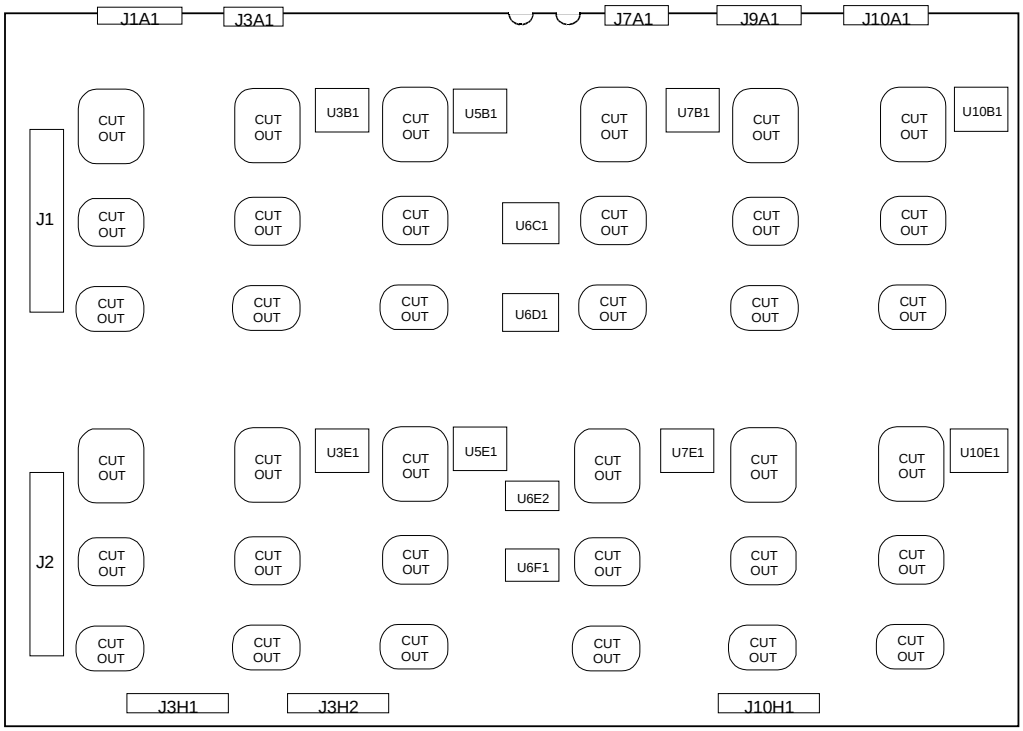


Figure 4-6. Wide Ultra SCSI Backplane Primary-side Placement

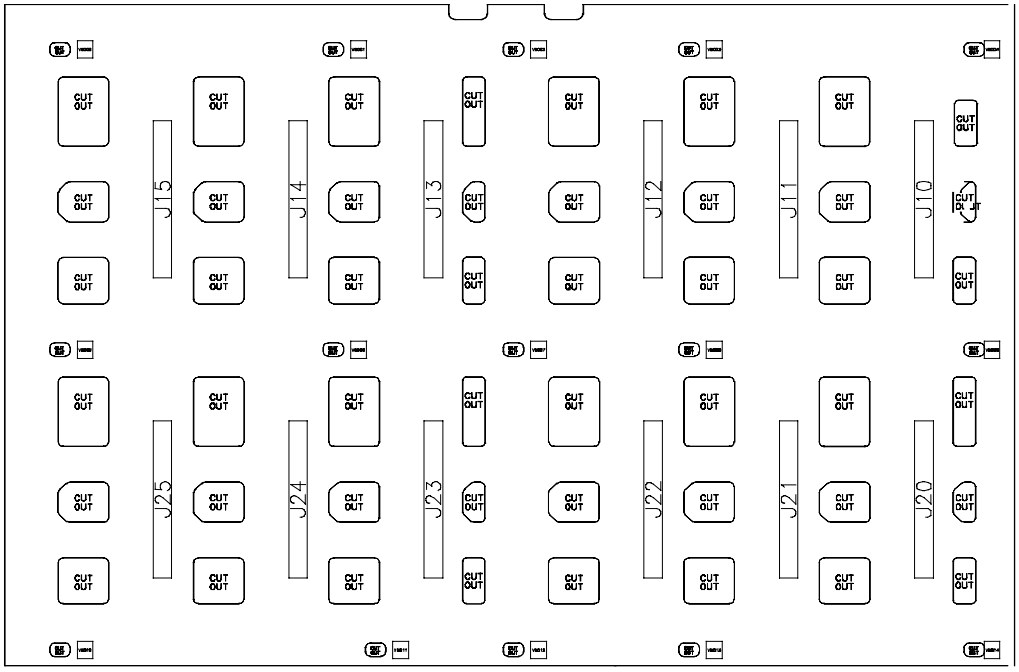


Figure 4-7. Wide Ultra SCSI Backplane Secondary-side Placement

Table 4-17. Wide Ultra SCSI Backplane Reference Designators

Component	Description	Location
J1	Primary channel connector	Primary side
J2	Secondary channel connector	Primary side
J10-J15	Hot-swap SCA connectors on primary channel	Secondary side
J20-J25	Hot-swap SCA connectors on secondary channel	Secondary side
J3H1, J10H1	Connectors for power cables from power distribution backplane	Primary side
J3H2	Connector for signal cable from power distribution backplane for BMC/FPC signals	Primary side
J1A1	Connector for I/O baseboard area fans cable	Primary side
J9A1, J10A1	Connectors for CPU baseboard are fans cables	Primary side
J2A1	Connector for 51/4" peripheral bay power cable	Primary side
J7A1	Connector for drive-bay intrusion switch cable	Primary side
J3A1	Connector for logic device programming	Primary side

4.3.1 SCSI ID

Each SCA connector has a fixed SCSI ID as described in Table 4-18. In addition, the SCSI controller on each channel is defined as ID 6. There are no jumpers on the backplane for the configuration of the SCSI IDs.

Table 4-18. SCSI IDs

Primary Channel		Secondary Channel	
SCSI ID	SCA connector	SCSI ID	SCA connector
ID0	J10	ID0	J20
ID1	J11	ID1	J21
ID2	J12	ID2	J22
ID3	J13	ID3	J23
ID4	J14	ID4	J24
ID5	J15	ID5	J25
ID6	SCSI controller	ID6	SCSI controller

4.3.2 Hot-swap Controller (HSC)

A Phillips 80C652 microcontroller on each SCSI channel provides the SCSI controller functions. It has a built-in I^2C interface and provides all of the intelligence for the Wide Ultra SCSI hot-swap backplane. Each HSC uses its own Flash for program code storage and static RAM for program variables and buffers.

4.3.3 Hot-swap Connectors

The Wide Ultra SCSI hot-swap backplane provides 12 hot-swap SCA-2 PressFit connectors, AMP 787900-1*, for inserting SCSI hard disk drives. Each connector provides power and SCSI signals to each drive.

4.3.4 SCSI Interface

There are two independent SCSI channels on the hot-swap backplane. The SCSI interface on the backplane provides the required additional circuitry between the SCSI bus and the microcontroller that contains the intelligence for the backplane. This allows the microcontroller to respond as a SCSI target. The interface is implemented using the Symbios 53C80S* SCSI interface chip. The SCSI controller is set to SCSI ID 6.

4.3.5 SCSI Active Termination

The SCSI active terminators provide SCSI-3 compliant termination for the backplane-end of the SCSI bus. It is required that the other end of the SCSI segment is properly terminated by the add-in SCSI controller, as required by the SCSI-3 specification.

4.3.6 Power Control

Power control on the Wide Ultra SCSI hot-swap backplane supports the features described below.

- Spin-down of a drive when failure is detected and reported (using enclosure services messages) via the SCSI bus. If an application or RAID controller detects a drive related problem that indicates a data risk, it takes the drive out of service and sends a spin-down SCSI command to the drive. This decreases the likelihood of drive damage during removal from the hot-swap drive bay. When a new drive is inserted, the power control waits a small amount of time for the drive to be fully seated, and then applies power to the drive in preparation for operation.
- If system power is on, the backplane immediately powers off a drive slot when it detects removal of a drive. This prevents possible damage to the drive when it is partially removed and reinserted, while full power is available. It also prevents disruption of the entire SCSI array from possible sags in supply voltage and the resultant current spikes.

4.3.7 FET Short Circuit Protection

The field effect transistor (FET) short circuit protection circuitry protects both 12 V and 5 V power control FETs located on theWide Ultra SCSI hot-swap backplane. This protection prevents damage to the FET circuitry if there is a power fault on a drive plugged into one of the slots.

4.3.8 Drive Status LED

Each SCSI drive has three drive indicators that are visible on the outside of the front bezel. The LEDs are located on the SCSI backplane and a series of light pipes directs the light to the front panel. The arrangement of these LEDs is shown in Figure 4-8.

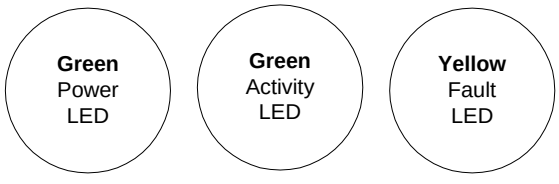


Figure 4-8. LED Drive Indicators

4.3.8.1 Power LED

The green power LED indicates that the drive is receiving power. The power LED control is driven by the FET switched +5 V applied to the drive.

4.3.8.2 Drive Activity LED

The green activity LED indicates that the drive is being accessed. Drive activity LED is driven by drive pin 77, which interfaces directly to the LED.

4.3.8.3 Fault LED

The yellow drive fault LED indicates the failure status for the drive. The hot-swap controller is responsible for turning the drive fault LED on or off according to the states specified by commands received via the IPMB Set Fault Light and SAF-TE. The LED is physically located on the Wide Ultra SCSI backplane and is driven from the backplane.

The fault LED blinks fast during an attempt to rebuild on empty slot or if a rebuild is interrupted.

The slow blinking fault LED indicates a predicted fault or rebuilding process. A steady ON fault LED indicates a faulty drive.

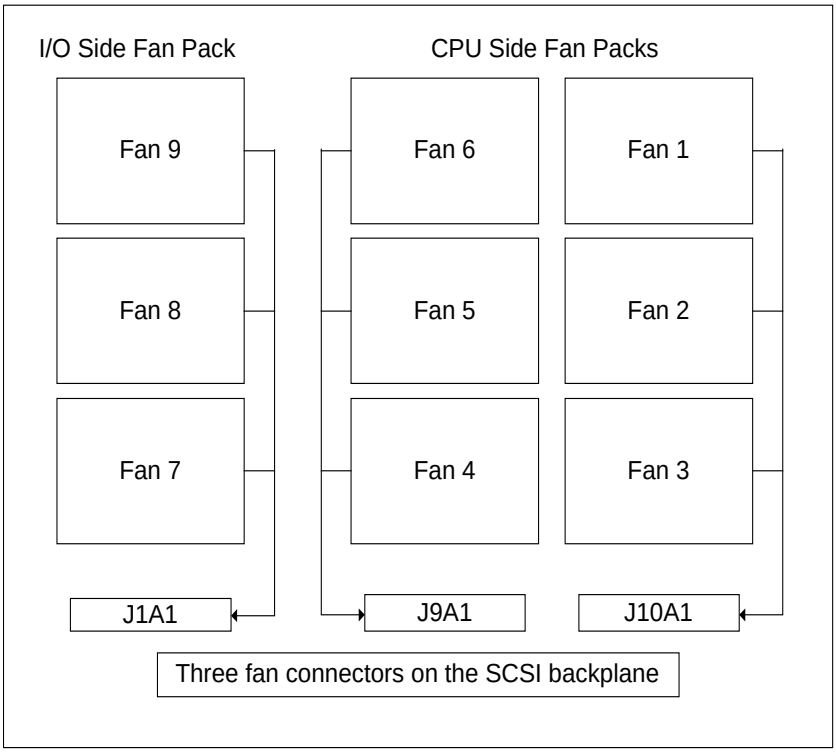
4.3.9 Cooling Fans

The Wide Ultra SCSI backplane supports nine system fans with a digital-output tachometer that is used by the microcontroller to assess the operating condition of the fans before total failure. The digital outputs of the fans are connected via two multiplexors to the input of each microcontroller. Six fans from the memory and CPU complex are connected to the primary microcontroller, and three fans from the I/O baseboard area are connected to the secondary microcontroller. Microcontroller program code is responsible for monitoring fan speed and reporting the condition of the fan via the IPMB bus.

Normally, fans in CPU baseboard and I/O baseboard areas run at 2560 RPM on nominal voltage (RPMs can vary by +-12%). The speed of the fans are sensed by the HSC and compared against a low speed threshold of 2176 RPM (15% below the nominal voltage RPM). The HSC issues a message on the IPMB when any one fan falls below this threshold. The BMC, on receiving this message, turns the fan fail LED to an ON state on the front panel. The message includes the number of the failed fan, which can be interpreted by server management software. It also asserts a signal to the power distribution board that causes the supply voltage for the fans to increase from nominal voltage of 10.2 V to 13 V, resulting in a speed-up of all remaining 8 fans to 2944 RPM (15% above the nominal voltage RPM).

Once a fan has failed, it should be replaced. The HSC will not take any action except that of reporting the second failure. The server management software can be configured to setup a number of alarms for multiple fan failures.

Figure 4-9 shows the chassis fan layout viewed from the rear side of the chassis. It also shows how the fans are numbered and how they are connected to the three fan connectors on the SCSI backplane.



Note: Fan layout as seen from the rear of the chasssis.

Figure 4-9. Chassis Fan Layout

4.3.10 Temperature Sensor

A Dallas DS1621* temperature sensor device is electrically connected to each HSC on its private I^2C bus. This device is used to monitor the drive bay temperature. The temperature may be read via SAF-TE and IPMB commands. In addition, setable temperature thresholds are provided via IPMB commands. The HSC is configured to issue an event message on the IPMB when the temperature threshold is crossed.

4.3.11 Power Supply Status

The HSC queries front panel controller for the status of power supplies via IPMB using the Get Power Supply Status command. The number of installed power supplies reported are used to update SAF-TE data. The status of the installed power supplies can be read via the SAF-TE Read Enclosure Status command. The power supply status is reported per the status field definitions in the *SAF-TE Specifications*.

4.3.12 Chassis Intrusion Signal

Two pass-through intrusion switches located on the chasiss drive bay doors are electrically connected to the SCSI backplane. These switches are used to indicate that the drive bay is being accessed when the front door is opened. Typically, both switches are closed. When an intrusion switch is opened by opening one of drive bay doors, it enables a chassis intrusion signal to indicate that the drive bays are being accessed.

The FPC monitors the state of the chassis intrusion signal. If event logging is enabled in the BIOS setup, the FPC generates a "Chassis Intrusion" event message when a drive bay intrusion occurs.

4.3.13 I²C Accessed Features

The primary HSC on the Wide Ultra SCSI backplane holds a 256-byte SEEPROM device on its private I²C bus.

This SEEPROM, an Atmel 24C02, is accessed via the HSC and is used to hold the serial number, part number, and other FRU inventory information, as well as miscellaneous application code about the Wide Ultra SCSI hot-swap backplane, which is used by the firmware. The 24C02 device on the primary HSC is accessible at the addresses show in Table 4-19.

Table 4-19. Wide Ultra SCSI Backplane I²C Address Map

Device	Function	I²C Address
Atmel 24C02*	SCSI Hot-swap backplane FRU information	A0h, A1h

The 24C02 SEEPROM, when accessed via the I²C bus, provides the FRU information found in Table 4-21.

The 24C02 SEEPROM has 256 bytes of programmable space, which is broken into four areas. Table 4-20 is a list of the programmable areas, a description of each area, and the space allocated to each area.

Table 4-20. 24C02 SEEPROM Programming Areas

Area	Size	Description
Common header	8 Bytes	Programming offsets to the other areas below.
Internal use	48 Bytes	This area is reserved for general purpose use by the Intel® server management firmware/controllers.
Board info	80 Bytes	Contains the board FRU information listed in Table 4-21.
Product info	120 Bytes	Available for OEM use. †

† An Intel provided utility, called the *FRU & SDR Load Utility,* allows the OEM to program any of the FRU SEEPROMs in the chassis.

Table 4-21 lists the board specific FRU information that will be programmed onto the board information area.

Table 4-21. FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. Date/Time	Time & date of board manufacture (value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/96)	000f593h (date & time translation shown below) f593h = 62867 min = 43 Days & 947 min = Feb 12, 1996, 3:47pm	2
Manufacturer	Board Manufacturer	Intel	1
Board Product Name	Board Name/Description	AD450NX Ultra SCSI Backplane	1
Board Serial Number	Intel Board Serial Number	N42385906	2
Board Part Number	Intel Board Part Number	6650049-002	2

Notes: **1.** Actual value programmed into the board.
2. Example value. Actual value will vary with each board and/or fab revision.

Table 4-22 identifies the exact purpose for which bytes are allocated within the 24C02 SEEPROM. This information is useful for those who will be directly accessing the hardware for information (i.e., BIOS developers and server management software developers).

Table 4-22. SCSI Backplan FRU SEEPROM Byte Map

Address	Length	Description	Default Value
0x00	1	Common Header Format Version	0x01
0x01	1	Internal Use Area Offset (8-byte multiples)	0x01
0x02	1	Chassis Information Area Offset (8-byte multiples)	0x00 (area not present)
0x03	1	Board Information Area Offset (8-byte multiples)	0x07
0x04	1	Product Information Area Offset (8-byte multiples)	0x11
0x05	2	Zero Padding	
0x07	1	Common Header Checksum	0xE6
0x08	48	Internal Use Area	
0x38	1	Board Information Area Format Version	0x01
0x39	1	Board Information Area Length (8-byte multiples)	0x0A
0x3A	1	Unicode Country Base	0x00
0x3B	3	Manufacture Date/Time	
0x3E	1	Board Manufacturer Type/Length Byte	0xC5
0x3F	5	Board Manufacturer (ASCII)	‘Intel’
0x44	1	Product Name Type/Length Byte	0xDC
0x45	28	Product Name	‘AD450NX Ultra SCSI Backplane’
0x61	1	Board Serial Number Type/Length Byte	0xCC
0x62	12	Board Serial Number	
0x6E	1	Board Part Number Type/Length Byte	0xCA
0x6F	10	Board Part Number	
0x79	1	No More Fields Flag	0xC1
0x7A	13	Zero Padding	
0x87	1	Board Information Area Checksum	
0x88	120	Product Information Area	

5. System Power Supply

The 420W active power factor corrected switching power supply used in the AD450NX server system has six outputs, AC to DC, +5.05 Vdc at 32 A, +3.3 Vdc at 15 A, +12 Vdc at 16 A with 20 A/10 sec peak current, and -12 Vdc at 1 A. There are Vbias (+16 to +20 Vdc) at 50 mA and a Vstby (+5 V) at 0.1 A outputs that are always on.

The power supply will be in a redundant/nonredundant power supply system with the possible configurations shown in Table 5-1. The system has redundant power only if four power supplies are installed in the system. Each power supply has an isolating device on each output so that the failure of one power supply does not affect the operation of the others. The power supply has active forced load sharing on the +5.05 Vdc, +3.3 Vdc, and +12 Vdc outputs. Each power supply is docked into the power distribution backplane, which provides connections for the DC outputs and alarm/control functions. The AC input is provided through a line cord plugged into the system-accessible-side of each power supply.

Table 5-1. System Configuration

Standard High End System (nonredundant)	Three Power Supplies
Redundant System (N+1 redundant)	Four Power Supplies

Figure 5-1 shows the 420 W power supply enclosure used in the AD450NX server system. The dimensions of the power supply are: 5 inches wide x 7 inches high x 9 inches deep.

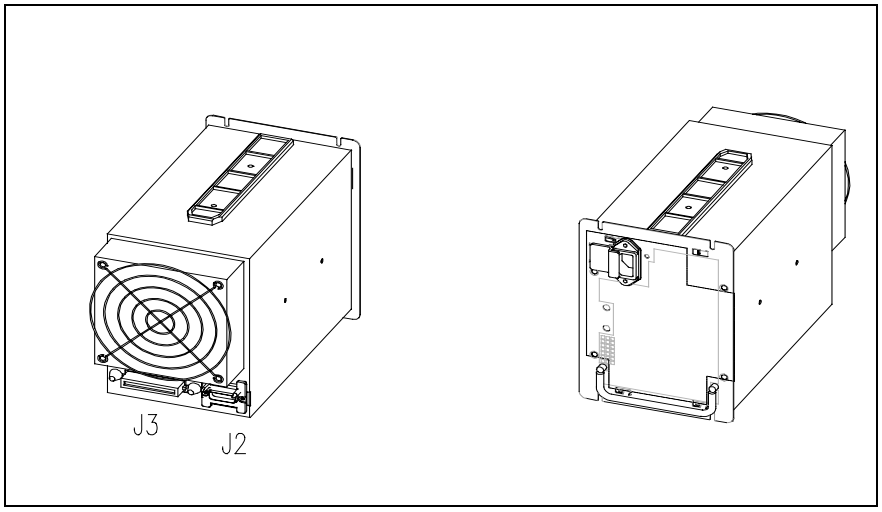


Figure 5-1. Power Supply Enclosure

The power supply has a minimum efficiency of 60% at all rated voltages and frequencies as specified in the *AC Input Specification* section of this chapter.

The power supply incorporates a universal power input with active power factor correction that reduces line harmonics in accordance with EN61000-3-2 standards.

5.1 AC Input Specification

The input voltage ranges specified in AC volts RMS are 100 to 120 VAC, and 200 to 240 VAC. These ratings are marked on the power supply labels. The power supply operates properly with as much as 10% harmonic distortion on the input AC voltage.

Table 5-2. AC Input Voltage

PARAMETER	MIN	NOM	MAX	UNITS
Vin (115)	90	100-120	132	Vrms
Vin (230)	180	200-240	264	Vrms
Vin Frequency	47	50/60	63	Hz

5.1.1 DC Output Voltage Specification

The power supply has the following DC outputs: +5.05 Vdc , +12 Vdc , +3.3 Vdc, -12 Vdc, +5.0 Vdc standby and Vbias. All DC outputs have an isolating device. The Vbias voltage is a diode-isolated output, (+16 to +20 Vdc) which is used to power up the circuits on the power supply distribution backplane. As with the +5 Vstby output, the Vbais output is present when the other outputs are disabled. All output grounds connect to the power supply chassis and to earth ground through the AC line cord.

5.1.2 DC Load Range Table (System Power)

The Table 5-3 specifies the current needed for four sample load ranges. For each load range, the number of power supplies needed to support that range is specified.

Table 5-3. DC Load Range Table

Load Range	+3.3 Vdc		+5.05 Vdc		+12 Vdc			-12 Vdc		+5 Vstby		Units	Number of power supplies in system
	min	max	min	max	min	max	peak	min	max	min	max		
#1	3.5	15.0	5.0	89.5	5.0	45.0	50.0	0.0	1.0	0.0	0.1	A	3 or 4
#2	3.5	28.5	32.0	89.5	5.0	45.0	50.0	0.0	1.0	0.0	0.1	A	3 or 4
#3	3.5	42.0	42.0	89.5	5.0	45.0	50.0	0.0	1.0	0.0	0.1	A	3 or 4
#4	3.5	42.0	5.0	89.5	0.2	45.0	50.0	0.0	1.0	0.0	0.36	A	3 or 4

Notes:

1. The sum of all +3.3 V loads must not exceed 42 A with 3 or 4 420 W supplies.
2. The sum of all +5 V loads must not exceed 89.5 A with 3 or 4 420 W supplies.
3. The sum of all +12 V loads must not exceed 45 A with 3 or 4 420 W supplies.

5.1.3 DC Output Maximum Load Rating

Using the worst case load share error specified in the *Forced Load Sharing* section, the maximum loads supplied by each power supply are shown in Table 5-4. These loads are extrapolated from the worst case conditions discussed in the section called *DC Load Range Table (System Power)* in this chapter.

Table 5-4. DC Output Maximum Rating

+5.05 Vdc	+12 Vdc	+12 Vdc peak (10 sec)	+3.3 Vdc	-12 Vdc	+5 Vstby	Vbias (+16 - +20 Vdc)
32 A max	16A max	20 A max	15 A max	1 A max	100 mA max	50 mA max

Note: The maximum DC output rating for combined 3 or 4 420 W power supplies is described in Table 5-3.

5.1.4 DC Output Minimum Load Rating

The minimum loading requirements on each power supply output are shown in Table 5-5. These values are extrapolated from the *DC Load Range Table (System Power)* section in this chapter.

Table 5-5. DC Output Minimum Load Rating

+5.05 Vdc	+12 Vdc	+3.3 Vdc	-12 Vdc	+5 Vstby	Vbias
3 A	1 A	1 A	0 A	0 A	0 A

5.1.5 Temperature Range

Table 5-6. Temperature Range

Operating Temp	0 to 50 °C
Storage Temp	-40 to +70 °C

5.1.6 Over-voltage Protection

An over-voltage condition is sensed on the 3.3 Vdc, 12 Vdc, and 5.05 Vdc outputs of each power supply and shut down the power supply per the following settings. The maximum values shown are voltages measured on the outputs of the power supply. The maximum OVP delay is the time between output maximum and the power supply shut down. The power supply shuts down and latches off within the time specified in Table 5-7. To turn the power supply on again, the AC input must be cycled off and then on.

Table 5-7. Over-voltage Protection Settings

Output	Max	Units	Max OVP Delay (μsec)
+5.05	6.50	volts	100
+12	15.00	volts	100
+3.3	4.50	volts	100

5.1.7 Over-current/Short Circuit Protection

Over-current protection exists on the +5.05 Vdc, +12 Vdc, and +3.3 Vdc outputs. This limits the output current of the power supply and shuts down the power supply. It does not limit the outputs to under 240 VA. All 240 VA current protection is done on the power supply backplane. The set points are greater than the maximum output currents for the +5 Vdc and +3.3 Vdc outputs and greater than the peak current for the +12 Vdc output. The power supply operates within current limit without damaging the power supply.

The -12 Vdc output is sensed for a short circuit condition. For short circuit protection the power supply shuts down and latches out all the outputs except the +5 Vdc stby and the Vbias. To turn the power supply on again, the AC line must be cycled off and then on.

5.2 Control Signals

5.2.1 Remote Sensing

There is a (+/-) remote sensing on the +5.05 Vdc, +12 Vdc and +3.3 Vdc outputs. The -12 Vdc, -5 Vdc, and +5 Vstby outputs are referenced to the (-) remote sense point. The loss of a remote sense connection does not cause the power supply to go into a high output voltage condition.

5.2.2 Forced Load Sharing

The +5.05 Vdc, +12 Vdc and +3.3 Vdc outputs have forced load sharing. The outputs share within 10% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating.

5.2.3 Power Good Signal

Each power supply provides a power good (PGOOD) signal. This signal indicates that all outputs have reached operating state.

5.2.4 Power Supply Failure (FAULT)

Each power supply provides an indicator for power supply failure. This sends a signal to the system indicating power supply failure. The needed logic levels of the power supply failure signal are shown in Table 5-8.

Table 5-8. Fault Signal

FAULT SIGNAL	VOLTAGE / TTL LEVEL	CURRENT
LOW STATE NO FAULT	0.4 V max	while sinking 4 mA
HIGH STATE FAULT	3.50 V min 5.25 V max	with a 100KΩ pull-up to +5 Vstby (pull-up is on the distribution backplane)

5.2.5 LED Indicators

A green POWER SUPPLY OK LED indicates that the power supply has not failed. A green CURRENT OK LED indicates the power supply is not current limited. The LEDs are placed on the power supply surface exterior to the system.

The LEDs are marked as shown in the section *LED Marking*. Table 5-9 specifies the conditions of the LEDs.

Table 5-9. LED Indicators

Power Supply Condition	Power Supply (green LED)	Current (green LED)
Marking	PS	I
Power supply ON and OK	ON	ON
Power supply failure	OFF	ON or OFF
Current limit	ON	OFF
Power supply disabled with the PON	ON	ON

5.2.6 Power Supply (DETECT) Signal

This signal is used to sense the number of power supplies in the system (operational or not). The DETECT signal on the power supply (pin 12 of J2) is connected to power ground or the output ground of the power supply. With no power supply plugged into the backplane, the DETECT signal is pulled up through a pull-up resistor to +5 Vstby on the backplane.

5.2.7 Power Supply Fan Requirements

The power supply incorporates a 120-mm fan to exhaust air. The fan circuitry implements *variable speed fan control* and fan failure detection. Temperature is detected at the power supply inlet.

The fan voltage ramps from 9 V at 32°C to 12 V at 42°C.

At temperatures below 32°C: 8 V ≤ fan voltage ≤ 9 V

At temperatures above 42°C: 12 V ≤ fan voltage ≤ 13 V

5.2.8 DC Power Enable/Disable (PON)

The DC Output Enable circuit is Safe Extra Low Voltage (SELV). This circuit enables or disables the +5.05 Vdc, +12 Vdc, +3.3 Vdc and -12 Vdc outputs only. The +5 Vstby and Vbias outputs are unaffected by this signal.

Table 5-10. DC Power Enable (PON) Signal Description

PON SIGNAL / VIN	VOLTAGE	CURRENT
HIGH, PWR SUPPLY ENABLED	4 V min	0.5 mA min
LOW, PWR SUPPLY DISABLED	2 V max or open circuit	

5.2.9 Indicator Status Table

The determination of a power supply failure is achieved by detecting several states of the power supply as described in Table 5-11.

Table 5-11. Power Supply Status

POWER SUPPLY STATE	SHUTDOWN POWER SUPPLY (not +5 Vstby or Vbias)	FAILURE SIGNAL	PGOOD SIGNAL	PS OK (GREEN LED)	I OK (GREEN LED)
Power supply operational and enabled (PON=on)	NO	LOW	HIGH	ON	ON
Over-voltage	YES	HIGH	LOW	OFF	OFF
Fan failure	YES	HIGH	LOW	OFF	OFF
Over-temperature	YES	HIGH	LOW	OFF	OFF
General failure	NA	HIGH	LOW	OFF	OFF or ON
Current limit (+5,+12,+3.3)	YES	HIGH	LOW	ON	OFF
Short circuit protection (-12)	YES	HIGH	LOW	OFF	OFF
Power supply disabled (PON=off)	YES	LOW	LOW	ON	ON

6. Server Management Features

The AD450NX server management architecture features several management controllers, which autonomously monitor server status and provide the interface to server management control functions. The controllers intercommunicate via an I^2C-based serial bus referred to as the Intelligent Platform Management Bus (IPMB). The firmware of the server management controllers is field upgradeable using the *Server Management Firmware Update Utility*.

Figure 6-1 represents the server management architecture of the AD450NX server system. Refer to the *A450NX MP Server Board Set Technical Product Specification* for further details on board set server management functionality.

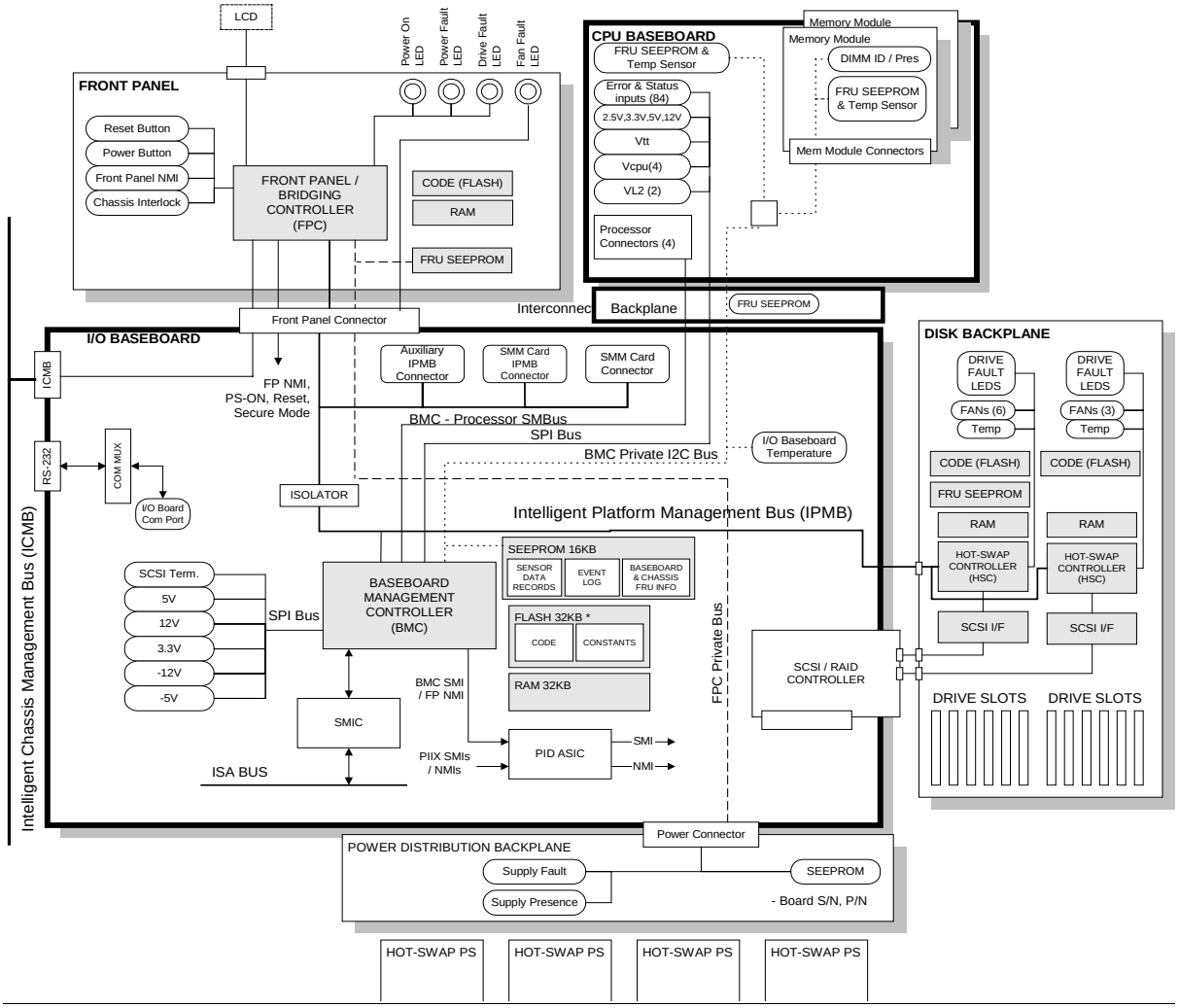


Figure 6-1. AD450NX Server Management Architecture Block Diagram

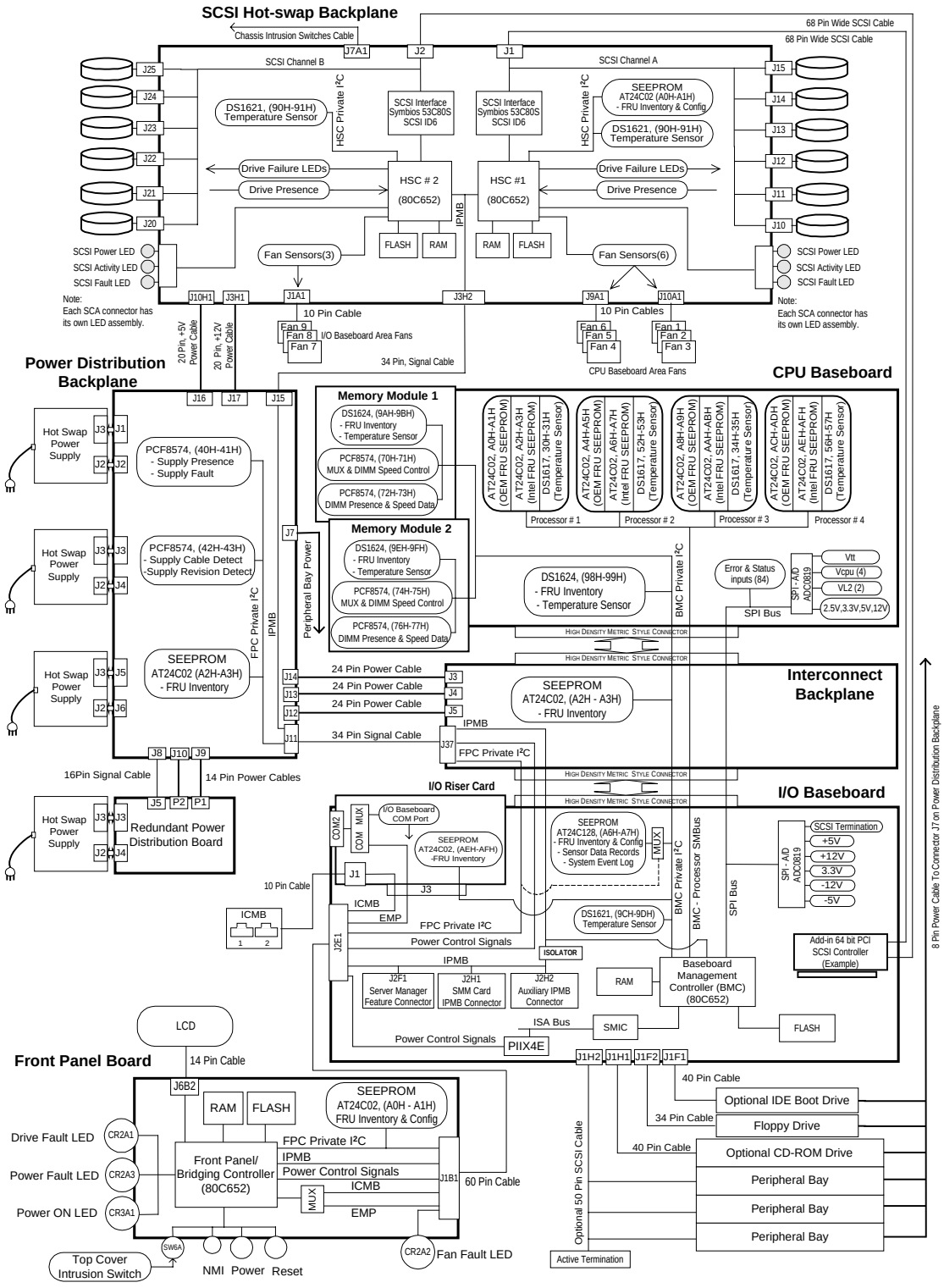


Figure 6-2. AD450NX Server Management Hardware Block Diagram

Figure 6-2 shows a detailed diagram of server management hardware on the AD450NX server system. This diagram describes the interconnection between all server management microcontrollers located on the chassis and A450NX board set. The major functions of each controller are summarized in the following sections.

6.1 Baseboard Management Controller (BMC)

The heart of AD450NX server management is the baseboard management controller (BMC). The BMC is located on the A450NX I/O baseboard. This controller provides primary server management monitoring capabilities.

The various server management functions provided by the BMC are listed below.

- Baseboard voltage and temperature monitoring
- Fan failure detection
- Fault resilient booting (FRB)
- Watchdog timer
- System event log management and access
- Sensor data record repository management and access
- POST code log
- Secure mode, video blank, and floppy write protect
- DIMM ID monitoring and presence detection

Details of the above listed features, as well as other server management features offered by the A450NX board set, are provided in the *A450NX Server Board Set Technical Product Specification*.

6.2 Front Panel Controller (FPC)

The front panel controller (FPC) on the AD450NX server system chassis front panel board manages the front panel operations. Since this controller is responsible for system power control, it is powered from the +5 V standby output of the power supply. The FPC provides the following server management capabilities:

- System power fault indication
- Front panel LCD interface
- Chassis intrusion detection and reporting
- ICMB to IPMB bridge
- EMP (COM2 redirection)
- Chassis FRU inventory

6.2.1 System Power Fault Indication

The FPC monitors the state of each power supply through its private I^2C bus. When a faulty power supply is detected, the FPC illuminates the Power Fault LED on the system's front panel. AC power must be removed from a faulty supply to clear the fault.

6.2.2 Front Panel LCD Interface

The front panel has a Stanley GMD1620A* LCD. The LCD and the corresponding LED backlighting unit are powered by the main +5 V power. Therefore, front panel LCD information is available only when the main +5 V of power is available. The display is used by the BIOS to display messages during POST. The LCD can also be used by the system management software as a status display during run-time. The display unit is controlled by the FPC and is accessed by the BIOS by sending IPMI commands to the FPC.

6.2.3 Chassis Cover Intrusion

The chassis cover intrusion switch is located on the front panel board. When the chassis top cover is removed, the intrusion switch enables the chassis intrusion signal indicating that the chassis is being accessed. The FPC monitors the state of the chassis intrusion signal from the front panel. The FPC debounces the signal and makes the status of the signal available via an IPMI command. If the event logging is enabled in the BIOS, the FPC also generates an event message when the chassis intrusion is detected. The chassis cover intrusion is logged as a "cover open" event in the SEL.

6.2.4 ICMB to IPMB Bridge

The front panel controller provides the bridging between the ICMB and the IPMB. The ICMB, with the ICMB bridge, provides a mechanism for interserver management communications. Multiple system units and peripheral chassis can be connected to the same ICMB. Through the ICMB, IPMB devices local to a server, such as the BMC, can access the local server management functions of external servers. This allows server management across multiple servers. Refer to Chapter 4 of this document for further details.

6.2.5 EMP (COM2 Redirection)

The EMP is a server management feature built directly onto the I/O riser card to provide remote server management capabilities via a modem or direct serial connection from the COM2 port. BIOS settings at the server define specific options for the hardware, such as whether the COM2 port on the server should function as a standard COM port or as an emergency management port. The EMP operates at 19.2 kB/s. The basic management features available through the EMP console are:

- System power up/down control
- System reset
- Access to the chassis FRU inventory information

6.3 Hot-swap Controller (HSC)

The dual channel AD450NX hot-swap backplane (HSBP) contains a dedicated hot-swap controller (HSC) on each channel. Each HSC is connected to other system boards via the IPMB. The HSC provides server management information through both the IPMB and the SCSI Accessed Fault-Tolerant Enclosures (SAF-TE). SAF-TE is an industry standard for communicating drive and slot status. The HSC:

- Implements the SAF-TE command set accessed through SCSI
- Provides an IPMB path for drive presence, drive fault status, backplane temperature, and fan failure
- Controls the fault lights and drive power on the AD450NX server system chassis hot-swap backplane
- Queries the power distribution backplane for power supply status
- Controls the fan supply voltage on the power distribution backplane, in case of fan failure
- Controls drive power on and off, facilitating hot swapping of drives

The SCSI backplane contains two processor complexes, each consisting of a Philips Semiconductor 8xC652* microcontroller (or equivalent), 30KB RAM, 32KB FLASH memory with 4KB boot block region, a Symbios Logic 53C80S* 8-bit SCSI interface chip, and associated support circuitry for controlling drive power, drive fault lights, etc.

The primary and secondary hot-swap controllers are responsible for the following system functions.

6.3.1 Drive Fault Light Control

The HSC is responsible for turning the drive fault lights on or off according to the states specified from commands received via SAF-TE.

6.3.2 Drive Presence Detection

The HSC detects drive presence and makes this information available via SAF-TE and the IPMB. It is the responsibility of the HSC firmware to make sure that the drive presence signals have been properly debounced.

6.3.3 Drive Power Control

The HSC firmware automatically powers up drives when they're detected as being inserted into the drive bays. Hardware on the SCSI backplane ensures that drive bays are automatically powered down when drives are removed. There are also SAF-TE and IPMB commands that allow inserted drives to be powered on and off.

6.3.4 Drive Bay Temperature Sensing

A Dallas Semiconductor DS1621* Serial Temperature Sensor device is connected to the HSC via a private I^2C bus. This device is used to monitor the drive bay temperature. The temperature of each drive bay is read via SAF-TE and IPMI commands once every two seconds. Programmable temperature thresholds are provided via IPMI commands. With this implementation, the HSC can be configured to issue an event message on the IPMB when the temperature threshold is crossed. The status for the temperature threshold crossing is also available via SAF-TE and the IPMB.

Table 6-1. Default SCSI Hot-swap Backplane Temperature Thresholds

Threshold	Upper Critical	Upper Non-Critical	Lower Critical	Lower Non-Critical
SCSI Hot-Swap Backplane	50C/122F	45C/113F	-10C/14F	0C/32F

6.3.5 Fan Sensing and Control

Fan sensing and control is under the control of the HSC. The primary HSC monitors six fans and the secondary HSC monitors three fans. The HSCs, if configured to do so in BIOS, issue an event message on the IPMB when the fan speed falls below a specified threshold. The status for the fan failure is available via both SAF-TE and the IPMB. In addition, the fans have a 'low' and 'high' speed control, which is controlled via the HSCs. Refer to the Cooling Fans section in Chapter 4 of this document for more details.

6.3.6 Power Supply Status Reporting via SAF-TE

Both the primary and secondary HSCs report the number of installed power supplies and their statuses.

6.3.7 Drive Bay Intrusion

The AD450NX server chassis contains chassis intrusion switches on each drive bay door. These switches are electrically connected to SCSI backplane. When either of the two drive bay doors is opened, the corresponding pass-through intrusion switch indicates that the drives are being accessed.

Even though the chassis intrusion switches for the drive bay doors are connected to the SCSI backplane, these sensors are monitored, via the IPMB, by the FPC. When an intrusion occurs, the FPC generates an event message that is recorded in the system event log (SEL). The drive bay intrusion is reported as a "chassis intrusion" event in the SEL.

6.4 Power Distribution Backplane

The server management features of the power distribution backplane are accessed by the FPC through the private I^2C bus. The power distribution backplane has the following features.

6.4.1 Power Supply Present and Fault

Each power supply has a present line and a fault line. These are monitored by an I^2C port on the FPC's private I^2C bus. A supply is present if its detect line is LOW. A supply is faulted if its fault line is HIGH. A fault condition causes main power from the respective supply to be turned off. AC power must be removed from a faulted supply to clear the fault.

6.4.2 Interconnect Cable Detect

In order to prevent operating the system with the interconnect backplane power cables disconnected, a circuit is included that senses the -12 V. This functionality is described in detail in Section 4.2.5.1 of this document. The cables can be sensed only after power is applied. Cable detects are monitored through the private I^2C bus on the FPC.

6.5 Server Management Buses

6.5.1 Intelligent Platform Management Bus (IPMB)

The Intelligent Platform Management Bus (IPMB) is a multimaster open-drain serial bus that is routed between major system modules. The BMC, FPC, and HSC use the IPMB to transmit messages. The bus is compatible electrically, and from a timing perspective, with the 100kB/s version of the *Phillips I^2C Bus Specification*. The IPMB supports both intelligent devices, such as server management microcontrollers, and nonintelligent devices, such as the FRU SEEPROM.

For further details, refer to the *A450NX MP Server Board Set Technical Product Specification.*

6.5.2 Intelligent Chassis Management Bus (ICMB)

The Intelligent Chassis Management Bus (ICMB), along with the ICMB bridge, provides a mechanism for interchassis management communications. Multiple systems and peripheral chassis can be connected to the same ICMB. Through the ICMB, intelligent devices local to a server (e.g., the BMC) can access the local server management functions of external servers, allowing server management across multiple servers.

6.5.2.1 IPMB-ICMB Bridging

The chassis front panel controller (FPC) acts as a bridge between the IPMB and the ICMB. The bridging controller provides a messaging connection between the IPMB and the ICMB. It also responds to ICMB discovery messages, and other bridge request messages, such as providing ICMB protocol version information.

6.6 FRU Inventory Information

All chassis boards hold a nonvolatile storage device that contains FRU inventory information. The FRU inventory information includes board serial number, part number, and revision information. It can also contain asset tag, product name, chassis, and OEM specific information. The information is provided to aid in system servicing, inventory, and asset tracking. The I^2C address, the content, and the format of FRU information about individual chassis boards are described in Chapter 4 of this document. The following chassis boards contain FRU information.

- Front panel board
- Power distribution backplane
- SCSI hot-swap backplane

The FRU device on the front panel holds FRU inventory information for the front panel board, as well as the for chassis.

In addition to the chassis boards, all the boards that make up the A450NX board set also hold a nonvolatile storage device for FRU informantion. The details of the A450NX board set FRU inventory information are provided in the *A450NX MP Server Board Set TPS*.

6.6.1 FRU & SDR Load Utility

The Intel provided FRU & SDR Load Utility allows FRU information for each individual board in the AD450NX server system to be loaded, read, and displayed.

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7. Connector Specifications

This chapter describes the connectors that connect various components of the AD450NX system. The discussion in this chapter includes an overview diagram of the AD450NX server system interconnections, as well as tables describing the signals and pinouts for the various connectors.

Figure 7-1 shows the interconnections of all of the boards used in the AD450NX server system.

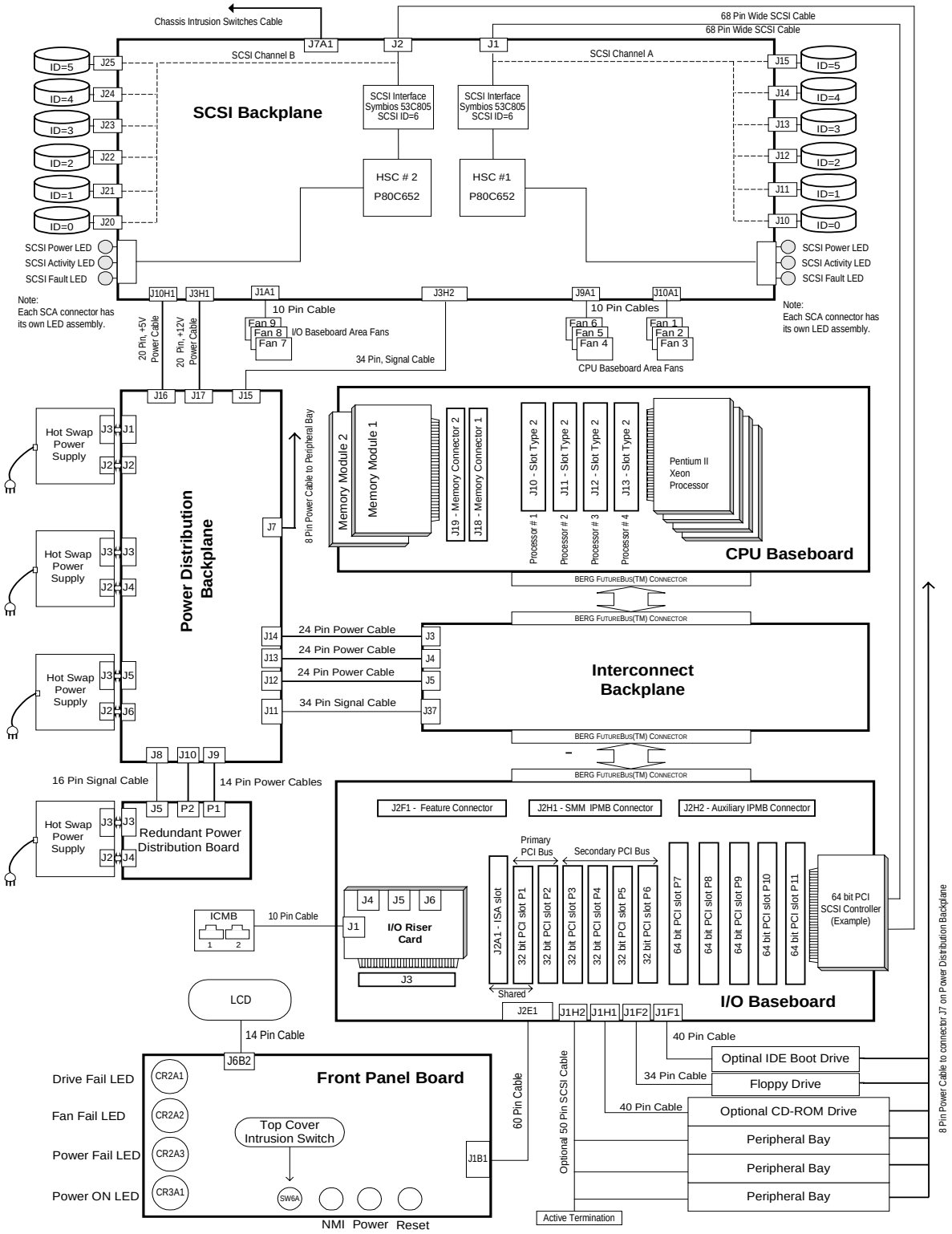

Figure 7-1. AD450NX Server System Interconnect Diagram

7.1 User-accessible I/O Connectors

The following section describes signals and pinouts for various user-accessible I/O connectors on the AD450NX server system board set.

7.1.1 Keyboard and Mouse Ports

These identical PS/2 compatible ports share a common housing. The top port is the mouse and the bottom port is the keyboard.

Table 7-1. Pin Assignment for Keyboard and Mouse Ports

Mouse		Keyboard	
Pin	**Signal**	**Pin**	**Signal**
1	MSEDAT (mouse data)	1	KEYDAT (keyboard data)
2	No connection	2	No connection
3	GND (ground)	3	GND (ground)
4	FUSED_VCC (+5 V)	4	FUSED_VCC (+5 V)
5	MSECLK (mouse clock)	5	KEYCLK (keyboard clock)
6	No connection	6	No connection

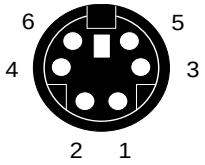

Figure 7-2. Keyboard or Mouse Connector

7.1.2 Serial Ports

The I/O baseboard provides two stacked RS-232C serial ports (the top one is COM1 and the bottom one is COM2). These ports are D-subminiature 9-pin connectors. Each serial port can be enabled separately with the configuration control provided on the I/O baseboard.

The COM2 serial port can be used either as an EMP or as a normal serial port. As an EMP, COM2 is used as a communication path by the server management RS-232 connection to the FPC on the front panel board. This provides a level of emergency management through an external modem. The RS-232 connection can be monitored by the FPC when the system is in a powered down (standby) state.

Table 7-2. Pin Assignment for Serial Port Connector

Pin	Signal
1	DCD
2	RXD
3	TXD

Pin	Signal
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RIA

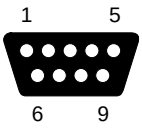

Figure 7-3. Serial Port Connector

7.1.3 Parallel Port

The IEEE 1284-compatible parallel port—used primarily for a printer—sends data in parallel format. The parallel port is accessed through a D-subminiature 25-pin connector.

Table 7-3. Pin Assignment for Parallel Port Connector

Pin	Signal	Pin	Signal
1	STROBE_L	14	AUFDXT_L (auto feed)
2	Data bit 0	15	ERROR_L
3	Data bit 1	16	INIT_L (initialize printer)
4	Data bit 2	17	SLCTIN_L (select input)
5	Data bit 3	18	GND (ground)
6	Data bit 4	19	GND
7	Data bit 5	20	GND
8	Data bit 6	21	GND
9	Data bit 7	22	GND
10	ACK_L (acknowledge)	23	GND
11	BUSY	24	GND
12	PE (paper end)	25	GND
13	SLCT (select)		

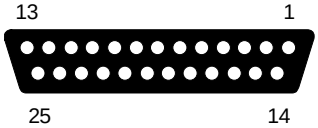

Figure 7-4. Parallel Port Connector

7.1.4 VGA Video Port

The video port interface is a standard VGA compatible 15-pin connector. Onboard video is supplied by a Cirrus Logic GD5446* PCI video controller with 2 MB of onboard video DRAM.

Table 7-4. Pin Assignment for Video Connector

Pin	Signal
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND (video ground, shield)
6–8	GND (video ground, shield)
9	No connection
10	GND (video ground)
11–12	No connection
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	No connection

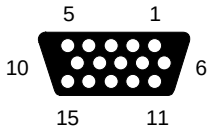

Figure 7-5. Video Connector

7.1.5 Universal Serial Bus (USB) Interface

The built-in USB ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports.

Table 7-5. Pin Assignment for Dual USB Connector

Pin	Signal	Description
A1	VCC	Over-current monitor line port 0
A2	DATAL0	Differential data line paired with DATAH0
A3	DATAH0	Differential data line paired with DATAL0
A4	GND	Ground potential
B1	VCC	Over-current monitor line port 1
B2	DATAL1	Differential data line paired with DATAH1
B3	DATAH1	Differential data line paired with DATAL1
B4	GND	Ground potential

Figure 7-6. Dual USB Connector

7.1.6 ICMB Connectors

The server provides two SEMCONN 6-pin connectors to allow daisy chained cabling. Information about ICMB can be found in Chapter 4 of this document.

Table 7-6. Pin Assignment for ICMB Connector

Pin	Signal
1	No connection
2	No connection
3	B (negative)
4	A (positive)
5	No connection
6	No connection

Figure 7-7. ICMB Connector

7.2 Wide Ultra SCSI Hot-swap Backplane Connectors

7.2.1 SCSI Input Connector

The 68-pin SCSI input connector on the SCSI hot-swap backplane is a nonshielded device.

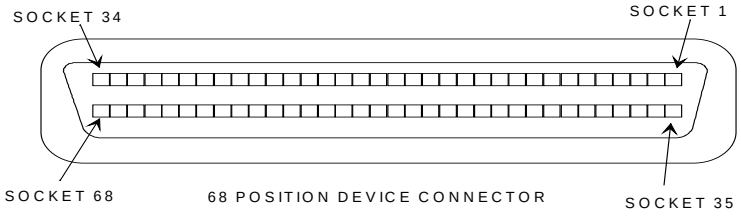

Figure 7-8. SCSI Input Connector, Nonshielded

Table 7-7. Pin Assignment for SCSI Input Connector (J1,J2)

Signal	Connector Contact Number	SCSI Bus Conductor Number	SCSI Bus Conductor Number	Connector Contact Number	Signal
GND (ground)	1	1	2	35	DB12_L
GND	2	3	4	36	DB13_L
GND	3	5	6	37	DB14_L
GND	4	7	8	38	DB15_L
GND	5	9	10	39	DBP1_L
GND	6	11	12	40	DB0_L
GND	7	13	14	41	DB1_L
GND	8	15	16	42	DB2_L
GND	9	17	18	43	DB3_L
GND	10	19	20	44	DB4_L
GND	11	21	22	45	DB5_L
GND	12	23	24	46	DB6_L
GND	13	25	26	47	DB7_L
GND	14	27	28	48	DBP_L
GND	15	29	30	49	GND
GND	16	31	32	50	GND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED	19	37	38	53	RESERVED
GND	20	39	40	54	GND
GND	21	41	42	55	ATN_L
GND	22	43	44	56	GND
GND	23	45	46	57	BSY_L
GND	24	47	48	58	ACK_L
GND	25	49	50	59	RST_L
GND	26	51	52	60	MSG_L
GND	27	53	54	61	SEL_L
GND	28	55	56	62	C/D_L
GND	29	57	58	63	REQ_L
GND	30	59	60	64	I/O_L
GND	31	61	62	65	DB8_L
GND	32	63	64	66	DB9_L
GND	33	65	66	67	DB10_L
GND	34	67	68	68	DB11_L

7.2.2 SCA-2 PressFit Connector

The SCA-2 PressFit connector is used on the secondary side of the hot-swap backplane. The pin out is the same as an SCA-1. Connector pin assignment is for the current draft *SFF-8046 Rev. 1.1* document.

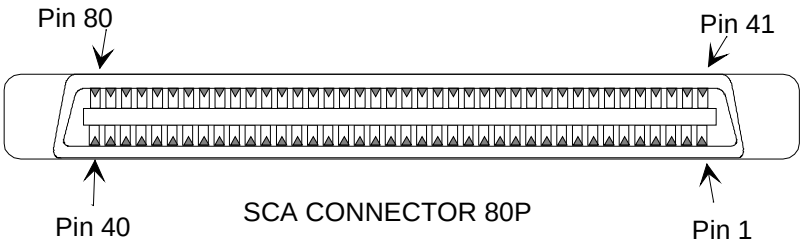

Figure 7-9. SCA-2 PressFit Connector

Table 7-8. Pin Assignment for SCA-2 PressFit Connector (J10-J15, J20-J25)

Pin	Signal		Signal		Pin
1	12 V Charge	(L)	(L)	12 V Ground	41
2	12 V	(S)	(L)	12 V Ground	42
3	12 V	(S)	(L)	12 V Ground	43
4	12 V	(S)	(S)	Mated 1	44
5	Reserved/ESI-1	(S)	(L)	EFW_L	45
6	Reserved/ESI-2	(S)	(L)	DIFFSNS	46
7)	DB_L(11)	(S)	(S)	Ground	47
8	DB_L(10)	(S)	(S)	Ground	48
9	DB_L(9)	(S)	(S)	Ground	49
10	DB_L(8)	(S)	(S)	Ground	50
11	I/O_L	(S)	(S)	Ground	51
12	REQ_L	(S)	(S)	Ground	52
13	C/D_L	(S)	(S)	Ground	53
14	SEL_L	(S)	(S)	Ground	54
15	MSG_L	(S)	(S)	Ground	55
16	RST_L	(S)	(S)	Ground	56
17	ACK_L	(S)	(S)	Ground	57
18	BSY_L	(S)	(S)	Ground	58
19	ATN_L	(S)	(S)	Ground	59
20	DB_L(P)	(S)	(S)	Ground	60
21	DB_L(7)	(S)	(S)	Ground	61
22	DB_L(6)	(S)	(S)	Ground	62
23	DB_L(5)	(S)	(S)	Ground	63
24	DB_L(4)	(S)	(S)	Ground	64
25	DB_L(3)	(S)	(S)	Ground	65
26	DB_L(2)	(S)	(S)	Ground	66
27	DB_L(1)	(S)	(S)	Ground	67
28	DB_L(0)	(S)	(S)	Ground	68
29	DB_L(P1)	(S)	(S)	Ground	69
30	DB_L(15)	(S)	(S)	Ground	70
31	DB_L(14)	(S)	(S)	Ground	71
32	DB_L(13)	(S)	(S)	Ground	72
33	DB_L(12)	(S)	(S)	Ground	73
34	5 V	(S)	(S)	Mated 2	74

Pin	Signal		Signal		Pin
35	5 V	(S)	(L)	5 V Ground	75
36	5 V Charge	(L)	(L)	5 V Ground	76
37	Spindle Sync	(L)	(L)	Active LED Out	77
38	MTRON	(L)	(L)	DLYD_START	78
39	SCSI ID (0)	(L)	(L)	SCSI ID (1)	79
40	SCSI ID (2)	(L)	(L)	SCSI ID (3)	80

7.2.3 Signal Connector

Table 7-9. Pin Assignment for Signal Connector (J3H2)

Pin	Signal	Pin	Signal
1	Ground	18	Ground
2	Ground	19	Intrusion_L
3	SCL	20	Ground
4	Ground	21	Fan_12 V_10V_L
5	Key	22	Ground
6	Ground	23	Intrusion_IN
7	SDA	24	Ground
8	Ground	25	HSBP_PGM_MODE
9	RST_HSBP_L	26	Ground
10	Ground	27	HSBP_PGM_ENABLE
11	PWR_GOOD	28	Ground
12	Ground	29	HSBP_PGM_SCLK
13	Interlock	30	Ground
14	Ground	31	HSBP_PGM_SDI
15	RST_ I2C _L	32	Ground
16	Ground	33	HSBP_PGM_SDO
17	Interlock_IN	34	Ground

7.2.4 +5 V Power Connector

Table 7-10. Pin Assignment for +5 V Power Connector (J10H1)

Pin	Signal	Color	Pin	Signal	Color
1	+5 V	white	11	+5 V	white
2	Ground	black	12	Ground	black
3	+5 V	white	13	+5 V	white
4	Ground	black	14	Ground	black
5	+5 V	white	15	+5 V	white
6	Ground	black	16	Ground	black
7	+5 V	white	17	+5 V	white
8	Ground	black	18	Ground	black
9	+5 V	white	19	+5 V	white
10	Ground	black	20	Ground	black

7.2.5 +12 V Power Connector

Table 7-11. Pin Assignment for +12 V Power Connector (J3H1)

Pin	Signal	Color	Pin	Signal	Color
1	+12V_R	white	11	+12V_R	white
2	Ground	black	12	Ground	black
3	+12V_R	white	13	+12V_R	white
4	Ground	black	14	Ground	black
5	+12V_L	white	15	+12V_L	white
6	Ground	black	16	Ground	black
7	+12V_L	white	17	+12V_L	white
8	Ground	black	18	Ground	black
9	+12V_P_BAY	white	19	+12VFAN_PWR	white
10	Ground	black	20	Ground	black

7.2.6 Fan Connector

Table 7-12. Pin Assignment for Fan Connectors (J1A1,J9A1,J10A1)

Pin	Signal	Color
1	Ground	black
2	signal	yellow
3	12VFAN_PWR	red
4	Ground	black
5	signal	yellow
6	12VFAN_PWR	red
7	Ground	black
8	signal	yellow
9	12VFAN_PWR	red

7.2.7 Intrusion Switch Connector

Table 7-13. Pin Assignment for Intrusion Switch Connector J7A1

Pin	Signal
1	INTRUSION_L
2	INTRUSION2 (connected to pin 3)
3	INTRUSION2 (connected to pin 2)
4	INTRUSION_IN

7.3 Front Panel Connector

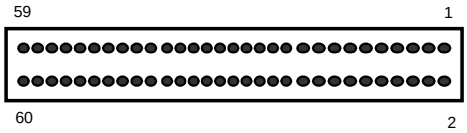

Figure 7-10.Front Panel Connector

Table 7-14 describes the interface signals between the I/O baseboard and front panel board. The suffix "_L" at the end of a signal name indicates that the signal is active low.

Table 7-14. Front Panel Connector Signal Descriptions (J1B1)

Signal(s)	Pin Number	Signaling Level	Source Component	Destination Component	Description
+5 V	2	PWR	PWR_DIST	FP	Main 5 V supply
COM2_TO_FP_EN	19	CMOS	FP	Riser Card	Connects the COM2 transceiver to the front panel for front panel redirection.
COM2_TO_SIO_EN_A	21	CMOS	FP	I/O	Connects the COM2 transceiver to the SMC Super I/O chip and the IPMB transceiver to the front panel.
CTS_TTL_FP	45	CMOS	Riser Card	FPC	COM2 redirection signal.
DCD_TTL_FP	41	CMOS	Riser Card	FPC	COM2 redirection signal.
DSR_TTL_FP	43	CMOS	Riser Card	FPC	COM2 redirection signal.
DTR_TTL_FP	55	CMOS	FPC	Riser Card	COM2 redirection signal.
FAN_FAILED_L	6	TTL	HSBP	FP	Signal from the power distribution board indicating a fan failure
FP_NMI_SWT_L	28	CMOS	FP	PIIX4E	System NMI switch. This is debounced by the BMC.
FP_TO_PIIX4_PWRBTN_L	12		FPC	PIIX4E	This signal is associated with ACPI. It is connected to the PWRBTN input to the PIIX4E. The PWRBTN# input signal can be used to generate an SMI# upon its assertion.
GROUND	1,4,14,17,32,39,42,49,52,57,60				Ground
HARD_RESET	26	TTL	FP	All components	Overall system reset from FP. Assert >500ms. Deassert >=0ms.
I2C_BACKUP_SCL	56	TTL, OC	BMC	FP	ICMB clock.
I2C_BACKUP_SDA	58	TTL, OC	BMC	FP	ICMB data.
I2C_CEL_CONNECT_BMC_A	46	CMOS	FP	I/O	Connects SEL serial EEPROM to BMC.
I2C_CEL_CONNECT_FPC	44	CMOS	FP	I/O	Connects SEL serial EEPROM to FPC.

Signal(s)	Pin Number	Signaling Level	Source Component	Destination Component	Description
I2C_FPC_SCL	48	CMOS, OC	FP	PWR_DIST	Private I^2C bus clock of the front panel.
I2C_FPC_SDA	50	CMOS, OC	FP	PWR_DIST	Private I^2C bus data of the front panel.
INTRUSION_L	10	TTL	HSBP	FP	Indicates SCSI hot-swap bay disk door has been opened.
ISP_FPC_EN_L	9	TTL	BMC	FP PLD	Enable pin for PLD reprogramming.
ISP_FPC_SDO	13	CMOS	FP PLD	BMC	Serial data output pin for PLD reprogramming.
ISP_MODE	11	TTL	BMC	FP PLD	Mode pin for PLD reprogramming.
ISP_SCLK	5	TTL	BMC	FP PLD	Clock pin for PLD reprogramming.
ISP_SDI	7	TTL	BMC	FP PLD	Serial data input pin for PLD reprogramming.
PS_PWR_ON	40	CMOS	FP,PWR_DIST	PWR_DIST, FP	Open-Collector signal telling power supplies to turn on. The signal is pulled low in the case of a 240 VA. The signal is both an input and output to the FPC.
PWR_CNTRL_RTC_L	36	TTL	SMC	FP	Power control signal from SMC. High time >5 ms. Low time 5 ms.
PWR_CNTRL_SFC_L	34	TTL	SMM	FP	Power control signal from SMM. High time >=5 ms. Low 5–100 ms.
PWR_GOOD	38	TTL	PWR_DIST	FP	Signal indicating power supplies are stable
Reserved	16,18,22,27,30,37,54,59				Reserved for future use.
RI_TTL_FP	47	TTL	Riser Card	FP	COM2 redirection signal.
RTS_TTL_FP	53	TTL	Riser Card	FP	COM2 redirection signal. Output from FPC, input to I/O Riser card.
SECURE_MODE_BMC	24	TTL	SMC	BMC/FP	Signal from SMC indicating a system-secure state.
SIN_TTL_COM2	29	TTL	Riser Card	FPC	COM2 redirection signal.
SIN_TTL_XIMB	31	TTL	Riser Card	FPC	ICMB receive.
SOUT_TTL_COM2	33	TTL	FPC	Riser Card	COM2 redirection signal.
SOUT_TTL_XIMB	35	TTL	FPC	Riser Card	ICMB transmit.
SPEAKER_DATA	8	TTL	SMC	FP	An amplified version of this signal drives the speaker on the front panel.
SYS_RESET_STATE	20	TTL	SMIC	undefined	Indication to the FPC that of the system reset state.
VCC_STDBY	3,15,25, 51	PWR	PWR_DIST	FP	Always-alive power to FP.
XIMB_SOUT_EN	23	TTL	FPC	Riser Card	Open collector signal. Output enables the ICMB transceivers TxD RS485 output.

† Signal is not used by Intel.

‡ Associated with front panel redirection. These signals remain active at the front panel connector even when COM2 has been connected to the SMC Super I/O chip on the I/O baseboard.

7.4 Power Distribution Backplane Connector

The pin assignments for various connectors on the power distribution backplane are described in the following tables.

Table 7-15. Pin Assignment For Connectors J1, J3 and J5

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Ground	7	VCC3	13	Ground	19	VCC3
2	Ground	8	VCC12	14	Ground	20	VCC12
3	Ground	9	-12VCC	15	Ground	21	VCC12
4	Ground	10	VCC12	16	Ground	22	VCC5
5	Ground	11	VCC5	17	Ground	23	VCC5
6	Ground	12	VCC5	18	VCC3	24	VCC5

Table 7-16. Pin Assignment For Connector J2

Pin	Signal	Pin	Signal
1	5V_RS	9	VBIAS
2	12V_SENSE	10	VCC5STBY
3	3V_RS	11	SUP1_FAULT
4	GND_SENSE	12	SUP1_PRESENT
5	+5.1 LS	13	SUP1_PGOOD
6	+12 LS	14	NC
7	+3.3 LS	15	SUP1_REV
8	PWR_ON_SUPPLIES		

Table 7-17. Pin Assignment For Connector J4

Pin	Signal	Pin	Signal
1	5V_RS	9	VBIAS
2	12V_SENSE	10	VCC5STBY
3	3V_RS	11	SUP2_FAULT
4	GND_SENSE	12	SUP2_PRESENT
5	+5.1 LS	13	SUP2_PGOOD
6	+12 LS	14	NC
7	+3.3 LS	15	SUP2_REV
8	PWR_ON_SUPPLIES		

Table 7-18. Pin Assignment For Connector J6

Pin	Signal	Pin	Signal
1	5V_RS	9	VBIAS
2	12V_SENSE	10	VCC5STBY
3	3V_RS	11	SUP3_FAULT
4	GND_SENSE	12	SUP3_PRESENT
5	+5.1 LS	13	SUP3_PGOOD
6	+12 LS	14	NC
7	+3.3 LS	15	SUP3_REV
8	PWR_ON_SUPPLIES		

Table 7-19. Pin Assignment for Connector J7

Pin	Signal
1	Ground
2	VCC12
3	VCC12
4	VCC5
5	Ground
6	Ground
7	Ground
8	VCC5

Table 7-20. Pin Assignment For Connector J8

Pin	Signal	Pin	Signal
1	5V_RS	9	+5.1 LS
2	VBIAS	10	SUP4_PGOOD
3	12V_SENSE	11	+12 LS
4	VCC5STBY	12	N/A
5	3V_RS	13	+3.3 LS
6	SUP4_FAULT	14	SUP4_REV
7	Ground_Sense	15	PWR_ON_SUP4
8	SUP4_PRESENT	16	CABLES_GOOD_L

Table 7-21. Pin Assignment For Connectors J9 and J10

Pin	Signal	Pin	Signal
1	Ground	8	Cable_Present_Loopback
2	Ground	9	VCC3
3	Ground	10	VCC3
4	Ground	11	VCC5
5	Ground	12	VCC5

Pin	Signal	Pin	Signal
6	VCC12	13	VCC5
7	VCC12	14	Ground

Table 7-22. Pin Assignment For Connector J11

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	HSBP_PGM_SDI	10	NC	19	RESET_HSBP_L	28	5V_SENSE
2	HSBP_PGM_SDO	11	VCC5STBY	20	Ground	29	GROUND_SENSE
3	HSBP_PGM_EN	12	Ground	21	VBIAS_FP	30	3V_SENSE
4	HSBP_PGM_SCLK	13	I2C_FPC_SCL	22	Reserved	31	Ground
5	INTRUSION_L	14	I2C_GLOBAL_SCL	23	PS_PWR_ON	32	Ground
6	I2C_GLOBAL_SDA	15	I2C_FPC_SDA	24	HSBP_PGM_MODE	33	NC
7	PWR_GOOD	16	Ground	25	Ground	34	NC
8	Ground	17	N/A	26	Ground		
9	VCC5STBY	18	Ground	27	12V_SENSE		

Table 7-23. Pin Assignment For Connector J12

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC5	7	VCC5	13	VCC12	19	VCC3
2	Ground	8	Ground	14	Ground	20	Ground
3	VCC5	9	VCC5	15	VCC12	21	VCC3
4	Ground	10	Ground	16	Ground	22	Ground
5	VCC5	11	VCC12	17	VCC3	23	VCC3
6	Ground	12	Ground	18	Ground	24	-12VCC

Table 7-24. Pin Assignment For Connector J13

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC5	7	VCC5	13	VCC12	19	VCC3
2	Ground	8	Ground	14	Ground	20	Ground
3	VCC5	9	VCC5	15	VCC12	21	VCC3
4	Ground	10	Ground	16	Ground	22	Ground
5	VCC5	11	VCC12	17	VCC3	23	VCC3
6	Ground	12	Ground	18	Ground	24	Cable2_L

Table 7-25. Pin Assignment For Connector J14

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC5	7	VCC5	13	VCC12	19	VCC3
2	Ground	8	Ground	14	Ground	20	Ground
3	VCC5	9	VCC5	15	VCC12	21	VCC3
4	Ground	10	Ground	16	Ground	22	Ground
5	VCC5	11	VCC12	17	VCC3	23	VCC3
6	Ground	12	Ground	18	Ground	24	Cable1_L

Table 7-26. Pin Assignment For Connector J15

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Ground	10	Ground	19	INTRUSION_L_IO	28	Ground
2	Ground	11	PWR_GOOD	20	Ground	29	HSBP_PGM_SCLK
3	I2C_GLOBAL_SCL	12	Ground	21	FAN_12V_10V_L	30	Ground
4	Ground	13	NC	22	Ground	31	HSBP_PGM_SDI
5	N/A	14	Ground	23	INTRUSION_IN_IO	32	Ground
6	Ground	15	NC	24	Ground	33	HSBP_PGM_SDO
7	I2C_GLOBAL_SDA	16	Ground	25	HSBP_PGM_MODE	34	Ground
8	Ground	17	NC	26	Ground		
9	RESET_HSBP_L	18	Ground	27	HSBP_PGM_ENABLE_L		

Table 7-27. Pin Assignment For Connector J16

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC5.1A	6	Ground	11	VCC5.1A	16	Ground
2	Ground	7	VCC5.1A	12	Ground	17	VCC5.1A
3	VCC5.1A	8	Ground	13	VCC5.1A	18	Ground
4	Ground	9	VCC5.1A	14	Ground	19	VCC5.1A
5	VCC5.1A	10	Ground	15	VCC5.1A	20	Ground

Table 7-28. Pin Assignment For Connector J17

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC12A	6	Ground	11	VCC12A	16	Ground
2	Ground	7	VCC12B	12	Ground	17	VCC12B
3	VCC12A	8	Ground	13	VCC12A	18	Ground
4	Ground	9	VCC12	14	Ground	19	VCCFAN
5	VCC12B	10	Ground	15	VCC12B	20	Ground

7.5 Redundant Power Distribution Board

The pin assignments for various connectors on the redundant power distribution board are described in Table 7-29 through Table 7-33.

Table 7-29. Pin Assignment for Connector J3

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Ground	7	VCC3	13	Ground	19	VCC3
2	Ground	8	VCC12	14	Ground	20	VCC12
3	Ground	9	NC†	15	Ground	21	VCC12
4	Ground	10	VCC12	16	Ground	22	VCC5
5	Ground	11	VCC5	17	Ground	23	VCC5
6	Ground	12	VCC5	18	VCC3	24	VCC5

† Not Connected

Table 7-30. Pin Assignment for Connector J4

Pin	Signal	Pin	Signal
1	5V_RS	9	VBIAS
2	12V_SENSE	10	VCC5STBY
3	3V_RS	11	SUP4_FAULT
4	GND_SENSE	12	SUP4_PRESENT
5	+5.1 LS	13	SUP4_PGOOD
6	+12 LS	14	Not Connected
7	+3.3 LS	15	SUP4_REV
8	PWR_ON_SUPPLY4		

Table 7-31. Pin Assignment for Connector J5

Pin	Signal	Pin	Signal
1	5V_RS	9	+5.1 LS
2	VBIAS	10	SUP4_PGOOD
3	12V_SENSE	11	+12 LS
4	VCC5STBY	12	Not Used
5	3V_RS	13	+3.3 LS
6	SUP4_FAULT	14	SUP4_REV
7	GND_SENSE	15	PWR_ON_SUPPLY4
8	SUP4_PRESENT	16	CABLES_GOOD_L

Table 7-32. Pin Assignment for Connector P1

P1 Pin	Wire to Board Connector	Signal
1	J6	Ground
2	J9	Ground
3	J10	Ground
4	J11	Ground
5	J12	Ground
6	J16	VCC12
7	J17	VCC12
8	J7	CABLE1_PRESENT_L
9	J14	VCC3
10	J15	VCC3
11	J18	VCC5
12	J19	VCC5
13	J20	VCC5
14	J13	Ground

Table 7-33. Pin Assignment for Connector P2

P2 Pin	Wire to Board Connector	Signal
1	J21	Ground
2	J22	Ground
3	J23	Ground
4	J24	Ground
5	J25	Ground
6	J29	VCC12
7	J30	VCC12
8	J8	CABLE2_PRESENT_L
9	J27	VCC3
10	J28	VCC3
11	J31	VCC5
12	J32	VCC5
13	J33	VCC5
14	J26	Ground

8. Reliability, Availability, and Serviceability

8.1 MTBF

Table 8-1 lists the calculated AD450NX server system hard Mean Time Between Failures (MTBF). A hard failure indicates a permanent or repeatable failure that can be readily remedied by replacing the faulty part with a good part. The MTBF calculations are derived using the procedures described in Intel's *Environmental Standards Handbook*, (document number 662394-03).

Table 8-1. AD450NX Server System MTBF at 35°C

Sub Assembly Description	Sub Assembly QTY	Total Sub Assembly MTBF (Hrs)	Total Sub Assembly Failure Rate (FITs)
CPU Baseboard (4 slot)	1	140,472	5,694
VRM Modules	6	512,847	9,359
I/O Baseboard	1	127,900	6,254
Processor	4	1,000,000	3,200
Memory Module	2	196,631	8,136
SCSI Backplane	1	135,631	5,898
LCD Display	1	690,322	1,159
Front Panel Board	1	1,005,136	796
Interconnect Backplane	1	713,674	1,121
I/O Riser Card	1	998,861	801
Power Distribution Backplane	1	208,026	3,845
Toshiba CD ROM	1	100,000	2,000
420W Power Supply	3	128,000	23,438
1.44MB 3.5" Floppy Drive	1	81,000	2,469
Chassis (Intrusion Switches)	1	18,518,519	9
Chassis Cooling Fans	0 [1]	330,000	NA
MTBF in Hrs [2]		**13,481**	
Total Failure Rate (FITs)			**74,177**

Notes: **1.** Chassis cooling fans are redundant in the factory default configuration. Generally a single fan failure does not require an *immediate* shutdown of the system. The chance of a second fan failure during this time is considered very slight. However, as soon as a replacement fan becomes available, the system must be shut down for the maintenance to be performed.

2. The MTBF numbers are for a standard system with four Pentium® II Xeon™ processors and two memory modules with 0 MB memory.

8.2 Serviceability

The AD450NX server system is designed for service by qualified technical personnel only. The desired Mean Time To Repair (MTTR) of the system is 30 minutes including diagnosis of the system problem. To meet this goal, the system enclosure and hardware have been designed to minimize the MTTR. Table 8-2 shows the maximum times a trained field service technician should take to perform the listed system maintenance procedures, after diagnosis of the system.

Table 8-2 Maintenance Procedure Performance Times

Maintenance Procedure	**Maximum Time to Perform**
Remove covers	1 minute
Remove and replace: Jigsaw Foam Air Baffle	2 minutes
Remove and replace: Two 3-fan Array Assemblies	5 minutes
Remove and replace: Memory Module	5 minutes
Remove and replace: Front-side Bus Terminator Module	4 minutes
Remove and replace: Intel® Pentium® II Xeon™ processor	2 minutes
Remove and replace: VRM	2 minutes
Remove and replace: Backplane Interconnect Assembly	8 minutes
Remove and replace: CPU Baseboard	15 minutes
Remove and replace: Front Panel Board	5 minutes
Remove and replace: 3-fan Array Assembly	3 minutes
Remove and replace: I/O Riser Card	5 minutes
Remove and replace: IO Baseboard (with no expansion cards)	15 minutes
Remove and replace: SCSI Backplane	15 minutes
Remove and replace: Power Backplane	10 minutes
Remove and replace: Power Supply	1 minute
Remove and replace: Expansion Board	5 minutes
Remove and replace: Disk Drive	1 minute
Overall MTTR (not including problem diagnosis)	**15 minutes**

9. Regulatory Certifications and Compliance

The AD450NX server system, consisting of the AD450NX server system chassis and the A450NX board set, meets specifications and regulations for safety and electromagnetic compatibility (EMC) as described in the following sections.

The AD450NX server system complies with *EU EMC Directive 89/336/EEC*, using standards *EN55022 Class B* and *EN50082-1*, and the *EU Low Voltage Directive 73/23/EEC*, using the *EN60 950* standard.

9.1 Safety Compliance

USA / Canada:	UL 1950 - CSA 950-95, 3rd Edition
Europe:	ERG (German GS Mark) to EN60950 2nd Edition with Amendments EU Low Voltage Directive (73/23/EEC) (CE Mark) EU Directive 93/68/EEC (Article 13 and Annex IV)
International:	NEMKO to IEC950 (A1 to A4) NEMKO to EN60950 (A1 to A3) NEMKO to EMKO-TSE(74-SEC) 207/94

9.1.1 Electromagnetic Compatibility (EMC)

USA:	FCC CFR 47 Parts 2 and 15, Tested Class A
Canada:	IC ICES-003 Class A
Europe:	EN55022, Class A EN50082-1 (Immunity) IEC 801-2 ESD Susceptibility IEC 801-3 Radiated Immunity IEC 801-4 Electrical Fast Transient EMC Directive (89/336/EEC) (CE Mark) EN 61000-3-2; -3, the Line Harmonics
International:	CISPR 22, Class A
Japan:	VCCI Class A ITE (CISPR 22 B Limit).

9.1.2 CE Mark

The CE marking on this product indicates that it is in compliance with the European community's EMC and Low Voltage Directives.

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10. Environmental Specifications

The AD450NX system has been tested to the environmental specifications as indicated in Table 10-1.

Table 10-1. Environmental Specifications Summary

Environmental Feature	Specification
Operating temperature	5° to 35°C (41° to 95°F)
Nonoperating temperature	-40°C to 70°C (-104° to 158°F)
Operating humidity	85%, noncondensing at 40°C (104°F) <33°C (59.4°F) wet bulb at 40°C (104°F) without peripherals
Nonoperating humidity	95%, noncondensing at +55°C (131°F)
Safety	UL 1950, CSA 950, IEC 950, ERG EN60 950, NEMKO
Emissions	FCC Class A; tested to CISPR 22/EN55022, Class B, and registered with VCCI
Immunity	Verified to comply with EN 50082-1
Electrostatic discharge (ESD)	Tested to ESD levels up to 20 kilovolts (kV) air discharge without physical damage per Intel environmental test specifications
Acoustic noise	<50 dBA @ 28°C measured at bystander position (~3 ft from system)
Mechanical shock, operating	2 G, 11 msec duration, 1/2 sine wave