# Intel® A450NX MP Server Board Set

## *Technical Product Specification*

**Revision 1.0**

**August 1998**

**Enterprise Server Group**

int<sub>e</sub>l®

# Revision History

| Date | Rev | Modifications |
|---|---|---|
| 06/08/98 | 0.1 | Compilation of first draft. |
| 08/98 | 1.0 | First external release. |
| | | |

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# Conventions and Terminology

| Term | Definition |
| --- | --- |
| µA | microamp (0.000001 amps) |
| µF | microfarad |
| µS | microsecond |
| A | ampere (amp) |
| ABP | address bit permuting |
| AC | Alternating current.  In the context normally used in this document this refers to the power main. |
| ACPI | advanced configuration and power interface |
| AGTL+ | Assisted Gunning Transceiver Logic +.  An Intel enhanced version of GTL (Gunning Transceiver Logic) |
| APIC | advanced programmable interrupt controller |
| ASIC | application specific integrated circuit |
| asserted | A signal is asserted when active.<br><br>Active-high (positive true) signals are asserted when in the high electrical state (near power potential). Active high signals do NOT have a _L symbol at the end of the name.<br><br>Active-low (negative true) signals are asserted when in the low electrical state (near ground potential). Active-low signal has a _L symbol at the end of the name. |
| BGA | ball grid array |
| BIST | built-in self test |
| BMC | baseboard management controller - located on I/O baseboard |
| bridge | The circuitry that connects one computer bus to another, allowing an agent on one to access the other. |
| byte | 8-bit quantity |
| CE Mark | indicates certification in the European community |
| CPU | central processing unit |
| CU | Configuration Utility |
| Deasserted | A signal is deasserted when inactive. |
| DIMM | dual Inline memory module. |
| DMA | direct memory access |
| DRAM | dynamic random access memory. |
| DSM | distributed shared memory. |
| DVD | digital video disk |
| DWORD | Double word or four bytes or a single 32-bit quantity. |
| EBDA | extended BIOS data area |
| ECC | Error correction code |
| ECP | enhanced capability port |
| EDO | extended data out |
| EEPROM | electrically erasable programmable read only memory |
| EMC | electromagnetic compatibility |
| EMI | electromagnetic interference |
| EPS | external product specification |
| ESCD | extended system configuration data |
| F | Fahrenheit |
| F16 BP | F16 backplane connecting CPU and I/O baseboards |
| F16 Bus | Fast 16-bit bus |
| Farad | unit of measure for capacitors |
| FP | front panel (contains power, reset, display, and XIMB server management features) |
| FPC | front panel controller |

| Term | Definition |
|------|------------|
| FRB | fault resilient booting |
| FRU | field replaceable unit |
| FSB | front-side bus |
| GB | gigabyte (1024 MB or 1,048,576KB or 1,073,741,824 bytes) |
| GB/s | gigabytes per second |
| HDD | hard disk drive |
| HSBP | SCSI hot-swap backplane |
| HSC | hot-swap controller |
| I/O | input/output |
| I$^2$C | Inter-integrated circuit |
| I$_2$O | intelligent I/O |
| IC | integrated circuit |
| ICMB | Intelligent Chassis Management Bus |
| IDE | integrated drive electronics |
| IOAPIC | I/O Intel® Advanced Programmable Interrupt Controller for symmetric multiprocessor systems |
| IPMB | Intelligent Platform Management Bus |
| IPMI | Intelligent Platform Management Interface |
| ISA | Industry Standard Architecture |
| ISC | Intel® Server Console |
| ISP | In-system programming |
| KB | kilobyte (1024 bytes) |
| MB | megabyte (1024 KB or 1,048,576 bytes) |
| MB/s | megabytes per second |
| Mbit | megabit |
| Mbps | megabits per second |
| MHz | megahertz |
| MIOC | memory and I/O bridge controller |
| MUX | multiplexer |
| mV | millivolts |
| N | Newtons |
| NMI | nonmaskable interrupt |
| ns | nanoseconds |
| OEM | original equipment manufacturer |
| OSPM | operating system directed power management |
| P2XP | Pentium® II Xeon™ processor |
| PAL | programmable array logic |
| PCC | power control circuitry |
| PCI | peripheral component interconnect |
| PD | presence detect |
| pF | picofarad ($10^{-12}$) |
| PID | programmable interrupt device |
| PIIX4E | PCI-ISA-IDE Xcelerator controller |
| PLD | programmable logic device |
| PnP | Plug and Play |
| POST | Power-on Self Test |
| PXB | PCI eXpansion bridge |
| RAM | random access memory |
| RAS/CAS | row address select/column address select |
| RCG | RAS/CAS generator (450NX Chip set) |

| Term | Definition |
|------|------------|
| ROM | read only memory |
| SCSI | small computer systems interface |
| SDR | sensor data record |
| SECC | single edge connector cartridge |
| SEEPROM | serial electrically erasable programmable read only memory |
| SEL | system event log |
| SM | server management |
| SMC | Standard Microsystems Corp. |
| SMIC | system management interface chip |
| SOJ | Plastic Small Outline J-lead package type |
| SPI | serial peripheral interface |
| SSU | System Setup Utility |
| Super I/O | SMC/IC which serves as keyboard port, serial ports, mouse port, and real-time clock for the system, located on the I/O baseboard. |
| SVGA | super video graphics array |
| TPS | technical product specification |
| TSOP | Thin Small Outline Package type |
| TTL | transistor-transistor logic |
| USB | Universal Serial Bus |
| USWC | uncacheable-speculative-write-combining |
| V | volt |
| VGA | video graphics array |
| VMC | voltage management controller |
| VRM | voltage regulator module |
| Vtt | termination voltage |
| WOL | Wake On LAN |
| WORD | two bytes or single 16-bit quantity |

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# 1.  Introduction

This document describes the architecture, functionality and interfaces of the A450NX board set.  The A450NX is a
1-4 processor server board set based on the Pentium® II Xeon™ processor and the Intel® 450NX PCIset.  The
Pentium II Xeon processor is the next generation Intel architecture processor beyond the current Pentium® II
processor.  Both the Pentium II Xeon processor and the 450NX PCIset have been optimized for 4-way server
applications.  Refer to the *A450NX MP Server Board Set Specification Update* for the most recent specification
updates concerning the board set.  The combination of these documents provides an updated overview of the
A450NX MP server board set.

## Features

- 1-4 Pentium® II Xeon™ processors

- Intel 450NX PCIset

- Support for up to 8 GB of 3.3 V EDO DRAM (DIMM's)

- Three peer PCI buses (two 32-bit and one 64-bit bus; all are 5 V and *Peripheral Component Interconnect
  (PCI) Local Bus Specification, Rev 2.1,* compliant)

- Eleven full length I/O slots (five 64-bit, six 32-bit, and one ISA [shared with one of the 32-bit PCI slots])

- Onboard Ultra or Fast/Wide SCSI controller for peripheral devices (Adaptec 7880*)

- Two IDE controllers

- PIIX4E PCI to ISA bridge

- Universal Serial Bus (USB)

- SMC Super I/O component to handle all PC legacy functions (keyboard, mouse, serial, parallel, etc.)

- Programmable interrupt device (PID) - custom Intel® ASIC which provides interrupt steering and I/O
  APIC capabilities

- Complete built-in server management capabilities

- Intelligent Platform Management Bus (IPMB) based on $I^2C$ for communicating server management
  information between all Intelligent Platform Management Interface (IPMI) compliant boards on the
  chassis

- Field replaceable unit (FRU) information stored on all boards (P/N, S/N, board name, etc.), and
  temperature sensors located on all major boards.

## Document Structure and Outline

The information contained in this document is organized into five chapters.  Each board in the A450NX board set
is described in detail in Chapter 2.  Additional chapters for added detail on server management and board set
specifications are also provided.  A description of each chapter is summarized below:

**Chapter 1:  Introduction**
  Provides an architectural overview of the A450NX board set

**Chapter 2:  Board Set Details**
  Provides the functional details of the board set

**Chapter 3:  BIOS Features**
  Describes the featues of the A450NX board set BIOS.

**Chapter 4:  Server Management Implementation**
  Describes the implementation details of the A450NX board set server management features.

**Chapter 5:  Board Set Specifications**
  Describes the electrical, mechanical, environmental, and regulatory specifications of the A450NX

board set.  It also provides specifications for the connectors and for the processor retention mechanism.

# 1.1 Architecture Overview

Figure 1-1 is a block diagram of the A450NX board set.  The following sections briefly describe the various aspects of the A450NX board set architecture.
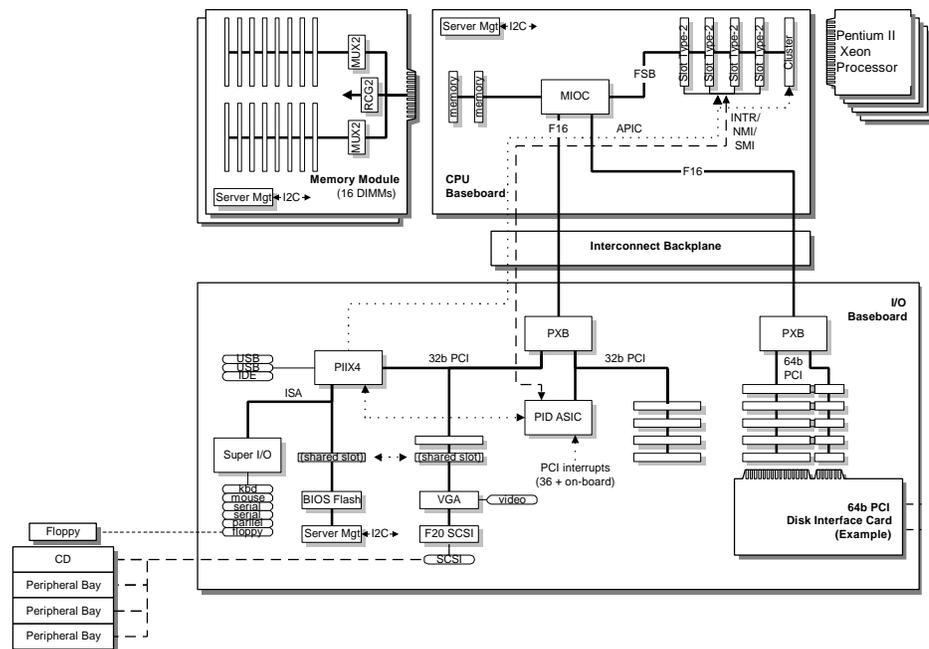


**Note:** Shows the 5-slot version of the CPU baseboard.  A 4-slot CPU baseboard is also available as part of the A450NX board set.  The Intel® AD450NX Server System only supports the 4-slot version.  See Chapter 2 of this document for CPU baseboard details.

*Figure 1-1. A450NX Board Set Block Diagram*

## 1.1.1 Board Set Overview

The A450NX board set is a dual baseboard design that contains a total of seven individual boards.

- CPU baseboard (contains the processor and memory complexes).  The CPU baseboard is available in both 4-slot and 5-slot versions.  The 5-slot CPU baseboard comes only as a board level product and will not be supported in the Intel® AD450NX server chassis.

- I/O baseboard (contains all I/O functions, including PCI and ISA slots)

- I/O riser card (plugs into the I/O baseboard and contains all legacy connectors (video connector, parallel port, 2 serial ports, keyboard and mouse connectors)

- Memory module (either two memory modules are required or one memory module and one memory terminator module)

- Memory terminator module (used to populate the secondary memory connector when only one memory Module is installed)

- Interconnect backplane (provides connection between the I/O baseboard and CPU baseboard.  Also provides the power interface for the entire board set.  Essentially, this is a passive backplane.)

- Front-side bus terminator module (used to terminate the processor bus when a processor is not installed into a processor slot. Can be also used to terminate the cluster slot on the 5-slot CPU baseboard)

The baseboards, when installed into a chassis, are physically placed back to back; connected to each other by the interconnect backplane. The two F16 buses of the 450NX PCIset electrically connect the two baseboards together. Power to the board set is supplied through the interconnect backplane.
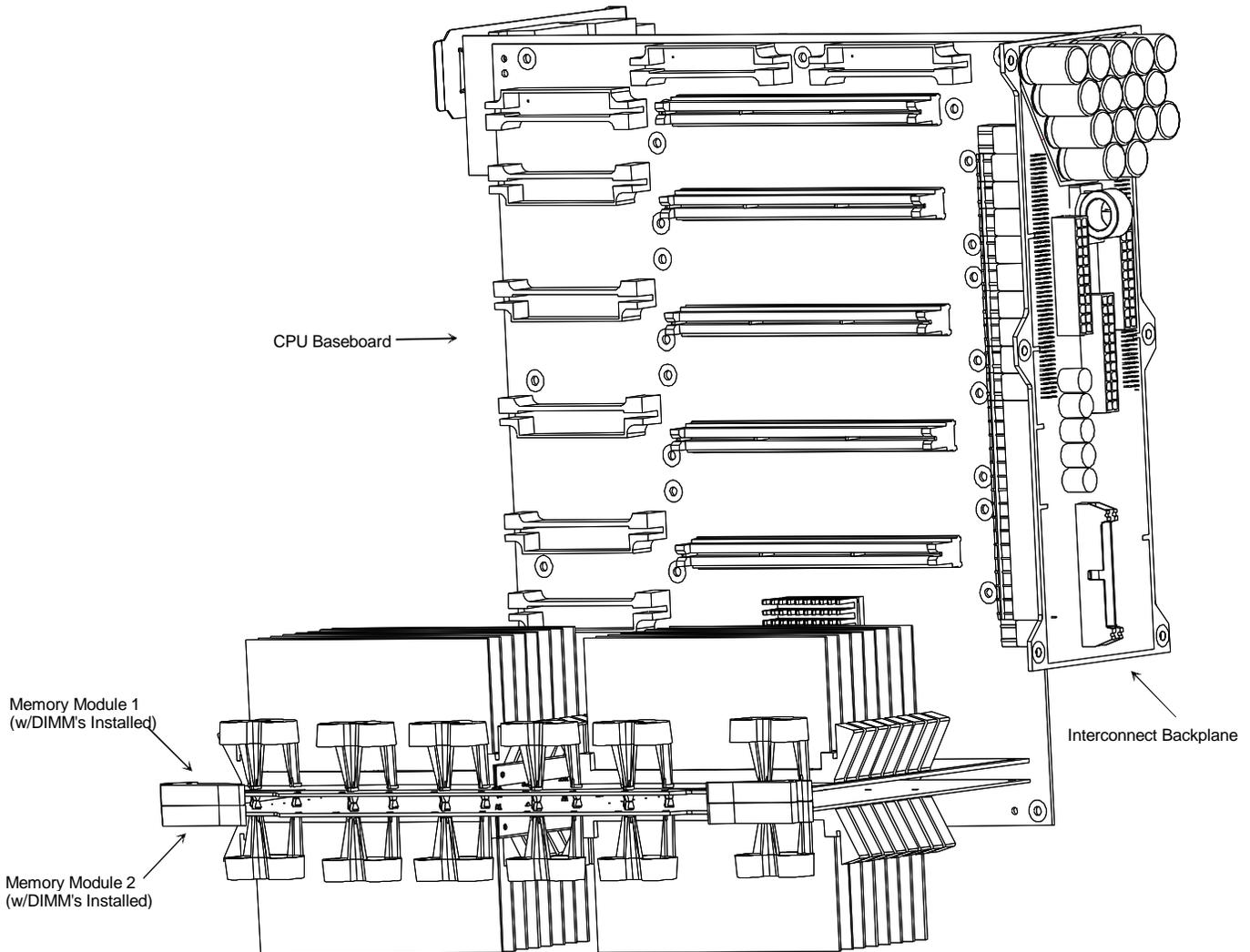


**Note:** The diagram above shows the 5-slot version of the CPU baseboard. A 4-slot CPU baseboard is also available as part of the A450NX board set. The Intel® AD450NX Server System supports only the 4-slot version. See Chapter 2 of this document for CPU baseboard details.

*Figure 1-2.     A450NX Board Set (CPU Baseboard Side)*
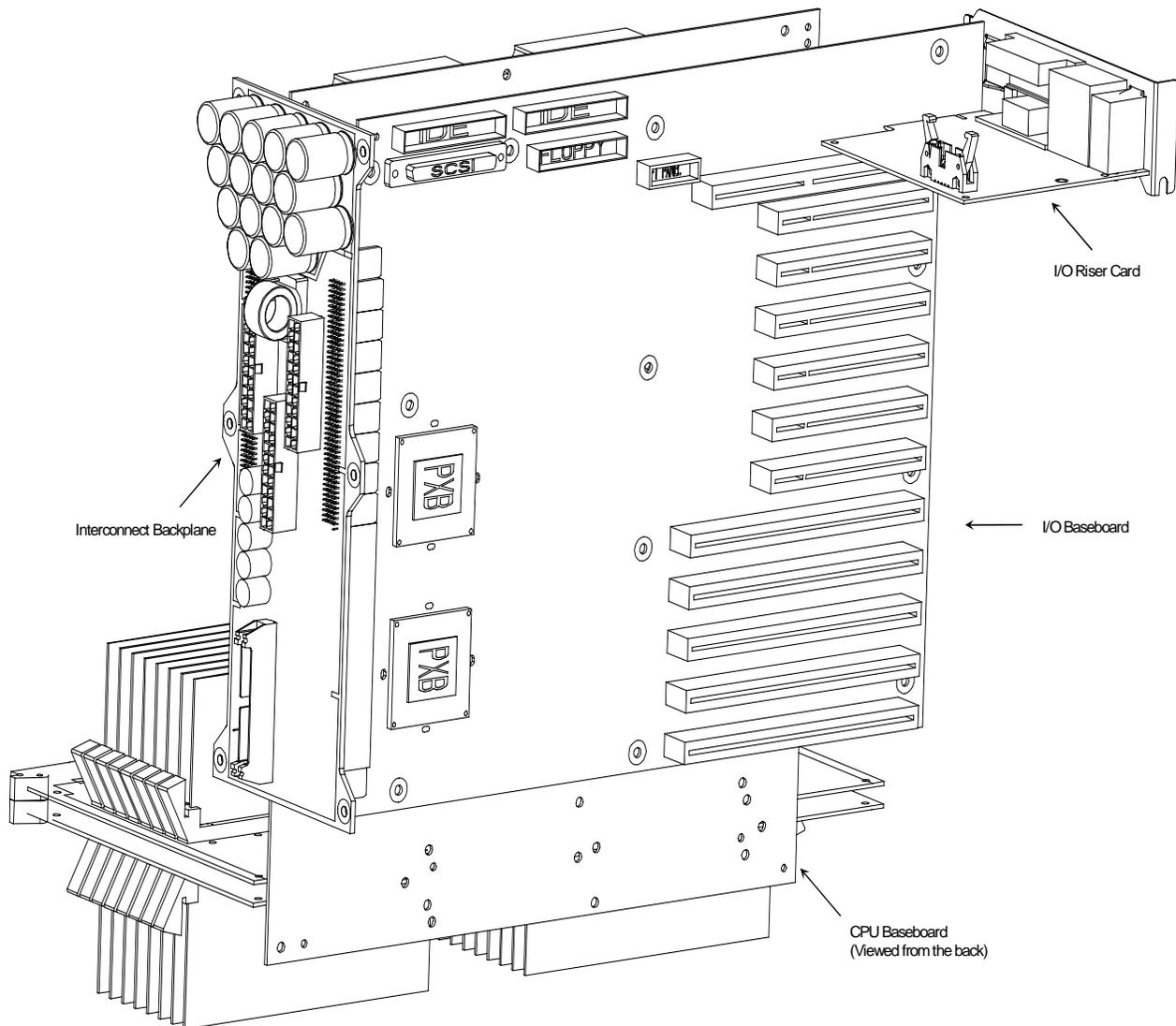
*Figure 1-3.     A450NX Board Set (I/O Baseboard Side)*

## 1.1.1.1   CPU Baseboard

The A450NX CPU baseboard is available in two versions, the 4-slot version and the 5-slot version.  Both versions support one to four Pentium II Xeon processors.  Each processor, packaged in a single-edge connector cartridge (SECC), includes a 100 MHz front-side bus interface, a processor core operating at four or more times the front-side bus frequency (400+ MHz), and a back-side bus that operates at the full frequency of the processor core and supports 512K, 1 MB or 2 MB of L2 cache.  Hardware support for processor fault resilient boot (FRB) is provided.  A front-side bus (FSB) terminator module is required for any unoccupied processor slot.

Along with support for 4 processors, the 5-slot version of the CPU baseboard provides an additional special connector, the distributed shared memory (DSM) cluster connector, on the front-side bus to support a DSM cluster card.  The DSM cluster connector is augmented with additional signals required for DSM clustering.  Note that the operation of the front-side bus is limited to 90 MHz when a cluster card is present.  An FSB terminator module (the same one used for the processor slots) is required if a cluster card is not installed.

**Note:** Usage of the cluster slot is limited.

The final component on the front-side bus is the MIOC component of the 450NX PCIset. This component provides interfaces to the memory subsystem and I/O expansion (F16) buses, in addition to the front-side bus. The memory subsystem interface is equipped with connectors for two A450NX memory modules. A memory terminator module can be used instead of a second memory module, if desired.

Power is supplied to the processors via plug-in voltage regulator modules (VRM). There are a total of six VRM sockets on the 4-slot CPU baseboard and eight VRM sockets on the 5-slot CPU baseboard. Six VRMs are used for the processors (four supply the processor core voltage, two supply the processor L2 cache voltage). VRMs may be installed incrementally as processors are added to the system or may be installed in advance of the processor to ease processor installations in the field. On the 5-slot CPU baseboard, two additional VRM sockets are provided to power a cluster card, should one be installed in an OEM designed system.

In addition to the facilities described above, the CPU baseboard also supports the A450NX server management architecture by providing nonvolatile storage of baseboard and server management data, digital and analog data monitoring hardware, processor disabling controls and access to memory module management data. The 5-slot CPU baseboard also provides Intelligent Platform Management Bus (IPMB) connection for the cluster connector. See Chapter 3 for more details on the CPU baseboard.

## 1.1.1.2    I/O Baseboard

The A450NX I/O baseboard provides the basis for a scalable, high performance, high-slot-count I/O subsystem. Three PCI bus segments are supported (all are peer buses), via two PXBs (the PXB is the PCI expander bridge component of the 450NX PCIset). Two 32-bit PCI segments are configured from the first PXB, while a single 64-bit PCI segment is configured from the second PXB. The 64-bit PCI segment hosts five PCI slots. There are a total of six 32-bit PCI slots on the two 32-bit bus segments (two slots on the primary (compatibility) 32-bit PCI bus, and four slots on the secondary 32-bit PCI bus).

The first of the two 32-bit PCI segments (known as the compatibility bus) hosts the PIIX4E ISA south bridge (with two IDE interfaces and two USB ports), a Cirrus Logic 5446* VGA controller (with 2 MB of video memory on the baseboard), an Adaptec 7880* Ultra/Fast-wide SCSI controller for legacy device support (i.e., CD-ROM, tape drives, etc.), and two PCI slots. One of the PCI slots is shared with the single ISA slot (provided by the PIIX4E). Also provided by the PIIX4E is an SMC FDC37C935AP* Super I/O component (providing two serial ports, a parallel port, a keyboard controller and PS/2 keyboard and mouse ports, a floppy disk interface, and a real-time clock), and an X-bus with 2 MB of BIOS flash and an interface to the server management hardware. Note that the connectors for the serial ports, parallel port, video, and the PS/2 keyboard and mouse ports are provided on a separate I/O riser card (which is part of the A450NX board set). The I/O riser card plugs into the I/O baseboard vertically, next to the ISA slot.

The secondary 32-bit PCI segment hosts four PCI slots, and the programmable interrupt device (PID) application specific integrated circuit (ASIC). The PID provides interrupt steering functions (including support logic for use with the 8259A interrupt controllers in the PIIX4E) and I/O Advanced Programmable Interrupt Controller (APIC) facilities. In addition to the standard IRQs, the PID supports a large number of PCI and onboard interrupt sources; a total of 64 interrupt routing table entries are available. A separate interrupt input will be provided for each of the four interrupts from every 64-bit PCI slot on the I/O baseboard. Separate INTA and INTB connections are provided from every 32-bit PCI slot, but INTC and INTD are bused (in a rotating pattern) from the slots on the 32-bit PCI segments; separate bused connections are provided for each 32-bit PCI segment.

In addition to the two 32-bit PCI bus segments, a third 64-bit PCI segment is included on the I/O baseboard. The only components that reside on this bus are the five 64-bit PCI expansion connectors, which can be used for installation of high performance, high bandwidth 64-bit PCI card adapters.

In addition to the facilities described above, the I/O baseboard also implements the core of the A450NX server management architecture. See Chapter 2 for more details about the I/O baseboard.

## 1.1.1.3    I/O Riser Card

The I/O riser card plugs into the I/O baseboard vertically and provides all of the necessary legacy connectors for video, parallel, serial, keyboard and mouse. The Intelligent Chassis Management Bus (ICMB) connects through the

I/O riser card as well.  All of the connectors are located on the riser card instead of on the I/O baseboard because of real estate constraints on the I/O baseboard.

The I/O riser card supports the AD450NX server management architecture by providing nonvolatile storage of module and server management data.  See Chapter 2 of this document for more details about the I/O riser card.

## 1.1.1.4    Memory Module (16-DIMM Version)

The A450NX memory module provides 16 sites for single high, 168-pin DIMMs, supporting up to 4 GB of 50 nanosecond (ns) or 60 ns 3.3 V buffered extended data out (EDO) DRAM; both 16-Mbit and 64-Mbit DRAMs may be used.  To properly terminate the memory bus, both memory slots must be populated by either two memory modules or one memory and one memory terminator module.  Each memory module is divided into four banks (4-DIMMs per bank) and always supports a 4:1 interleave.  The minimum configuration is four 32-MB DIMMs (one bank).  The supported memory sizes range from 128 MB to 8 GB (4 GB per module).  Supported memory configurations are:

- 32-, 64- and 256-MB DIMM modules
- 50 ns or 60 ns DRAM
- 4-, 8-, 16-, 24-, or 32-DIMMs (total number of DIMMs on both memory modules)
- Equal number of DIMMs in each module (except when only four DIMMs are used, then all four DIMMs must be in the primary module - Module 1)
- All DIMMs on a module must be identical in size and speed
- DIMM sizes may differ between memory modules in the dual memory module configuration

The memory module contains the RAS/CAS generator (RCG) and multiplexor (MUX) components of the 450NX PCIset.  Each memory module (alone) can provide a peak bandwidth of 800 MB/s.  In order to achieve the maximum system memory bandwidth (1.067 GB/s peak), both memory modules must be installed and must contain at least two 4:1 interleaved banks per module (i.e., 16 DIMM's).

The memory module also supports the A450NX server management architecture by providing nonvolatile storage of module and server management data and digital I/O hardware for determination of the installed DIMM types.  See Chapter 2 for more details about the memory module.

## 1.1.1.5    Front-side Bus Terminator Module

The front-side bus (FSB) terminator module provides the necessary electrical termination for the processor's front-side advanced gunning transceiver logic + ( AGTL+) bus.  The FSB terminator module is used if a processor is not installed into one of the processor slots.  The FSB terminator module may also be used to terminate the cluster slot when using the 5-slot CPU baseboard.  All processor slots must contain either a processor or an FSB terminator module for the bus to operate correctly.  Similarly, on the 5-slot CPU baseboard, the cluster slot must have either a cluster card, which provides the proper bus termination, or an FSB terminator module installed.

The memory module supports the AD450NX server management architecture by providing nonvolatile storage of module and server management data.  See Chapter 2 for more details about the FSB terminator module.

## 1.1.2    I/O Bus Support

## 1.1.2.1    PCI Bus

The A450NX board set provides three PCI peer buses; two 32-bit segments and one 64-bit segment.  There are a total of six 32-bit PCI slots and five 64-bit slots.  All three PCI buses are 5 V (with support for both 5 V and 3.3 V signaling), 33 MHz and compliant to the *PCI Local Bus Specification, Rev 2.1*.  The PCI buses are operated synchronously with the processor bus, using the processor bus clock as a master clock.  The input clock, received over the F16 interface, is divided by three to support the 33 MHz PCI bus.  The board set will support PCI adapters

that draw power from both 3.3 V and 5 V (signaling), although the power allocation from 3.3 V may be limited. Note that the 64-bit slots will accept both 32 and 64-bit adapters.

## 1.1.2.2    ISA Bus

The Intel® 82371AB PCI to ISA/IDE Accelerator (PIIX4E) component provides the bridge interconnect from the primary 32-bit PCI bus to an ISA bus.  The PIIX4E also provides two IDE channels as well as the Universal Serial Bus (USB) interface.  The ISA bus contains one slot, which is shared with the first PCI slot on the primary 32-bit PCI bus.  Also on the ISA bus are the BIOS flash component, the SMC Super I/O component and the main A450NX board set server management controller.  The SMC Super I/O component provides all legacy connections including keyboard, mouse, floppy disk controller, one parallel port and two serial ports.  The server management interface chip (SMIC) and the baseboard server management controller (BMC) are the heart of the A450NX board set's server management functionality.  The SMIC is implemented with the programmable logic device (PLD), while the BMC is implemented with an 80C652* microcontroller.  The SMIC actually resides on the ISA bus, while the BMC is located behind the SMIC.

## 1.1.3    DSM Cluster Connector Support

The 5-slot CPU baseboard has a fifth slot on the processor bus that allows a DSM cluster controller to be installed. Due to the complexity of designing a cluster controller, and Intel's limited ability to support such efforts, this slot may **not** be used for clustering applications, and must have an FSB terminator module installed at all times. However, a limited number of OEMs are designing a cluster controller specifically for the A450NX board set.

**Note:**    The Intel® AD450NX Server System chassis, which is specifically designed for the A450NX board set, supports only the 4-slot CPU baseboard.  It does not support the 5-slot CPU baseboard and, hence, does not support the installation of a cluster card.

# 1.2    Component Details

## 1.2.1    Microprocessor

The A450NX board set supports 1 to 4 slot-2 generation processors.  The slot 2 processor is packaged in a 330-pin single-edge connector cartridge (SECC), and contains a processor core, L2 cache components, and miscellaneous other components mounted to a fiberglass substrate.  The substrate is then mounted to a cartridge, which includes a heat plate to which a heat sink is attached for heat dissipation.

Initial production will use the Pentium II Xeon processor .  The Pentium II Xeon processor is the next generation of Intel architecture processors following the Pentium® II processor.  The internal architecture of the Pentium II Xeon processor core is similar to that of the Pentium II processor (super scalar, super pipelined, speculative execution, 16KB L1 instruction cache, a 16KB data cache, and MMX™ technology).

Unlike the Pentium II processor, the Pentium II Xeon processor has a full speed (core frequency) interface between the processor core and the L2 cache.  Also, the Pentium II Xeon processor supports either 512K, 1 MB or 2 MB L2 caches.

Initial processor core frequencies are targeted at 400 MHz and will increase in 50 MHz increments.  The CPU baseboard has jumpers allowing the installation of processor frequencies ranging from 300 MHz to 650 MHz in 50 MHz increments.  There will be limitations as to which processor frequencies will be supported.  All processors in the system must be running at the same frequency and with the same size L2 cache.  Also, mixed processor steppings will be supported on a limited basis.

It is also planned that the A450NX board set will support the next generation of the Pentium II Xeon processor.

# 1.2.2    450NX PCIset

The A450NX board set is based on the Intel® 450NX PCIset.  The 450NX is optimized for server platforms and offers the following features not found on previous Intel chip sets.

- Support for greater than 4 GB of memory addressing (36-bit addressing)
- Support for greater than two PCI peer buses
- 64-bit PCI bus support

In addition, the I/O performance of the 450NX has been increased from previous chip sets.

- 100 MHz front-side bus frequency with a peak bandwidth of 800 MB/s
- Dedicated 100 MHz memory bus with a peak bandwidth of 1.067 GB/s
- Two dedicated I/O buses (F16 buses) each with a peak bandwidth of 400 MB/s

The 450NX PCIset is comprised of four unique components; there are nine components over all.

- One memory and I/O component (MIOC), located on the CPU baseboard
- Two PCI eXpansion bus (PXB) components, both located on the I/O baseboard
- Two RAS/CAS generators (RCG), one located on each memory module
- Four data path multiplexors (MUX), two located on each memory module

## 1.2.2.1    MIOC

The memory & I/O component (MIOC) is packaged in a 540-pin ball grid array (BGA) package.  The MIOC provides the interface between the processor bus, the memory bus and both of the F16 I/O buses.  The MIOC dissipates 13-14 W and will be shipped with a heat sink.

## 1.2.2.2    PXB

The PCI eXpansion bridge (PXB) component is packaged in a 540-pin BGA package.  It provides the interface between the F16 I/O bus and the PCI buses.  The PXB can be configured to provide either two 32-bit PCI buses, or a single 64-bit PCI bus.  Two PXBs are located on the I/O baseboard.  One of them, PXB-0, is configured to provide the primary (compatibility) and secondary 32-bit PCI buses.  The other, PXB-1, is configured to provide a single 64-bit PCI bus.  Each PXB dissipates 7-8 W and will be shipped with a heat sink.

## 1.2.2.3    RCG

The RAS/CAS generator (RCG) is packaged in a 324-pin BGA package.  It drives the RAS, CAS address and Write Enable signals to the DRAM array.  One RCG component is located on each memory module.  The RCG dissipates 2 W and does not need a heat sink.

## 1.2.2.4    MUX

The data path multiplexor (MUX) component is packaged in a 324-pin BGA package.  It drives and receives the data to and from the DRAM array.  Two MUX components are located on each memory module.  The MUX dissipates 2.5 W and does not need a heat sink.

# 1.2.3    PID

The programmable interrupt device (PID) is an Enterprise Server Group/Intel® ASIC designed specifically for the A450NX board set and is not available as a stand alone component.  The PID provides interrupt steering functions (including support logic for use with the 8259A interrupt controllers in the PIIX4E) and I/O APIC facilities.  In

addition to the standard IRQs, the PID supports a large number of PCI and onboard interrupt sources; a total of 64 interrupt routing table entries are available.  A separate interrupt input is provided for each of the four interrupts from every 64-bit PCI slot on the I/O baseboard.  Separate INTA and INTB connections are provided from every 32-bit PCI slot, but INTC and INTD are bused (in a rotating pattern) from the slots on the 32-bit PCI segments; separate bused connections are provided for each 32-bit PCI segment.  The PID is packaged in a 256-pin BGA package.

# 1.3　Performance

The core of the A450NX board set is the Pentium II Xeon processor and the Intel 450NX PCIset.  Table 1-1 shows the capabilities of each of the major buses on A450NX.  The values shown are peak bandwidth capable on the bus.  Actual sustained bandwidth will be lower and will vary with the configuration of the server (i.e., adapter cards, operating system, etc.) and the application(s) being run.

*Table 1-1.　　Peak Bus Bandwidth*

| Bus | Frequency | Bus Width | Peak Band Width | Signaling Technology |
|---|---|---|---|---|
| Processor | 100 MHz[1] | 72-bits | 800 MB/s | AGTL+ |
| Memory[2] | 100 MHz | 72-bits | 1.067 MB/s[3] | AGTL+ |
| F16 (each)[2] | 100 MHz | 16-bits | 400 MB/s | AGTL+ |
| PCI-64 | 33 MHz | 64-bits | 266 MB/s | TTL/LV-TTL |
| PCI-32 (each) | 33 MHz | 32-bits | 133 MB/s | TTL/LV-TTL |

Notes:　**1.**　The maximum frequency of the processor bus on the 5-slot CPU baseboard is 90 MHz, when the cluster connector is populated with a cluster card.

　　　　**2.**　Bus drives data on both edges of the clock.

　　　　**3.**　1.067 GB/s bandwidth is with two memory modules installed and populated with at least 8 DIMMs in each module. Maximum bandwidth with only one memory module populated is 800 MB/s.

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# 2. Board Set Details

This chapter describes the functionality of the individual boards that make up the A450NX server system board set, showing their functional blocks and board layouts. The A450NX board set consists of the I/O baseboard, the CPU baseboard, the memory module, the memory terminator module, the I/O riser card, the front-side bus terminator module, and the interconnect backplane make up the A450NX server board set.

# 2.1   I/O Baseboard

This section describes the features of the A450NX I/O baseboard.  The I/O baseboard and the CPU baseboard are connected through the A450NX interconnect backplane.  The A450NX I/O baseboard contains all I/O interfaces for the A450NX server board set.

## Features

The  has the following features:

- Three functionally independent PCI buses
- Integrated Adaptec AIC-7880* SCSI controller (peripheral devices only [CD-ROM, tape drive, etc.])
- Integrated IDE controller supporting two IDE buses
- Onboard video, serial, parallel, Universal Serial Bus (USB)
- Five 32-bit PCI slots
- Five 64-bit PCI slots
- One shared ISA/32-bit PCI slot
- $I^2C$ server management interface

**Note:**   Except for the AIC-7880 controller mentioned above, which is intended for use with devices that are typically located in the 5.25" peripheral device bay (CD-ROMs, tape drives, etc.), mass storage controllers are not integrated onto the I/O baseboard.  Adapter cards are expected to be utilized for this purpose.

## 2.1.1   Block Diagram

Figure 2-1 illustrates the general architecture of the A450NX I/O baseboard.
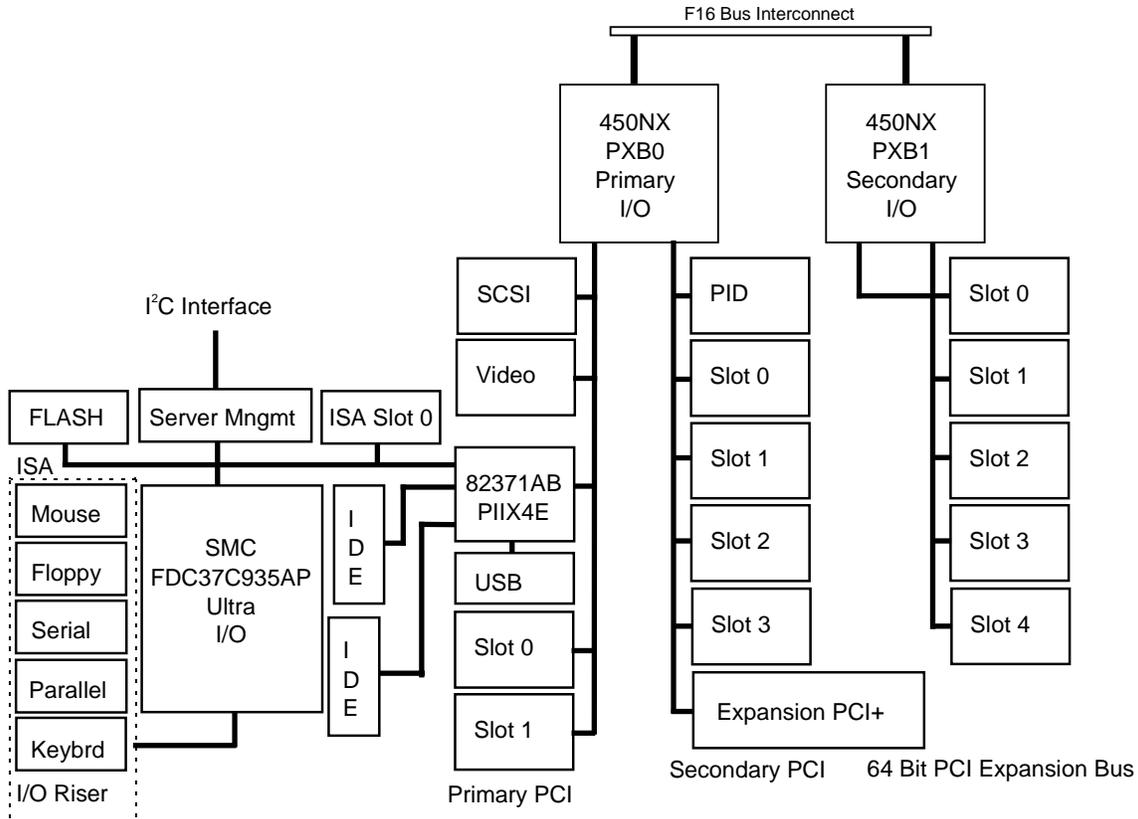


*Figure 2-1.      A450NX I/O Baseboard Block Diagram*

The A450NX I/O baseboard provides the primary input/output interface of the A450NX board set.  The board interfaces with the A450NX CPU baseboard by means of the interconnect backplane.

## 2.1.2   I/O Riser Card

In order to conserve space on the , many legacy connections have been moved to a riser card attached to the baseboard.  Connections to the video, keyboard, mouse, COM ports, parallel port, and ICMB interface are all provided through the I/O riser card.

## 2.1.3   Component Placement Diagrams

Figure 2-2 and Figure 2-3 are diagrams generated from the actual layout database.  They show the primary components of the I/O baseboard and the I/O riser card, as well as the position of the components on the printed circuit board.  The table following each figure, Table 2-1 and Table 2-2 respectively, identifies the major components using the reference designators to locate items in the plot.

*Figure 2-2.    I/O Baseboard Placement Plot*

*Table 2-1.     Major Component Reference (I/O Baseboard)*

| Reference Designator | Name and Description |
|---|---|
| J1A1 | USB Connector |
| J2A1 | ISA Connector |
| J1B1 | I/O Riser Card Connector |
| P1–P2 | Primary 32-bit PCI Slots |
| P3–P6 | Secondary 32-bit PCI slots |
| P7–P11 | 64-bit PCI slots |
| J3D1 | In-system Programming (Used to program the SIMC and PCI error PAL. Used by Intel for test purposes only.  Will be removed on future revision of production boards.) |
| J2E1 | Front Panel Connector |
| J1F1 | IDE Connector:  Primary Channel |
| J1F2 | Floppy Disk Drive Connector |
| J2F1 | Server Management Feature Connector |
| J1H1 | IDE Connector:  Secondary Channel |
| J1H2 | SCSI Connector (for peripheral devices) |
| J2H1–J2H2 | Auxiliary IPMB Connectors |
| J3H1 | Configuration Jumper Block |
| J6G1 | Custom OEM Connector (not for general use - will be removed on future revision of production boards.) |
| J7G2 | In-system Programming Connector (Used to program the BMC control PAL.  Used by Intel for test purposes only.  Will be removed on future revision of production boards.) |
| U1B1 | 2 MB BIOS Flash Device |
| U1C1, U1D1, U1D2, U1E1 | 2 MB Video DRAM |
| U3D1 | Cirrus Logic GD5446* VGA Controller |
| U2J2 | Adaptec AIC-7880* Ultra/Wide SCSI Controller |
| U2E2 | SMC Ultra I/O* Component |
| U3G2 | PIIX4E, PCI to ISA Bridge Device |
| U5E1 | SMIC (Server Management Interface Chip) |
| U4F1 | BMC (Baseboard Management Controller) |
| U5F2 | Flash to hold the BMC code.  32KBx8 (or 64KBx8), socketed device |
| U5F4 | 32KBx8 RAM for BMC |
| U4D1 | PID (Programmable Interrupt Device) |
| U5J1 | PXB-0  (PCI Bus Expander for the 32-bit PCI buses) |
| U7J1 | PXB-1  (PCI Bus Expander for the 64-bit PCI bus) |
| B7G1 | Battery |
| J2J1 | Interconnect Power Module Block |
| J5J1 | Interconnect Signal Module Block |
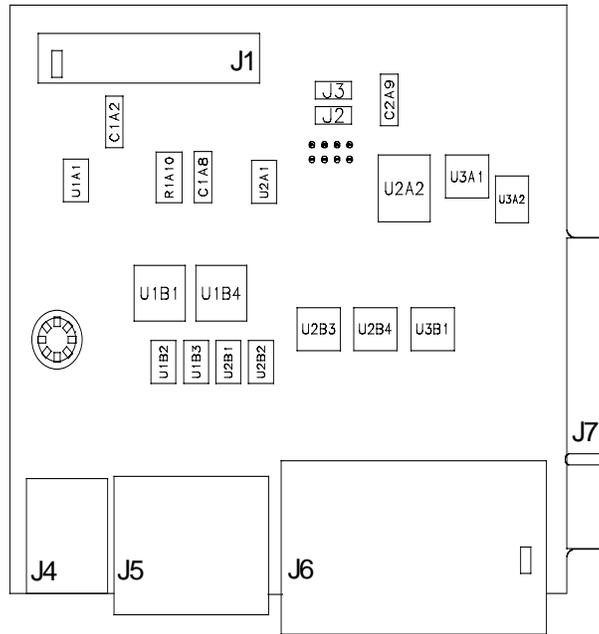
*Figure 2-3.    I/O Riser Card Placement Plot*


*Table 2-2.    Major Component Reference (I/O Riser Card)*

| Reference Designator | Name and Description |
|---|---|
| J1 | ICMB Connector |
| J4 | Combined Mouse and Serial Connector |
| J5 | COM 1 & COM 2 Serial Port Connectors |
| J6 | Combined Paralleled and Video Connector |
| J7 | Edge Connector -- Plugs into connector J3 on I/O baseboard |

# 2.1.4   Functional Architecture

The I/O baseboard design is partitioned into five functional blocks:

- F16 (Expander) Bus Interface
- Primary 32-bit PCI Bus
- Secondary 32-bit PCI Bus
- 64-bit PCI Bus
- System Management Logic

The functional block for the A450NX I/O baseboard is shown in Figure 2-1.  This section provides the operational details of each functional block.

## 2.1.4.1    F16 Bus Interface

The F16 bus, a proprietary, high speed bus, connects each of the two PCI expander bridges (PXBs) with the memory I/O controller (MIOC), which is located on the A450NX CPU baseboard.  For reliability, the bus is parity protected.

Operating at 100 MHz and transferring data on both the rising and falling clock edges, each F16 bus is capable of transfers at a peak data rate of 400 MB/s, which is more than sufficient to sustain the full bandwidth required by two PCI buses.

The A450NX I/O baseboard utilizes two F16 bus interfaces when communicating with the A450NX CPU baseboard.

## 2.1.4.2    Intel® 82450NX PCI Bridge (PXB)

Two PXB components reside on the A450NX I/O baseboard.  Each PXB supports 5 V, 33 MHz, *PCI Rev 2.1* compliant interfaces.  One of the components is configured to drive two 32-bit buses, while a second PXB component is configured to support a single, dedicated, 64-bit PCI interface.

The PCI buses are operated synchronously with the processor bus, using the processor bus clock as a master clock. The PCI input clock, received over the F16 bus interface, is divided by three to support the 33-MHz PCI bus.

The PXB supports all transactions defined for the *PCI Rev 2.1* bus, except that cache coherency is not supported, either between PCI devices or between the PCI and processor buses.

## 2.1.4.3    Primary 32-bit PCI Bus

Conforming to the *Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1 (PCI, Rev. 2.1)*, the primary 32-bit PCI bus is configured on the baseboard with the necessary devices to boot the operating system. The Intel® 82371AB PCI to ISA/IDE Accelerator (PIIX4E) component provides the bridge for interconnect to ISA devices, as well as the Universal Serial Bus interface.  The boot flash ROM is directly connected to the ISA bus and under control of the PIIX4E.

An Adaptec AIC-7880 Ultra-SCSI* chip provides a 16-bit, high speed, SCSI interface for peripheral devices (CD-ROMs, tape drives, etc.).  This high performance adapter is capable of providing data rates of up to 40 MB/s in 16-bit operations to ensure maximum data throughput while minimizing PCI bus overhead.  To ensure data integrity at high speeds, the AIC-7880 has an advanced SCSI I/O cell that automatically and continuously adjusts the slew rate on the REQ, ACK, parity, and data pins to compensate for variations in SCSI cable loading.

Onboard video is supplied by a Cirrus Logic GD5446* PCI video controller with 2 MB of onboard video DRAM. The CL-GD5446 VisualMedia accelerator is a 64-bit DRAM based SVGA controller with hardware-accelerated BitBLT*, video playback, and video capture to the frame buffer.  It combines the Cirrus Logic V-Port* with a multiformat frame buffer for cost effective video playback.  The onboard video also features a 64-bit GUI BitBLT engine with double-buffered, memory-mapped control registers.

The system management logic is also connected to this bus indirectly through the ISA bus.

This bus provides two, full length, 32-bit expansion slots (identified as P1 and P2).  One slot is shared with the ISA expansion slot.

When external PCI video adapters are added, they should be added to the primary 32-bit PCI bus.  When detected, the BIOS automatically disables the onboard Cirrus Logic GD5446 video controller.

A brief overview of the primary components connected to the primary 32-bit PCI bus is provided in the following sections.

### 2.1.4.3.1    Adaptec AIC-7880* SCSI Controller

A single Adaptec AIC-7880 SCSI chip provides an embedded SCSI controller on the primary 32-bit PCI bus.  The configuration registers define PCI-related parameters for the AIC-7880 device.  The AIC-7880 supports all mandatory registers in the PCI configuration space header, including the vendor ID, device ID, class code, revision ID, header type, and command and status fields.

The AIC-7880 is intended for control of peripheral devices only and not for mass storage (with the possible exception of a single boot drive). The AIC-7880 should be used for tape drives, CD-ROM's, DVD devices, etc. It can be configured for either Fast/Wide or Ultra SCSI mode. System level mass storage control should be provided via add-in adapter cards.

SCSI configuration registers are accessed as 32-bit (DWORD) quantities. For example, the Status register (06H - 07H) is the high word and the Command register (04H - 05H) is the low word of a DWORD access.

## 2.1.4.3.2    Cirrus Logic GD5446* PCI Video Controller

The Cirrus Logic GD5446 PCI video controller is connected to the primary 32-bit PCI bus and is used to provide onboard VGA capability to the A450NX I/O baseboard. The CL-GD5446 includes a glueless 32-bit PCI bus interface. This interface features full PCI compliance, including optimized PCI burst write, which supports PCI writes to the frame buffer at greater than 55 MB/s.

The frame buffer is addressable through a 16-MB window consisting of three 4-MB, byte-swapping apertures, and a special video aperture. The VGA control registers are relocatable anywhere in the 64KB space (allowing multiple devices in a single system).

The CL-GD5446 is automatically disabled by BIOS, if a video adapter is detected on the primary 32-bit PCI bus expansion slots.

### 2.1.4.3.2.1    Video Modes

The CL-GD5446 provides all standard IBM* VGA modes. Table 2-3 and Table 2-4 show all supported video modes.

Table 2-3.      Standard VGA Modes

| Modes Hex | Colors | Char. x Row | Char. Cell | Screen Format | Display Mode | Pixel Freq. (MHz) | Horiz. Freq. (KHz) | Vert. Freq. (Hz) |
|-----------|--------|-------------|------------|---------------|--------------|-------------------|--------------------|------------------|
| 0, 1 | 16/256KB | 40 x 25 | 9 x 16 | 360 X 400 | Text | 14 | 31.5 | 70 |
| 2, 3 | 16/256KB | 80 x 25 | 9 x 16 | 720 X 400 | Text | 28 | 31.5 | 70 |
| 4, 5 | 4/256KB | 40 x 25 | 8 x 8 | 320 X 200 | Graphics | 12.5 | 31.5 | 70 |
| 6 | 2/256KB | 80 x 25 | 8 x 8 | 640 X 200 | Graphics | 25 | 31.5 | 70 |
| 7 | Mono | 80 x 25 | 9 x 16 | 720 X 400 | Text | 28 | 31.5 | 70 |
| D | 16/256KB | 40 x 25 | 8 x 8 | 320 X 200 | Graphics | 12.5 | 31.5 | 70 |
| E | 16/256KB | 80 x 25 | 8 x 14 | 640 X 200 | Graphics | 25 | 31.5 | 70 |
| F | Mono | 80 x 25 | 8 x 14 | 640 X 350 | Graphics | 25 | 31.5 | 70 |
| 10 | 16/256KB | 80 x 25 | 8 x 14 | 640 X 350 | Graphics | 25 | 31.5 | 70 |
| 11 | 2/256KB | 80 x 30 | 8 x 16 | 640 X 480 | Graphics | 25 | 31.5 | 60 |
| 11+ | 2/256KB | 80 x 30 | 8 x 16 | 640 X 480 | Graphics | 31.5 | 37.9 | 72 |
| 11+ | 2/256KB | 80 x 30 | 8 x 16 | 640 X 480 | Graphics | 31.5 | 37.5 | 75 |
| 12 | 16/256KB | 80 x 30 | 8 x 16 | 640 X 480 | Graphics | 25 | 31.5 | 60 |
| 12+ | 16/256KB | 80 x 30 | 8 x 16 | 640 X 480 | Graphics | 31.5 | 37.9 | 72 |
| 12+ | 16/256KB | 80 x 30 | 8 x 16 | 640 X 480 | Graphics | 31.5 | 37.5 | 75 |
| 12+ | 16/256KB | 80 x 30 | 8 x 16 | 640 X 480 | Graphics | 35.8 | 43.3 | 85 |
| 13 | 256/256KB | 40 x 25 | 8 x 8 | 320 X 200 | Graphics | 12.5 | 31.5 | 70 |

*Table 2-4:    Extended VGA Modes*

| Mode(s) in Hex | Colors | Char x Row | Char Cell | Screen Format | Pixel Freq. (MHz) | Horiz. Freq. (KHz) | Vert. Freq. (Hz) |
|---|---|---|---|---|---|---|---|
| 58, 6A | 16/256KB | 100 x 37 | | 800 X 600 | 36 | 35.2 | 56 |
| 58, 6A | 16/256KB | 100 x 37 | | 800 X 600 | 40 | 37.8 | 60 |
| 58, 6A | 16/256KB | 100 x 37 | | 800 X 600 | 50 | 48.1 | 72 |
| 58, 6A | 16/256KB | 100 x 37 | | 800 X 600 | 49.5 | 46.9 | 75 |
| 5C | 256/256KB | 100 x 37 | | 800 X 600 | 36 | 35.2 | 56 |
| 5C | 256/256KB | 100 x 37 | | 800 X 600 | 40 | 37.9 | 60 |
| 5C | 256/256KB | 100 x 37 | | 800 X 600 | 50 | 48.1 | 72 |
| 5C | 256/256KB | 100 x 37 | | 800 X 600 | 49.5 | 46.9 | 75 |
| 5C | 256/256KB | 100 x 37 | | 800 X 600 | 56.25 | 53.7 | 85 |
| 5D[†] | 16/256KB | 128 x 48 | | 1024 X 768 | 44.9 | 35.5 | 43 |
| 5D | 16/256KB | 128 x 48 | | 1024 X 768 | 65 | 48.3 | 60 |
| 5D | 16/256KB | 128 x 48 | | 1024 X 768 | 75 | 56 | 70 |
| 5D[†] | 16/256KB | 128 x 48 | | 1024 X 768 | 77 | 58 | 72 |
| 5D | 16/256KB | 128 x 48 | | 1024 X 768 | 78.5 | 60 | 75 |
| 5E | 256/256KB | 80 x 25 | | 640 x 400 | 25 | 31.5 | 70 |
| 5F | 256/256KB | 80 x 30 | | 640 X 480 | 25 | 31.5 | 60 |
| 5F | 256/256KB | 80 x 30 | | 640 X 480 | 31.5 | 37.9 | 72 |
| 5F | 256/256KB | 80 x 30 | | 640 X 480 | 31.5 | 37.5 | 75 |
| 5F | 256/256KB | 80 x 30 | | 640 X 480 | 36 | 43.3 | 85 |
| 65 | 64KB | - | - | 800 X 600 | 36 | 35.2 | 56 |
| 65 | 64KB | - | - | 800 X 600 | 40 | 37.8 | 60 |
| 65 | 64KB | - | - | 800 X 600 | 50 | 48.1 | 72 |
| 65 | 64KB | - | - | 800 X 600 | 49.5 | 46.9 | 75 |
| 65 | 64KB | - | - | 800 X 600 | 56.25 | 53.7 | 85 |
| 66 | 32KB[‡] | - | - | 640 X 480 | 25 | 31.5 | 60 |
| 66 | 32KB[‡] | - | - | 640 X 480 | 31.5 | 37.9 | 72 |
| 66 | 32KB[‡] | - | - | 640 X 480 | 31.5 | 37.5 | 75 |
| 66 | 32KB[‡] | - | - | 640 X 480 | 36 | 43.3 | 85 |
| 67 | 32KB[‡] | - | - | 800 X 600 | 36 | 35.2 | 56 |
| 67 | 32KB[‡] | - | - | 800 X 600 | 40 | 37.8 | 60 |
| 67 | 32KB[‡] | - | - | 800 X 600 | 50 | 48.1 | 72 |
| 67 | 32KB[‡] | - | - | 800 X 600 | 49.5 | 46.9 | 75 |
| 67 | 32KB[‡] | - | - | 800 X 600 | 56.25 | 53.7 | 85 |
| 68 | 32KB[‡] | - | - | 1024 x 768 | 44.9 | 35.5 | 43 |
| 68 | 32KB[‡] | - | - | 1024 x 768 | 65 | 48.3 | 60 |
| 68 | 32KB[‡] | - | - | 1024 x 768 | 75 | 56 | 70 |
| 68 | 32KB[‡] | - | - | 1024 x 768 | 78.7 | 60 | 75 |
| 68 | 32KB[‡] | - | - | 1024 x 768 | 94.5 | 68.3 | 85 |
| 69[†] | 32KB[‡] | - | - | 1280 x 1024 | 75 | 48 | 43 |

| Mode(s) in Hex | Colors | Char x Row | Char Cell | Screen Format | Pixel Freq. (MHz) | Horiz. Freq. (KHz) | Vert. Freq. (Hz) |
|---|---|---|---|---|---|---|---|
| 69[†] | 32KB[‡] | - | - | 1280 x 1024 | 108 | 65 | 60 |
| 6C[†] | 16/256KB | 160 x 64 | 8 x 16 | 1280 X 1024 | 75 | 48 | 43 |
| 6D[†] | 256/256KB | 160 x 64 | 8 x 16 | 1280 X 1024 | 75 | 48 | 43 |
| 6D | 256/256KB | 160 x 64 | 8 x 16 | 1280 X 1024 | 108 | 65 | 60 |
| 6D | 256/256KB | 160 x 64 | 8 x 16 | 1280 X 1024 | 126 | 76 | 71.2 |
| 6D | 256/256KB | 160 x 64 | 8 x 16 | 1280 X 1024 | 135 | 80 | 75 |
| 71 | 16M | - | - | 640 X 480 | 25 | 31.5 | 60 |
| 71 | 16M | - | - | 640 X 480 | 31.5 | 37.9 | 72 |
| 71 | 16M | - | - | 640 X 480 | 31.5 | 37.5 | 75 |
| 71 | 16M | - | - | 640 X 480 | 36 | 43.3 | 85 |
| 74[†] | 64KB[†] | - | - | 1024 X 768 | 44.9 | 35.5 | 43 |
| 74 | 64KB | - | - | 1024 X 768 | 65 | 48.3 | 60 |
| 74 | 64KB | - | - | 1024 X 768 | 75 | 56 | 70 |
| 74 | 64KB | - | - | 1024 X 768 | 78.7 | 60 | 75 |
| 74 | 64KB | - | - | 1024 X 768 | 94.5 | 68.3 | 85 |
| 75[†] | 64KB[†] | - | - | 1280 X 1024 | 75 | 48 | 43 |
| 78 | 16M | - | - | 800 x 600 | 36 | 35.2 | 56 |
| 78 | 16M | - | - | 800 x 600 | 40 | 37.8 | 60 |
| 78 | 16M | - | - | 800 x 600 | 50 | 48.1 | 72 |
| 78 | 16M | - | - | 800 x 600 | 49.5 | 46.9 | 75 |
| 78 | 16M | - | - | 800 x 600 | 56.25 | 53.7 | 85 |
| 79 | 16M | - | - | 800 x 600 | 44.9 | 35.5 | 43 |
| 79 | 16M | - | - | 1024 x 768 | 65 | 483 | 60 |
| 79 | 16M | - | - | 1024 x 768 | 75 | 56 | 70 |
| 79 | 16M | - | - | 1024 x 768 | 78.7 | 60 | 75 |
| 79 | 16M | - | - | 1024 x 768 | 94.5 | 68.3 | 85 |
| 7C | 256/256KB | 144 x 54 | 8 x 16 | 1152 x 864 | 94.5 | 63.9 | 70 |
| 7C | 256/256KB | 144 x 54 | 8 x 16 | 1152 x 864 | 108 | 67.5 | 75 |
| 7D | 64KB | - | - | 1152 x 864 | 94.5 | 63.9 | 70 |
| 7D | 64KB | - | - | 1152 x 864 | 94.5 | 67.5 | 75 |

† Indicates Interlaced Mode

‡ Indicates 32KB Direct-Color/256-Color Mixed Mode

## 2.1.4.3.3     Expansion Slots

Two standard 32-bit PCI expansion slots are user accessible on the primary PCI bus.  These slots compete for access to the bus along with the other components mounted to the bus.

## 2.1.4.3.4     Intel® 82371AB PCI to ISA/IDE Accelerator

The Intel® 82371AB PCI to ISA/IDE Accelerator (PIIX4E) component provides the bridge for interconnect to ISA devices and two IDE channels, as well as the USB interface.

### 2.1.4.3.5 Universal Serial Bus (USB)

The I/O baseboard's PIIX4E also provides the capability for two USB channels. The board set provides support for the USB bus, but does so with limitations. These limitations are done to help ensure that the physical security measures, which are expected on server platforms, are in place. Without these use limitations, the USB might otherwise be used to gain unauthorized access to the system (e.g., via USB keyboard), even though the BIOS is set up to operate in secure mode. Supported use of the USB is discussed below.

- Intel will not support legacy mode for USB devices (i.e., any and all USB devices will be functional only after a USB-aware operating system is up and running and has loaded the appropriate USB driver. This means USB devices will not be functional during the Power-on Self Test (POST)).

- Primary use of USB will be for nonhuman input devices (e.g., modems, backup storage devices, etc.). Human input devices will not be supported and will not be validated by Intel. (i.e., Intel will not validate or guarantee that human input devices such as keyboards, mice, joysticks, etc., work.) However, Intel will not do anything to preclude operation of these devices, they simply will not be validated.

- USB will be supported only with USB-aware operating systems (e.g., NT 5.0).

## 2.1.4.4 ISA Bus

The ISA bus provides a single ISA slot, which is physically shared with the first PCI slot on the primary 32-bit PCI bus (P1). The BIOS device, SMC Ultra I/O* controller and the SMIC are also located on the ISA bus.

### 2.1.4.4.1 SMC FDC37C937APM* Ultra I/O Controller

The SMC FDC37C937APM* incorporates the following:components:

- keyboard interface
- real-time clock
- SMC's true CMOS 765B* floppy disk controller (FDC)
- SMC's advanced digital data separator*
- 16 byte data FIFO
- two NS16C550A* compatible universal asynchronous receiver/transmitters (UART)
- one multimode parallel port (includes chip protect circuitry, plus enhanced parallel port (EPP) and enhanced capability port (ECP) support)
- on-chip 24 mA AT bus drivers
- game port chip select
- two-floppy direct-drive-support
- ACCESS bus
- soft power management
- system management interrupt (SMI) support

The true CMOS 765B core provides 100% compatibility with PC/XT* and PC/AT* architectures, in addition to providing data overflow and underflow protection. The SMC advanced digital data separator incorporates SMC's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with National Semiconductor's 16C550 UART. The parallel port, the IDE interface, and the game port select logic are compatible with IBM PC/AT architecture, as well as EPP and ECP. The FDC37C937APM incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C937APM provides features for compliance with the *Advanced Configuration and Power Interface Specification* (ACPI). These features include support of both legacy and ACPI power management models through

the selection of SMI, which is enabled via BIOS.  It implements a 24-bit power management timer, power button override event (4-second button hold to turn off the system), and either rising or falling edge triggered interrupts.

The FDC37C937APM provides support for the *ISA Plug-and-Play Standard (Version 1.0a)*.  Through internal configuration registers, the I/O address of each of the FDC37C937APM's logical devices, the DMA channel, and the IRQ channel may be programmed.  There are 480 I/O address location options, 13 IRQ options, and three DMA channel options for each logical device.  The FDC37C937APM does not require any external filter components and is, therefore, easy to use and offers lower system cost and reduced board area.  The FDC37C937APM is software and register compatible with SMC's proprietary 82077AA* core.

### 2.1.4.4.2    BIOS Flash Device

The onboard BIOS is located in an onboard 2-MB flash device attached directly to the ISA bus.  The device is enabled under the control of the PIIX4E.  The device is accessed in byte-wide mode.  The BIOS can be updated by means of an update utility at boot time by inserting a bootable floppy into the drive that contains the updated BIOS image as well as the update utility software.  The BIOS contains a recovery boot option, which is described in more detail in Chapter 3 of this document.  This jumper configuration forces the BIOS to update without user intervention. A series of beeps indicates the beginning and end of the programming process.

## 2.1.4.5    Secondary 32-bit PCI Bus

The secondary 32-bit PCI bus is also *PCI Rev 2.1*, compliant.  The programmable interrupt device (PID), an Intel designed application specific integrated circuit (ASIC), resides on the secondary 32-bit PCI bus for system interrupt handling.  The PID is an interrupt controller that provides the interrupt steering.  The PID contains the logic required to provide 8259A mode, advanced programmable interrupt controller (APIC) mode, and advanced configuration and power interface (ACPI) functionality.  The PID includes a PCI, APIC, and PIIX4E interface.  The secondary 32-bit PCI bus also contains four, full length, 32-bit user accessible expansion slots (identified as P3, P4, P5 and P6).

**Note:**   Due to architectural limitations of the 450NX PCIset, all expansion video cards must be placed on the primary 32-bit PCI bus.

### 2.1.4.5.1    Programmable Interrupt Device (PID)

The A450NX I/O baseboard incorporates an ASIC referred to as the PID.  The PID is an Intel designed interrupt controller ASIC that provides interrupt steering functions including ISA 8259A, and I/O APIC mode controller operations.  The PID provides up to 15 IRQs and 48 PCI-interrupt inputs.

To minimize the possibility of interrupt conflicts, especially with increased use of multiported adapter cards, the PID provides at least two dedicated interrupts per 32-bit PCI slot and four dedicated interrupts per 64-bit PCI slot.  Table 2-5 summarizes the interrupt mappings.

*Table 2-5.     Interrupt Mappings*

| PID Interrupt | PCI Interrupt | Component/ PCI Slot Number | PCI Bus |
|---|---|---|---|
| 0 | D | P11 | PCI-64 |
| 1 | C | P11 | PCI-64 |
| 2 | B | P11 | PCI-64 |
| 3 | A | P11 | PCI-64 |
| 4 | D | P10 | PCI-64 |
| 5 | C | P10 | PCI-64 |
| 6 | B | P10 | PCI-64 |
| 7 | A | P10 | PCI-64 |
| 8 | D | P9 | PCI-64 |

| PID Interrupt | PCI Interrupt | Component/<br>PCI Slot Number | PCI Bus |
|---|---|---|---|
| 9 | C | P9 | PCI-64 |
| 10 | B | P9 | PCI-64 |
| 11 | A | P9 | PCI-64 |
| 12 | D | P8 | PCI-64 |
| 13 | C | P8 | PCI-64 |
| 14 | B | P8 | PCI-64 |
| 15 | A | P8 | PCI-64 |
| 16 | D | P7 | PCI-64 |
| 17 | C | P7 | PCI-64 |
| 18 | B | P7 | PCI-64 |
| 19 | A | P7 | PCI-64 |
| 20 | A | PXB-1 | PCI-64 |
| 21 | B | P3 | Secondary 32-bit |
| 22 | A | P3 | Secondary 32-bit |
| 23 | B | P4 | Secondary 32-bit |
| 24 | A | P4 | Secondary 32-bit |
| 25 | B | P5 | Secondary 32-bit |
| 26 | A | P5 | Secondary 32-bit |
| 27 | B | P6 | Secondary 32-bit |
| 28 | A | P6 | Secondary 32-bit |
| 29 | C/D/C/D | P3/P4/P5/P6 † | Secondary 32-bit |
| 30 | D/C/D/C | P3/P4/P5/P6 † | Secondary 32-bit |
| 31 | --- | Custom OEM Slot | Secondary 32-bit |
| 32 | --- | Video | Primary 32-bit |
| 33 | D | PIIX4E | Primary 32-bit |
| 34 | --- | PXB-0 | Secondary 32-bit |
| 35 | --- | PXB-0 | Primary 32-bit |
| 36 | C/D | P1/P2 † | Primary 32-bit |
| 37 | D/C | P1/P2 † | Primary 32-bit |
| 38 | B | P1 | Primary 32-bit |
| 39 | A | P1 | Primary 32-bit |
| 40 | B | P2 | Primary 32-bit |
| 41 | A | P2 | Primary 32-bit |
| 42 | --- | On-board SCSI ‡ | Primary 32-bit |
| 43 | 0 | Cluster Bridge | Primary 32-bit |
| 44 | --- | MIOC | --- |
| 45 | Unused | --- | --- |
| 46 | NMI | PIIX4E | --- |
| 47 | Unused | --- | --- |

† Shared Interrupt

‡ Only one interrupt supported

## 2.1.4.6   64-bit PCI Bus

The 64-bit PCI bus provides the user with five full length, *PCI Rev 2.1* compliant, expansion slots on a dedicated high performance bus.  Communication with other system resources is performed through the PXB.

**Notes:**    1.    Both 32-bit and 64-bit PCI adapters may be plugged into the 64-bit slots.  The 32-bit adapters, however, will not take advantage of the extra bandwidth provided by the 64-bit bus.

             2.    Due to architectural limitations of the 450NX PCIset, all expansion video cards must be placed on the primary 32-bit PCI bus.

# 2.1.5   Board Configuration Jumpers

Configuration jumpers exist on the A450NX I/O baseboard to enable the user to recover the BIOS, clear a CMOS password, or clear all CMOS settings.  Positioning of the jumpers as shown in Figure 2-4 provides the default system configuration.  Reserved jumpers may not be populated in shipping configurations.  The default configurations are shown in Table 2-6 in bold face type.  The configuration jumper block is located at J3H1, near PXB-0 and in line with the 32-bit PCI slots (P3 & P4).

```
J3H1  A  B  C
  1  ( ) ( | | ) ( )   Reserved
  2  ( ) ( |███| )      In Circuit Program
  3  ( ) ( |███| )      Flash Programming
  4  ( ) ( | | ) ( )   Reserved
  5  ( ) ( |███| )      Password Clear
  6  ( ) (███| | )      CMOS Clear
  7  ( ) (███| | )      Recovery Boot
  8  ( ) ( ) ( )        Reserved
  9  ( ) ( | | )        In System Program Enable
 10  ( ) ( | | )        Reserved
```
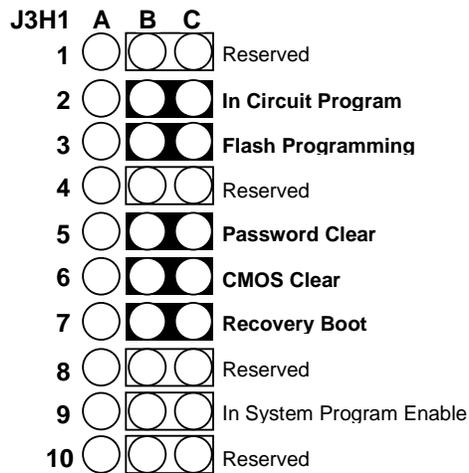
*Figure 2-4.    Configuration Jumper Block (J3H1)*

*Table 2-6.    J3H1 Board Configuration Jumpers*

| Jumper | Function |
|---|---|
| 1(B–C) | Reserved |
| 1(A–B) | Reserved |
| 2(B–C) | **Permits server management to program onboard programmable devices (BMC, FPC, HSC)** |
| 2(A–B) | Do not allow server management to program onboard programmable devices |
| 3(B–C) | **Apply 12 V to programming pins; BIOS setting can be updated (written to)** |
| 3(A–B) | Apply GND to programming pins; write-protect/memory |
| 4(B–C) | Reserved |
| 4(A–B) | Reserved |
| 5(B–C) | **Do not clear CMOS password** |
| 5(A–B) | Clear CMOS password |

| Jumper | Function |
|--------|----------|
| 6(B–C) | **Do not clear CMOS** |
| 6(A–B) | Clear CMOS |
| 7(B–C) | **Normal Boot** (Jumper is REQUIRED for system boot) |
| 7(A–B) | Boot recovery BIOS |
| 8(B–C) | Reserved |
| 8(A–B) | Reserved |
| 9(B–C) | Disable programming of onboard ISP parts |
| 9(A–B) | Enable programming of onboard ISP parts |
| 10(B–C) | Reserved |
| 10(A–B) | Reserved |

**Note: Bold** indicates the default jumper position

## 2.1.6   Boot Order

The I/O baseboard provides the system with a variety of methods for detecting and booting an operating system.  The BIOS scans devices and user configurable option slots in a specific sequence.  Knowing the precise sequence the BIOS will detect, setup, and boot, greatly assists in system definition.  The default boot order is listed below.  However, there are many factors, including user changes to the BIOS setup, which may affect the actual boot order of a particular configuration.  The exact IDSEL numbers are shown in the following table to help in determining the actual boot order.

<u>**Default Boot Order**</u>

- Floppy
- ISA
- IDE (Primary)
- IDE (Secondary)
- Primary 32-Bit PCI Bus
    - ⇒ P1
    - ⇒ Onboard SCSI (AIC-7880)
    - ⇒ P2
- Secondary 32-bit PCI Bus
    - ⇒ P3
    - ⇒ P4
    - ⇒ P5
    - ⇒ P6
- 64-bit PCI Bus
    - ⇒ P7
    - ⇒ P8
    - ⇒ P9
    - ⇒ P10
    - ⇒ P11

*Table 2-7.      Device Configuration Order*

| Location | Bus | IDSEL | Comment |
|---|---|---|---|
| J1F2 | ISA | None | Floppy Drive |
| J2A1 | ISA | None | Compatibility (Legacy) Boot Slot 1 [†] |
| J1F1 | IDE | None | Primary IDE |
| J1H1 | IDE | None | Secondary IDE |
| P1 | Primary PCI | 25 | Expansion Slot [†] |
| J1H2 | Primary PCI | 26 | Onboard SCSI |
| P2 | Primary PCI | 27 | Expansion Slot [†] |
| U3D1 | Primary PCI | 28 | Onboard Video |
| U3G2 | Primary PCI | 31 | PIIX4E Component |
| P3 | Secondary PCI | 20 | Expansion Slot |
| P4 | Secondary PCI | 21 | Expansion Slot |
| P5 | Secondary PCI | 22 | Expansion Slot |
| P6 | Secondary PCI | 23 | Expansion Slot |
| U4D1 | Secondary PCI | 25 | PID Component |
| P7 | 64 Bit PCI | 20 | Expansion Slot |
| P8 | 64 Bit PCI | 21 | Expansion Slot |
| P9 | 64 Bit PCI | 22 | Expansion Slot |
| P10 | 64 Bit PCI | 23 | Expansion Slot |
| P11 | 64 Bit PCI | 24 | Expansion Slot |

[†] User supplied video adapters may be installed only in P1,P2 or ISA slots.

## 2.1.7   Server Management

The heart of server management is the baseboard management controller (BMC).  External communication can be established with the BMC through the SMIC.  The server management logic maintains a system event log (SEL) to store important system information.  System voltage levels are monitored by the server management logic.  Also included in the A450NX server management module are hardware hooks to perform in-system programming (ISP) of the system programmable logic.

The server management logic also provides monitoring or control of other system devices including video, floppy disks, chassis fans, and BIOS flash.

### 2.1.7.1   Memory Map

This section contains a server management device map and an I/O memory map.

*Table 2-8.      Server Management Device Maps*

| FUNCTION | ADDRESS RANGE | ACCESS | Width |
|---|---|---|---|
| I/O Board A/D converter | SPI Bus | | |
| CPU Board A/D converter | SPI Bus | | |
| SMIC | FC00 - FFFF | See SMIC section | Byte |
| Output Latch #1 | F800 - FBFF | Write | Byte |

| FUNCTION | ADDRESS RANGE | ACCESS | Width |
|---|---|---|---|
| | | (Read RAM Shadow) | |
| Output Latch #0 | F400 - F7FF | Write<br>(Read RAM Shadow) | Byte |
| RAM, Output Latch Shadow | F400 - FBFF | Execute, Read, Write<br>(Shadows Output Lathes) | Byte |
| Input Latch | F000 - F3FF | Read | Byte |
| RAM # 1 | Not assigned | Not defined | Byte |
| RAM # 0 | 8000 - EFFF | Execute, Read, Write | Byte |
| FLASH, OPS | 1000 - 7FFF | Execute, Read, Write | Byte |
| FLASH, BOOT | 0000 - 1000 | Execute, Read | Byte |

Table 2-9 provides a cross-reference between the I/O signals and the individual devices.  These can be referenced against the device maps to resolve the absolute address.

*Table 2-9.    Server Management I/O Memory Map*

| Topic | Signal | Device | Access | Offset | Bit |
|---|---|---|---|---|---|
| Not Applicable | Not Applicable<br>(Muxed Address/Data BUS) | Micro Port 0 | - | - | 0 to 7 |
| SPI Bus | SPI_CLK - Bit 0 | Micro Port 1 | RW | - | 0 |
| SPI Bus | SPI_MISO - Bit 6 | Micro Port 1 | RW | - | 1 |
| SPI Bus | SPI_MOSI - Bit 5 | Micro Port 1 | RW | - | 2 |
| SPI Bus | SPI_SEL_2_L -Bit 3 | Micro Port 1 | RW | - | 3 |
| SPI Bus | SPI_SEL_3_L - Bit 4 | Micro Port 1 | RW | - | 4 |
| Memory | BMC_OP_CLR_L | Micro Port 1 | RW | - | 5 |
| Global I$^2$C Bus | I2C_GLOBAL_SCL | Micro Port 1 | RW | - | 6 |
| Global I$^2$C Bus | I2C_GLOBAL_SDA | Micro Port 1 | RW | - | 7 |
| Not Applicable | Not Applicable<br>(Upper Address Bus) | Micro Port 2 | - | - | 0–7 |
| BMC Private I$^2$C Bus | I2C_BMC_SCL | Micro Port 3 | - | - | 0 |
| BMC Private I$^2$C Bus | I2C_BMC_SDA | Micro Port 3 | - | - | 1 |
| Processor to BMC Interrupt | INTR0_SMIC_L | Micro Port 3 | R | - | 2 |
| Secure Mode | SECURE_MODE_KB_L | Micro Port 3 | R | - | 3 |
| BMC - Processor SMBus | I2C_DS2P_SCL | Micro Port 3 | RW | - | 4 |
| BMC - Processor SMBus | I2C_DS2P_SDA | Micro Port 3 | RW | - | 5 |
| BMC_RD_L | Reserved | Micro Port 3 | - | - | 6 |
| BMC_WR_L | Reserved | Micro Port 3 | - | - | 7 |
| Interrupts | FP_NMI_SWT_L | Input Latch | R | - | 0 |
| In Circuit Logic Programming | ISP_HSBP_SDO | Input Latch | R | - | 1 |
| Not Used | Not Used | Input Latch | R | - | 2 |
| In Circuit Logic Programming | ISP_FPC_SDO | Input Latch | R | - | 3 |
| Memory | BMC_FRC_UPDATE_L | Input Latch | R | - | 4 |
| Keylock | KEYLOCK_FROM_SFC_L | Input Latch | R | - | 5 |

| Topic | Signal | Device | Access | Offset | Bit |
|---|---|---|---|---|---|
| Bios Flash | FLASH_WP_L | Input Latch | R | - | 6 |
| Timer Halt | FRB_TIMER_HALT_L | Input Latch | R | - | 7 |
| Keylock | KEYLOCK_SFC_L | Output Latch # 0 | RW | -- | 0 |
| Fans | FAN_FAILED_L | Output Latch # 0 | RW | - | 1 |
| Interrupts | PX4_EXTSMI_L | Output Latch # 0 | RW | - | 2 |
| Secure Mode | SECURE_MODE_BMC | Output Latch # 0 | RW | - | 3 |
| Floppy Drive | FD_READ_ONLY_L | Output Latch # 0 | RW | - | 4 |
| Video | BLANK_VID | Output Latch # 0 | RW | - | 5 |
| Interrupts | BMC_FP_NMI_L | Output Latch # 0 | RW | - | 6 |
| Output Latches | LATCH_2_EN_L | Output Latch # 0 | RW | - | 7 |
| In Circuit Logic Programming | ISP_SCLK | Output Latch # 1 | RW | -- | 0 |
| In Circuit Logic Programming | ISP_MODE | Output Latch # 1 | RW | - | 1 |
| In Circuit Logic Programming | ISP_EN_L | Output Latch # 1 | RW | - | 2 |
| In Circuit Logic Programming | ISP_EN2_L | Output Latch # 1 | RW | - | 3 |
| In Circuit Logic Programming | ISP_IO_EN_L | Output Latch # 1 | RW | - | 4 |
| In Circuit Logic Programming | ISP_FPC_EN_L | Output Latch # 1 | RW | - | 5 |
| In Circuit Logic Programming | SPI_SEL_0 | Output Latch # 1 | RW | - | 6 |
| In Circuit Logic Programming | SPI_SEL_1 | Output Latch # 1 | RW | - | 7 |
| ISA to BMC Bridge | ISA_BMC_DATA_REG | PLD | - | 0xFF01 | 7..0 |
| ISA to BMC Bridge | ISA_BMC_CTRL_REG | PLD | - | 0xFF02 | 7..0 |
| ISA to BMC Bridge | ISA_BMC_FLAG_REG | PLD | - | 0xFF03 | 7..0 |
| Reset | PROC_RESET_NOW | PLD | R | 0xFF04 | 7 |
| Reset | PROC_RESET_HI_LO | PLD | RW | 0xFF04 | 6 |
| Reset | PROC_RESET_LO_HI | PLD | RW | 0xFF04 | 5 |
| Reset | PWR_GOOD_LAST_RESET | PLD | RW | 0xFF04 | 4 |
| Memory | BMC_A16_PAGE | PLD | RW | 0xFF04 | 3 |
| Reset | FW_FORCE_RST_LATCH | PLD | | 0xFF04 | 2 |
| Reset | RESET_HSBP_L | PLD | RW | 0xFF04 | 1 |
| Reset/Interrupt | BMC_SERR_L | PLD | RW | 0xFF04 | 0 |
| Not Used | Not Used | PLD | | 0xFF05 | 7 |
| Not Used | Not Used | PLD | | 0xFF05 | 6 |
| Not Used | Not Used [Was: SFC_RST_L] | PLD | R | 0xFF05 | 5 |
| Not Used | Not Used [Was: FP_NMI_SWT_L] | PLD | R | 0xFF05 | 4 |
| Memory | FW_BOOT_BLOCK_PGM_EN (from jumper block) | PLD | R | 0xFF05 | 3 |
| Memory | FW_BOOT_BLOCK_PGM_EN_L (from processors) | PLD | R | 0xFF05 | 2 |
| Watchdog | SW_WATCHDOG_EN | PLD | R | 0xFF05 | 1 |
| Watchdog | WDO_307_L | PLD | R | 0xFF05 | 0 |
| Not Used | Not Used | PLD | RW | 0xFF06 | 7.0 |

## 2.1.7.2    System Event Log (Serial EEPROM)

The system event log is implemented with a 128KB serial EEPROM device, Atmel part number AT24C128W*.  In addition to the system event log, the SEEPROM is used to store the board field replaceable unit (FRU) information (as well as system FRU information, when installed into the AD450NX server system chassis).  See Chapter 4 of this document for more details.

## 2.1.7.3    I$^2$C Accessed Features

The I/O baseboard and I/O riser card contain the following I$^2$C accessible devices, which contain FRU information:

- AT24C128*      -  I/O baseboard FRU information
- AT24C02*        -  256-byte SEEPROM containing I/O riser card FRU information

FRU information for both the I/O baseboard and I/O riser card is stored in SEEPROM devices located on each board.  The devices are accessed via the BMC.  The SEEPROM devices are accessible at the addresses shown in Table 2-10.

*Table 2-10.    I/O Baseboard & I/O Riser Card I$^2$C Address Map*

| Device | Function | I$^2$C Address |
|---|---|---|
| AT24C128* | I/O baseboard FRU information | A6h,A7h |
| AT24C02* | I/O riser card FRU information | AEh,AFh |

Both the AT24C128 and AT24C02 will provide board FRU information.  The FRU information is read and made available by the Intel® Server Console® (ISC).

### 2.1.7.3.1    I/O Baseboard FRU Information

256 bytes of the 128KB SEEPROM located on the I/O baseboard is dedicated to storage of FRU information.  The 256 bytes of programmable space is broken into four areas.  Table 2-11 lists these four areas, a brief description of each, and the space allocated to each area.

*Table 2-11.    SEEPROM Programming Areas (I/O Baseboard)*

| Area | Size | Description |
|---|---|---|
| Common Header | 8 Bytes | Programming offsets to the other areas below. |
| Internal Use | 72 Bytes | This area is reserved for general purpose use by the Intel® Server Management Firmware/Controllers. |
| Board Info | 64 Bytes | Contains the board FRU information listed in Table 2-12. |
| Product Info | 112 Bytes | Programmed as shown below when the I/O baseboard is installed into the AD450NX server system chassis. Otherwise this area is not programmed by Intel and is available for OEM use. † |

† Intel provided FRU & SDR load utilities can be used to program this area.  Refer to the FRU & SDR Load Utility documentation for details.

Table 2-12 lists the board specific FRU information that will be programmed into the board information area.

*Table 2-12.    Board FRU Information (I/O Baseboard)*

| Board Information | | | |
|---|---|---|---|
| **Information** | **Description** | **Example** | **Notes** |
| Mfg. Date/Time | Time & date of board manufacture (Value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/96) | 0x00f593<br><br>(Date & time translation shown below)<br>f593h = 62867min (Feb 12, 1996 3:47pm) | 2 |
| Manufacturer | Board Manufacturer | Intel | 1 |
| Board Product Name | Board Name/Description | A450NX I/O baseboard | 1 |
| Board Serial Number | Intel Board Serial Number | INBR42385906 | 2 |
| Board Part Number | Intel Board Part Number | 662379-001 | 2 |

**Notes:**   **1.**  Actual value programmed into the board.

            **2.**  Example value.  Actual value will vary with each board and fab revision.

Table 2-13 lists the board specific FRU information that will be programmed into the product information area. Note that this information is programmed only when the I/O baseboard is installed into the AD450NX server system chassis.  This area will be left blank if the I/O baseboard is purchased as a board level product.

*Table 2-13.    Product FRU Information (I/O Baseboard)*

| Product Information | | | |
|---|---|---|---|
| **Information** | **Description** | **Example** | **Notes** |
| Manufacturer Name | System Manufacturer Name | Intel | 1 |
| Product Name | System Name/Description | AD450NX Server System | 1 |
| Part Number/Model Number | Intel System Top Assembly Part Number | 670305-101 | 2 |
| Product Version | Not Used.<br>0 Bytes allocated. | --- | 1 |
| Product Serial Number | Intel System Serial Number | N42385906 | 2 |
| Asset Tag | Not used.<br>0 Bytes allocated | **---** | 1 |

**Notes:**   **1.**  Actual value programmed into the board.

            **2.**  Example value.  Actual value will vary with each board and system revision.

Table 2-14 identifies exactly how the 256 bytes of FRU information are allocated within the AT24C128 SEEPROM. This information is useful for those who will be accessing the hardware directly for information (e.g., BIOS developers and server management software developers).

**Note:**  For clarity, the programmed information shown in  is for the board level product only.  Additional information that would be programmed into the product information area for the system level product is not provided.

*Table 2-14.    SEEPROM Content Location (I/O Baseboard)*

| Address | Length | Description | Default Value |
|---------|--------|-------------|---------------|
| 0x00 | 1 | Common Header Format Version | 0x01 |
| 0x01 | 1 | Internal Use Area Offset (8-byte multiples) | 0x01 |
| 0x02 | 1 | Chassis Information Area Offset (8-byte multiples) | 0x00 (area not present) |
| 0x03 | 1 | Board Information Area Offset (8-byte multiples) | 0x0A |
| 0x04 | 1 | Product Information Area Offset (8-byte multiples) | 0x12 |
| 0x05 | 2 | Zero Padding | |
| 0x07 | 1 | Common Header Checksum | 0XE2 |
| 0x08 | 72 | Internal Use Area | |
| 0x50 | 1 | Board Information Area Format Version | 0x01 |
| 0x51 | 1 | Board Information Area Length (8-byte multiples) | 0x08 |
| 0x52 | 1 | Unicode Country Base | 0x00 |
| 0x53 | 3 | Manufacture Date/Time | |
| 0x56 | 1 | Board Manufacturer Type/Length Byte | 0xC5 |
| 0x57 | 5 | Board Manufacturer (ASCII) | 'Intel' |
| 0x5C | 1 | Product Name Type/Length Byte | 0xD4 |
| 0x5D | 20 | Product Name | 'A450NX I/O baseboard' |
| 0x71 | 1 | Board Serial Number Type/Length Byte | 0xCC |
| 0x72 | 12 | Board Serial Number | ………… |
| 0x7E | 1 | Board Part Number Type/Length Byte | 0xCA |
| 0x7F | 10 | Board Part Number | ………. |
| 0x89 | 1 | No More Fields Flag | 0xC1 |
| 0x8A | 5 | Zero Padding | |
| 0x8F | 1 | Board Information Area Checksum | 0x0D |
| 0x90 | 112 | Product Information Area | |

## 2.1.7.3.2    I/O Riser Card FRU Information

The AT24C02 SEEPROM has 256 bytes of programmable space, which is broken into four areas.  Table 2-15 lists these four areas, a brief description of each, and the space allocated to each area.

*Table 2-15.    SEEPROM Programming Areas (I/O Riser Card)*

| Area | Size | Description |
|------|------|-------------|
| Common Header | 8 Bytes | Programming offsets to the other areas below. |
| Internal Use | 48 Bytes | This area is reserved for general purpose use by the Intel® Server Management Firmware/Controllers. |
| Board Info | 80 Bytes | Contains the board FRU information listed in Table 2-16. |
| Product Info | 120 Bytes | Available for OEM use. [†] |

† Intel provided FRU & SDR load utility can be used to program this area.  Refer to the FRU & SDR Load Utility documentation for details

Table 2-16 lists the board specific FRU information that will be programmed into the board information area.

*Table 2-16.    FRU Information (I/O Riser Card)*

| Board Information | | | |
|---|---|---|---|
| **Information** | **Description** | **Example** | **Notes** |
| Mfg. Date/Time | Time & date of board manufacture. (Value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/96) | 0x000f593h<br>(Date & time translation shown below)<br>0xf593h = 62867 min<br>         = 43 Days & 947 min<br>         = Feb 12, 1996, 3:47pm | 2 |
| Manufacturer | Board Manufacturer | Intel | 1 |
| Board Product Name | Board Name/Description | A450NX I/O Riser Card | 1 |
| Board Serial Number | Intel Board Serial Number | INBR42385906 | 2 |
| Board Part Number | Intel Board Part Number | 679267-001 | 2 |

**Notes:**    1.  Actual value programmed into the board.
              2.  Example value.  Actual value will vary with each board and fab revision.

Table 2-17 identifies exactly which bytes are allocated to what purpose within the AT24C02 SEEPROM.  This information is useful for those who will be accessing the hardware directly for information (e.g., BIOS developers and server management software developers).

*Table 2-17.    SEEPROM Content Location (I/O Riser Card)*

| Address | Length | Description | Default Value |
|---|---|---|---|
| 0x00 | 1 | Common Header Format Version | 0x01 |
| 0x01 | 1 | Internal Use Area Offset (8-byte multiples) | 0x01 |
| 0x02 | 1 | Chassis Information Area Offset (8-byte multiples) | 0x00 (area not present) |
| 0x03 | 1 | Board Information Area Offset (8-byte multiples) | 0x07 |
| 0x04 | 1 | Product Information Area Offset (8-byte multiples) | 0x11 |
| 0x05 | 2 | Zero Padding | |
| 0x07 | 1 | Common Header Checksum | 0xE6 |
| 0x08 | 48 | Internal Use Area | |
| 0x38 | 1 | Board Information Area Format Version | 0x01 |
| 0x39 | 1 | Board Information Area Length (8-byte multiples) | 0x0A |
| 0x3A | 1 | Unicode Country Base | 0x00 |
| 0x3B | 3 | Manufacture Date/Time | |
| 0x3E | 1 | Board Manufacturer Type/Length Byte | 0xC5 |
| 0x3F | 5 | Board Manufacturer (ASCII) | 'Intel' |
| 0x44 | 1 | Product Name Type/Length Byte | 0xD5 |
| 0x45 | 21 | Product Name | 'A450NX I/O Riser Card' |
| 0x5A | 1 | Board Serial Number Type/Length Byte | 0xCC |
| 0x5B | 12 | Board Serial Number | ………… |
| 0x67 | 1 | Board Part Number Type/Length Byte | 0xCA |
| 0x68 | 10 | Board Part Number | ………. |
| 0x72 | 1 | No More Fields Flag | 0xC1 |
| 0x73 | 20 | Zero Padding | |
| 0x87 | 1 | Board Information Area Checksum | |
| 0x88 | 120 | Product Information Area | |

# 2.2  CPU Baseboard

This section describes the features of the A450NX CPU baseboard, which is part of the Intel® A450NX Server Board Set.  The CPU baseboard plugs into the CPU board connector on the A450NX interconnect backplane.  There are two versions of the A450NX CPU baseboard: the 4-slot version and the 5-slot version.  Both versions of the CPU baseboard are very similar in functionality, with a few exceptions.  The 5-slot version is also known as the CPU baseboard with cluster connector.  Section 2.2.1 through Section 2.2.7 of this chapter describe both the 4- and 5-slot CPU baseboard, whereas, Section 2.2.7 discusses only the differences between the two versions.

**Note:** The AD450NX server system only uses the 4-slot CPU baseboard.

## Features

The A450NX CPU baseboards, both the 4- and the 5- slot versions, have the following features:

- Four slot-2 connectors to accommodate 1-4 Pentium® II Xeon™ processors
- Two 300-pin memory connectors for two memory modules
- Onboard DC-DC converter for the CPU baseboard and memory module Vtt currents
- Four sockets for voltage regulator module (VRM) 8.3 converters to supply power to the processor core component of the four Pentium II Xeon processors
- Two sockets for VRM 8.3 converters for the L2 cache voltage for the Pentium II Xeon processors
- $I^2C$, serial peripheral interface (SPI) and server management interfaces

The following features apply only to the 5-slot version of the CPU baseboard:

- Two sockets for optional VRM 8.2 converters to provide power for an OEM-designed distributed shared memory (DSM) cluster card
- One cluster connector for an optional cluster interconnect board
- An advanced programmable interrupt controller (APIC) jumper for optional PICCLK frequency selection

## 2.2.1   Placement Diagram

Figure 2-5 shows the placement of the major components and connectors on the CPU baseboard.  Note that jumpers J7, J8, and J14 are used for the optional cluster card.
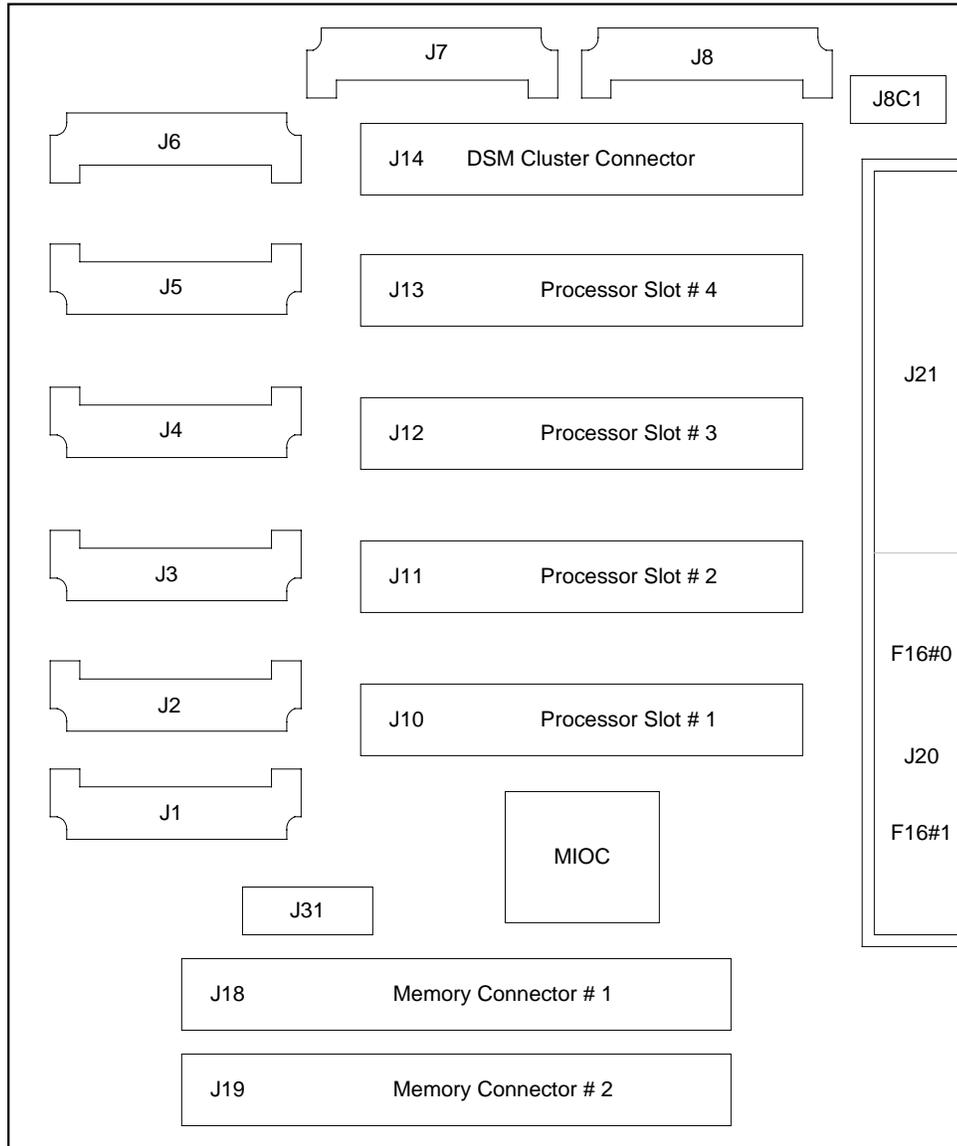


*Figure 2-5.     CPU Baseboard Layout (5-slot)*

Table 2-18 lists the major components of the CPU baseboard.  The connectors listed in Table 2-18 are from the bottom of Figure 2-5.

*Table 2-18.    Major Component Reference (CPU Baseboard)*

| Reference Designator | Name and Description |
|---|---|
| J19 | Memory module #2 connector (secondary) |
| J18 | Memory module #1 connector (primary) |
| J31 | Board configuration jumper block |
| J1 | VRM - Provides power for processor slot #1 (processor core power only) |
| J2 | VRM - Provides power for processor slots #1 and #2 (L2 cache power only) |
| J3 | VRM - Provides power for processor slot #2 (processor core power only) |
| J4 | VRM - Provides power for processor slot #3 (processor core power only) |
| J5 | VRM - Provides power for processor slots #3 and #4 (L2 cache power only) |
| J6 | VRM - Provides power for processor slot #4 (processor core power only) |
| J7, J8 (top) | VRM - Provide power for an OEM designed DSM cluster card at slot #5 |
| J8C1 | APIC jumper block  (only on 5-slot board) |
| F16#0 | F16 bus to the two 32-bit PCI buses (J20) |
| F16#1 | F16 bus to the one 64-bit PCI bus (J20) |

## 2.2.2   Memory Interface

The A450NX memory subsystem consists of two memory modules, each containing sixteen 72-bit wide DIMM sockets.  With the largest DIMM size allowed in each socket (256 MB), each memory module can provide up to 4 GB of extended data out (EDO) memory capacity.  The memory interface is extensible to potential future versions of the A450NX memory module.

Like the processor bus, the memory bus also uses AGTL+ signaling technology.  However, a source synchronous scheme is used on this bus enabling data transfers at 200 MHz.  This is achieved by sending two strobes, offset by 180 degrees, together with data, both running at 100 MHz, and using them to capture the data at destination.  The strobes are single ended.  Like the processor bus, the memory bus has to be terminated at all connectors; thus both memory connectors must always be populated with memory modules or one memory module and a memory termination module.  One common address/control bus is routed from the MIOC component on the CPU baseboard to the two memory modules.  In addition, there are dedicated control signals for each of the memory module connectors.

The second memory module connector orientation is reversed with respect to the first connector to minimize the CPU baseboard dimension and to shorten the address/control bus to the memory module.  As a result, the DIMMs of the first memory board face towards the processors, while the DIMMs of the second memory module face away from the processors.

## 2.2.3   Voltage Regulators

The voltage supply for each of the four processor cores is supplied independently by one VRM 8.3 converter, for a total of four VRMs.  Two additional VRM 8.3 converters provide the voltage supply for the L2 caches; one VRM 8.3 is shared between two processors.  This arrangement requires that the L2 voltages within a processor pair be identical.  The voltage management controller (VMC) compares the voltage ID (VID) bits from the two L2s and, if different, the VMC disables the VRM 8.3.  Note that VRM 8.3 has remote sensing.

For all processors installed into the CPU baseboard, the VRM supplying current for both the core and L2 cache of that processor must be populated.  Figure 2-5 and Table 2-18 indicate which VRMs must be installed for a given processor.  If a processor is not installed, the corresponding VRM(s) may either be installed in the socket or the

socket may be left empty. If the VRM is installed even though its corresponding processor is not, circuitry on the CPU baseboard disables the VRM.

There are two additional VRM sockets for the cluster slot in the 5-slot version. VRMs complying with the VRM 8.2 specification should be used in these. Note that VRM 8.2 does not have remote sensing, whereas VRM 8.3 does.

All converters for the processor voltages convert off of the +12 V supply rail. The CPU baseboard also has one large switching regulator for the AGTL+ termination voltage (1.5 V) required on the CPU baseboard, memory modules, and processors, and a small +2.5 V linear regulator for the 2.5 V logic (clock buffers and voltage shifters). Both of these regulators convert off of the +5 V supply rail.

# 2.2.4  Configuring Baseboard Jumpers

There are two jumper blocks on the CPU baseboard:

> J31    - Bus Ratio Jumper Block (both 4- and 5-slots)
>
> J8C1  - APIC Jumper Block (only for 5-slot)

## 2.2.4.1    J31 – Bus Ratio Jumper Block

This jumper block serves three functions (refer to Figure 2-6):

1. controls the VRMs and server management outputs (see Table 2-19),
2. determines core to bus ratio (see Table 2-20), and
3. provides parking space for unused jumper pegs.

*Table 2-19.    Board Configuration Jumper Block (VRMs, Server Management)*

| Pins 1-2 | Pins 3-4 | Status |
|---|---|---|
| 1 | 1 | Disables VRMs |
| 1 | 0 | Reserved |
| 0 | 1 | Disable Server Management |
| 0 | 0 | Default / Normal Operation |

Notes:  1.  **Key:** 0-open; 1-closed

2.  Jumpers across pins 1-2 and 3-4 are for internal Intel validation only. In normal operation these jumpers would be open.

Jumpers across pins 5-6, 7-8, and 9-10 determine the processor core to the front-side bus frequency ratio. In configuration without the cluster board, the bus frequency (supplied by the onboard transistor-transistor logic (TTL) oscillator) is 100 MHz. When the cluster board is present (5-slot version only), the maximum bus frequency supported is 90 MHz, which is supplied by the cluster card. Defined ratios are shown in Table 2-20. Core frequencies shown are based on 100 MHz bus frequency.

*Table 2-20.    Board Configuration Jumper Block (Bus Ratio)*

| Pins 5-6 | Pins 7-8 | Pins 9-10 | Bus Ratio | Core Freq. (MHz) |
|---|---|---|---|---|
| 1 | 1 | 1 | 11:2 | 550 |
| 1 | 1 | 0 | 9:2 | 450 |
| 1 | 0 | 1 | 7:2 | 350 |
| 1 | 0 | 0 | Reserved | |
| 0 | 1 | 1 | 5:1 | 500 |

| Pins 5-6 | Pins 7-8 | Pins 9-10 | Bus Ratio | Core Freq. (MHz) |
|----------|----------|-----------|-----------|------------------|
| 0 | 1 | 0 | 4:1 | 400 |
| 0 | 0 | 1 | 3:1 | 300 |
| 0 | 0 | 0 | Reserved | |

**Key:** 0-open; 1-closed

There are three parking positions available for the safekeeping of the jumper pegs. These jumper pegs can be parked across pins 11-12, 13-14, and 15-16.
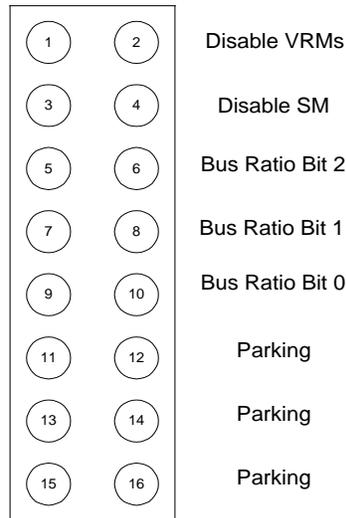


*Figure 2-6.     J31 Jumper Block Pinout*

## 2.2.4.2    J8C1 – APIC Jumper Block (5-slot Version Only)

This 3-pin jumper is available only for the 5-slot version. This sets the frequency of the PICCLKs (APIC clock input) to be either 1/4 (default) or 1/8 of the front-side bus (FSB) clock (also known as BCLK) frequency. For systems configured for functional redundancy check (FRC) mode of operation, PICCLKs must be 1/4 of BCLK.

*Table 2-21.     APIC Jumper Block to Set PICCLK Frequency*

| J8C1 Jumper | Setting | PICCLK |
|-------------|---------|--------|
| Pins 1/2 | Closed (default) | BCLK / 4 |
| Pins 2/3 | Closed | BCLK / 8 |

# 2.2.5    Populating Processors

Processors must be populated starting at the first slot 2 (J10), then at the second slot 2 (J11), and so on. The empty slots must be populated with FSB termination cards. The fifth slot-2 (J14) on the 5-slot baseboard must be populated with an FSB termination module or with a cluster board (which should have FSB termination as specified in the cluster board specification).

## 2.2.6 Mixing of Processors of Different Frequency and Stepping

Processors are validated to operate within a minimum and maximum frequency window. For instance, a processor rated as 350 MHz is not guaranteed to operate beyond 350 MHz, but may be guaranteed to operate down to 300 MHz. Refer to the *Pentium® II Xeon™ Processor Specification* for supported valid ranges. Consequently, processors of different frequency ratings may have different valid ranges. ***The common range among the different processors determines the overall valid frequency range within which the core-to-bus ratio jumper (J31) needs to be set.*** This means the lowest rated processor would determine the overall core-to-bus ratio, compromising the performance achievable with the higher rated processors in the system.

Though Intel recommends using identical processor steppings in multiprocessor systems (as this is the only configuration that receives full validation across all of Intel's testing), Intel does not actively prevent (and will support) the use of various steppings of the Pentium II Xeon processor together in multiple processor (MP) systems. However, since Intel cannot validate every possible combination of devices, each stepping of a device is fully validated against only the latest steppings of other processors and chip set components. Refer to the *Pentium®II Xeon™ Processor Specification* for further details on issues related to mixed processor steppings in an MP system.

## 2.2.7 4-slot CPU Baseboard Differences

The 4-slot and 5-slot versions of A450NX CPU baseboards are very similar. Important differences do exist, however, and are outlined in this section. Comparisons are made against specific previous sections of this chapter, which describe the 5-slot version.

Both versions of the CPU baseboard support up to 4 processors. However, in the 5-slot version, the fifth slot-2 connector is provided for a cluster board extension, which is not available for the 4-slot version. This is the major difference between the two versions. Except for this, the two versions are similar both in function and layout.

## Features

Same as 5-slot baseboard except:

- there is no cluster connector or the two VRM 8.2 sockets that were associated with the cluster; and
- there is no APIC jumper block for user settable PICCLK frequency.

### 2.2.7.1 Placement Diagram

Refer to Figure 2-5. The 4-slot CPU baseboard does not contain the cluster connector (J14), the two VRM 8.2 sockets (J7, J8), and the APIC jumper (J8C1). Otherwise, both versions of baseboard are similar.

### 2.2.7.2 Server Management Interface

Refer to Figure 4-1 for more detail on server management architecture. The server management logic on the 4-slot baseboard is the same as on the 5-slot version, except the portion of the IPMB bus, which connects the cluster slot, does not exist on the 4-slot baseboard. The $I^2C$ address map remains the same for all other devices.

### 2.2.7.3 Configuration of Baseboard Jumpers

The 4-slot baseboard contains only the bus ratio jumper. The settings for this jumper are the same as those discussed in Section 2.2.5 for the 5-slot baseboard. The APIC jumper is not available in the 4-slot baseboard. By default, the PICCLKs are set to BCLK/4. This means that with a 100 MHz onboard clock, the PICCLKs run at 25 MHz. FRC mode is available in this configuration also.

## 2.2.8    Server Management Features

The private I$^2$C buses provide access to basic temperature, configuration and inventory information.  The CPU baseboard contains the following I$^2$C accessible devices:

- Baseboard FRU information and temperature sensor Dallas (DS1624*)
- Processor temperature sensors in Pentium II Xeon processors
- Processor FRU information SEEPROM
- Memory modules (for more details, refer to Chapter 5, which describes the memory module)

These server management features are accessed via the BMC on the A450NX I/O baseboard.  The I$^2$C devices are accessible at the following addresses:

*Table 2-22.    CPU Baseboard I$^2$C Address Map*

| Device and Bus Name | I$^2$C Address |
|---|---|
| ***Devices on** Pentium® II Xeon™ processor **SMBus:*** | |
| Processor #1: OEM_EEPROM \|   Intel_EEPROM \| A2D converter | A0h,A1h   \|   A2h,A3h   \|   30h,31h |
| Processor #2: OEM_EEPROM \|   Intel_EEPROM \| A2D converter | A4h,A5h   \|   A6h,A7h   \|   52h,53h |
| Processor #3: OEM_EEPROM \|   Intel_EEPROM \| A2D converter | A8h,A9h   \|   AAh,ABh   \|   34h,35h |
| Processor #4: OEM_EEPROM \|   Intel_EEPROM \| A2D converter | ACh,ADh   \|   AEh,AFh   \|   56h,57h |
| Terminator card (if present ) at 1$^{st}$ processor  slot   OEM_EEPROM | A0h,A1h |
| Terminator card (if present ) at 2$^{nd}$ processor  slot   OEM_EEPROM | A4h,A5h |
| Terminator card (if present ) at 3$^{rd}$ processor  slot   OEM_EEPROM | A8h,A9h |
| Terminator card (if present ) at 4$^{th}$ processor  slot   OEM_EEPROM | ACh,Adh |
| ***Devices on IPMB Bus [5-slot version only]:*** | |
| DSM Cluster board | ACh,Adh |
| Terminator card (if present ) at cluster slot   OEM_EEPROM | ACh,Adh |
| ***Devices on BMC Private I2C Bus:*** | |
| CPU baseboard temperature and FRU information | 98h,99h |
| Memory Module #1 I/O (Port 0) | 70h,71h |
| Memory Module #1 I/O (Port 1) | 72h,73h |
| Memory Module #1 temperature & FRU information | 9Ah,9Bh |
| Memory Module #2 I/O (Port 0) | 74h,75h |
| Memory Module #2 I/O (Port 1) | 76h,77h |
| Memory Module #2 temperature & FRU information | 9Eh,9Fh |

## 2.2.8.1    DS1624 SEEPROM

The DS1624, when accessed via the BMC private I$^2$C bus, provides the temperature of the baseboard, as measured at the DS1624, as well as the following FRU information.  The FRU information is read and made available by the Intel® Server Console® (ISC).

The DS1624 SEEPROM has 256 bytes of programmable space, which is broken into four areas.  Table 2-23 is a list of the areas, with a description and the amount of space allocated to each.

*Table 2-23.    DS1624 SEEPROM Programming Areas*

| Area | Size | Description |
|---|---|---|
| Common Header | 8 bytes | Programming offsets to the other areas below. |
| Internal Use | 48 bytes | This area is reserved for general-purpose use by the Intel® Server Management Firmware/Controllers. |
| Board Info | 80 bytes | Contains the board FRU information listed in Table 2-24. |
| Product Info | 120 bytes | Available for OEM use.$^{†}$ |

$^{†}$  The Intel provided FRU & SDR Load Utility allows OEMs to program this area.  Refer to the FRU and SDR Load Utility documentation for more details.

Table 2-24 lists the board specific FRU information that will be programmed into the board information area.

*Table 2-24.    FRU Information*

| Board Information | | | |
|---|---|---|---|
| **Information** | **Description** | **Example** | **Notes** |
| Mfg. Date/Time | Time & date of board manufacture (Value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/96) | 000f593h<br>(Date & time translation shown below)<br>f593h = 62867 min<br>= 43 Days & 947 min<br>= Feb 12, 1996, 3:47pm | 2 |
| Manufacturer | Board Manufacturer | Intel | 1 |
| Board Product Name | Board Name/Description | A450NX CPU Baseboard w/Cluster | 1,3 |
| Board Serial Number | Intel Board Serial Number | INBR85906000 | 2 |
| Board Part Number | Intel Board Part Number | 663008-002 | 2 |

**Notes:**   1.  Actual value programmed into the board.
2.  Example value.  Actual value will vary for each board and fab revision.
3.  The board product name for the 4-slot CPU baseboard is 'A450NX CPU Baseboard No Cluster.'

Table 2-25 identifies exactly which bytes are allocated to what purpose within the DS1624 SEEPROM.  This information is useful for those who will be accessing the hardware directly for information (i.e., BIOS developers and server management software developers).

*Table 2-25.    SEEPROM Byte Map*

| Address | Length | Description | Default Value |
|---|---|---|---|
| 0x00 | 1 | Common Header Format Version | 0x01 |
| 0x01 | 1 | Internal Use Area Offset (8-byte multiples) | 0x01 |
| 0x02 | 1 | Chassis Information Area Offset (8-byte multiples) | 0x00 (area not present) |
| 0x03 | 1 | Board Information Area Offset (8-byte multiples) | 0x07 |
| 0x04 | 1 | Product Information Area Offset (8-byte multiples) | 0x11 |
| 0x05 | 2 | Zero Padding | |
| 0x07 | 1 | Common Header Checksum | 0xE6 |
| 0x08 | 48 | Internal Use Area | |
| 0x38 | 1 | Board Information Area Format Version | 0x01 |
| 0x39 | 1 | Board Information Area Length (8-byte multiples) | 0x0A |
| 0x3A | 1 | Unicode Country Base | 0x00 |
| 0x3B | 3 | Manufacture Date/Time | |
| 0x3E | 1 | Board Manufacturer Type/Length Byte | 0xC5 |
| 0x3F | 5 | Board Manufacturer (ASCII) | 'Intel' |
| 0x44 | 1 | Product Name Type/Length Byte | 0xDF |
| 0x45 | 31 | Product Name† | 'A450NX CPU Baseboard w/Cluster' |
| 0x64 | 1 | Board Serial Number Type/Length Byte | 0xCC |
| 0x65 | 12 | Board Serial Number | ………… |
| 0x71 | 1 | Board Part Number Type/Length Byte | 0xCA |
| 0x72 | 10 | Board Part Number | ……… |

| Address | Length | Description | Default Value |
|---|---|---|---|
| 0x7C | 1 | No More Fields Flag | 0xC1 |
| 0x7D | 10 | Zero Padding | |
| 0x87 | 1 | Board Information Area Checksum | 0xEA |
| 0x88 | 120 | Product Information Area | |

† The board product name for the 4-slot CPU baseboard is 'A450NX CPU Baseboard No Cluster.'

Temperature and EEPROM data may be accessed via I$^2$C commands to the DS1624 device. Table 2-26 is taken from the DS1624 data sheet.

*Table 2-26.    EEPROM Command Set*

| INSTRUCTION | DESCRIPTION | PROTOCOL | 2-WIRE BUS DATA AFTER ISSUING PROTOCOL | NOTES |
|---|---|---|---|---|
| TEMPERATURE CONVERSION COMMANDS | | | | |
| Read Temperature | Read last converted temperature value from temperature register. | AAh | <read 2 bytes data> | |
| Start Convert T | Initiates temperature conversion. | EEh | Idle | |
| Stop Convert T | Halts temperature conversion. | 22h | Idle | |
| MEMORY COMMANDS | | | | |
| Access Memory | Reads or writes to 256-byte EEPROM memory. | 17h | <write data> | |
| Access Config | Reads or writes configuration data to configuration register. | ACh | <write data> | |

# 2.3   Front-side Bus Terminator Module

This section describes the features of the front-side bus (FSB) terminator module.  The FSB terminator module was designed for use with the A450NX CPU baseboard.

## Features

• Terminates the processors front-side bus AGTL+ signals

• FRU information

## 2.3.1   Architectural Overview

The A450NX CPU baseboard provides four slot-2 connectors, which can populate up to four processors (and an additional cluster card on the 5-slot CPU baseboard).  The absence of a processor on any of these slot-2 connectors requires that an FSB terminator module replace it.  For example, if only two processors are installed on a 5-slot CPU baseboard, then three additional FSB terminator modules are needed to populate the remaining three slot-2 connectors; two for the processor slots and one for the cluster slot.

The FSB terminator module provides the following features:

• The necessary termination for the AGTL+ signals on the processors front-side bus

• FRU information (P/N, S/N, board ID, etc.) via $I^2C$

### 2.3.1.1   Usage Model

The terminator module was designed in such a way that it can be used in the processor slots on both 4-slot and 5-slot CPU baseboards.  It can also be used in the cluster slot on a 5-slot CPU baseboard.

#### 2.3.1.1.1   Processor Slot

When the FSB terminator module is used with the Intel designed processor and the FSB terminator retention mechanism, an additional plastic housing is attached to the terminator module.  The housing snaps into holes on the terminator module.  A preliminary diagram of the plastic housing is shown in Figure 2-7.  The housing was added to give the terminator module a mechanical and thermal profile similar to the Pentium II Xeon slot-2 processor cartridge (i.e., it exhibits similar thermal flow properties as a Pentium II Xeon slot-2 processor with heatsink).
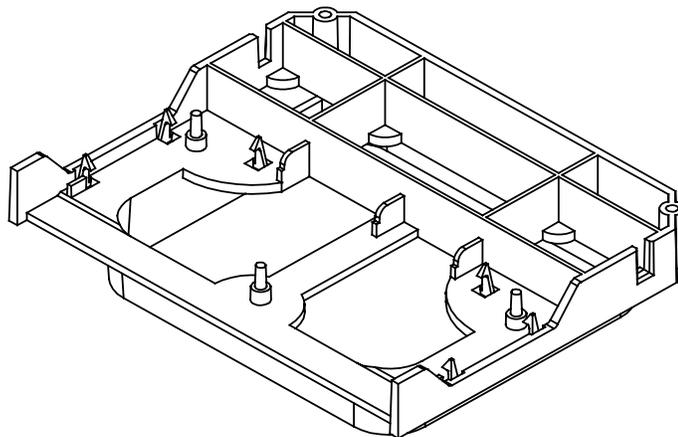


*Figure 2-7.    Plastic Housing for Processor Slot Retention*

## 2.3.1.1.2    Cluster Slot

An Intel designed retention mechanism is available for the FSB terminator module, when the module is used in the cluster slot on the 5-slot CPU baseboard.  The module and retention mechanism are inserted into the slot-2 connector and held in place by two separate brackets of the cluster slot retention mechanism.  The cluster slot retention mechanism is designed only for the FSB terminator module and will not accommodate an OEM provided cluster card (unless the cluster card is built to the same dimensional specifications as the FSB terminator module).  Figure 2-8 diagrams two different views of the cluster slot retention bracket.
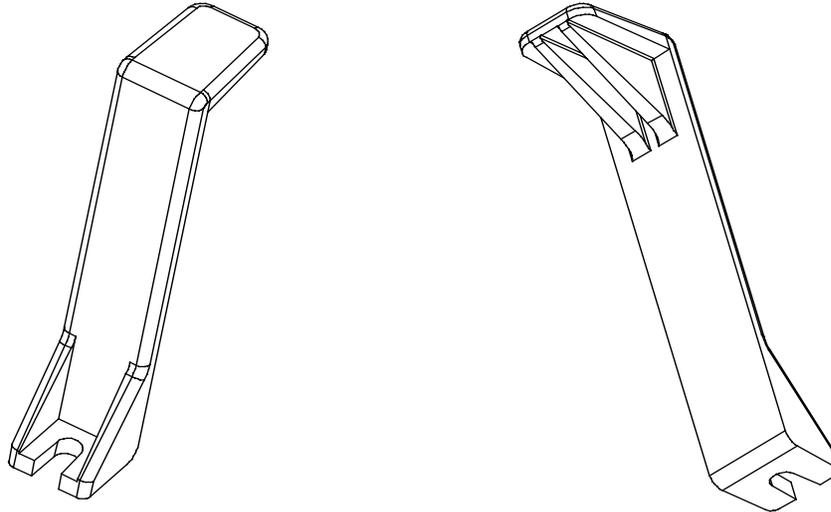


*Figure 2-8.      Cluster Slot Terminator Module Retention Mechanism*

# 2.3.1.2    Placement Diagram

Figure 2-9 shows the primary components of the FSB terminator module and their positions on the printed circuit board.  Table 2-27 maps reference designators to device names.
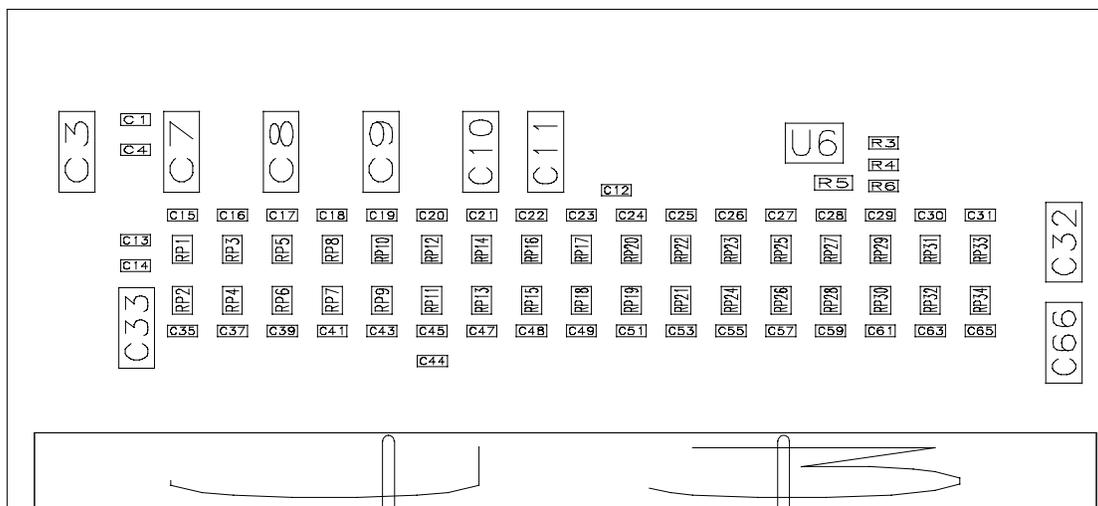


*Figure 2-9.      FSB Terminator Module Placement Diagram*

*Table 2-27.    Reference Designator Decoder*

| Reference Designator | Description |
|---|---|
| U6 | AT24C02 SEEPROM |
| J3 | FSB Interface connector |

## 2.3.1.3    Server Management Features

The FSB terminator module contains the following I$^2$C accessible device:

- AT24C02 - SEEPROM containing FRU information

The FRU device information is accessible at the addresses shown in Table 2-28.

*Table 2-28.    FSB Terminator Module Address Map*

| Device | Function | Bus Name | Slot | Address | CPU Baseboard Type |
|---|---|---|---|---|---|
| AT24C02* | FSB Term. Module FRU Information | Processor SMBus | Processor Slot #1 | A0h,A1h | 4 and 5 slots |
| AT24C02 | FSB Term. Module FRU Information | Processor SMBus | Processor Slot #2 | A4h,A5h | 4 and 5 slots |
| AT24C02 | FSB Term. Module FRU Information | Processor SMBus | Processor Slot #3 | A8h,A9h | 4 and 5 slots |
| AT24C02 | FSB Term. Module FRU Information | Processor SMBus | Processor Slot #4 | ACh,ADh | 4 and 5 slots |
| AT24C02 | FSB Term. Module FRU Information | IPMB | Cluster Slot | ACh,ADh | 5 slots only |

**Notes:**    1. The AT24C02 address and management buses are different depending on which slot the FSB terminator module is plugged into.  The addresses are hard coded into the CPU baseboard.

2. If the module is plugged into one of the processor slots on the A450NX board set, the AT24C02 device can be accessed through the Pentium® II Xeon™ slot-2 processor SMBus via the BMC only.  For the FSB terminator modules installed in the cluster slot (of a 5-slot CPU baseboard), the AT24C02 device can be accessed via the Intelligent Platform Management Bus (IPMB) by the BMC, or any other Intelligent Platform Management Interfaces (IPMI) compliant management controller in the chassis.

The AT24C02, when accessed, will provide FRU information for the board.  The FRU information is read and made available by the Intel® Server Console (ISC).

The AT24C02 SEEPROM has 256 bytes of programmable nonvolatile memory, which is broken into four areas. Table 2-29 provides a list of the areas, a description each area, and the space allocated to each area.

*Table 2-29.    AT24C02 SEEPROM Programming Areas*

| Area | Size | Description |
|---|---|---|
| Common Header | 8 bytes | Programming offsets to the other areas below. |
| Internal Use | 48 bytes | This area is reserved for general purpose use by Intel® Server Management Firmware/Controllers. |
| Board Info | 80 bytes | Contains the board FRU information listed in Table 2-30. |
| Product Info | 120 bytes | Available for OEM use.† |

†   An FRU & SDR Load Utility is provided by Intel that allows OEMs to program that area.  Please refer to the *FRU & SDR Load Utility* documentation for details.

Table 2-30 lists the specific board FRU information that is programmed into the board information area during manufacturing assembly.

*Table 2-30.    FRU Information*

| Board Information | | | |
|---|---|---|---|
| **Information** | **Description** | **Example** | **Notes** |
| Mfg. Date/Time | Time & Date of board manufacture  (Value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/98) | 0x00f593h<br><br>(Date & time translation shown below)<br>f593h = 62867 min<br>     = 43 Days & 947 min<br>     = Feb 12, 1996, 3:47pm | 2 |
| Manufacturer | Board Manufacturer | Intel | 1 |
| Board Product Name | Board Name/Description | A450NX FSB Terminator Module | 1 |
| Board Serial Number | Intel Board Serial Number | INBR42385906 | 2 |
| Board Part Number | Intel Board Part Number | 663077-001 | 2 |

**Notes:**   **1.**  Actual value programmed into the board.
          **2.**  Example value.  Actual value will vary with each board and fab revision.

Table 2-31 identifies exactly which bytes are allocated to what purpose within the AT24C02 SEEPROM.  This information is useful for those who will be accessing the hardware directly for information (e.g., BIOS developers and server management software developers).

*Table 2-31.    SEEPROM Content Location*

| Address | Length | Description | Default Value |
|---|---|---|---|
| 0x00 | 1 | Common Header Format Version | 0x01 |
| 0x01 | 1 | Internal Use Area Offset (8-byte multiples) | 0x01 |
| 0x02 | 1 | Chassis Information Area Offset (8-byte multiples) | 0x00 (area not present) |
| 0x03 | 1 | Board Information Area Offset (8-byte multiples) | 0x07 |
| 0x04 | 1 | Product Information Area Offset (8-byte multiples) | 0x11 |
| 0x05 | 2 | Zero Padding | |
| 0x07 | 1 | Common Header Checksum | 0xE6 |
| 0x08 | 48 | Internal Use Area | |
| 0x38 | 1 | Board Information Area Format Version | 0x01 |
| 0x39 | 1 | Board Information Area Length (8-byte multiples) | 0x0A |
| 0x3A | 1 | Unicode Country Base | 0x00 |
| 0x3B | 3 | Manufacture Date/Time | |
| 0x3E | 1 | Board Manufacturer Type/Length Byte | 0xC5 |
| 0x3F | 5 | Board Manufacturer (ASCII) | 'Intel' |
| 0x44 | 1 | Product Name Type/Length Byte | 0xDC |
| 0x45 | 28 | Product Name | 'A450NX FSB Terminator Module' |
| 0x61 | 1 | Board Serial Number Type/Length Byte | 0xCC |
| 0x62 | 12 | Board Serial Number | ............ |
| 0x6E | 1 | Board Part Number Type/Length Byte | 0xCA |
| 0x6F | 10 | Board Part Number | .......... |
| 0x79 | 1 | No More Fields Flag | 0xC1 |
| 0x7A | 13 | Zero Padding | |
| 0x87 | 1 | Board Information Area Checksum | 0xC7 |
| 0x88 | 120 | Product Information Area | |

# 2.4   Memory and Memory Terminator Modules

This section describes the features of the A450NX memory and memory terminator modules.  The A450NX memory module is a high-capacity DRAM memory board based on the 450NX chip set.  The memory module has been designed for use with the A450NX CPU baseboard, which has two memory module connectors.  The memory terminator module provides electrical termination for the memory and I/O controller (MIOC) memory bus in the event that only one memory module is in use in the system.  The memory terminator has the same mechanical dimensions but lacks the DIMM sockets, chip set elements, and presence detect (PD) bit readout hardware of the memory module.

Both CPU baseboard memory interface connectors must be populated in order to properly terminate the Advanced Gunning Transceiver Logic + (AGTL+) memory bus.  This can be done by installing two memory modules or one memory module and one memory terminator module.

## Features

- Up to 4 GB of error correction code (ECC) memory per module using 16 72-bit dual inline memory modules (DIMMs), for a total of 8 GB using two modules

- 60 nanosecond (ns) and 50 ns 3.3 V buffered EDO DRAM

- Four-way interleaving

- Minimum configuration of 128 MB using four 32-MB DIMMs

- Supports buffered DIMMs with capacity of 32 MB, 64 MB, and 256 MB.  Other DRAM sizes may function correctly but will not be validated.

- Provides server management data, including thermal monitoring, FRU information, and presence detect bit access

## 2.4.1   Placement Diagrams

The diagrams on the following pages were generated from the actual layout database and show the primary components of the A450NX memory and memory terminator modules and their position on the printed circuit boards.  Table 2-32 maps reference designator to device name for the A450NX memory module.

*Table 2-32.    Memory Module Placement Diagram Reference Designators*

| Reference Designator | Description |
|---|---|
| U3D1 | MUX0, Data Path Multiplexor for data bits 0-35. 324-ball BGA. |
| U6D1 | MUX1, Data Path Multiplexor for data bits 36-71, 324-ball BGA. |
| U5D1 | RCG, RAS/CAS generator for banks A-D, 324-ball BGA. |
| U9D1 | DS1624*, I$^2$C EEPROM and temperature sensor [package]. |
| J1-J4 | 168-pin DIMM sockets, Bank A. |
| J5-J8 | 168-pin DIMM sockets, Bank B. |
| J9-J12 | 168-pin DIMM sockets, Bank C. |
| J12-J16 | 168-pin DIMM sockets, Bank D. |
| J21 | Memory Interface Connector (Futurebus*) |
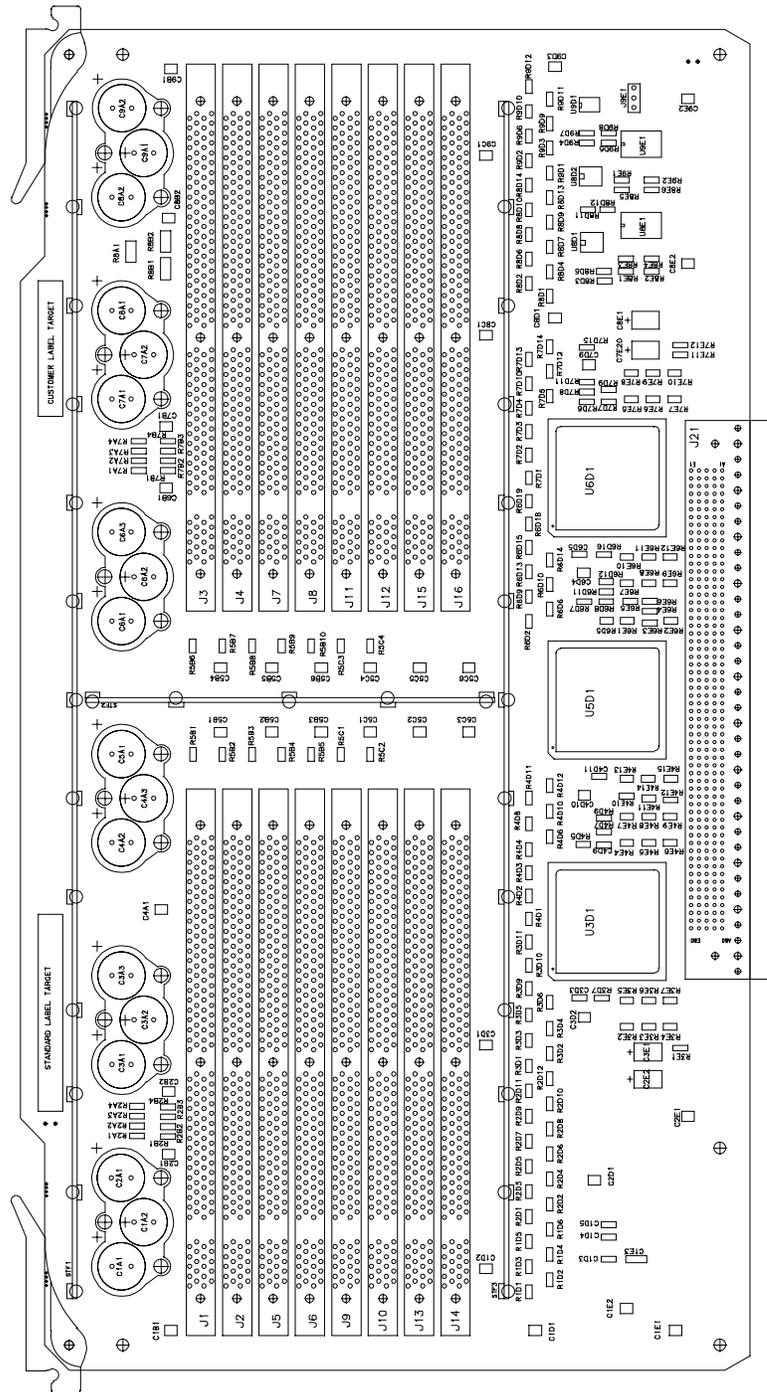
*Figure 2-10.   Memory Module Placement Diagram*
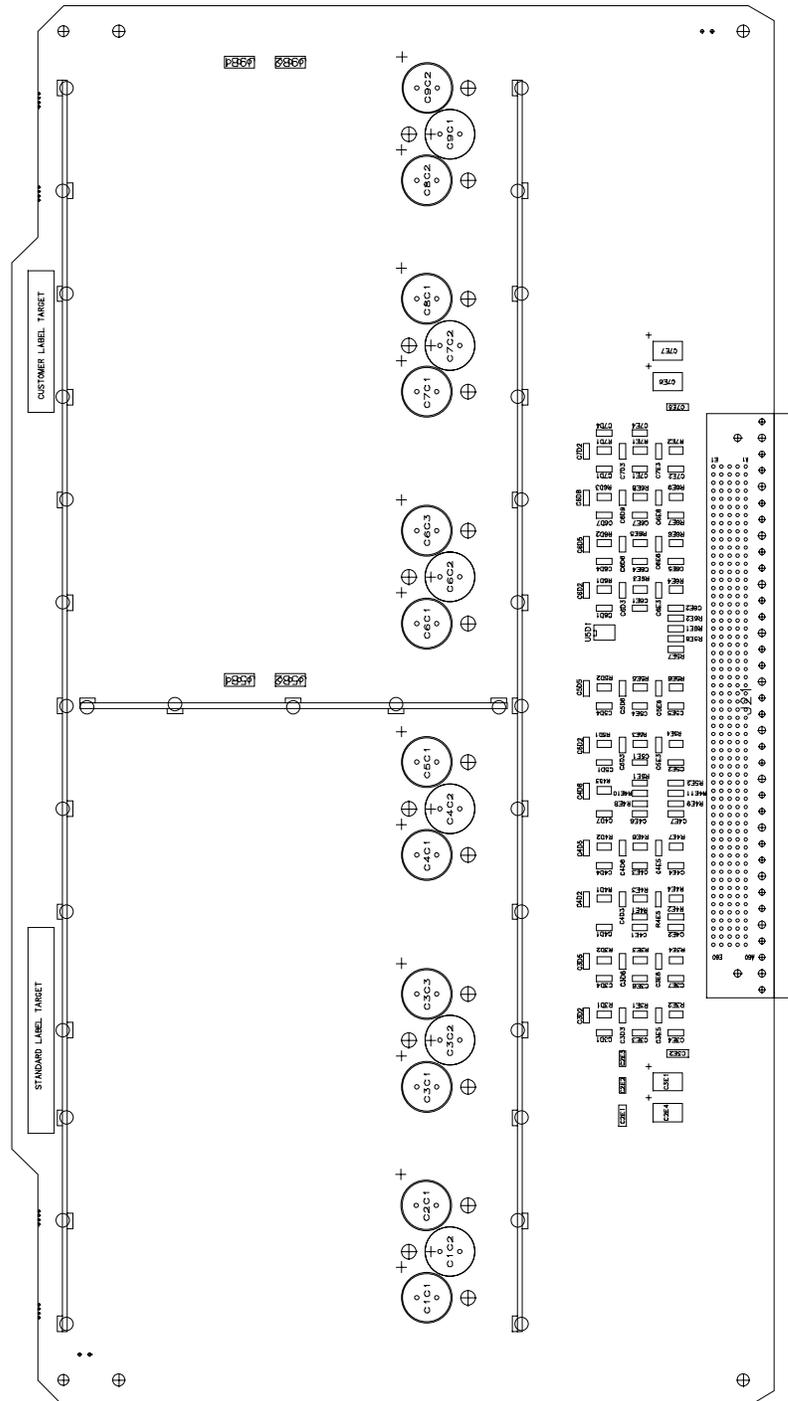
*Figure 2-11.   Memory Terminator Module Placement Diagram*

## 2.4.2   EDO DRAM Array

The memory array on the A450NX memory module consists of sixteen 72-bit (64-bit data plus 8 ECC bits) DIMM sockets.  These sockets are divided into four banks of four sockets each (labeled A through D).  The A450NX board set and memory module supports only 4:1 interleaving of the these banks.  With 4:1 interleaving, all four DIMM within a bank must be populated.  The four DIMMs are organized as follows, using the reference designators for Bank A as an example:

        J1     Interleave 0
        J2     Interleave 1
        J3     Interleave 2
        J4     Interleave 3

Each interleave provides access to 72 bits of data, thus 4:1 interleaving yields 288-bits (32 bytes) per transaction, which is one cache line for the Pentium II Xeon processor.  With two memory modules in a system, the modules can complete DRAM transactions at a maximum rate of once every 30 ns (when consecutive transactions hit in different memory modules) for a maximum data rate of 1.067 GB/s.

Note that to achieve the maximum sustainable bandwidth, the memory modules must be configured so that
1. memory accesses can alternate back and forth between boards and
2. it is possible to get a continuous stream of row misses.

Condition 2 can be achieved only if at least four banks of memory are populated.  To meet both conditions 1 and 2, a minimum of four banks must be populated, two on each memory module.

While using the single memory module and memory terminator configuration, the card to card consecutive transactions scheme is not possible.  As such, this configuration has a reduced maximum data transfer rate of 800 MB/s.

There are several types of DIMM components available.  Table 2-33 shows which combinations of DIMM components can be functionally used in the A450NX memory module.  As a result of the numerous combinations possible between DIMM size, speed, vendor and location in the module, not all combinations will be validated by Intel.

*Table 2-33.     Memory Module DIMM Types*

| Category | DIMM Variety |
|---|---|
| Speed | 50 ns, 60 ns |
| Capacity/ Organization/ Refresh | 16 MB: 16 Mbit, 2Mx8 DRAM, 2K Refresh[1, 2] |
| | 32 MB: 16 Mbit, 4Mx4 DRAM;2K or 4K Refresh[1] |
| | 32 MB: 4 Mx16 & 4MBx4 Combined, 2K or 4K Refresh[1] |
| | 64 MB: 64 Mbit, 8Mx8 DRAM; 4K Refresh[1] |
| | 128 MB: 64 Mbit, 16Mx4 DRAM; 4K or 8K Refresh[1, 2] |
| | 256 MB: Double-high; 64 Mbit, 16Mx4 DRAM; 4K or 8K Refresh[1] |
| Voltage | 3.3 V |
| Data Width | x72 (ECC) |
| Page Mode | EDO |
| Buffered/Non | Buffered |
| Maximum Height | 2.4 inches |
| DRAM Package | TSOP |

Notes:   1.   The A450NX memory module supports CAS-before-RAS (CBR) refresh only.
                 When selecting a module, make sure that the target refresh number corresponds
                 to CBR refresh.
         2.   Should function correctly, but will not be validated.

The memory module will not work with any interleave scheme other than 4:1 interleaving.  As a result, there are bank population requirements.  The following bullets outline the configurations expected to function in the A450NX board set.  However, **ONLY A LIMITED SUBSET** of the possible combinations from these parameters will be

validated and supported by Intel.  The population requirements that will result in an Intel validated configuration are discussed in the paragraph below.

- All banks used must be fully populated with four DIMMs

- 16 MB, 32 MB, 64 MB, 128 MB, and 256 MB capacity DIMMs

- 50 ns or 60 ns DIMM speeds (DIMM speeds may be mixed from bank to bank, but all DIMMs will run the speed of the slowest installed DIMM)

- 4, 8, 12, 16, 20, 24, 28, or 32 DIMMs (total number of DIMMs in a dual memory module configuration)

- 4, 8, 12, 16 DIMMs (total number of DIMMs in a single memory module and single memory terminator configuration)

- Banks are be populated from the top to the bottom of a given card (see Figure 2-12 through Figure 2-19).

- All DIMMs in a given bank are of uniform size.  DIMM sizes may change from bank to bank.

**The following memory configurations will be validated and fully supported by Intel.**

**Note:**   Only the following configuration rules should be used to populate the memory module.  If other configurations are desired (as discussed in the previous configuration rules), they need be validated by the OEM.

- All banks used must be fully populated with four DIMMs

- 32 MB, 64 MB, and 256 MB DIMMs

- 50 ns or 60 ns DIMM speeds (all DIMMs installed must be of identical speed)

- 4, 8, 16, 24, or 32 DIMMs (total number of DIMMs in a dual  memory module configuration)

- 4, 8, 12, 16 DIMMs (total number of DIMMs in a single memory module and single memory terminator configuration)

- Equal number of DIMMs in each memory module in the dual memory module configuration (except when only four DIMMs are used.  In this case, the four DIMMs must be installed in Bank A of the primary memory module)

- All DIMMs on a module must be of identical size and speed

- DIMM sizes may differ between memory modules in the dual memory module configuration

To take advantage of address bit permuting (ABP), which increases memory access performance across sequential cache line accesses, the following rules must be followed:

- All banks that are used must be populated with four DIMMs.

- There must be a power of two banks populated (2, 4, or 8 banks).

- All banks in an ABP group (8 DIMMs in 2-bank permuting, 16 DIMMs in 4-bank permuting, or 32 DIMMs in 8-bank permuting) must be the same size.

- All populated banks must be adjacent and must start at bank 0.

- If there are two memory modules in the system, both must be configured to allow equivalent ABP settings. For example, the chip set cannot support 2-bank permuting on one board and 4-bank permuting on the other.

To take advantage of card-to-card interleaving (C2C), which provides maximum performance across sequential cache line accesses, the following rules must be followed:

- All ABP rules above must be followed.

- Two memory cards must be used, and corresponding banks must be identically populated with DIMMs of the same size and type.

Figure 2-12 through Figure 2-19 are given as a graphical representation of the supported configuration requirements discussed above.  These figures describe the population order only and do not specify the DIMM capacity/speed

combination requirements (refer back to the supported capacity/speed requirements given above).  Also, refer to the ABP and C2C restrictions discussed above to maximize memory data transfer performance.

Figure 2-12 through Figure 2-16 graphically describe the population order while using a dual memory module configuration.
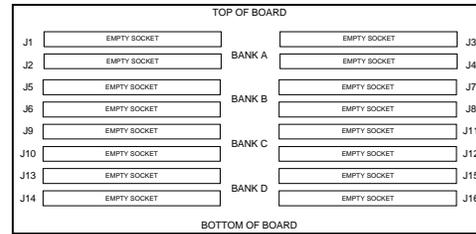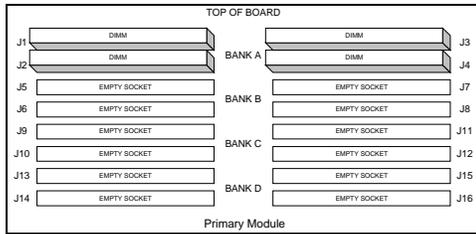
*Figure 2-12.  4:1 Interleave with 4 DIMMs (Two Memory Modules)*
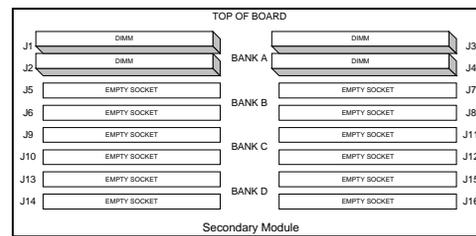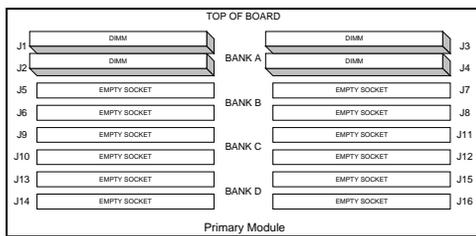
*Figure 2-13.  4:1 Interleave with 8 DIMMs (Two Memory Modules)*
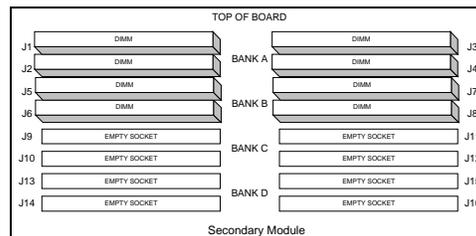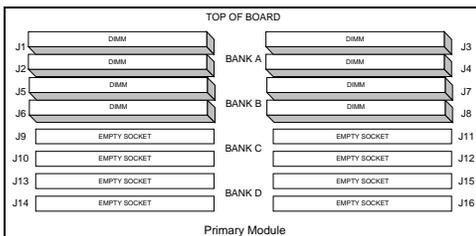
*Figure 2-14.  4:1 Interleave with 16 DIMMs (Two Memory Modules)*
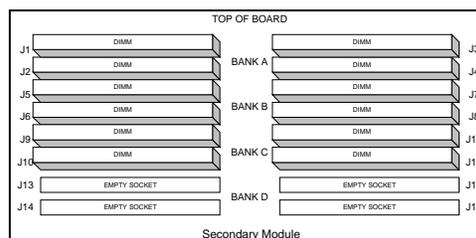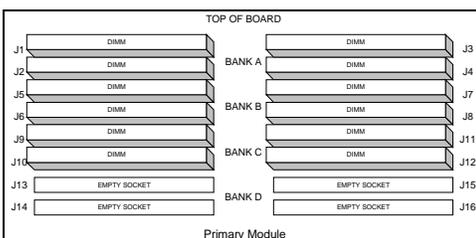
*Figure 2-15.  4:1 Interleave with 24 DIMMs (Two Memory Modules)*
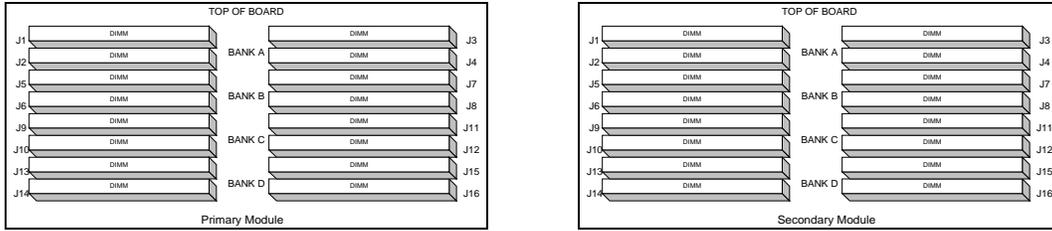
*Figure 2-16.    4:1 Interleave with 32 DIMMs (Two Memory Modules)*

Figure 2-17 through Figure 2-19 graphically describe the population order while using a single memory module and memory terminator configuration. As above, these diagrams represent only the population order of the DIMMs into the module. They do not describe capacity/speed combination requirements.
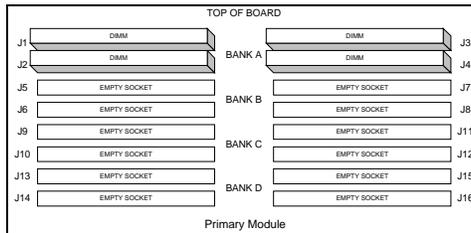


*Figure 2-17.    4:1 Interleave with 4 DIMMs (Memory Module + Terminator)*
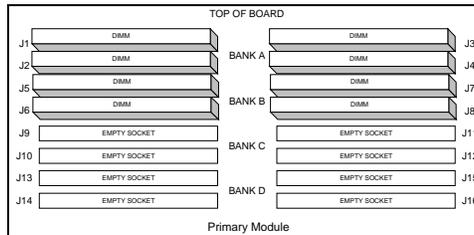


*Figure 2-18.    4:1 Interleave with 8 DIMMs (Memory Module + Terminator)*
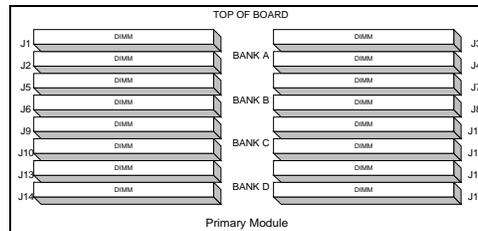


*Figure 2-19.    4:1 Interleave with 16 DIMMs (Memory Module + Terminator)*

The server management firmware scans for the speed of all DIMMs during the POST. If all DIMMs are found to contain 50-ns devices, then server management changes the DIMM speed to 50 ns. The default DIMM speed is 60 ns.

# 2.4.3   Server Management Interface

The A450NX memory module provides system management software with information about board operating temperature and DIMM configuration in addition to FRU information about the memory module itself.
This data comes from three devices that reside on the baseboard memory controller's (BMC) private $I^2C$ bus. Temperature and FRU data are provided by a Dallas DS1624* EEPROM connected to the $I^2C$ bus.  DIMM configuration data (presence, organization, size, speed, etc.) can be accessed via two Philips PCF8574A* 8-bit I/O ports.  The $I^2C$ addresses of the three devices are listed in Table 2-34.  Note that the address of a device depends on which of the two memory connectors forms the interface between the CPU baseboard and the memory module.

## 2.4.3.1   $I^2C$ Accessed Features

The memory module contains the following $I^2C$ accessible devices:

- DS1624 - Temperature sensor and SEEPROM containing FRU information
- PCF8574A - 8-bit I/O ports, which contain DIMM configuration information

These devices are accessed via the BMC on the A450NX I/O baseboard.  The $I^2C$ devices are accessible at the addresses listed in Table 2-34:

*Table 2-34.    Memory Module $I^2C$ Address Map*

| Device | Function | $I^2C$ Address | |
|---|---|---|---|
| | | Mem Slot #1 (Primary) | Mem Slot #2 (Secondary) |
| DS1624* | Memory Module Temp. Sensor & FRU Info | 9Ah | 9Eh |
| PCF8574A* | I/O Port 0 | 70h | 74h |
| PCF8574A | I/O Port 1 | 72h | 76h |

Notes:  1.  The device addresses are different depending on which slot the memory module is plugged into.
        2.  The $I^2C$ addresses are hard coded by the CPU baseboard.

The memory terminator module contains the following $I^2C$ accessible devices:

- DS1624 - Temperature sensor and SEEPROM containing FRU information

This device is accessed via the BMC on the A450NX I/O baseboard and is accessible at the addresses listed in Table 2-35:

*Table 2-35.    Memory Terminator Module $I^2C$ Address Map*

| Device | Function | $I^2C$ Address | |
|---|---|---|---|
| | | Mem Slot #1 (Primary) | Mem Slot #2 (Secondary) |
| DS1624* | Memory Terminator Module Temp. Sensor & FRU Info | 90h | 94h |

Notes:  1.  The device addresses are different depending on which slot the memory module is plugged into.
        2.  The $I^2C$ addresses are hard coded by the CPU baseboard.

### 2.4.3.1.1   DS1624* SEEPROM

The DS1624, when accessed via the $I^2C$ bus, will provide the temperature of the module, as measured at the DS1624, as well as the FRU information noted in Table 2-37.  The FRU information is read and made available by the Intel® Server Console (ISC).  The DS1624 SEEPROM has 256 bytes of programmable space, which is broken into four areas.  Table 2-36 is a list of the areas, a description of each area, and the space allocated to each area.

*Table 2-36. DS1624 SEEPROM Programming Areas*

| Area | Size | Description |
|---|---|---|
| Common Header | 8 bytes | Programming offsets to the other areas below. |
| Internal Use | 48 bytes | This area is reserved for general purpose use by the Intel® Server Management Firmware/Controllers. |
| Board Info | 80 bytes | Contains the board FRU information listed in Table 2-37. |
| Product Info | 120 bytes | Available for OEM use.† |

† The Intel provided FRU & SDR load utility allows OEMs to program any of the FRU SEEPROM on the A450NX board set. Refer to the *FRU & SDR Load Utility documentation* for more details

Table 2-37 and Table 2-38 list the board-specific FRU information that will be programmed into the board information area of the memory module and the memory terminator module EEPROMs.

*Table 2-37. FRU Information: Memory Module*

| Board Information | | | |
|---|---|---|---|
| Information | Description | Example | Notes |
| Mfg. Date/Time | Time & date of board manufacture (Value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/96) | 000f593h<br><br>(Date and time translation shown below)<br>f593h = 62867 min<br><br>= 43 Days & 947 min<br>= Feb 12, 1996, 3:47pm | 2 |
| Manufacturer | Board Manufacturer | Intel | 1 |
| Board Product Name | Board Name/Description | A450NX 16-DIMM Memory Module | 1 |
| Board Serial Number | Intel Board Serial Number | INBR42385906 | 2 |
| Board Part Number | Intel Board Part Number | 667829-201 | 2 |

**Notes:** 1. Actual value programmed into the board.
2. Example value. Actual value will vary with each board and fab revision.

*Table 2-38. FRU Information: Memory Terminator Module*

| Board Information | | | |
|---|---|---|---|
| Information | Description | Example | Notes |
| Mfg. Date/Time | Time & date of board manufacture (Value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/96) | 000f593h<br><br>(Date and time translation shown below)<br>f593h = 62867 min<br><br>= 43 Days & 947 min<br>= Feb 12, 1996, 3:47pm | 2 |
| Manufacturer | Board Manufacturer | Intel | 1 |
| Board Product Name | Board Name/Description | A450NX memory terminator module | 1 |
| Board Serial Number | Intel Board Serial Number | INBR42385906 | 2 |
| Board Part Number | Intel Board Part Number | 667829-201 | 2 |

**Notes:** 1. Actual value programmed into the board.
2. Example value. Actual value will vary with each board and fab revision.

Table 2-39 and Table 2-40 identify exactly the memory allocation within the DS1624 SEEPROM. This information is useful for those who will be accessing the hardware directly for information (e.g., BIOS developers and server management software developers).

*Table 2-39. SEEPROM EEPROM Byte Map - Memory Module*

| Address | Length | Description | Default Value |
|---|---|---|---|
| 0x00 | 1 | Common Header Format Version | 0x01 |
| 0x01 | 1 | Internal Use Area Offset (8-byte multiples) | 0x01 |
| 0x02 | 1 | Chassis Information Area Offset (8-byte multiples) | 0x00 (area not present) |
| 0x03 | 1 | Board Information Area Offset (8-byte multiples) | 0x07 |
| 0x04 | 1 | Product Information Area Offset (8-byte multiples) | 0x11 |
| 0x05 | 2 | Zero Padding | |
| 0x07 | 1 | Common Header Checksum | 0xE6 |
| 0x08 | 48 | Internal Use Area | |
| 0x38 | 1 | Board Information Area Format Version | 0x01 |
| 0x39 | 1 | Board Information Area Length (8-byte multiples) | 0x0A |
| 0x3A | 1 | Unicode Country Base | 0x00 |
| 0x3B | 3 | Manufacture Date/Time | |
| 0x3E | 1 | Board Manufacturer Type/Length Byte | 0xC5 |
| 0x3F | 5 | Board Manufacturer (ASCII) | 'Intel' |
| 0x44 | 1 | Product Name Type/Length Byte | 0xDC |
| 0x45 | 28 | Product Name | 'A450NX 16-DIMM Memory Module' |
| 0x61 | 1 | Board Serial Number Type/Length Byte | 0xCC |
| 0x62 | 12 | Board Serial Number | ………… |
| 0x6E | 1 | Board Part Number Type/Length Byte | 0xCA |
| 0x6F | 10 | Board Part Number | ………. |
| 0x79 | 1 | No More Fields Flag | 0xC1 |
| 0x7A | 13 | Zero Padding | |
| 0x87 | 1 | Board Information Area Checksum | 0x93 |
| 0x88 | 120 | Product Information Area | |

*Table 2-40. SEEPROM Byte Map - Memory Terminator Module*

| Address | Length | Description | Default Value |
|---|---|---|---|
| 0x00 | 1 | Common Header Format Version | 0x01 |
| 0x01 | 1 | Internal Use Area Offset (8-byte multiples) | 0x01 |
| 0x02 | 1 | Chassis Information Area Offset (8-byte multiples) | 0x00 (area not present) |
| 0x03 | 1 | Board Information Area Offset (8-byte multiples) | 0x07 |
| 0x04 | 1 | Product Information Area Offset (8-byte multiples) | 0x11 |
| 0x05 | 2 | Zero Padding | |
| 0x07 | 1 | Common Header Checksum | 0xE6 |
| 0x08 | 48 | Internal Use Area | |
| 0x38 | 1 | Board Information Area Format Version | 0x01 |
| 0x39 | 1 | Board Information Area Length (8-byte multiples) | 0x0A |
| 0x3A | 1 | Unicode Country Base | 0x00 |

| Address | Length | Description | Default Value |
|---------|--------|-------------|---------------|
| 0x3B | 3 | Manufacture Date/Time | |
| 0x3E | 1 | Board Manufacturer Type/Length Byte | 0xC5 |
| 0x3F | 5 | Board Manufacturer (ASCII) | 'Intel' |
| 0x44 | 1 | Product Name Type/Length Byte | 0xDF |
| 0x45 | 31 | Product Name | 'A450NX Memory Terminator Module' |
| 0x64 | 1 | Board Serial Number Type/Length Byte | 0xCC |
| 0x65 | 12 | Board Serial Number | ………… |
| 0x71 | 1 | Board Part Number Type/Length Byte | 0xCA |
| 0x72 | 10 | Board Part Number | ……… |
| 0x7C | 1 | No More Fields Flag | 0xC1 |
| 0x7D | 10 | Zero Padding | |
| 0x87 | 1 | Board Information Area Checksum | 0x29 |
| 0x88 | 120 | Product Information Area | |

Temperature and EEPROM data may be accessed via $I^2C$ commands to the DS1624 device.  Table 2-41 is taken from the DS1624 data sheet.

*Table 2-41.     EEPROM Command Set*

| INSTRUCTION | DESCRIPTION | PROTOCOL | 2-WIRE BUS DATA AFTER ISSUING PROTOCOL | NOTES |
|-------------|-------------|----------|----------------------------------------|-------|
| TEMPERATURE CONVERSION COMMANDS | | | | |
| Read Temperature | Read last converted temperature value from temperature register. | AAh | <read 2 bytes data> | |
| Start Convert T | Initiates temperature conversion. | EEh | idle | |
| Stop Convert T | Halts temperature conversion. | 22h | idle | |
| MEMORY COMMANDS | | | | |
| Access Memory | Reads or writes to 256-byte EEPROM memory. | 17h | <write data> | |
| Access Config | Reads or writes configuration data to configuration register. | ACh | <write data> | |

# 2.5   Interconnect Backplane

This section describes the features of the A450NX interconnect backplane.  The interconnect backplane connects the CPU baseboard and the I/O baseboard of the A450NX via a primary and secondary F16 bus, using server management and other miscellaneous signals.  It also provides an interface to the power supply subsystem, as well as power and power filtering to the CPU and I/O baseboards.

## Features

- 400 MB/s bandwidth per F16 bus at 100 MHz bus frequency

- Cableless interface between CPU and I/O baseboards

- Power distribution to CPU and I/O baseboards

- Interface between I/O baseboard and power distribution system

- Passive power transient filtering via bulk decoupling capacitors for +5 V and +12 V

- Power-cable fault detect

## 2.5.1   Board Overview

The primary components on the interconnect backplane are the two male connectors;  these connectors provide the high speed signal interconnects between, as well as power distribution to, the CPU and I/O baseboards.  These connectors are the Futurebus style manufactured by Berg.  There are three Molex Mini-Fit, Jr.* 24-pin connectors that connect to the power distribution system's power cables.  A secondary 34-pin connector is present for server management signal connections and other miscellaneous signals to the power distribution system.

Figure 2-20 diagrams the major components of the A450NX interconnect backplane, their interconnections, and their approximate locations on the board.  Note that the capacitors, power connectors and server management connector are placed on the primary side of the board, whereas the Berg Futurebus connectors are on the secondary side of the board.

# Interconnect Backplane
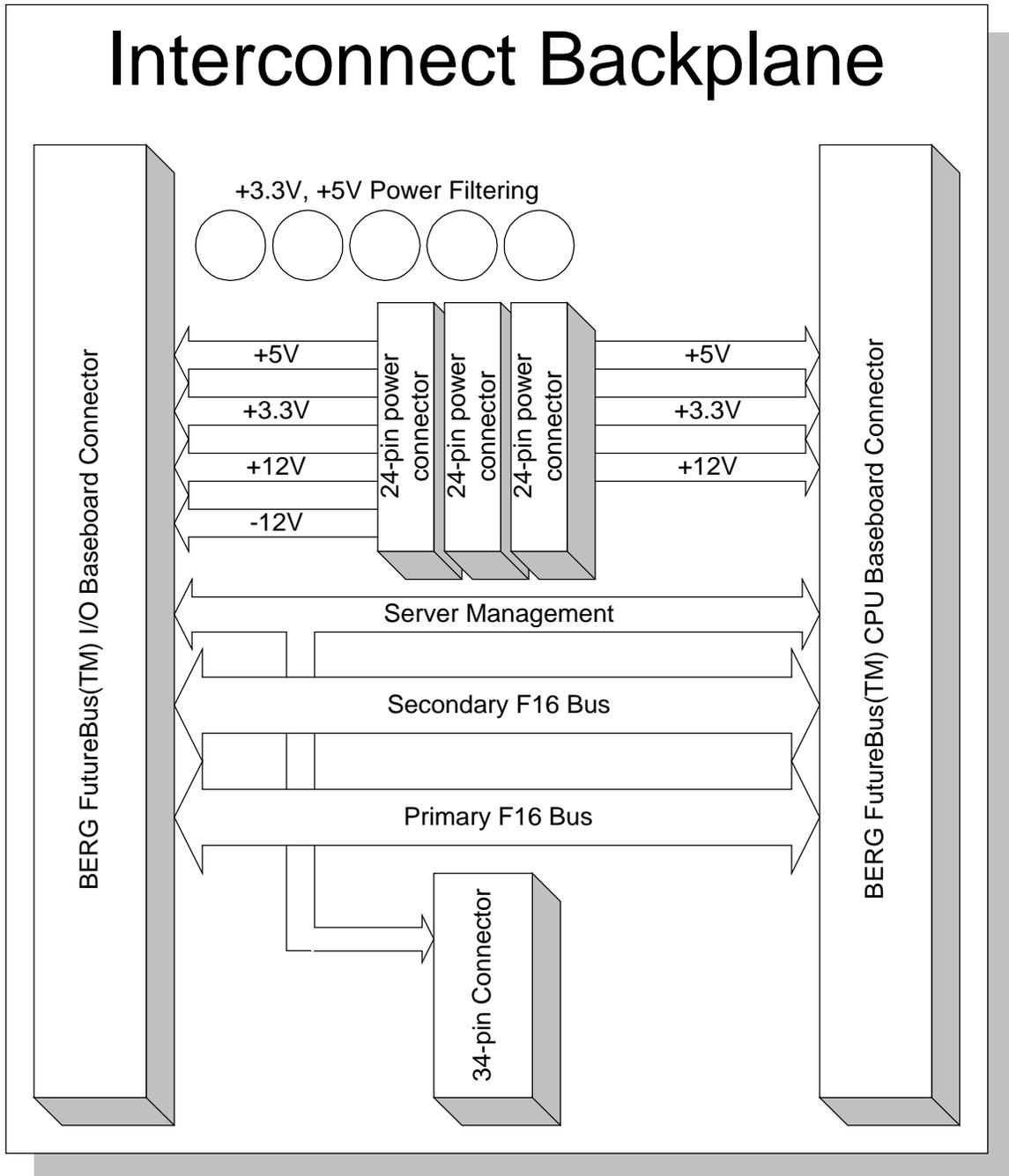


*Figure 2-20.  A450NX Interconnect Backplane Components*

## 2.5.2  Power Cable Fault Detect

The three Molex Mini-Fit Jr. connectors' -12 V line also provide a mechanism to detect a cable fault.  The fault generally occurs when a power cable has not been plugged in properly, when one or more of the -12 V lines has been severed, or when the -12 V source from the power distribution backplane (in the case of an AD450NX server system) is not valid.  The current for -12 V is provided from the power distribution backplane (or other power supply system) via one cable; two return paths are provided via the other two cables.  (See Figure 2-21.)
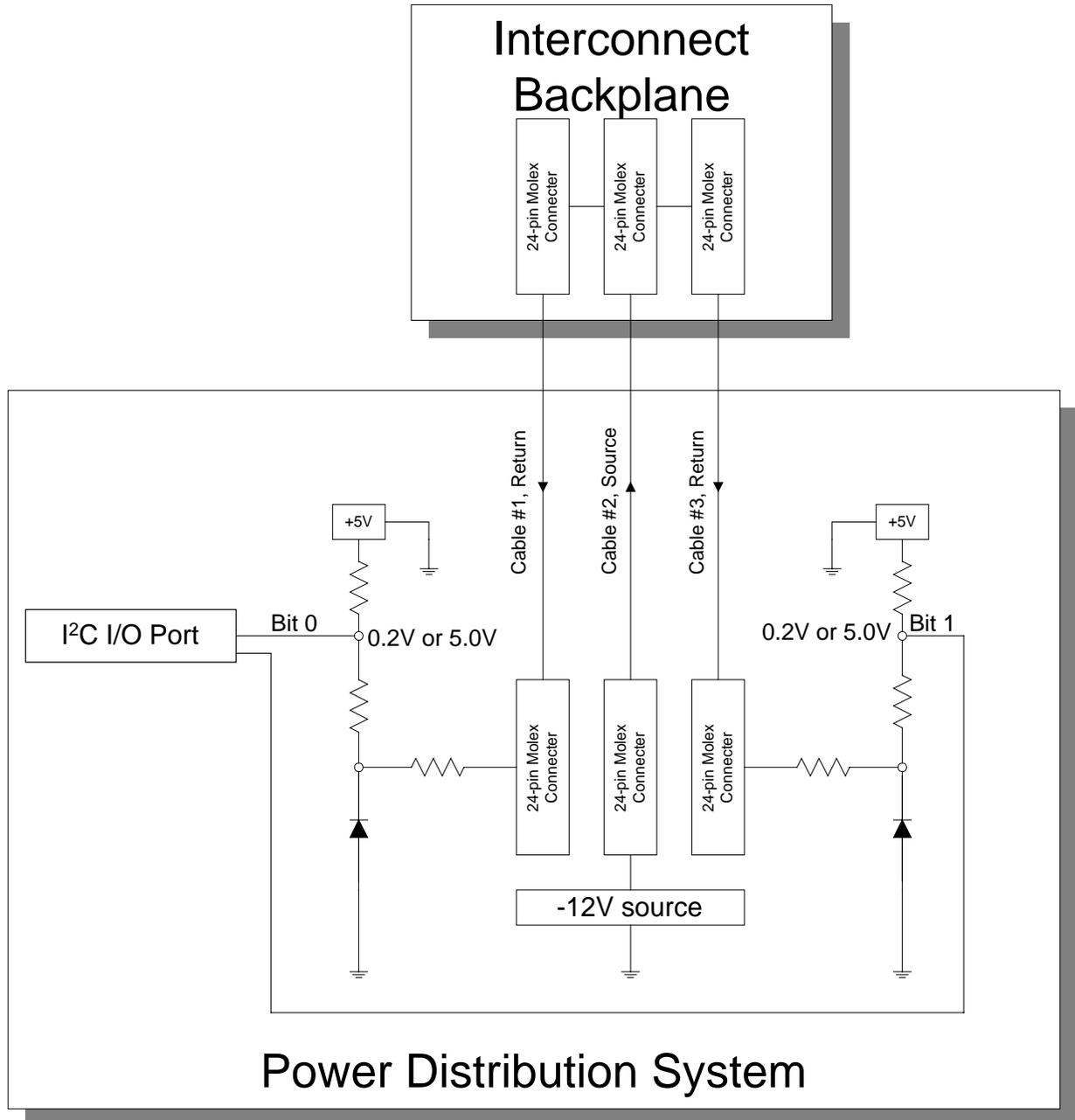
**Note:** The power distribution system shown in the above diagram is not a part of the A450NX board set and must be provided by the system integrator.

*Figure 2-21.    Power Cable Fault Detect*

Voltage-sensing circuitry in the power distribution system detects the presence or absence of one or both voltage returns and provides server management with this two bits of information.

Only when all three cables are plugged in, are intact, and the -12 V supply is good, will both bits be asserted. (Assume an asserted bit indicates a good cable and supply.)  A faulty center-cable (-12 V *source*) or *both* faulty side-cables (-12 V *return*) will deassert both bits.  A good source cable and *one* faulty side-cable will produce one asserted and one deasserted bit, depending on which side cable is faulty.  (See Figure 2-21 and Table 2-42.)  Since the current drawn from the -12 V will be limited, one cable is sufficient to supply this current.  Such a mechanism

also allows all three cables from the power distribution system to the interconnect backplane to be identical, making assembly easier and more reliable.

Table 2-42 shows the logic that describes the inferred state of the power cables based on information obtained from the power cable fault detect mechanism.

*Table 2-42.    Power Cable Fault Detect Logic*

| Bit 0 | Bit 1 | Meaning |
|-------|-------|---------|
| 0 | 0 | All three cables are intact and the -12 V supply is good |
| 0 | 1 | Cable 3 is severed or disconnected.  Cables 1, 2, and -12 V supply are good |
| 1 | 0 | Cable 1 is severed or disconnected.  Cables 2, 3, and -12 V supply are good |
| 1 | 1 | Cable 2 and/or cables 1 and 3 is/are severed or disconnected, or -12 V supply is not good |

# 2.5.3   $I^2C$ Accessed Features

The interconnect backplane holds a 256-byte SEEPROM device, which resides on the BMC private $I^2C$ bus.  This device, an Atmel 24C02*, is accessed via the BMC on the I/O baseboard.  The 24C02 device is accessible at the addresses shown in Table 2-43:

*Table 2-43.    Interconnect Backplane $I^2C$ Address Map*

| Device | Function | $I^2C$ Address |
|--------|----------|----------------|
| 24C02 | Interconnect Backplane FRU Info | A2h, A3h |

The 24C02, when accessed via the $I^2C$ bus, provides the FRU information shown in Table 2-45.  The FRU information is read and made available by the Intel® Server Console (ISC).

The 24C02 SEEPROM has 256 bytes of programmable nonvolatile memory, which is broken into four areas.  Table 2-44 provides a list of the areas, a description of each area, and the space allocated to each area.

*Table 2-44.    24C02 SEEPROM Programming Areas*

| Area | Size | Description |
|------|------|-------------|
| Common Header | 8 bytes | Programming offsets to the other areas below |
| Internal Use | 48 bytes | This area is reserved for general-purpose use by the Intel® Server Management Firmware/Controllers. |
| Board Info | 80 bytes | Contains the board FRU information listed in Table 2-45. |
| Product Info | 120 bytes | Available for OEM use.† |

† An FRU & SDR Load Utility is provided by Intel that allows OEMs to program this area.  Refer to the *FRU & SDR Load Utility* documentation for details.

Table 2-45 lists the board specific FRU information that will be programmed into the board information area.

*Table 2-45.    FRU Information*

| Board Information | | | |
|-------------------|--|--|--|
| Information | Description | Example | Notes |
| Mfg. Date/Time | Time & date of board manufacture (value programmed (in hex) is the number of minutes after 0:00 | 000f593h (Date & time translation shown below) f593h = 62867 min = 43 days & 947 min | 2 |

| Board Information | | | |
|---|---|---|---|
| **Information** | **Description** | **Example** | **Notes** |
| | hrs 1/1/96) | = Feb 12, 1996, 3:47pm | |
| Manufacturer | Board Manufacturer | Intel | 1 |
| Board Product Name | Board Name/Description | A450NX Interconnect Backplane | 1 |
| Board Serial Number | Intel Board Serial Number | INBR42385906 | 2 |
| Board Part Number | Intel Board Part Number | 6650049-002 | 2 |

**Notes:** **1.** Actual value programmed into the board.

**2.** Example value.  Actual value will vary with each board and fab revision.

Table 2-46 identifies exactly which bytes are allocated to what purpose within the 24C02 SEEPROM.  This information is useful for those who will be accessing the hardware directly for information (e.g., BIOS developers and server management software developers).

*Table 2-46.     SEEPROM Byte Map*

| Address | Length | Description | Default Value |
|---|---|---|---|
| 0x00 | 1 | Common Header Format Version | 0x01 |
| 0x01 | 1 | Internal Use Area Offset (8-byte multiples) | 0x01 |
| 0x02 | 1 | Chassis Information Area Offset (8-byte multiples) | 0x00 (area not present) |
| 0x03 | 1 | Board Information Area Offset (8-byte multiples) | 0x07 |
| 0x04 | 1 | Product Information Area Offset (8-byte multiples) | 0x11 |
| 0x05 | 2 | Zero Padding | |
| 0x07 | 1 | Common Header Checksum | 0xE6 |
| 0x08 | 48 | Internal Use Area | |
| 0x38 | 1 | Board Information Area Format Version | 0x01 |
| 0x39 | 1 | Board Information Area Length (8-byte multiples) | 0x0A |
| 0x3A | 1 | Unicode Country Base | 0x00 |
| 0x3B | 3 | Manufacture Date/Time | |
| 0x3E | 1 | Board Manufacturer Type/Length Byte | 0xC5 |
| 0x3F | 5 | Board Manufacturer (ASCII) | 'Intel' |
| 0x44 | 1 | Product Name Type/Length Byte | 0xDD |
| 0x45 | 29 | Product Name | 'A450NX Interconnect Backplane' |
| 0x62 | 1 | Board Serial Number Type/Length Byte | 0xCC |
| 0x63 | 12 | Board Serial Number | ............ |
| 0x6F | 1 | Board Part Number Type/Length Byte | 0xCA |
| 0x70 | 10 | Board Part Number | .......... |
| 0x7A | 1 | No More Fields Flag | 0xC1 |
| 0x7B | 12 | Zero Padding | |
| 0x87 | 1 | Board Information Area Checksum | 0xE9 |
| 0x88 | 120 | Product Information Area | |

# 3. BIOS Features

This chapter describes the features of the A450NX BIOS. The BIOS features are grouped into categories and are described in the following sections.

# 3.1 Ease-of-use Features

The following sections discuss the ease-of-use features of the A450NX BIOS.

## 3.1.1 Plug and Play

The A450NX BIOS supports the following industry standards for full Plug and Play compatibility:

- *Plug and Play ISA Specification, Rev. 1.0a*
- *System Management BIOS (SMBIOS) Specification, Ver. 2.1*
- *Extended System Configuration Data Specification, Rev. 1.02A*
- *Peripheral Component Interconnect (PCI) Local Bus Specification, Rev. 2.1 (PCI, Rev 2.1)*

**Note:** The A450NX BIOS does not support auto-detection of floppy-drive type, but IDE drives and floppy media are automatically detected.

### 3.1.1.1 Resource Allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Intel® servers. The BIOS scans for the following in the order listed:

1. **ISA devices.** If an ISA device is found, it is initialized and given resource priority over other devices of the same type, which are plugged into the system.
2. **Add-in PCI devices (e.g., PCI adapter cards).** If found, the BIOS initializes and allocates resources to these devices.
3. **Onboard video, IDE, and SCSI devices.** If equivalent functionality is not found offboard, the BIOS will allocate resources according to the parameters set up by the System Setup Utility (SSU). The add-in video adapter in the ISA bus or PCI bus 0 takes precedence over the onboard video controller.

### 3.1.1.2 PCI Auto-configuration

The A450NX BIOS supports the INT 1Ah, AH = B1h functions, in conformance with the *PCI Rev. 2.1*. System POST performs auto-detection and auto-configuration of ISA, ISA Plug-n-Play, and PCI devices. This process maps each device into memory and/or I/O space, and assigns IRQs and DMA channels as required, so that there are no conflicts prior to booting the system. Drivers and operating system (OS) programs can determine the installed devices and their assigned resources using the BIOS interface functions. In general, the PCI devices are scanned and initialized from low device number to high device number (and also low to high bus number) as shown below. However, scan and boot order may be affected by the implementation of the *BIOS Boot Specification, Ver. 1.00*. See the section called *Boot Device Selection and Ordering* in this chapter.

Devices on the PCI bus are initialized in the following order:

1. On the primary 32-bit PCI bus [PXB0-A]:
   **SLOT0 -> onboard SCSI -> SLOT1 -> onboard VIDEO**
2. On the secondary 32-bit PCI bus [PXB0-B]:
   **SLOT0 -> SLOT1 -> SLOT2 -> SLOT3**

3. On the 64 bit PCI bus (third bus) [PXB1-A]
   **SLOT0 -> SLOT1 -> SLOT2 -> SLOT3 -> SLOT4**

Note the naming/numbering convention of the PCI buses attached to the host bus. The BIOS may enumerate the buses differently based on the type and number of PCI cards installed in the system. For example, if there are a number of cards with PCI-to-PCI bridges installed in the slots, it will affect the bus numbering, including the host PCI bus numbers. So, for clarity, we will refer to bus PXB0-A, bus PXB0-B, and bus PXB1-A when referring to the host PCI buses. An example of PCI bus enumeration follows.

*Example 1:*

If there were no PCI devices in any of the slots that had PCI-to-PCI bridges on them, the buses would be enumerated as follows:

| Physical PCI Bus | Enumerated PCI Bus |
|---|---|
| 0-A | 0 |
| 0-B | 1 |
| 1-A | 2 |

*Example 2:*

If there were PCI devices in bus 0A and bus 0B that had PCI-to-PCI (P2P) bridges on them, the buses would be enumerated as follows:

| Physical PCI Bus | Enumerated PCI Bus |
|---|---|
| 0-A | 0 |
| P2P bridge on 0-A | 1 |
| 0-B | 2 |
| P2P bridge on 0-B | 3 |
| 1-A | 4 |

The PCI interrupts are routed to ISA IRQs or IOAPIC through the PID ASIC. The PID supports IRQ map registers that are used to map PCI IRQ to ISA IRQ.

## 3.1.1.3   Legacy ISA Configuration

The SSU is provided to help the user configure the legacy ISA devices. The SSU allows the end user to reserve the legacy ISA system resource and save the information into extended system configuration data (ESCD) nonvolatile random access memory (NVRAM). The POST resource management will not allocate the resources that are reserved for legacy ISA cards to PnP devices.

## 3.1.1.4   Onboard Device Auto-configuration

The A450NX BIOS detects all onboard devices and assigns appropriate resources. The BIOS dispatches the option ROM code for the onboard devices to the DOS compatibility region (C0000h to DFFFFh) and transfers control to the entry point, if enabled by the user.

## 3.1.1.5   Automatic Detection of Video Adapters

The A450NX BIOS looks for video adapters in the following order:
   1. ISA
   2. PCI
   3. Onboard, I/O baseboard

The onboard (or offboard) video BIOS is shadowed starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to add-in devices. Some video adapters request resources in the compatibility range. Only adapters on PCI bus 0-A, which are requesting compatibility resources, will be given the resources. Adapters that require compatibility resources cannot be placed on PCI bus 0-B or bus 1-A. Adapters behind a PCI-to-PCI bridge cannot request compatibility resources. Refer to *PCI Rev 2.1* for the limitations.

A special VGA devnode option is provided in the BIOS setup to support PCI legacy VGA cards, which are not PCI 2.x compliant.  When this option is enabled, the BIOS reserves up to 0x9000h address of I/O for Bus 0-A.  This should be used for debug purposes only.  By enabling this option, the user should be aware of the limitations of accommodating large I/O configurations on Bus 0-B and Bus 1-A.

## 3.1.2   Auto-detection of Processor Type and Speed

The A450NX BIOS automatically detects the processor stepping(s) installed in the system and configures the system accordingly.  The BIOS detects the processor speed for all processors based on a jumper setting on the A450NX CPU baseboard.  The BIOS displays the number of processors, and their speed prior to booting the operating system. It is preferred that all processors installed in a system be the same speed and same stepping; however, the BIOS allows the mixing of stepping under certain conditions.  See the section called Multiple Processor Speed Support in this chapter for more details.

## 3.1.3   Mouse and Keyboard Port Swapping

The A450NX BIOS allows users to plug the keyboard or PS/2 mouse connectors into either PS2 port on the I/O riser card.  It detects and initializes the keyboard and mouse accordingly.

## 3.1.4   Memory Sizing

During POST the BIOS:

- Tests and sizes memory
- Configures the memory controller

The memory-sizing algorithm determines the size of each row of DIMMs.  The BIOS always initializes ECC memory.  The BIOS is capable of detecting, sizing, and testing any amount of RAM, up to the physical maximum of 8 GB.  The BIOS is capable of reporting up to 64 MB using INT 15h, AX = 88h.  It can report up to 4 GB using INT 15h, function E801h.  Using INT 15h, function E820h, the BIOS can report system memory regions up to the physical maximum of 8 GB.

The A450NX BIOS reclaims all the memory lost due to PCI allocation, APIC and BIOS flash region, if there is more than 4 GB of system memory.  The BIOS supports full remapping and 2/4 way address bit permuting (ABP).  The BIOS also provides a setup option to select memory testing every DWORD, a DWORD every KB or a DWORD every MB.  Selecting memory testing a DWORD every MB increases the boot speed.  The ABP feature can be disabled using the BIOS Setup.

## 3.1.5   LCD Display

The A450NX BIOS supports a front panel LCD for the display of informative messages.  During POST the BIOS displays memory sizing information, BIOS revision information, cache size, keyboard and mouse presence, and POST error codes.

## 3.1.6   Boot Delay

The boot delay feature can be selected from setup through the advanced options menus.  It provides a five second delay towards the end of POST.  Its purpose is to allow the user to view all messages displayed by the BIOS during POST.

## 3.1.7    I₂O Support

Intelligent I/O (I$_2$O) defines a standard architecture for intelligent I/O, an approach to I/O in which low level interrupts are off loaded from the CPU to I/O processors (IOP).  IOPs are designed specifically to handle I/O with support for message passing between multiple independent processors.  The A450NX BIOS supports run-time services for I$_2$O devices.

## 3.1.8    ACPI Support

The Advanced Configuration and Power Interface (ACPI) specification is the key element in Operating System Directed Power Management (OSPM).  The OSPM provides support for an orderly transition from existing (legacy) hardware to ACPI hardware.  The ACPI interface gives the OS direct control over the power management and Plug and Play functions of the computer.

A450NX BIOS supports S1 Sleeping State & S4 Sleeping State.  The power button and (Power Management Event (PME) WakeOnLan (WOL) can wake from S1.  Until an OS sends a command to SWITCH TO ACPI Mode, the power button acts as a power switch.  While entering ACPI mode, the BIOS communicates with the front panel controller to switch into ACPI mode.  In this mode, the power button acts as both a sleep button and a power button. If the power button is pressed momentarily (less than 4 sec) the PIIX4E treats it as a sleep button and informs the OS/AML (ACPI machine language) to switch to S1 state.  If the power button is pressed for more than 4 seconds, it is treated as a power cycle and the system is powered down.  The power button can also be configured via the OS to enter hibernation.

### 3.1.8.1    Implementation Details Of S1

S1 sleep state can be entered by pressing the power button or by direction from the OS.  In this state no system context is lost, including CPU, caches, memory and all chip set I/O.  Momentarily pressing the power button wakes the system from S1 state.  The PME WOL feature of the A450NX is implemented only for S1 state.

### 3.1.8.2    Implementation Details Of S4

The S4 sleeping state is the lowest power, longest wakeup latency sleeping state supported by ACPI.  State S4 is also called SaveToDisk (STD).  This state can be entered either by pressing the power button, if the power button is configured for hibernation under the OS, or from the hibernate option in OS shut-down menu.  If this state is invoked, the OS will store to the hard drive the context of all processes such as applications, memory, chip set, and processor, and then it will power down the system.  When system power is reinitiated, the OS restores all the processes from the disk including the launching of all of the applications.

# 3.2    Performance Features

For enhanced performance, the A450NX BIOS supports the features discussed in the following section.

## 3.2.1    Symmetric Multiprocessor Support

The A450NX BIOS complies with all requirements of the *Intel® Multiprocessor Specification (MPS), version 1.4*, for symmetric multiprocessing support, as well as *Intel® Multiprocessor Specification (MPS), version 1.1*, for backward compatibility.  The version number can be configured using the Configuration Utilities (CU).

### 3.2.1.1    Multiple Processor Support

On reset, all the processors compete to become the bootstrap processor (BSP). If a serious error is detected on a processor during built-in-self-tests (BIST), that processor does not participate in the initialization protocol.  The first processor (typically with the highest APIC ID) that successfully passes BIST is automatically selected by the

hardware as the BSP and starts executing from the reset vector (F000:FFF0h). A processor that does not perform the role of BSP is referred to as an application processor (AP).

The BSP is responsible for executing the POST and preparing the machine to boot the OS. The A450NX BIOS performs several other tasks in addition to those required for MPS support, as described in the *Intel® Multiprocessor Specification (MPS), Version* 1.4. These tasks are part of the fault resilient booting algorithm. At the time of booting, the system is in virtual wire mode and the BSP alone is programmed to accept local interrupts (INTR driven by the programmable interrupt controller (PIC) and the nonmaskable interrupt). As a part of the boot process, the BSP wakes up the APs. When awakened, the APs program their memory type range registers (MTRR) to be identical to those of the BSP. All APs execute a halt instruction with their local interrupts disabled.

### 3.2.1.2    Multiple Processor Speed Support

The A450NX BIOS supports processors with various clock frequencies without changes to the BIOS, but only across different system configurations. All installed processors in any one system must run at the same frequency (i.e., the bus and core frequencies of all processors must be the same). This is guaranteed by a jumper setting on the CPU baseboard, which programs the core to bus frequency ratio for all processors in the system.

Though Intel recommends using identical stepping of processor silicon in multiprocessor systems whenever possible (as this is the only configuration that receives full validation across all of Intel's testing), the BIOS does support mixing processor stepping. However, the support of mixed stepping will be limited to those steppings that do not have known incompatibilities. Typically, each new stepping of a device is fully validated only against the latest stepping of other processors and chip set components.

The A450NX BIOS does not support mixing processor cache sizes. The BIOS reports and logs an error for mixed stepping.

## 3.2.2    Cache

By default, the A450NX BIOS enables the L1 and L2 caches to write-back mode for all main system memory. The system shadow memory is initialized to be cached but write protected. In this case, it will not generate memory write cycles, which may destroy the shadow memory or cause a bad cycle.

Some video memory buffers can be initialized with uncacheable-speculative-write-combining (USWC) memory attribute, which combines the line memory cycle into a burst memory cycle to speed up video buffer performance. All other memory outside of the main system memory is initialized as not cacheable.

## 3.2.3    Memory Speed Optimization

The memory DIMM speed is obtained from server management via the BMC private management bus. The default memory DIMM speed is 60 nanoseconds (ns). Therefore, if memory DIMM speeds are mixed, or if the speed of all the DIMMs is 60 ns, the speed setting remains at the slower default value of 60 ns. If, however, the memory speed of **all** DIMMs is found to be 50 ns, the A450NX BMC program resets the DIMM speed to 50 ns.

## 3.2.4    Option ROM Shadowing

All onboard adapter ROMs and PCI adapter ROMs are shadowed into RAM in the ISA-compatible ROM adapter memory space between C0000h to DFFFFh. Cacheable BIOS ROMs found on ISA devices are shadowed into adapter memory space in the same range after initialization. PCI BIOS ROMs are always shadowed. The memory hole from 15 MB-16 MB will not be supported by the BIOS.

# 3.3   Security Features

The A450NX BIOS provides a number of security features.  This section describes the security features and operating model.  Some of these events, such as entering secure mode via a hot key, cannot take place unless the keyboard is connected to the KBC, and will not be supported when the keyboard is connected to a USB port.

## 3.3.1   Operating Model

Table 3-1 summarizes the operation of security features supported by the A450NX BIOS.

*Table 3-1.        Security Features Operating Model*

| Mode | Entry Method/Event | Entry Criteria/Qualifier | Behavior | Exit Criteria | After Exit |
|------|--------------------|--------------------------|----------|---------------|------------|
| Secure mode | Keyboard inactivity timer; programming of KBC hot key | User password/ KBC inactivity timer (set by CU) | • Screen goes blank (if enabled in Setup)<br>• Floppy writes are disabled (if selected in Setup)<br>• Power and reset switches on front panel are disabled<br>• No mouse or keyboard input is accepted | User password | • Video is restored<br>• Floppy writes are enabled<br>• Power and reset switches are enabled<br>• Keyboard and mouse inputs are accepted |
| Secure boot | Power On/Reset | User password/ secure boot enabled in CU | • Boots drive C: if drive A is empty<br>• Prompts for password, if drive A is not empty<br>• Video is blanked (if enabled in Setup)<br>• Floppy writes are disabled (if selected in Setup)<br>• Power and reset switches on the front panel are disabled<br>• No mouse or keyboard input is accepted | User password | • Floppy writes are enabled<br>• Power and reset switches are enabled<br>• Keyboard and mouse inputs are accepted<br>• System attempts to boot from drive A |
| User password boot (AT style) | Power On/Reset | User password/ secure boot disabled in CU | • System halts for user password before booting<br>• Video is blanked (if enabled in Setup)<br>• Floppy writes are disabled (if selected by Setup)<br>• Power and reset switches on the front panel are disabled<br>• No mouse or keyboard input is accepted. | User password | • Power and reset-switches are enabled<br>• Keyboard and mouse inputs are accepted<br>• Boot sequence is determined by Setup options |
| Power and reset switch lockout | Same as secure mode above | User-programmed option (using Setup) | Power and reset buttons are disabled on front panel | User clears option | Power and reset switches enabled |

# 3.3.2   Password Protection

Through the use of passwords, BIOS prevents unauthorized tampering with the system.  Once secure mode is enabled, access to the system is allowed only after the correct password(s) is entered.  Each of two passwords, for user and supervisor, can be created during system configuration using the ROM based Setup Utility.

If only a user password is set (no supervisor password), this password is the only one required to boot the machine or run Setup.  If both passwords are enabled, either password can be used to boot the machine or enable the keyboard and/or mouse, but only the supervisor password allows the system configuration to be changed using Setup.

The supervisor password is provided as a means to control access to the basic system configuration independently of other access controls.  For example, the system hardware configuration can be controlled by a supervisor while others control access to the machine's file system.

Once set, a password can be disabled by deleting it in Setup or by setting the Clear Password jumper on the I/O baseboard.

## 3.3.2.1   Inactivity Timer

If the inactivity timer function is enabled, and no keyboard or mouse actions have occurred for the specified time-out period, the following occurs until the user password is entered:

- Keyboard and mouse input is inhibited
- Video is blanked (if programmed in CU)
- Floppy drive is write protected (if enabled)
- Front panel buttons locked out (if enabled)

Using the CU, the user may specify a time-out period of 1 to 120 minutes.

## 3.3.2.2   Hot Key Activation

A hot key can activate secure mode immediately, rather than having to wait for the inactivity time-out to expire.  The hot key combination is set using the CU.

## 3.3.2.3   Password Clear Switch

The BIOS reads the password clear switch (located on the I/O baseboard) to determine if it is set.  If set, both user and administrator passwords are cleared from CMOS and password protection is disabled.

# 3.3.3   Boot Without Keyboard

The system can boot with or without a keyboard.  The BIOS displays whether it detected a keyboard or not before booting.  There is no entry in the CU for keyboard enable/disable.  The presence of the keyboard is detected automatically during POST, and the keyboard is tested if present.

# 3.3.4   Floppy Write Protection

If enabled in Setup, floppy disk writes are disabled when the system is in secure mode.  Floppy write protection is only in effect while the system is in secure mode.  Otherwise, write protection is disabled.

# 3.3.5   Front Panel Lock

If Front Panel Lock is enabled in Setup, the front panel, power switch and reset button, are disabled when in secure mode.

## 3.3.6   Secure Boot Mode

Secure boot mode lets the system boot and run the OS, but no mouse or keyboard input is accepted until the user password is entered.  Setup is used to enable the secure boot mode feature.  In secure boot mode, if the BIOS detects a floppy disk in the A drive at boot time, it prompts the user for a password.  When the password is entered, the system can boot from the floppy and secure mode is disabled.  Any one of the secure mode triggers, as described in Table 3-1 will cause the system to go back into secure mode.  If there is no disk in drive A, the system boots from the C drive and is placed in secure mode automatically.  All of those secure mode features which are enabled go into effect at boot time.

## 3.3.7   Video Blanking

If enabled in Setup, the video display will be off when the system is in secure mode.  Exiting secure mode will enable the video display.  While the video is blank, the user must enter the password to exit secure mode.

# 3.4   Reliability Features

The A450NX BIOS supports several features to create a robust computing environment.  These features are described in the following sections.

## 3.4.1   Defective DIMM Detection and Remapping

The ECC memory subsystem on the A450NX board set is able to detect single-bit errors (SBE) and multi-bit errors (MBE) during reads from and writes to system DRAM.  SBEs can be detected and corrected, whereas MBEs can be detected but cannot be corrected.

During POST memory testing, detection of single-bit and multi-bit errors in DRAM banks is enabled.  If an error is detected during POST, the bad location is avoided by reducing the usable memory in that bank so that the byte containing the hard error is no longer accessible.

Depending on where exactly the error is, BIOS divides down the bank size by 2, thereby lowering the top of the bank until the failing location is above the newly lowered top of bank.  This continues until a worst case bank size of 0 is reached.  With a max of 1 GB supported per bank, the minimum loss per bank will be 512 MB and the maximum will be 1 GB per bank.

The defective DIMM detection and memory remapping is done automatically by the BIOS during the POST and does not require any user intervention.  The BIOS logs the errors in the nonvolatile system event log.

DIMM speed is programmed by the BMC firmware.

### 3.4.1.1   Memory Configuration Algorithm

BIOS requires at least 64 MB of good memory to start up.  If there is no DIMM population or all DIMMs are bad, the BIOS sounds a beep code error (1-3-3-1) and POST is terminated.

It should be noted that during this memory size detection process, the BIOS does not distinguish between absent DIMMs and bad DIMMs.  Although single-bit errors are correctable errors, they are considered serious enough to remove the entire bank altogether.  This bank removal process continues iteratively for all banks until the BIOS finds at least 64 MB of memory good in one bank, or if all banks have been removed, it emits the 1-3-3-1 beep code and halts the system.  A bank is removed if any of the four DIMMs that make up the bank have any error, single or multiple bit.

In the event that the BIOS disables or resizes a bank during POST, an error message displays with the DIMM and board numbers of the failing memory.  Elimination of hard errors in this way during POST is done as a precaution to

prevent an SBE from becoming an MBE after the system has booted and to prevent SBEs from being detected and logged each time the failed location(s) are accessed.

DIMM resizing during POST comes with a restriction. If address-bit permuting (ABP) and/or card-to-card (C2C) interleaving have been turned on, resizing is not possible. However, error messages are still displayed at the end of POST, and errors are still logged.

After POST memory testing, automatic scrubbing of SBEs is enabled in the MIOC. If an error is a single-bit error, the 450NX automatically corrects the data before it is returned. If the error is an MBE, the condition is considered fatal and, after the error is logged, an NMI is generated telling the OS to handle this fatal error.

## 3.4.2 Logging Critical Events

If enabled by the CU, the A450NX BIOS has the ability to log critical and informational events to nonvolatile memory. The event log area is managed by the BMC and can be accessed by sending IPMB commands to the BMC. A critical event is one that may result in the system being shut down to prevent catastrophic side effects from propagating to other parts of the system. Multi-bit and parity errors in the memory subsystem are considered critical errors, as are bus errors, and most errors that generate a nonmaskable interrupt (NMI), which may subsequently generate an SMI. These errors include I/O channel check, software generated NMI, and PCI system error (SERR) and parity error (PERR) events.

## 3.4.3 CMOS Default Override

The BIOS detects the state of the CMOS default switch (configuration jumper on the I/O baseboard). If set to **CMOS Clear** prior to power on or hard reset, the BIOS changes CMOS and NVRAM settings to a default state with no exceptions, which guarantees the system's ability to boot from floppy. Password settings are unaffected by CMOS clear.

The BIOS does not clear the ESCD parameter block.

If the CMOS clear jumper is not set, ISA NVRAM still may be cleared if:

- the ISA NVRAM does not checksum to zero; or
- setting the Reset System Configuration Data field to "Yes" in Setup clears the ESCD.

## 3.4.4 BIOS Recovery Mode

In the case of a corrupt BIOS or an unsuccessful update of the system BIOS, the A450NX can boot in recovery mode. It requires that drive A: be setup to support a 3.5" 1.44 MB floppy drive. This is the mode of last resort, used only when the main system BIOS will not come up. In recovery mode operation, iFLASH (in noninteractive mode only) automatically updates only the main system BIOS. iFLASH senses that the system is in recovery mode and automatically attempts to update the system BIOS.

Before powering up the system, move the BIOS recovery jumper to the recovery state. Moving the recovery jumper causes the recovery BIOS (also known as boot block) to be executed instead of the normal BIOS. The recovery BIOS is a self-contained image that exists solely as a fail-safe mechanism to flash in a new BIOS image. Obtain a bootable DOS-compatible diskette that contains a copy of the BIOS release. Boot the system from the A: drive using this diskette, which executes a special AUTOEXEC.BAT file from the BIOS release. The batch file invokes iFLASH, which updates the flash ROM with the BIOS found on the diskette.

**NOTE:** During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes between two and four minutes. A successful update ends with two high-pitched beeps. A failure is indicated by a long series of short beeps.

If a failure occurs, it is most likely that one or more of the system BIOS iFLASH files is corrupt or missing. After a successful update, power down the system and move the recovery jumpers to the default position. Power up the

system and verify that the BIOS version number matches the version of the entire BIOS that you originally attempted to update.

CMOS is not cleared when the system BIOS is updated.  Remember that any additional or different languages that were present before updating will need to be reloaded to flash.

# 3.5   Boot Features

The A450NX BIOS identifies all initial program load (IPL) devices in the system and attempts to boot from them in the order specified in Setup.  IPL devices include the BIOS Aware IPL Device (BAID) as well as PnP cards containing an option ROM.  The A450NX BIOS supports the *BIOS Boot Specification 1.01* (BBS).

## 3.5.1   Boot Device Selection and Ordering

By adhering to the *BIOS Boot Specification, 1.01.* the A450NX BIOS gives the user the ability to order the list of boot devices, via the boot menu in the flash-resident Setup utility.  All boot devices are detected and listed.  The user can choose the order of the devices from which the machine attempts to boot.  This list is maintained until the user changes it again in Setup or, overrides it during POST by pressing the <ESC> key and selecting a new boot device from the list of available devices.

By pressing <ESC> during POST, users have the option of overriding the boot sequence specified in Setup by selecting a different primary boot device.  This override is valid only for that specific boot.  Subsequent boots will revert back to the order specified in Setup.  If the chosen device fails to load the operating system, the BIOS reverts to the previous boot sequence.  The <ESC> hot key is valid while the "Press <F2> key to enter Setup" message is displayed at the bottom of the screen.  At the end of POST, if the <ESC> key was pressed, a popup boot menu is displayed to allow the user to change the boot device choice, or to enter Setup and permanently change the boot order.

The system boots in the order chosen by the user, with the exception of legacy devices.  Legacy devices are those devices that tend to take control of the boot process altogether by hooking the boot vector (interrupt 19h).  Further, they provide no means for identifying themselves as an IPL device.  Therefore, the BIOS cannot selectively boot from one of several legacy IPL devices in a system.  The current implementation of the BBS specification supports up to eight devices.  If greater than eight devices are present in the system configuration, the user should disable the multiboot option in Setup.  If a BBS compliant adapter controls a number of drives that cause the eight-device limit to be exceeded, the multiboot option must be disabled.

## 3.5.2   PnP Option ROM Support

Bootable PnP cards containing an option ROM are supported.  There are two varieties of PnP cards.  One variety is the boot connection vector (BCV) devices such as SCSI hard drives.  The other variety is the bootstrap entry vector (BEV) devices such as a PnP ISA Ethernet controller.  BCVs generally install themselves into the INT 13h services by hooking INT 13h, while BEVs do not.  The BIOS supports both BCVs and BEVs.

# 3.6   Console Redirection

The BIOS supports redirection of both video and keyboard via a serial link (COM1 or COM2).  When console redirection is enabled, local (host server) keyboard input and video output is passed both to the local keyboard and video connections, and to the remote console via the serial link.  Keyboard inputs from both sources are considered valid and video is displayed to both outputs.  Optionally, the system can be operated without a host keyboard or monitor attached to the system and run entirely via the remote console.  Only text-based programs such as flash-resident Setup can be accessed via console redirection.

## 3.6.1   Operation

When redirecting through a modem (as opposed to a null modem cable), the modem needs to be configured with:

- auto-answer (e.g., ATS0=2 to answer after 2 rings)
- modem reaction to DTR set to return to command state (e.g., AT&D1)

Failure to provide the second configuration above causes the modem either to drop the link when the server reboots (as in AT&D0), or make the modem unresponsive to server baud rate changes (as in AT&D2).

The Setup option for handshaking must be set to CTS/RTS + CD.  CD refers to carrier detect.  In selecting this form of handshaking, the server is prevented from sending video updates to a modem that is not connected to a remote modem.  If this is not selected, video update data being sent to the modem will inhibit many modems from answering an incoming call.

When console redirection is selected via Setup, redirection is loaded into memory and activated during POST. While redirection cannot be removed without rebooting, it can be inhibited and restarted.  When inhibited, the serial port is released by redirection and may be used by another application.  Restarting will reclaim the serial port and continue redirection.  Inhibiting/restarting is accomplished through the following INT 16h mechanism.  The standard INT 16h (keyboard handler) function ah=05h places a keystroke in the key buffer, just as if an actual key had been pressed.  Keystrokes so buffered are examined by redirection, and if a valid command string has been sent, it is executed.  The following commands are supported in this fashion:

- Esc-CDZ0    - Inhibit Console Redirection.
- Esc-CDZ1    - Restart Console Redirection.

In order to inhibit redirection, the software must call INT 16h, function ah=05h five times to place the five keys in the key buffer.  Keystrokes sent to the INT 16h buffers for purposes of invoking a command <u>are</u> buffered, and should be removed via the normal INT 16h calls to prevent these keystrokes from being passed on to another application.

## 3.6.2   Keystroke Mappings

During console redirection, the **remote** terminal (which may be a dumb terminal or a system with a modem running a communication program) sends keystrokes to the **local** server.  The **local** server passes video back over this same link.

For keys that have an ASCII mapping, such as A and Ctrl-A, the remote simply sends the ASCII character.  For keys that do not have an ASCII mapping, such as F1 and Alt-A, the remote must send a string of characters as defined in Table 3-2.  The strings are based on the ANSI terminal standard.  Since the ANSI terminal standard does not define all the keys on the standard 101 key U.S. keyboard, mappings for these keys (e.g., F5 - F12, Page Up, and Page Down) were created.

**Alt** key combinations are created by sending the combination **^[}** followed by the character to be alt modified.  Once this alt key combination is sent (^[}), the next keystroke sent will be translated into its alt key mapping (i.e., if ^[} is mapped to Shift-F1, then pressing Shift-F1 followed by 'a' would send an Alt-a to the server).

The remote terminal can force a refresh of its video by sending  **^[{**.

Presently, unusual combinations outside of the ANSI mapping and not in Table 3-2 are not supported (e.g., Ctrl-F1).

*Table 3-2.     Non-ASCII Key Mappings*

| Key | Normal | Shift | Ctrl | Alt |
|-----|--------|-------|------|-----|
| ESC | ^[ | NS | NS | NS |
| F1 | ^[OP | NS | NS | NS |
| F2 | ^[OQ | NS | NS | NS |

| Key | Normal | Shift | Ctrl | Alt |
|-----|--------|-------|------|-----|
| F3 | ^[OR | NS | NS | NS |
| F4 | ^[OS | NS | NS | NS |
| F5 | ^[OT | NS | NS | NS |
| F6 | ^[OU | NS | NS | NS |
| F7 | ^[OV | NS | NS | NS |
| F8 | ^[OW | NS | NS | NS |
| F9 | ^[OX | NS | NS | NS |
| F10 | ^[OY | NS | NS | NS |
| F11 | ^[OZ | NS | NS | NS |
| F12 | ^[O1 | NS | NS | NS |
| Print Screen | NS | NS | NS | NS |
| Scroll Lock | NS | NS | NS | NS |
| Pause | NS | NS | NS | NS |
| Insert | ^[[L | NS | NS | NS |
| Delete | (7Fh) | NS | NS | NS |
| Home | ^[[H | NS | NS | NS |
| End | ^[[K | NS | NS | NS |
| Pg Up | ^[[M | NS | NS | NS |
| Pg Down | ^[[2J | NS | NS | NS |
| Up Arrow | ^[[A | NS | NS | NS |
| Down Arrow | ^[[B | NS | NS | NS |
| Right Arrow | ^[[C | NS | NS | NS |
| Left Arrow | ^[[D | NS | NS | NS |
| Tab | (09h) | NS | NS | NS |

NS = Not supported, (xxh) = ASCII character xx

*Table 3-3.      ASCII Key Mappings*

| Key | Normal | Shift | Ctrl | Alt |
|-----|--------|-------|------|-----|
| backspace | (08h) | (08h) | (7Fh) | ^[}(08h) |
| (accent) ' | ' | (tilda) ~ | NS | ^[}' |
| 1 | 1 | ! | NS | ^[}1 |
| 2 | 2 | @ | NS | ^[}2 |
| 3 | 3 | # | NS | ^[}3 |
| 4 | 4 | $ | NS | ^[}4 |
| 5 | 5 | % | NS | ^[}5 |
| 6 | 6 | ^ | NS | ^[}6 |
| 7 | 7 | & | NS | ^[}7 |
| 8 | 8 | * | NS | ^[}8 |
| 9 | 9 | ( | NS | ^[}9 |
| 0 | 0 | ) | NS | ^[}0 |
| (dash) - | - | (under) _ | (1Fh) | ^[}- |
| = | = | + | NS | ^[}= |
| a to z | a to z | A to Z | (01h) to (1Ah) | ^[}a to ^[}z |
| [ | [ | { | (1Bh) | ^[}[ |

| Key | Normal | Shift | Ctrl | Alt |
|---|---|---|---|---|
| ] | ] | } | (1Dh) | ^[}] |
| \ | \ | \| | (1Ch) | ^[}\ |
| (semi-colon) ; | ; | (colon) : | NS | ^[}; |
| (apostrophe) ' | ' | (quote) " | NS | ^[}' |
| (comma) , | , | < | NS | ^[}, |
| (period) . | . | > | NS | ^[}. |
| / | / | ? | NS | ^[}/ |
| (space) | (20h) | (20h) | (20h) | ^[}(20h) |

NS = not supported, (xxh) = ASCII character xx

## 3.6.3    Limitations

Console redirection is a real mode BIOS extension and does not operate outside of real mode. Console redirection will not work once the operating system or a driver like EMM386 takes the processor into protected mode. If an application takes the processor in and out of protected mode, it should inhibit redirection before entering protected mode and restart it once back into real mode. Video is redirected by scanning and sending changes in text video memory. Thus, console redirection is unable to redirect video in graphics mode. Keyboard redirection functions via the BIOS INT 16h handler. Software bypassing this handler will not receive redirected keystrokes.

# 3.7    DMI Support

The main component of Desktop Management Interface (DMI) is the management information format (MIF) database. This database contains all of the information about the computing system and its components. Using DMI, a system administrator can obtain the types, capabilities, operational status, installation date, and other information about the system components.

The A450NX BIOS complies with *System Management BIOS (SMBIOS) Specification, 2.1,* and implements all mandatory function calls. The SMBIOS follows the System Device Node model used by PnP, and uses PnP BIOS functions to access SMBIOS information. PnP functions 50h-5Fh are assigned for SMBIOS interface. Each of the SMBIOS PnP functions is available in both real mode and 16-bit protected mode. General purpose nonvolatile (GPNV) storage as defined in the *System Management BIOS (SMBIOS) Specification, 2.1,* will be provided. The total size of the GPNV storage area is at least 128 bytes. The exact size depends upon availability of nonvolatile memory. A handle parameter is passed into GPNV function calls to specify which GPNV area is to be accessed.

The BIOS also constructs a table containing DMI information in shadow memory so that it is available to the drivers that require this information without performing BIOS calls.

The SMBIOS structure table is broken into two parts:

- SMBIOS entry point header structure
- SMBIOS structure table

The SMBIOS entry point header structure can be found in the 0F0000h to 0FFFFFh physical address area of memory and is paragraph (16 byte) aligned.

*Table 3-4.      SMBIOS Header Structure*

| ELEMENT | LENGTH | DESCRIPTION |
|---|---|---|
| Header | 5 Bytes | _DMI_ |
| Checksum | 1 Byte | Checksum of SMBIOS header structure |
| Length | 2 Bytes | Total length of SMBIOS structure table |

| ELEMENT | LENGTH | DESCRIPTION |
|---|---|---|
| BIOS Structure Table Address | 4 Bytes | 32-bit physical address of beginning of byte aligned DMI structure table |
| NumStructures | 1 Byte | Total number of structures within the DMI structure table |
| DmiBIOSRevision | 1 Byte | Revision of the SMBIOS extensions |

The SMBIOS structure table contains all of the SMBIOS structures fully packed together. The structures in this table can be parsed out and would be in the exact format returned by the SMBIOS extension function 51h, *GetDmiStructure*. This table is static. The BIOS will create this table before passing control to the OS, but it does not update the table while the OS is running, even if there are configuration changes. The *System Management BIOS (SMBIOS) Specification, 2.1,* describes the format of the SMBIOS structure table. Additionally, the A450NX BIOS supports GPNV areas as required by the manufacturing process.

The following are SMBIOS types supported by the A450NX BIOS.

Type 0: 1 for the system BIOS, 1 for video BIOS and 1 for SCSI BIOS
Type 1, Type 2, Type 3, Type 4, Type 5, Type 6, Type 7, Type 8, Type 9, Type 10, Type 11, Type 12,  Type 13, Type 16 and Type 17.

# 3.8   USB Support

A USB-aware OS will enable the USB functionality and can make use of USB devices. The A450NX BIOS does not provide legacy support for the USB keyboard and mouse.

USB devices can resume the system from an ACPI S1 state. USB devices cannot wakeup a system from an S4 state.

# 3.9   Configuration Utilities (CU)

The configuration utilities (CU) provide the means to configure onboard resources and add-in cards. The utilities are provided in two forms: the System Setup Utility (SSU) and the Flash-resident Setup Utility.

Configuration of onboard devices is done using the Setup Utility embedded in flash ROM. Setup provides enough configuration functionality to boot a system diskette or other media such as a CD-ROM, which are shipped with the hardware that contains the SSU. The SSU is required for configuration of PCI and ISA add-in cards. The SSU is released on diskette or CD-ROM. Setup is always provided in flash memory for basic system configurations.

SSU is PCI-aware and conforms to the *Plug and Play ISA Specification,Ver. 1.0a*. The SSU works with any compliant **.**CFG or **.**OVL files supplied by the peripheral device manufacturer. Intel supplies only the **.**OVL and **.**CFG files for the system baseboard.

The configuration utilities modify the CMOS RAM and NVRAM, under direction of the user. The actual hardware configuration is accomplished by the BIOS POST routines and the PnP Auto-configuration Manager. The configuration utilities always update a checksum for both areas, so that any potential data corruption is detectable by the BIOS before hardware configuration takes place. If the data is corrupted, the BIOS requests that the system be reconfigured before it is rebooted.

If the disk-based SSU is used, a logo is automatically displayed before the SSU is executed. The logo can be customized by an OEM.

Refer to the *AD450NX Server System Product Guide (Intel Part #678269-002)* for details on when to use the configuration utilities and the options available to the user for system configuration.

# 3.10 Flash Update Utility

iFLASH loads a fresh copy of the system software, including system BIOS, into flash ROM.  The loaded code and data include the following:

- Onboard video BIOS and SCSI BIOS
- Setup Utility
- User Binary Area

When running iFLASH in interactive mode, the user may choose to save, update, or verify a particular flash area. Saving a flash area takes a mirror image of the specified flash area and copies it to a file or series of files on hard or floppy disk.  Updating a flash area takes a file or series of files from hard or floppy disk, and loads it in the specified area of flash ROM.  Verifying a flash area compares an existing flash area against a file or series of files on hard or floppy disk.  The primary purpose of iFLASH is to reprogram the flash area.  Future versions may not support verification and save operations.  In interactive mode, iFLASH can display the header information of selected files.

**NOTES:** The flash-resident setup field in System Management Mode is located on the Server Menu.  This field must be **enabled** for iFLASH to run properly.  This field is enabled by default.

The utility iFLASH must be run without the presence of a 386 Protected Mode control program, such as Windows or EMM386.  iFLASH uses the processor's flat addressing mode to update the flash area.

Following is a typical example of how the areas of flash ROM are defined in the Flash Table (Table 3-5).  The Block Base Address field contains the base address of each block, as located at the top of the address space.

*Table 3-5.     Flash Table*

| Base Address | Length | Usage |
|---|---|---|
| 0FFF80000h | 10000h | ESCD,VPD and SCSI NVRAM |
| 0FFF90000h | 8000h | SMM Binary |
| 0FFF98000h | 4000h | User Binary |
| 0FFF9C000h | 4000h | BIOS Block |
| 0FFFA0000h | 12000h | Language Block |
| 0FFFB2000h | D000h | BIOS Block |
| 0FFFC0000h | 4000h | Console Redirection Binary |
| 0FFFC4000h | C000h | BIOS Block |
| 0FFFD0000h | 10000h | BIOS Block |
| 0FFFE0000h | C000h | Reserved Block |
| 0FFFEC000h | 4000h | Recovery Block |
| 0FFFFF000h | 10000h | BIOS Block |

# 3.11 Loading the System BIOS

A new A450NX BIOS is contained in the .BIx files.  The number of .BIx files is determined by the size of the A450NX BIOS area in flash ROM (see Table 3-5 for further information on logical area 1 - System BIOS).  As of this writing, the system BIOS area contains eight files (512KB).  The files are named as follows:

        xxxxxxxx.BIO

        xxxxxxxx.BI1

        xxxxxxxx.BI2

The first eight letters of each file name on the release diskette can be of any value, but cannot be renamed.  Each file contains a link to the next file in the sequence.  iFLASH does a link check before updating to ensure that the process

is successful.  However, the first file in the list can be renamed, but all subsequent file names must remain unchanged.

When an update of the system BIOS is complete, the system is automatically rebooted.  The user binary area is also updated during a system BIOS update.

# 3.12 User Binary Area

The A450NX includes a 16KB area in flash for implementation-specific OEM add-ons.  The user binary area can be saved and updated exactly as described above in the *Loading the System BIOS* section.  Only one file is needed.  The valid extension for user files is **.**USR.

A user binary may be a run-time binary or a POST-time-only binary.  In the A450NX BIOS, which was released when this specification was written, a run-time user binary is loaded at the physical address 000D8000h - 000DBFFFh, a size of 16KB.  The load location, however, may change in future BIOS releases.  This makes it important that user binaries be location independent.

A POST-time user binary may be loaded anywhere in the conventional (0 - 640KB) memory area and discarded at the time of OS boot.

# 3.13 System Resources

## 3.13.1  Memory Map

*Table 3-6.          System Memory Map*

| Address Range | Amount | Function |
|---|---|---|
| 00000000 – 0009FFFF | 640KB | Base (conventional) system memory |
| 000A0000 – 000AFFFF | 128KB | ISA video buffer |
| 000C0000 – 000D7FFF | 96KB | Add-in option ROMs (video, SCSI…) |
| 000C0000 – 000D7FFF | 96KB | Add-in option ROMs |
| 000D8000 – 000DBFFF | 16KB | Allocated to run-time user binary, if enabled/programmed, otherwise can be used for option ROMs |
| 000DC000 – 000DFFFF | 16KB | Allocated to console redirection, if enabled, otherwise can be used for option ROMs |
| 000E0000 – 000FFFFF | 128KB | System BIOS shadowed |
| 00100000 - PCI memory allocated to first PCI device | | Typically it can go up to 3 GB |
| FEC00000 – FEC0FFFF | 64KB | Reserved.  Unused on this platform<br>Reclaimed.  If main memory exceeds this region |
| FEC10000 – FEC1FFFF | 64KB | IOAPIC allocated to the PID<br>Reclaimed.  If main memory exceeds this region |
| FEC20000 – FECFFFFF | 896KB | Reserved<br>Reclaimed.  If main memory exceeds this region |
| FEE00000 - FEF00000 | 1 MB | LOCAL APIC<br>Reclaimed.  If main memory exceeds this region |
| FF000000 – FFDFFFFF | 14 MB | Unused<br>Reclaimed.  If main memory exceeds this region |
| FFE00000 – FFFFFFFF | 2 MB | Main system BIOS |
| 100000000 – 1FFFFFFFF | 4 GB | If memory exists |

**Note:** The term main memory in the above table refers to the added physical memory.

## 3.13.2  I/O Map

*Table 3-7.  System I/O Address Map*

| I/O Address | Resource |
|---|---|
| 0000 – 001F | DMA Controller |
| 0020 – 0021 | Interrupt Controller 1 |
| 0022 – 0040 | Unused/Reserved |
| 0040 – 005F | Programmable Timer |
| 0060 & 0064 | Keyboard Controller |
| 0061 | NMI Status & Control Register |
| 0070 | NMI Mask Bit and RTC Index Address |
| 0071 | Real-time Clock |
| 0072 | Real-time Clock extended index register |
| 0073 | Real-time Clock extended data register |
| 0080 – 008F | DMA Low Page Register |
| 0092 | Port 92 Register |
| 00A0 – 00A1 | Interrupt Controller 2 |
| 00B2 | Advanced Power Management Control |
| 00B3 | Advanced Power Management Status |
| 00C0 – 00DF | DMA Controller |
| 00F0 | Coprocessor Error |
| 0170 – 0177 | Secondary IDE Controller |
| 01F0 – 01F7 | Primary IDE Controller |
| 0278 – 027F | Parallel Port 2 (relocatable) |
| 02E8 – 02EF | Serial Port  4 (relocatable) |
| 02F8 – 02FF | Serial Port 2 (relocatable) |
| 0370 – 0377 | Secondary Floppy |
| 0378 – 037F | Parallel Port 1 (relocatable) |
| 03BC – 03BF | Parallel Port 3 |
| 03E8 – 03EF | Serial Port 2 (relocatable) |
| 03F8 – 03FF | Serial Port 1 (relocatable) |
| 0CF8 | PCI Configuration Address Register |
| 0CFC | PCI Data Address Register |
| 0CF9 | Reset Control |
| 04D0 – 04D1 | INTC Edge/Level Register |
| 0C00 – 0C7F | Power Management Base Address |
| 0CA8 – 0CAF | SMIC Decoder |
| 0CC0 – 0CCF | SM Base Address |
| 2000 – FFFF | Allocated to the PCI devices |

## 3.13.3  PCI Configuration Space Map

*Table 3-8.  PCI Configuration Space Map*

| Host Bus Number | Device Number (Hex) | Description |
|---|---|---|
| 0 | 48 | Slot 1 |
| 0 | 50 | Onboard 7880* |
| 0 | 58 | Slot 2 |
| 0 | 60 | On board video |
| 0 | 78 | PIIX4 |
| 0 | 80 | MIOC |
| 0 | 90 | PXB-0A |
| 0 | 98 | PXB-0B |
| 0 | A0 | PXB-1A |
| 1 | 20 | Slot 3 |

| Host Bus Number | Device Number (Hex) | Description |
|---|---|---|
| 1 | 28 | Slot 4 |
| 1 | 30 | Slot 5 |
| 1 | 38 | Slot 6 |
| 1 | 48 | PID |
| 2 | 20 | Slot 7 |
| 2 | 20 | Slot 8 |
| 2 | 20 | Slot 9 |
| 2 | 20 | Slot 10 |
| 2 | 20 | Slot 11 |

## 3.13.4  Interrupts Map

*Table 3-9.*      System Interrupts Map

| IRQ | Device |
|---|---|
| NMI | Parity error |
| 0 | Interval timer |
| 1 | Keyboard buffer full |
| 2 | Reserved, cascade interrupt from slave PIC |
| 3 | Onboard serial port B (COM2) or add-in board |
| 4 | Onboard serial port A (COM1) or add-in board |
| 5 | Parallel port LPT2 or add-in board |
| 6 | Onboard diskette (floppy) controller |
| 7 | Parallel port LPT1 or add-in board |
| 8 | Real-time clock (RTC) |
| 9 | Reserved/Used for ACPI |
| 10 | (add-in board) |
| 11 | (add-in board) |
| 12 | Onboard PS/2 mouse port or add-in board |
| 13 | Math coprocessor error |
| 14 | Primary IDE hard drive controller, if enabled |
| 15 | Secondary IDE hard drive controller, if enabled |

**Note:**    Add-in board can be PCI or ISA

## 3.13.5  DMA Channels

*Table 3-10.*    DMA Channel Map

| Channel | Device |
|---|---|
| 0 | (add-in board) |
| 1 | (add-in board) |
| 2 | Floppy drive |
| 3 | PCI IDE (selectable) |
| 4 | PCI IDE (selectable) |
| 5 | (add-in board) |
| 6 | (add-in board) |
| 7 | (add-in board) |

# 3.14 Error Messages and Error Codes

The system BIOS displays error messages on the video screen. Prior to video initialization, beep codes inform the user of errors. POST error codes are logged in the system event log, as well as the extended BIOS data area (EBDA).

The BIOS displays POST error codes on the video monitor.

Table 3-11 and Table 3-12 define POST Port-80h codes, POST beep codes, POST error codes, and system error messages.

## 3.14.1  POST Port-80h Codes

The BIOS indicates the current testing phase during POST after the video adapter has been successfully initialized by writing a 2-digit hex code to I/O location 80h. If a Port-80h card is installed, it displays this 2-digit code on a pair of hex display LEDs.

*Table 3-11.    Port-80h Code Definition*

| Code | Meaning |
|------|---------|
| CP | Phoenix check point (Port-80) code |

Table 3-12 contains the Port-80 codes displayed during the boot process. A beep code is a series of individual beeps on the system speaker, each of equal length. Table 3-12 describes the error conditions associated with each beep code and the corresponding POST checkpoint code as seen by a Port 80h card (e.g., if an error occurs at checkpoint 20h, a beep code of 1-3-1-1 is generated).

*Table 3-12.    Standard BIOS Port-80 Codes*

| CP | Beeps | Reason |
|----|-------|--------|
| 02 | | Verify real mode |
| 04 | | Get processor type |
| 06 | | Initialize system hardware |
| 08 | | Initialize chip set registers with initial POST values |
| 09 | | Set in POST flag |
| 0A | | Initialize processor registers |
| 0B | | Enable processor cache |
| 0C | | Initialize caches to initial POST values |
| 0E | | Initialize I/O |
| 0F | | Initialize the local bus IDE |
| 10 | | Initialize power management |
| 11 | | Load alternate registers with initial POST values |
| 12 | | Restore processor control word during warm boot |
| 14 | | Initialize keyboard controller |
| 16 | 1-2-2-3 | BIOS ROM checksum |
| 18 | | 8254 timer initialization |
| 1A | | 8237 DMA controller initialization |
| 1C | | Reset programmable interrupt controller |
| 20 | 1-3-1-1 | Test DRAM refresh |

| CP | Beeps | Reason |
|----|-------|--------|
| 22 | 1-3-1-3 | Test 8742 keyboard controller |
| 24 | | Set ES segment register to 4 GB |
| 28 | 1-3-3-1 | Autosize DRAM. Beep code indicates not enough RAM available |
| 2A | | Clear 512KB base RAM |
| 2C | | Reserved |
| 2E | 1-3-4-3 | Base RAM failure, not enough memory to continue POST |
| 30 | | Reserved |
| 32 | | Test processor bus-clock frequency |
| 34 | | Test CMOS |
| 35 | | RAMInitialize alternate chip set registers |
| 36 | | Warm start shutdown |
| 37 | | Reinitialize the chip set (MB only) |
| 38 | | Shadow system BIOS ROM |
| 39 | | Reinitialize the cache (MB only) |
| 3A | | Autosize cache |
| 3C | | Configure advanced chip set registers |
| 3D | | Load alternate registers with CMOS values |
| 40 | | Set initial processor speed new |
| 42 | | Initialize interrupt vectors |
| 44 | | Initialize BIOS interrupts |
| 46 | 2-1-2-3 | Check ROM copyright notice |
| 47 | | Initialize manager for PCI Option ROMs |
| 48 | | Check video configuration against CMOS |
| 49 | | Initialize PCI bus and devices |
| 4A | | Initialize all video adapters in system |
| 4B | | Display QuietBoot screen |
| 4C | | Shadow video BIOS ROM |
| 4E | | Display copyright notice |
| 50 | | Display processor type and speed |
| 52 | | Test keyboard |
| 54 | | Set key click, if enabled |
| 56 | | Enable keyboard |
| 58 | 2-2-3-1 | Test for unexpected interrupts |
| 5A | | Display prompt **Press F2 to enter SETUP** |
| 5C | | Test RAM between 512KB and 640KB |
| 60 | | Test extended memory |
| 62 | | Test extended memory address lines |
| 64 | | Jump to UserPatch1 |
| 66 | | Configure advanced cache registers |
| 68 | | Enable external and processor caches |
| 6A | | Display external cache size |
| 6C | | Display shadow message |
| 6E | | Display nondisposable segments |
| 70 | | Display error messages |
| 72 | | Check for configuration errors |

| CP | Beeps | Reason |
|----|-------|--------|
| 74 | | Test real-time clock |
| 76 | | Check for keyboard errors |
| 7A | | Test for key lock on |
| 7C | | Set up hardware interrupt vectors |
| 7E | | Test coprocessor, if present |
| 80 | | Detect and install external RS232 ports |
| 82 | | Detect and install external parallel ports |
| 85 | | Initialize PC-compatible PnP ISA devices |
| 86 | | Reinitialize onboard I/O ports |
| 88 | | Initialize BIOS data area |
| 8A | | Initialize extended BIOS data area |
| 8C | | Initialize floppy controller |
| 90 | | Initialize hard-disk controller |
| 91 | | Initialize local-bus hard-disk controller |
| 92 | | Jump to UserPatch2 |
| 93 | | Build MPTABLE for multiprocessor system |
| 94 | | Disable A20 address line |
| 95 | | Install CD ROM for boot |
| 96 | | Clear huge ES segment register |
| 98 | 1-2 | Search for option ROMs.  One long, two short beeps on checksum failure |
| 9A | | Shadow option ROMs |
| 9C | | Set up power management |
| 9E | | Enable hardware interrupts |
| A0 | | Set time of day |
| A2 | | Check key lock |
| A4 | | Initialize typematic rate |
| A8 | | Erase F2 prompt |
| AA | | Scan for F2 key stroke |
| AC | | Enter SETUP |
| AE | | Clear in-POST flag |
| B0 | | Check for errors |
| B2 | | POST done – prepare to boot operating system |
| B4 | 1 | One short beep before boot |
| B5 | | Display Multiboot menu |
| B6 | | Check password (optional) |
| B8 | | Clear global descriptor table |
| BC | | Clear parity checkers |
| BE | | Clear screen (optional) |
| BF | | Check virus and backup reminders |
| C0 | | Try to boot with INT 19 |
| DO | | Interrupt handler error |
| D2 | | Unknown interrupt error |
| D4 | | Pending interrupt error |
| D6 | | Initialize option ROM error |
| D8 | | Shutdown error |

| CP | Beeps | Reason |
|----|-------|--------|
| DA |  | Extended block move |
| DC |  | Shutdown 10 error |
| FB |  | FRB in progress |
| FC |  | 5 sec wait for BMC to initialize |
| FD |  | FRB 2 watchdog timer failed, reset will occur in 5 seconds |

# 3.14.2  POST Error Codes and Messages

Table 3-13 defines POST error codes and associated messages.  These codes may change in the future as the Phoenix* BIOS matures and includes the support for POST error code display.

*Table 3-13.    POST Error Messages and Codes*

| Code | Error Message |
|------|---------------|
| 0002 | Primary Boot Device Not Found |
| 0010 | Cache Memory Failure, Do Not Enable Cache |
| 0015 | Primary Output Device Not Found |
| 0016 | Primary Input Device Not Found |
| 0042 | ISA Config contains invalid info |
| 0050 | PnP Memory Conflict: |
| 0051 | PnP 32-bit Memory Conflict: |
| 0052 | PnP IRQ Conflict: |
| 0053 | PnP DMA Conflict: |
| 0054 | PnP Error Log Is Full |
| 0055 | Bad PnP Serial ID Checksum: |
| 0056 | Bad PnP Resource Data Checksum: |
| 0060 | Keyboard Is Locked ...  Please Unlock It |
| 0070 | CMOS Time & Date Not Set |
| 0080 | Option ROM has bad checksum |
| 0083 | Shadow Of PCI ROM Failed |
| 0085 | Shadow Of ISA ROM Failed |
| 0131 | Floppy Drive A: |
| 0132 | Floppy Drive B: |
| 0135 | Floppy Disk Controller Failure |
| 0140 | Shadow Of System BIOS Failed |
| 0170 | Disabled CPU slot # |
| 0171 | CPU Failure – CPU #  1 |
| 0172 | CPU Failure – CPU #  2 |
| 0173 | CPU Failure – CPU #  3 |
| 0174 | CPU Failure – CPU #  4 |
| 0175 | CPU modules are incompatible or one is not present. |
| 0176 | Previous CPU Failure – CPU #  1 |
| 0177 | Previous CPU Failure – CPU #  2 |
| 0178 | Previous CPU Failure – CPU #  3 |
| 0179 | Previous CPU Failure – CPU #  4 |
| 0180 | Attempting to boot with failed CPU |
| 0181 | BSP switched, system may be in uniprocessor mode |
| 0191 | CMOS Battery Failed |

| Code | Error Message |
|------|---------------|
| 0195 | CMOS System Options Not Set |
| 0198 | CMOS Checksum Invalid |
| 0200 | Failure Fixed Disk |
| 0210 | Stuck Key |
| 0211 | Keyboard error |
| 0212 | Keyboard Controller Failed |
| 0213 | Keyboard locked - Unlock key switch |
| 0220 | Monitor type does not match CMOS - Run SETUP |
| 0230 | System RAM Failed at offset |
| 0231 | Shadow RAM Failed at offset |
| 0232 | Extended RAM Failed at address line |
| 0232 | Extended RAM Failed at offset |
| 0250 | System battery is dead - Replace and run SETUP |
| 0251 | System CMOS checksum bad - Default configuration used |
| 0260 | System timer error |
| 0270 | Real time clock error |
| 0271 | Check date and time settings |
| 0280 | Previous boot incomplete - Default configuration used |
| 0289 | System Memory Size Mismatch |
| 0295 | Address Line Short Detected |
| 0297 | Base Or Extended Memory Error: Board #, DIMM # |
| 0299 | ECC Error Correction Failure |
| 02B0 | Diskette drive A error |
| 02B1 | Diskette drive B error |
| 02B2 | Incorrect Drive A type - run SETUP |
| 02B3 | Incorrect Drive B type - run SETUP |
| 02D0 | System cache error - Cache disabled |
| 02F0 | CPU ID |
| 02F5 | DMA Test Failed |
| 02F6 | Software NMI Failed |
| 02F7 | Fail-safe Timer NMI Failed |
| 0370 | Keyboard Controller Error |
| 0373 | Keyboard Stuck Key Detected |
| 0375 | Keyboard and Mouse Swapped |
| 0430 | Timer Channel 2 Failure |
| 0440 | Gate-A20 Failure |
| 0441 | Unexpected Interrupt in Protected Mode |
| 0445 | Master Interrupt Controller Error |
| 0446 | Slave Interrupt Controller Error |
| 0450 | Master DMA Controller Error |
| 0451 | Slave DMA Controller Error |
| 0452 | DMA Controller Error |
| 0460 | Fail-safe Timer NMI Failure |
| 0461 | Software Port NMI Failure |
| 0465 | Bus Timeout NMI in Slot |
| 0467 | Expansion Board NMI in Slot |
| 0510 | PCI Parity Error |
| 0611 | IDE configuration changed |
| 0612 | IDE configuration error - device disabled |

| Code | Error Message |
|------|---------------|
| 0613 | Com A configuration changed |
| 0614 | Com A configuration error - device disabled |
| 0615 | Com B configuration changed |
| 0616 | Com B configuration error - device disabled |
| 0617 | Floppy configuration changed |
| 0618 | Floppy configuration error - device disabled |
| 0619 | Parallel port configuration changed |
| 061A | Parallel port configuration error - device disabled |
| 0710 | System Board Device Resource Conflict |
| 0711 | Static Device Resource Conflict |
| 0780 | PCI Segment 1 memory request exceeds 998 MB |
| 0781 | PCI Segment 1 I/O requests exceeds 12KB |
| 0782 | PCI I/O request exceeds amount available |
| 0783 | PCI memory request exceeds amount available |
| 0784 | Illegal bus for memory request below 1 MB |
| 0785 | Memory request below 1 MB exceeds 1 MB |
| 0800 | PCI I/O Port Conflict |
| 0801 | PCI Memory Conflict |
| 0802 | PCI IRQ Conflict |
| 0804 | PCI ROM not found, May Be OK For This Card: |
| 0805 | Insufficient Memory to Shadow PCI ROM: |
| 0806 | Memory Allocation Failure for Second PCI Segment |
| 0810 | Floppy Disk Controller Resource Conflict |
| 0811 | Primary IDE Controller Resource Conflict |
| 0812 | Secondary IDE Controller Resource Conflict |
| 0815 | Parallel Port Resource Conflict |
| 0816 | Serial Port 1 Resource Conflict |
| 0817 | Serial Port 2 Resource Conflict |
| 0820 | Expansion Board Disabled in Slot |
| 0900 | NVRAM Checksum Error, NVRAM Cleared |
| 0903 | NVRAM Data Invalid, NVRAM Cleared |
| 0982 | I/O Expansion Board NMI in Slot |
| 0984 | Expansion Board Disabled in Slot |
| 0985 | Fail-safe Timer NMI |
| 0986 | System Reset caused by Watchdog Timer |
| 0987 | Bus Timeout NMI in Slot |
| 8100 | Processor 0 failed BIST |
| 8101 | Processor 1 failed BIST |
| 8102 | Processor 2 failed BIST |
| 8103 | Processor 3 failed BIST |
| 8104 | Processor 0 Internal error (IERR) |
| 8105 | Processor 1 Internal error (IERR) |
| 8106 | Processor 0 Thermal Trip error |
| 8107 | Processor 1 Thermal Trip error |
| 8108 | Watchdog timer failed on last boot |
| 810B | Processor 0 failed initialization |
| 810C | Processor 0 disabled |
| 810D | Processor 1 disabled |
| 810E | Processor 0 failed FRB-3 timer |

| Code | Error Message |
|------|---------------|
| 810F | Processor 1 failed FRB-3 timer |
| 8110 | Server Management Interface failed to function |
| 8128 | Processor 2 Internal error (IERR) |
| 8129 | Processor 3 Internal error (IERR) |
| 8130 | Processor 2 Thermal Trip error |
| 8131 | Processor 3 Thermal Trip error |
| 8138 | Processor 2 failed FRB-3 timer |
| 8139 | Processor 3 failed FRB-3 timer |
| 8140 | Processor 2 disabled |
| 8141 | Processor 3 disabled |
| 8148 | Processor 1 failed initialization |
| 8149 | Processor 2 failed initialization |
| 814A | Processor 3 failed initialization |
| 814B | BMC in Update Mode |
| 8150 | NVRAM Cleared by Jumper |
| 8152 | ESCD Data Cleared |
| 8153 | Password Cleared by Jumper |
| 8160 | Unable to apply BIOS update for Processor 1 |
| 8161 | Unable to apply BIOS update for Processor 2 |
| 8162 | Unable to apply BIOS update for Processor 3 |
| 8163 | Unable to apply BIOS update for Processor 4 |
| 8168 | Processor 1 L2 cache failed |
| 8169 | Processor 2 L2 cache failed |
| 816A | Processor 3 L2 cache failed |
| 816B | Processor 4 L2 cache failed |
| 8170 | BIOS does not support current stepping for Processor 1 |
| 8171 | BIOS does not support current stepping for Processor 2 |
| 8172 | BIOS does not support current stepping for Processor 3 |
| 8173 | BIOS does not support current stepping for Processor 4 |
| 8180 | PXB1 failed to respond |
| 8181 | Mismatch Among Processors Detected |
| 8182 | L2 cache size mismatch |
| 8200 | Baseboard Management Controller failed to function |
| 8201 | Front Panel Controller failed to function |
| 8203 | Primary Hot-swap Controller failed to function |
| 8204 | Secondary Hot-swap Controller failed to function |

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# 4. Server Management Implementation

This chapter provides the server management architecture of the A450NX board set. The server management features are listed below.

## Features

- Voltage monitoring

- Temperature monitoring

- Processor voltage ID (VID) monitoring and processor presence detection

- DIMM ID monitoring and presence detection

- Chassis fan failure detection

- System power control

- Watchdog timer

- Baseboard management controller (BMC) private management bus interface

- System management software (SMS) and system management mode (SMM) Intelligent Platform Management Bus (IPMB) message receiver

- Event message receiver

- System event log (SEL) management and access

- Sensor data record (SDR) repository management and access

- Processor nonmaskable interrupt (NMI) monitoring

- Front panel NMI monitoring and NMI generation

- Processor system management interface (SMI) monitoring

- Timestamp clock

- Power-on self test (POST) code log

- Secure mode support

- Fault resilient booting (FRB) support

# 4.1 Server Management Overview

The A450NX server management architecture revolves around a microcontroller and a parallel I/O-mapped interface for control of server management functions. Both components are located on the A450NX I/O baseboard. The onboard microcontroller provides a centralized interface for other microcontrollers, which an OEM may choose to integrate into their own custom chassis boards (e.g., front panel, hard disk backplane, power distribution backplane).

Figure 4-1 shows the A450NX board set integrated into the Intel® AD450NX Server System chassis, and is an example of the server management possibilities available to the designer.
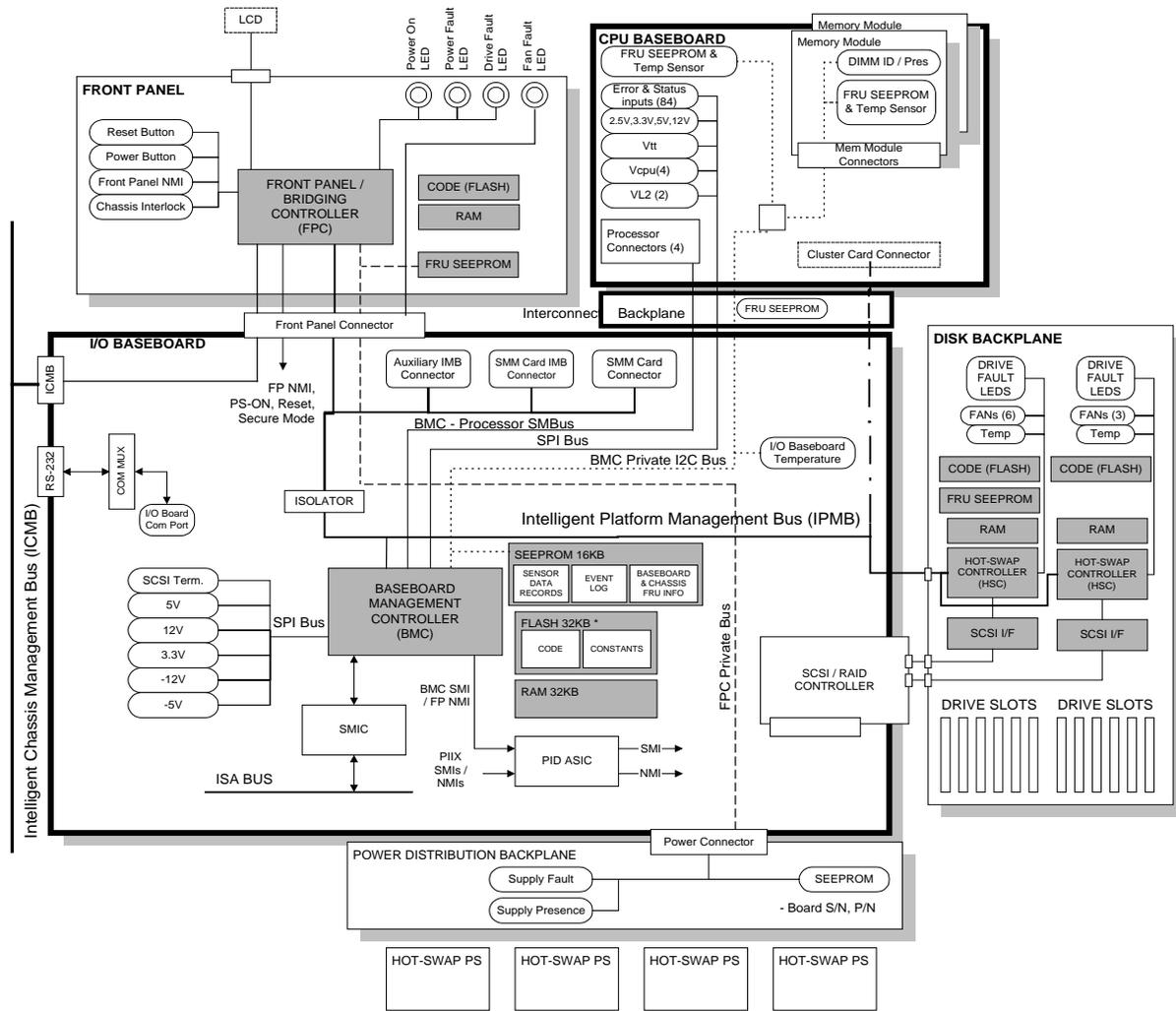
*Figure 4-1.     A450NX Server Management Architecture Diagram*

# 4.2   Platform Management Hardware

The A450NX board set server management features are implemented using a BMC and an ISA/BMC interface device called the System Management Interface Chip (SMIC).

Other key server management hardware components are:

- Buses, such as the IPMB, the microcontroller private $I^2C$ buses, and the ISA bus

- Nonintelligent devices, such as serial EEPROMs (SEEPROMs)

- Nonvolatile storage to hold the FRU inventory and default configurations, the sensor data record (SDR), and the system event log (SEL)

- Connectors between the various boards and components

# 4.2.1    Baseboard Management Controller (BMC)

The heart of A450NX server management is the baseboard management controller (BMC). The BMC is located on the A450NX I/O baseboard. This controller provides primary server management monitoring capabilities. Associated with the BMC is a nonvolatile storage that holds the SEL, the SDR repository, the operational code, and the configuration defaults for the BMC itself.

The BMC supports the Intelligent Platform Management Interface (IPMI) and the $I^2C$ interface. The BMC uses IPMI protocol to communicate with other intelligent management controllers on the chassis boards via the IPMB. The BMC also uses the $I^2C$ interface to communicate with nonintelligent devices on its private management bus. The BMC can be accessed from the ISA bus via the SMIC.

## 4.2.1.1    BMC Features

The BMC provides various server management functions, some of which are discussed in the following sections.

### 4.2.1.1.1    Voltage Monitoring

The BMC scans voltages using the serial parallel interface (SPI) bus connected to the analog-to-digital (A/D) converter. The SPI bus is local to the I/O baseboard and CPU baseboard. It is isolated from the IPMB by the BMC.

Each time a channel is scanned, the BMC compares the current reading to assigned thresholds stored in the SDR, sets the appropriate status and, if a threshold has been crossed and BIOS has been enabled, generates an event message in the system event log. The BMC scans each voltage sensor once every 5 seconds in a sequential, revolving fashion, with the polling rate dependent on the number of voltage sensors.

Both the upper critical threshold and the lower critical threshold may be set.

The thresholds and event message configuration are programmable via the ISA/BMC interface. The voltage readings, thresholds, sensor configuration, and failure status can be read via the same interface.

### 4.2.1.1.2    Baseboard Voltage Monitoring

The A/D converter, manufactured by National Semiconductor as part number ADC0819, is located on the I/O baseboard (see Figure 4-1). This device monitors all voltages on the I/O baseboard and provides the data to the BMC. The following I/O baseboard voltages are monitored:

- I/O baseboard +5 V
- I/O baseboard +12 V
- I/O baseboard +3.3 V
- I/O baseboard -12 V
- I/O baseboard -5 V
- Vcc standby
- Wide SCSI bus termination (3 channels)

Table 4-1 shows the default voltage threshold values.

*Table 4-1.    Voltage Thresholds*

| Voltage | Upper Critical | Lower Critical |
|---|---|---|
| 3.3 V | 3.645 V | 3.077 V |
| 12 V | 13.098 V | 10.738 V |
| 5 V | 5.527 V | 4.390 V |
| 5 V Standby | 5.527 V | 4.390 V |

| Voltage | Upper Critical | Lower Critical |
|---|---|---|
| -12 V | -10.720 V | -13.420 V |
| -5 V | -4.240 V | -5.860 V |
| SCSI Termination | 3.136 V | 2.508 V |

### 4.2.1.1.3    Processor Voltage Monitoring

The BMC is responsible for monitoring the voltage for each Pentium® II Xeon™ slot-2 processor supply and for the termination voltage and support logic supplies.  The following voltages are monitored: 1.5 V, 2.5 V, 3.3 V, 5 V, 12 V, CPU core voltages and processor cache voltages.  The BMC interfaces to an external multichannel A/D converter.  Four of the A/D channels are used for these voltage scanning functions.  The BMC maintains internal thresholds against which the A/D readings are compared.  The BMC generates an event message on the IPMB when the thresholds are crossed.  The following processor voltages are monitored:

- Processor 1 core voltage
- Processor 2 core voltage
- Processor 3 core voltage
- Processor 4 core voltage
- CPU +2.5 V
- CPU +1.5V (front-side bus termination voltage)
- CPU +3.3 V
- CPU +5 V
- CPU +12 V
- Processor 1&2 cache voltage
- Processor 3&4 cache voltage

Table 4-2 shows the default processor voltage threshold values.

*Table 4-2.     Processor Voltage Thresholds*

| Voltage | Upper Critical | Lower Critical |
|---|---|---|
| Core Voltage | 2.175 V | 1.666 V |
| CPU 2.5 V | 2.744 V | 2.254 V |
| CPU 3.3 V | 3.645 V | 3.077 V |
| CPU 5 V | 5.527 V | 4.390 V |
| CPU 12 V | 13.932 V | 10.062 V |
| Processor Cache | 3.724 V | 1.666 V |
| Processor Bus Termination | 1.724 V | 1.274 V |

### 4.2.1.1.4    Temperature Monitoring

The BMC polls eight temperature sensor devices, which are accessed as nonintelligent devices on the BMC private I²C bus.  One sensor is located on the I/O baseboard, one is on the CPU baseboard, four are in the processor cartridges, and two are on the memory modules (see Figure 4-1).  The current temperature readings, thresholds, sensor configuration, and failure status can be read via the ISA or Intelligent Platform Management Bus interfaces to the BMC.

The BMC monitors the temperature sensors via its private management bus.  This bus is isolated from the IPMB by the BMC.  The BMC obtains the reading from the sensor, compares the readings to a set of thresholds and, if enabled in BIOS, generates an event message in the system event log when a threshold is crossed.

The BMC scans the temperature sensors in a sequential, revolving fashion.  Two thresholds are supported for the temperature sensor: the upper critical threshold and the lower critical threshold.  Critical indicates a situation that demands immediate attention to prevent or reduce damage.

Table 4-3 displays the temperature sensor devices, the device types, and the manner by which they are accessed by the BMC.  Table 4-4 displays the default temperature thresholds.

*Table 4-3.        Temperature Sensors Monitored by the BMC*

| Temperature Sensor | Device | Access |
|---|---|---|
| I/O Baseboard Temperature | DS1621* | BMC Private I$^2$C Bus |
| CPU Baseboard Temperature | DS1624 | BMC Private I$^2$C Bus |
| Processor 1 Temperature | DS1617 | Processor SMBus |
| Processor 2 Temperature | DS1617 | Processor SMBus |
| Processor 3 Temperature | DS1617 | Processor SMBus |
| Processor 4 Temperature | DS1617 | Processor SMBus |
| Memory Module 1 Temp. | DS1624 | BMC Private I$^2$C Bus |
| Memory Module 2 Temp. | DS1624 | BMC Private I$^2$C Bus |

*Table 4-4.        Default Temperature Thresholds*

| Threshold | Upper Critical | Lower Critical |
|---|---|---|
| I/O Baseboard (PXB) | 45 °C/113 °F | -10 °C/14 °F |
| CPU Baseboard | 50 °C/122 °F | -10 °C/14 °F |
| Processor | 70 °C/158 °F | 0 °C/32 °F |
| Memory Module 1 | 50 °C/122 °F | -10 °C/14 °F |
| Memory Module 2 [†] | 45 °C/113 °F | -10 °C/14 °F |

[†] Different air flow in vicinity of this module allows different critical value.

### 4.2.1.1.5    Processor Voltage ID (VID) Monitoring and Processor Presence Detection

The voltage ID (VID) signals from the processors are used to configure the onboard processor voltage regulator circuits on the CPU baseboard using an IPMI command via the BMC.  The BMC sensors read the processor status to determine presence and voltage (VID).  The VID information read from the processor overrides any thresholds that were provided in the SDR.  However, the override of the SDR values is only in effect while the system is powered on; it does not alter the default values of the SDR.

## 4.2.1.2    DIMM ID Monitoring and Presence Detection

The BMC supplies the interface to the identification (ID) information provided by the DIMMs .  The DIMMs contribute the main DRAM memory for the system.  This information includes the size, speed, and type of DIMM installed.  The information also indicates presence, (whether a DIMM is physically inserted into the socket).

The BMC provides commands for reading the DIMM ID information.  These commands are executable from ISA and from the IPMB.  The memory modules make this information available to the BMC via the BMC private bus.

## 4.2.1.3    Fault Resilient Booting (FRB) Support

The BMC works in conjunction with the BIOS to implement Fault Resilient Booting (FRB).  The BMC specifically implements FRB-2 and FRB-3.  The FRB feature allows a multiprocessor system to detect certain types of boot-strap processor failures.  If a failure is detected, it asserts a signal to disable the errant processor/processor socket, resets the system and then restarts the system with one of the remaining processors serving as the boot-strap processor

(BSP). The BMC does not disable the processor if it is the last remaining processor in the system, nor does it allow all processors to be disabled simultaneously.

### 4.2.1.3.1    FRB-3

FRB-3 refers to the level of FRB at which a watchdog timer is started on power-up or which hard resets in a multiprocessor (MP) system. The watchdog timer must be stopped by BIOS, which requires the BSP to actually run BIOS code. If the timer is not stopped, the BSP is disabled, the system is reset, and another processor becomes the BSP. Thus, FRB-3 provides verification on power-up of a functional BSP (which was assigned the BSP role by the hardware) that can actually run code. If so configured in BIOS, the BMC also generates an internal event message for the FRB-3 failure event.

FRB requires multiple processors. The BMC uses the VID bits to verify that there are at least two processors installed in the system. If only one processor is present, the FRB-3 timer is not started.

BSP assignment is deterministic (i.e., when multiple processors are present, the BSP selection occurs in a known sequence).

If an FRB-3 timeout occurs during the boot sequence, the current BSP is disabled and the system is reset. This process repeats until the system boots without an FRB-3 timeout or until all processors except the last one are disabled. The BMC will not disable the last remaining processor.

### 4.2.1.3.2    FRB-2

FRB-2 is a level of FRB at which the BIOS uses the BMC watchdog timer to back up its operation during POST. The BIOS sets a bit in the BMC indicating that the BIOS is in the FRB-2 phase of operation.

The BIOS sets this bit after it has determined which processor is the BSP, and has saved this information. At this time, BIOS can set the FRB-2 bit, load the BMC watchdog timer with the new timeout interval, and disable FRB-3. This sequence ensures that there is no gap in watchdog timer coverage between FRB-3 and FRB-2. If the timer expires while the FRB-2 function is selected in the timer use flags, the BMC generates an FRB-2 timeout event message. The BMC then hard resets the system. The BIOS is responsible for disabling FRB-2 timeout prior to exiting POST.

### 4.2.1.3.3    FRB-1

FRB-1 is implemented mostly by the BIOS. The BIOS detects the failure of the BSP by examining the processor's built-in self test (BIST) results. If a BIST failure is indicated, the BIOS takes its own steps to record the event so that it can be logged later. The BIOS then disables the processor by allowing the FRB-3 timeout to occur.

## 4.2.2    SEEPROM Information

The BMC SEEPROM is used for holding the following information:

- **System Event Log (SEL).** This is a 7.75KB area of the SEEPROM that is used to hold the SEL.
- **Sensor Data Record (SDR) Repository.** This is an 8KB area of SEEPROM that is used to hold the sensor data records.
- **FRU Inventory Information.** The BMC implements a logical FRU inventory device. The SEEPROM device provides a 256 byte area of nonvolatile storage for this information.
- **BMC Configuration Defaults.** A portion of the FRU inventory area, referred to as the *internal use area* is used for holding configuration defaults for the BMC itself.

## 4.2.3　System Management Interface Chip (SMIC)

The SMIC application-specific integrated circuit (ASIC) provides a parallel I/O-mapped interface between the ISA bus and the BMC.  This interface is used for communication between the BMC and system management software (SMS) running under the operating system (OS).

## 4.2.4　System Event Log (SEL)

The SEL is a repository for the system's critical event information.  The SEL is maintained in the I/O baseboard's SEEPROM by the BMC.  Commands for accessing the SEL can be delivered to the BMC via the ISA SMIC interface or via the IPMB.  This makes system event information accessible *in-band* by the BIOS routines and SMS such as LANDesk® Server Manager, and *out-of-band* via the SMM card or other intelligent management device connected to the IPMB.

## 4.2.5　Sensor Data Record (SDR) Repository

The BMC maintains a special region of the I/O baseboard's SEEPROM for the SDRs.  This area is used for storing sensor data records for all the sensor devices located on the A450NX board set, as well for sensor devices located on any additional system/chassis boards.

Sensor data records contain information that identifies which device holds a sensor, the number of that sensor and its type, the kinds of events it can generate, and the initial threshold values of the sensor.  Sensor data records also hold information offsets and constants for converting the raw sensor readings to standard units (e.g., mA, volts, rpm, etc.). The system management software uses this information to get the sensor locations and conversion factors that it uses when polling the sensors.

The FRU & SDR Load utility can be used to read the SDR repository.

## 4.2.6　System Management Buses

The A450NX board set implements the following buses for use in system management:

## 4.2.6.1　Intelligent Platform Management Bus (IPMB)

The IPMB is a multimaster, open-drain, serial bus that is routed between the major system boards.  The bus is both electrical and timing compatible with the $I^2C$ bus specification, and it supports both intelligent management controllers and nonintelligent devices (e.g., SEEPROM).  Intelligent management controllers communicate with each other via the IPMB.  An example of this is the AD450NX server system, in which the BMC communicates with management microcontrollers on the front panel and the SCSI hot-swap backplane via the IPMB).

The BMC communicates with other management controllers, over the IPMB, using IPMI commands.  The IPMB can also support devices that do not adhere to the IPMI protocol; including nonintelligent devices such as $I^2C$ serial EEPROMs.

### 4.2.6.1.1　IPMB Electrical Isolation

The IPMB electrical isolation circuitry on the I/O baseboard allows the FPC, the SMM Card Feature Connector, the SMM card IPMB connector and the auxiliary IPMB connector to be accessed when the rest of the system is powered down. These isolated, always alive parts are powered by 5V Standby Power. This isolation ensures that the FPC can be accessed when 5V powered IPMB devices on other segments of the IPMB 'ground out' the bus when power is removed.

This functionality is labeled as "isolator" on the I/O baseboard in Figure 4-1.

## 4.2.6.2    BMC Private Management Bus

A number of the devices that the BMC monitors, or to which it provides access, are connected to the BMC private management bus.  The BMC private management bus is a single-master $I^2C$ bus that is solely driven by the BMC. The BMC is considered to be the owner of the devices on its private management bus.

The BMC private management bus is local to the CPU baseboard and the I/O baseboard.  The private management bus is isolated from the IPMB by the BMC.  This provides several benefits, including faster polling accesses (since there is no IPMB arbitration) and a reduction of IPMB traffic and address space.

Table 4-5 displays the devices that are managed by the BMC and the boards on which those devices are located.

*Table 4-5.   BMC Managed Devices*

| Name | Device | Board |
| --- | --- | --- |
| FRU/SEL Serial EEPROM | AT24C128* | I/O Baseboard |
| Temp Sensor PXB | DS1621* | I/O Baseboard |
| Serial EEPROM | AT24C02* | I/O Riser Card |
| Serial EEPROM | AT24C02 | Interconnect Backplane |
| I/O Port A | PCF8574* | Memory Module 1 |
| I/O Port B | PCF8574 | Memory Module 1 |
| Serial EEPROM/Temp Sensor | DS1624* | Memory Module 1 |
| IO Port A | PCF8574 | Memory Module 2 |
| IO Port B | PCF8574 | Memory Module 2 |
| Serial EEPROM/Temp Sensor | DS1624 | Memory Module 2 |
| Serial EEPROM/Temp Sensor | DS1624 | CPU Baseboard |
| Temp Sensor | DS1617* | Processor 1 |
| Serial EEPROM | AT24C02[†] | Processor 1 |
| Temp Sensor | DS1617 | Processor 2 |
| Serial EEPROM | AT24C02[†] | Processor 2 |
| Temp Sensor | DS1617 | Processor 3 |
| Serial EEPROM | AT24C02[†] | Processor 3 |
| Temp Sensor | DS1617 | Processor 4 |
| Serial EEPROM | AT24C02[†] | Processor 4 |

[†] There are two AT24C02 devices on this component, the processor FRU and the OEM FRU.

## 4.2.6.3    Serial Peripheral Interface (SPI) Bus

The serial peripheral interface (SPI) bus provides information about the processor slots, the processors installed in those slots and the A/D converters on the CPU baseboard.  The SPI bus is accessed through the BMC.  Capabilities of the SPI bus include:

- Error and status inputs – including processor ID bits and control outputs
- 16-channel A/D converter for monitoring CPU baseboard voltages

The SPI bus is composed of four separate scan chains to minimize the length of each chain, thus keeping the access latency short.  The first chain provides access to the error and status information (e.g., processor internal errors and DIMM memory errors from the MIOC).  The second chain provides access to the A/D converters (e.g., processor core voltage and the 2.5 V, 3.3 V and 5 V supplies).  The third SPI chain provides error and status information such as VID for processors 1 and 2 and their L2 cache VID.  The fourth SPI chain provides error and status information for processors 3 and 4.

### 4.2.6.4    Processor SMBus

The SMBus provides BMC access to temperature sensors on the processor cartridge.  The bus also provides access to two FRU information areas that are available from each individual processor.  The first FRU area is read only and provides data such as part number, core and L2 stepping, core frequency, and voltages for the processor and L2.  The second FRU area is available for OEM use.  Once OEM information is written to this FRU, it can be write-protected so that the data cannot be easily overwritten.

### 4.2.6.5    Intelligent Chassis Management Bus (ICMB)

The Intelligent Chassis Management Bus (ICMB), along with the ICMB bridge, provides a mechanism for interchassis management communications.  Multiple systems and peripheral chassis can be connected to the same ICMB.  Through the ICMB, intelligent devices local to a server (e.g., the BMC) can access the local server management functions of external servers, allowing server management across multiple servers.

#### 4.2.6.5.1    IPMB-ICMB Bridging

A chassis front panel controller (FPC) acts as a bridge between the IPMB and the ICMB.  The bridging controller provides a messaging connection between the IPMB and the ICMB.  It also responds to ICMB discovery messages, and other bridge request messages, such as providing ICMB protocol version information.

**Note:**    The A450NX board set does not contain the IPMB-ICMB bridge.  This functionality must be added on an OEM designed front panel board.  However, the front panel board for the Intel® AD450NX server system does include the IPMB-ICMB bridge.

## 4.2.7    FRU Inventory Information

Every board in the A450NX board set holds a nonvolatile storage device that contains FRU inventory information. All FRU inventory devices on the A450NX board set reside on the BMC private management bus and can be accessed only via the BMC.  The exception is the cluster slot on the 5-slot CPU baseboard.  The FRU information for the front-side bus (FSB) terminator card plugged into the cluster slot is available only via the IPMB and can be accessed by the BMC or any other IPMI-compliant microcontroller on the chassis.

The FRU inventory information includes board serial number, part number, and revision information.  It can also contain asset tag, product name, chassis, and OEM specific information.  The information is provided to aid in system servicing, inventory, and asset tracking.  The $I^2C$ address, the content, and the format of FRU information about individual boards are described in Chapter 2 of this document.  The following boards contain FRU information.

- I/O baseboard
- CPU baseboard
- Interconnect backplane
- Memory module
- Memory terminator module
- FSB terminator module
- I/O riser card

### 4.2.7.1    FRU & SDR Load Utility

The FRU & SDR Load Utility allows FRU information for each individual board in the A450NX board set to be loaded, read, and displayed.

# 4.2.8   Platform Management Connectors

The A450NX board set provides several connectors for the interconnections of the server management signals across the board set.  Connections are also provided to extend the IPMB to additional boards in the chassis like the front panel board, SCSI hot-swap backplane and the power distribution backplane.

The connections provided by the A450NX board set to allow OEM designed components to integrate into the server management architecture are as follows:

## 4.2.8.1   Front Panel Connector

The front panel connector on the I/O baseboard provides system control and management interconnections, including IPMB, ICMB, EMP, and other system management signals.  The front panel connector signals are described in Chapter 2 of this document.

## 4.2.8.2   SMM Card Feature Connector

The feature connector is provided for use by the Intel® Server Monitor Module (SMM) card, also known as the emergency management card.  The signals provided by this connector allow the SMM card to take full control of the system.  The feature connector, when attached to an SMM card, provides the following functionality:

- Monitors additional voltages and sends out voltage alerts
- Monitors additional temperatures and sends out temperature alerts
- Allows the administrator to power-up/down the server from a remote location
- Provides the ability to redirect the console to a remote location

For pinout information for this connector, see Chapter 2 of this document.

## 4.2.8.3   IPMB Connectors

There are two IPMB connectors on the I/O baseboard.

- SMM card IPMB connector
- Auxiliary IPMB connector

The SMM card IPMB connector and the auxiliary connector are located on the portion of the IPMB that is powered by the +5 V standby.  Therefore, these connections allow communication with the front panel controller (FPC) while the system is powered down.  This makes it possible to control system power via IPMI commands to the FPC.

### 4.2.8.3.1   SMM Card IPMB Connector

The SMM card IPMB connector is a 3-pin CD-ROM-audio-style, shrouded header.  This connector provides IPMB access for future SMM cards, which may not rely on the SMM card feature connector.  The SMM card IPMB connector is located near the SMM card feature connector.

### 4.2.8.3.2   Auxiliary IPMB Connector

The auxiliary IPMB connector is also a 3-pin CD-ROM-audio-style shrouded header located on the I/O baseboard.  The connector is provided for SMM-type cards, which might be used by an OEM or a system integrator.  For auxiliary IPMB connector specifications, see Chapter 2 of this document.

## 4.2.8.4   Interconnect Backplane SM Connector

The server management connector, located on the interconnect backplane, provides support for an IPMB connection to other chassis related boards, such as the power distribution and SCSI hot-swap backplanes.  The server management connector of the AD450NX server system also carries the FPC's private $I^2C$ signals to the power distribution backplane.

# 5. Board Set Specifications

This chapter describes the specifications for the entire A450NX board set.  The board set is tested to the environmental and regulatory specifications listed in this chapter.  This is a board level specification only.  The system level specification is beyond the scope of this document.

# 5.1   Electrical Specification

Table 5-1 shows the tolerances and minimum/maximum currents for +3.3 V, +5 V, +12 V, and -12 V for the complete A450NX board set, the CPU and I/O baseboards, the memory modules, the FSB termination modules, the interconnect backplane, and the I/O riser card.  The power supply system must meet these requirements at the input to the interconnect backplane to ensure complete board set functionality.  All the values are specified at the remote sense points on the interconnect backplane.

*Off voltage* is the maximum voltage allowed on each domain during a power-off condition.  In the case of the AD450NX server system chassis, this voltage is present any time AC power is present and is an artifact of the power supplies used in that system.  The A450NX board set will draw a certain amount of current at these voltages.  The A450NX board set does not use -5 V.  5 V standby must be present at any time AC power is present.

*Table 5-1.     A450NX Board Set Voltage and Current Requirements Summary*

| Voltage Domain | Static[1] Tolerance | Dynamic[2] Tolerance | Min[3] di/dt | Min[3] Current | Max[4] Current | Max[4,5] Current Step | Test Load[6] Step di/dt | Capacitive[7] Load (Min) |
|---|---|---|---|---|---|---|---|---|
| 3.3 V | +5%/-1.5% | +5%/-3.5% | 0.1 A/µs | 8 A | 60 A | 28 A | 2.5 A/µs | 160,000 µF |
| 5.0 V | NA | +5/-3% | 0.1 A/µs | 1.8 A | 52 A | 12 A | 2.5 A/µs | 33,000 µF |
| 12 V | NA | +5%/-4% | 0.15 A/µs | 0.2 A | 35 A | 18 A | 0.15 A/µs | 3600 µF |
| +5.0 V Stby | NA | +5%/-3% | 0.1 A/µs | 10 mA | 155 mA | 145 mA | 0.1 A/µs | 4000 pf |
| -12.0 V | NA | ± 10% | 0.1 A/µs | 0 A | 1.2 A | 1 A | 0.1 A/µs | 0.2 µF |
| Ripple/Noise | 80 mV of noise in the range of 1kHz to 1 MHz is allowed on the 3.3 V plane.  This voltage is measured at the F16 connector, and is required in addition to set-point accuracy and line/load regulation (see note 1). | | | | | | | |
| Max Allowable Off Voltage (V$_{off-max}$) | 5% of nominal value for +3.3 V, +5.0 V, +12.0 V, -12.0 V. | | | | | | | |

**Notes:** 1.   Tolerance includes set-point accuracy and line/load regulation.  This value is based on a recovery time of 500 microseconds to return to static tolerance requirements after the specified maximum dynamic load occurs.  Since the dynamic tolerance cannot be widened beyond the static tolerance requirements, only the dynamic requirements are specified for the +5 V and +12 V lines.

2.   Tolerance includes set point accuracy, line/load regulation, and transient loading.

3.   Minimum system configuration is as follows: 1 idle processor, 2 VRMs, 4 FSB termination modules (3 in the case of a 4-slot CPU baseboard), no cluster card (5-slot CPU baseboard only), two memory cards with 128 MB of RAM, no I/O adapter cards, no front panel, no I/O riser card, no keyboard, no mouse, no video, no parallel-port connections, no bus activity.  (Each FSB termination module draws approximately 200 mA of current from +5 V.  This value can be subtracted from the minimum +5 v current for configurations using the 4-slot CPU baseboard.)

4. Maximum system configuration is as follows: 4x65 W processors and their associated VRMs operating at 80% efficiency, no cluster card (5-slot baseboard only), 1 FSB termination module (5-slot baseboard only), keyboard, mouse, video, parallel-port connected, two memory modules (8 GB of RAM total), no front panel, 120Kbaud on COM2, and all I/O adapter slots sinking maximum allowable current (41 A @ +5 V, 23 A @ +3.3 V). (Each FSB termination module draws approximately 200 mA of current from +5 V. This value can be subtracted from the maximum +5 v current for configurations using the 4-slot CPU baseboard.)

5. This assumes that total current steps from PCI adapters will be no more than 12 A for +5 V and no more than 6 A for +3.3 V.

6. This is the slew rate at which the power supply should be tested to meet the board requirements.

7. The power supply must meet the requirements with this amount of low ESR bulk capacitance on each output. The equivalent ESR must be <= 1.1 mohms for the 3.3 V capacitance and <= 4.5 mohms for the 5 V & 12.0 V capacitance. The 12.0 V values are stated for a system with all VRMs installed.

Table 5-2 describes the power-up and power-down timing requirements for the A450NX board set.

*Table 5-2.      A450NX Board Set Voltage Timing and Sequencing Requirements*

| Parameter | Description | Specification |
|---|---|---|
| Trise-max | Voltage Rise Time. This is the time it takes for all voltages (+3.3 V, +5 V, +12 V, -12 V) to be within their specified values from the time the voltages begin their rise from $V_{off-max}$ | 350 ms. Must be monotonic starting 10 ms before PWR_GOOD assertion. |
| sTrise-min | Minimum allowable rise time for all voltages. Values smaller than this may prevent some devices in the system from initializing properly. | 10 ms from the time the voltage starts rising |
| Tfall-max | Voltage Fall Time. This is the time it takes for all voltages to drop to $V_{off-max}$ from the time the power supply is turned off. | 500 ms |
| Toff | Minimum Voltage Off Time. This is the time the power supplies must be powered down before being powered back up again. | 100 ms |
| Tsequence-on | Voltage sequencing during power-on and power-off. | None. All voltages can come up or down in any order as long as they meet the above timing requirements and reach specified values within 100 ms of each other. |

**Note:** All parameters measured at the sense points of the interconnect backplane.

## 5.1.1   Power Budget

Table 5-3 shows the breakdown of current consumption for both a minimally and a fully configured A450NX system.  Power is easily calculated from the numbers provided.  This table is provided for reference only and is not meant to provide the exact current usage in a system.  Note that the interconnect backplane draws negligible current.

*Table 5-3.    A450NX Board Set Voltage and Current Requirements Detail*

| | +3.3 V | | +5 V | | +12 V | | +5 V Standby | | -12 V | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min[1] Current | Max [2] Current | Min[1] Current | Max [2] Current | Min[1] Current | Max [2] Current | Min[1] Current | Max [2] Current | Min[1] Current | Max [2] Current |
| CPU baseboard with processor/s | 4.6 A | 4.6 A | 0.8 A | 6.2 A | 0.2 A | 28.5 A | 0 A | 0 A | 0 A | 0 A |
| RAM | 1 A | 24.1 A | 0 A | 0 A | 0 A | 0 A | 0 A | 0 A | 0 A | 0 A |
| Cluster card [8] | 0 A | 0 A | 0 A | 6.8 A | 0 A | 7.0 A | 0 A | 0 A | 0 A | 0 A |
| **TOTAL (CPU)** | **5.6 A** | **29 A** | **0.8 A** | **6.2 A** | **0.2 A** | **28.5 A** | **0 A** | **0 A** | **0 A** | **0 A** |
| | | | | | | | | | | |
| I/O baseboard | 0.2 A | 5 A | 0.7 A | 4.25 A | 0 A | 0 A | 5 mA | 5 mA | 0 A | 0 A |
| PCI/ISA [3][4][5][6][7] | 0 A | 23 A | 0 A | 41 A | 0 A | 6.0 A | 0 A | 0 mA | 0 A | 1.2 A |
| I/O riser card | 0 A | 0 A | 0 A | 70 mA | 0 A | 25 mA | 5 mA | 150 mA | 0 A | 0 A |
| Front panel [8] | 0 A | 0 A | 0 A | 250 mA | 0 A | 0 A | 0 A | 170 mA | 0 A | 0 A |
| **TOTAL (I/O)** | **0.2 A** | **28 A** | **0.7 A** | **45.6 A** | **0 A** | **6.03 A** | **10 mA** | **155 mA** | **0 A** | **1.2 A** |
| | | | | | | | | | | |
| **A450NX Total Current (CPU,I/O)** | **5.8 A** | **57 A** | **1.5 A** | **51.8 A** | **0.2 A** | **34.5 A** | **10 mA** | **155 mA** | **0 A** | **1.2 A** |
| **A450NX Total Power** | **19. 1W** | **188 W** | **7.5 W** | **259.0 W** | **2.4 W** | **414.4 W** | **0.05 W** | **0.78 W** | **0 W** | **14.4 W** |

**Notes:**
    **1.** Minimum system configuration is as follows: 1 idle processor, 2 VRMs, 4 FSB termination modules (3 in the case of a 4-slot baseboard), no cluster card (5-slot baseboard only), two memory cards with 128 MB of RAM, no I/O adapter cards, no front panel, no I/O riser card, no keyboard, no mouse, no video, no parallel-port connections, no bus activity.  (Each FSB termination module draws approximately 200 mA of current from +5 V.  This value can be subtracted from the minimum +5 v current for configurations using the 4-slot CPU baseboard.)
    **2.** Maximum system configuration is as follows: 4x65 W processors and their associated VRMs operating at 80% efficiency, no cluster card (5-slot baseboard only), 1 FSB termination module (5-slot baseboard only), keyboard, mouse, video, parallel-port connected, two memory cards with 8 GB of RAM, and all I/O adapter slots filled.  (Each FSB termination module draws approximately 200 mA of current from +5 V.  This value can be subtracted from the maximum +5 v current for configurations using the 4-slot CPU baseboard).
    **3.** Current not to exceed 7.58 A (25 W) per PCI slot or 23 A total for all PCI expansion slots on +3.3 V.
    **4.** Current not to exceed 5 A (25 W) per PCI slot or 41 A total for all expansion slots on +5 V.
    **5.** Current not to exceed 2 A (10 W) per ISA slot or 41 A total for all expansion slots on +5 V.
    **6.** Current not to exceed 500 mA per PCI or ISA slot or 6 A total for all expansion slots on +12 V.
    **7.** Current not to exceed 100 mA per slot or 1.2 A total for all expansion slots on -12 V.
    **8.** These values are included for reference only and are not included in the maximum configuration requirements.

## 5.1.2   Absolute Maximum Ratings

Operation of the A450NX board set at conditions beyond those shown in Table 5-4 may cause permanent damage to the system.  Exposure to absolute maximum rating conditions for extended periods may affect the boards life expectancy and reliability.

*Table 5-4.    Absolute Maximum Ratings*

| | |
|---|---|
| Storage Temperature | -55° C to +70° C |
| Voltage of any signal with respect to ground | -0.3 V to Vdd [†] + 0.3 V |
| +3.3 V supply with respect to ground | -0.3 V to +4.3 V |
| +5 V supply with respect to ground | -0.3V to +6.5 V |
| +12 V supply with respect to ground | -0.3 V to 14 V |

[†] Vdd means supply voltage for the device

# 5.2 Mechanical Specifications

This section describes the mechanical specification of all the individual boards that are a part of the A450NX board set. It also describes the processor retention mechanism and the cluster slot heat sinks.

## 5.2.1 I/O Baseboard

Figure 5-1 and Figure 5-2show the mechanical specifications for the A450NX I/O baseboard and I/O riser card. All dimensions are given in inches. Connector dimensions are shown relative to pin 1.
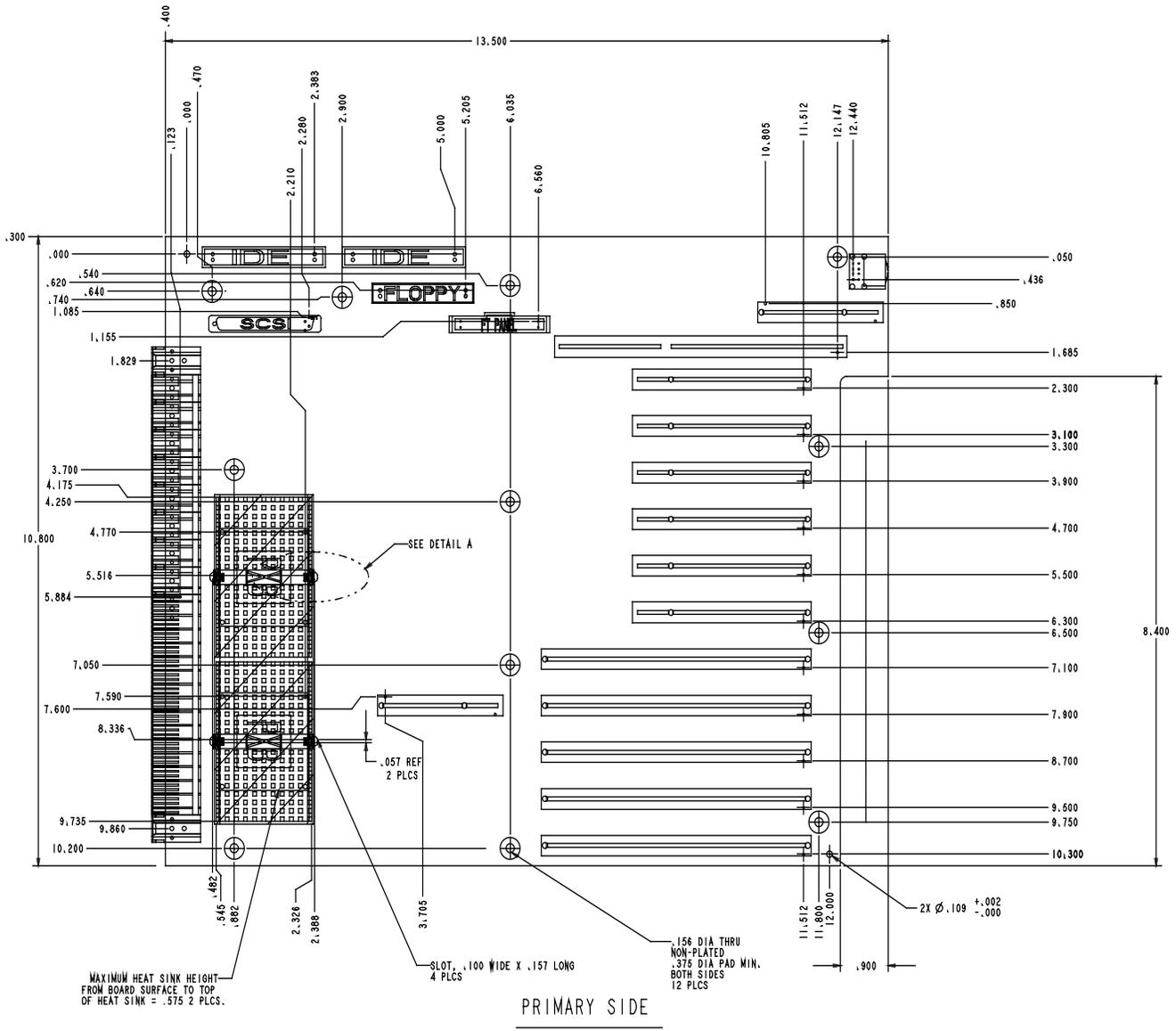


*Figure 5-1. A450NX I/O Baseboard Mechanical Diagram*

**Notes supporting the I/O baseboard mechanical drawing:**

- All dimensions, unless listed as reference, are critical and must be adhered to in order to ensure board compatibility with the chassis.
- Second side lead protrusion is 0.100" maximum.

- Connectors are dimensioned to pin 1.
- Dimensions, unless otherwise specified, are per Intel PB Fabrication 454979.
- Dimensions are per ANSI Y14.5M.
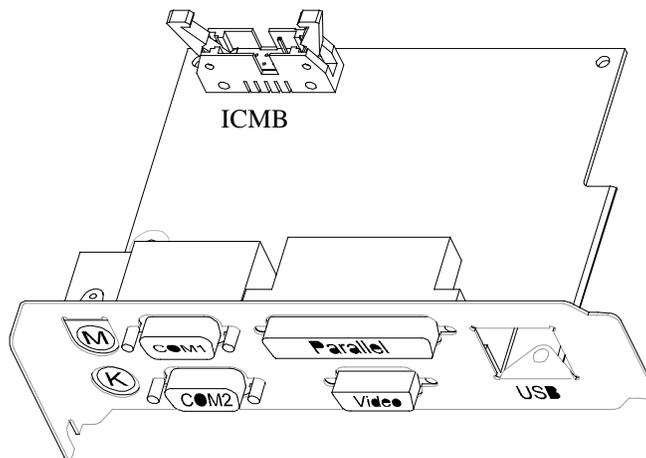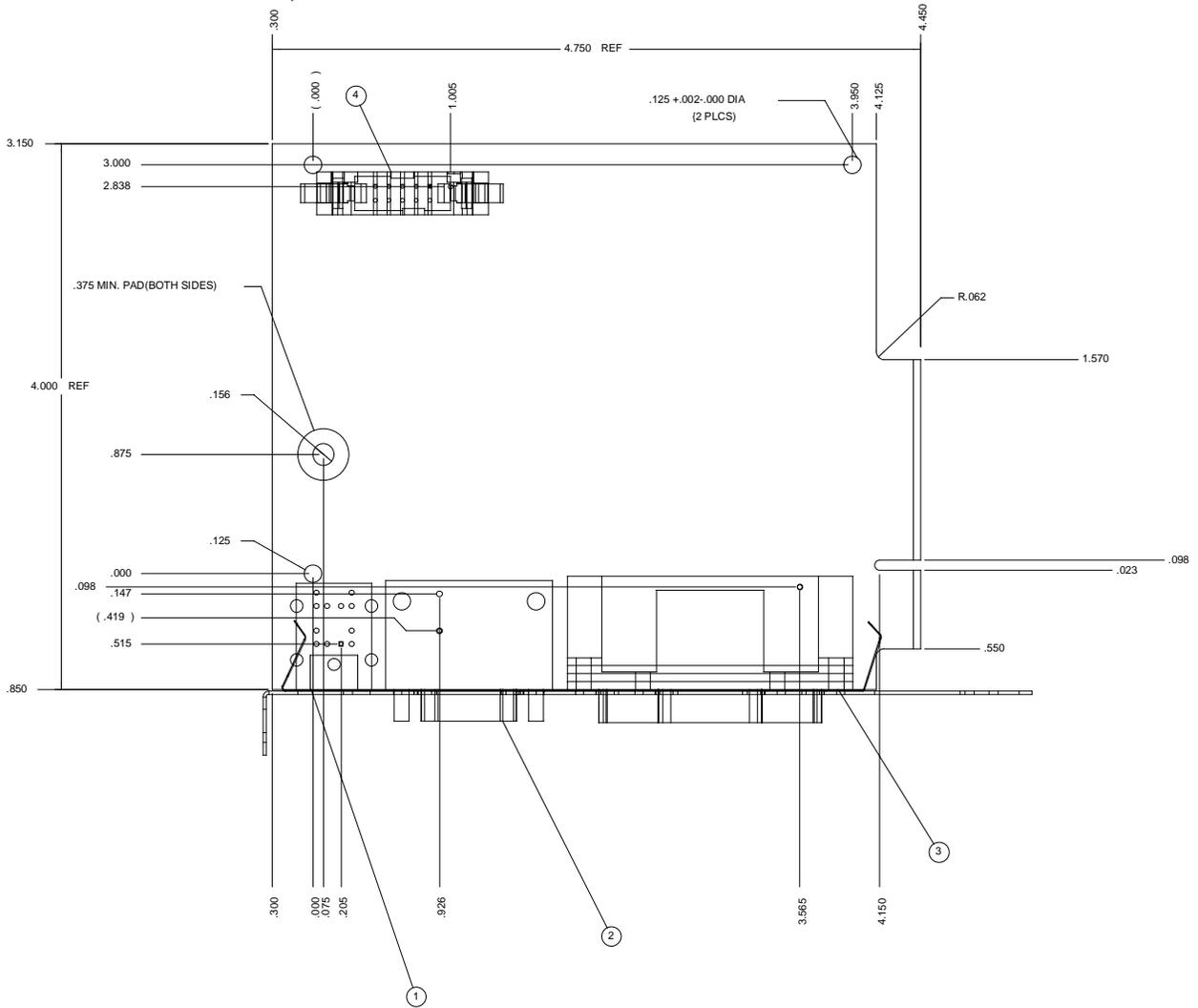


*Figure 5-2.    I/O Riser Card Mechanical Diagram*

## 5.2.2   CPU Baseboard

Figure 5-3 diagrams the mechanical specifications and the connector positions for the CPU baseboard.  All dimensions are given in inches.  Note that this diagram shows the board, which supports the cluster option; the top most slot-2 connector and two VRM sockets are removed in the noncluster version of the CPU board.



*Figure 5-3.     CPU Baseboard Mechanical Drawing*

The form factor and mounting hole locations on the 4-slot baseboard are the same as those on the 5-slot version. Figure 5-4 shows the mechanical layout of the 4-slot CPU baseboard.

*Figure 5-4.      4-slot CPU Baseboard Mechanical Drawing*

## 5.2.3    Front-side Bus Terminator Module

Figure 5-5 diagrams the mechanical specifications of the FSB terminator module.  All dimensions are given in inches.
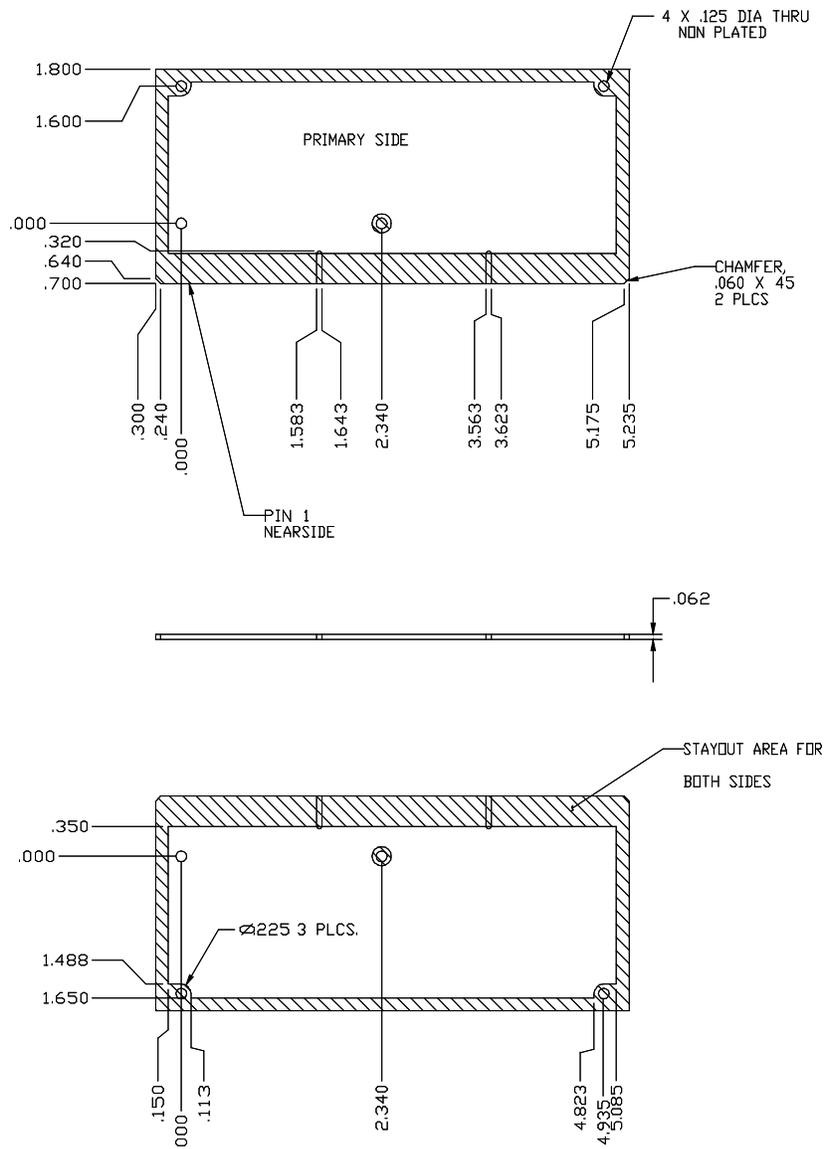


*Figure 5-5.     FSB Terminator Mechanical PB Drawing*

## 5.2.4   Memory and Memory Terminator Modules

Figure 5-6 and Figure 5-7 show the mechanical specifications of the A450NX memory and memory terminator modules.  All dimensions are given in inches.
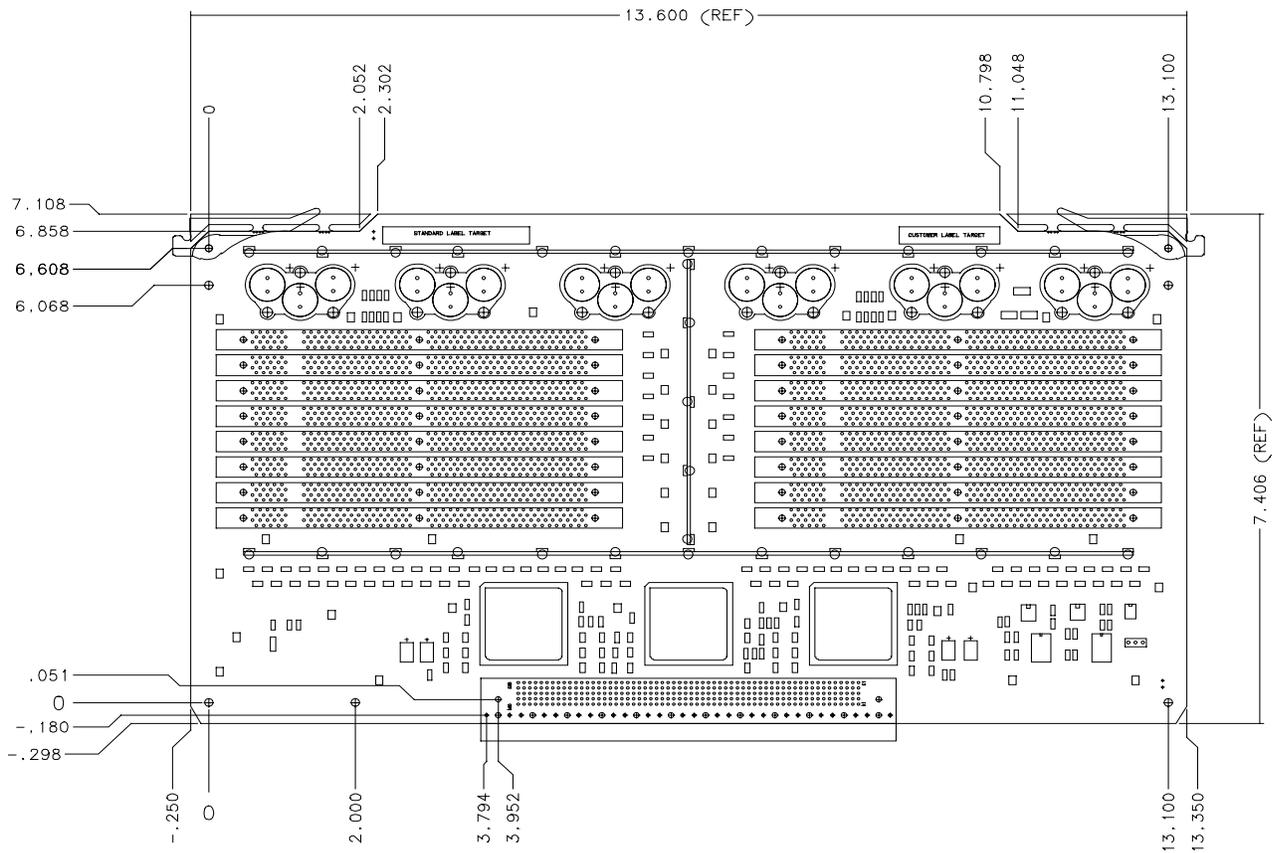


*Figure 5-6.      Memory Module Mechanical Specification*
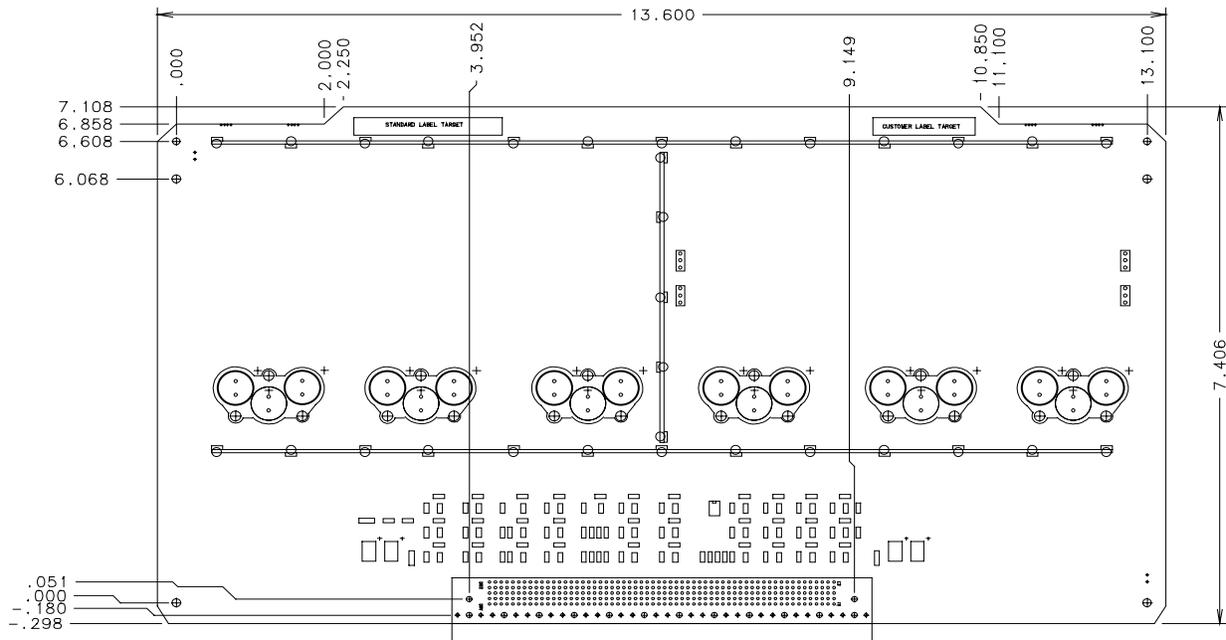
*Figure 5-7.      Memory Terminator Module Mechanical Specification*

# 5.2.5   Interconnect Backplane

Figure 5-8 diagrams the basic mechanical outlines of the A450NX interconnect backplane.  All dimensions are given in inches.  The remote-sense locations for the power supplies are on the 34-pin connector as shown in the drawings.

The I/O baseboard and CPU baseboard, when installed into the interconnect backplane, are 1.952" apart as measured from the back edge of each board.  This value should be used for chassis standoff dimensions.  Note, however, both baseboards have surface mount components on their backsides which are no taller than 0.100".  This additional height is **NOT** included in the 1.952" dimension.
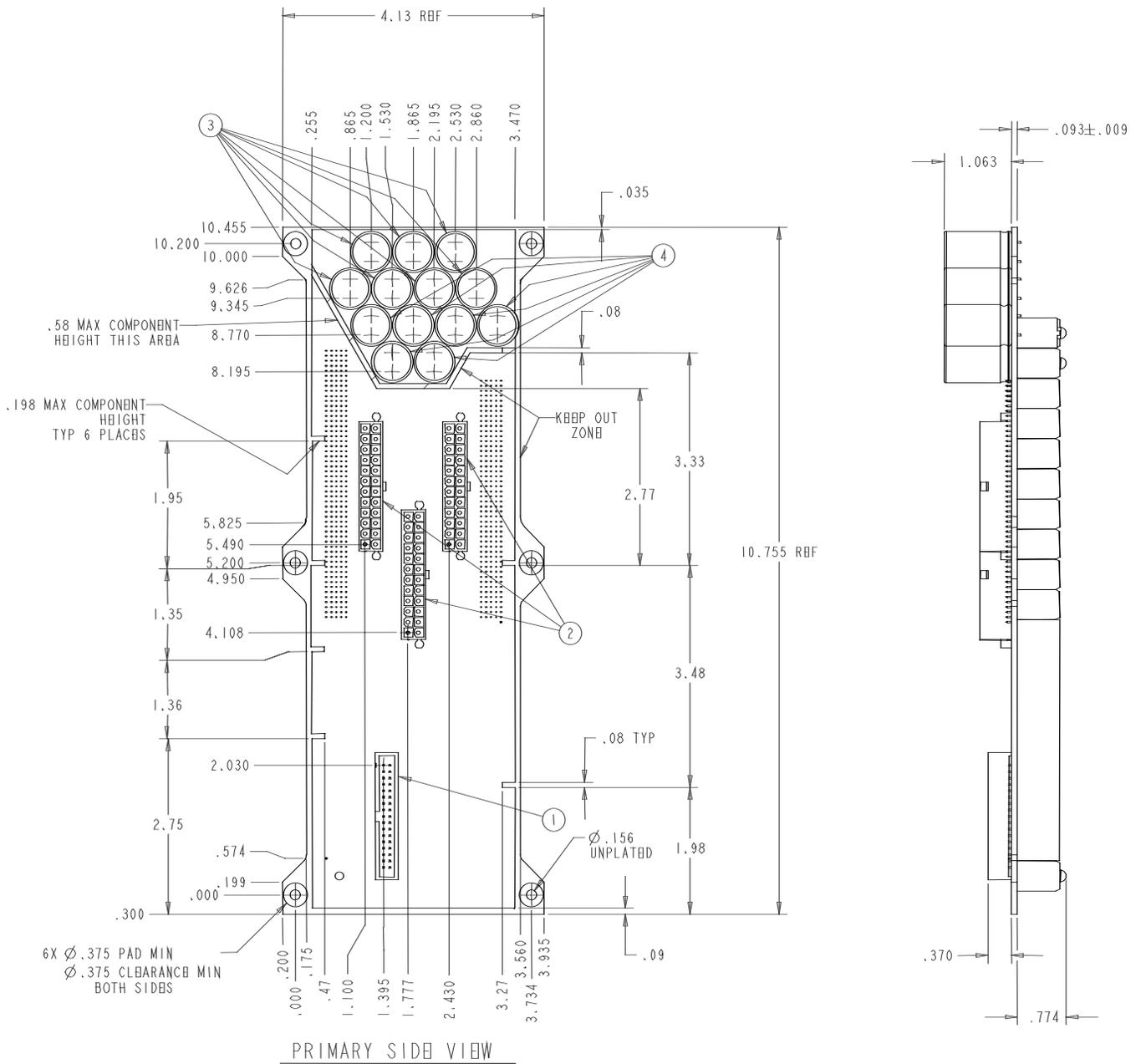


*Figure 5-8.      Primary Side Mechanical Outline*

# 5.3   Processor Retention Mechanism

Shown conceptually in Figure 5-9 are four processor modules with heat sinks on a 5-slot baseboard.  The two memory modules and VRMs are not shown.
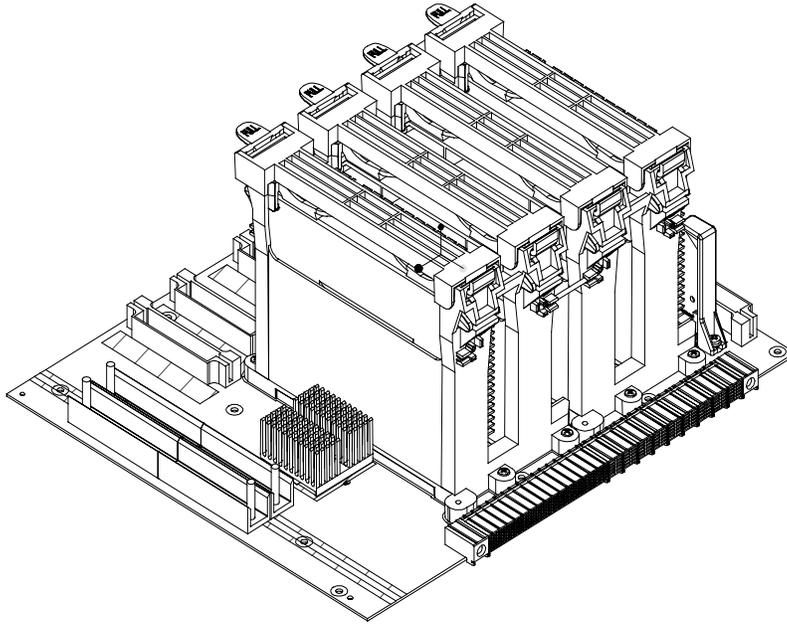


*Figure 5-9.     CPU Baseboard Processor Retention Mechanism*

The processor retention module is a rigid plastic molded support pod that encapsulates the processors on the CPU baseboard.  Up to four processors may be present in the system, with terminator assemblies inserted into unpopulated processor slots.

The support pods are modular.  Each pod is mounted through clearance holes in the baseboard directly into standoffs in the chassis center bulkhead.  Direct chassis mounting minimizes stress on the baseboard by stiffening the board and transmitting the load directly to the sheet metal chassis.  There is one support pod for every two processors.

The two individual modules are physically tied together with a side wire bracket (see Figure 5-13), one on each side, to form a rigid structural assembly.  Top covers are then mounted to each pod to further support the processor during shock and vibration.

A drawing of each component is shown in Figure 5-10, Figure 5-11, Figure 5-12, and Figure 5-13 respectively.
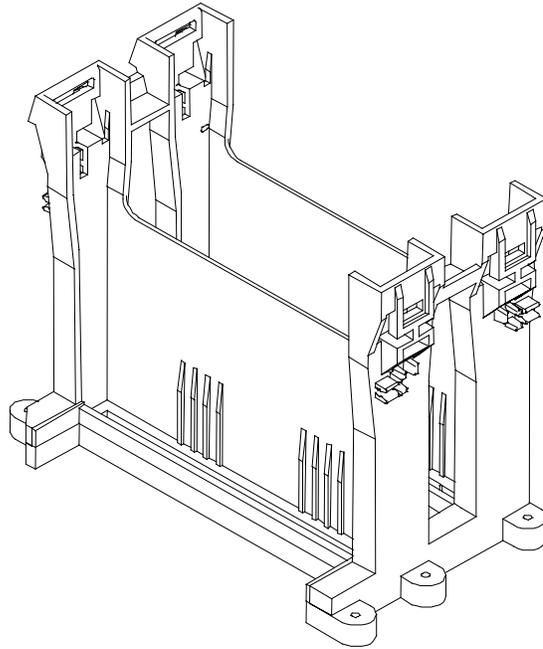
*Figure 5-10.   Processor/Terminator Base*
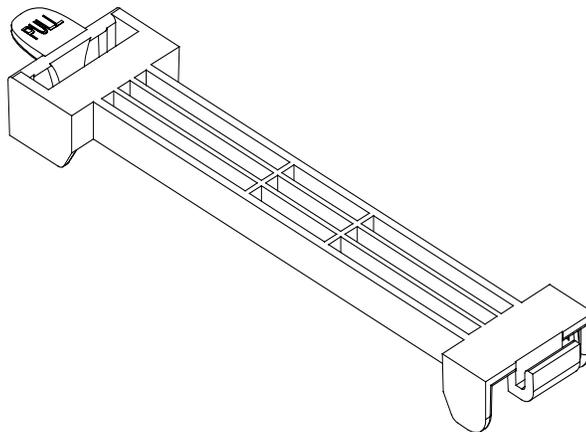


*Figure 5-11.   Processor Retention Cover*
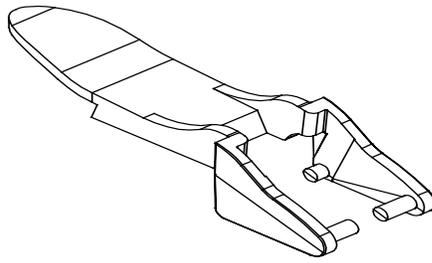
*Figure 5-12.    Insertion and Extraction Lever*
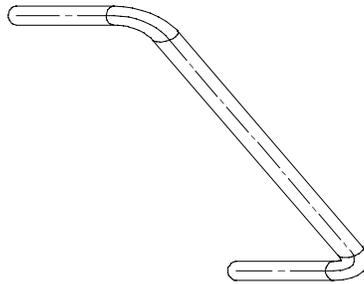


*Figure 5-13.    Base Bracket Clip*

# 5.4   Cluster Slot Retention Mechanism

Figure 5-14 diagrams the mechanical specification of the cluster slot terminator retention mechanism for use with 5-slot CPU baseboards.  Dimensions are given in inches.
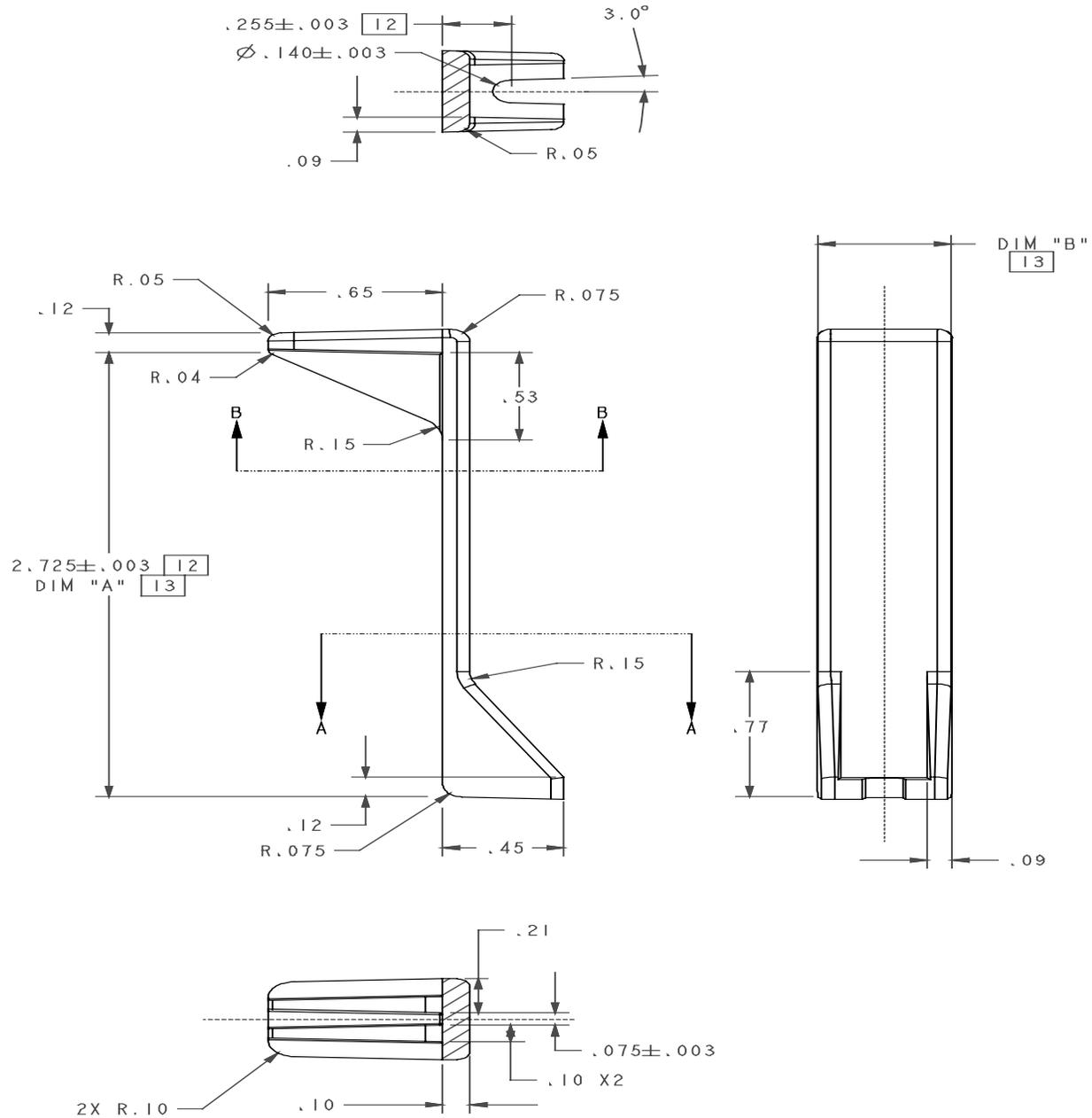


*Figure 5-14.    Cluster Slot Terminator Retention Bracket Mechanical Drawing*

# 5.5   Processor Heat Sink

The processor heat sink is 5.20″ X 4.24″ X 1.00″ and is attached to the processor heat plate with five screws.  The heat sink will be manufactured with the thermal grease already applied.
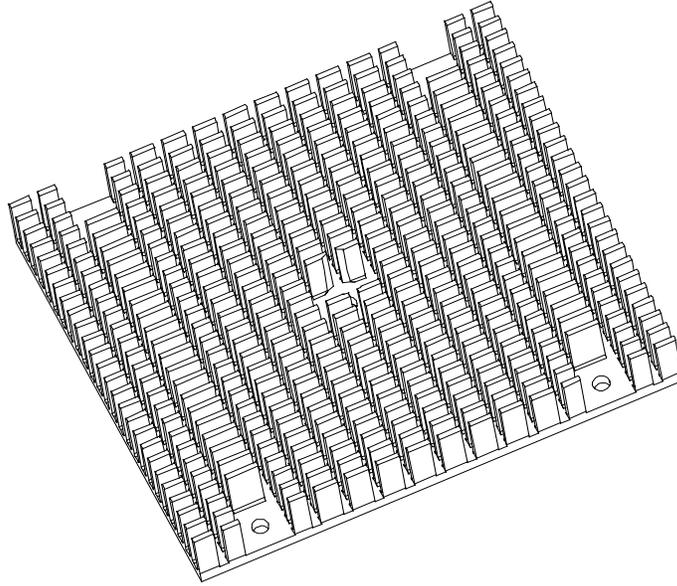


*Figure 5-15.    Processor Heat Sink*

# 5.6   MIOC Heat Sink

The MIOC component of the NX chip set will come from Intel's factory with a 1.75″x1.75″x1.0″ heat sink.  The heat sink is attached with a clip, which is retained by the CPU baseboard.
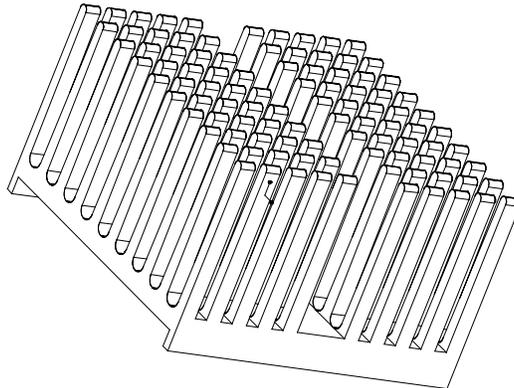


*Figure 5-16.    MIOC Heat Sink*

# 5.7 Connector Specifications

This section describes the specifications for the connectors that are used on the A450NX board set.  Each connector is described in the section that relates to the board on which it is located.

## 5.7.1 I/O Baseboard

Table 5-5 shows the reference designators, quantity, manufacturer, and part number for connectors on the I/O baseboard.  The items in Table 5-5 reference the components shown on Figure 2-2 of this document.

*Table 5-5.     A450NX I/O Baseboard Connector Definitions*

| Item | Description | Connector Type † | Intel Part | Quantity | Locations |
|---|---|---|---|---|---|
| 1 | PCI Connectors (64-bit) | AMP 145034-1* | 201082-092 | 5 | P7–P11 |
| 2 | PCI Connectors (32-bit) | AMP 646255-1* | 201082-060 | 6 | P1–P6 |
| 3 | ISA Connector | AMP 176139-2* | 108768-050 | 1 | J2A1 |
| 4 | Legacy Connections | AMP 650090-3* | 201082-080 | 1 | J1B1 |
| 5 | Front Panel Connector | AMP 104068-1* | 201794-060 | 1 | J2E1 |
| 6 | SCSI (Wide) Connector | Fox Conn/Hon Haj QA01343-P4* | 628525-069 | 1 | J1H2 |
| 7 | Floppy Disk Port Connection | AMP 111944-7* | 201418-034 | 1 | J1F2 |
| 8 | IDE Connector | AMP 111945-8* | 201418-040 | 2 | J1F1, J1H1 |
| 9 | Monoblock F16 Bus Connector | BERG 73956-9003* | 696451-501 | 1 | J5J1 |
| 10 | Monoblock Power Module | BERG 73956-9004* | 696453-501 | 1 | J2J1 |
| 11 | USB Connector | Fox Conn/Hon Haj UB1112C-D1* | 642575-001 | 1 | J1A1 |

† Representative manufacturer and part number.

Table 5-6 shows the reference designators, quantity, manufacturer, and part number for connectors on the I/O riser card.  The items in Table 5-6 reference the components shown on Figure 2-3 of this document.

*Table 5-6.     A450NX I/O Riser Card Connector Definitions*

| Item | Description | Connector Type | Intel Part | Qnty | Locations |
|---|---|---|---|---|---|
| 1 | MultifunctionMouse Connector / Keyboard Connector | Fox Conn/Hon Haj MH11063-D0 | 201377-001 | 1 | J4 |
| 2 | Multifunction Dual Serial Port Connector | Fox Conn/Hon Haj DM10156-73 | 201004-013 | 1 | J5 |
| 3 | Multifunction VGA Connector / Parallel Port Connector | AMP 750433-2 | 201325-001 | 1 | J6 |
| 4 | ICMB Cable Interface Connector | AMP 111988-1 | 661966-001 | 1 | J1 |

## 5.7.1.1   F16 Bus Connector

*Table 5-7.       F16 Connector Pinout*

| Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|
|  | A1 | GND | B1 | GND | C1 |  | D1 | PIC_CLK | E1 |
| IO_TCK | A2 |  | B2 |  | C2 | STP_CLK_L | D2 | GND | E2 |
| IO_TDO | A3 | GND | B3 | IO_TMS | C3 | IO_TRST_L | D3 | PICD(1) | E3 |
| BMC_SPI_BUS(1) | A4 | IO_TDI | B4 | PWRGDB | C4 | PICD(0) | D4 | GND | E4 |
| BMC_SPI_BUS(6) | A5 | GND | B5 | A20M_L | C5 | INIT_L | D5 | RESET_PWR_DIST_L | E5 |
| BMC_SPI_BUS(0) | A6 | CPU_SPI_RESET_L | B6 | PROC_RESET_L | C6 | GND | D6 | GND | E6 |
| I2C_BMC_SCL | A7 | GND | B7 | GND | C7 | BMC_SPI_BUS(2) | D7 | BMC_SPI_BUS(4) | E7 |
| I2C_BMC_SDA | A8 | BMC_SPI_BUS(3) | B8 | BMC_SPI_BUS(5) | C8 | GND | D8 | GND | E8 |
| NMI_5V | A9 | GND | B9 | SMI_L | C9 | X0IB_L | D9 | CIB_INT0 | E9 |
| GND | A10 | IGNNE_L | B10 | I2C_GLOBAL_SDA | C10 | IO_PWRGD | D10 | GND | E10 |
| X0D_L(0) | A11 | GND | B11 | GND | C11 | I2C_GLOBAL_SCL | D11 | INTR | E11 |
| X0D_L(1) | A12 | X0XRTS_L | B12 | X0HRTS_L | C12 | GND | D12 | GND | E12 |
| X0D_L(3) | A13 | GND | B13 | GND | C13 | RESET_HSBP_L | D13 | FERR_L | E13 |
| X0D_L(4) | A14 | X0D_L(2) | B14 | X0BE_L(0) | C14 | GND | D14 | GND | E14 |
| GND | A15 | GND | B15 | GND | C15 |  | D15 | X0BLK_L | E15 |
| X0D_L(6) | A16 | X0D_L(5) | B16 | X0PAR_L | C16 | GND | D16 | GND | E16 |
| X0D_L(8) | A17 | GND | B17 | GND | C17 |  | D17 | X0RST_L | E17 |
| X0D_L(9) | A18 | X0D_L(7) | B18 | X0ADS_L | C18 | GND | D18 | GND | E18 |
| GND | A19 | GND | B19 | X0D_L(11) | C19 |  | D19 |  | E19 |
| X0D_L(12) | A20 | X0D_L(10) | B20 | X0BE_L(1) | C20 | GND | D20 | GND | E20 |
| X0D_L(14) | A21 | GND | B21 | X0XSTBN_L | C21 | X0XSTBP_L | D21 |  | E21 |
| X0D_L(15) | A22 | X0D_L(13) | B22 | GND | C22 | GND | D22 | GND | E22 |
| GND | A23 | GND | B23 | ISP_HSBP_SDO | C23 | X0HSTBP_L | D23 | GND | E23 |
| X0CLK | A24 |  | B24 | GND | C24 | X0HSTBN_L | D24 | GND | E24 |
| GND | A25 | GND | B25 |  | C25 | ISP_MODE | D25 | ISP_EN_L | E25 |
|  | A26 | ISP_SCLK | B26 | GND | C26 |  | D26 | GND | E26 |
|  | A27 | GND | B27 |  | C27 |  | D27 | (-12V) | E27 |
| ISP_SDO | A28 |  | B28 | GND | C28 | (-12V) | D28 | GND | E28 |
| INTRUSION_L | A29 | GND | B29 |  | C29 | ISP_EN2_L | D29 | CPU_SLP_L | E29 |
| ISP_SDI | A30 |  | B30 |  | C30 | GND | D30 | GND | E30 |
| VCC_STDBY | A31 | GND | B31 | GND | C31 |  | D31 |  | E31 |

| Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|
| I2C_FPC_SCL | A32 | VCC_STDBY | B32 | | C32 | | D32 | GND | E32 |
| I2C_FPC_SDA | A33 | GND | B33 | GND | C33 | X1IB_L | D33 | PWR_GOOD | E33 |
| GND | A34 | I2C_DS2P_SDA | B34 | I2C_DS2P_SCL | C34 | PS_PWR_ON | D34 | GND | E34 |
| X1D_L(0) | A35 | GND | B35 | GND | C35 | | D35 | | E35 |
| X1D_L(1) | A36 | X1RTS_L | B36 | X1HRTS_L | C36 | GND | D36 | GND | E36 |
| X1D_L(3) | A37 | GND | B37 | GND | C37 | | D37 | | E37 |
| X1D_L(4) | A38 | X1D_L(2) | B38 | X1BE_L(0) | C38 | GND | D38 | GND | E38 |
| GND | A39 | GND | B39 | GND | C39 | | D39 | X1BLK_L | E39 |
| X1D_L(6) | A40 | X1D_L(5) | B40 | X1PAR_L | C40 | GND | D40 | GND | E40 |
| X1D_L(8) | A41 | GND | B41 | GND | C41 | | D41 | X1RST_L | E41 |
| X1D_L(9) | A42 | X1D_L(7) | B42 | X1ADS_L | C42 | GND | D42 | GND | E42 |
| GND | A43 | GND | B43 | X1D_L(11) | C43 | | D43 | MIOC_INTREQ_L | E43 |
| X1D_L(12) | A44 | X1D_L(10) | B44 | X1BE_L(1) | C44 | GND | D44 | GND | E44 |
| X1D_L(14) | A45 | GND | B45 | X1XSTBN_L | C45 | X1XSTBP_L | D45 | | E45 |
| X1D_L(15) | A46 | X1D_L(13) | B46 | GND | C46 | GND | D46 | GND | E46 |
| GND | A47 | GND | B47 | | C47 | X1HSTBP_L | D47 | GND | E47 |
| X1CLK | A48 | | B48 | GND | C48 | X1HSTBN_L | D48 | GND | E48 |

**Note:** Pins with no assignment (blank) are reserved. These signals may, or may not be electrically active and should be left as no connection on any interface card.

The I/O baseboard uses a connector equivalent to the BERG 73956-9003* to interface with the A450NX CPU baseboard.

## 5.7.1.2   PCI Connectors (32-bit)

*Table 5-8.    PCI Connectors (32-bit)*

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|-----|--------|-----|--------|
| A1 | TRST_L | A32 | AD16 | B1 | -12V | B32 | AD17 |
| A2 | +12V | A33 | +3.3V | B2 | TCK | B33 | C/BE2_L |
| A3 | TMS | A34 | FRAME_L | B3 | GND | B34 | GND |
| A4 | TDI | A35 | GND | B4 | TDO | B35 | IRDY_L |
| A5 | +5V | A36 | TRDY_L | B5 | +5V | B36 | +3.3V |
| A6 | INTA_L | A37 | GND | B6 | +5V | B37 | DEVSEL_L |
| A7 | INTC_L | A38 | STOP_L | B7 | INTB_L | B38 | GND |
| A8 | +5V | A39 | +3.3V | B8 | INTD_L | B39 | LOCK_L |
| A9 | RESERVED | A40 | SDONE | B9 | PRSNT1_L | B40 | PERR_L |
| A10 | +5V | A41 | SB0_L | B10 | RESERVED | B41 | +3.3V |
| A11 | RESERVED | A42 | GND | B11 | PRSNT2_L | B42 | SERR_L |
| A12 | GND [†] | A43 | PAR | B12 | GND [†] | B43 | +3.3V |
| A13 | GND [†] | A44 | AD15 | B13 | GND [†] | B44 | C/BE1_L |

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|-----|--------|-----|--------|
| A14 | RESERVED | A45 | +3.3V | B14 | RESERVED | B45 | AD14 |
| A15 | RESET_L | A46 | AD13 | B15 | GND | B46 | GND |
| A16 | +5V | A47 | AD11 | B16 | CLK | B47 | AD12 |
| A17 | GRANT_L | A48 | GND | B17 | GND | B48 | AD10 |
| A18 | GND | A49 | AD9 | B18 | REQ_L | B49 | GND |
| A19 | RESERVED | A50 |  | B19 | +5V | B50 |  |
| A20 | AD30 | A51 |  | B20 | AD31 | B51 |  |
| A21 | +3.3V | A52 | C/BEO_L | B21 | AD29 | B52 | AD8 |
| A22 | AD28 | A53 | +3.3V | B22 | GND | B53 | AD7 |
| A23 | AD26 | A54 | AD6 | B23 | AD27 | B54 | +3.3V |
| A24 | GND | A55 | AD4 | B24 | AD25 | B55 | AD5 |
| A25 | AD24 | A56 | GND | B25 | +3.3V | B56 | AD3 |
| A26 | IDSEL | A57 | AD2 | B26 | C/BE3_L | B57 | GND |
| A27 | +3.3V | A58 | AD0 | B27 | AD23 | B58 | AD1 |
| A28 | AD22 | A59 | +5V | B28 | GND | B59 | +5V |
| A29 | AD20 | A60 | REQ64_L | B29 | AD21 | B60 | ACK64_L |
| A30 | GND | A61 | +5V | B30 | AD19 | B61 | +5V |
| A31 | AD18 | A62 | +5V | B31 | +3.3V | B62 | +5V |

† Indicates slot serves +5 V compliant devices only.

The I/O baseboard uses a connector equivalent to the AMP 646255-1* to interface with the 32-bit PCI bus.

## 5.7.1.3    PCI Connectors (64-bit)

A 64-bit PCI connector is identical to a 32-bit PCI connector for pins A1-A62 and B1-B62.  Table 5-9 indicates the extension pins necessary for PCI-64 compliance.

*Table 5-9.      PCI Connectors (64-bit)*

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| A63 | GND | B63 | RESERVED |
| A64 | C/BE7_L | B64 | GND |
| A65 | C/BE5_L | B65 | C/BE6_L |
| A66 | +5V | B66 | C/BE4_L |
| A67 | PAR64 | B67 | GND |
| A68 | AD62 | B68 | AD63 |
| A69 | GND | B69 | AD61 |
| A70 | AD60 | B70 | +5V |
| A71 | AD58 | B71 | AD59 |
| A72 | GND | B72 | AD57 |
| A73 | AD56 | B73 | GND |
| A74 | AD54 | B74 | AD55 |
| A75 | +5V | B75 | AD53 |
| A76 | AD52 | B76 | GND |

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| A77 | AD50 | B77 | AD51 |
| A78 | GND | B78 | AD49 |
| A79 | AD48 | B79 | +5V |
| A80 | AD46 | B80 | AD47 |
| A81 | GND | B81 | AD45 |
| A82 | AD44 | B82 | GND |
| A83 | AD42 | B83 | AD43 |
| A84 | +5V | B84 | AD41 |
| A85 | AD40 | B85 | +5V |
| A86 | AD38 | B86 | AD39 |
| A87 | GND | B87 | AD37 |
| A88 | AD36 | B88 | +5V |
| A89 | AD34 | B89 | AD35 |
| A90 | GND | B90 | AD33 |
| A91 | AD32 | B91 | GND |
| A92 | RESERVED | B92 | RESERVED |
| A93 | GND | B93 | RESERVED |
| A94 | RESERVED | B94 | GND |

The I/O baseboard uses a connector equivalent to the AMP 145034-1* to interface with the 64-bit PCI bus.

## 5.7.1.4   SCSI Connector

*Table 5-10.    SCSI Connector*

| Signal Name | Conn. Pin | Cable Pin | Cable Pin | Conn. Pin | Signal Name |
|---|---|---|---|---|---|
| GROUND | 1 | 1 | 2 | 35 | -DB(12) |
| GROUND | 2 | 3 | 4 | 36 | -DB(13) |
| GROUND | 3 | 5 | 6 | 37 | -DB(14) |
| GROUND | 4 | 7 | 8 | 38 | -DB(15) |
| GROUND | 5 | 9 | 10 | 39 | -DB(P1) |
| GROUND | 6 | 11 | 12 | 40 | -DB(0) |
| GROUND | 7 | 13 | 14 | 41 | -DB(1) |
| GROUND | 8 | 15 | 16 | 42 | -DB(2) |
| GROUND | 9 | 17 | 18 | 43 | -DB(3) |
| GROUND | 10 | 19 | 20 | 44 | -DB(4) |
| GROUND | 11 | 21 | 22 | 45 | -DB(5) |
| GROUND | 12 | 23 | 24 | 46 | -DB(6) |
| GROUND | 13 | 25 | 26 | 47 | -DB(7) |
| GROUND | 14 | 27 | 28 | 48 | -DB(P) |
| GROUND | 15 | 29 | 30 | 49 | GROUND |
| GROUND | 16 | 31 | 32 | 50 | GROUND |
| TERMPWR | 17 | 33 | 34 | 51 | TERMPWR |

| Signal Name | Conn. Pin | Cable Pin | Cable Pin | Conn. Pin | Signal Name |
|---|---|---|---|---|---|
| TERMPWR | 18 | 35 | 36 | 52 | TERMPWR |
| RESERVED (NC) | 19 | 37 | 38 | 53 | RESERVED |
| GROUND | 20 | 39 | 40 | 54 | GROUND |
| GROUND | 21 | 41 | 42 | 55 | -ATN |
| GROUND | 22 | 43 | 44 | 56 | GROUND |
| GROUND | 23 | 45 | 46 | 57 | -BSY |
| GROUND | 24 | 47 | 48 | 58 | -ACK |
| GROUND | 25 | 49 | 50 | 59 | -RST |
| GROUND | 26 | 51 | 52 | 60 | -MSG |
| GROUND | 27 | 53 | 54 | 61 | -SEL |
| GROUND | 28 | 55 | 56 | 62 | -C/D |
| GROUND | 29 | 57 | 58 | 63 | -REQ |
| GROUND | 30 | 59 | 60 | 64 | -I/O |
| GROUND | 31 | 61 | 62 | 65 | -DB(8) |
| GROUND | 32 | 63 | 64 | 66 | -DB(9) |
| GROUND | 33 | 65 | 66 | 67 | -DB(10) |
| GROUND | 34 | 67 | 68 | 68 | -DB(11) |

The I/O baseboard uses a connector equivalent to the FOXCONN QA01343-P4* or equivalent to interface to the SCSI bus.

## 5.7.1.5   ISA Connector

*Table 5-11.    ISA Connector*

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| B1 | GND | A1 | IOCHK_L |
| B2 | RESET | A2 | SD7 |
| B3 | +5V | A3 | SD6 |
| B4 | IRQ9 | A4 | SD5 |
| B5 | -5V | A5 | SD4 |
| B6 | DRQ2 | A6 | SD3 |
| B7 | -12V | A7 | SD2 |
| B8 | SRDY_L | A8 | SD1 |
| B9 | +12V | A9 | SD0 |
| B10 | GND | A10 | IOCHRDY |
| B11 | SMEMW_L | A11 | AEN |
| B12 | SMEMR_L | A12 | SA19 |
| B13 | IOW_L | A13 | SA18 |
| B14 | IOR_L | A14 | SA17 |
| B15 | DACK#_3 | A15 | SA16 |
| B16 | DRQ3 | A16 | SA15 |
| B17 | DACK1_L | A17 | SA14 |

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| B18 | DRQ1 | A18 | SA13 |
| B19 | REFRESH | A19 | SA12 |
| B20 | BCLK | A20 | SA11 |
| B21 | IRQ7 | A21 | SA10 |
| B22 | IRQ6 | A22 | SA9 |
| B23 | IRQ5 | A23 | SA8 |
| B24 | IRQ4 | A24 | SA7 |
| B25 | IRQ3 | A25 | SA6 |
| B26 | DACK2_L | A26 | SA5 |
| B27 | TC | A27 | SA4 |
| B28 | BALE | A28 | SA3 |
| B29 | +5V | A29 | SA2 |
| B30 | 14MHz | A30 | SA1 |
| B31 | GND | A31 | SA0 |
| D1 | MEMCS16_L | C1 | SGHE_I |
| D2 | IOCS16_L | C2 | LA23 |
| D3 | IRQ10 | C3 | LA22 |
| D4 | IRQ11 | C4 | LA21 |
| D5 | IRQ12 | C5 | LA20 |
| D6 | IRQ15 | C6 | LA19 |
| D7 | IRQ14D | C7 | LA18 |
| D8 | ACK0_L | C8 | LA17 |
| D9 | DRQ0 | C9 | MEMR_L |
| D10 | DACK5_L | C10 | MEMW_L |
| D11 | DRQ5 | C11 | SD8 |
| D12 | DACK6_L | C12 | SD9 |
| D13 | DRQ6 | C13 | SD10 |
| D14 | DACK7_L | C14 | SD11 |
| D15 | DRQ7 | C15 | SD12 |
| D16 | +5V | C16 | SD13 |
| D17 | MASTER16_L | C17 | SD14 |
| D18 | GND | C18 | SD15 |

The  I/O baseboard uses a connector equivalent to the AMP 176139-2* or equivalent to interface to the ISA bus.

## 5.7.1.6    IDE Connector

*Table 5-12.    IDE Connector*

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | RSTDRV | 2 | GROUND |
| 3 | DD7 | 4 | DD8 |
| 5 | DD6 | 6 | DD9 |
| 7 | DD5 | 8 | DD10 |
| 9 | DD4 | 10 | DD1 |
| 11 | DD3 | 12 | DD12 |
| 13 | DD2 | 14 | DD13 |
| 15 | DD1 | 16 | DD14 |
| 17 | DD0 | 18 | DD15 |
| 19 | GROUND | 20 | KEY PIN |
| 21 | DRQ | 22 | GROUND |
| 23 | DIOW | 24 | GROUND |
| 25 | DIOR | 26 | GROUND |
| 27 | IORDY | 28 | CSEL |
| 29 | DACK | 30 | GROUND |
| 31 | IRQ | 32 | No Connection |
| 33 | DA1 | 34 | No Connection |
| 35 | DA0 | 36 | DA2 |
| 37 | CS1P_L | 38 | DS3P_L |
| 39 | DHACT_L | 40 | GROUND |

The I/O baseboard uses a connector equivalent to the AMP 111945-8* 40-pin header or equivalent to interface to both the primary and secondary IDE buses.

## 5.7.1.7    Floppy Disk Port Connection

*Table 5-13.    Floppy Disk Connector*

| Pin | Name | Pin | Name |
|-----|------|-----|------|
| 1 | GND | 2 | FD_DENSEL |
| 3 | GND | 4 | n/c |
| 5 | Key | 6 | FD_DRATE0 |
| 7 | GND | 8 | FD_INDEX_L |
| 9 | GND | 10 | FD_MTR0_L |
| 11 | GND | 12 | FD_DR1_L |
| 13 | GND | 14 | FD_DR0_L |
| 15 | GND | 16 | FD_MTR1_L |
| 17 | FD_MSEN1 | 18 | FD_DIR_L |
| 19 | GND | 20 | FD_STEP_L |

| Pin | Name | Pin | Name |
|-----|------|-----|------|
| 21 | GND | 22 | FD_WDATA_L |
| 23 | GND | 24 | FD_WGATE_L |
| 25 | GND | 26 | FD_TRK0_L |
| 27 | FD_MSEN0 | 28 | FD_WPROT_L |
| 29 | GND | 30 | FD_RDATA_L |
| 31 | GND | 32 | FD_HDSEL_L |
| 33 | GND | 34 | FD_DSKCHG_L |

The I/O baseboard uses a connector equivalent to the AMP 111944-7* or equivalent to interface to the floppy port.

## 5.7.1.8 USB Connector

*Table 5-14.    USB Connector*

| Pin | Signal | Description |
|-----|--------|-------------|
| A1 | VCC | Over Current Monitor Line Port 0 |
| A2 | DATAL0 | Differential Data Line Paired with DATAH0 |
| A3 | DATAH0 | Differential Data Line Paried with DATAL0 |
| A4 | GND | Ground Potential |
| B1 | VCC | Over Current Monitor Line Port 1 |
| B2 | DATAL1 | Differential Data Line Paired with DATAH1 |
| B3 | DATAH1 | Differential Data Line Paried with DATAL1 |
| B4 | GND | Ground Potential |

The I/O baseboard uses a connector equivalent to the FOXCONN/Hon Haj DM10156-73* or equivalent to interface to the USB.

## 5.7.1.9 Front Panel Connector

*Table 5-15.    Front Panel Connector*

| Header Pin Number | Signal(s) | Header Pin Number | Signal(s) |
|-------------------|-----------|-------------------|-----------|
| 1 | GROUND | 2 | +5V |
| 3 | VCC_STDBY | 4 | GROUND |
| 5 | ISP_SCLK | 6 | FAN_FAILED_L |
| 7 | ISP_SDI | 8 | SPEAKER_DATA |
| 9 | ISP_FPC_EN_L | 10 | INTRUSION_L |
| 11 | ISP_MODE | 12 | Reserved |
| 13 | ISP_FPC_SDO | 14 | GROUND |
| 15 | VCC_STDBY | 16 | BMC_TO_FPC_RST_CMD |
| 17 | GROUND | 18 | PROC_RESET_L |
| 19 | COM2_TO_FP_EN | 20 | SYS_RESET_STATE |
| 21 | COM2_TO_SIO_EN_A | 22 | RST_SFC_L |

| Header Pin Number | Signal(s) | Header Pin Number | Signal(s) |
|---|---|---|---|
| 23 | XIMB_SOUT_EN | 24 | SECURE_MODE_BMC |
| 25 | VCC_STDBY | 26 | HARD_RESET |
| 27 | Reserved | 28 | FP_NMI_SWT_L |
| 29 | SIN_TTL_COM2 | 30 | Reserved |
| 31 | SIN_TTL_XIMB | 32 | GROUND |
| 33 | SOUT_TTL_COM2 | 34 | PWR_CNTRL_SFC_L |
| 35 | SOUT_TTL_XIMB | 36 | PWR_CNTRL_RTC_L |
| 37 | Reserved | 38 | PWR_GOOD |
| 39 | GROUND | 40 | PS_PWR_ON |
| 41 | DCD_TTL_FP | 42 | GROUND |
| 43 | DSR_TTL_FP | 44 | I2C_CEL_CONNECT_FPC |
| 45 | CTS_TTL_FP | 46 | I2C_CEL_CONNECT_BMC_A |
| 47 | RI_TTL_FP | 48 | I2C_FPC_SCL |
| 49 | GROUND | 50 | I2C_FPC_SDA |
| 51 | VCC_STDBY | 52 | GROUND |
| 53 | RTS_TTL_FP | 54 | Reserved |
| 55 | DTR_TTL_FP | 56 | I2C_BACKUP_SCL |
| 57 | GROUND | 58 | I2C_BACKUP_SDA |
| 59 | Key Position | 60 | GROUND |

## 5.7.1.10  Server Management Feature Connector Pin Assignments

*Table 5-16.     Feature Connector Pin Assignments*

| Pin | Name | Pin | Name |
|---|---|---|---|
| 1 | SMI# | 2 | I2CCLK |
| 3 | CONP | 4 | key |
| 5 | PWROFF# | 6 | I2CDATA |
| 7 | LPOK | 8 | KEYUNLK |
| 9 | NMI | 10 | HostAUX |
| 11 | RESET# | 12 | GND |
| 13 | GND | 14 | key |
| 15 | SECURE | 16 | GND |
| 17 | INTRUD# | 18 | NMI_L |
| 19 | INIT_L | 20 | GND |
| 21 | KB_DATA | 22 | MS_DATA |
| 23 | KB_CLK | 24 | MS_CLK |
| 25 | Key | 26 | RESET_BMC_L |

## 5.7.1.11  Auxilliary IPMB (I$^2$C) Connector

*Table 5-17.    IPMB Connector*

| Name | Pin |
|------|-----|
| CLK  | 1   |
| GND  | 2   |
| DATA | 3   |

## 5.7.1.12  Legacy Connections

The I/O baseboard provides connection to VGA, serial, parallel, mouse and keyboard functions by means of an I/O riser card mounted to the baseboard.  The I/O riser card provides a direct user interface. Table 5-18 provides the pinout of the connector on the I/O baseboard, whereas the following sections provide the pinout of the user level interfaces of the A450NX I/O riser card.

*Table 5-18.    Legacy Connections*

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| A1  | VCC_STDBY    | B1  | +5V           |
| A2  | KB_DATA      | B2  | MS_DATA       |
| A3  | KB_CLK       | B3  | MS_CLK        |
| A4  | +5 V         | B4  | SIN_TTL_XIMB  |
| A5  | SOUT_TTL_XIMB| B5  | SIN_TTL_COM2  |
| A6  | PP_SLCT      | B6  | SP0_DCD_L     |
| A7  | PP_PE        | B7  | SP1_DCD_L     |
| A8  | PP_BUSY      | B8  | SP0_SIN       |
| A9  | PP_ACK_L     | B9  | Ground        |
| A10 | Ground       | B10 | SP1_SIN       |
| A11 | PP_DR7       | B11 | SP0_RI_L      |
| A12 | PP_DR6       | B12 | SP1_RI_L      |
| A13 | PP_DR5       | B13 | Ground        |
| A14 | PP_DR4       | B14 | SP0_DTR_L     |
| A15 | Ground       | B15 | SP1_DTR_L     |
| A16 | PP_DR3       | B16 | SP0_SOUT      |
| A17 | PP_DR2       | B17 | SP1_SOUT      |
| A18 | PP_DR1       | B18 | No Connection |
| A19 | PP_DR0       | B19 | SP0_DSR_L     |
| A20 | Ground       | B20 | SP1_DSR_L     |
| A21 | PP_STB_L     | B21 | SP0_RTS_L     |
| A22 | PP_SLIN_L    | B22 | Ground        |
| A23 | PP_INIT_L    | B23 | SP1_RTS_L     |
| A24 | PP_ERR_L     | B24 | SP0_CTS_L     |
| A25 | PP_AFD_L     | B25 | SP1_CTS_L     |
| A26 | I2C_BMC_SCL  | B26 | RTL_TTL_FP_L  |

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| A27 | DSR_TTL_FP | B27 | DTR_TTL_FP_L |
| A28 | CTS_TTL_FP | B28 | DCD_TTL_FP_L |
| A29 | RT_TTL_FP | B29 | I2C_BMC_SDA |
| | Key block | | |
| A30 | COM2_TO_STD_EN | B30 | XIMB_SOUT_EN |
| A31 | COM2_TO_FP_EN | B31 | SOUT_TTL_COM2 |
| A32 | Ground | B32 | PWR_GOOD |
| A33 | Ground | B33 | Ground |
| A34 | Ground | B34 | Ground |
| A35 | V_BLUE | B35 | V_VSYNC |
| A36 | Ground | B36 | Ground |
| A37 | V_GREEN | B37 | V_HSYNC |
| A38 | Ground | B38 | Ground |
| A39 | V_RED | B39 | VR_DDCDAT |
| A40 | Ground | B40 | VR_DDCCLK |

The I/O baseboard uses a connector equivalent to the AMP 650090-3* connector to connect the A450NX I/O riser card to the .  The B signals listed in Table 5-18 are located on the primary side of the I/O riser card (USB connector side, if looking at the I/O baseboard).  The A signals are located on the secondary side of the I/O riser card (ISA slot side, if looking at the I/O baseboard).  Pin 1 is located nearest the front of the card (away from the connectors on the I/O riser card and towards the PXB heat sinks).  Pin 40 is located nearest the connectors.

# 5.7.2    VGA Connector

*Table 5-19.    Video Port Connector Pin Out*

| Pin | Signal | Description | Pin | Signal | Description |
|-----|--------|-------------|-----|--------|-------------|
| 1 | RED | Analog color signal R | 2 | GREEN | Analog color signal G |
| 3 | BLUE | Analog color signal B | 4 | n/c | No connect |
| 5 | GND | Video ground (shield) | 6 | GND | Video ground (shield) |
| 7 | GND | Video ground (shield) | 8 | GND | Video ground (shield) |
| 9 | n/c | No connect | 10 | GND | Video ground |
| 11 | n/c | No connect | 12 | n/c | No connect |
| 13 | HSYNC | Horizontal Sync | 14 | VSYNC | Vertical Sync |
| 15 | n/c | No connect | | | |

## 5.7.2.1    Serial Port Connector

*Table 5-20.    Serial Port Connector*

| Pin | Name | Description | Pin | Name | Description |
|-----|------|-------------|-----|------|-------------|
| 1 | DCD | Data Carrier Detected | 2 | RXD | Receive Data |
| 3 | TXD | Transmit Data | 4 | DTR | Data Terminal Ready |
| 5 | GND | Ground | 6 | DSR | Data Set Ready |

| Pin | Name | Description | Pin | Name | Description |
|-----|------|-------------|-----|------|-------------|
| 7 | RTS | Return to Send | 8 | CTS | Clear to Send |
| 9 | RIA | Ring Indication Active | | | |

The I/O baseboard uses a connector equivalent to the FOXCONN/Hon Haj DM10156-73* connector to interface with each serial port.

## 5.7.2.2    Parallel Port Connector

*Table 5-21      Parallel Port Connector*

| Pin | Name | Pin | Name |
|-----|------|-----|------|
| 1 | STROBE_L | 14 | AUFDXT_L |
| 2 | D0 | 15 | ERROR_L |
| 3 | D1 | 16 | INIT_L |
| 4 | D2 | 17 | SLCTIN_L |
| 5 | D3 | 18 | GND |
| 6 | D4 | 19 | GND |
| 7 | D5 | 20 | GND |
| 8 | D6 | 21 | GND |
| 9 | D7 | 22 | GND |
| 10 | ACK_L | 23 | GND |
| 11 | BUSY | 24 | GND |
| 12 | PE | 25 | GND |
| 13 | SLCT | | |

## 5.7.2.3    Mouse Connector

*Table 5-22.     Mouse Connector*

| Pin | Signal | Description |
|-----|--------|-------------|
| 7 | MSEDAT | Mouse Data |
| 8 | (NC) | |
| 9 | GND | |
| 10 | FUSED_VCC | |
| 11 | MSECLK | Mouse Clock |
| 12 | (NC) | |

## 5.7.2.4    Keyboard Connector

*Table 5-23.     Keyboard Connector*

| Pin | Signal | Description |
|-----|--------|-------------|
| 1 | KEYDAT | Keyboard Data |
| 2 | (NC) | |

| Pin | Signal | Description |
|-----|--------|-------------|
| 3 | GND | |
| 4 | FUSED_VCC | |
| 5 | KEYCLK | Keyboard Clock |
| 6 | (NC) | |

## 5.7.3   CPU Baseboard

Table 5-24 shows the reference designators, quantity, manufacturer, and part number for connectors on the CPU baseboard.  The items in Table 5-24 reference the components shown on the CPU baseboard layout diagram, Figure 2-5.

*Table 5-24.    CPU Baseboard (5-slot) Connector Definition*

| Item | Ref. Designator(s) | Qty | Mfr. And Part # | Description |
|------|--------------------|-----|-----------------|-------------|
| 1 | J10, J11, J12, J13, J14 | 5 | MOLEX 71109-5005* | Slot type 2 and DSM cluster connector 330-pin |
| 2 | J1, J2, J3, J4, J5, J6, J7, J8 | 8 | BERG 95798-011* | VRM 8 socket 40-pin |
| 3 | J18A, J18B, J19A, J19B | 2 | BERG 73481-101* | Memory connector 150 signal and power pins; 1 of each to make one 300-pin memory connector |
| | | 2 | BERG 73481-102* | |
| 4 | J20 | 1 | BERG 73956-9002* | 240-pin signal module connector plus guide post (5 row x 48 pins) (Futurebus+* style) |
| 5 | J21 | 1 | BERG 73957-9001* | 90-blade power module connector plus guide post (Futurebus+ style) |
| 6 | J31 | 1 | MOLEX 90367-7015* | Bus Ratio Jumper block |
| 7 | J8C1 | 1 | AMP 146225-3* | APIC Jumper block |

**Note:** The 4-slot CPU baseboard does not have DSM cluster connectors (J14) and its corresponding two VRM sockets (J7, J8) and the APIC jumper block (J8C1).  The remaining connectors are the same on both the 4-slot and the 5-slot CPU baseboards.

## 5.7.4   Memory and Memory Terminator Module

The memory module and memory terminator module (also known as memory boards) use Berg Futurebus+* pin-and-socket connectors for interfacing with the CPU baseboard.  Each of the two memory boards uses one connector.  Therefore, there are two connectors.  Each of these two connectors actually consists of two 150-pin Futurebus+ modules, forming a single 300-pin memory connector.  To achieve a 1:1 signal/ground ratio, half of the signal pins on the modules are connected to ground.  Sections 3.4.1.4 and 3.4.1.5 give the pinouts for these connectors.  Note that the individual modules are designated references of J18A, J18B, J19A, and J19B, but each pair of modules makes up one connector and is more simply referred-to as J18 and J19, respectively.  Each connector, therefore, has rows numbered 1-60 (two sets of pins that would otherwise each be numbered 1-30).  Note that in Table 5-25, signals marked with parentheses and *no* comma indicate one signal of a bus, for example ADDRESS(1).  Signals marked with parentheses and *one* comma indicate a single signal which is differentiated between the two memory connectors (first connector 1, then connector 2), for example EXAMPLE_SIGNAL(A,B)_L would refer to two similar signals that appear on the same pin at each connector, one of which is EXAMPLE_SIGNALA_L and the other of which is EXAMPLE_SIGNALB_L.
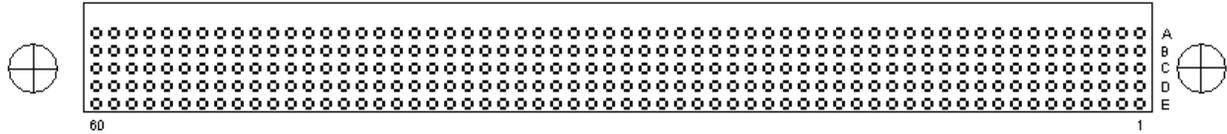
*Figure 5-17.   CPU Baseboard Memory Connector Pin Diagram*

Figure 5-17 represents a top view of the connector pins.  Each pin is rated at 1A.

*Table 5-25.     CPU Baseboard Memory Signal Connector Pinout*

| Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin |
|---|---|---|---|---|---|---|---|---|---|
| GND | A01 | MD_L(36) | B01 | GND | C01 | MD_L(37) | D01 | +3.3V | E01 |
| +1.5V | A02 | +3.3V | B02 | DSTBN_L(2) | C02 | GND | D02 | MD_L(38) | E02 |
| GND | A03 | MD_L(39) | B03 | GND | C03 | MD_L(40) | D03 | +3.3V | E03 |
| MD_L(41) | A04 | +3.3V | B04 | DSTBP_L(2) | C04 | GND | D04 | MD_L(42) | E04 |
| GND | A05 | MD_L(43) | B05 | GND | C05 | MD_L(44) | D05 | +3.3V | E05 |
| MD_L(45) | A06 | +3.3V | B06 | MD_L(46) | C06 | GND | D06 | MD_L(47) | E06 |
| GND | A07 | MD_L(48) | B07 | GND | C07 | MD_L(49) | D07 | +3.3V | E07 |
| MD_L(50) | A08 | +3.3V | B08 | MD_L(51) | C08 | GND | D08 | MD_L(52) | E08 |
| GND | A09 | MD_L(53) | B09 | GND | C09 | WDEVT_L | D09 | +3.3V | E09 |
| DCMPLT(A,B)_L | A10 | +3.3V | B10 | MD_L(54) | C10 | GND | D10 | DVALID(A,B)_L | E10 |
| GND | A11 | GND | B11 | +1.5V | C11 | MD_L(55) | D11 | +3.3V | E11 |
| MUXCLK1(A,B) | A12 | GND | B12 | MD_L(56) | C12 | GND | D12 | MD_L(57) | E12 |
| GND | A13 | GND | B13 | +1.5V | C13 | MD_L(58) | D13 | +3.3V | E13 |
| MD_L(59) | A14 | +3.3V | B14 | DSTBP_L(3) | C14 | GND | D14 | MD_L(60) | E14 |
| GND | A15 | MD_L(61) | B15 | GND | C15 | MD_L(62) | D15 | +3.3V | E15 |
| MD_L(63) | A16 | +3.3V | B16 | DSTBN_L(3) | C16 | GND | D16 | MD_L(64) | E16 |
| GND | A17 | MD_L(65) | B17 | GND | C17 | MD_L(66) | D17 | +3.3V | E17 |
| +1.5V | A18 | +3.3V | B18 | MD_L(67) | C18 | GND | D18 | MD_L(68) | E18 |
| GND | A19 | MD_L(69) | B19 | GND | C19 | MD_L(70) | D19 | +3.3V | E19 |
| MD_L(71) | A20 | +3.3V | B20 | +3.3V | C20 | GND | D20 | +3.3V | E20 |
| GND | A21 | NC | B21 | GND | C21 | NC | D21 | +3.3V | E21 |
| +3.3V | A22 | +3.3V | B22 | CARD_NUM(,2) | C22 | GND | D22 | I2C_BMC_SCL | E22 |
| GND | A23 | GND | B23 | +1.5V | C23 | PWRGDB | D23 | +3.3V | E23 |
| SDRAM(A,B)_CLK | A24 | GND | B24 | PHIT(A,B)L | C24 | GND | D24 | I2C_BMC_SDA | E24 |
| GND | A25 | GND | B25 | +1.5V | C25 | RHIT(A,B)_L | D25 | +3.3V | E25 |
| +1.5V | A26 | +3.3V | B26 | RCMPLT(A,B)_L | C26 | GND | D26 | +3.3V | E26 |
| GND | A27 | CARD(0,1)_L | B27 | GND | C27 | GRCMPLT_L | D27 | +3.3V | E27 |
| CMND0_L | A28 | +3.3V | B28 | BANK0_L | C28 | GND | D28 | BANK1_L | E28 |
| GND | A29 | BANK2_L | B29 | GND | C29 | CMND1_L | D29 | +3.3V | E29 |
| GDCMPLT_L | A30 | +3.3V | B30 | ROW_L | C30 | GND | D30 | CSTB_L | E30 |
| GND | A31 | GND | B31 | +1.5V | C31 | MA_L(0) | D31 | +3.3V | E31 |
| RCGCLK0(A,B) | A32 | GND | B32 | MA_L(1) | C32 | GND | D32 | MA_L(2) | E32 |
| GND | A33 | GND | B33 | +1.5V | C33 | MA_L(3) | D33 | +3.3V | E33 |
| MA_L(4) | A34 | +3.3V | B34 | MA_L(5) | C34 | GND | D34 | MA_L(6) | E34 |
| GND | A35 | MA_L(7) | B35 | GND | C35 | MA_L(8) | D35 | +3.3V | E35 |
| MA_L(9) | A36 | +3.3V | B36 | MA_L(10) | C36 | GND | D36 | MA_L(11) | E36 |
| GND | A37 | MA_L(12) | B37 | GND | C37 | MA_L(13) | D37 | +3.3V | E37 |
| +1.5V | A38 | +3.3V | B38 | MEM(A,B)_TMS | C38 | GND | D38 | +3.3V | E38 |
| GND | A39 | GND | B39 | +1.5V | C39 | MEM(A,B)_TRST_L | D39 | +3.3V | E39 |
| RCGCLK1(A,B) | A40 | GND | B40 | MEM(A,B)_TDI | C40 | GND | D40 | (MEMB_TDI,IO_TDI) | E40 |
| GND | A41 | GND | B41 | +1.5V | C41 | MEM(A,B)_TCK | D41 | +3.3V | E41 |
| MD_L(0) | A42 | +3.3V | B42 | MD_L(1) | C42 | GND | D42 | MD_L(2) | E42 |
| GND | A43 | MD_L(3) | B43 | GND | C43 | MD_L(4) | D43 | +3.3V | E43 |

| Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|--------|-----|--------|-----|--------|-----|
| MD_L(5) | A44 | +3.3V | B44 | DSTBN_L(0) | C44 | GND | D44 | MD_L(6) | E44 |
| GND | A45 | MD_L(7) | B45 | GND | C45 | MD_L(8) | D45 | +3.3V | E45 |
| MD_L(9) | A46 | +3.3V | B46 | DSTBP_L(0) | C46 | GND | D46 | MD_L(10) | E46 |
| GND | A47 | MD_L(11) | B47 | GND | C47 | MD_L(12) | D47 | +3.3V | E47 |
| MD_L(13) | A48 | +3.3V | B48 | MD_L(14) | C48 | GND | D48 | MD_L(15) | E48 |
| GND | A49 | D0FF1_L | B49 | GND | C49 | DOFF0_L | D49 | +3.3V | E49 |
| MD_L(16) | A50 | +3.3V | B50 | DSEL(0,1)_L | C50 | GND | D50 | MRESET_L | E50 |
| GND | A51 | GND | B51 | +1.5V | C51 | MD_L(17) | D51 | +3.3V | E51 |
| MUXCLK0(A,B) | A52 | GND | B52 | MD_L(18) | C52 | GND | D52 | MD_L(19) | E52 |
| GND | A53 | GND | B53 | +1.5V | C53 | MD_L(20) | D53 | +3.3V | E53 |
| MD_L(21) | A54 | +3.3V | B54 | MD_L(22) | C54 | GND | D54 | MD_L(23) | E54 |
| GND | A55 | MD_L(24) | B55 | GND | C55 | MD_L(25) | D55 | +3.3V | E55 |
| MD_L(26) | A56 | +3.3V | B56 | DSTBP_L(1) | C56 | GND | D56 | MD_L(27) | E56 |
| GND | A57 | MD_L(28) | B57 | GND | C57 | MD_L(29) | D57 | +3.3V | E57 |
| +1.5V | A58 | +3.3V | B58 | DSTBN_L(1) | C58 | GND | D58 | MD_L(30) | E58 |
| GND | A59 | MD_L(31) | B59 | GND | C59 | MD_L(32) | D59 | +3.3V | E59 |
| MD_L(33) | A60 | +3.3V | B60 | MD_L(34) | C60 | GND | D60 | MD_L(35) | E60 |

## 5.7.5   Interconnect Backplane

Table 5-26 shows the quantity and manufacturer's part numbers for all connectors on the interconnect backplane.

*Table 5-26.    Interconnect Backplane Connector Definitions*

| Qty. | Mfr(s). and Part # | Description |
|------|--------------------|-------------|
| 1 | Similar to BERG 73926-1001* | Futurebus power module, CPU side |
| 1 | Similar to BERG 73925-1003* | Futurebus power module, I/O side |
| 1 | Similar to BERG 73925-1002* | Futurebus signal module, CPU side |
| 1 | Similar to BERG 73925-1001* | Futurebus signal module, I/O side |
| 4 | Similar to BERG 70295-001* | Futurebus receptacle guide pin |
| 3 | Similar to MOLEX 39-29-9242* | Mini-Fit, Jr. 24-pin power connector |
| 1 | Similar to AMP 111944-7* | 34-pin server management connector |

## 5.7.5.1   Power Connectors

The interconnect backplane channels power from the power distribution system to the I/O and CPU baseboards. Power input to the interconnect backplane is accomplished via three Molex Mini-Fit, Jr. power connectors.  These connectors provide +5 V, +3 V, +12 V, -12 V, and ground to the interconnect backplane; these voltages are also routed to the Berg Futurebus connectors and bulk capacitors.

Table 5-27 describes the pinouts for the three Molex Mini-Fit, Jr. power connectors and the wire colors of the cables that plug into them from the power distribution backplane in the AD450NX server chassis.  Note, all three connectors have the identical pinout.

*Table 5-27.    Power Connector Pinout*

| Pin | Signal | Color | Pin | Signal | Color |
|-----|--------|-------|-----|--------|-------|
| 1 | +5V | RED | 13 | +12V | YELLOW |
| 2 | GROUND | BLACK | 14 | GROUND | BLACK |

| Pin | Signal | Color | Pin | Signal | Color |
|-----|--------|-------|-----|--------|-------|
| 3 | +5V | RED | 15 | +12V | YELLOW |
| 4 | GROUND | BLACK | 16 | GROUND | BLACK |
| 5 | +5V | RED | 17 | +3.3V | ORANGE |
| 6 | GROUND | BLACK | 18 | GROUND | BLACK |
| 7 | +5V | RED | 19 | +3.3V | ORANGE |
| 8 | GROUND | BLACK | 20 | GROUND | BLACK |
| 9 | +5V | RED | 21 | +3.3V | ORANGE |
| 10 | GROUND | BLACK | 22 | GROUND | BLACK |
| 11 | +12V | YELLOW | 23 | +3.3V | ORANGE |
| 12 | GROUND | BLACK | 24 | -12V | BLACK |

# 5.8   Board Level Environmental Specifications

The A450NX board set meets the Intel® *Board Environmental Specification 112000, Rev. G,* with the following exception:

- The minimum operating temperature is specified at +5° C (instead of 0° C).

*Table 5-28.    Board Level Environmental Specifications*

| Temperature | |
|---|---|
| Operating | +5° C to +55° C [†] |
| Non-operating | -40° C to +70° C |
| **Temperature, thermal map** | Must not exceed maximum integrated circuit (IC) junction temperature as specified in the component data sheets |
| **Thermal Shock** | |
| Non-operating | -40° to 70° C (-40° to 158° F) |
| **Shock** | |
| Unpackaged | Trapezoidal, 50 g, 170 in/sec. |
| Packaged | Half sine, 2 msec          Simulated Free Fall<br>Product Weight                Height<br>   < 20-lbs.                        42”<br>      21-40                         36”<br>      41-80                         30”<br>      81-100                        24” |
| **Vibration** | |
| Unpackaged | 5 Hz to 500 Hz, Sine sweep 0.5 G, 15 minutes at each of 3 resonant points |
| | 5 Hz to 500 Hz, 3.1 gRMS random |
| Packaged | 10 Hz to 500 Hz, 1.0 gRMS random |
| **Humidity** | |
| Operating | 85% relative humidity (noncondensing) at 55° C (131° F) |
| Non-operating | 92% relative humidity (noncondensing) at 55° C (131° F) |
| **Altitude** | |
| Operating | To 10,000 ft (3,048 m) |
| Non-operating | To 50,000 ft (15,240 m) |
| **Electrostatic Discharge (ESD)** | |
| Operating | Tested as part of system to 25kV; no component damage |
| **EMI** | |
| Operating | Tested as part of system; required to meet EMI emission requirements |

[†] Chassis design must provide proper air flow.

# 5.9   Thermal Requirements

The recommended air flow for the A450NX CPU baseboard is a minimum of 300 linear feet per minute (LFM) at 40° C, as measured at the right edge of the processor heat sink (closest to the F16 connector).  Intel recommends that air flow direction be from right to left (i.e., from the F16 connector to the VRMs on the CPU baseboard).

To operate within specifications, the A450NX I/O baseboard and the A450NX memory modules require a minimum air flow of 150 LFM at a maximum ambient temperature of 40° C.

These specifications are given as an aid to custom chassis designers.  All chassis and cooling designs should be verified to ensure that all board level components are kept within their respective thermal requirements.

# 5.10 Regulatory Compliance

## Safety:

| U.S. & Canada | UL1950-CSA 950-95, $3^{rd}$ Edition (UL,cUL) |
|---|---|
| Europe | EN 60950, $2^{nd}$ Edition<br><br>IEC 950, $2^{nd}$ Edition<br><br>CE Mark (Declaration of Conformity to European Directive 73/23/EEC) |

## EMC:

When configured in a compatible host system:

| U.S. & Canada | Verified to FCC, CFR Part 15, Class B & IEC-003 |
|---|---|
| Europe | Verified to EN55022 & EN50082-1<br><br>CE Mark (Declaration of Conformity to European Directive 89/336/EEC) |
| Japan | Verified to VCCI (CISPR 22, Class B) |
| Australia / New Zealand | Verified to AS/NZS 3548, Class B |