Intel® A450NX Server System Event Log (SEL) Messages

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2/23/99

Revision Information

Date	Revision	Change
2/23/99	0.40	corrected error in BIOS table

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1. Introduction

This document is provided as a reference to the information displayed by the System Event Log (SEL) Viewer on the Intel® A450NX boards and server systems. It provides a tabular description of the event that has been recorded in the SEL.

1.1 Document Organization

This document is primarily composed of tables containing possible conditions that occur in the SEL along with a definition of the SEL data.

Section 1 contains a brief introduction to the SEL and the SEL Viewer, along with a glossary of terms and acronyms used in this document.

Section 2 contains a table of SEL information generated from the sensors in the Intel® A450NX platform.

Section 3 contains tables of SEL information generated from the Intel® A450NX BIOS.

Section 4 contains tables of SEL information generated from the Intel® A450NX POST.

1.2 Conventions and Terminology

This document uses the following terms and abbreviations:

Table 1-1: Glossary

Term	Definition
BIOS	Basic Input Output System.
BMC	Baseboard Management Controller.
BSP	Boot Strap Processor.
Byte	An 8-bit quantity.
CMOS	In terms of this specification, this describes the PC/AT* compatible region of battery-backed 128 bytes of memory, which normally resides on the baseboard.
DIMM	Dual-inline Memory Module. Name for the plug in modules used to hold the system's DRAM (Dynamic Random Access Memory).
ECC	Error-correcting Code. Refers to a set of additional bits on system RAM that are used to provide a check code that is used to verify memory data integrity.
EEPROM	Electronically Erasable Programmable Read Only Memory
EMP	Emergency Management Port
EvMRev	Event Message Revision
FPC	Front Panel controller
FRB	Fault Resilient Booting. A term used to describe system features and algorithms that improve the likelihood of the detection of, and recovery from, processor failures in a multiprocessor system.
FRU	Field Replaceable Unit.

Term	Definition
HSC	Hot-Swap Controller. Name for the microcontroller that implements the SAF-TE command set and controls the fault lights and drive power on a N440BX Backplane.
IERR	Internal Error. A signal from the Pentium® II Xeon™ processor indicating an internal error condition.
IPMB	Intelligent Platform Management Bus. Name for the architecture, protocol, and implementation of a special bus that interconnects the baseboard and chassis electronics and provides a communications media for system platform management information.
IPMI	Intelligent Platform Management Interface. This protocol is used for communication between microcontrollers, System Management Software, and other 'intelligent' devices on the IPMB.
ISC	Intel® Server Control
NMI	Non-maskable Interrupt. The highest priority interrupt in the system, after SMI. This interrupt has traditionally been used to notify the operating system fatal system hardware error conditions, such as parity errors and unrecoverable bus errors.
NVRAM	Non-Volatile RAM.
PERR	Parity Error. A signal on the PCI bus that indicates a parity error on the bus.
POST	Power On Self Test.
SAF-TE	SCSI Accessed Fault-tolerant Enclosure specification. Describes a set of SCSI commands whereby drive fault status can be sent to an enclosure for the purpose of presenting that fault information with external indicators, such as fault lights. Other commands are provided so certain management information about the enclosure, such as temperature, voltage, number of drive bays, power status, etc., can be retrieved.
SCU	System Configuration Utility. No longer in use. Replaced by SSU.
SDR	Sensor Data Record. A data record that provides platform management sensor type, locations, event generation, and access information.
SEEPROM	Serially Accessed EEPROM (see definition for EEPROM)
SEL	System Event Log. A non-volatile storage area and associated interfaces for storing system platform event information for later retrieval.
SERR	System Error. A signal on the PCI bus that indicates a 'fatal' error on the bus.
SSU	System Setup Utility. Replaces the SCU

1.3 Overview

The System Event Log (SEL) is a non-volatile repository for system events. The SEL Viewer provides an interface for the server administrator to view the SEL. The administrator can use this information to:

- Monitor the server for both warnings, such as when the chassis door on a server has been opened, or potential critical problems, such as when a processor has failed or a temperature threshold has been crossed.
- Examine all system event log entries recorded by the Baseboard Management Controller (BMC). These events can be generated from the BMC, Hot Swap Controller (HSC), Front Panel (FP), BIOS and all the events generated by the firmware.
- Examine SEL records by sensor Type and Number in hex or verbose mode
- Examine SEL records by event Type in hex or verbose mode
- Examine SEL records from a previously stored binary file in hex or verbose mode.

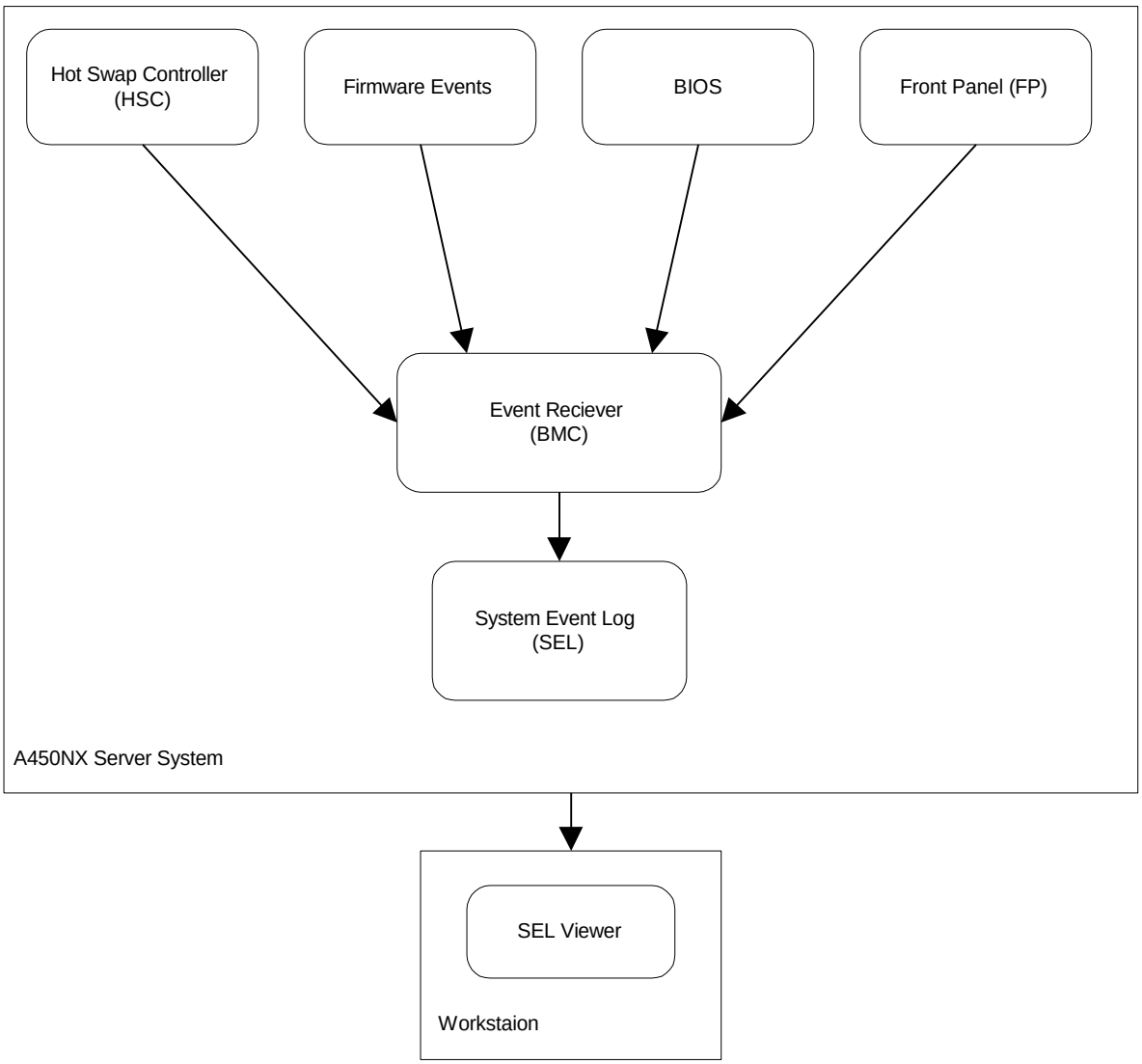

Figure 1-1: Event Message Flow

1.3.1 Sensors

The Intel® A450NX Server System contains sensors that monitor System Health. For example, a management controller that scans temperatures and voltages provides an interface to this information as 'temperature sensors' and 'voltage sensors'.

In the event that a sensor reading exceeds the predefined range, an Event Message is generated. This Event Message is passed to the Baseboard Management Controller (BMC). The BMC passes the event message to the

System Event Log (SEL) where it becomes available for querying by the System Event Log Viewer.

1.3.2 Front Panel Controller

The Front Panel Controller (FPC) powers up when the 5v DC standby becomes available.

The FPC has a SEEPROM that stores FRU information such as the Device Id, Part number, Firmware Version, etc. LEDs on the FP are used to indicate the chassis status.

FPC monitors the state of the Chassis Intrusion and Cover Open Signal. System reset, power control and LCD display are also accomplished through the FPC. The FPC accepts IPMB and ICMB commands and delivers responses as well as reporting status/error conditions by issuing event messages to the designated event receiver.

1.3.3 Event Generator

The BMC itself will typically be responsible for monitoring and managing the system board. For example, monitoring baseboard temperatures and voltages. As such, the BMC will also be an Event Generator, sending the Event Messages that it generates internally to its Event Receiver functionality.

1.3.4 Event Receiver

The Event Receiver is the device that receives Event Messages. In the main computing unit, a particular management controller, referred to as the Baseboard Management Controller (BMC), is normally the Event Receiver for the system.

1.3.5 BIOS

The system BIOS (Basic I/O System) firmware serves many important roles in platform management. It loads and initializes the system management hardware interfaces so they can be accessed later by System Management Software and the Operating System. The BIOS works with the system hardware and management controllers during POST to implement checks of the system and management hardware.

1.3.6 System Event Log (SEL)

The System Event Log (SEL) is the repository for the Event Messages. The System Event Log is implemented as non-volatile storage to ensure that Critical Events entered into the SEL can be retrieved for ‘post-mortem analysis’ should a system failure occur. The platform’s System Event Log is typically of limited size. On Intel® A450NXservers the SEL can hold up to 496 entries or about 8KB. Therefore, it is important to clear the SEL periodically.

If the SEL becomes full it will not delete previous entries. This prevents the first event record, which may provide the most important information on a critical event from being deleted before it can be viewed. If, however, management software such as Intel® Server Control (ISC) has been installed on the server system, it will manage the SEL. ISC will automatically clear the SEL when the log approaches fullness. Since ISC provides a variety of alerting capabilities for critical events it eliminates the need to retain older SEL entries until they are viewed.

1.3.7 Summary of the message flow

A management controller on the Intelligent Platform Management Bus (IPMB) such as the Hot Swap Controller (HSC) scans for events (i.e. Backplane temperature). When an event occurs an Event Message gets send via the IPMB to the designated event receiver, the Baseboard Management Controller (BMC). The BMC receives the Event Message and saves it to the System Event Log. The BMC also generates logs event Messages for its own internally detected events such as Watchdog timeouts and Voltage Events.

1.3.8 SEL Viewer Screen

The SEL Viewer is the user interface to the SEL. This interface can be run both from the Emergency Management Port (EMP) and the System Setup Utility (SSU). It extracts information from the SEL and presents it to the user in either a hex or verbose format. It also provides support for the user to save the current SEL data to a file for later use or clear the current SEL records at the server. If using SSU, the records can be cleared directly from the interface. If using EMP, clearing the log has to be done through the BIOS set up.

Figure 1-2 gives a better idea of the type of information that can be gathered by looking at the SEL Viewer. For documentation purposes, the EMP interface is used here.

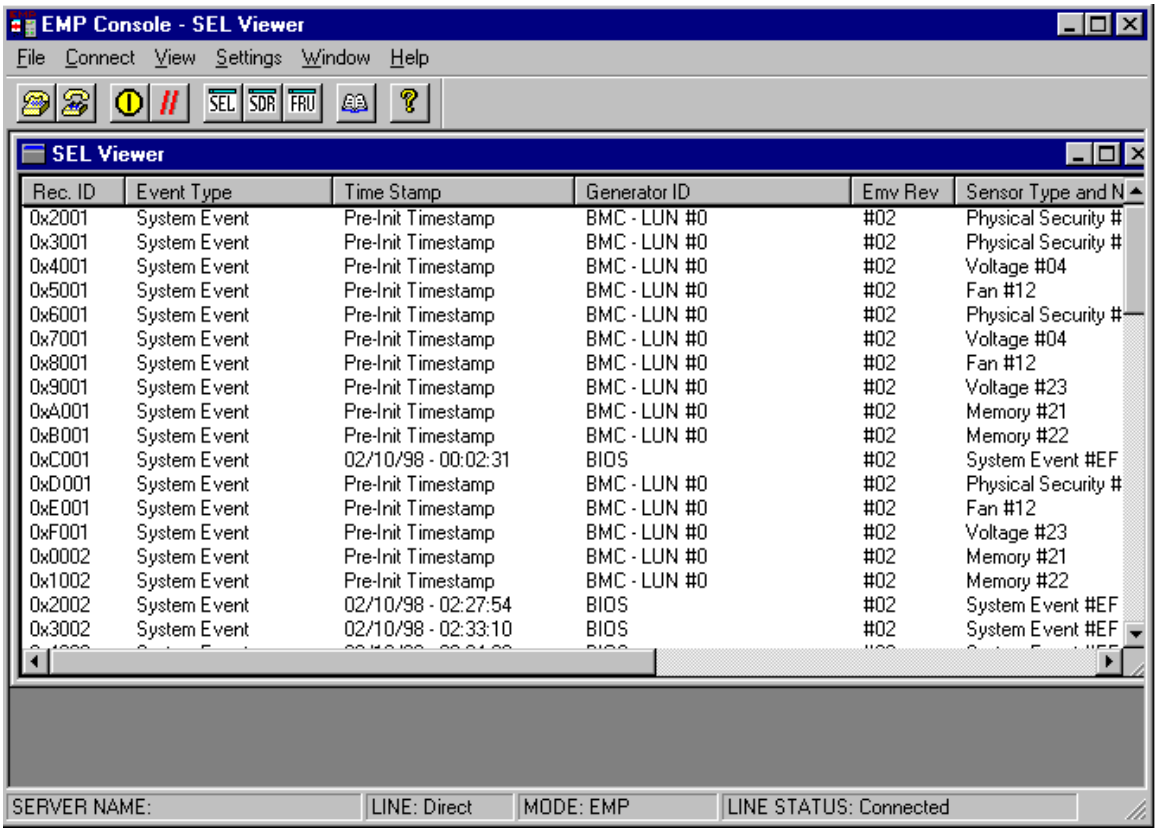

Figure 1-2: SEL Viewer Screen

Rec. ID – A unique id that is generated for each event in the SEL.

Event Type – Indicates what the event pertains to. Currently holds the value of "System Event". This field is for future use.

Time Stamp – The time and the date that the error was generated (Pre_Init Timestamp means no timestamp is available.

Generator ID – This field identifies the device that generated the Event Message.

EmvRev. – This field is used to identify different revisions of the Event Message format. Currently holds the value of "#02". This field is for future use.

Sensor Type – Indicates the event class or type of sensor that generated the Event Message. See table 2-1 for the list of Sensor Types.

Sensor Number – A unique number (within a given sensor device) representing the 'sensor' within the management controller that generated the Event Message. Sensor numbers are used for both identification and access of sensor information, such as getting and setting sensor thresholds. See Table 2-1 for the list of Sensor Types.

Event Description - Short description of the event that generating the entry in the SEL Viewer.

2. Sensor Type Codes

The Sensor Type Code Table provides information regarding:

- The type of sensor generating the SEL entry
- The name of the sensor
- The microcontroller which initiated the SEL entry
- The warning or error which initiated the SEL entry

2.1 Using The System Event Log for Sensor Event Messages

This section uses an example SEL entry to explain the use of the System Event Log Table. For ease of reading and understanding the Event Messages, the verbose view is used. The differences between the verbose view and the hexadecimal view are explained where necessary.

The example on the following page uses Rec. ID 0xE005 (the fourth line of data) in Figure 2-1. This Event Message has been reported by the BMC against Fan #10, otherwise known as Backplane Fan 3 speed. This was determined as follows:

1. Locate the Sensor Type and Sensor Number displayed in **the Sensor Type and Number** field in the SEL Viewer screen (Figure 2-1). This data displays as Fan #10. The Sensor Type (Fan) is displayed first, followed by the Sensor Number #10).
2. Use Table 2-1 to locate “Fan” in the Sensor Type (verbose) column.

   Note: If the example event in Figure 2-1 were displayed in the hexadecimal view, instead of Fan #10,” the Sensor Type and Number would display “04 #10” and it would be necessary to look for “04” in the Hex area of the Sensor Type column.
3. Locate Sensor Number “#10” in the **Sensor Number** column of the table.
4. Use the **Sensor Name** column in the table to determine the sensor or component that caused the Event Message.
5. Use the **Generator ID** column to determine the HSC generated the SEL message.
6. The **Event Description** column of the SEL Viewer screen can be used to obtain more detailed information regarding the event, in this case that a lower critical error has occurred.

Note that Table 2-1 displays six fans (Sensor Type 04) rather than nine and six drive slots (Sensor Type 0D) rather than twelve. All nine fans and twelve drives in the AD450NX server system do have Event Messages reported against them.

The first six fans and the first six drives use the Primary HSC Generator ID. The other three fans and the other six drives use the Secondary HSC Generator ID.

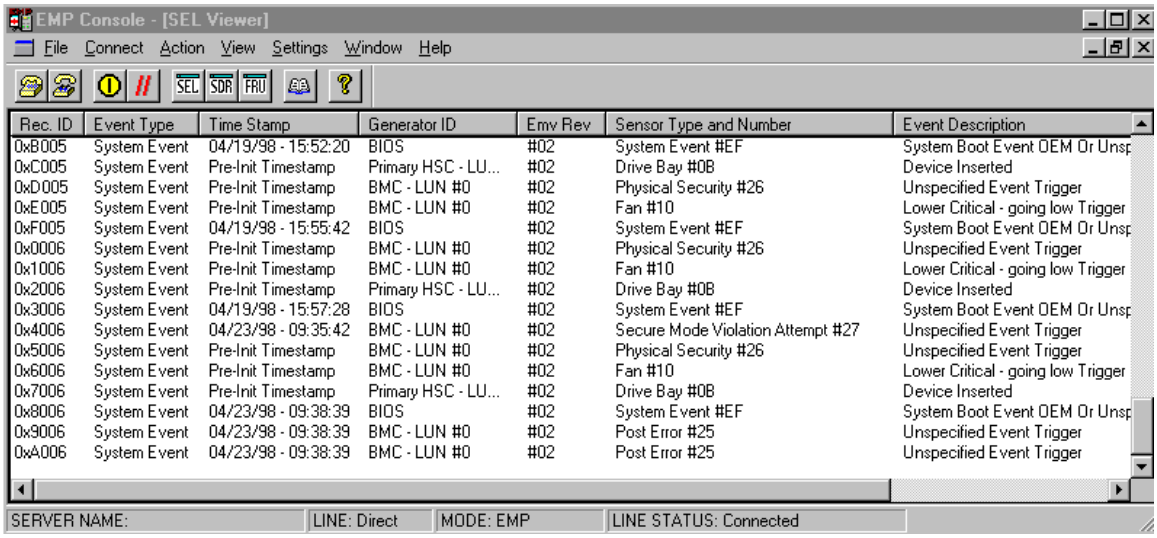

Figure 2-1: Sensor Events

Table 2-1: Sensor System Event Log Table

Sensor Type		Sensor Number	Sensor Name	Generator ID
Verbose	**Hex**			
Temperature	**01**			**BMC+HSC**
		#0A	PXB Temp Monitor	BMC
		#01	Backplane Temperature	HSC1
		#16	CPU Baseboard Temperature Sensor	BMC
		#17	Processor 1 Temperature Sensor	BMC
		#18	Processor 2 Temperature Sensor	BMC
		#19	Processor 3 Temperature Sensor	BMC
		#1A	Processor 4 Temperature Sensor	BMC
		#1B	Memory Module 1 Temperature Sensor	BMC
		#1C	Memory Module 2 Temperature Sensor	BMC
Voltage	02			
		#01	I/O Baseboard +3.3V	BMC
		#02	I/O Baseboard +12V	BMC
		#03	I/O Baseboard +5V	BMC
		#04	VCC _ Stand by	BMC
		#05	I/O Baseboard -12V	BMC
		#06	I/O Baseboard -5V	BMC
		#07	I/O Baseboard SC_VREF1 (SCSI Term. 1)	BMC

Sensor Type		Sensor Number	Sensor Name	Generator ID
Verbose	**Hex**			
		#08	I/O Baseboard SC_VREF2 (SCSI Term. 2)	BMC
		#09	I/O Baseboard SC_VREF3 (SCSI Term. 2)	BMC
		#0B	VccP1	BMC
		#0C	VccP2	BMC
		#0D	VccP3	BMC
		#0E	VccP4	BMC
		#0F	VTT (Processor +1.5V)	BMC
		#10	Processor +2.5 V	BMC
		#11	Processor +3.3V	BMC
		#12	Processor +5V	BMC
		#13	Vcc_L2_1 (For Processors 1 & 2)	BMC
		#14	Vcc_L2_1 (For Processors 3 & 4)	BMC
		#15	Processor +12	BMC
		#21	Slot 1 VID	BMC
		#22	Slot 2 VID	BMC
		#23	Slot 3 VID	BMC
		#24	Slot 4 VID	BMC
		#25	L2 1 VID	BMC
		#26	L2 2 VID	BMC
		#27	L2 3 VID	BMC
		#28	L2 4 VID	BMC
Fan	**04**			
		#0E	Fan 1 speed	HSC1, HSC2
		#0F	Fan 2 speed	HSC1, HSC2
		#10	Fan 3 speed	HSC1, HSC2
		#11	Fan 4 speed	HSC1
		#12	Fan 5 speed	HSC1
		#13	Fan 6 speed	HSC1
Physical Security (Chassis Intrusion)	**05**			
		#03	Chassis Intrusion	FP
		#04	Cover Open	FP

Sensor Type		Sensor Number	Sensor Name	Generator ID
Verbose	**Hex**			
Secure Mode Violation Attempt	**06**			
		#01	Power Button Secure Mode Violation	FP
		#02	Reset Button Secure mode Violation	FP
Processor	**07**			**BMC**
		#1D	Processor 1 Status	BMC
		#1E	Processor 2 Status	BMC
		#1F	Processor 3 Status	BMC
		#20	Processor 4 Status	BMC
Power Supply	**08**			**FP**
		#06	Power Supply 1	FP
		#07	Power Supply 2	FP
		#08	Power Supply 3	FP
		#09	Power Supply 4	FP
Power Unit	**09**			**FP**
		#05	Power Unit Status	FP
Memory	**0C**			
		#29	DIMM 1 Presence Memory Module 1	BMC
		#2A	DIMM 2 Presence Memory Module 1	BMC
		#2B	DIMM 3 Presence Memory Module 1	BMC
		#2C	DIMM 4 Presence Memory Module 1	BMC
		#2D	DIMM 5 Presence Memory Module 1	BMC
		#2E	DIMM 6 Presence Memory Module 1	BMC
		#2F	DIMM 7 Presence Memory Module 1	BMC
		#30	DIMM 8 Presence Memory Module 1	BMC
		#31	DIMM 9 Presence Memory Module 1	BMC
		#32	DIMM 10 Presence Memory Module 1	BMC
		#33	DIMM 11 Presence Memory Module 1	BMC
		#34	DIMM 12 Presence Memory Module 1	BMC
		#35	DIMM 13 Presence Memory Module 1	BMC
		#36	DIMM 14 Presence Memory Module 1	BMC
		#37	DIMM 15 Presence Memory Module 1	BMC
		#38	DIMM 16 Presence Memory Module 1	BMC
		#39	DIMM 1 Presence Memory Module 2	BMC
		#3A	DIMM 2 Presence Memory Module 2	BMC
		#3B	DIMM 3 Presence Memory Module 2	BMC

Sensor Type		Sensor Number	Sensor Name	Generator ID
Verbose	**Hex**			
		#3C	DIMM 4 Presence Memory Module 2	BMC
		#3D	DIMM 5 Presence Memory Module 2	BMC
		#3E	DIMM 6 Presence Memory Module 2	BMC
		#3F	DIMM 7 Presence Memory Module 2	BMC
		#40	DIMM 8 Presence Memory Module 2	BMC
		#41	DIMM 9 Presence Memory Module 2	BMC
		#42	DIMM 10 Presence Memory Module 2	BMC
		#43	DIMM 11 Presence Memory Module 2	BMC
		#44	DIMM 12 Presence Memory Module 2	BMC
		#45	DIMM 13 Presence Memory Module 2	BMC
		#46	DIMM 14 Presence Memory Module 2	BMC
		#47	DIMM 15 Presence Memory Module 2	BMC
		#48	DIMM 16 Presence Memory Module 2	BMC
Drive Slot (Bay)	**0D**			
		#02	Drive Slot 0 Status	HSC1, HSC2
		#03	Drive Slot 1 Status	HSC1, HSC2
		#04	Drive Slot 2 Status	HSC1, HSC2
		#05	Drive Slot 3 Status	HSC1, HSC2
		#06	Drive Slot 4 Status	HSC1, HSC2
		#07	Drive Slot 5 Status	HSC1, HSC2
		#08	Drive Slot 0 Presence	HSC1, HSC2
		#09	Drive Slot 1 Presence	HSC1, HSC2
		#0A	Drive Slot 2 Presence	HSC1, HSC2
		#0B	Drive Slot 3 Presence	HSC1, HSC2
		#0C	Drive Slot 4 Presence	HSC1, HSC2
		#0D	Drive Slot 5 Presence	HSC1, HSC2
POST Error	**0F**			
		#4B	See POST table	
Watchdog	**11**			
		#49	BMC Watchdog	BMC
System Event	**12**			
		#EF	See BIOS table	

Sensor Type		Sensor Number	Sensor Name	Generator ID
Verbose	**Hex**			
Critical Interrupt	**13**			
		#4A	Front Panel Interrupt	BMC
Cable / Interconnect	**1B**			
		#0A	F16 cable 1	FP
		#0B	F16 cable 2	FP
		#0C	Power Supply 4 Cable	FP

3. BIOS Error Messages

The BIOS is responsible for monitoring and logging certain System Events, Memory Errors and Critical Interrupts. The BIOS sends an event request message to BMC to log the event. Some errors such as the processor failure are logged during early POST.

3.1 Using The System Event Log for BIOS Event Messages

This section uses an example SEL entry to explain the use of the SEL Viewer with a BIOS Event Message. To fully interpret a BIOS Event Message, both verbose and hexadecimal views may need to be used. In this example, the verbose view is used and the differences between the verbose view and hexadecimal view are noted where necessary.

The example on the following page uses Rec. ID 0x8005 (the first line of data) in Figure 3-1. This Event Message has been reported by the BIOS and indicates the system has been booted. This was determined as follows:

1. In the diagram below, the Sensor Type and Number is indicated as System Event #EF in Verbose mode.

   Note in Table 3-1 that two events are labeled as System Event #EF. In this case, it is possible to identify the record using the information in the Event Description in the verbose view. However, in the event that it is difficult to identify the Event in Verbose mode, viewing the data in Hex mode will provide an Event Description of E7 01 FF FF. This data corresponds directly to unique identifying information in the table.

2. The Generator ID in both the diagram and in the table indicates the BIOS generated the Event Message.

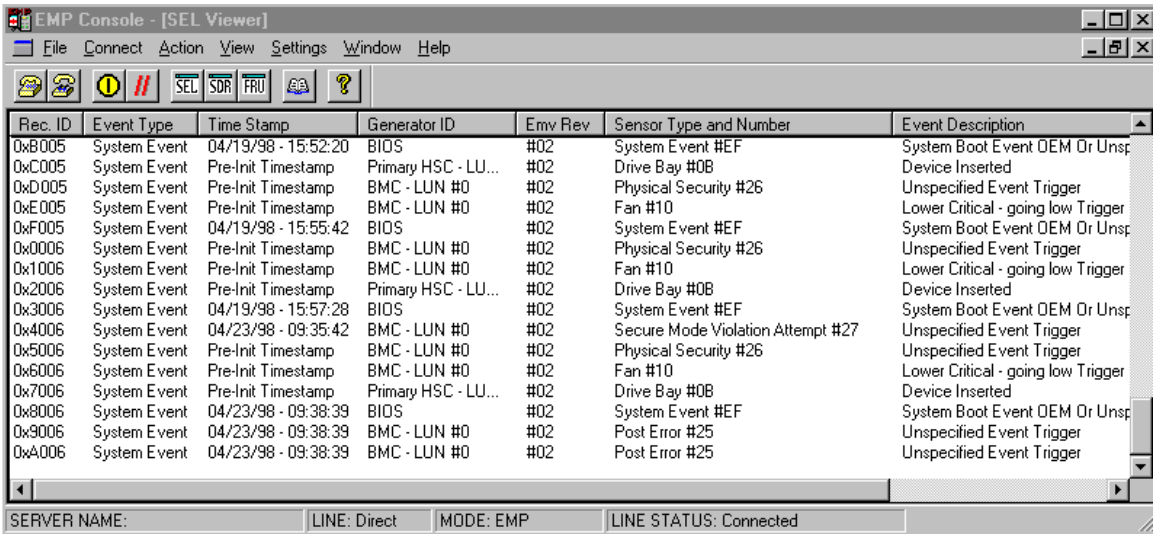

Figure 3-1 : BIOS (and Sensor) Events

Table 3-1: BIOS System Event Log Table

Sensor Type and Number		Event Description in hex	Event Type
Verbose	**Hex**		
Memory #EF	0C EF	E7 20 slot# DIMM#[1]	single bit memory error
Memory #EF	0C EF	E7 21 slot# DIMM#[1]	multi bit memory error
Memory #EF	0C EF	E7 22 slot# DIMM#[1]	memory parity error
System Event #EF	12 EF	E7 00 FF FF	System Reconfiguration
System Event #EF	12 EF	E7 01 FF FF	System Boot
Critical Interrupt #EF	13 28	E7 00 FF FF	Front Panel NMI
Critical Interrupt #EF	13 28	E7 01 FF FF	bus time-out
Critical Interrupt #EF	13 28	E7 02 FF FF	I/O check
Critical Interrupt #EF	13 28	E7 03 FF FF	Software NMI
Critical Interrupt #EF	13 28	E7 04 FF FF	NMI PERR
Critical Interrupt #EF	13 28	E7 05 FF FF	NMI SERR
Critical Interrupt #EF	13 28	E7 44 00 14	BINIT Expander Parity
Critical Interrupt #EF	13 28	E7 44 00 24	PCI PERR
Critical Interrupt #EF	13 28	E7 44 00 26	PCI DATA Parity Error
Critical Interrupt #EF	13 28	E7 44 FF 10	AERR Address Parity Error
Critical Interrupt #EF	13 28	E7 44 FF 15	BINIT Response Parity
Critical Interrupt #EF	13 28	E7 44 FF 16	BINIT Request parity
Critical Interrupt #EF	13 28	E7 45 00 13	BINIT Protocol Violation
Critical Interrupt #EF	13 28	E7 45 00 18	SERR Protocol Violation
Critical Interrupt #EF	13 28	E7 45 00 19	SERR Parity on Transmit
Critical Interrupt #EF	13 28	E7 45 00 20	SERR Parity on Receive
Critical Interrupt #EF	13 28	E7 45 00 21	SERR Parity on address
Critical Interrupt #EF	13 28	E7 45 00 22	SERR Inbound Timeout

Sensor Type and Number		Event Description in hex	Event Type
Verbose	Hex		
Critical Interrupt #EF	13 28	E7 45 00 23	SERR BUS parity
Critical Interrupt #EF	13 28	E7 45 00 25	PCI SERR
Critical Interrupt #EF	13 28	E7 45 FF 11	BERR HOST BUS generic
Critical Interrupt #EF	13 28	E7 45 FF 12	BINIT Hostbus Hardfail
Critical Interrupt #EF	13 28	E7 48 00 00	BINIT Hostbus ECC
Critical Interrupt #EF	13 29	E8 60 00 FF	IMB Command Error

Note 1: The slot# and DIMM# are included for memory events

4. POST Event Messages

BIOS events that are generated in the pre boot period, such as clearing CMOS, are logged during early stage POST as Sensor Type “0F --“ (in hexadecimal view) under the Sensor Type and Number column. The “--“ here indicates the Sensor Number. This value will change, depending upon the nature of the Event Message.

4.1 Using the System Event Log for POST Event Messages

This section uses an example SEL entry to explain the use of the SEL Viewer with a POST Event Message. To fully interpret a POST Event Message, both verbose and hexadecimal views may need to be used. In this example, the hexadecimal view is used.

The example on the following page uses Rec. ID a006 (the second line of data) in Figure 4-1. This Event Message has been reported by the POST and indicates “NVRAM Data Invalid, NVRAM cleared.” This was determined as follows:

1. To use this table, view the SEL Viewer entries in hex mode. The Sensor Type and Number column indicates a Sensor Type 0F. All POST Event Messages use this Sensor Type.

2. As indicated by “-- --“in Table 4-1, the first two bytes of the four-byte Event Description are not used.

3. The third and fourth bytes of the Event Description are 52 and 81.

4. The Error Message column indicates the cause of error that caused the entry in the SEL.

5. The Pause on Error column indicates how the BIOS will respond to this event.

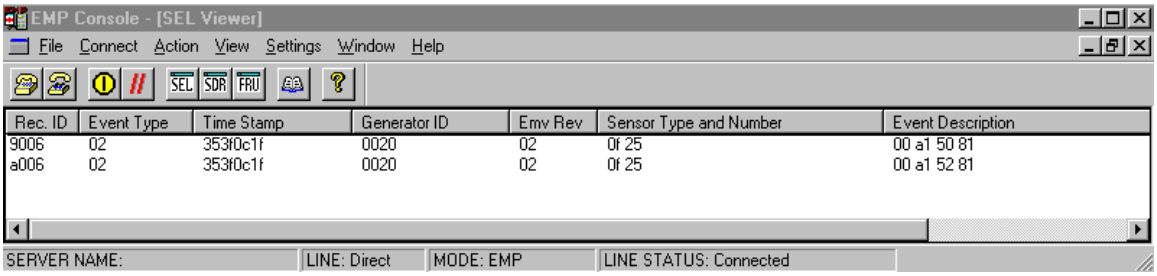

Figure 4-1: POST Events

Table 4-1. POST Code System Event Log Table

Code	Error Message
-- -- 00 08	PCI I/O Port Conflict
-- -- 00 09	NVRAM Checksum Error, NVRAM Cleared
-- -- 00 81	Processor 0 failed BIST
-- -- 00 82	Baseboard Management Controller failed to function
-- -- 01 08	PCI Memory Conflict
-- -- 01 81	Processor 1 failed BIST
-- -- 01 82	Front Panel Controller failed to function
-- -- 02 00	Primary Boot Device Not Found
-- -- 02 08	PCI IRQ Conflict
-- -- 02 81	Processor 2 failed BIST
-- -- 03 09	NVRAM Data Invalid, NVRAM Cleared
-- -- 03 81	Processor 3 failed BIST
-- -- 03 82	Primary Hot-swap Controller failed to function
-- -- 04 08	PCI ROM not found, May Be OK For This Card:
-- -- 04 81	Processor 0 Internal error (IERR)
-- -- 04 82	Secondary Hot-swap Controller failed to function
-- -- 05 08	Insufficient Memory to Shadow PCI ROM:
-- -- 05 81	Processor 1 Internal error (IERR)
-- -- 06 08	Memory Allocation Failure for Second PCI Segment
-- -- 06 81	Processor 0 Thermal Trip error
-- -- 07 81	Processor 1 Thermal Trip error
-- -- 08 81	Watchdog timer failed on last boot
-- -- 0B 81	Processor 0 failed initialization
-- -- 0C 81	Processor 0 disabled
-- -- 0D 81	Processor 1 disabled

Code	Error Message
-- -- 0E 81	Processor 0 failed FRB-3 timer
-- -- 0F 81	Processor 1 failed FRB-3 timer
-- -- 10 00	Cache Memory Failure, Do Not Enable Cache
-- -- 10 05	PCI Parity Error
-- -- 10 07	System Board Device Resource Conflict
-- -- 10 08	Floppy Disk Controller Resource Conflict
-- -- 10 81	Server Management Interface failed to function
-- -- 11 07	Static Device Resource Conflict
-- -- 11 08	Primary IDE Controller Resource Conflict
-- -- 12 08	Secondary IDE Controller Resource Conflict
-- -- 15 00	Primary Output Device Not Found
-- -- 15 08	Parallel Port Resource Conflict
-- -- 16 00	Primary Input Device Not Found
-- -- 16 08	Serial Port 1 Resource Conflict
-- -- 17 08	Serial Port 2 Resource Conflict
-- -- 20 08	Expansion Board Disabled in Slot
-- -- 28 81	Processor 2 Internal error (IERR)
-- -- 29 81	Processor 3 Internal error (IERR)
-- -- 30 04	Timer Channel 2 Failure
-- -- 30 81	Processor 2 Thermal Trip error
-- -- 31 01	Floppy Drive A:
-- -- 31 81	Processor 3 Thermal Trip error
-- -- 32 01	Floppy Drive B:
-- -- 35 01	Floppy Disk Controller Failure
-- -- 38 81	Processor 2 failed FRB-3 timer
-- -- 39 81	Processor 3 failed FRB-3 timer
-- -- 40 01	Shadow Of System BIOS Failed
-- -- 40 04	Gate-A20 Failure
-- -- 40 81	Processor 2 disabled
-- -- 41 04	Unexpected Interrupt in Protected Mode
-- -- 41 81	Processor 3 disabled
-- -- 42 00	ISA Config contains invalid info
-- -- 45 04	Master Interrupt Controller Error
-- -- 46 04	Slave Interrupt Controller Error
-- -- 48 81	Processor 1 failed initialization
-- -- 49 81	Processor 2 failed initialization
-- -- 4A 81	Processor 3 failed initialization
-- -- 50 00	PnP Memory Conflict:
-- -- 50 04	Master DMA Controller Error
-- -- 50 81	NVRAM Cleared by Jumper

Code	Error Message
-- -- 51 00	PnP 32-bit Memory Conflict:
-- -- 51 04	Slave DMA Controller Error
-- -- 52 00	PnP IRQ Conflict:
-- -- 52 04	DMA Controller Error
-- -- 52 81	ESCD Data Cleared
-- -- 53 00	PnP DMA Conflict:
-- -- 53 81	Password Cleared by Jumper
-- -- 54 00	PnP Error Log Is Full
-- -- 55 00	Bad PnP Serial ID Checksum:
-- -- 56 00	Bad PnP Resource Data Checksum:
-- -- 60 00	Keyboard Is Locked ... Please Unlock It
-- -- 60 04	Fail-safe Timer NMI Failure
-- -- 60 81	Unable to apply BIOS update for Processor 1
-- -- 61 04	Software Port NMI Failure
-- -- 61 81	Unable to apply BIOS update for Processor 2
-- -- 62 81	Unable to apply BIOS update for Processor 3
-- -- 63 81	Unable to apply BIOS update for Processor 4
-- -- 65 04	Bus Timeout NMI in Slot
-- -- 67 04	Expansion Board NMI in Slot
-- -- 68 81	Processor 1 L2 cache failed
-- -- 69 81	Processor 2 L2 cache failed
-- -- 6A 81	Processor 3 L2 cache failed
-- -- 6B 81	Processor 4 L2 cache failed
-- -- 70 00	CMOS Time & Date Not Set
-- -- 70 01	Disabled CPU slot #
-- -- 70 03	Keyboard Controller Error
-- -- 70 81	BIOS does not support current stepping for Processor 1
-- -- 71 01	CPU Failure – CPU # 1
-- -- 71 81	BIOS does not support current stepping for Processor 2
-- -- 72 01	CPU Failure – CPU # 2
-- -- 72 81	BIOS does not support current stepping for Processor 3
-- -- 73 01	CPU Failure – CPU # 3
-- -- 73 03	Keyboard Stuck Key Detected
-- -- 73 81	BIOS does not support current stepping for Processor 4
-- -- 74 01	CPU Failure – CPU # 4
-- -- 75 01	CPU modules are incompatible or one is not present.
-- -- 75 03	Keyboard and Mouse Swapped
-- -- 76 01	Previous CPU Failure – CPU # 1
-- -- 77 01	Previous CPU Failure – CPU # 2
-- -- 78 01	Previous CPU Failure – CPU # 3

Code	Error Message
-- -- 79 01	Previous CPU Failure – CPU # 4
-- -- 80 00	Option ROM has bad checksum
-- -- 80 01	Attempting to boot with failed CPU
-- -- 80 07	PCI Segment 1 memory request exceeds 998 MB
-- -- 80 81	PXB1 failed to respond
-- -- 81 01	BSP switched, system may be in uniprocessor mode
-- -- 81 07	PCI Segment 1 I/O requests exceeds 12KB
-- -- 81 81	Mismatch Among Processors Detected
-- -- 82 07	PCI I/O request exceeds amount available
-- -- 82 09	I/O Expansion Board NMI in Slot
-- -- 82 81	L2 cache size mismatch
-- -- 83 00	Shadow Of PCI ROM Failed
-- -- 83 07	PCI memory request exceeds amount available
-- -- 84 07	Illegal bus for memory request below 1 MB
-- -- 84 09	Expansion Board Disabled in Slot
-- -- 85 00	Shadow Of ISA ROM Failed
-- -- 85 07	Memory request below 1 MB exceeds 1 MB
-- -- 85 09	Fail-safe Timer NMI
-- -- 86 09	System Reset caused by Watchdog Timer
-- -- 87 09	Bus Timeout NMI in Slot
-- -- 89 02	System Memory Size Mismatch
-- -- 91 01	CMOS Battery Failed
-- -- 95 01	CMOS System Options Not Set
-- -- 95 02	Address Line Short Detected
-- -- 97 02	Base Or Extended Memory Error: Board #, DIMM #
-- -- 98 01	CMOS Checksum Invalid
-- -- 99 02	ECC Error Correction Failure