A450NX MP Server Board Set

Specification Update

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The A450NX Server Board Set may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Such errata are not covered by Intel's warranty. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications before placing your product order.

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Revision History

Date of Revision	Version	Description
August, 1998	-000	This document is the first Specification Update for the *Intel*[®] *A450NX MP Server Board Set Technical Product Specification.*
September, 1998	-001	Added Errata 15 and updated Tables 1 and 8.
February, 1999	-002	Updated Tables 1 – 5, 8; Errata
March, 1999	-003	Updated Table 1; Errata
April, 1999	-004	Updated Table 1, 2, 3, Errata and BIOS POST codes
May, 1999	-005	Updated Table 3, Errata and Specification Changes
October, 1999	-006	Updated Table 3 and added Cascades jumper settings to Table 10
March, 2000	-007	Updated Table 3
April, 2000	-008	Updated Table 1 and Errata 19, and 20
June, 2000	-009	Updated Errata 21 and 22
July, 2000	-010	Updated Table 4

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Preface

This document is an update to the specifications contained in the *A450NX MP Server Board Set Technical Product Specification*. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It contains Specification Changes, Specification Clarifications, and Documentation Changes.

This document does not cover errata related to the AD450NX Server System. Refer to the *AD450NX Server System Specification Update* and the errata document for specification updates concerning the AD450NX Server System.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated into the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact on a complex design situation. These clarifications will be incorporated into the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated into the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the behavior of the A450NX MP Server Board Set to deviate from published specifications. Hardware and software designed to be used with any given printed board assembly (PBA) and firmware revision level must assume that all errata documented for that PBA and firmware revision level are present.

General Information

For a complete revision history of system and board set level components, refer to the most recent Monthly Conversion Summary document for the A450NX and AD450NX product. Basic A450NX MP Server Board Set Identification information is shown in the Table 1.

Table 1 - Basic A450NX MP Server Board Set Identification Information

Component (Module) Description	Base PBA Number	PBA Revision Number	Fab Rev	Released BIOS/SSU/ firmware Revision	Suggested BIOS/SSU/ firmware Revision	Notes (See below)
CPU Baseboard	663008	402	4.0			
(4-slot)		501	4.1			
		601	4.2			
		801	8.0			
		802	8.01			
CPU Baseboard	703631	104	1.3			
(5-Slot)		201	2.0			
		301	2.1			
		501	5.0			
		502	5.01			
I/O Baseboard	662379	402	3.2	BIOS PR4, SDR38	BIOS PR4, SDR38 or 40	1
		403	3.2	BIOS PR4, SDR38	BIOS PR4, SDR38 or 40	2
		404	3.2	BIOS PR4, SDR38	BIOS PR4, SDR38 or 40	2
		405	3.2	BIOS PR5, SDR40, SMIC85, BMC22	BIOS PR5, SDR40, SMIC85, BMC22	2
		407	3.2	BIOS PR7, SDR40, SMIC85, BMC23	BIOS PR7, SDR40, SMIC85, BMC23	2
		501	3.4	BIOS PR9, SDR 42, SMIC 86, BMC 25	BIOS PR10, SDR 42, SMIC 86, BMC 25	2
		502	3.5	BIOS PR13, SDR 42, SMIC86, BMC 26	BIOS PR13, SDR 42, SMIC 86, BMC 26	2
		503	3.5	BIOS PR13, SDR 42, SMIC86, BMC 26	BIOS PR13, SDR 42, SMIC 86, BMC 26	2
Memory Module	667829	304	3.0			
		401	3.0			
Memory Termination Module	665573	001	1.1			
FSB (Front-side Bus) Termination Module	665394	302	2.2			
I/O Riser Card	679267	102	2.1			
		201	2.0			
Interconnect (AIC) Backplane	665049	201	3.0			
		202	3.0			

Notes: 1. B0 stepping of the PXB. Recommend not using IDE connectors.

2. B1 stepping of the PXB (as available). Using IDE connectors is fine.

The Enterprise Server Group (ESG) supports the Performance Microprocessor Division's (PMD) position on mixed steppings in MP systems, however please note that you can not mix processors with cache steppings requiring different voltages in the same system. The AD450NX system architecture implements one VRM to supply the same voltage to the cache core of two processors.

The following Table 2 indicates which stepping of the Pentium® II Xeon™ processor can be mixed within the same system. Table 3 indicates which stepping of the Pentium® III Xeon™ processor can be mixed within the same system. An "X" denotes which stepping can be mixed and a blank indicates the A450NX MP Server Board Set does not support the given BIOS/stepping combination. NS indicates that processors with that S-Spec number are not supported in the AD450NX System.

Table 2 - Supported Pentium® II Xeon™ Processor / BIOS Combinations

PROCESSOR STEPPING	B0	B0	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1
FREQUENCY	400MHz	400MHz	400MHz	400MHz	400MHz	400MHz	450MHz	450MHz	450MHz	450MHz	450MHz	450MHz	450MHz	450MHz
CACHE SIZE	512K	1M	512K	512K	1M	1M	512K	512K	512K	512K	1M	1M	2M	2M
STEPPING ID	0652h	0652h	0653h	0653h	0653h	0653h	0653 h	0653 h	0653 h	0653 h	0653 h	0653 h	0653 h	0653 h
S-SPEC	SL344	SL345	SL34H	SL35N	SL34J	SL35P	SL2XJ	SL33T	SL354	SL36W	SL2XK	SL33U	SL2XL	SL33V
SL344	x													
SL345		x												
SI34H			x	x										
SL35N			x	x										
SL34J					x	x								
SL35P					x	x								
SL2XJ							x			x				
SL33T														
SL354														
SL36W							x			x				
SL2XK											x	x		
SL33U											x	x		
SL2XL													x	x
SL33V													x	x
BIOS														
PRODUCTION RELEASE 8	x	x	x	x	x	x	x	NS	NS	x	x	x	x	x

Table 3 - Supported Pentium® III Xeon™ Processor / BIOS Combinations

PROCESSOR STEPPING	B0	B0	B0	B0	B0	B0	C0	C0	C0	C0	C0	C0
FREQUENCY	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	550MHz	550MHz	550MHz
CACHE SIZE	512K	512K	1M	1M	2M	2M	512K	1M	2M	512K	1M	2M
STEPPING ID	0672 H	0672 H	0672 H	0672 H	0672 H	0672 H	0673 H	0673 H	0673 H	0673 H	0673 H	0673 H
S-SPEC	SL2XU	SL3C9	SL2XV	SL3CA	SL2XW	SL3CB	SL385	SL386	SL387	SL3LM	SL3LN	SL3LP
SL2XU	x	x					x					
SL3C9	x	x					x					
SL2XV			x	x				x				
SL3CA			x	x				x				
SL2XW					x	x			x			
SL3CB					x	x			x			
SL385	x	x					x					
SL386			x	x				x				
SL387					x	x			x			
SL3LM										x		
SL3LN											x	
SL3LP												x
BIOS												
PRODUCTION RELEASE 13	x	x	x	x	x	x	x	x	x	x	x	x

Table 4 - Supported Pentium® III Xeon™ Cascade Processor / BIOS Combinations / 4-5 Slots

PROCESSOR STEPPING	A0	A0	A0'	A0'								
FREQUENCY	700MHz	700MHz	700MHz	700MHz								
CACHE SIZE	1M	2M	1M	2M								
STEPPING ID	6A0H	6A0H	6A0H	6A0H								
S-SPEC	SL3U4	SL3WZ	SL4GD	SL4GF								
SL3U4	X											
SL3WZ		X										
SL4GD			X									
SL4GF				X								
BIOS												
ASPEN 4-SLOT			X	X								
ASPEN 5-SLOT	X	X	X	X								
PRODUCTION RELEASE 16	X	X	X	X								

Table 5 - Intel® 450NX PCIset components (all 100 MHz)

TYPE	STEPPING	S-SPEC
82451 (MIOC)	B1	SL2RV
82452 (RCG)	B0	SL2RW
82453 (MUX)	B0	SL2RX
82454 (PXB)	B1	SL2ZA
82454 (PXB)	B0	SL2RU
82454 (PXB)	C0	SL36R

Summary Table of Changes

The following table indicates the Specification Changes, Specification Clarifications, or Documentation Changes that apply to the A450NX MP Server Board Set. Intel intends to fix some of the errata in the future, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLES

Doc:	Document change or update that will be implemented.
Fix:	Intel intends to fix this erratum in a future revision of the hardware or software associated with the A450NX MP Server System. (Fix in future release)
Fixed:	This erratum has been fixed.
NoFix:	There are no plans to fix this erratum. (Will not fix)
Shaded:	This erratum is either new or modified from the previous version of the document.

Table 6 - A450NX Server Board Set Errata

NO.	PLANS	ERRATA
1	Fixed	Clearing CMOS may cause system time/date to reset
2	Fixed	Berg FutureBus* insertion force exceeds specification
3	Fixed	IRQs remain unchanged after CMOS cleared and "Reset Data Configuration" selected
4	Fix	Error may occur when changing boot drive from SCSI to IDE
5	No Fix	UDMA enabled in the BIOS SETUP does not work for DOS
6	Fixed	Drive parameters not correctly auto detected for a CDROM
7	Fixed	SDR record has incorrect Slot 1-4 and L2 1-4 VID voltage formulas
8	No Fix	Events are not routed to the event message buffer unless event message SMI is enabled
9	Fixed	BMC firmware race condition occurs after a processor thermal trip error, causing two processors to be disabled, instead of just the thermal tripped processor.
10	Fix	BMC20 - Get SEL command "partial get" functionality does not work
11	Fix	BMC20 - Get SEL Entry (storage 43h) reads last record on invalid record ID
12	Fixed	OEM VESA string for the onboard Cirrus GD5446* video chip set is incorrectly set to "STBNITRO 64V"
13	Fixed	4-Slot CPU baseboard caps (fuses) bend upon insertion of the top memory board
14	Fixed	The 420-W power supply regulation specified for -12 V is too wide for PCI slots under a heavy load
15	Fixed	Processor temperature readings may not be reported correctly
16	Fixed	PCI Restreaming buffer not supported on C0 stepping of PXB
17	Fixed	CORFE I2O adapter card does not initialize
18	No Fix	BIOS successful boot event message not reported
19	No Fix	The APIC clock on AD450NX CPU board is undershoot
20	No Fix	Red Hat Linux 6.1 fail to boot on AD450NX with Cascade 650Mhz Processor
21	No Fix	Recovery boot always required memory populated in bank 0
22	Fixed	Design Spec Violation when VRM is not installed on the A450NX CPU board.

Table 7 indicates the hardware or software revisions in which each erratum was fixed when applicable.

CODES USED IN FOLLOWING TABLE

Doc:	Document change or update that will be implemented.
Fix:	Intel intends to fix this erratum in a future revision of the hardware or software associated with the A450NX MP Server Board Set. (Fix in future release)
Fixed:	This erratum has been fixed.
NoFix:	There are no plans to fix this erratum. Will not fix
Shaded:	This erratum is either new or modified from the previous version of the document.

Table 7- Fixed In

NO.	PLANS	CPU Baseboard (4 slot)	CPU Baseboard (5 slot)	I/O Baseboard	Memory Module	Memory Termination Module	FSB Termination Module	I/O Riser Card	Interconnect Backplane	Others
1	Fixed									BIOS PR6
2	Fixed	663008-601	703631-301	662379-501					664893-204	
3	Fixed									BIOS PR6
4	Fix									
5	No Fix									
6	Fixed									BIOS PR6
7	Fixed									SDR41
8	No Fix									
9	Fixed									BMC23
10	Fix									
11	Fix									
12	Fixed									BIOS PR7
13	Fixed		703631-201							
14	Fixed									500W P/S
15	Fixed	663008-601	703631-301							
16	Fixed									BIOS PR9
17	Fixed									BIOS PR11
18	No Fix									
19	No Fix									
20	No Fix									
21	No Fix									
22	Fixed	-601	-301							

Errata

1. Clearing CMOS may cause system time/date to reset

DESCRIPTION: When clearing CMOS with the jumper, the systems clock time defaults back to 12:00 on 02/02/1996.

IMPLICATIONS: An error message at boot time is generated alerting the user of the change in the system time/date. This message appears until the system time/date has been reset.

WORKAROUND: Enter Setup mode and reset the system date/time.

STATUS: Fixed in BIOS PR6

2. Berg FutureBus* insertion force exceeds specification

DESCRIPTION: The custom mono-block connectors used on the A450NX board set exceed the manufacturer's specification for insertion force. The press-block portion is improperly sized, and there is a 1-degree tilt of the contacts within the header portion (I/O and CPU baseboards).

IMPLICATIONS: This problem will result in an increased force required to seat the FutureBus connectors of both the CPU and I/O baseboard to the mating connector on the A450NX Interconnect (AIC) Backplane. System designs that simultaneously engage both the CPU and I/O baseboards with the AIC backplane, such as the AD450NX Server System will be more significantly impacted then other designs that engage the boards individually

WORKAROUND: The CPU and I/O baseboards will be manufactured with a discrete-block power receptacle as an alternate to the custom mono-block part. That discrete-block part will be used until the manufacturer to be within specification changes the mono-block (preferred for manufacturing) part.

STATUS: FIXED

3. IRQs remain unchanged after CMOS cleared and "Reset Data Configuration" selected

DESCRIPTION: When CMOS is cleared and "Reset Data Configuration" has been selected and executed, the IRQs for adapter cards in the system may not change from the value that was set prior to the CMOS clear.

IMPLICATIONS: This has been observed on IRQs that were set using the System Setup Utility (SSU).

WORKAROUND: Use the SSU to reset the IRQs as desired after the CMOS clear action.

STATUS: Fixed in BIOS Production Release 6 (PR6)

4. Error may occur when changing boot drive from SCSI to IDE

DESCRIPTION: Under certain conditions when changing the boot drive from SCSI to an IDE drive, an error may be reported. The error which has been observed as a result is 'Expansion ROM not initialized--PCI mass storage controller.'

IMPLICATIONS: This may result in some or all drives not being recognized at bootup.

WORKAROUND: Remove IDE drives from the IDE buses, reboot, shut down the system, then reconnect the IDE drives and reboot again. A message stating "configuration has been updated" may be displayed.

If this does not trigger recovery from the error, the CMOS may need to be cleared.

STATUS: Fix in future release

5. UDMA enabled in the BIOS SETUP does not work for DOS

DESCRIPTION: When UDMA transfer mode for a IDE hard drives is enabled by the Setup (User mode) in BIOS, the INT13 function does not utilize DMA mode. It continues to work in standard mode. DOS utilizes INT13 BIOS calls, and will not show any UDMA related performance difference.

IMPLICATIONS: UDMA enabled in the BIOS SETUP does not work for DOS.

WORKAROUND: None identified. However, with the settings correctly set for UDMA on WindowsNT/95 using with UDMA capable drivers should work.

STATUS: Will Not Fix

6. Drive parameters not correctly auto detected for a CDROM

DESCRIPTION: A problem was found with the BIOS, which fails to update the drive parameters when a CDROM replaces a previously connected hard disk. This problem will only occur if a user removes an installed IDE hard drive and then adds a IDE CD-ROM. BIOS will fail to update the drive parameters correctly for the new CD-ROM. Instead, the IDE drive parameters will still be present when the parameters should have been Auto Detected for the CD-ROM.

IMPLICATIONS: The CD-ROM continues to show parameters of the previous hard disk.

WORKAROUND: Go to Setup, use F9 in setup to load the defaults. This will correct the parameters for the CDROM.

Or, once the user has disconnected the hard disk, go through the POST to boot at least once without connecting any hard drive. Next, connect the CDROM. The setup now will have the correct CDROM parameters.

STATUS: Fixed in BIOS Production Release 6 (PR6)

7. SDR record has incorrect Slot 1-4 and L2 1-4 VID voltage formulas

DESCRIPTION: The Slot 1 through 4 and L2 1-4 VID (Voltage Identification) shows incorrect sensors (0x21 - 0x28). In the SDR (Sensor Data Record), the 'M' value should be 0x19 and the 'R exp/B exp' should be 0xA0.

IMPLICATIONS: This problem was discovered by evaluation of the values in the SDR (Sensor Data Records) file. The values referred to be constants used in a formula to deliver an informational value. The desired behavior is that the SDR values used will produce correct informational voltage readings. The wrong constant values in the SDR would result in an incorrect calculation. Note that the actual voltage supplied to the processor is determined through the processor and VRM (voltage regulator module) hardware. This is independent of the server management software numbers displayed to the user.

WORKAROUND: None identified

STATUS: Fixed in Sensory Data Record v.41 (SDR41)

8. Events are not routed to the event message buffer unless event message SMI is enabled

DESCRIPTION: Routing an event to the event message buffer requires SMI (Server Management Interrupt) to be enabled. This should be independent of SMI being enabled.

An example of an event message is when the temperature in the system crosses a threshold, and the temperature sensor needs to send a message that the threshold has been crossed. The over temperature event message will be stored into the System Event Log (SEL), however the over temperature event message also needs to be passed to the event message buffer (also referred to as the SMS buffer). It is passed to the SMS buffer so that server management software, like LANDesk® Server Manager can be notified of the event and alert the user. If event message SMIs are not enabled, the event will not be sent to the SMS buffer, and thus server management software will not be notified of the event.

IMPLICATIONS: This erratum does not have a significant impact on the product functionality or current applications that work with the firmware.

WORKAROUND: None identified

STATUS: Will Not Fix

9. BMC firmware race condition occurs after a processor thermal trip error, causing two processors to be disabled, instead of just the thermal tripped processor

DESCRIPTION: An erratum was found in the BMC (baseboard management controller) firmware that caused a race condition involving two tasks. The anomaly will manifest itself in a four-processor configuration when a thermal trip error occurs. The desired behavior is that upon next boot the bad processor would be disabled and the system would boot with the remaining three processors.

Observed behavior is that upon next boot the system hangs for 6 minutes and then boots with two processors disabled and two processors enabled.

The problem happens when a processor's internal core temperature has exceeded 170°C.

IMPLICATIONS: First, if server management software were up, alerts would have been sent as the processor temperature went through noncritical and critical thresholds – to provide a warning to the user. Second, the

problem is seen only in system failure mode (failed processor), not in normal operating mode. Third, under the failed processor, the system should recover in a degraded mode, which it does. However, the mode is somewhat more degraded, a 6-minute wait and two disabled processors instead of one disabled processor. Fourth, the system is in need of repair due to the thermal trip.

WORKAROUND: If processor thermal trip failure occurs, subsequent reboot, resetting or power-cycling the system within the 6-minute will cause the next boot to correctly come up with three processors enabled. In a system with four processors, and if the user allows the system to hang for the full six to seven minutes, the system will reset and boot with two processors disabled. BIOS will display messages indicating which two processors will display a message indicating which were disabled. BIOS will also display a message indicating which processor reported an internal thermal trip condition. Otherwise, the user can go into the BIOS Setup server management screen and request "Processor Retest" to enable the disabled processor(s) and clear the thermal trip history.

STATUS: Fixed in BMC23

10. BMC20 - Get SEL command "partial get" functionality does not work

DESCRIPTION: The Get SEL (System Event Log) Entry 'Storage.43h' command does not return valid data if "Offset into record" is equal to any value other than zero (start of record), or if "Bytes to read" is equal to any value other than 10h or FFh (both 10h and FFh cause the full 16 bytes of a SEL entry to be read).

IMPLICATIONS: The Get SEL command "partial get" functionality was not implemented. The current server management software does work with the firmware as it exists. The Get SEL command "partial get" would allow retrieval of a section of data instead of all the data.

WORKAROUND: To avoid this problem, always use the Get SEL Entry command with "Offset into record" equal to zero and "Bytes to read" equal to 10h or FFh. Customers who wish to write a SEL viewer may avoid this problem using the Get SEL "full get" command in place of the "partial get."

STATUS: Fix in future release

11. BMC20 - Get SEL Entry (storage 43h) reads last record on invalid record ID

DESCRIPTION: The Get SEL (System Event Log) Entry <Storage 43h> command returns the last SEL record if "SEL Record ID" is equal to an invalid record ID.

IMPLICATIONS: The current default functionality is that the last record will be returned when an invalid record ID is requested. The result was that the last SEL record is returned in all cases when a bad record ID number is provided.

WORKAROUND: Currently all known utilities for viewing the SEL are able to function with the firmware. To avoid this problem, always use the Get SEL Entry command with valid SEL Record IDs (0000h = first entry, subsequent record IDs are returned in the "Next SEL Record ID" fields in the response data, FFFFh = last entry). This may be a consideration to OEMs writing a SEL viewer.

STATUS: Fix in future release

12. OEM VESA string for the onboard Cirrus GD5446* video chip set is incorrectly set to "STBNITRO 64V"

DESCRIPTION: The OEM VESA string on the A450NX server board set returned by VESA BIOS call AX=4F00h (Return Super VGA Information) is "STB NITRO 64V".

This may manifest to an end user when Solaris* is installed on an AD450NX server system. It detects the onboard video controller as an STB Nitro 64V* video card. The STB Nitro 64V is a Cirrus GD5446* based card.

IMPLICATIONS: The impact is that possible confusion for the user who is unaware that the video is a Cirrus GD5446 and not an STB card, which is based on the Cirrus GD5446 chip set. This is the OEM string. This string is for informational purposes only and does not affect any video-specific functionality.

WORKAROUND: None identified

STATUS: Fixed in Cirrus Logic Video BIOS* 1.35 and incorporated into BIOS Production Release 7 (PR7)

13. 4-Slot CPU baseboard caps (fuses) bend upon insertion of the top memory board

DESCRIPTION: Two capacitors (FUSES between the memory board connector and F16 connector) stand higher than the connectors, thus allowing the memory board to bend the components, which could break off.

IMPLICATIONS: This problem may occur on all current 4-slot CPU boards.

WORKAROUND: None identified, but a short-term fix in the factory is implementing prebent fuse at R8J1

STATUS: Fixed

14. The 420-W power supply regulation specified for -12 V is too wide for PCI slots under a heavy load

DESCRIPTION: The problem may occur when heavily loading the -12 V power to the PCI slots. If the power is operating at ±10% (worst case) regulation tolerance, and a maximum current is drawn (100 mA on all slots), a voltage of less than (closer to ground) -12 V minus 10% = -10.8 V is possible. An IR drop on the copper from the I/O baseboard power connector to the PCI slots would be a contributing factor. This may also be a result of the spec of ±10% at the slot and ±10% regulation tolerance for the supply.

IMPLICATIONS: The probability of this occurring is very low. Test measurements of four power supplies resulted in worst case regulation at about -4%. No problems have been observed.

WORKAROUND: None identified.

STATUS: Fixed in 500-W power supply

15. Processor temperature readings may not be reported correctly

DESCRIPTION: During system power-up, the Intel® A450NX CPU baseboard may incorrectly initialize the processor slot temperature sensor IDs resulting in incorrect processor temperature data being reported to server management software. The processor temperature sensor is a new feature on the A450NX 4-way platform, which was not available on previous 4-way platforms.

IMPLICATIONS: If the CPU baseboard incorrectly initializes the temperature sensor IDs during power up, when server management software tries to read the current temperature of the installed processors, the temperature data returned may be incorrect or missing.

WORKAROUND: Do not try to read the processor temperature sensors.

STATUS: Fixed in the 4 and 5 slot CPU boards.

16. PCI Restreaming buffer not supported on C0 stepping of the PXB

DESCRIPTION: When continuous pre-fetch mode and restreaming buffers are both enabled, it is possible to see data corruption on the PCI bus when multiple masters are driving. This corruption has been observed only in systems where continuous pre-fetch AND restreaming buffers are enabled. For this reason, it is recommended that customers disable PCI restreaming buffers. Please note that this recommendation is consistent with recommendations for previous PXB steppings, and PCI performance is still expected to improve with the C0-stepping.

IMPLICATIONS: If data corruption occurs on the PCI bus, an OS halt may occur.

WORKAROUND: Fixed in BIOS Production Release 9 (PR9) which allows a user to enable continuous pre-fetch without enabling the restreaming buffer. Additionally, the user option to enable restreaming is removed from this BIOS.

17. CORFE* I2O adapter card does not initialize

DESCRIPTION: It has been documented that if a certain card (Intel® EtherExpress™ PRO100+ or Adaptec* 3940AUW) is present in any PCI slot on PCI bus segment 2, (slots 3, 4, 5 or 6) the error "resource Conflict - PCI: Bus:03, Device:08, Function:00" will occur after POST. Even when attempting to use the System Setup Utility (SSU) to resolve the conflict, the error will persist. The error will go away only when the card (EtherExpress PRO100+ or Adaptec 3940AUW) is removed from a slot on the PCI bus segment 2 and placed in PCI slots 1 or 2.

IMPLICATIONS: The CORFE* I2O card cannot be initialized and used in the system.

WORKAROUND: Fixed in Production Release BIOS 11. In certain configurations of adapter cards, an arithmetic error in the BIOS can result in very large adapter memory requests.

18. BIOS successful boot event message not documented

DESCRIPTION: The AD450NX BIOS generates an event on successful boot up but it does not document the contents of this event message. The message generated is "0x11 0x00 0x02 0x12 0xEF 0xE7 0x01 0xFF 0xFF".

IMPLICATIONS: No affects on the system functionality.

WORKAROUND: Will not fix.

19. The APIC clock on the AD450NX CPU board undershoots the specification

DESCRIPTION: The APIC clock on the AD450NX CPU board has been identified to undershoot the specification by 0.4volts. The spec for the absolute max voltage is Vtt +0.7V and the min voltage is Vtt -0.3V.

IMPLICATIONS: This undershoot of 0.7V only lasts for a few picoseconds and has had no measurable effect to the functionality of the board. Implementing a fix to this board could impact the very sensitive rise and fall times of the APIC clock and for this reason Intel does not feel that a fix should be implemented at this point in the product lifecycle. Additionally a costly full board set requalification would be necessary as the result of a Front Side Bus (FSB) change.

WORKAROUND: Will not fix.

20. Red Hat Linux 6.1 fails to boot on AD450NX with Cascades Processor

DESCRIPTION: Although Red Hat Linux 6.1 flawlessly proceeded and completed installation on an AD450NX system with Cascades processors installed, upon subsequent system rebooting, it fails to boot with the following appearing on screen, "LIL".

IMPLICATIONS: Red Hat Linux 6.1 fails to boot.

WORKAROUND: Go into the BIOS default configuration for the Host Adapter at Advanced Configuration, set the "Extended BIOS Translation to DOS Drive >1 gigabyte" option to "DISABLED". The system will boot normally after this workaround had been implemented.

21. Recovery boot requires memory to be populated in bank 0

DESCRIPTION: During testing of the BIOS recovery feature on the platforms, if bank 1 of the memory board is populated with memory and bank 0 is left empty, the system will alarm a beep code and will not perform the recovery boot.

IMPLICATIONS: Recovery boot will fail if memory is not populated in bank 0.

WORKAROUND: Will not fix, Recovery boot always requires memory to be populated in bank 0.

22. Design Spec Violation when VRM is not installed on the A450NX CPU board.

DESCRIPTION: Each VRM socket on the CPU board has two outputs that feed into a 74ACT08 logical "AND" gate and then invert the signal to produce the PowerGood signal (PWRGD). When a VRM is not present, one of the inputs to the 74ACT08 is pulled down to approximately 0.83V. This design violated the specification of the voltage input low for 74ACT08 logical gate.

IMPLICATIONS:. If a VRM fails or a VRM associated with L2 cache is not present, the system may not boot.

WORKAROUND: This will be fixed by disabling the "VRM absence detection circuitry" on -301 Aspen 5 slot CPU boards and on -601 Aspen 4 slot CPU boards.

Specification Changes

The specification changes listed in this section apply to *the A450NX MP Server Board Set Technical Product Specification*. All specification changes will be incorporated into a future release of the *A450NX MP Server Board Set Technical Product Specification*.

CODES USED IN FOLLOWING TABLE

Doc:	Document change or update that will be implemented.
Fix:	Intel intends to fix this erratum in a future revision of the hardware or software associated with the A450NX MP Server Board Set. (Fix in future release)
Fixed:	This erratum has been fixed.
NoFix:	There are no plans to fix this erratum. Will not fix
Shaded:	This erratum is either new or modified from the previous version of the document.

Table 8 - Specification Changes

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	BIOS POST Code Correction
2	Doc	CPU Jumper Settings

1. BIOS POST code correction

The following are corrections to the Table 3-13 POST Error Messages and Codes in section 3.14.2 of the A450NX MP Server Board Set TPS.

Table 9 - POST Error Messages and Codes

Code	Error Message
0010	Cache Memory Failure, Do Not Enable Cache (Not used on A450NX –see 02D0)
02D0	System cache error - Cache disabled
0060	Keyboard Is Locked ... Please Unlock It (Not used on A450NX –see 0213)
0213	Keyboard locked - Unlock key switch
0070	CMOS Time & Date Not Set (Not used on A450NX –see 0271)
0271	Check date and time settings
0083	Shadow Of PCI ROM Failed (Not used on A450NX)
0131	Floppy Drive A: (Not used on A450NX –see 02B0)
02B0	Diskette drive A error
0132	Floppy Drive B: (Not used on A450NX –see 02B1)
02B1	Diskette drive B error
0191	CMOS Battery Failed (Not used on A450NX –see 0250)
0250	System battery is dead - Replace and run SETUP
0198	CMOS Checksum Invalid (Not used on A450NX –see 0251)
0251	System CMOS checksum bad - Default configuration used
0370	Keyboard Controller Error (Not used on A450NX –see 0212)
0212	Keyboard Controller Failed
0373	Keyboard Stuck Key Detected (Not used on A450NX –see 0210)
0210	Stuck Key
0450	Master DMA Controller Error (Not used on A450NX –see 02F5)

Code	Error Message
0451	Slave DMA Controller Error (Not used on A450NX –see 02F5)
0452	DMA Controller Error (Not used on A450NX –see 02F5)
02F5	DMA Test Failed
0460	Fail-safe Timer NMI Failure (Not used on A450NX –see 02F7)
02F7	Fail-safe Timer NMI Failed
0461	Software Port NMI Failure (Not used on A450NX –see 02F6)
02F6	Software NMI Failed
0465	Bus Timeout NMI in Slot (Not used on A450NX)
0467	Expansion Board NMI in Slot (Not used on A450NX)
0805	Insufficient Memory to Shadow PCI ROM: (Not used on A450NX)
8100	Processor 1 failed BIST (Please note this has changed from Processor 0 to 1)
8101	Processor 2 failed BIST (Please note this has changed from Processor 1 to 2)
8102	Processor 2 failed BIST (Not used on A450NX –see 8120)
8120	Processor 3 failed BIST
8103	Processor 3 failed BIST (Not used on A450NX –see 8121)
8121	Processor 4 failed BIST
0820	Expansion Board Disabled in Slot (Not used on A450NX)
0982	I/O Expansion Board NMI in Slot (Not used on A450NX)
0984	Expansion Board Disabled in Slot (Not used on A450NX)
0985	Fail-safe Timer NMI (Not used on A450NX – see 02F7)
02F7	Fail-safe Timer NMI Failed
0987	Bus Timeout NMI in Slot (Not used on A450NX)

2. CPU Jumper Settings

Table 10 - Board Configuration Jumper Block (Bus Ratio)

Pins 5-6	Pins 7-8	Pins 9-10	Pins 11-12	Bus Ratio	Core Freq. (MHz)
0	0	0	0	Reserved	--
0	0	0	1	6:1	600
0	0	1	0	3:1	300
0	0	1	1	7:1	700
0	1	0	0	4:1	400
0	1	0	1	8:1	800
0	1	1	0	5:1	500
1	0	0	0	Reserved	--
1	0	0	1	13:2	650
1	0	1	0	7:2	350
1	0	1	1	15:2	750
1	1	0	0	9:2	450
1	1	1	0	11: 2	550

Key: 0-open; 1-closed

Specification Clarifications

The specification clarifications listed in this section apply to *the A450NX MP Server Board Set Technical Product Specification*. All specification clarifications will be incorporated into a future release of the *A450NX MP Server Board Set Technical Product Specification*.

CODES USED IN FOLLOWING TABLE

Doc: Document change or update that will be implemented.

Fix: Intel intends to fix this erratum in a future revision of the hardware or software associated with the A450NX MP Server Board Set. (Fix in future release)

Fixed: This erratum has been fixed.

NoFix: There are no plans to fix this erratum. Will not fix

Shaded: This erratum is either new or modified from the previous version of the document.

Table 11 - Specification Clarifications

NO.	PLANS	SPECIFICATION CLARIFICATIONS
1	Doc	AD450NX Product Guide correction

1. AD450NX Product Guide correction

The following are corrections to the Table 3-13 POST Error Messages and Codes in section 3.14.2 of the A450NX MP Server Board

The AD450NX MP Server System Product Guide does not correctly represent the I/O board configuration jumpers in table 17-1 on page 233. Password Clear, CMOS Clear and BIOS Recovery are listed as pins 6, 7 and 8. They should actually be pins 5, 6 and 7 respectively, as indicated in the diagram below. However please note that the A450NX Board Set Technical Product Specification has the same jumper block diagram for the I/O board and all jumpers are correctly labeled. Please reference this diagram on page 2-13 of the board set TPS as well as below.
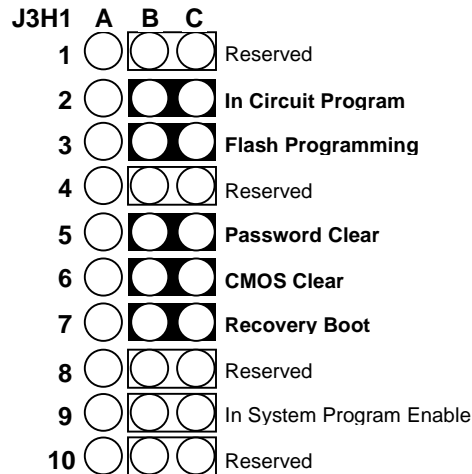

Figure 1 - Configuration Jumper Block (J3H1)