

PCI OPTION FINGERS & ISO BUFFERS



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ROBERT COLPOYS
ENGINEER:
ROBERT COLPOYS

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TITLE:
BMP BASEBOARD
DATE LAST MODIFIED:
Mon Aug 15 13:58:11 2005

DWG.#:
C73014

REV:
04

D

C

B

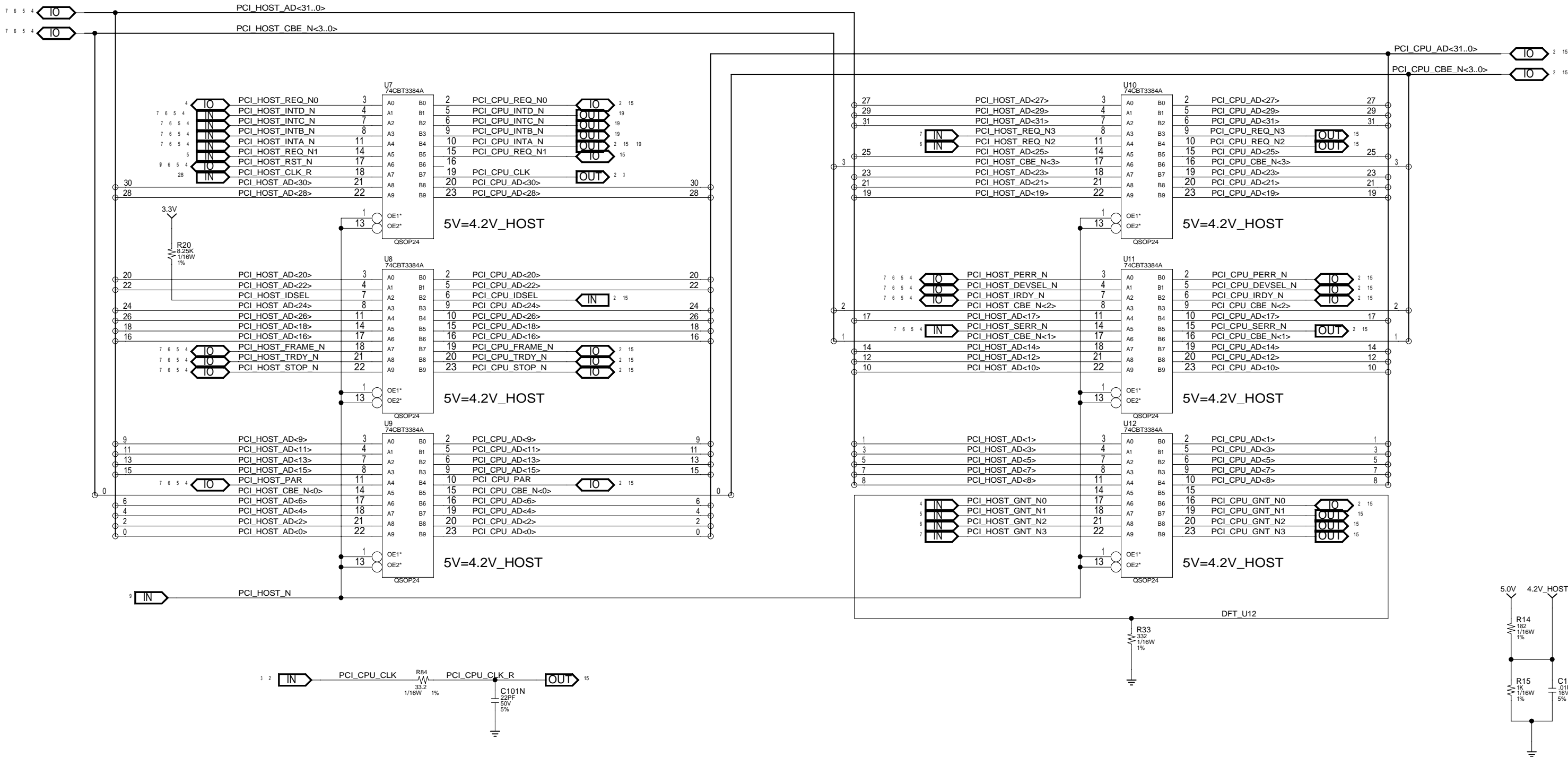
A

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A



PCI HOST BUFFERS

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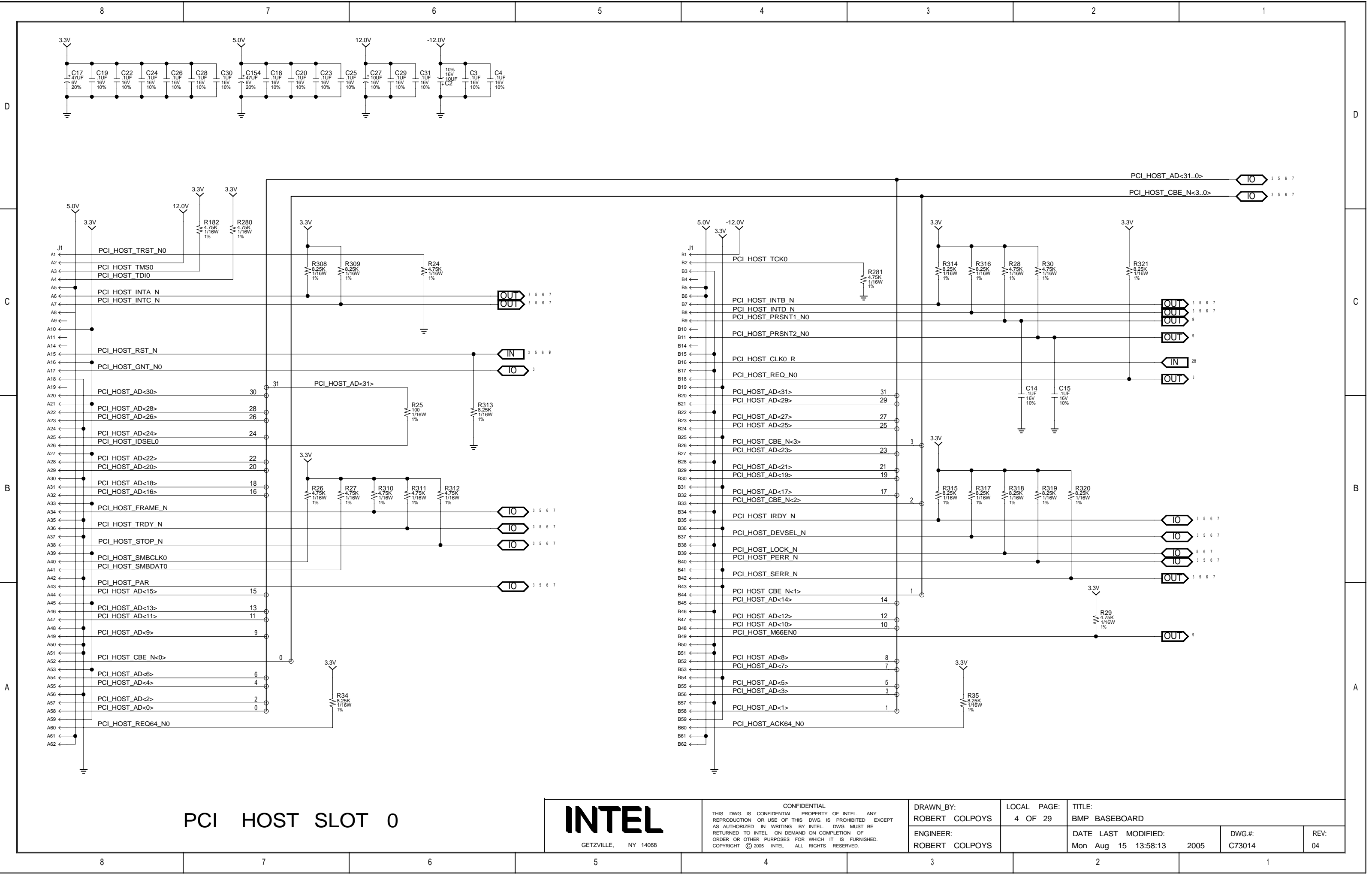
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PCI HOST SLOT 0



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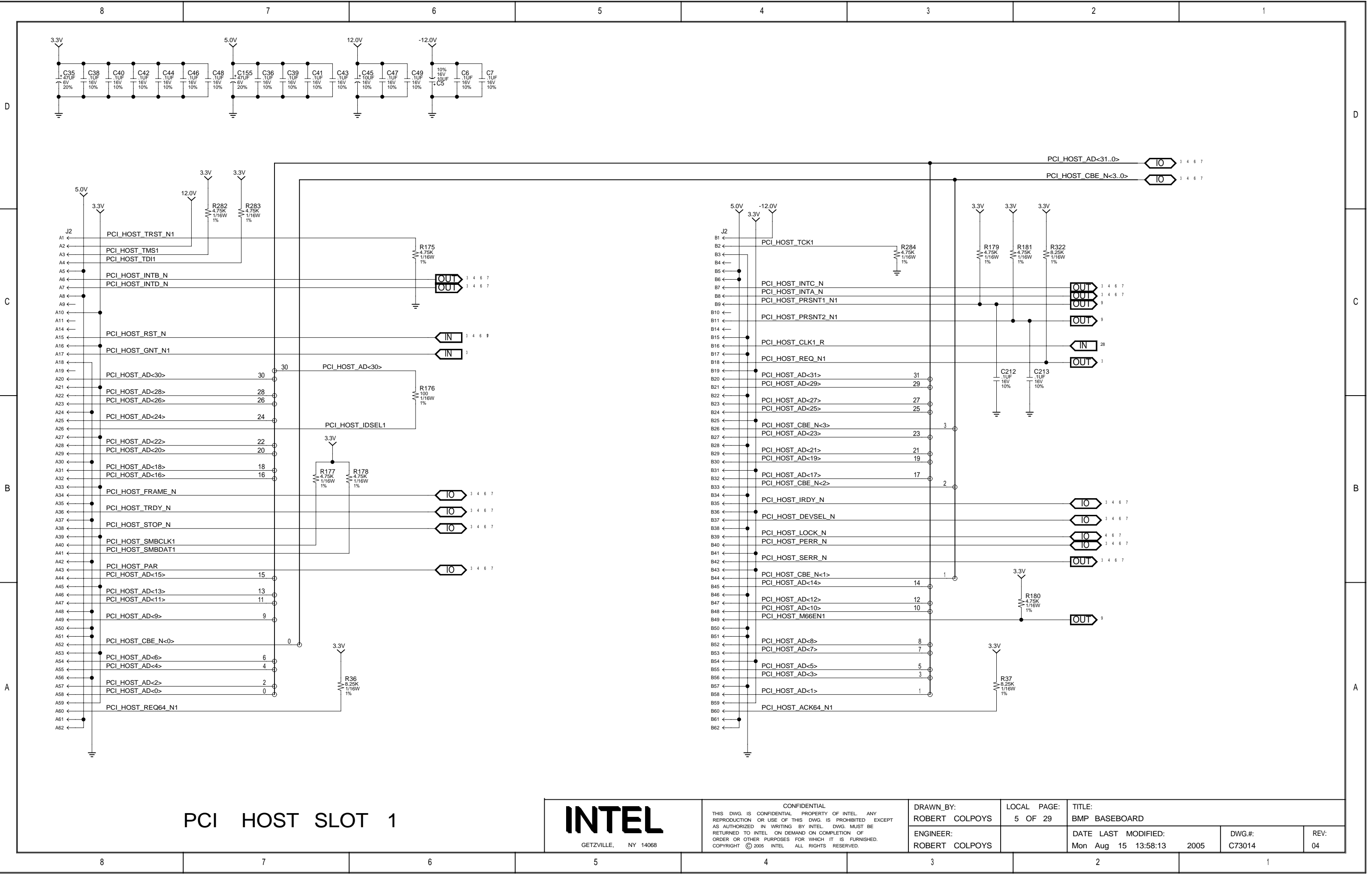
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PCI HOST SLOT 1

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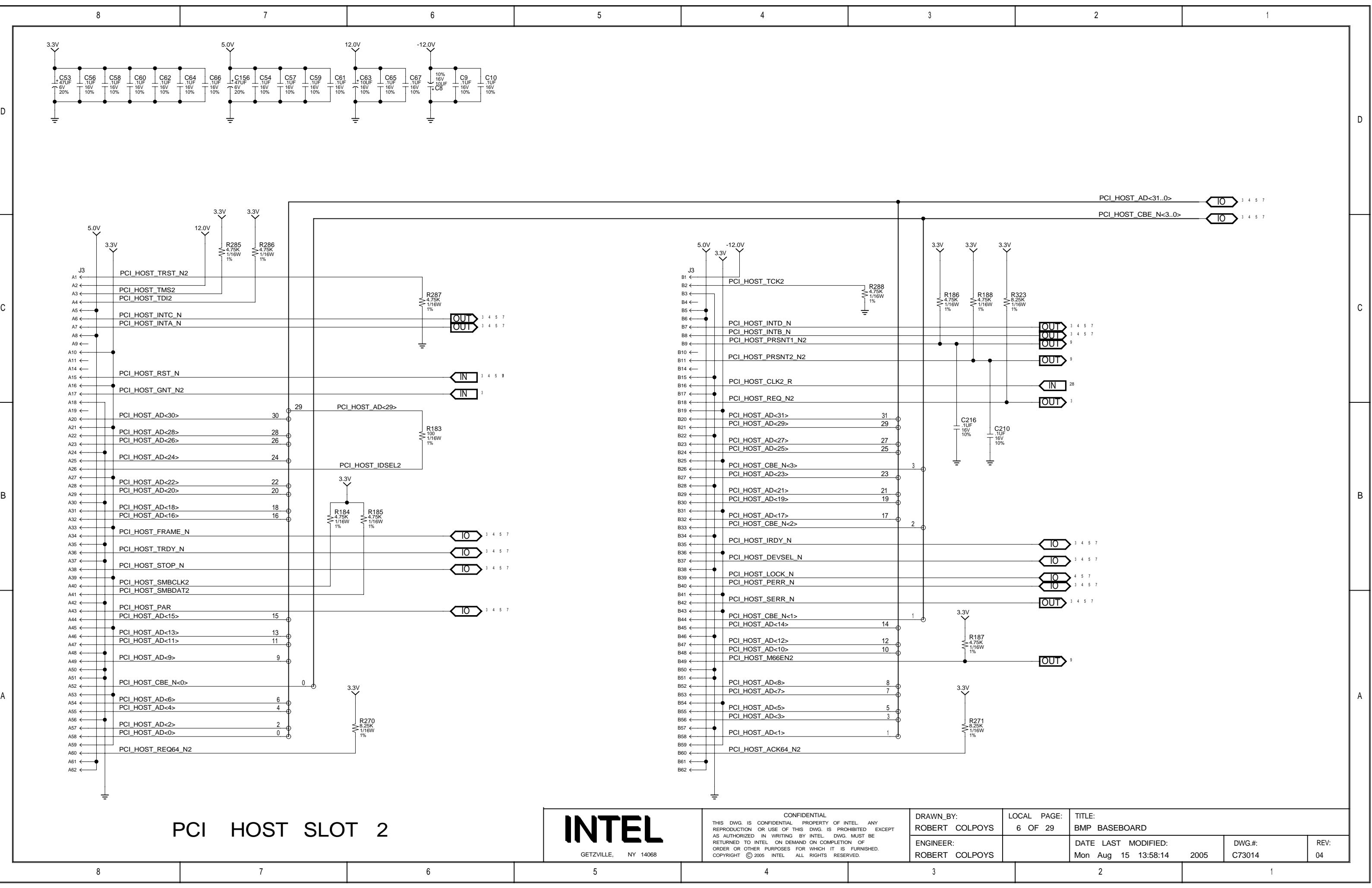
LOCAL PAGE:
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PCI HOST SLOT 2

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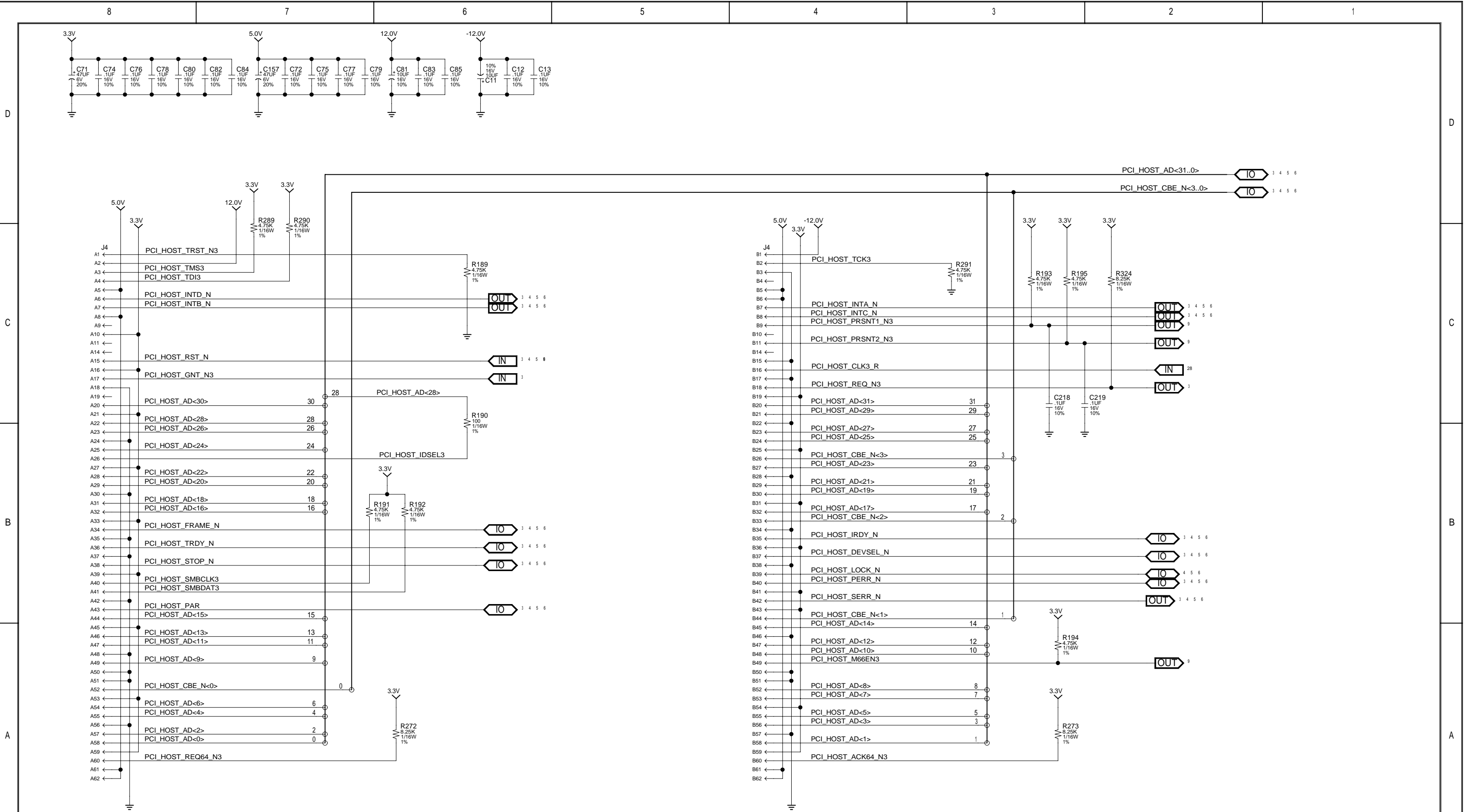
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ENGINEER:
ROBERT COLPOYS

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TITLE:
BMP BASEBOARD
DATE LAST MODIFIED:
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04

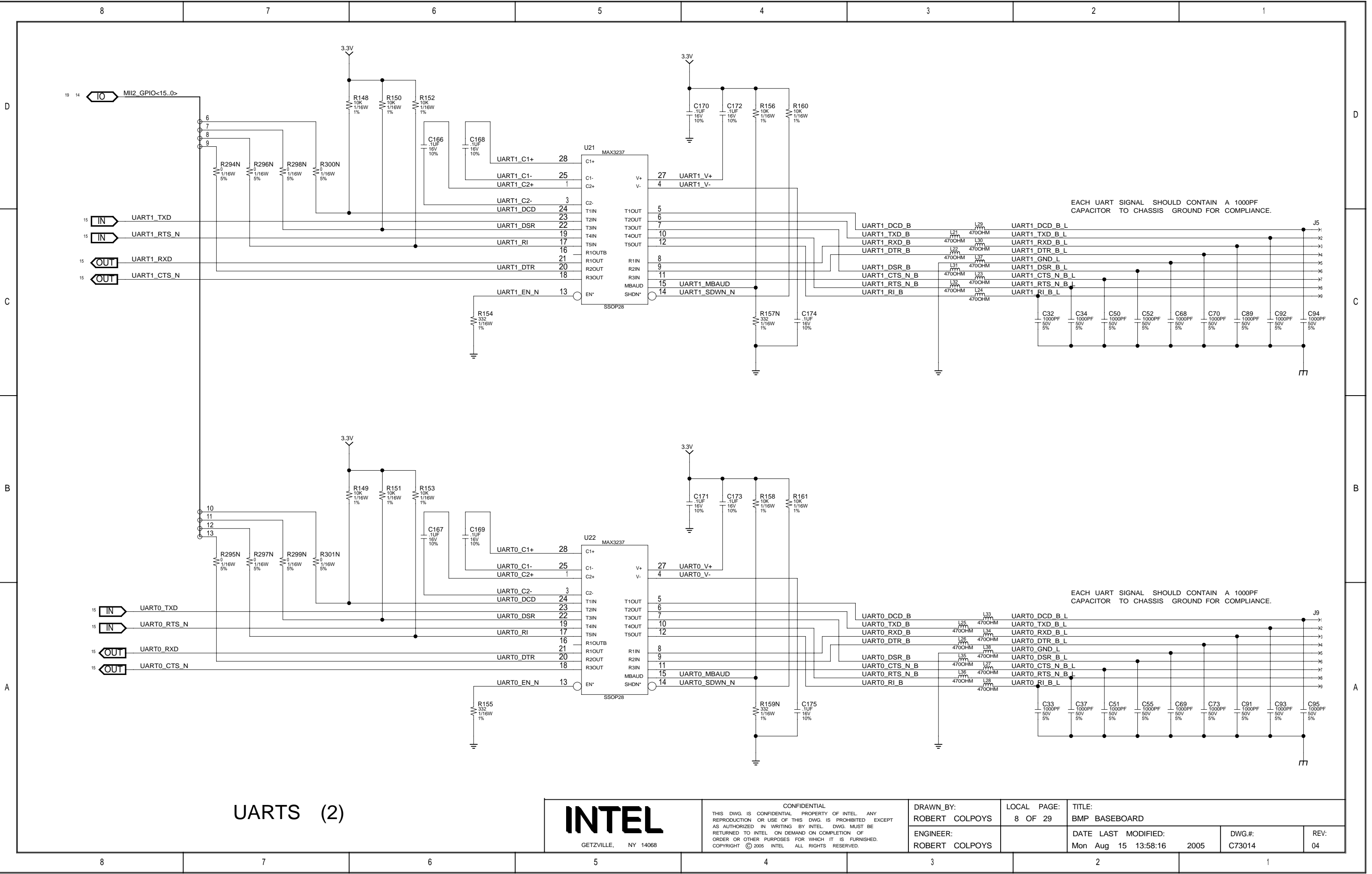


PCI HOST SLOT 3



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ENGINEER:
ROBERT COLPOYS

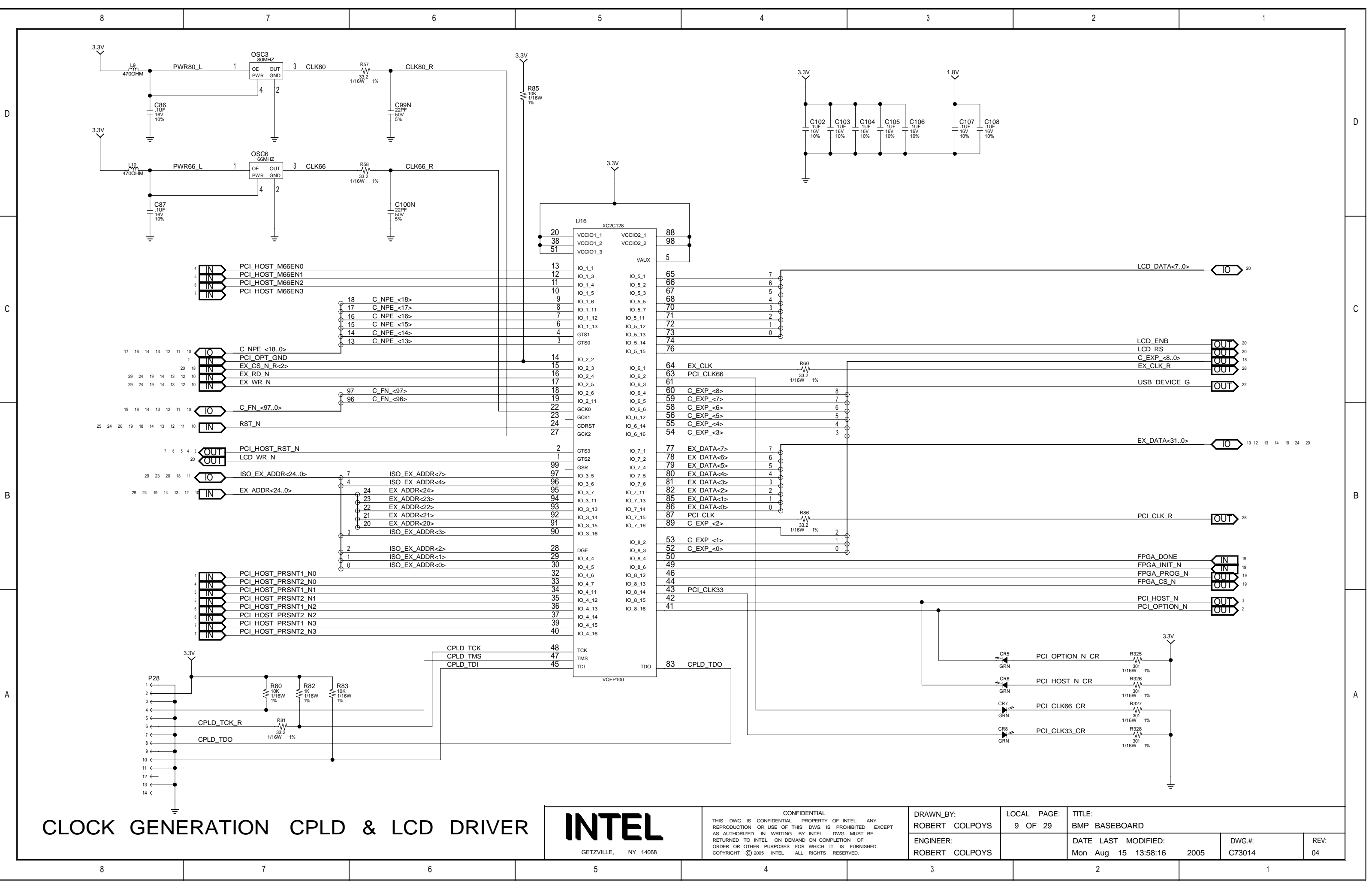
LOCAL PAGE:
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BMP BASEBOARD

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Mon Aug 15 13:58:16 2005

DWG.#:
C73014

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04



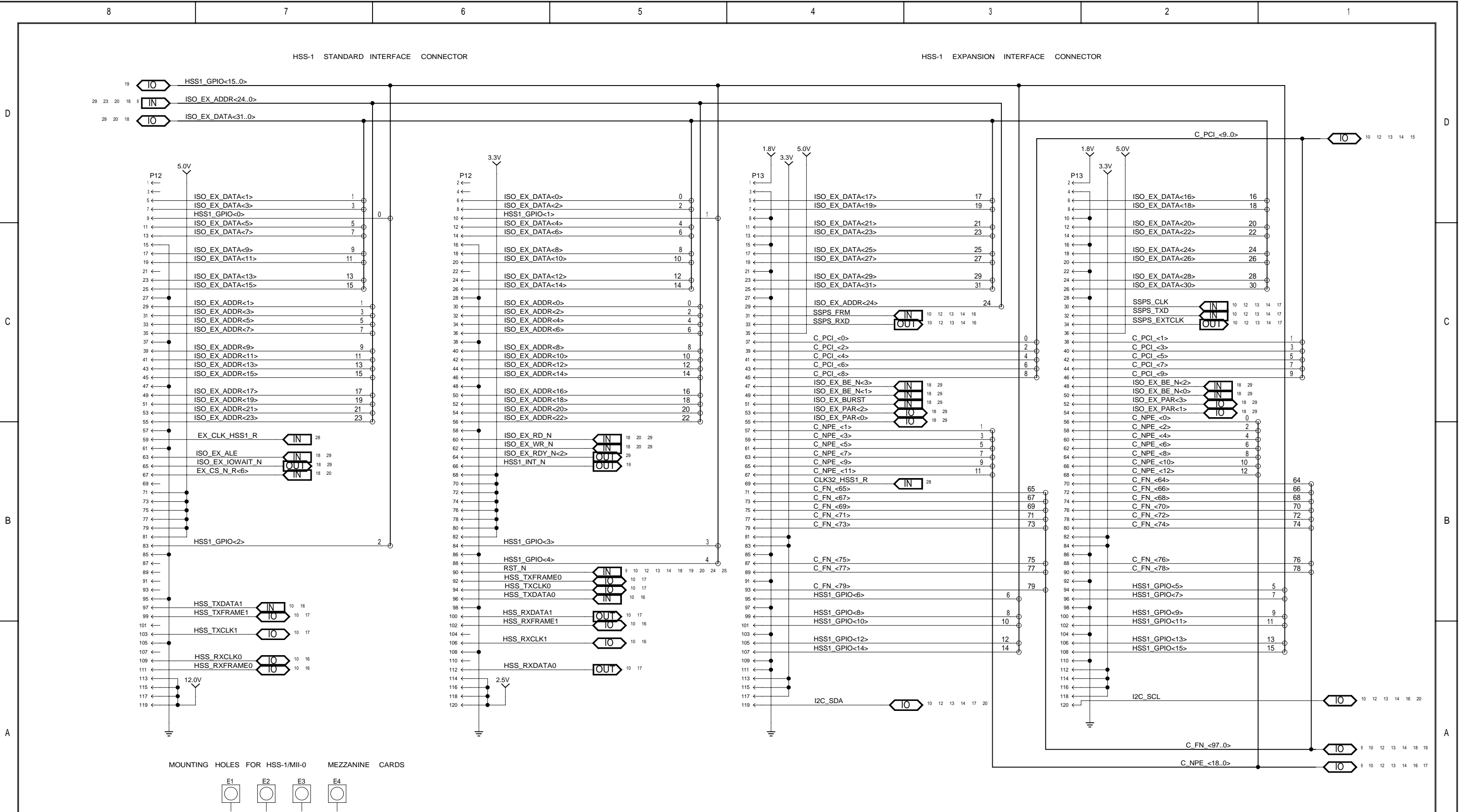
CLOCK GENERATION CPLD & LCD DRIVER



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HSS-1 MEZZANINE CONNECTORS



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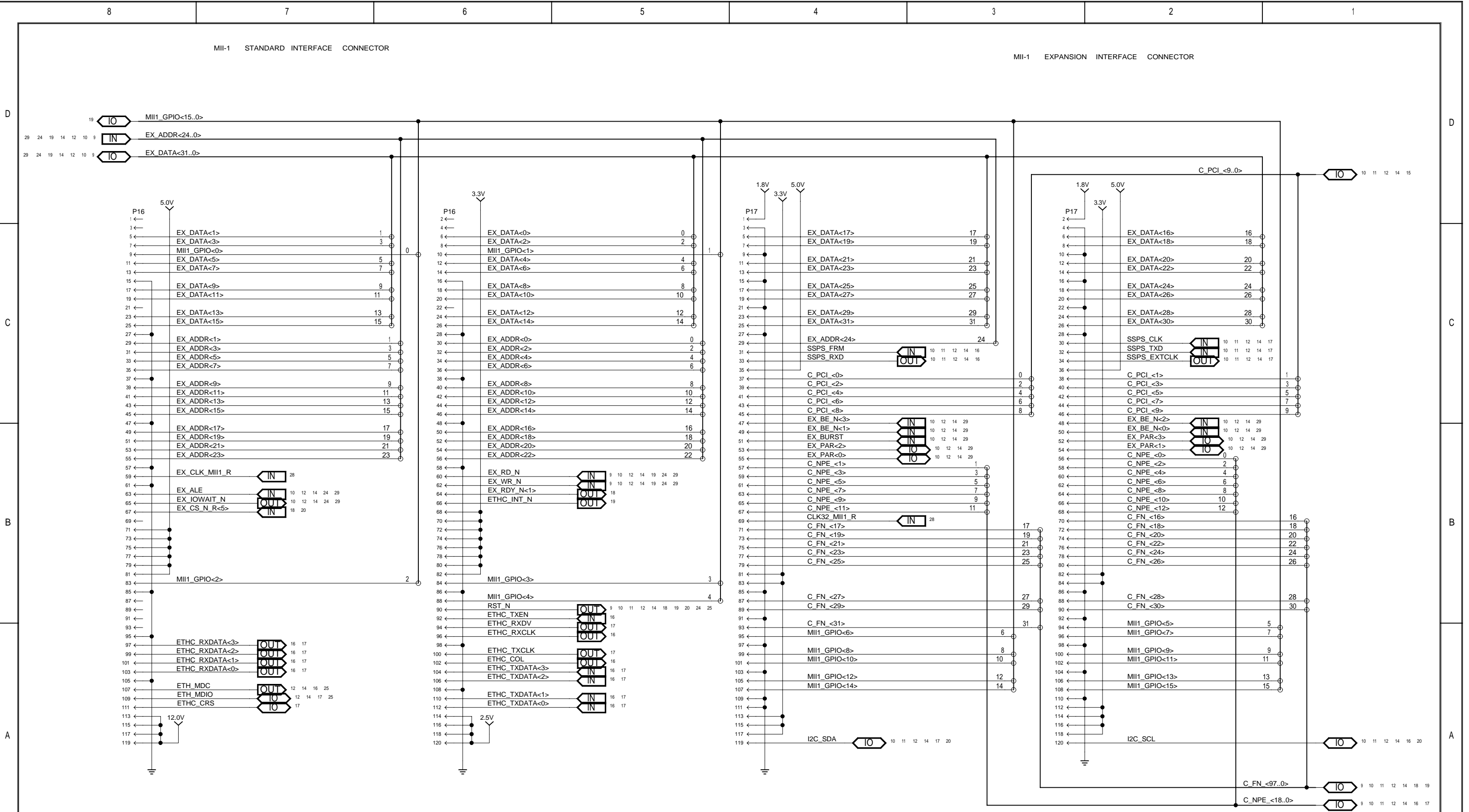
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ROBERT COLPOYS
ENGINEER:
ROBERT COLPOYS

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MII-1 (NPE-C) MEZZANINE CONNECTORS



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ROBERT COLPOYS	13 OF 29	BMP BASEBOARD			
ENGINEER:		DATE LAST MODIFIED:	DWG.:	REV:	
ROBERT COLPOYS		Mon Aug 15 13:58:20 2005	C73014	04	

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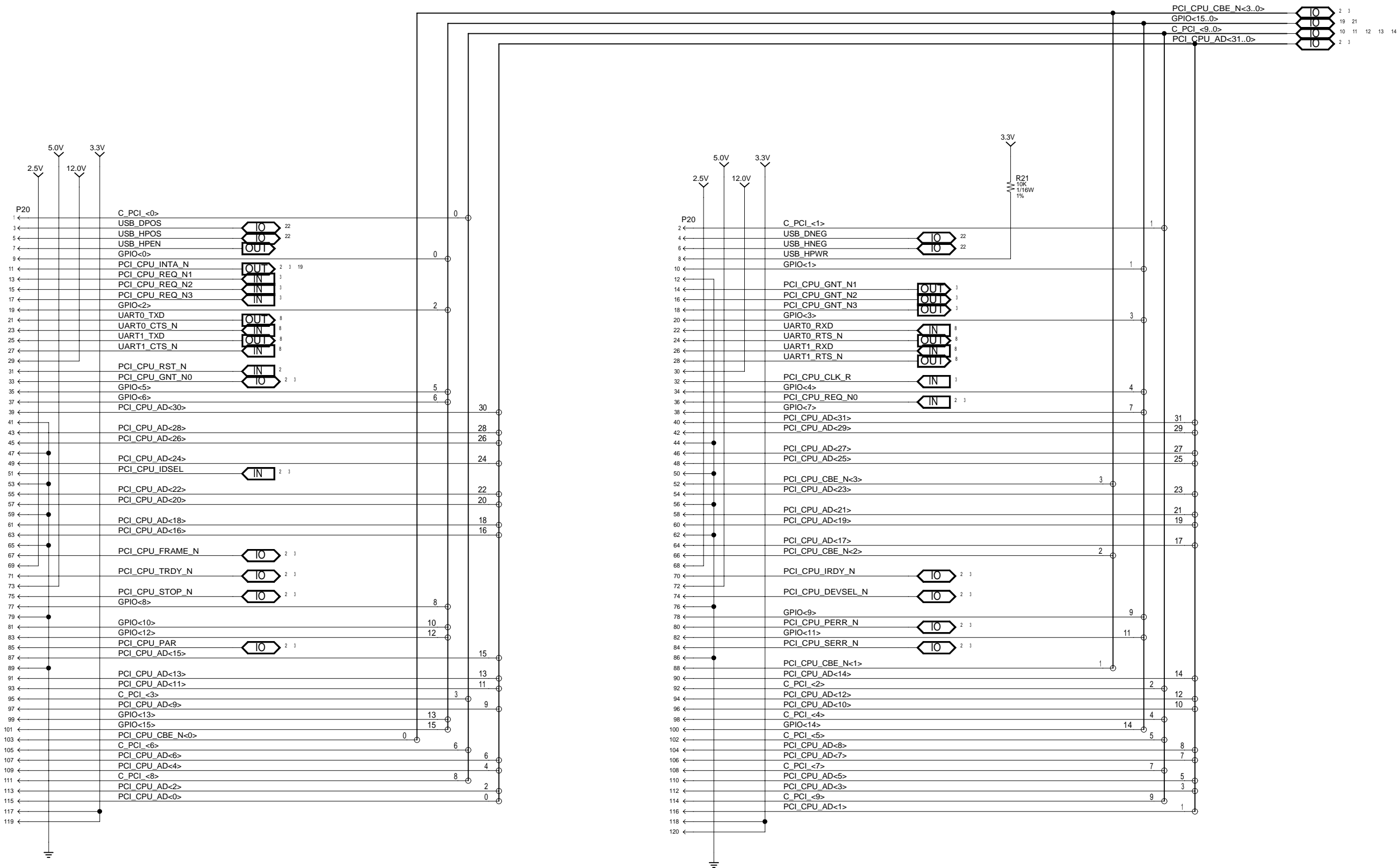
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CPU MODULE PCI CONNECTOR

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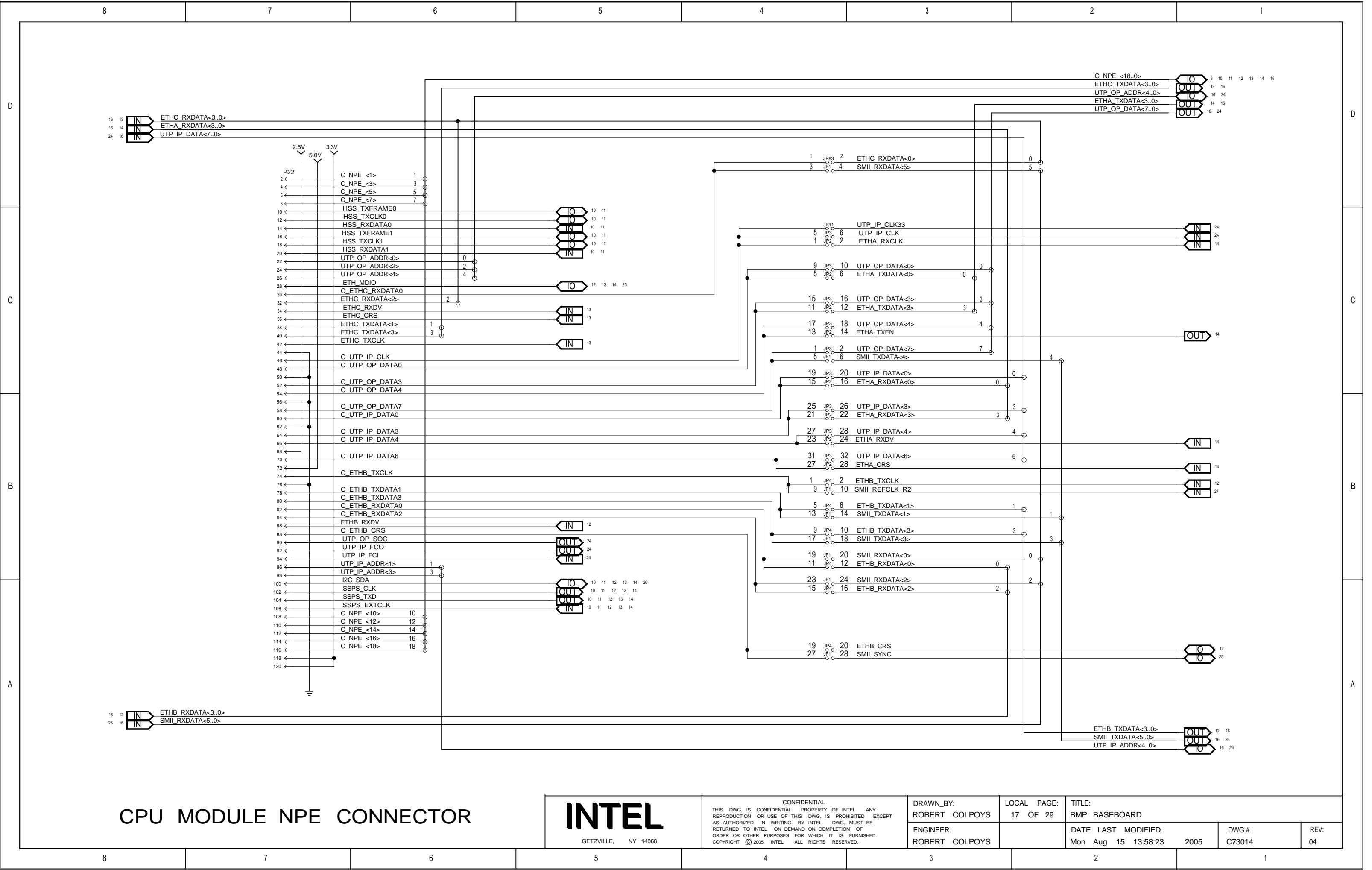
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ROBERT COLPOYS
ENGINEER:
ROBERT COLPOYS

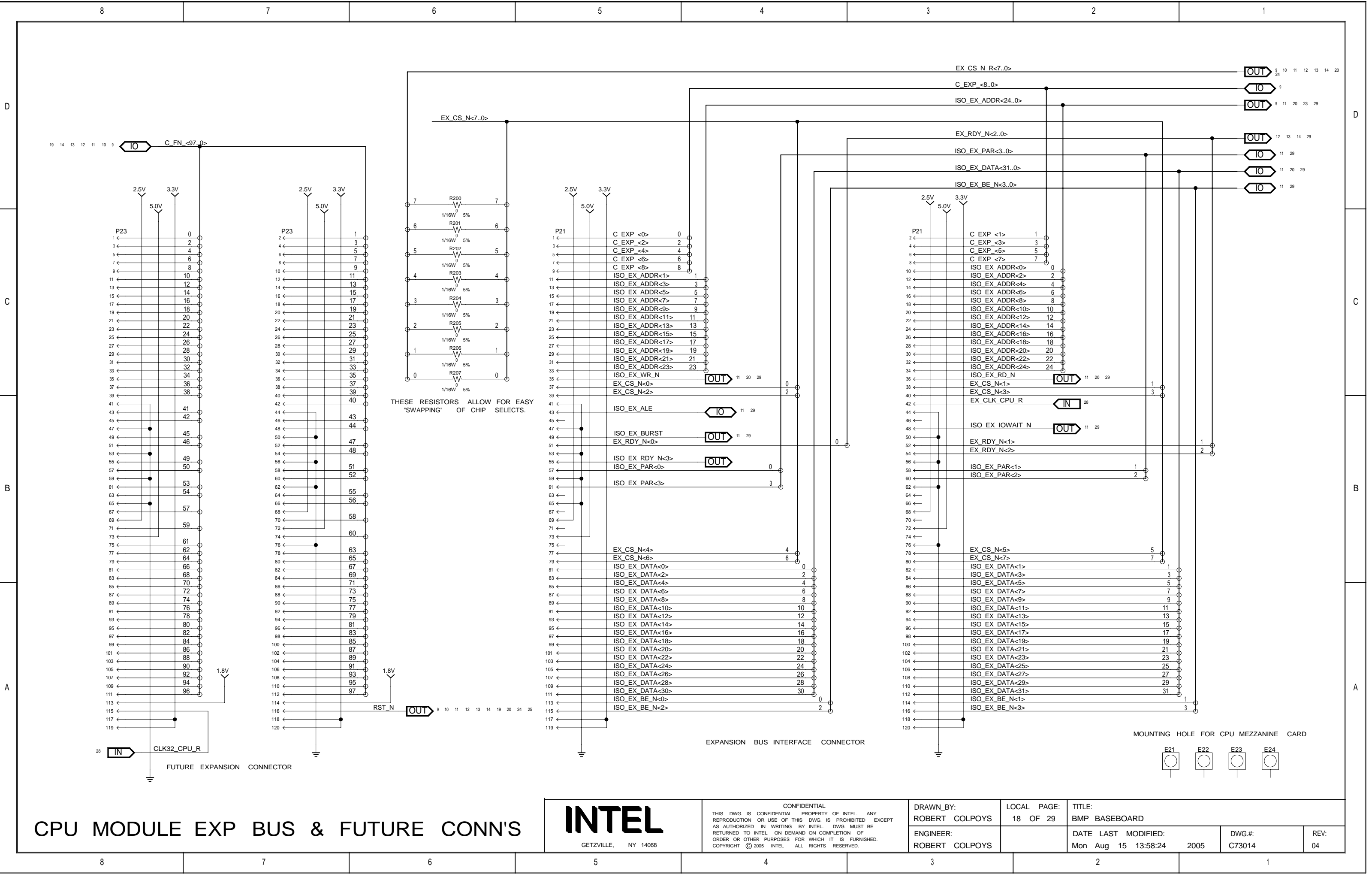
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CPU MODULE EXP BUS & FUTURE CONN'S



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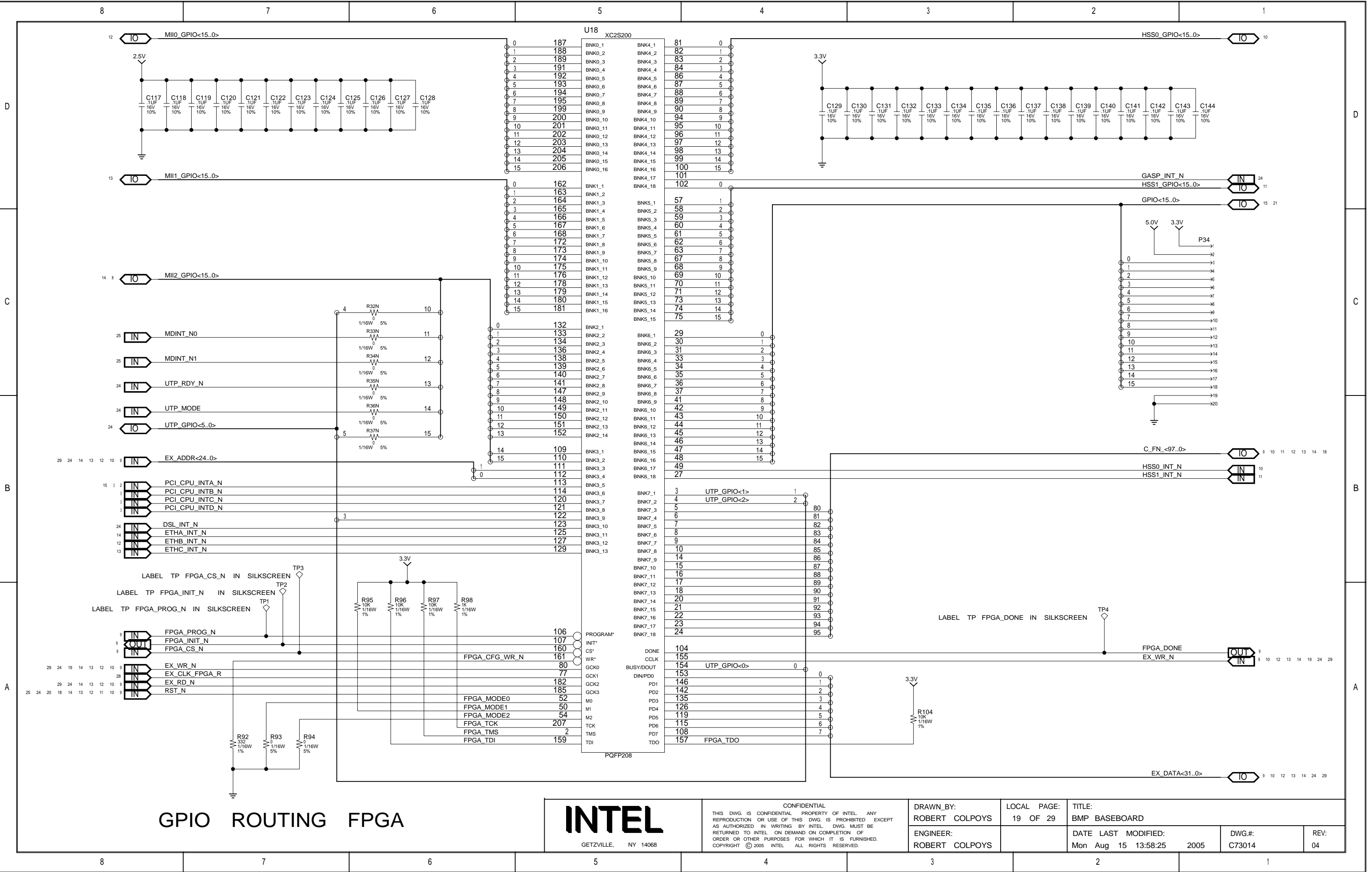
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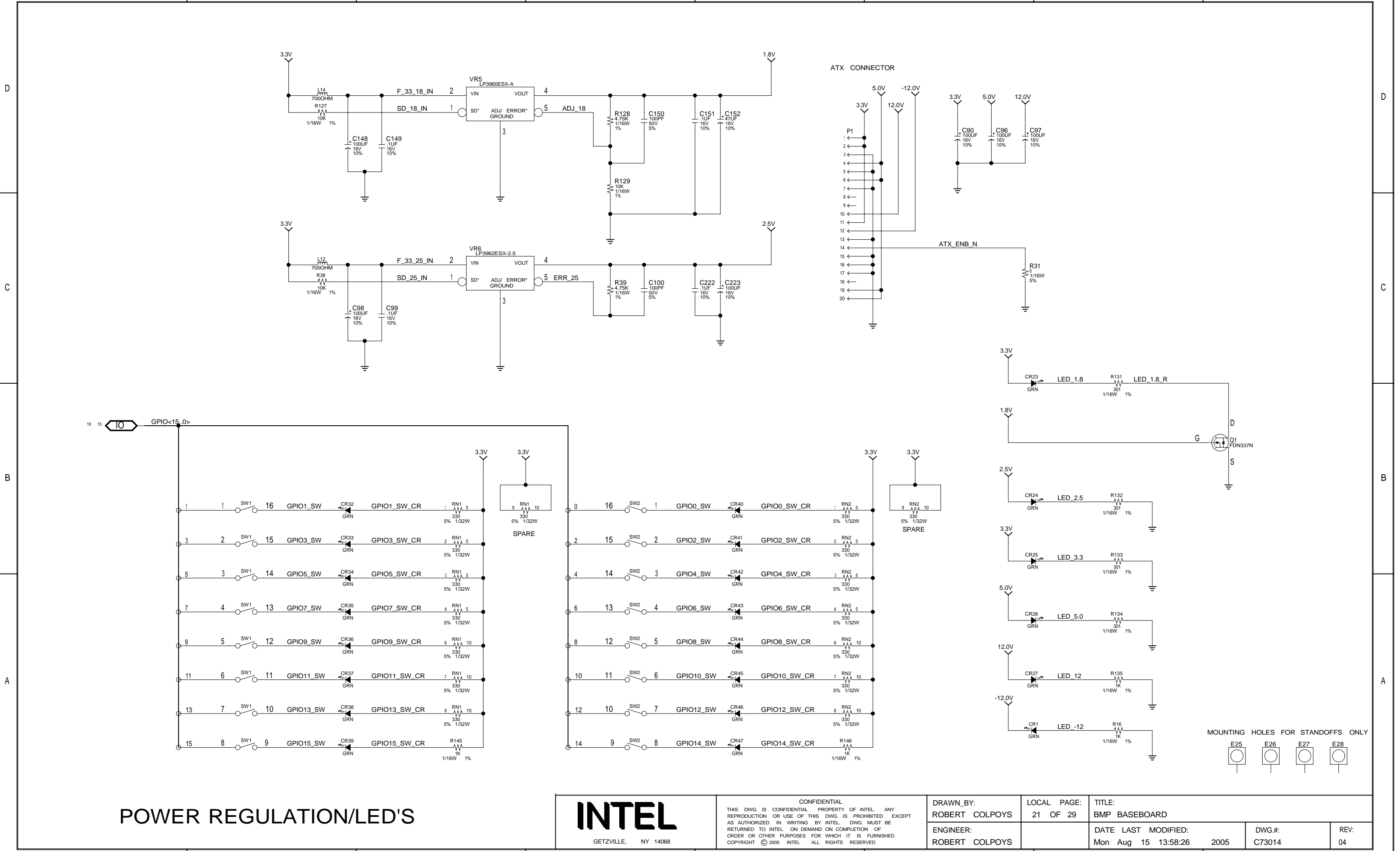
GPIO ROUTING FPGA



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POWER REGULATION/LED'S

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DWG.#:
C73014

REV:
04

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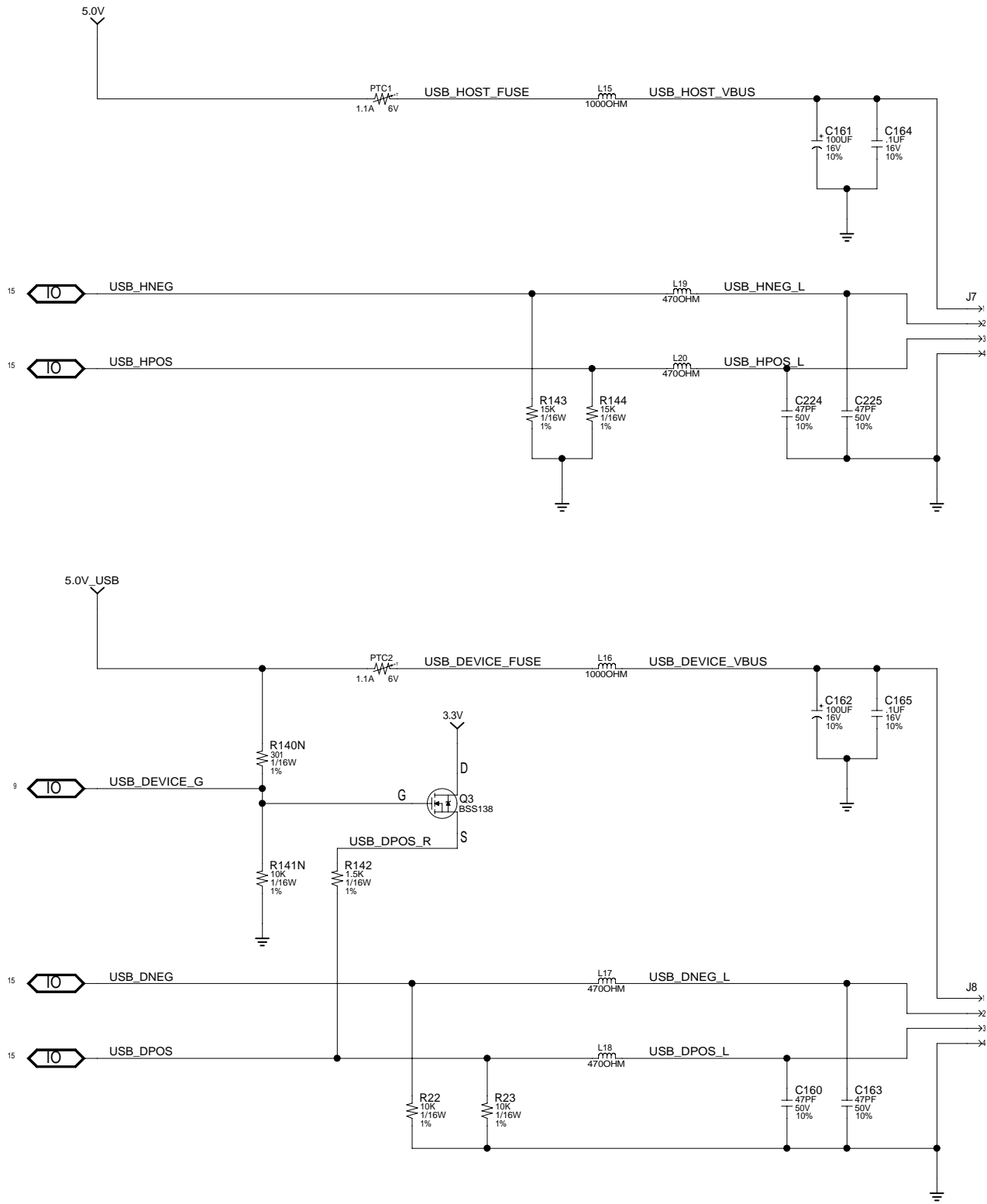
A

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A



USB HOST / USB DEVICE

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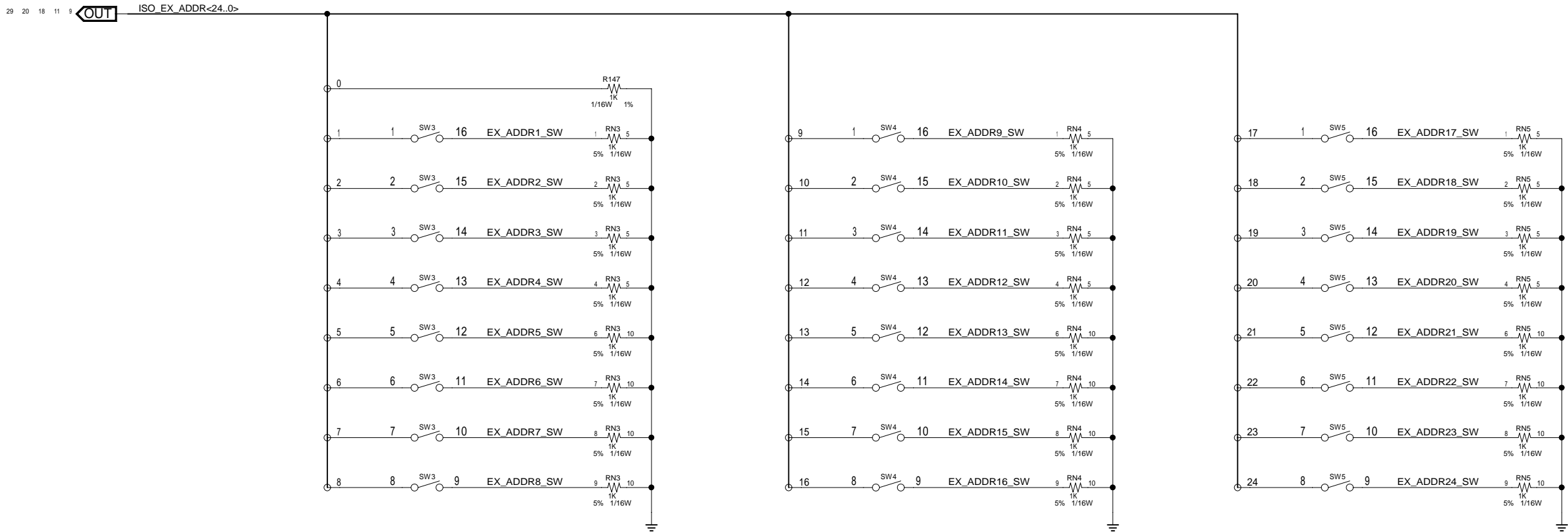
TITLE:
BMP BASEBOARD

DATE LAST MODIFIED:
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DWG.#:
C73014

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04

THE FUNCTION OF THE NPU RESET EXP BUS CONFIG STRAPS
IS SPECIFIC TO THE CPU. THE DESCRIPTION OF THESE
STRAPS ARE DEFINED ON THE SPECIFIC CPU MODULE SCHEMATICS.

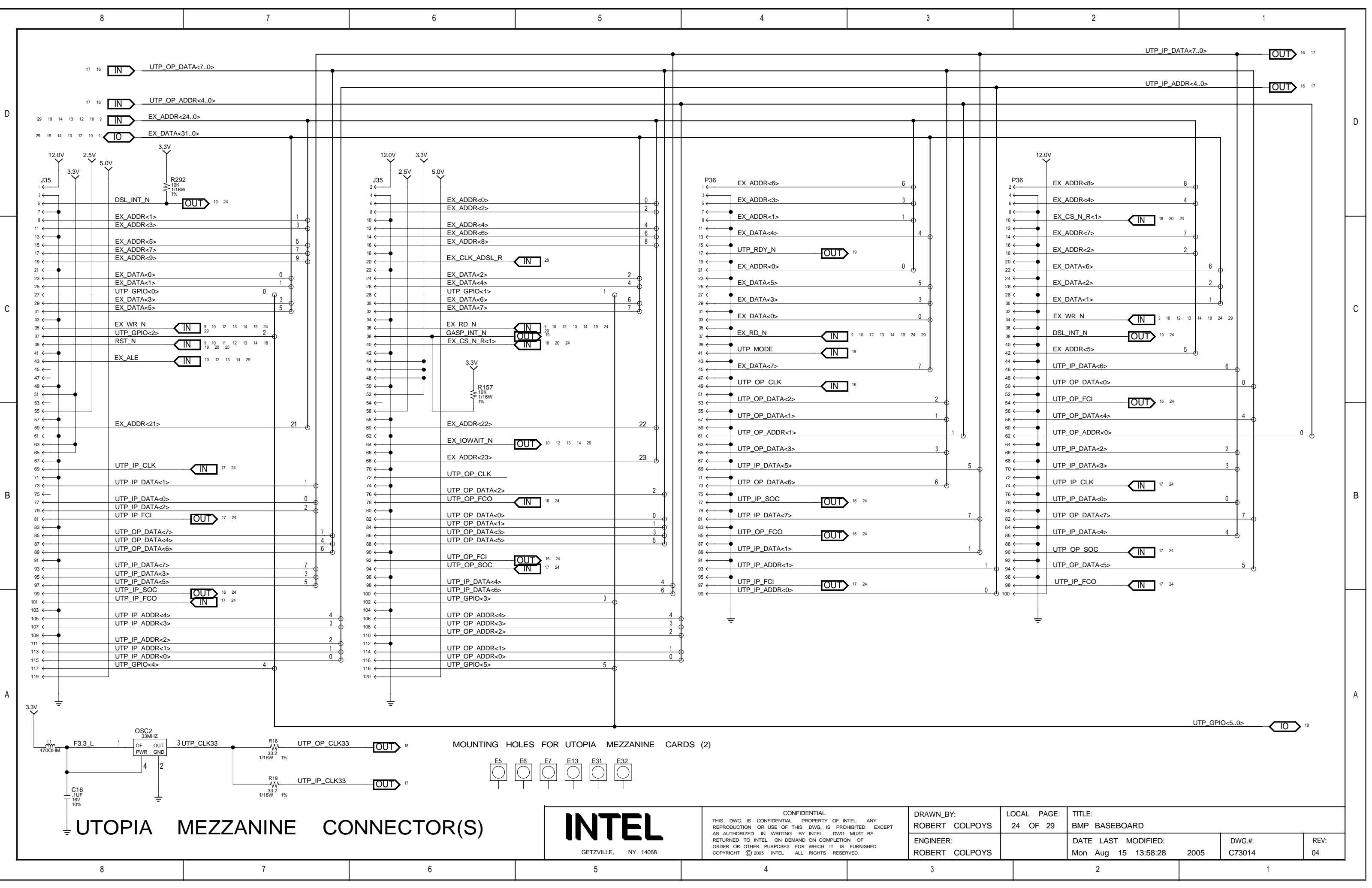


NPU RESET EXP BUS CONFIG STRAPS



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ENGINEER: ROBERT COLPOYS		DATE LAST MODIFIED: Mon Aug 15 13:58:28 2005	DWG.#: C73014	REV: 04



UTOPIA MEZZANINE CONNECTOR(S)



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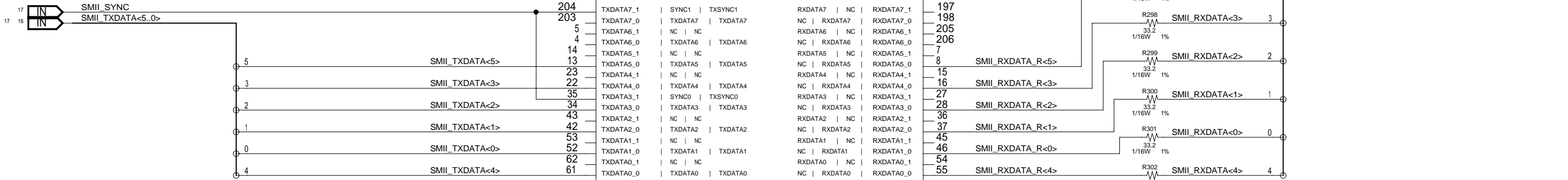
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C73014

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NPE	SMII_TX/RXDATA
A	4
B	0,1,2,3
C	5

D

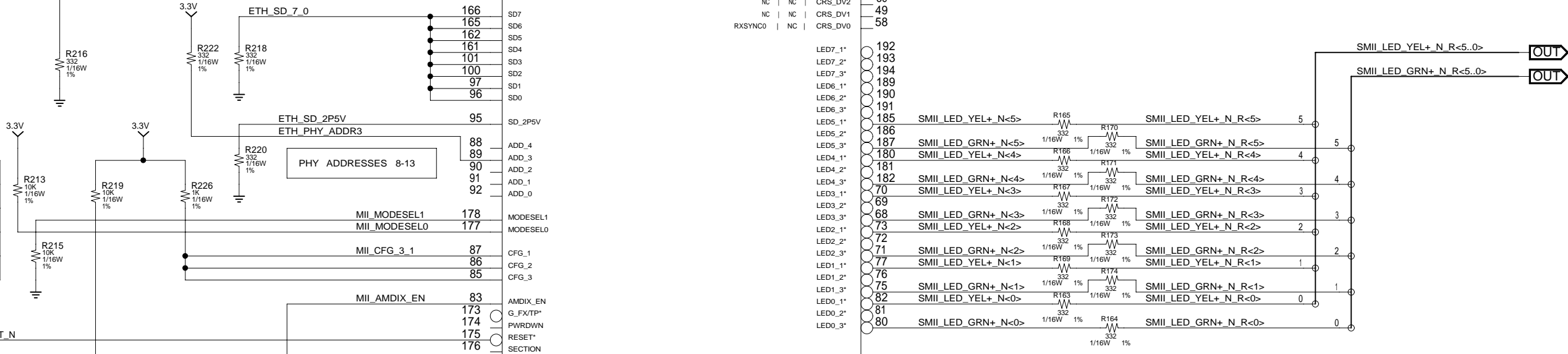


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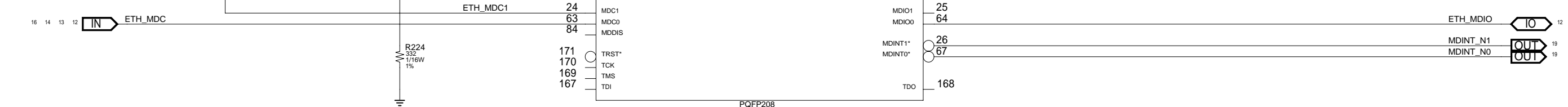


B

MODESEL1	MODESEL0	MODE
0	0	RMII
0	1	SMII
1	0	SS-SMII
1	1	RESERVED



A



SMII CPU INTERFACE



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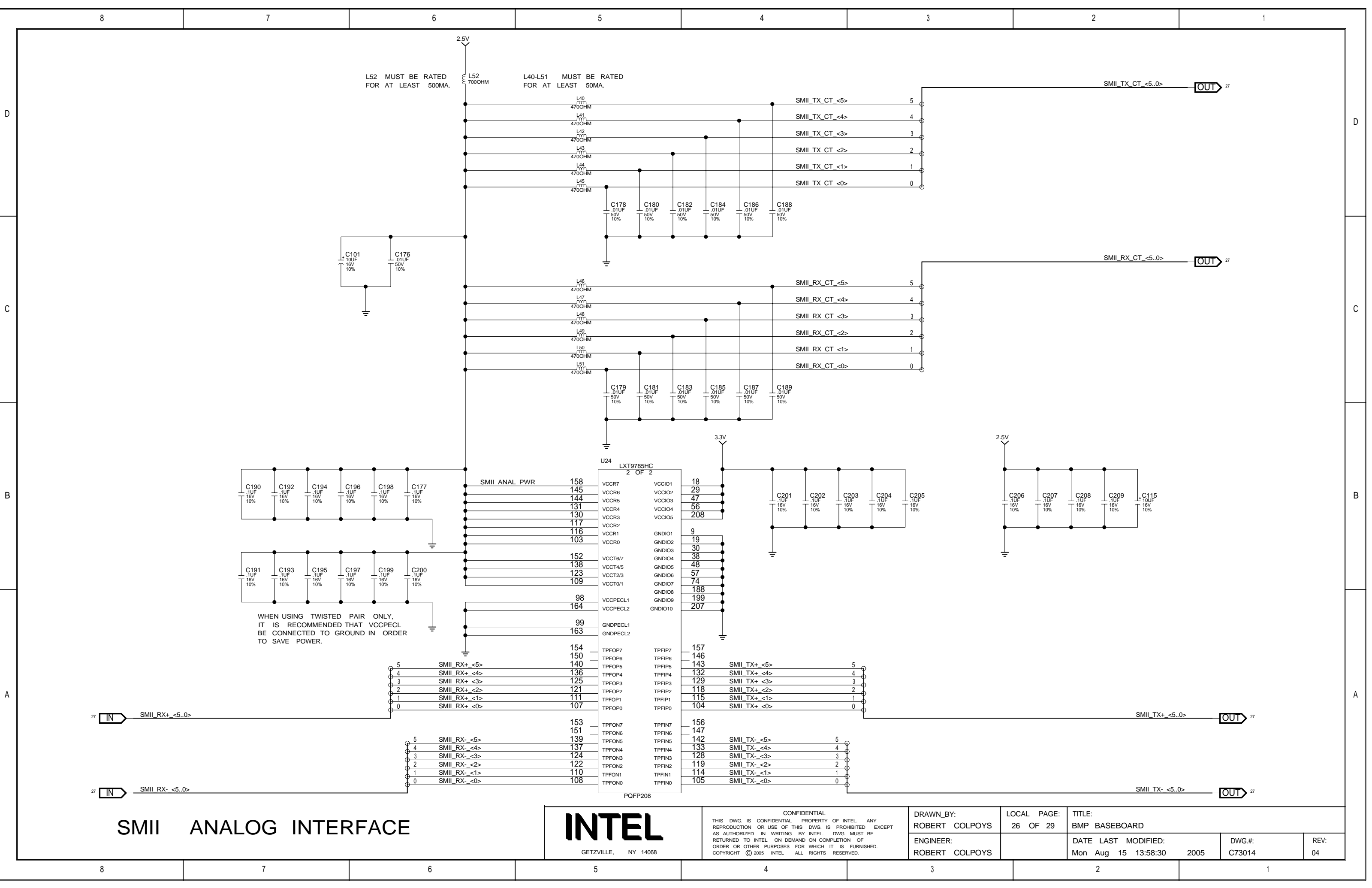
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SMII ANALOG INTERFACE



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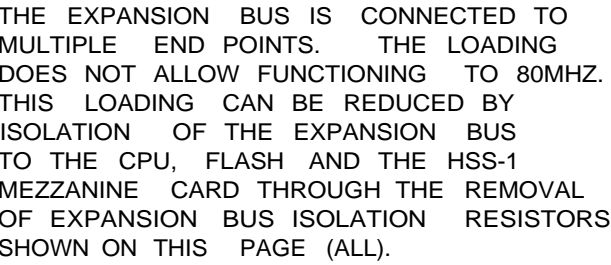
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