Intel® IXDP465 Development Platform

User's Guide

September 2005

Order Number: 306462, Revision: 004
September 2005

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Revision History

Date	Revision	Description
September 2005	004	Corrected document order number; no other changes from 003 version.
August 2005	003	Updates for this release include: • Figure 13: added new figure describing MAC Address Label. • Table 55: rewrote LED definitions to match the silkscreen. • Figure 14: corrected typo for +1.8 V Power LED to make it match the silkscreen. • Section 3.19: updated core voltage references from 1.4 V to 1.5 V for Intel® IXP465 Network Processor at 667 MHz. • Figure 19: updated figure with new voltage regulator and resistor value. • Appendix A: added fis command clarifications. • Added more than 200 document clarifications that resulted from a review cycle of technical, grammar, and overall formatting. (These changes not shown with change bars.)
May 2005	002	Updates for this release include: Added new switch, jumper, and LED figures, revised SMII section, added software-enabled features section in Introduction, added IXP460 and IXP45X emulation section in Overview, updated Appendix A, miscellaneous edits for consistency among headings, captions, etc.
April 2005	001	First edition

Intel® IXDP465 Development Platform Introduction 1

1.1 Purpose

This document provides detailed design information for the Intel® IXDP465 Development Platform.

The IXDP465 platform includes the basic blocks of an Intel® IXP465 Network Processor-based system, including the IXP465 network processor, DDR memory, PCI, and connectors through which UTOPIA level 2, MII, FXS, FXO, T1/E1 and power devices are connected. Several mezzanine cards designed in conjunction with the IXDP465 baseboard plug in through the UTOPIA level 2, MII, or HSS connectors. See Chapter 5, “Mezzanine Card Hardware Design” for detailed information about the design of these mezzanine cards.

1.2 Intended Audience

The intended audience for this document includes hardware architects and developers who are developing both hardware and software for applications based on the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors. The IXDP465 platform is designed (in conjunction with the design of several modules) to meet the market requirements for a flexible customer-oriented platform. This platform demonstrates the IXP465 network processor capabilities in a system and enables IXP465 software development. Customers can base their designs on portions of the IXDP465 platform design.

1.3 Prerequisites

The Intel® IXDP465 Development Platform supports all available features for the Intel® IXP465 Network Processor. Many features, such as the IXP465 network processor engine (NPE) functions, are enabled by a specific revision of the Intel-supplied software.

Refer to Table 2, “Related Intel Documentation” on page 13 for a list of all hardware, software, and platform documents that will assist in the development process. In particular, the following documents provide details on feature availability:

- *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet* has a complete list of available product features.
- *Intel® IXP400 Software Programmer’s Guide* provides information on the features that are enabled in a particular software release.

The IXDP465 platform features that require enabling by software supplied by Intel are summarized in Table 1.

Table 1. Intel® IXDP465 Development Platform Features Summary

Features that do not require enabling software	Features that require enabling software from Intel
Intel XScale® Core -- up to 667 MHz	Cryptography unit (random number generator and exponentiation unit)
PCI v. 2.2 33/66 MHz (Host/Option)	Encryption/Authentication (AES/AES-CCM/3DES/DES/ SHA-1/SHA-256/SHA-384/SHA-512/MD-5
USB 1.1 Device Controller	Two High-Speed Serial (HSS) interfaces
USB 2.0 Host Controller (High-Speed Mode is not supported)	Three Network Processor Engines (NPEs)
DDRI SDRAM interface	Up to three MII interfaces
Master/target capable expansion bus	Up to six SMII interfaces
Two UARTs	One UTOPIA Level 2 interface
Internal Bus Performance Monitoring Unit	IEEE-1588 Hardware Assist
16 GPIOs	
Four internal timers	
Synchronous Serial Protocol (SSP) port	
I^2C interface	
Spread spectrum clocking for reduced EMI	
Packaging • 544-pin PBGA • Commercial/extended temperature • Lead-free support	

It is recommended that users have access to the documents listed in Table 2 and refer to them when necessary. This document does not explore the IXP465 network processor internal architecture, but describes the processor's interfaces to peripherals that are used on the IXDP465 platform. Schematics and a bill of materials are available in the IXDP465 platform documentation kit (zip file) at http://developer.intel.com/design/network/products/npfamily/ixdp465.htm or through your local Intel sales representative.

1.4 Related Documentation

Table 2 and Table 3 list documentation from Intel and from other sources that provide additional information for the development of hardware and software based on the Intel® IXP465 Network Processor.

Table 2. Related Intel Documentation

Title	Document #	Location
Intel® IXDP465 Development Platform Quick Start Guide	305825	IXP4XX Documentation Web Page†
Intel® IXDP465 Development Platform Specification Update	306509	Intel Representative
Intel® IXDP465 Development Platform Documentation Kit	N/A	IXP4XX Documentation Web Page†
Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual	306262	IXP4XX Documentation Web Page†
Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet	306261	IXP4XX Documentation Web Page†
Intel® IXP400 Software Programmer's Guide	252539	IXP4XX Documentation Web Page†
Intel® IXP400 Software Specification Update	273795	IXP4XX Documentation Web Page†
Designing Embedded Networking Applications Essential Insights for Developers of Intel® IXP4XX Network Processor Systems	N/A	http://www.intel.com/intelpress/sum_ixp4.htm
Intel® XScale™ Core Developer's Manual	273473	IXP4XX Documentation Web Page†
Intel StrataFlash® Memory (J3) Datasheet	290667	http://www.intel.com/design/flcomp/products/j3/techdocs.htm
Intel® PRO/100 Desktop Adapter technical documentation	N/A	http://www.intel.com/network/connectivity/products/desktop_adapters.htm
Intel® LXT9785/9785E Fast Ethernet Octal Transceiver Datasheet	249241	http://www.intel.com/design/network/products/lan/docs/lxt9785_docs.htm

† This document is available at: http://www.intel.com/design/network/products/npfamily/docs/ixp4xx.htm

Table 3. Related External Documentation

Title and Revision	Location
PCI Local Bus Specification, Rev. 2.2	http://www.pcisig.com/
MiniPCI Specification, 1.0	http://www.pcisig.com/
UTOPIA Level 2 Specification, Revision 1.0	http://www.atmforum.com/
Universal Serial Bus Specification, Revision 1.1	http://www.usb.org/
JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79D	http://www.jedec.org

1.5 Terminology

Table 4 lists the acronyms and common terms used in this manual.

Table 4. List of Terminology (Sheet 1 of 2)

Acronym	Descriptions
ADSL	Asymmetric Digital Subscriber Line
Assert	Logically active value of a signal or bit
ATM	Asynchronous Transfer Mode
CPE	Customer Premise Equipment
CPLD	Complex Programmable Logic Device
DDR	Double-Data Rate
DMA	Direct Memory Access
DSL	Digital Subscriber Line
E1	Euro 1 trunk line
FPGA	Field Programmable Gate Array
FXO	Foreign Exchange Office
FXS	Foreign Exchange Subscriber
GPIO	General-Purpose Input/Output
HPI	Host-Port Interface
HSS	High-Speed Serial (port)
IP	Internet Protocol
IXP	Internet Exchange Processor
LAN	Local Area Network
LSB	Least-Significant Byte
MAC	Media Access Controller
MDIO	Management Data Input/Output
mezzanine card	A circuit board that attaches to the development platform baseboard and provides additional functionality. Mezzanine cards may be stackable. Also called daughtercard.
MII	Media-Independent Interface
MSB	Most-Significant Byte
NPE	Network Processor Engine
NPM	Network Processor Module
PCI	Peripheral Component Interface
PHY	Physical Layer (Layer 1) Interface
Reserved	A field that may be used by an implementation. Software should not modify reserved fields or depend on any values in reserved fields.
RX	Receive (HSS is receiving from off-chip)
SDRAM	Synchronous Dynamic Random Access Memory
SMII	Serial Media Independent Interface
T1	Type 1 trunk line

Table 4. List of Terminology (Sheet 2 of 2)

Acronym	Descriptions
TDM	Time Division Multiplex
TX	Transmit (HSS is transmitting off-chip)
UART	Universal Asynchronous Receiver-Transmitter
UTOPIA	Universal Test and Operation PHY Interface for ATM
WAN	Wide-Area Network

Intel® IXDP465 Development Platform Overview 2

The Intel® IXDP465 Development Platform consists of a baseboard and network processor module plus add-on mezzanine cards.

The IXDP465 baseboard features are:

- USB connectors (1 Host, 1 Device)
- Two serial ports
- Four PCI slots (for the IXDP465 as a PCI host system)
- One PCI finger (for the IXDP465 as a PCI option card)
- I^2C EEPROM
- Flash memory
- SMII Multi-Pack Interface
- LCD Display and LEDs
- Switches and Jumpers
- Power Regulators and Interface
- Connectors and Standoff provisions to Network Processor Module and all mezzanine cards

The network processor module and mezzanine cards that are delivered as part of the IXDP465 platform are:

- Intel® IXP465 Network Processor/DDR module (x16 memory model)
- One Intel® IXPETM465 Ethernet PHY mezzanine card (used in one of three MII mezzanine slots)

Optional mezzanine cards (purchased separately) include:

- Intel® IXPDSM465 ADSL UTOPIA level 2 mezzanine card

  Note: This card is the same design as the one for the Intel® IXDP425 Development Platform.

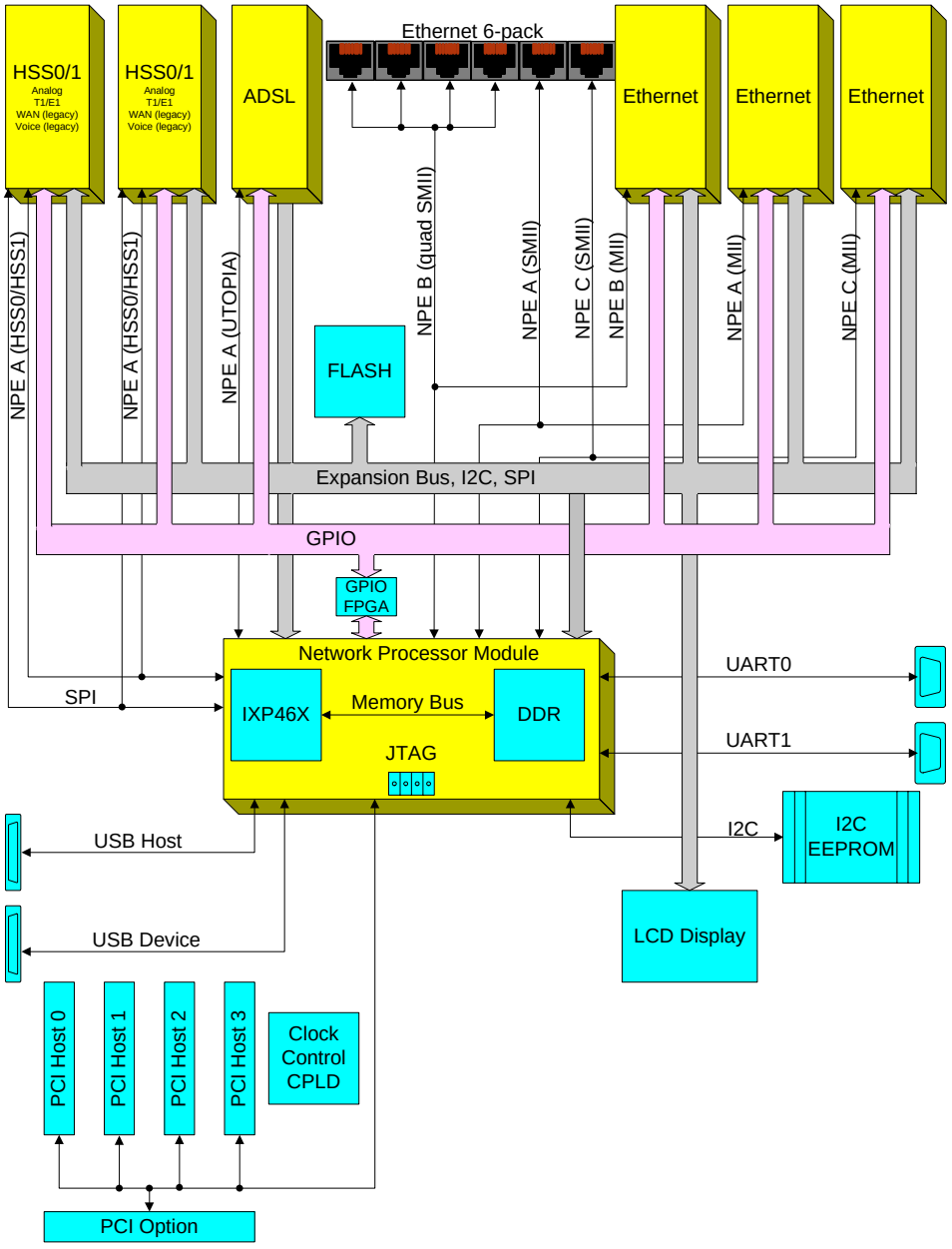
- Intel® IXPVM465 Analog Voice mezzanine card (4-FXS, 1-FXO)
- Intel® IXPFRM465 Quad T1/E1 mezzanine card
- Two additional Intel® IXPETM465 Ethernet PHY mezzanine cards (3 total for the platform)

The following sections describe the features and interfaces on the IXDP465 baseboard and the mezzanine cards in more detail.

2.1 IXDP465 Baseboard

The connections between the devices on the baseboard and mezzanine cards are shown in Figure 1. Details on each device are described in the following sections.

Figure 1. IXDP465 Baseboard Functional Block Diagram



Note: Components in yellow represent separate module and mezzanine assemblies that are external to the IXDP465 baseboard.

2.2 Network Processor Module

The Network Processor Module (NPM) for the Intel® IXDP465 Development Platform is:

- Intel® IXP465 Network Processor/DDR Module (x16 memory model)

See Chapter 4, "Network Processor Module Hardware Design" for details about this NPM.

The IXDP465 platform is used for development of products using the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors. Although the IXDP465 platform is shipped with a fully-featured IXP465 network processor operating at 533 MHz, the platform can be used to develop products that require either an Intel® IXP460 Network Processor or an Intel® IXP455 Network Processor. These processors support subsets of the IXP465 processor features, so certain features on the IXP465 can be disabled through software to emulate the IXP460 and IXP455 processors.

Emulation is accomplished by accessing the **EXP_UNIT_FUSE_RESET** register via software and writing a **1** to the fuse bit number that corresponds to the feature to be disabled. For a full description of this register, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*. (See Table 2 on page 13 for the document order number.)

Table 5 shows the default fuse bit settings for the fully-featured IXP465 network processor. Other rows in the table show the fuse bit settings that can disable a feature to emulate IXP460 or IXP455 network processor operation.

Table 5. Fuse Bit Settings for Network Processor Emulation

	Features of Intel® IXP45X and Intel® IXP46X Product Line of Network Processors																			
Processor	**ECC/1588**	**PCI**	**NPE-C (crypto)**	**NPE-B (no crypto)**	**NPE-A (WAN)**	**Ethernet C (crypto)**	**Ethernet B (no crypto)**	**UTOPIA**	**HSS/HDLC**	**Hash/AES/DES**	**UDC (USB Device)**	**RCOMP_disable**	**Core speed**	**Core speed**	**RSA**	**Ethernet B [1-3]**	**Ethernet A**	**USB Host**	**UCP (phy_limit[1])**	**UCP (phy_limit[0])**
Intel® IXP465 (533 MHz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Intel® IXP460 (533 MHz)	0	0	0	0	1	0	0	1	1	1	0	0	0	0	1	1	1	0	0	0
Intel® IXP455 (533 MHz)	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Fuse Bit Number†	23	22	21	20	19	18	17	16	13	10	9	8	7	6	5	4	3	2	1	0

† Available to software via EXP_UNIT_FUSE_RESET register.

2.3 Mezzanine Cards

Each IXDP465 mezzanine card has two 120-pin connectors associated with it. The first connector, referred to in this document as the **standard connector**, shares the identical pinout as the mezzanine connector developed for the previous generation IXDP425 platform. The standard connector reuses standard signals (such as HSS, MII, Expansion Bus, and Status) thus allowing the IXDP425 mezzanine cards to directly plug into the new IXDP465 platform.

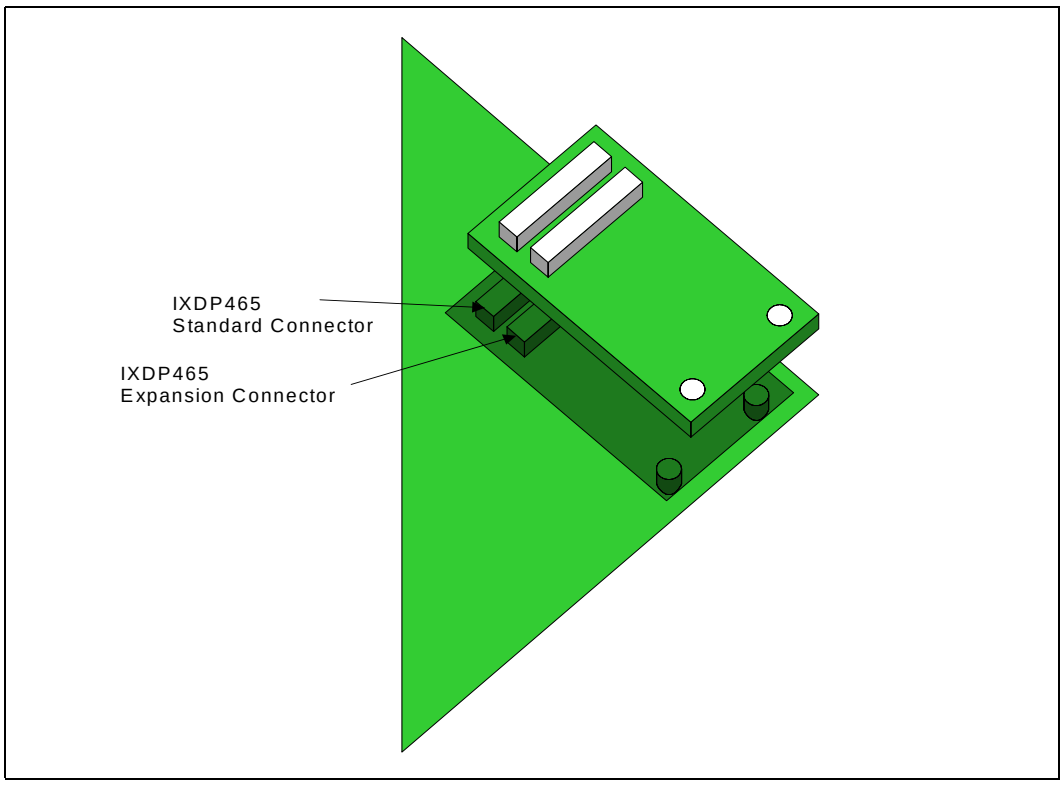
The second connector is for IXDP465-specific features and is referred to in this document as the **expansion connector**. This second connector includes the expansion bus extension, along with SPI, I^2C, and all 16 GPIOs. The IXDP465-specific expansion connector contains a board identification scheme and future expansion signals.

Note: The IXPDSM465 ADSL UTOPIA level 2 mezzanine card uses the standard 120-pin connector only, not the expansion connector, because it is the same card designed for the IXDP425 development platform.

All mezzanine cards supported by the IXDP465 platform can be accessed simultaneously. It is possible to boot and operate the IXDP465 platform over the NPE Ethernet ports with all the mezzanine cards installed and still have access to all test points.

All mezzanine cards are provided with the following voltages: +1.8 V, +2.5 V, +3.3 V, +5.0 V, +12.0 V.

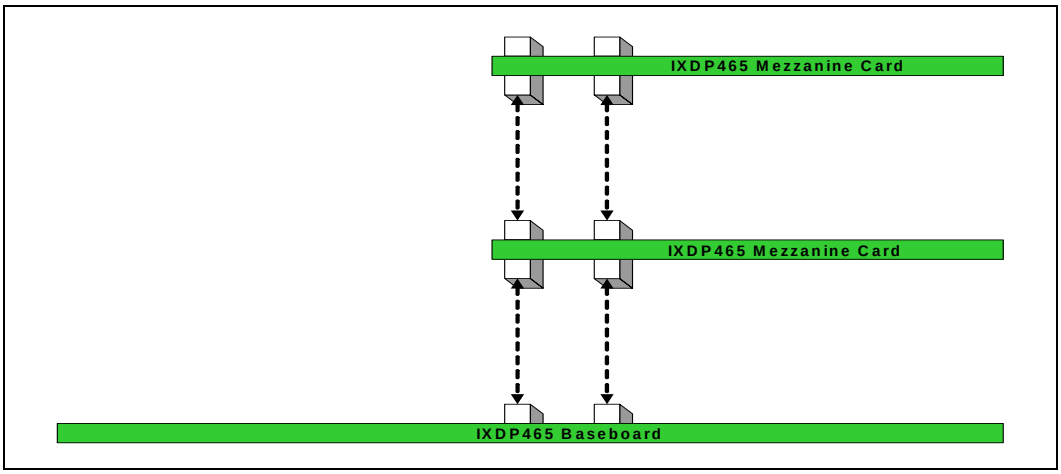
Figure 2. IXDP465 Mezzanine Card Attachment



2.4 Mezzanine Card Stacking

Some IXDP465 mezzanine cards include the ability to stack up to eight cards. This feature requires the mezzanine card to mirror the connectors from the bottom to the top to propagate the signals from the IXDP465 baseboard to each stacked card. Figure 3 shows an example of stacking mezzanine cards two-high.

Figure 3. IXDP465 Mezzanine Card Stacking



2.5 Mezzanine Card Expansion Connector

The mezzanine card expansion connector has IXP465 network processor-specific features, such as the expansion bus extension along with SPI, I^2C, and all 16 General-Purpose Input/Output (GPIOs). This IXP465-specific expansion connector includes a board identification scheme and future expansion signals. Table 6 describes the expansion connector signals that are common across all mezzanine cards. The Legend describing the color-codes for the signals follows the table.

Note: The standard connector signal definitions for each type of mezzanine card are listed in Chapter 5, "Mezzanine Card Hardware Design".

The mezzanine card GPIO signals are routed to the network processor GPIO through the GPIO FPGA as shown in Figure 1. The expansion signals (C_xxx_n) are connected to the network processor expansion signals (for future expansion of processor peripherals).

Table 6. Mezzanine Card Expansion Connector Common Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
+1.8 V	1	C_PCI_4	41	+3.3 V	81
+1.8 V	2	C_PCI_5	42	+3.3 V	82
GND	3	C_PCI_6	43	+3.3 V	83
GND	4	C_PCI_7	44	+3.3 V	84
EX_DATA17	5	C_PCI_8	45	GND	85
EX_DATA16	6	C_PCI_9	46	GND	86
EX_DATA19	7	EX_BE_N3	47	--	87
EX_DATA18	8	EX_BE_N2	48	--	88
GND	9	EX_BE_N1	49	--	89
GND	10	EX_BE_N0	50	--	90
EX_DATA21	11	EX_BURST	51	GND	91
EX_DATA20	12	EX_PAR3	52	GND	92
EX_DATA23	13	EX_PAR2	53	--	93
EX_DATA22	14	EX_PAR1	54	MCE_GPIO5	94

Table 6. Mezzanine Card Expansion Connector Common Signals (Sheet 2 of 2)

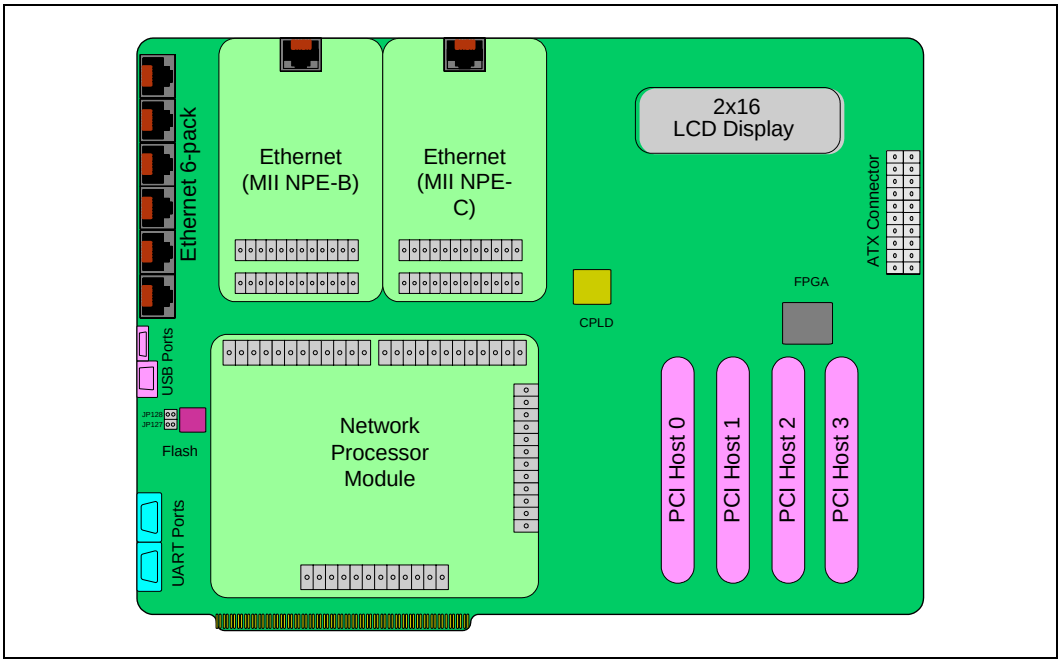
Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	15	EX_PAR0	55	MCE_GPIO6	95
GND	16	C_NPE_0	56	MCE_GPIO7	96
EX_DATA25	17	C_NPE_1	57	GND	97
EX_DATA24	18	C_NPE_2	58	GND	98
EX_DATA27	19	C_NPE_3	59	MCE_GPIO8	99
EX_DATA26	20	C_NPE_4	60	MCE_GPIO9	100
GND	21	C_NPE_5	61	MCE_GPIO10	101
GND	22	C_NPE_6	62	MCE_GPIO11	102
EX_DATA29	23	C_NPE_7	63	GND	103
EX_DATA28	24	C_NPE_8	64	GND	104
EX_DATA31	25	C_NPE_9	65	MCE_GPIO12	105
EX_DATA30	26	C_NPE_10	66	MCE_GPIO13	106
GND	27	C_NPE_11	67	MCE_GPIO14	107
GND	28	C_NPE_12	68	MCE_GPIO15	108
EX_ADDR24	29	CLK32	69	GND	109
SSP_CLK	30	--	70	GND	110
SSP_FRM	31	--	71	ID0	111
SSP_TXD	32	--	72	ID1	112
SSP_RXD	33	--	73	ID2	113
SSP_EXTCLK	34	--	74	ID3	114
+5.0 V	35	--	75	ID4	115
+5.0 V	36	--	76	ID5	116
C_PCI_0	37	--	77	ID6	117
C_PCI_1	38	--	78	ID7	118
C_PCI_2	39	--	79	I2C_SDA	119
C_PCI_3	40	--	80	I2C_SCL	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
SPI signals	blue
mezzanine card GPIO signals	maroon
expansion signals (C_xxx_n)	black
mezzanine card ID signals	red
I^2C signals	gray
32.768 MHz clock signal	gold

2.6 Component Placement Diagrams

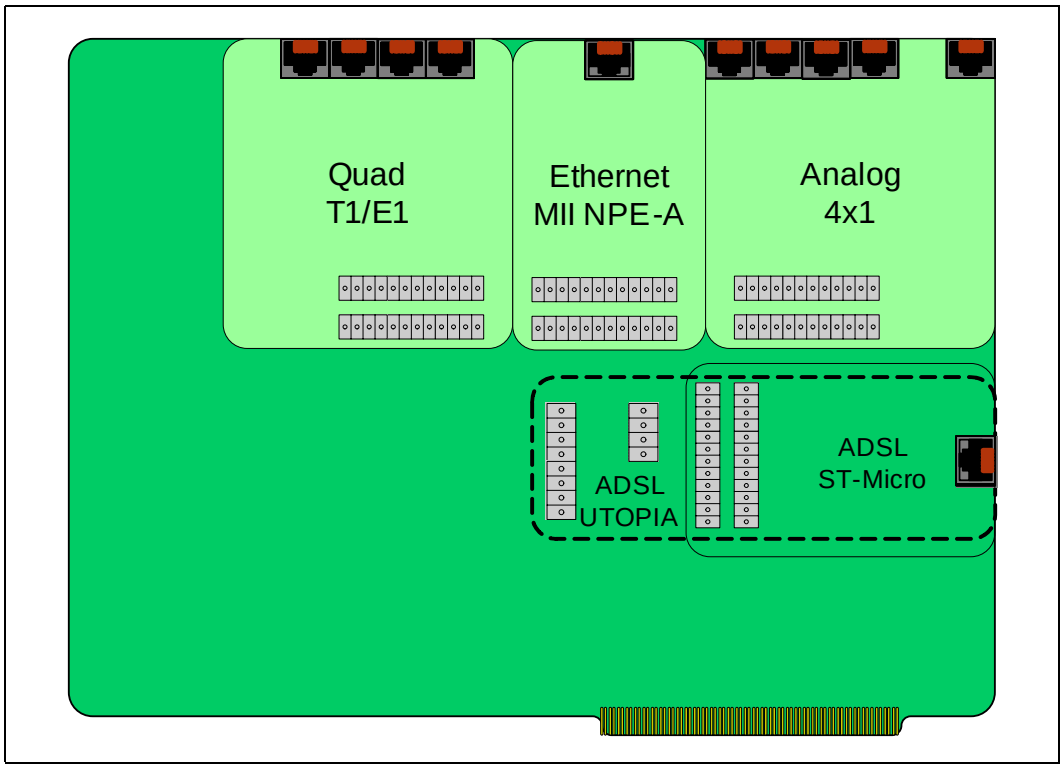
Figure 4 and Figure 5 show the placement drawings for the top and bottom of the IXDP465 platform.

Figure 4. IXDP465 Development Platform Components (Top View)



Note: Figure 5 displays two options for ADSL cards. Either a UTOPIA or ST-Micro mezzanine card may be installed in the appropriate connector slot.

Figure 5. IXDP465 Development Platform Components (Bottom View)



IXDP465 Baseboard Hardware Design 3

This chapter covers the design details of all interfaces, components and features contained on the Intel® IXDP465 Development Platform baseboard.

3.1 Network Processor Module Interface

The interface to the Network Processor Module (NPM) for the Intel® IXDP465 Development Platform is provisioned on the baseboard assembly using four 120-pin connectors for the signaling and power requirements. These connectors are low-profile, 13mm stack height, surface mount connectors with center ground planes. The connectors support NPEs and peripherals, the expansion bus, the PCI bus, and one connector which is reserved for future needs. See Chapter 4, "Network Processor Module Hardware Design" for full details of the NPM interface connectors and pinouts.

For more information about the IXP465 network processor, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

3.2 PCI Interface

The IXDP465 platform (baseboard and network processor module) can function as a four-port PCI host or as a PCI option card. When plugged into a PCI slot as an option card, the IXDP465 baseboard senses that it is plugged in and automatically reverts to Option mode (bootstraps using one of the option slot grounds).

The PCI architecture is shown in Figure 6. A set of isolation buffers placed between the IXP465 network processor and the four PCI host connectors ensures that PCI trace routing lengths are not violated in Option mode. These buffers are placed in a high impedance state when the board recognizes it has been installed as an option card. No soldering or rework is required to change from Host to Option mode.

There are four 3.3 V slots capable of holding full length PCI 2.2 cards. PCI-to-miniPCI converters support miniPCI cards on the platform. When configured as a 4-port PCI host, the IXDP465 baseboard slots can operate at either 66 MHz or 33 MHz.

When the IXDP465 baseboard is the PCI host, resets are driven to the PCI devices from the IXDP465 platform reset circuit. When the IXDP465 baseboard is a PCI option device, resets are driven to the IXDP465 platform through the PCI option fingers.

The IXDP465 platform has LEDs that indicate the PCI interface status. Table 7 describes the PCI LEDs. See Figure 14 on page 82 for the LED locations on the board.

Figure 6. PCI Architecture

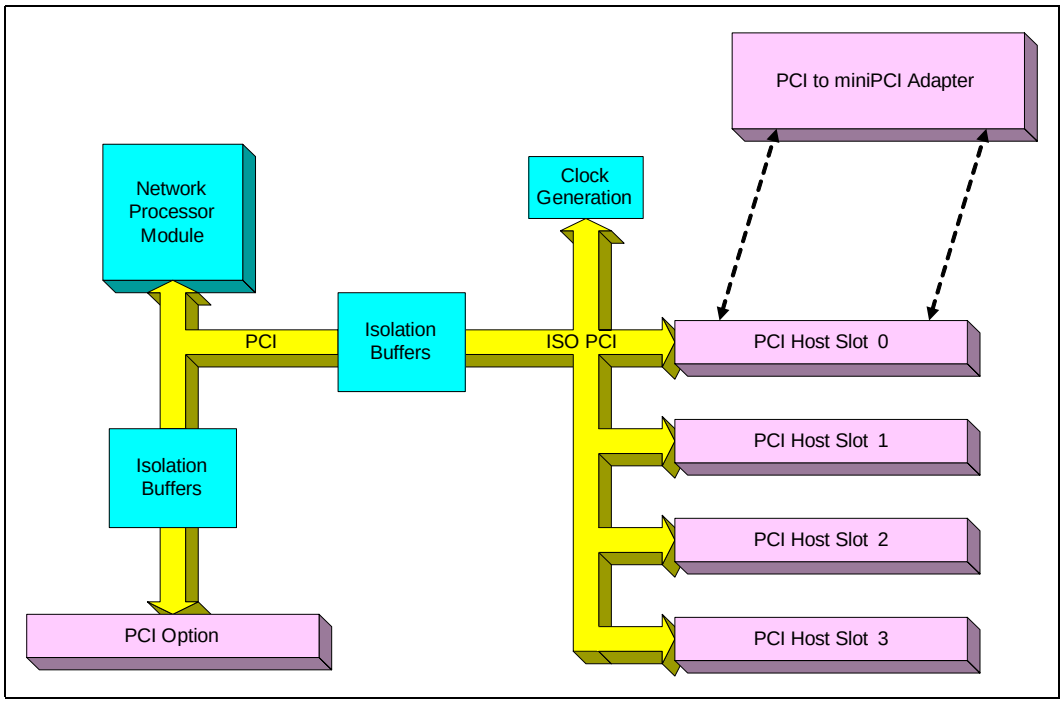


Table 7. PCI LED Indicators

LED	LED Indication When ON	Color
PCI Host	PCI is in host mode	Green
PCI Option	PCI is in option mode	Green
PCI 66 MHz	PCI is 66 MHz (host mode only)	Green
PCI 33 MHz	PCI is 33 MHz (host mode only)	Green

3.2.1 PCI Signal Naming Conventions

Table 8 describes how the PCI bus is divided into three distinct sections for naming convention purposes. These conventions are also used for naming the signals in the IXDP465 platform schematics.

Table 8. PCI Signal Naming Conventions

PCI Section	PCI Signal Naming for Section
PCI host slots (1-4)	PCI_HOST_abc…xyz
PCI option fingers	PCI_OPT_abc…xyz
PCI connection to the processor	PCI_CPU_abc…xyz
Note: abc…xyz represents the signal name from the PCI specification.	

3.2.2 PCI Mode of Operation Selection

The PCI mode of operation is automatically sensed by the clock control CPLD. See Section 3.22.4, PCI Option Sensing for more detailed information.

3.2.3 PCI Clocking

A CPLD (Complex Programmable Logic Device) controls the PCI clock. In Option mode, the PCI clock is generated by the host (through the PCI finger) and the CPLD drives the PCI clock output to logic 1 to reduce noise. In Host mode, the CPLD drives the PCI clock.

The CPLD monitors the M66EN signals from the four slots and automatically sets up the proper clock frequency. If all slots are 66 MHz capable, the CPLD selects the 66 MHz clock. If any slots are not 66 MHz capable, the CPLD selects the 33 MHz clock. A 66 MHz oscillator clocks the CPLD.

A four-port zero delay buffer (Cypress CY2305*) drives the four PCI slot clocks and the network processor module PCI clock. When the IXDP465 baseboard is in Option mode, the CPLD drives the four PCI slot clock outputs to logic 1 to reduce noise.

CPLD programming is accomplished through the CPLD JTAG Programming Header. See Figure 15 for the location and settings of the JTAG Emulator and CPLD Programming Headers.

For an overall memory address map and the expansion bus memory map for the IXDP465 platform, see Section 3.3.5, Expansion Bus Address Map.

3.2.4 PCI Host Mode Operation

The IXDP465 baseboard supports four external 32-bit PCI devices (3.3 V only) when configured as a PCI host. Both 33 MHz and 66 MHz PCI bus operation are supported. In PCI host mode, the IXDP465 baseboard supports up to four PCI expander cards in PCI slots. In PCI option mode, the IXDP465 baseboard baseboard is plugged into a standard PCI backplane through a card edge connection on the board. (See Section 3.2.5, PCI Option Mode Operation for details.)

See the following tables for pin assignment details:

- Table 10, “PCI Host Slot-0 Pin Assignments” on page 28
- Table 11, “PCI Host Slot-1 Pin Assignments” on page 29
- Table 12, “PCI Host Slot-2 Pin Assignments” on page 30
- Table 13, “PCI Host Slot-3 Pin Assignments” on page 31

In Host mode, the IDSEL signals on the PCI slots are connected to the PCI_AD bus as listed in Table 9. When the IXDP465 baseboard is an option device, the IDSEL is driven straight out of the PCI option connector to the IXDP465 baseboard.

Table 9. IDSEL Mappings

Device	IDSEL Signal
Slot 0 (Host mode)	PCI_AD31
Slot 1 (Host mode)	PCI_AD30
Slot 2 (Host mode)	PCI_AD29
Slot 3 (Host mode)	PCI_AD28
IXDP465 baseboard (Option mode)	PCI_IDSEL

Note: The PCI IDSEL signals for the IXDP465 baseboard are the same as those used on the baseboard (IXMB425) for the IXDP425 development platform.

Table 10. PCI Host Slot-0 Pin Assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	PCI_HST_TRST_N0	A33	3.3 V	B1	PCI_-12V_N0	B33	PCI_HST_CBE_N2
A2	12.0 V	A34	PCI_HST_FRAME_N	B2	PCI_HST_TCK0	B34	GND
A3	PCI_HST_TMS0	A35	GND	B3	GND	B35	PCI_HST_IRDY_N
A4	PCI_HST_TDI0	A36	PCI_HST_TRDY_N	B4	PCI_HST_TDO0	B36	3.3 V
A5	5.0 V	A37	GND	B5	5.0 V	B37	PCI_HST_DEVSEL_N
A6	PCI_HST_INTA_N	A38	PCI_HST_STOP_N	B6	5.0 V	B38	GND
A7	PCI_HST_INTC_N	A39	3.3 V	B7	PCI_HST_INTB_N	B39	PCI_HST_LOCK_N
A8	5.0 V	A40	PCI_HST_SMBCLK0	B8	PCI_HST_INTD_N	B40	PCI_HST_PERR_N
A9	-	A41	PCI_HST_SMBDAT0	B9	PCI_HST_PRSNT1_N0	B41	3.3 V
A10	3.3 V	A42	GND	B10	-	B42	PCI_HST_SERR_N
A11	-	A43	PCI_HST_PAR	B11	PCI_HST_PRSNT2_N0	B43	3.3 V
A14	-	A44	PCI_HST_AD15	B14	-	B44	PCI_HST_CBE_N1
A15	PCI_HST_RST_N	A45	3.3 V	B15	GND	B45	PCI_HST_AD14
A16	3.3 V	A46	PCI_HST_AD13	B16	PCI_HST_CLK0	B46	GND
A17	PCI_HST_GNT_N0	A47	PCI_HST_AD11	B17	GND	B47	PCI_HST_AD12
A18	GND	A48	GND	B18	PCI_HST_REQ_N0	B48	PCI_HST_AD10
A19	-	A49	PCI_HST_AD9	B19	3.3 V	B49	PCI_HST_M66EN0
A20	PCI_HST_AD30	A50	GND	B20	PCI_HST_AD31	B50	GND
A21	3.3 V	A51	GND	B21	PCI_HST_AD29	B51	GND
A22	PCI_HST_AD28	A52	PCI_HST_CBE_N0	B22	GND	B52	PCI_HST_AD8
A23	PCI_HST_AD26	A53	3.3 V	B23	PCI_HST_AD27	B53	PCI_HST_AD7
A24	GND	A54	PCI_HST_AD6	B24	PCI_HST_AD25	B54	3.3 V
A25	PCI_HST_AD24	A55	PCI_HST_AD4	B25	3.3 V	B55	PCI_HST_AD5
A26	PCI_HST_IDSEL0	A56	GND	B26	PCI_HST_CBE_N3	B56	PCI_HST_AD3
A27	3.3 V	A57	PCI_HST_AD2	B27	PCI_HST_AD23	B57	GND
A28	PCI_HST_AD22	A58	PCI_HST_AD0	B28	GND	B58	PCI_HST_AD1
A29	PCI_HST_AD20	A59	3.3 V	B29	PCI_HST_AD21	B59	3.3 V

Table 10. PCI Host Slot-0 Pin Assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A30	GND	A60	PCI_HST_REQ64_N0	B30	PCI_HST_AD19	B60	PCI_HST_ACK64_N0
A31	PCI_HST_AD18	A61	5.0 V	B31	3.3 V	B61	5.0 V
A32	PCI_HST_AD16	A62	5.0 V	B32	PCI_HST_AD17	B62	5.0 V

For PCB designs that use PCI Host slots, the following Host slot 0 signals need pull-up resistors attached:

PCI_HST_TMS0	PCI_HST_TDI0	PCI_HST_INTA_N	PCI_HST_INTB_N
PCI_HST_INTC_N	PCI_HST_INTD_N	PCI_HST_INTD_N	PCI_HST_TRDY_N
PCI_HST_STOP_N	PCI_HST_SMBCLK0	PCI_HST_SMBDAT0	PCI_HST_PRSNT1_N
PCI_HST_PRSNT2_N	PCI_HST_IRDY_N	PCI_HST_DEVSEL_N	PCI_HST_LOCK_N
PCI_HST_PERR_N	PCI_HST_SERR_N	PCI_HST_M66EN0	PCI_HST_ACK64_N0
PCI_HST_REQ64_N0	PCI_HST_REQ_N0		

For PCB designs that use PCI Host slots, the following Host slot 0 signals need pull-down resistors attached:

PCI_HST_TRST_N0	PCI_HST_RST_N	PCI_HST_TCK0

Table 11. PCI Host Slot-1 Pin Assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	PCI_HST_TRST_N1	A33	3.3 V	B1	PCI_-12V_N1	B33	PCI_HST_CBE_N2
A2	12.0 V	A34	PCI_HST_FRAME_N	B2	PCI_HST_TCK1	B34	GND
A3	PCI_HST_TMS1	A35	GND	B3	GND	B35	PCI_HST_IRDY_N
A4	PCI_HST_TDI1	A36	PCI_HST_TRDY_N	B4	PCI_HST_TDO1	B36	3.3 V
A5	5.0 V	A37	GND	B5	5.0 V	B37	PCI_HST_DEVSEL_N
A6	PCI_HST_INTA_N	A38	PCI_HST_STOP_N	B6	5.0 V	B38	GND
A7	PCI_HST_INTC_N	A39	3.3 V	B7	PCI_HST_INTB_N	B39	PCI_HST_LOCK_N
A8	5.0 V	A40	PCI_HST_SMBCLK1	B8	PCI_HST_INTD_N	B40	PCI_HST_PERR_N
A9	-	A41	PCI_HST_SMBDAT1	B9	PCI_HST_PRSNT1_N1	B41	3.3 V
A10	3.3 V	A42	GND	B10	-	B42	PCI_HST_SERR_N
A11	-	A43	PCI_HST_PAR	B11	PCI_HST_PRSNT2_N1	B43	3.3 V
A14	-	A44	PCI_HST_AD15	B14	-	B44	PCI_HST_CBE_N1
A15	PCI_HST_RST_N	A45	3.3 V	B15	GND	B45	PCI_HST_AD14
A16	3.3 V	A46	PCI_HST_AD13	B16	PCI_HST_CLK1	B46	GND
A17	PCI_HST_GNT_N1	A47	PCI_HST_AD11	B17	GND	B47	PCI_HST_AD12
A18	GND	A48	GND	B18	PCI_HST_REQ_N1	B48	PCI_HST_AD10
A19	-	A49	PCI_HST_AD9	B19	3.3 V	B49	PCI_HST_M66EN1
A20	PCI_HST_AD30	A50	GND	B20	PCI_HST_AD31	B50	GND

Table 11. PCI Host Slot-1 Pin Assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A21	3.3 V	A51	GND	B21	PCI_HST_AD29	B51	GND
A22	PCI_HST_AD28	A52	PCI_HST_CBE_N0	B22	GND	B52	PCI_HST_AD8
A23	PCI_HST_AD26	A53	3.3 V	B23	PCI_HST_AD27	B53	PCI_HST_AD7
A24	GND	A54	PCI_HST_AD6	B24	PCI_HST_AD25	B54	3.3 V
A25	PCI_HST_AD24	A55	PCI_HST_AD4	B25	3.3 V	B55	PCI_HST_AD5
A26	PCI_HST_IDSEL1	A56	GND	B26	PCI_HST_CBE_N3	B56	PCI_HST_AD3
A27	3.3 V	A57	PCI_HST_AD2	B27	PCI_HST_AD23	B57	GND
A28	PCI_HST_AD22	A58	PCI_HST_AD0	B28	GND	B58	PCI_HST_AD1
A29	PCI_HST_AD20	A59	3.3 V	B29	PCI_HST_AD21	B59	3.3 V
A30	GND	A60	PCI_HST_REQ64_N1	B30	PCI_HST_AD19	B60	PCI_HST_ACK64_N1
A31	PCI_HST_AD18	A61	5.0 V	B31	3.3 V	B61	5.0 V
A32	PCI_HST_AD16	A62	5.0 V	B32	PCI_HST_AD17	B62	5.0 V

For PCB designs that use PCI Host slots, the following Host slot 1 signals need pull-up resistors attached:

PCI_HST_TMS1	PCI_HST_TDI1	PCI_HST_SMBCLK1	PCI_HST_SMBDAT1
PCI_HST_REQ64_N1	PCI_HST_PRSNT1_N	PCI_HST_PRSNT2_N	PCI_HST_REQ_N1
PCI_HST_M66EN1	PCI_HST_ACK64_N1		

For PCB designs that use PCI Host slots, the following Host slot 1 signals need pull-down resistors attached:

PCI_HST_TRST_N1 PCI_HST_TCK1

Table 12. PCI Host Slot-2 Pin Assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	PCI_HST_TRST_N2	A33	3.3 V	B1	PCI_-12V_N2	B33	PCI_HST_CBE_N2
A2	12.0 V	A34	PCI_HST_FRAME_N	B2	PCI_HST_TCK2	B34	GND
A3	PCI_HST_TMS2	A35	GND	B3	GND	B35	PCI_HST_IRDY_N
A4	PCI_HST_TDI2	A36	PCI_HST_TRDY_N	B4	PCI_HST_TDO2	B36	3.3 V
A5	5.0 V	A37	GND	B5	5.0 V	B37	PCI_HST_DEVSEL_N
A6	PCI_HST_INTA_N	A38	PCI_HST_STOP_N	B6	5.0 V	B38	GND
A7	PCI_HST_INTC_N	A39	3.3 V	B7	PCI_HST_INTB_N	B39	PCI_HST_LOCK_N
A8	5.0 V	A40	PCI_HST_SMBCLK2	B8	PCI_HST_INTD_N	B40	PCI_HST_PERR_N
A9	-	A41	PCI_HST_SMBDAT2	B9	PCI_HST_PRSNT1_N2	B41	3.3 V
A10	3.3 V	A42	GND	B10	-	B42	PCI_HST_SERR_N
A11	-	A43	PCI_HST_PAR	B11	PCI_HST_PRSNT2_N2	B43	3.3 V
A14	-	A44	PCI_HST_AD15	B14	-	B44	PCI_HST_CBE_N1

Table 12. PCI Host Slot-2 Pin Assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A15	PCI_HST_RST_N	A45	3.3 V	B15	GND	B45	PCI_HST_AD14
A16	3.3 V	A46	PCI_HST_AD13	B16	PCI_HST_CLK2	B46	GND
A17	PCI_HST_GNT_N2	A47	PCI_HST_AD11	B17	GND	B47	PCI_HST_AD12
A18	GND	A48	GND	B18	PCI_HST_REQ_N2	B48	PCI_HST_AD10
A19	-	A49	PCI_HST_AD9	B19	3.3 V	B49	PCI_HST_M66EN2
A20	PCI_HST_AD30	A50	GND	B20	PCI_HST_AD31	B50	GND
A21	3.3 V	A51	GND	B21	PCI_HST_AD29	B51	GND
A22	PCI_HST_AD28	A52	PCI_HST_CBE_N0	B22	GND	B52	PCI_HST_AD8
A23	PCI_HST_AD26	A53	3.3 V	B23	PCI_HST_AD27	B53	PCI_HST_AD7
A24	GND	A54	PCI_HST_AD6	B24	PCI_HST_AD25	B54	3.3 V
A25	PCI_HST_AD24	A55	PCI_HST_AD4	B25	3.3 V	B55	PCI_HST_AD5
A26	PCI_HST_IDSEL2	A56	GND	B26	PCI_HST_CBE_N3	B56	PCI_HST_AD3
A27	3.3 V	A57	PCI_HST_AD2	B27	PCI_HST_AD23	B57	GND
A28	PCI_HST_AD22	A58	PCI_HST_AD0	B28	GND	B58	PCI_HST_AD1
A29	PCI_HST_AD20	A59	3.3 V	B29	PCI_HST_AD21	B59	3.3 V
A30	GND	A60	PCI_HST_REQ64_N2	B30	PCI_HST_AD19	B60	PCI_HST_ACK64_N2
A31	PCI_HST_AD18	A61	5.0 V	B31	3.3 V	B61	5.0 V
A32	PCI_HST_AD16	A62	5.0 V	B32	PCI_HST_AD17	B62	5.0 V

For PCB designs that use PCI Host slots, the following Host slot 2 signals need pull-up resistors attached:

PCI_HST_TMS2	PCI_HST_TDI2	PCI_HST_SMBCLK2	PCI_HST_SMBDAT2
PCI_HST_REQ64_N2	PCI_HST_PRSNT2_N	PCI_HST_PRSNT2_N	PCI_HST_REQ_N2
PCI_HST_M66EN2	PCI_HST_ACK64_N2		

For PCB designs that use PCI Host slots, the following Host slot 2 signals need pull-down resistors attached:

PCI_HST_TRST_N2 PCI_HST_TCK2

Table 13. PCI Host Slot-3 Pin Assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	PCI_HST_TRST_N3	A33	3.3 V	B1	PCI_-12V_N3	B33	PCI_HST_CBE_N2
A2	12.0 V	A34	PCI_HST_FRAME_N	B2	PCI_HST_TCK3	B34	GND
A3	PCI_HST_TMS3	A35	GND	B3	GND	B35	PCI_HST_IRDY_N
A4	PCI_HST_TDI3	A36	PCI_HST_TRDY_N	B4	PCI_HST_TDO3	B36	3.3 V
A5	5.0 V	A37	GND	B5	5.0 V	B37	PCI_HST_DEVSEL_N
A6	PCI_HST_INTA_N	A38	PCI_HST_STOP_N	B6	5.0 V	B38	GND

Table 13. PCI Host Slot-3 Pin Assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A7	PCI_HST_INTC_N	A39	3.3 V	B7	PCI_HST_INTB_N	B39	PCI_HST_LOCK_N
A8	5.0 V	A40	PCI_HST_SMBCLK3	B8	PCI_HST_INTD_N	B40	PCI_HST_PERR_N
A9	-	A41	PCI_HST_SMBDAT3	B9	PCI_HST_PRSNT1_N3	B41	3.3 V
A10	3.3 V	A42	GND	B10	-	B42	PCI_HST_SERR_N
A11	-	A43	PCI_HST_PAR	B11	PCI_HST_PRSNT2_N3	B43	3.3 V
A14	-	A44	PCI_HST_AD15	B14	-	B44	PCI_HST_CBE_N1
A15	PCI_HST_RST_N	A45	3.3 V	B15	GND	B45	PCI_HST_AD14
A16	3.3 V	A46	PCI_HST_AD13	B16	PCI_HST_CLK3	B46	GND
A17	PCI_HST_GNT_N3	A47	PCI_HST_AD11	B17	GND	B47	PCI_HST_AD12
A18	GND	A48	GND	B18	PCI_HST_REQ_N3	B48	PCI_HST_AD10
A19	-	A49	PCI_HST_AD9	B19	3.3 V	B49	PCI_HST_M66EN3
A20	PCI_HST_AD30	A50	GND	B20	PCI_HST_AD31	B50	GND
A21	3.3 V	A51	GND	B21	PCI_HST_AD29	B51	GND
A22	PCI_HST_AD28	A52	PCI_HST_CBE_N0	B22	GND	B52	PCI_HST_AD8
A23	PCI_HST_AD26	A53	3.3 V	B23	PCI_HST_AD27	B53	PCI_HST_AD7
A24	GND	A54	PCI_HST_AD6	B24	PCI_HST_AD25	B54	3.3 V
A25	PCI_HST_AD24	A55	PCI_HST_AD4	B25	3.3 V	B55	PCI_HST_AD5
A26	PCI_HST_IDSEL3	A56	GND	B26	PCI_HST_CBE_N3	B56	PCI_HST_AD3
A27	3.3 V	A57	PCI_HST_AD2	B27	PCI_HST_AD23	B57	GND
A28	PCI_HST_AD22	A58	PCI_HST_AD0	B28	GND	B58	PCI_HST_AD1
A29	PCI_HST_AD20	A59	3.3 V	B29	PCI_HST_AD21	B59	3.3 V
A30	GND	A60	PCI_HST_REQ64_N3	B30	PCI_HST_AD19	B60	PCI_HST_ACK64_N3
A31	PCI_HST_AD18	A61	5.0 V	B31	3.3 V	B61	5.0 V
A32	PCI_HST_AD16	A62	5.0 V	B32	PCI_HST_AD17	B62	5.0 V

For PCB designs that use PCI Host slots, the following Host slot 3 signals need pull-up resistors attached:

PCI_HST_TMS3	PCI_HST_TDI3	PCI_HST_SMBCLK3	PCI_HST_SMBDAT3
PCI_HST_REQ64_N3	PCI_HST_PRSNT3_N	PCI_HST_PRSNT2_N	PCI_HST_REQ_N3
PCI_HST_M66EN3	PCI_HST_ACK64_N3		

For PCB designs that use PCI Host slots, the following Host slot 3 signals need pull-down resistors attached:

PCI_HST_TRST_N3	PCI_HST_TCK3

3.2.5 PCI Option Mode Operation

In PCI option mode, the IXDP465 baseboard is plugged into a standard PCI backplane through a card edge connection on the board. When the IXDP465 baseboard is an Option device, the PCI slots and all associated circuitry are not accessible. The isolation buffers are tri-stated and do not allow access to the four PCI host slots. Isolation buffers are placed between the IXP465 network processor and the PCI fingers to allow for support of Universal PCI.

A mini-PCI interface is achieved through a PCI-to-miniPCI adapter card to allow capabilities such as wireless LAN (for example, 802.11 a or b). PCI version 2.2 is used.

In Option mode, the IXDP465 baseboard can still receive its power from the ATX power supply connected to the baseboard and not use the PCI power. This feature eliminates both non-compliance with the PCI power rails and also any issues related to PCI power limitations. The external power must be applied before the PCI host power is applied.

The isolation buffers are disabled until PCI host power is recognized to remove the possibility of the IXDP465 baseboard trying to power up the PCI host (indirectly through the PCI interface).

Table 14. PCI Option Fingers Pin Assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	-	A32	PCI_OPT_AD16	B1	-	B32	PCI_OPT_AD17
A2	-	A33	PCI_3.3V	B2	-	B33	PCI_OPT_CBE_N2
A3	-	A34	PCI_OPT_FRAME_N	B3	GND	B34	GND
A4	PCI_OPT_JTAG_CHN	A35	GND	B4	PCI_OPT_JTAG_CHN	B35	PCI_OPT_IRDY_N
A5	-	A36	PCI_OPT_TRDY_N	B5	-	B36	PCI_3.3V
A6	PCI_OPT_INTA_N	A37	GND	B6	-	B37	PCI_OPT_DEVSEL_N
A7	PCI_OPT_INTC_N	A38	PCI_OPT_STOP_N	B7	PCI_OPT_INTB_N	B38	GND
A8	-	A39	PCI_3.3V	B8	PCI_OPT_INTD_N	B39	PCI_OPT_LOCK_N
A9	-	A40	PCI_OPT_SMBCLK	B9	PCI_OPT_PRSNT1_N	B40	PCI_OPT_PERR_N
A10	-	A41	PCI_OPT_SMBDAT	B10	-	B41	PCI_3.3V
A11	-	A42	GND	B11	PCI_OPT_PRSNT2_N	B42	PCI_OPT_SERR_N
A14	-	A43	PCI_OPT_PAR	B14	-	B43	PCI_3.3V
A15	PCI_OPT_RST_N	A44	PCI_OPT_AD15	B15	GND	B44	PCI_OPT_CBE_N1
A16	-	A45	PCI_3.3V	B16	PCI_OPT_CLK	B45	PCI_OPT_AD14
A17	PCI_OPT_GNT_N	A46	PCI_OPT_AD13	B17	GND	B46	GND
A18	GND	A47	PCI_OPT_AD11	B18	PCI_OPT_REQ_N	B47	PCI_OPT_AD12
A19	-	A48	GND	B19	-	B48	PCI_OPT_AD10
A20	PCI_OPT_AD30	A49	PCI_OPT_AD9	B20	PCI_OPT_AD31	B49	PCI_OPT_M66EN
A21	PCI_3.3V	A52	PCI_OPT_CBE_N0	B21	PCI_OPT_AD29	B52	PCI_OPT_AD8
A22	PCI_OPT_AD28	A53	PCI_3.3V	B22	GND	B53	PCI_OPT_AD7
A23	PCI_OPT_AD26	A54	PCI_OPT_AD6	B23	PCI_OPT_AD27	B54	PCI_3.3V
A24	GND	A55	PCI_OPT_AD4	B24	PCI_OPT_AD25	B55	PCI_OPT_AD5
A25	PCI_OPT_AD24	A56	GND	B25	PCI_3.3V	B56	PCI_OPT_AD3
A26	PCI_OPT_IDSEL	A57	PCI_OPT_AD2	B26	PCI_OPT_CBE_N3	B57	PCI_OPT_GND

Table 14. PCI Option Fingers Pin Assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A27	PCI_3.3V	A58	PCI_OPT_AD0	B27	PCI_OPT_AD23	B58	PCI_OPT_AD1
A28	PCI_OPT_AD22	A59	-	B28	GND	B59	-
A29	PCI_OPT_AD20	A60	PCI_OPT_REQ64_N	B29	PCI_OPT_AD21	B60	PCI_OPT_ACK64_N
A30	GND	A61	-	B30	PCI_OPT_AD19	B61	-
A31	PCI_OPT_AD18	A62	-	B31	PCI_3.3V	B62	-

Pull-up resistors are required for the following PCI Option signals:

PCI_OPT_INTB_N PCI_OPT_INTC_N PCI_OPT_INTD_N PCI_OPT_SMBCLK
PCI_OPT_SMBDAT

3.3 Expansion Bus

3.3.1 Expansion Bus Loading

The IXDP465 platform has been tuned to drive up to eight loads, but the devices on the expansion bus may not be able to quickly drive such a large load. To compensate for this, timings on the expansion bus are adjusted using network processor internal registers. If an edge rises slowly due to low drive strength, the IXP465 network processor must wait an extra cycle before the value is read. There are no buffers to increase drive strength on the expansion bus, although customers can choose to add buffers in their own designs.

To test the maximum performance of the expansion bus (80 MHz), there is a set of isolation resistors (0 Ω) on the expansion bus. All isolation resistors are identified on one of the last pages of the baseboard schematics provided in the IXDP465 documentation kit. The resistors break the expansion bus into two sections. Removal of these resistors will reduce the expansion bus load. When removed, the only devices on the expansion bus are the HSS-1 mezzanine card connectors, flash, and configuration switches.

3.3.2 Expansion Bus Configuration Straps

The expansion bus address lines (**EX_ADDR24 - EX_ADDR0**) are used for configuration strapping options during boot-up. At the de-assertion of reset, the values on these lines are read to determine the board configuration. The defined configuration strapping is shown in Table 15.

The expansion bus address lines are connected to DIP switches (SW3, SW4, and SW5 in Figure 7) allowing a line to be pulled low (0 level in Table 15 and Table 16) using an on-board 1 kΩ pull-down resistor with the switch in ON position. If the line is not pulled down using the switch in OFF position, then a weak pull-up internal to the IXP465 network processor will pull the line high (1 level in Table 15 and Table 16).

The expansion bus address lines address lines correspond to the bits in Table 15. Several of the straps are overridden by the clock control CPLD for the hardware to operate properly.

The DIP switch locations on the board and the default values are shown in Figure 7 on page 37.

Table 15. Configuration Strapping Options

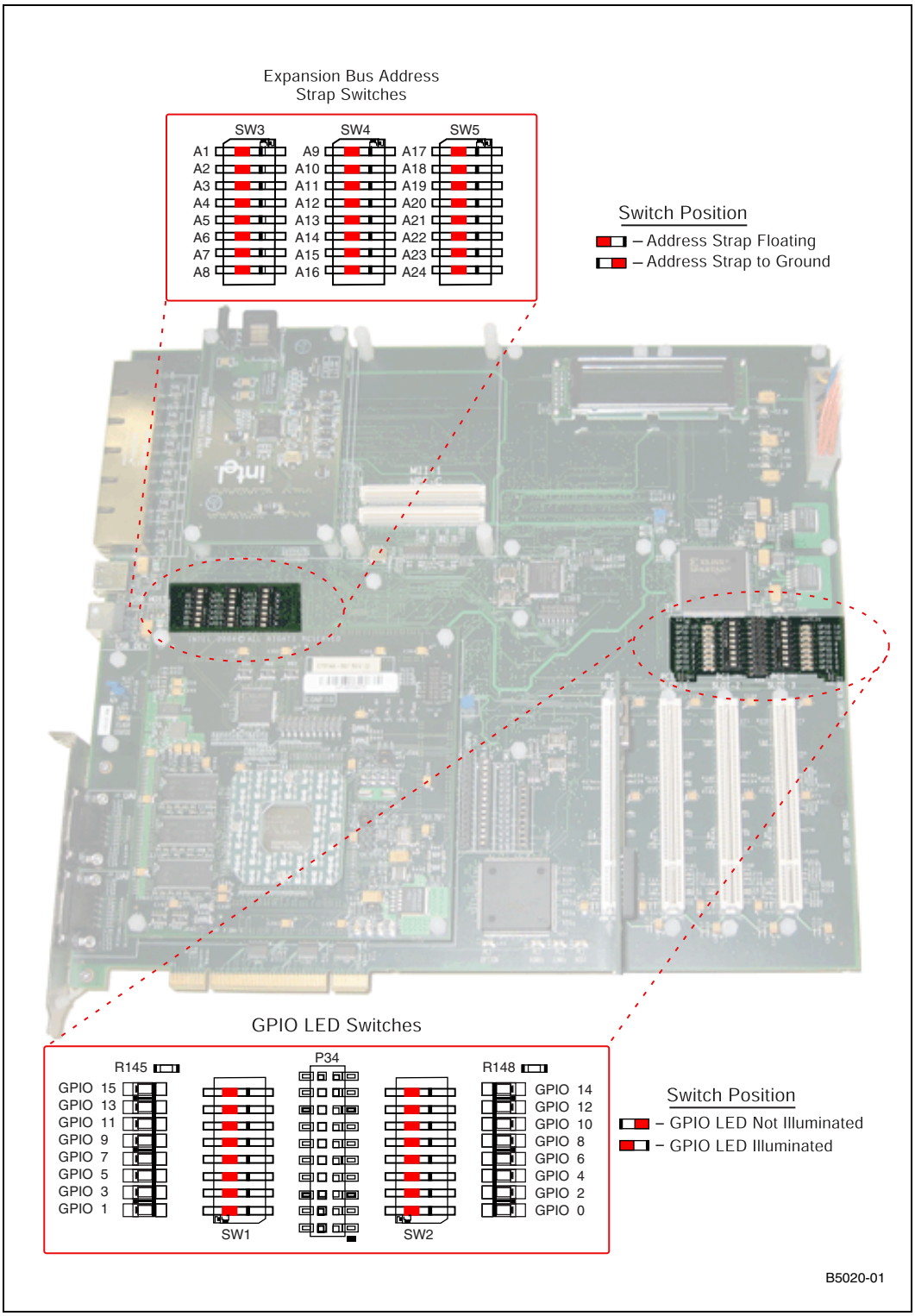
EX_ADDR Bit	Name	Description
24	Reserved	Reserved
23-21	Clock Setting	See Table 16 for details.
20-17	Customer	Customer-defined bits
16-11	Reserved	Reserved
10	IOWAIT_CS0	1 = EX_IOWAIT_N is sampled during the read/write Expansion bus cycles. 0 = EX_IOWAIT_N is ignored for read and write cycles to Chip select 0 if EXP_TIMING_CS0 is configured to Intel mode. Typically, IOWAIT_CS0 must be pulled down to Vss when attaching a Synchronous Intel® StrataFlash on Chip select 0. If EXP_TIMING_CS0 is reconfigured to Intel Synchronous mode during boot-up, the Expansion bus controller only ignores EX_IOWAIT_N during write cycles.
9	EXP_MEM_DRIVE	See the values defined for Bit 5, **EXP_DRIVE**
8	USB CLOCK	Controls the USB clock select 1 = USB Host/Device clock is generated internally 0 = USB Device clock is generated from GPIO[0] USB Host clock is generated from GPIO[1]. When generating a spread spectrum clock on OSC_IN, GPIO[0] is driven from the system board to generate a 48 MHz clock for the USB Device and GPIO[1] is driven from the system board to generate a 60 MHz clock for the USB Host.
7	32_FLASH	1 = 32-bit data bus 0 = 8/16 bit data bus based on 8/16_FLASH bit
6	EXP_ARB	Configures the Expansion bus arbiter 0 = External arbiter for Expansion bus 1 = Expansion bus controller arbiter enabled
5	EXP_DRIVE	Expansion bus low/medium/high drive strength. The drive strength depends on the configuration of **EXP_DRIVE** and **EXP_MEM_DRIVE** (Bit 9) 00 = Reserved 01 = Medium drive 10 = Low drive 11 = High drive
4	PCI_ CLK	Sets the PCI interface clock speed 0 = 33 MHz 1 = 66 MHz
3	Reserved	Reserved
2	PCI_ARB	Enables the PCI Controller arbiter 0 = PCI arbiter disabled 1 = PCI arbiter enabled
1	PCI_ HOST	Configures the PCI Controller as PCI bus host 0 = PCI as non-host 1 = PCI as host
0	8/16	Specifies the data bus width of the flash memory device if 32_FLASH bit = 0 0 = 16-bit data bus if 32_FLASH = 0 1 = 8-bit data bus if 32_FLASH = 0

Table 16. Configuration Strapping Clock Settings

Speed (Factory Part Speed)	EX_ADDR(23)	EX_ADDR(22)	EX_ADDR(21)	Actual Core Speed
667 MHz	1	X	X	667 MHz
667 MHz	0	0	0	667 MHz
667 MHz	0	0	1	533 MHz
667 MHz	0	1	0	266 MHz
667 MHz	0	1	1	400 MHz
533 MHz	1	X	X	533 MHz
533 MHz	0	0	0	533 MHz
533 MHz	0	0	1	533 MHz
533 MHz	0	1	0	266 MHz
533 MHz	0	1	1	400 MHz
400 MHz	1	X	X	400 MHz
400 MHz	0	0	0	400 MHz
400 MHz	0	0	1	400 MHz
400 MHz	0	1	0	266 MHz
400 MHz	0	1	1	400 MHz
266 MHz	X	X	X	266 MHz

Figure 7 shows the location and default settings of all Expansion Bus Address Strap Switches. Figure 7 also shows the location of all GPIO LED switches, which are discussed in more detail in Section 3.13, GPIO.

Figure 7. Switch Locations and Default Settings



3.3.3 Expansion Bus Clock Generation

The expansion bus clock is generated from a CPLD, and its frequency is software-selectable by writing to the registers defined in Section 3.22.1.1.1. The selectable frequencies are 33 MHz, 40 MHz, 66 MHz or 80 MHz. Individual expansion bus clocks are generated for the mezzanine cards (including the network processor module) by a 9-port zero delay buffer (Cypress CY2309). The default setting after a reset is 33 MHz.

3.3.4 Expansion Bus Chip Selects

The IXDP465 platform supports up to eight devices on the expansion bus. The expansion bus chip selects listed in Table 17 are assigned to allow for support of IXDP425 mezzanine cards (i.e., legacy support). Also, the connectors used are identical in size and pinout as those used on the IXDP425 / IXCDP1100 platform. A second connector on each mezzanine card allows for expansion of the expansion data bus to 32 bits and future expansion.

Table 17. Expansion Bus Chip Select Assignments

Chip Select	Device Assignment
CS0	Flash
CS1	ADSL/UTOPIA level 2
CS2	LCD Display, GPIO FPGA, Clock Control CPLD[a]
CS3	HSS0[b]
CS4	MII-0 (Ethernet Module 0)
CS5	MII-1 (Ethernet Module 1)
CS6	HSS1[b]
CS7	MII-2 (Ethernet Module 2)

a. The LCD display, the GPIO FPGA and the clock control CPLD share this chip select. The clock control CPLD decodes upper address signals and produce three separate chip selects.
b. CS3 and CS6 are routed to both HSS connectors so that mezzanine card modules can be stacked.

The chip selects are routed through zero-Ω resistors on the IXDP465 baseboard. If a chip select is needed for a different device, the resistor can be depopulated and the signal routed from the resistor to the new device as a jumper wire.

3.3.5 Expansion Bus Address Map

Table 18 defines the overall address map for the IXDP465 platform. The IXDP465 platform expansion bus address map is defined in Table 19. For additional memory mapping details of all IXP465 network processor interfaces and registers, please refer to the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

Table 18. IXDP465 Overall Address Mapping (Sheet 1 of 2)

Start Address	End Address	Size	Use
0x00000000	0x0FFFFFFF	246 Mbytes	Expansion bus/DDR[a]
0x00000000	0x3FFFFFFF	1 Gbytes	DDR
0x40000000	0x47FFFFFF	128 Mbytes	Reserved

Table 18. IXDP465 Overall Address Mapping (Sheet 2 of 2)

Start Address	End Address	Size	Use
0x48000000	0x4FFFFFFF	128 Mbytes	PCI
0x50000000	0x5FFFFFFF	256 Mbytes	Expansion bus
0x60000000	0x63FFFFFF	64 Mbytes	Queue manager
0xC0000000	0xCFFFFFFF	256 Mbytes	Configuration
0xCD000000	0xCDFFFFFF	256 Mbytes	USB Host Controller

a. After reset, the expansion bus is mapped to 0x00000000. When the remap bit of the IXP465 network processor expansion bus configuration register is set to '1', DDR is mapped to 0x00000000 and the expansion bus is still accessible at 0x50000000.

The IXDP465 platform expansion bus address map is defined in Table 19.

Table 19. IXDP465 Expansion Bus Address Mapping

Start Address	Size	Use
0x50000000 (CS0)	32 Mbytes	Flash
0x52000000 (CS1)	32 Mbytes	UTOPIA mezzanine card
0x54000000 (CS2)	1 byte	Clock Control CPLD – Control/Status register
0x54000001 (CS2)	1 byte	Clock Control CPLD – PCI Host Present register
0x54000002 (CS2)	1 byte	Clock Control CPLD – PCI Host 66 MHz Enabled register
0x54000003 (CS2)	1 byte	Clock Control CPLD – GPIO FPGA Programming register
0x54100000 (CS2)	1 byte	GPIO FPGA – Indirect Address register
0x54100001 (CS2)	1 byte	GPIO FPGA – Indirect Data register
0x54100002 (CS2)	1 byte	GPIO FPGA – Revision register
0x54100003 (CS2)	1 byte	GPIO FPGA – Scratchpad register
0x54200000 (CS2)	1 byte	LCD Display – Command register
0x54300000 (CS2)	1 byte	LCD Display – Data register
0x54400000 (CS2)	1 byte	CPU CPLD – Revision register
0x54400001 (CS2)	1 byte	CPU CPLD – I^2C Enable register
0x56000000 (CS3)	32 Mbytes	HSS-0 mezzanine card
0x58000000 (CS4)	32 Mbytes	MII-0 mezzanine card
0x5A000000 (CS5)	32 Mbytes	MII-1 mezzanine card
0x5C000000 (CS6)	32 Mbytes	HSS-1 mezzanine card
0x5E000000 (CS7)	32 Mbytes	MII-2 mezzanine card

3.3.6 Expansion Bus LCD Display

A 2 x16-digit LCD display is provided on the expansion bus for software debug. **EX_DATA[7:0]** drives the display.

For information about accessing the LCD display, refer to Section 3.22.1.3, LCD Display Instruction Register.

3.4 BootROM

An Intel® 28F256J3C 64-pin BGA packaged flash is installed on the IXDP465 platform. The flash is connected to IXP465 network processor's expansion bus. The IXDP465 platform supports 8 Mbytes to 32 Mbytes of flash and ships with 32 Mbytes.

The IXDP465 platform always requests a starting boot address of 0x0 on **EX_ADDR[24:0]**.

The IXDP465 platform is based on a 16-bit data bus. The Clock Control CPLD sets the expansion bus after reset to 16-bit mode. The Clock Control CPLD design does not support 8-bit mode. A JTAG Header is provisioned on the platform, to allow re-programming of the CPLD for designs that require customized modes. See Figure 15 on page 84 for the header location.

The **FLASH_STS** pin on the flash is tied to a yellow LED to indicate when the device is being programmed on the IXDP465 platform. It is pulled up through a 10 KΩ resistor since it is an open drain output.

A 0.1 µF ceramic capacitor is connected between each of the device's three V_{CC} pins and ground. In addition, a 4.7 µF electrolytic capacitor is placed between **V_{CC}** and **GND** at the array's power supply connection.

Two jumpers (**JP127 /JP128)** on expansion bus address signals (**EX_ADDR24** and **EX_ADDR23**) partition the flash device into four sections. Table 20 defines the flash sectioning. See Appendix A, "Updating the IXDP465 Flash Memory" for information about how to use RedBoot to update the content of these sections.

Table 20. Flash Sectioning

EX_ADDR24 Jumper	EX_ADDR23 Jumper	Start Address	End Address	Section Size	Bootloader
installed	installed	0x00000000	0x01FFFFFF	32 Mbyte	RedBoot*
installed	not installed	0x00800000	0x00FFFFFF	8 Mbyte	VxWorks* bootrom
not installed	installed	0x01000000	0x01FFFFFF	16 Mbyte	--
not installed	not installed	0x01800000	0x01FFFFFF	8 Mbyte	--

3.5 UTOPIA Connector

The IXDP465 platform supports up to 31 PHYs on the UTOPIA level 2 interface (the maximum amount supported by the IXP465 network processor) through a 2x60-pin mezzanine card connector (Amp 5-179010-5). The UTOPIA level 2 and Expansion Bus signals are routed to this connector to allow a variety of DSL PHY modules to be configured, including PHY modules from the IXDP425 development platform. See Table 75 on page 113 for the connector pin definitions.

Note: All IXP465 network processor engine (NPE) functions require Intel-supplied software. For information about using this software, see the *Intel® IXP400 Software Programmer's Guide*. For information about the availability of this enabling software, contact your Intel sales representative.

Table 21 lists the pull-up resistors used on the UTOPIA level 2 interface. These signals are IXP465 network processor signals that must not be left floating when a module is not plugged into the connector. The 10 KΩ resistor value was chosen so that a DSL module can easily over-drive the signal state provided by the pull-up. Decoupling is handled on each module.

Table 21. UTOPIA Level 2 Resistors

Signal	Pull to Value	Resistor Value
UTP_OP_CLK	+3.3 V	10 KΩ
UTP_IP_CLK	+3.3 V	10 KΩ
UTP_IP_DATA[7:0]	+3.3 V	10 KΩ
UTP_IP_FCI	+3.3 V	10 KΩ
UTP_IP_SOC	+3.3 V	10 KΩ
UTP_OP_FCI	+3.3 V	10 KΩ
UTP_OP_FCO	+3.3 V	10 KΩ
UTP_IP_FCO	+3.3 V	10 KΩ

3.6 HSS Connectors

The IXDP465 platform implements two sets of connectors dedicated to HSS devices. The HSS connectors support the HSS interfaces. The first connector of this connector pair is the same connector (physically and in pinout) that is supported on the IXDP425 / IXCDP1100 platform (for compatibility with previous platform versions). The second connector provides for increased expansion bus capability on the IXP465 network processor.

The primary HSS interface for the HSS-0 connector is **HSS0**, with **HSS1** as the secondary, alternate HSS interface. This arrangement allows for stacking up to eight mezzanine cards using reserved pins on the IXDP465 interface standard connector. The primary HSS interface for the HSS-1 connector is **HSS1**, with **HSS0** as the secondary HSS interface.

This connector supports the following mezzanine cards (using the HSS interface):

- IXPVM465 Analog Voice mezzanine card (4-FXS, 1-FXO)
- IXPFRM465 Quad T1/E1 mezzanine card

Note: Although previous platforms have combined the HSS and UTOPIA interfaces on one connector, the IXDP465 platform separates the interfaces to allow more flexible configuration options.

The mezzanine card connector (Amp 179031-5) has been designed to accommodate the signals needed for these supported devices. The expansion bus is routed to the connector for a control interface. Both HSS0 and HSS1 signals are routed to this connector. The expansion bus signal pinout on the connector is the same as on the MII connector to provide an option for designing an HPI module to fit on either connector.

Table 22 lists the pull-up resistors placed on the IXDP465 baseboard. The resistor placement follows the requirements listed in the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*. The 10 KΩ resistor value was chosen so that a DSL module can easily over-drive the signal state provided by the pull-up. Decoupling is handled on each module.

Table 22. HSS0/1 Resistors

Signal	Pull to Value	Resistor Value
HSS0/1_TXDATA0/1	+3.3 V	10 KΩ
HSS0/1_TXFRAME0/1	+3.3 V	10 KΩ
HSS0/1_TXCLK0/1	+3.3 V	10 KΩ
HSS0/1_RXDATA0/1	+3.3 V	10 KΩ
HSS0/1_RXFRAME0/1	+3.3 V	10 KΩ
HSS0/1_RXCLK0/1	+3.3 V	10 KΩ

3.6.1 HSS-0 Mezzanine Card Interface

To achieve compatibility with the IXDP425 / IXCDP1100 platform, the following features are designed into the IXDP465 platform interface standard connector for the HSS mezzanine card slot:

- Connector part number Amp 5-179010-5
- Exact pin-out match with the IXDP425 development platform
- Primary connection to HSS0
- Use of expansion bus chip select 3
- Use of expansion bus ready 3

The IXDP465 platform expansion bus connector for the HSS mezzanine card slot contains the following signal groups:

- IXP465 SPI
- IXP465 I^2C
- IXP465 extended expansion bus
- 16 GPIO
- Mezzanine ID byte (stacking)
- 32 pins for future expansion (common to all mezzanine cards)
- 16 pins for future expansion (dedicated to this mezzanine card)
- Additional power

The IXDP465 platform HSS-0 standard interface connector signal definitions are defined in Table 23. The power signals are +2.5 V, +3.3 V, +5.0 V and +12.0 V. The expansion bus signals provide the 16 LSB of the data bus, the 24 LSB of the address bus, chip select 3, clocking and control to the mezzanine card. The interrupt signal from the mezzanine card is routed to the GPIO FPGA. The JTAG signals are not used. The primary HSS signals are connected to HSS-0. The secondary HSS signals are connected to HSS-1. The GPIO signals route to the GPIO FPGA. The Legend describing the color-codes for the signals follows the table.

Table 23. HSS-0 Mezzanine Card Standard Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
-	1	EX_ADDR11	41	5.0 V	81
-	2	EX_ADDR10	42	3.3 V	82
-	3	EX_ADDR13	43	HSS0_GPIO2	83
-	4	EX_ADDR12	44	HSS0_GPIO3	84
EX_DATA1	5	EX_ADDR15	45	GND	85
EX_DATA0	6	EX_ADDR14	46	GND	86
EX_DATA3	7	GND	47	-	87
EX_DATA2	8	GND	48	HSS0_GPIO4	88
HSS0_GPIO0	9	EX_ADDR17	49	-	89
HSS0_GPIO1	10	EX_ADDR16	50	RST_N	90
EX_DATA5	11	EX_ADDR19	51	-	91
EX_DATA4	12	EX_ADDR18	52	HSS_TXFRAME1	92
EX_DATA7	13	EX_ADDR21	53	-	93
EX_DATA6	14	EX_ADDR20	54	HSS_TXCLK1	94
GND	15	EX_ADDR23	55	GND	95
GND	16	EX_ADDR22	56	HSS_TXDATA1	96
EX_DATA9	17	GND	57	HSS_TXDATA0	97
EX_DATA8	18	GND	58	GND	98
EX_DATA11	19	EX_CLK_HSS0	59	HSS_TXFRAME0	99
EX_DATA10	20	EX_RD_N	60	HSS_RXDATA0	100
-	21	GND	61	-	101
-	22	EX_WR_N	62	HSS_RXFRAME0	102
EX_DATA13	23	EX_ALE	63	HSS_TXCLK0	103
EX_DATA12	24	EX_RDY_N3	64	-	104
EX_DATA15	25	EX_IOWAIT_N	65	GND	105
EX_DATA14	26	HSS0_INT_N	66	HSS_RXCLK0	106
GND	27	EX_CS_N3	67	-	107
GND	28	3.3 V	68	GND	108
EX_ADDR1	29	-	69	HSS_RXCLK1	109
EX_ADDR0	30	3.3 V	70	-	110
EX_ADDR3	31	5.0 V	71	HSS_RXFRAME1	111
EX_ADDR2	32	3.3 V	72	HSS_RXDATA1	112
EX_ADDR5	33	5.0 V	73	12 V	113
EX_ADDR4	34	3.3 V	74	2.5 V	114
EX_ADDR7	35	5.0 V	75	12 V	115
EX_ADDR6	36	3.3 V	76	2.5 V	116
GND	37	5.0 V	77	12 V	117

Table 23. HSS-0 Mezzanine Card Standard Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	38	3.3 V	78	2.5 V	118
EX_ADDR9	39	5.0 V	79	12 V	119
EX_ADDR8	40	3.3 V	80	2.5 V	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
GPIO signals	maroon
HSS0 signals (primary)	black
HSS1 signals (secondary)	red
not used (JTAG signals)	gray
interrupt signal	gold

The IXDP465 platform HSS-0 mezzanine card expansion connector signal definitions are defined in Table 24. The power signals are +1.8 V, +3.3 V, and +5.0 V. The expansion bus signals provide the 16 MSB of the data bus and the 1 MSB of the address bus.

The common (among all mezzanine cards) and dedicated (this mezzanine card only) future expansion signals connect to the network processor module and are intended for use with future peripherals.

The SPI signals connect to the IXP465 network processor SPI peripheral. The I^2C signals connect to the IXP465 network processor I^2C peripheral. The HSS-0 GPIO signals connect to the GPIO FPGA. The mezzanine card ID signals are used for board ID when the cards are stacked. The Legend describing the color-codes for the signals follows the table.

Table 24. HSS-0 Mezzanine Card Expansion Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
1.8 V	1	C_PCI_4	41	3.3 V	81
1.8 V	2	C_PCI_5	42	3.3 V	82
GND	3	C_PCI_6	43	3.3 V	83
GND	4	C_PCI_7	44	3.3 V	84
EX_DATA17	5	C_PCI_8	45	GND	85
EX_DATA16	6	C_PCI_9	46	GND	86
EX_DATA19	7	EX_BE_N3	47	C_FN_59	87
EX_DATA18	8	EX_BE_N2	48	C_FN_60	88
GND	9	EX_BE_N1	49	C_FN_61	89
GND	10	EX_BE_N0	50	C_FN_62	90
EX_DATA21	11	EX_BURST	51	GND	91
EX_DATA20	12	EX_PAR3	52	GND	92

Table 24. HSS-0 Mezzanine Card Expansion Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_DATA23	13	EX_PAR2	53	C_FN_63	93
EX_DATA22	14	EX_PAR1	54	HSS0_GPIO5	94
GND	15	EX_PAR0	55	HSS0_GPIO6	95
GND	16	C_NPE_0	56	HSS0_GPIO7	96
EX_DATA25	17	C_NPE_1	57	GND	97
EX_DATA24	18	C_NPE_2	58	GND	98
EX_DATA27	19	C_NPE_3	59	HSS0_GPIO8	99
EX_DATA26	20	C_NPE_4	60	HSS0_GPIO9	100
GND	21	C_NPE_5	61	HSS0_GPIO10	101
GND	22	C_NPE_6	62	HSS0_GPIO11	102
EX_DATA29	23	C_NPE_7	63	GND	103
EX_DATA28	24	C_NPE_8	64	GND	104
EX_DATA31	25	C_NPE_9	65	HSS0_GPIO12	105
EX_DATA30	26	C_NPE_10	66	HSS0_GPIO13	106
GND	27	C_NPE_11	67	HSS0_GPIO14	107
GND	28	C_NPE_12	68	HSS0_GPIO15	108
EX_ADDR24	29	CLK32_HSS0	69	GND	109
SSPS_CLK	30	C_FN_48	70	GND	110
SSPS_FRM	31	C_FN_49	71	GND (ID0)	111
SSPS_TXD	32	C_FN_50	72	3.3 V (ID1)	112
SSPS_RXD	33	C_FN_51	73	3.3 V (ID2)	113
SSPS_EXTCLK	34	C_FN_52	74	3.3 V (ID3)	114
5.0 V	35	C_FN_53	75	3.3 V (ID4)	115
5.0 V	36	C_FN_54	76	3.3 V (ID5)	116
C_PCI_0	37	C_FN_55	77	3.3 V (ID6)	117
C_PCI_1	38	C_FN_56	78	3.3 V (ID7)	118
C_PCI_2	39	C_FN_57	79	I^2C_SDA	119
C_PCI_3	40	C_FN_58	80	I^2C_SCL	120

Legend	
power signals	purple
expansion bus signals	green
common future expansion signals	blue
dedicated future expansion signals (this card only)	black
SPI signals	red

Legend (Continued)	
I2C signals)	gold
GPIO signals	maroon
Clock signal	lavender

3.6.2 HSS-1 Mezzanine Card Interface

To achieve compatibility with the IXDP425 / IXCDP1100 platform, the following features are designed into the IXDP465 platform interface standard connector for the HSS-1 mezzanine card:

- Connector part number Amp 5-179010-5
- Exact pinout match
- Primary connection to HSS1
- Use of expansion bus chip select 6
- Use of expansion bus ready 2

The mezzanine card expansion connector contains the following signal groups:

- IXP465 network processor SPI
- IXP465 network processor I^2C
- IXP465 network processor extended expansion bus
- 16 GPIO
- Mezzanine ID byte (for stacking)
- 32 pins for future expansion (common to all mezzanine cards)
- 16 pins for future expansion (dedicated to this mezzanine card)
- Additional power

The IXDP465 platform HSS-1 standard connector signal definition is described in Table 25. The power signals are +2.5 V, +3.3 V, +5.0 V, and +12.0 V. The expansion bus signals provide the 16 LSB of the data bus, the 24 LSB of the address bus, chip select 6, clocking and control to the mezzanine card. The interrupt signal from the mezzanine card is routed to the GPIO FPGA. The JTAG signals are not used. The primary HSS signals are connected to HSS-1. The secondary HSS signals are connected to HSS-0. The GPIO signals route to the GPIO FPGA. The Legend describing the color-codes for the signals follows the table.

Table 25. HSS-1 Mezzanine Card Standard Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
-	1	EX_ADDR11	41	5.0 V	81
-	2	EX_ADDR10	42	3.3 V	82
-	3	EX_ADDR13	43	HSS1_GPIO2	83
-	4	EX_ADDR12	44	HSS1_GPIO3	84
EX_DATA1	5	EX_ADDR15	45	GND	85
EX_DATA0	6	EX_ADDR14	46	GND	86

Table 25. HSS-1 Mezzanine Card Standard Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_DATA3	7	GND	47	-	87
EX_DATA2	8	GND	48	HSS1_GPIO4	88
HSS1_GPIO0	9	EX_ADDR17	49	-	89
HSS1_GPIO1	10	EX_ADDR16	50	RST_N	90
EX_DATA5	11	EX_ADDR19	51	-	91
EX_DATA4	12	EX_ADDR18	52	HSS_TXFRAME0	92
EX_DATA7	13	EX_ADDR21	53	-	93
EX_DATA6	14	EX_ADDR20	54	HSS_TXCLK0	94
GND	15	EX_ADDR23	55	GND	95
GND	16	EX_ADDR22	56	HSS_TXDATA0	96
EX_DATA9	17	GND	57	HSS_TXDATA1	97
EX_DATA8	18	GND	58	GND	98
EX_DATA11	19	EX_CLK_HSS1	59	HSS_TXFRAME1	99
EX_DATA10	20	EX_RD_N	60	HSS_RXDATA1	100
-	21	GND	61	-	101
-	22	EX_WR_N	62	HSS_RXFRAME1	102
EX_DATA13	23	EX_ALE	63	HSS_TXCLK1	103
EX_DATA12	24	EX_RDY_N2	64	-	104
EX_DATA15	25	EX_IOWAIT_N	65	GND	105
EX_DATA14	26	HSS1_INT_N	66	HSS_RXCLK1	106
GND	27	EX_CS_N6	67	-	107
GND	28	3.3 V	68	GND	108
EX_ADDR1	29	-	69	HSS_RXCLK0	109
EX_ADDR0	30	3.3 V	70	-	110
EX_ADDR3	31	5.0 V	71	HSS_RXFRAME0	111
EX_ADDR2	32	3.3 V	72	HSS_RXDATA0	112
EX_ADDR5	33	5.0 V	73	12 V	113
EX_ADDR4	34	3.3 V	74	2.5 V	114
EX_ADDR7	35	5.0 V	75	12 V	115
EX_ADDR6	36	3.3 V	76	2.5 V	116
GND	37	5.0 V	77	12 V	117
GND	38	3.3 V	78	2.5 V	118
EX_ADDR9	39	5.0 V	79	12 V	119
EX_ADDR8	40	3.3 V	80	2.5 V	120

Legend	
power signals	purple
extended expansion bus signals	green
GPIO signals	maroon
HSS1 signals (primary)	black
HSS0 signals (secondary)	red
not used (JTAG signals)	gray
interrupt signal	gold

The IXDP465 platform HSS-1 expansion connector signal definition is described in Table 26. The power signals are +1.8 V, +3.3 V, and +5.0 V. The expansion bus signals provide the 16 MSB of the data bus and the 1 MSB of the address bus. The common (among all mezzanine cards) and dedicated (this mezzanine card only) future expansion signals connect to the network processor module and are intended for use with future peripherals.

The SPI signals connect to the IXP465 network processor SPI peripheral. The I^2C signals connect to the IXP465 I^2C peripheral. The GPIO signals connect to the GPIO FPGA. The mezzanine card ID signals are used for the board ID when stacking HSS mezzanine cards. The Legend describing the color-codes for the signals follows the table.

Table 26. HSS-1 Mezzanine Card Expansion Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
1.8 V	1	C_PCI_4	41	3.3 V	81
1.8 V	2	C_PCI_5	42	3.3 V	82
GND	3	C_PCI_6	43	3.3 V	83
GND	4	C_PCI_7	44	3.3 V	84
EX_DATA17	5	C_PCI_8	45	GND	85
EX_DATA16	6	C_PCI_9	46	GND	86
EX_DATA19	7	EX_BE_N3	47	C_FN_75	87
EX_DATA18	8	EX_BE_N2	48	C_FN_76	88
GND	9	EX_BE_N1	49	C_FN_77	89
GND	10	EX_BE_N0	50	C_FN_78	90
EX_DATA21	11	EX_BURST	51	GND	91
EX_DATA20	12	EX_PAR3	52	GND	92
EX_DATA23	13	EX_PAR2	53	C_FN_79	93
EX_DATA22	14	EX_PAR1	54	HSS1_GPIO5	94
GND	15	EX_PAR0	55	HSS1_GPIO6	95
GND	16	C_NPE_0	56	HSS1_GPIO7	96
EX_DATA25	17	C_NPE_1	57	GND	97
EX_DATA24	18	C_NPE_2	58	GND	98
EX_DATA27	19	C_NPE_3	59	HSS1_GPIO8	99
EX_DATA26	20	C_NPE_4	60	HSS1_GPIO9	100
GND	21	C_NPE_5	61	HSS1_GPIO10	101

Table 26. HSS-1 Mezzanine Card Expansion Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	22	C_NPE_6	62	HSS1_GPIO11	102
EX_DATA29	23	C_NPE_7	63	GND	103
EX_DATA28	24	C_NPE_8	64	GND	104
EX_DATA31	25	C_NPE_9	65	HSS1_GPIO12	105
EX_DATA30	26	C_NPE_10	66	HSS1_GPIO13	106
GND	27	C_NPE_11	67	HSS1_GPIO14	107
GND	28	C_NPE_12	68	HSS1_GPIO15	108
EX_ADDR24	29	CLK32_HSS1	69	GND	109
SSPS_CLK	30	C_FN_64	70	GND	110
SSPS_FRM	31	C_FN_65	71	GND (ID0)	111
SSPS_TXD	32	C_FN_66	72	3.3 V (ID1)	112
SSPS_RXD	33	C_FN_67	73	3.3 V (ID2)	113
SSPS_EXTCLK	34	C_FN_68	74	3.3 V (ID3)	114
5.0 V	35	C_FN_69	75	3.3 V (ID4)	115
5.0 V	36	C_FN_70	76	3.3 V (ID5)	116
C_PCI_0	37	C_FN_71	77	3.3 V (ID6)	117
C_PCI_1	38	C_FN_72	78	3.3 V (ID7)	118
C_PCI_2	39	C_FN_73	79	I^2C_SDA	119
C_PCI_3	40	C_FN_74	80	I^2C_SCL	120

Legend	
power signals	purple
expansion bus signals	green
common future expansion signals	blue
dedicated future expansion signals (this card only)	black
SPI signals	red
I2C signals)	gold
GPIO signals	maroon
Clock signal	lavender

3.7 SMII Multi-Pack Interface

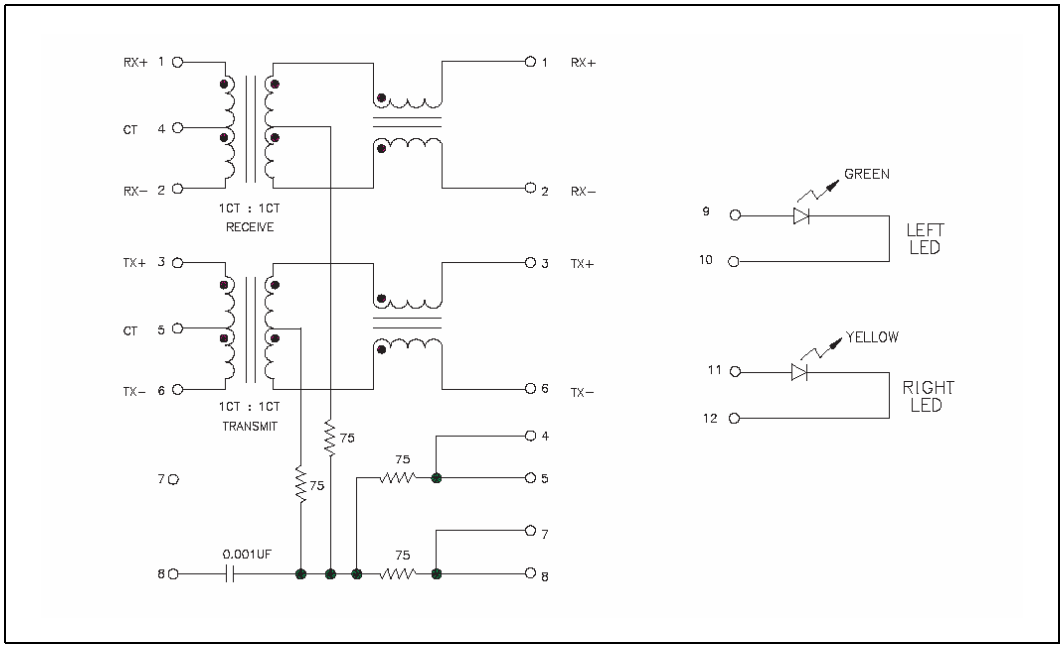
The IXDP465 platform supports a six-pack SMII. This interface uses a 6-gang RJ-45 connector with integrated magnetics. It is designed as a 6-port switch function that supports simple 802.1 bridging as well as future expansion to 802.1Q VLAN. For further information about what features are currently supported, see the *Intel® IXP400 Software Programmer's Guide*. When the IXDP465 platform is configured to use the 6-pack SMII, the three mezzanine card MII connectors are

disabled. To exercise all six ports of Ethernet, the proper configuration of NPE functions must be selected through proper software programming of fuse bits in the **EXP_UNIT_FUSE_RESET** register immediately after reset. For information about the possible NPE function configurations, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

3.7.1 Multi-Gang Jack

The IXDP465 platform contains a 6-port RJ-45 gang jack (Pulse Engineering part number J8064D668A) with integrated magnetics. Each port has two LEDs (one green, one yellow) controlled by the PHY. The software programs the PHY (through the MII interface) to illuminate the LEDs according to certain events such as activity, half-full duplex, 10/100 MHz, etc. Figure 8 shows the integrated magnetics within the gang jack.

Figure 8. RJ-45 Jack with Integrated Magnetics

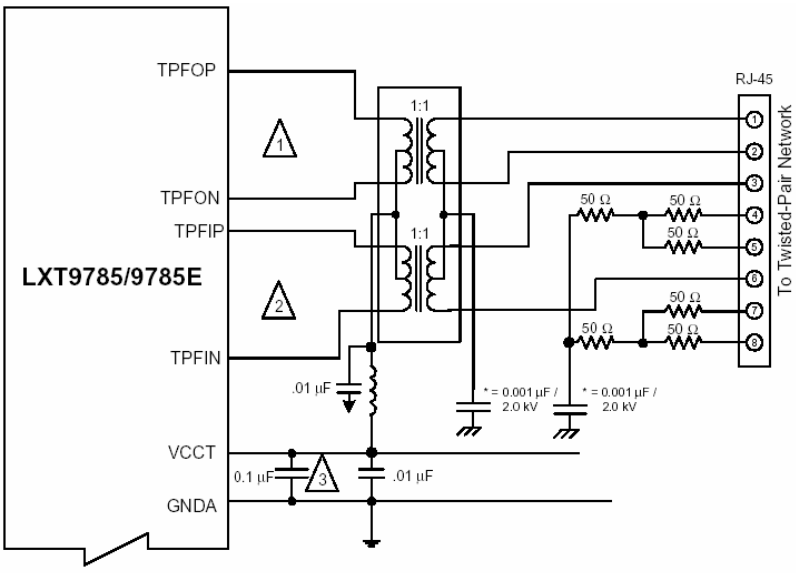


3.7.2 SMII PHY Connection

The IXDP465 platform contains an 8-port SMII PHY (Intel® HBLXT9785HC.DO 853353) to connect the NPE SMII interface to the onboard Ethernet magnetics (not the mezzanine card MII interface). Figure 9 depicts this connection.

Note: Only six of the eight SMII PHY Ethernet ports (ports 0 - 5) are used by the IXDP465 platform.

Figure 9. Octal PHY Connection to Magnetics



1. The 100Ω transmit load termination resistor typically required is integrated in the LXT9785/9785E.
2. The 100Ω receive load termination resistor typically required is integrated in the LXT9785/9785E.
3. Recommended 0.1 µF capacitor to improve EMI performance.

The IXDP465 platform applies impedance matching techniques to the differential **Tx** and **Rx** pairs of each Ethernet port.

The IXDP465 platform allows all Ethernet modes to be tested. This includes MII (through the three mezzanine cards) and SMII (through the multi-port PHY). The IXDP465 platform has user-selectable jumpers to test these options, as shown in Figure 11. Figure 10 shows the logical connections of NPE signals to the specific types of configurations (i.e, MII, SMII, UTOPIA).

Figure 10. NPE Function Connections

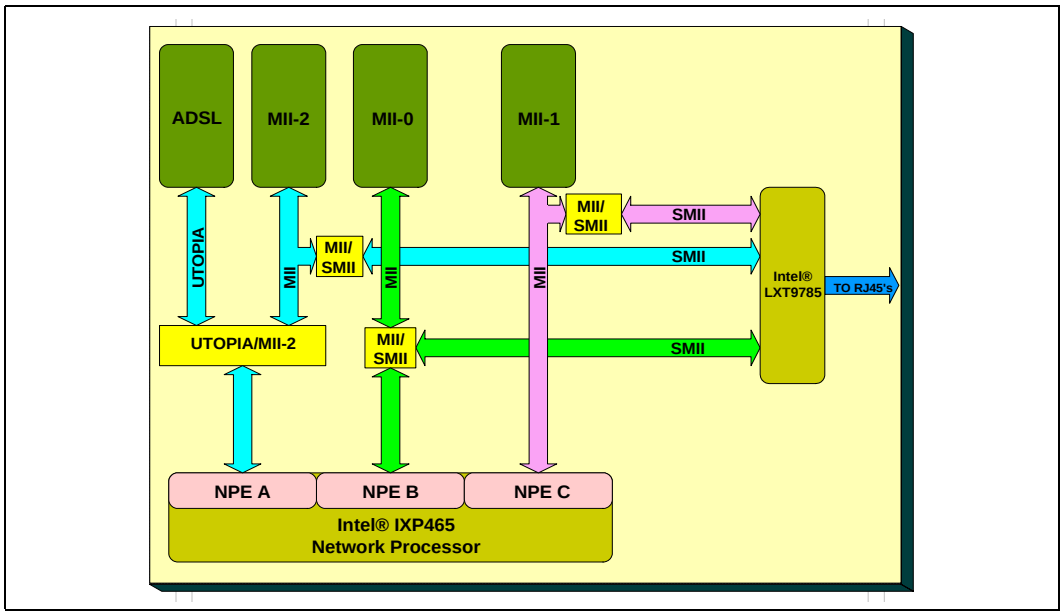


Table 27 through Table 32 define the NPE signals and their associated functions for each type of MII interface.

The IXDP465 platform has a separate oscillator for use with SMII mode. The clock frequency is jumper-selectable via JP9 and JP11, as shown in Figure 11.

A clock driver minimizes noise. Each clock signal contains a series resistor and parallel capacitor to reduce noise.

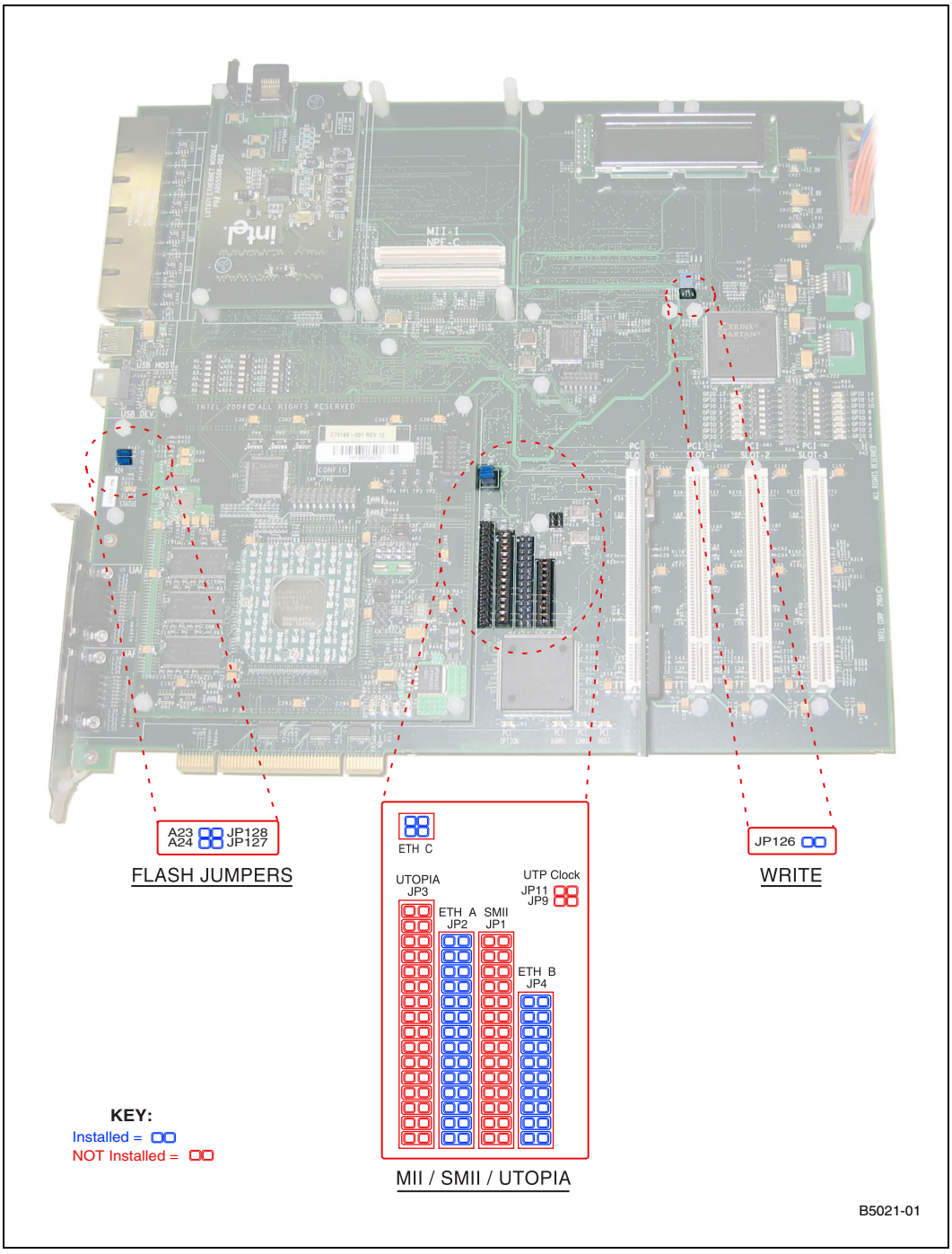
The SMII interface requires a 125 MHz, +/- 50ppm reference. The reference clock must be enabled at all times. The 125 MHz clock characteristics include:

- Duty cycle distortion no greater than 40 to 60%.
- Voltage levels: VOH > 2.0 V for VCCIO = 3.3+/- 5%;
  VOH > 1.75 V for VCCIO = 2.5 +/- 5%.

A recommended clock for 125 MHz operation is the Saronix ST4130A*.

The reference clock generates transmit signals and recovers receive signals. A crystal-based clock is recommended over a derived clock (i.e., PLL-based) to minimize transmit jitter. Regardless of clock source, careful consideration must be given to physical placement, board layout, and signal routing of the source to maintain the highest possible level of signal integrity.

Figure 11. Jumper Locations and Default Settings



3.7.3 NPE-A,B,C SMII Configurations

SMII features can be disabled or enabled on each of the three NPEs when they are connected to SMII ports. As a result, there are eight unique SMII configurations with different implementations of NPE functionality. These eight possible configurations as defined in Table 27 and referred to in subsequent sections that cover NPE jumper pin assignments. Select one of the following configurations, which range from disabling all six SMII interface modes (CFG #1) to enabling all six SMII interface modes across all three NPEs (CFG #8).

Table 27. NPE SMII Configurations

NPE/SMII Port	SMII Configuration Number							
	CFG #1	CFG #2	CFG #3	CFG #4	CFG #5	CFG #6	CFG #7	CFG #8
NPE C (SMII 5)	OFF	ON	OFF	ON	OFF	ON	OFF	ON
NPE A (SMII 4)	OFF	OFF	ON	ON	OFF	OFF	ON	ON
NPE B (SMII 3-0)	OFF	OFF	OFF	OFF	ON	ON	ON	ON

Notes:

Table Key:
OFF = SMII functionality is disabled for this NPE
ON = SMII functionality is enabled for this NPE

Once a specific SMII configuration is selected from Table 27, then the required NPE jumper pin assignments for JP1, JP2, JP3, JP4, and JP65/JP93 shown in Figure 11 are determined by using the appropriate SMII Configuration Number column in the tables provided in Section 3.8, NPE Jumper Block Pin Assignments.

3.8 NPE Jumper Block Pin Assignments

Note: The “CFG #” columns in the tables in this section refer to SMII configurations defined in Table . If you are not using SMII with any of the NPEs, then “CFG #1” is the correct column to use for NPE jumper settings.

3.8.1 NPE-A,B,C SMII Jumper Block (JP1)

The IXP465 network processor contains NPE pins that have multiple functions. The SMII jumper block connects specific shared NPE signals to the multi-port PHY. Table 28 shows the pin definitions for the SMII jumper block as well as the JP1 jumper pin assignments, which depend on the SMII Configuration (CFG #) selected in Table 27. To find the location of JP1 on the IXDP465 baseboard, see Figure 11.

Table 28. SMII Jumper Block (JP1) Pin Assignments (Sheet 1 of 2)

JP1 Pin	Network Processor Signal	JP1 Pin	SMII Signal	CFG #1	CFG #2	CFG #3	CFG #4	CFG #5	CFG #6	CFG #7	CFG #8
1	C_ETHC_TXDATA0	2	SMII_TXDATA5	---	IN	---	IN	---	IN	---	IN
3	C_ETHC_RXDATA0	4	SMII_RXDATA5	---	IN	---	IN	---	IN	---	IN
5	C_UTP_OP_DATA7	6	SMII_TXDATA4	---	---	IN	IN	---	---	IN	IN

Table 28. SMII Jumper Block (JP1) Pin Assignments (Sheet 2 of 2)

JP1 Pin	Network Processor Signal	JP1 Pin	SMII Signal	CFG #1	CFG #2	CFG #3	CFG #4	CFG #5	CFG #6	CFG #7	CFG #8
7	C_UTP_IP_DATA7	8	SMII_RXDATA4	---	---	IN	IN	---	---	IN	IN
9	C_ETHB_TXCLK	10	SMII_REFCLK_R2	---	---	---	---	IN	IN	IN	IN
11	C_ETHB_TXDATA0	12	SMII_TXDATA0	---	---	---	---	IN	IN	IN	IN
13	C_ETHB_TXDATA1	14	SMII_TXDATA1	---	---	---	---	IN	IN	IN	IN
15	C_ETHB_TXDATA2	16	SMII_TXDATA2	---	---	---	---	IN	IN	IN	IN
17	C_ETHB_TXDATA3	18	SMII_TXDATA3	---	---	---	---	IN	IN	IN	IN
19	C_ETHB_RXDATA0	20	SMII_RXDATA0	---	---	---	---	IN	IN	IN	IN
21	C_ETHB_RXDATA1	22	SMII_RXDATA1	---	---	---	---	IN	IN	IN	IN
23	C_ETHB_RXDATA2	24	SMII_RXDATA2	---	---	---	---	IN	IN	IN	IN
25	C_ETHB_RXDATA3	26	SMII_RXDATA3	---	---	---	---	IN	IN	IN	IN
27	C_ETHB_CRS	28	SMII_SYNC	---	---	---	---	IN	IN	IN	IN

Notes:

Table Key:
--- = JP1 Jumpers must NOT be installed
IN = JP1 Jumpers must be installed

3.8.2 NPE-A MII Jumper Block (JP2)

The IXP465 network processor contains NPE pins that have multiple functions. The NPE-A MII jumper block connects specific shared NPE signals to the MII NPE-A mezzanine card. Table 29 shows the pin definitions for the NPE-A MII jumper block as well as the JP2 jumper pin assignments, which depend on the SMII Configuration (CFG #) selected in Table 27. To find the location of JP2 on the IXDP465 baseboard, see Figure 11.

Table 29. NPE-A MII Jumper Block (JP2) Pin Assignments (Sheet 1 of 2)

JP2 Pin	Network Processor Signal	JP2 Pin	MII Signal	CFG #1	CFG #2	CFG #3	CFG #4	CFG #5	CFG #6	CFG #7	CFG #8
1	C_UTP_IP_CLK	2	ETHA_RXCLK	OPT	OPT	---	---	OPT	OPT	---	---
3	C_UTP_OP_CLK	4	ETHA_TXCLK	OPT	OPT	---	---	OPT	OPT	---	---
5	C_UTP_OP_DATA0	6	ETHA_TXDATA0	OPT	OPT	---	---	OPT	OPT	---	---
7	C_UTP_OP_DATA1	8	ETHA_TXDATA1	OPT	OPT	---	---	OPT	OPT	---	---
9	C_UTP_OP_DATA2	10	ETHA_TXDATA2	OPT	OPT	---	---	OPT	OPT	---	---
11	C_UTP_OP_DATA3	12	ETHA_TXDATA3	OPT	OPT	---	---	OPT	OPT	---	---
13	C_UTP_OP_DATA4	14	ETHA_TXEN	OPT	OPT	---	---	OPT	OPT	---	---
15	C_UTP_IP_DATA0	16	ETHA_RXDATA0	OPT	OPT	---	---	OPT	OPT	---	---
17	C_UTP_IP_DATA1	18	ETHA_RXDATA1	OPT	OPT	---	---	OPT	OPT	---	---
19	C_UTP_IP_DATA2	20	ETHA_RXDATA2	OPT	OPT	---	---	OPT	OPT	---	---
21	C_UTP_IP_DATA3	22	ETHA_RXDATA3	OPT	OPT	---	---	OPT	OPT	---	---

Table 29. NPE-A MII Jumper Block (JP2) Pin Assignments (Sheet 2 of 2)

JP2 Pin	Network Processor Signal	JP2 Pin	MII Signal	CFG #1	CFG #2	CFG #3	CFG #4	CFG #5	CFG #6	CFG #7	CFG #8
23	C_UTP_IP_DATA4	24	ETHA_RXDV	OPT	OPT	---	---	OPT	OPT	---	---
25	C_UTP_IP_DATA5	26	ETHA_COL	OPT	OPT	---	---	OPT	OPT	---	---
27	C_UTP_IP_DATA6	28	ETHA_CRS	OPT	OPT	---	---	OPT	OPT	---	---

Notes:

Table Key:
--- = JP2 jumpers must NOT be installed

OPT = JP2 jumpers can optionally be installed (all 14 jumpers IN) to enable NPE-A MII Mode with NPE-A UTOPIA Mode disabled

3.8.3 NPE-A UTOPIA Jumper Block (JP3)

The IXP465 network processor contains NPE pins that have multiple functions. The UTOPIA jumper block connects UTOPIA-specific signals to the UTOPIA mezzanine card connectors (J35 and P36). Table 30 shows the pin definitions for the UTOPIA jumper block as well as the JP3 jumper pin assignments, which depend on the SMII Configuration (CFG #) selected in Table 27. To find the location of JP3 on the IXDP465 baseboard, see Figure 11.

Table 30. NPE-A UTOPIA Jumper Block (JP3) Pin Assignments

JP3 Pin	Network Processor Signal	JP3 Pin	UTOPIA Signal	CFG #1	CFG #2	CFG #3	CFG #4	CFG #5	CFG #6	CFG #7	CFG #8
1	C_UTP_OP_DATA7	2	UTP_OP_DATA7	OPT	OPT	---	---	OPT	OPT	---	---
3	C_UTP_IP_DATA7	4	UTP_IP_DATA7	OPT	OPT	---	---	OPT	OPT	---	---
5	C_UTP_IP_CLK	6	UTP_IP_CLK	OPT	OPT	---	---	OPT	OPT	---	---
7	C_UTP_OP_CLK	8	UTP_OP_CLK	OPT	OPT	---	---	OPT	OPT	---	---
9	C_UTP_OP_DATA0	10	UTP_OP_DATA0	OPT	OPT	---	---	OPT	OPT	---	---
11	C_UTP_OP_DATA1	12	UTP_OP_DATA1	OPT	OPT	---	---	OPT	OPT	---	---
13	C_UTP_OP_DATA2	14	UTP_OP_DATA2	OPT	OPT	---	---	OPT	OPT	---	---
15	C_UTP_OP_DATA3	16	UTP_OP_DATA3	OPT	OPT	---	---	OPT	OPT	---	---
17	C_UTP_OP_DATA4	18	UTP_OP_DATA4	OPT	OPT	---	---	OPT	OPT	---	---
19	C_UTP_IP_DATA0	20	UTP_IP_DATA0	OPT	OPT	---	---	OPT	OPT	---	---
21	C_UTP_IP_DATA1	22	UTP_IP_DATA1	OPT	OPT	---	---	OPT	OPT	---	---
23	C_UTP_IP_DATA2	24	UTP_IP_DATA2	OPT	OPT	---	---	OPT	OPT	---	---
25	C_UTP_IP_DATA3	26	UTP_IP_DATA3	OPT	OPT	---	---	OPT	OPT	---	---
27	C_UTP_IP_DATA4	28	UTP_IP_DATA4	OPT	OPT	---	---	OPT	OPT	---	---
29	C_UTP_IP_DATA5	30	UTP_IP_DATA5	OPT	OPT	---	---	OPT	OPT	---	---
31	C_UTP_IP_DATA6	32	UTP_IP_DATA6	OPT	OPT	---	---	OPT	OPT	---	---

Notes:

Table Key:
--- = JP3 jumpers must NOT be installed
OPT = JP3 jumpers can optionally be installed (all 16 jumpers IN) to enable NPE-A UTOPIA Mode with NPE-A MII Mode disabled

3.8.4 NPE-B MII Jumper Block (JP4)

The IXP465 network processor contains NPE pins that have multiple functions. The NPE-B MII jumper block connects specific shared NPE signals to the MII NPE-B mezzanine card. Table 31 shows the pin definitions for the NPE-B MII jumper block as well as the JP4 jumper pin assignments, which depend on the SMII Configuration (CFG #) selected in Table 27. To find the location of JP4 on the IXDP465 baseboard, see Figure 11.

Table 31. NPE-B MII Jumper Block (JP4) Pin Assignments

JP4 Pin	Network Processor Signal	JP4 Pin	MII Signal	CFG #1	CFG #2	CFG #3	CFG #4	CFG #5	CFG #6	CFG #7	CFG #8
1	C_ETHB_TXCLK	2	ETHB_TXCLK	OPT	OPT	OPT	OPT	---	---	---	---
3	C_ETHB_TXDATA0	4	ETHB_TXDATA0	OPT	OPT	OPT	OPT	---	---	---	---
5	C_ETHB_TXDATA1	6	ETHB_TXDATA1	OPT	OPT	OPT	OPT	---	---	---	---
7	C_ETHB_TXDATA2	8	ETHB_TXDATA2	OPT	OPT	OPT	OPT	---	---	---	---
9	C_ETHB_TXDATA3	10	ETHB_TXDATA3	OPT	OPT	OPT	OPT	---	---	---	---
11	C_ETHB_RXDATA0	12	ETHB_RXDATA0	OPT	OPT	OPT	OPT	---	---	---	---
13	C_ETHB_RXDATA1	14	ETHB_RXDATA1	OPT	OPT	OPT	OPT	---	---	---	---
15	C_ETHB_RXDATA2	16	ETHB_RXDATA2	OPT	OPT	OPT	OPT	---	---	---	---
17	C_ETHB_RXDATA3	18	ETHB_RXDATA3	OPT	OPT	OPT	OPT	---	---	---	---
19	C_ETHB_CRS	20	ETHB_CRS	OPT	OPT	OPT	OPT	---	---	---	---

Notes:
Table Key:
--- = JP4 jumpers must NOT be installed
OPT = JP4 jumpers can optionally be installed (all 10 jumpers IN) to enable NPE-B MII Mode.

3.8.5 NPE-C MII Jumpers (JP65/JP93)

Note: JP65 and JP93 are currently identified as **ETH C** on the baseboard. To find the jumper location, see Figure 11.

The IXP465 network processor contains NPE pins that have multiple functions. The NPE-C MII jumpers connect specific shared NPE signals to the NPE-C mezzanine card. Table 32 shows the pin definitions for the NPE-C MII jumpers as well as the JP65/JP93 jumper pin assignments, which depend on the SMII Configuration (CFG #) selected in Table 27.

Table 32. NPE-C MII Jumpers (JP65/JP93) Pin Assignments

JP Pin	Network Processor Signal	JP Pin	MII Signal	CFG #1	CFG #2	CFG #3	CFG #4	CFG #5	CFG #6	CFG #7	CFG #8
JP65 pin 1	C_ETHC_TXDATA0	JP65 pin 2	ETHC_TXDATA0	OPT	OPT	OPT	OPT	---	---	---	---
JP93 pin 1	C_ETHC_RXDATA0	JP93 pin 2	ETHC_RXDATA0	OPT	OPT	OPT	OPT	---	---	---	---

Notes:
Table Key:
--- = JP65/JP93 jumper must NOT be installed
OPT = JP65/JP93 jumpers can optionally be installed (both jumpers IN) to enable NPE-C MII Mode.

3.9 MII Mezzanine Card Connectors

Support for MII is through three MII connectors. When the six-pack SMII is enabled, these connectors are disabled through the clock control CPLD. To be compatible with the IXDP425 / IXCDP1100 platform, the default mode is MII Mode. (That is, enable the three mezzanine card connectors and disable the 6-port SMII IC by holding in reset.) A module containing a single Ethernet PHY, wireless LAN, Home PNA, switch, or repeater is supported on each connector. The 802.3 standard MII connector can also be placed on a module to connect to the board's MII signals. An SMII PHY can also be used on this interface.

For detailed information about the MII mezzanine cards, see Section 5.2, IXPETM465 Ethernet Mezzanine Card. The connector on the baseboard is Amp 179031-5. Table 33 describes the pull-up and pull-down resistors required on the MII interface. The 10 KΩ resistor value was chosen so a module can easily drive over the pull-down. Decoupling is handled on each module.

Table 33. MII Resistors

Signal	Pull-To Value	Resistor Value
ETHA_RXDATA[3:0]	3.3 V	10 KΩ
ETHA_RXDV	3.3 V	10 KΩ
ETHA_COL	GND	10 KΩ
ETHA_CRS	3.3 V	10 KΩ
ETH_MDIO	3.3 V	10 KΩ
ETHB_RXDATA[3:0]	3.3 V	10 KΩ
ETHB_RXDV	3.3 V	10 KΩ
ETHB_COL	GND	10 KΩ
ETHB_CRS	3.3 V	10 KΩ
ETHC_RXDATA[3:0]	3.3 V	10 KΩ
ETHC_RXDV	3.3 V	10 KΩ
ETHC_COL	GND	10 KΩ
ETHC_CRS	3.3 V	10 KΩ
ETHA_TXCLK	3.3 V	10 KΩ
ETHA_RXCLK	3.3 V	10 KΩ
ETHB_TXCLK	3.3 V	10 KΩ
ETHB_RXCLK	3.3 V	10 KΩ
ETHC_TXCLK	3.3 V	10 KΩ
ETHC_RXCLK	3.3 V	10 KΩ

3.9.1 MII-0 Mezzanine Cards

To achieve compatibility with the IXDP425 / IXCDP1100 platform, the following features have been designed into the IXDP465 platform MII-0 mezzanine card standard connector:

- Connector part number Amp 5-179010-5
- Exact pin-out match with the IXDP425 connector

- Connection to MII on NPE-B
- Use of expansion bus chip select 4
- Use of expansion bus ready 0

The mezzanine card expansion connector has the following signal groups:

- IXP465 SPI
- IXP465 I^2C
- IXP465 extended expansion bus
- 16 GPIO
- Mezzanine Card ID byte (for stacking)
- 32 pins for future expansion (common to all mezzanine cards)
- 16 pins for future expansion (dedicated to this mezzanine card)
- Additional power

The IXDP465 platform MII-0 standard connector signals are described in Table 34. The power signals are +2.5 V, +3.3 V, +5.0 V and +12.0 V. The expansion bus signals provide the 16 LSB of the data bus, the 24 LSB of the address bus, chip select 4, clocking, and control to the mezzanine card for switching I/O and GPIO through software. There are MII signals connected to NPE-B and a few MII signals that are common across the MII devices. The GPIO signals route to the GPIO FPGA. The Legend describing the color-codes for the signals follows the table.

Note: The JTAG signals are not used.

Table 34. MII-0 Mezzanine Card Standard Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
-	1	EX_ADDR11	41	5.0 V	81
-	2	EX_ADDR10	42	3.3 V	82
-	3	EX_ADDR13	43	MII0_GPIO2	83
-	4	EX_ADDR12	44	MII0_GPIO3	84
EX_DATA1	5	EX_ADDR15	45	GND	85
EX_DATA0	6	EX_ADDR14	46	GND	86
EX_DATA3	7	GND	47	-	87
EX_DATA2	8	GND	48	MII0_GPIO4	88
MII0_GPIO0	9	EX_ADDR17	49	-	89
MII0_GPIO1	10	EX_ADDR16	50	RST_N	90
EX_DATA5	11	EX_ADDR19	51	-	91
EX_DATA4	12	EX_ADDR18	52	ETHB_TXEN	92
EX_DATA7	13	EX_ADDR21	53	-	93
EX_DATA6	14	EX_ADDR20	54	ETHB_RXDV	94
GND	15	EX_ADDR23	55	GND	95
GND	16	EX_ADDR22	56	ETHB_RXCLK	96
EX_DATA9	17	GND	57	ETHB_RXDATA3	97

Table 34. MII-0 Mezzanine Card Standard Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_DATA8	18	GND	58	GND	98
EX_DATA11	19	EX_CLK_MII0	59	ETHB_RXDATA2	99
EX_DATA10	20	EX_RD_N	60	ETHB_TXCLK	100
-	21	GND	61	ETHB_RXDATA1	101
-	22	EX_WR_N	62	ETHB_COL	102
EX_DATA13	23	EX_ALE	63	ETHB_RXDATA0	103
EX_DATA12	24	EX_RDY_N0	64	ETHB_TXDATA3	104
EX_DATA15	25	EX_IOWAIT_N	65	GND	105
EX_DATA14	26	ETHB_INT_N	66	ETHB_TXDATA2	106
GND	27	EX_CS_N4	67	ETHB_TXDATA1	107
GND	28	3.3 V	68	GND	108
EX_ADDR1	29	-	69	ETHB_TXDATA0	109
EX_ADDR0	30	3.3 V	70	ETH_MDC	110
EX_ADDR3	31	5.0 V	71	ETHB_CRS	111
EX_ADDR2	32	3.3 V	72	ETH_MDIO	112
EX_ADDR5	33	5.0 V	73	12 V	113
EX_ADDR4	34	3.3 V	74	2.5 V	114
EX_ADDR7	35	5.0 V	75	12 V	115
EX_ADDR6	36	3.3 V	76	2.5 V	116
GND	37	5.0 V	77	12 V	117
GND	38	3.3 V	78	2.5 V	118
EX_ADDR9	39	5.0 V	79	12 V	119
EX_ADDR8	40	3.3 V	80	2.5 V	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
GPIO signals	maroon
MII signals (connected to NPE-B)	black
MII signals (common)	red
not used (JTAG signals)	gray
interrupt signal	gold

The IXDP465 platform MII-0 expansion connector signal definition is described in Table 35. The power signals are +1.8 V, +3.3 V, and +5.0 V. The expansion bus signals provide the 16 MSB of the data bus and the 1 MSB of the address bus. The common (among all mezzanine cards) and dedicated (this mezzanine card only) future expansion signals connect to the network processor module and are intended for use with future peripherals. The SPI signals connect to the IXP465

network processor SPI peripheral. The I^2C signals connect to the IXP465 I^2C peripheral. The GPIO signals connect to the GPIO FPGA. The mezzanine card ID signals are used for board ID when stacking. The Legend describing the color-codes for the signals follows the table.

Table 35. MII-0 Mezzanine Card Expansion Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
1.8 V	1	C_PCI_4	41	3.3 V	81
1.8 V	2	C_PCI_5	42	3.3 V	82
GND	3	C_PCI_6	43	3.3 V	83
GND	4	C_PCI_7	44	3.3 V	84
EX_DATA17	5	C_PCI_8	45	GND	85
EX_DATA16	6	C_PCI_9	46	GND	86
EX_DATA19	7	EX_BE_N3	47	C_FN_11	87
EX_DATA18	8	EX_BE_N2	48	C_FN_12	88
GND	9	EX_BE_N1	49	C_FN_13	89
GND	10	EX_BE_N0	50	C_FN_14	90
EX_DATA21	11	EX_BURST	51	GND	91
EX_DATA20	12	EX_PAR3	52	GND	92
EX_DATA23	13	EX_PAR2	53	C_FN_15	93
EX_DATA22	14	EX_PAR1	54	MII0_GPIO5	94
GND	15	EX_PAR0	55	MII0_GPIO6	95
GND	16	C_NPE_0	56	MII0_GPIO7	96
EX_DATA25	17	C_NPE_1	57	GND	97
EX_DATA24	18	C_NPE_2	58	GND	98
EX_DATA27	19	C_NPE_3	59	MII0_GPIO8	99
EX_DATA26	20	C_NPE_4	60	MII0_GPIO9	100
GND	21	C_NPE_5	61	MII0_GPIO10	101
GND	22	C_NPE_6	62	MII0_GPIO11	102
EX_DATA29	23	C_NPE_7	63	GND	103
EX_DATA28	24	C_NPE_8	64	GND	104
EX_DATA31	25	C_NPE_9	65	MII0_GPIO12	105
EX_DATA30	26	C_NPE_10	66	MII0_GPIO13	106
GND	27	C_NPE_11	67	MII0_GPIO14	107
GND	28	C_NPE_12	68	MII0_GPIO15	108
EX_ADDR24	29	CLK32_MII0	69	GND	109
SSPS_CLK	30	C_FN_0	70	GND	110
SSPS_FRM	31	C_FN_1	71	GND (ID0)	111
SSPS_TXD	32	C_FN_2	72	3.3 V (ID1)	112
SSPS_RXD	33	C_FN_3	73	3.3 V (ID2)	113
SSPS_EXTCLK	34	C_FN_4	74	3.3 V (ID3)	114
5.0 V	35	C_FN_5	75	3.3 V (ID4)	115

Table 35. MII-0 Mezzanine Card Expansion Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
5.0 V	36	C_FN_6	76	3.3 V (ID5)	116
C_PCI_0	37	C_FN_7	77	3.3 V (ID6)	117
C_PCI_1	38	C_FN_8	78	3.3 V (ID7)	118
C_PCI_2	39	C_FN_9	79	I2C_SDA	119
C_PCI_3	40	C_FN_10	80	I2C_SCL	120

Legend	
power signals	purple
expansion bus signals	green
common future expansion signals	blue
dedicated future expansion signals (this card only)	black
SPI signals	red
I2C signals)	gold
GPIO signals	maroon
Clock signal	lavender

3.9.2 MII-1 Mezzanine Card

To achieve compatibility with the IXDP425 / IXCDP1100 platform, the following features have been designed into the IXDP465 platform interface standard connector for the MII-1 mezzanine card:

- Connector part number Amp 5-179010-5
- Exact pin-out match
- Connection to MII on NPE-C
- Uses expansion bus chip select 5
- Uses expansion bus ready 1

The mezzanine card expansion connector contains the following signal groups:

- IXP465 SPI
- IXP465 I^2C
- IXP465 extended expansion bus
- 16 GPIO
- Mezzanine Card ID byte (stacking)
- 32 pins for future expansion (common to all mezzanine cards)
- 16 pins for future expansion (dedicated to this mezzanine card)
- Additional power

The IXDP465 platform MII-1 standard connector signal definition is described in Table 36. The power signals are +2.5 V, +3.3 V, +5.0 V and +12.0 V. The expansion bus signals provide the 16 LSB of the data bus, the 24 LSB of the address bus, chip select 5, clocking and control to the mezzanine card. The interrupt signal from the mezzanine card is routed to the GPIO FPGA. There are MII signals connected to NPE-C and some MII signals are common across the MII devices. The GPIO signals route to the GPIO FPGA. The Legend describing the color-codes for the signals follows the table.

Note: The JTAG signals are not used.

Table 36. MII-1 Mezzanine Card Standard Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
-	1	EX_ADDR11	41	5.0 V	81
-	2	EX_ADDR10	42	3.3 V	82
-	3	EX_ADDR13	43	MII1_GPIO2	83
-	4	EX_ADDR12	44	MII1_GPIO3	84
EX_DATA1	5	EX_ADDR15	45	GND	85
EX_DATA0	6	EX_ADDR14	46	GND	86
EX_DATA3	7	GND	47	-	87
EX_DATA2	8	GND	48	MII1_GPIO4	88
MII1_GPIO0	9	EX_ADDR17	49	-	89
MII1_GPIO1	10	EX_ADDR16	50	RST_N	90
EX_DATA5	11	EX_ADDR19	51	-	91
EX_DATA4	12	EX_ADDR18	52	ETHC_TXEN	92
EX_DATA7	13	EX_ADDR21	53	-	93
EX_DATA6	14	EX_ADDR20	54	ETHC_RXDV	94
GND	15	EX_ADDR23	55	GND	95
GND	16	EX_ADDR22	56	ETHC_RXCLK	96
EX_DATA9	17	GND	57	ETHC_RXDATA3	97
EX_DATA8	18	GND	58	GND	98
EX_DATA11	19	EX_CLK_MII1	59	ETHC_RXDATA2	99
EX_DATA10	20	EX_RD_N	60	ETHC_TXCLK	100
-	21	GND	61	ETHC_RXDATA1	101
-	22	EX_WR_N	62	ETHC_COL	102
EX_DATA13	23	EX_ALE	63	ETHC_RXDATA0	103
EX_DATA12	24	EX_RDY_N1	64	ETHC_TXDATA3	104
EX_DATA15	25	EX_IOWAIT_N	65	GND	105
EX_DATA14	26	ETHC_INT_N	66	ETHC_TXDATA2	106
GND	27	EX_CS_N5	67	ETHC_TXDATA1	107
GND	28	3.3 V	68	GND	108
EX_ADDR1	29	-	69	ETHC_TXDATA0	109
EX_ADDR0	30	3.3 V	70	ETH_MDC	110

Table 36. MII-1 Mezzanine Card Standard Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_ADDR3	31	5.0 V	71	ETHC_CRS	111
EX_ADDR2	32	3.3 V	72	ETH_MDIO	112
EX_ADDR5	33	5.0 V	73	12 V	113
EX_ADDR4	34	3.3 V	74	2.5 V	114
EX_ADDR7	35	5.0 V	75	12 V	115
EX_ADDR6	36	3.3 V	76	2.5 V	116
GND	37	5.0 V	77	12 V	117
GND	38	3.3 V	78	2.5 V	118
EX_ADDR9	39	5.0 V	79	12 V	119
EX_ADDR8	40	3.3 V	80	2.5 V	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
GPIO signals	maroon
MII signals (connected to NPE-B	black
MII signals (common)	red
not used (JTAG signals)	gray
interrupt signal	gold

The IXDP465 platform MII-1 expansion connector signal definition is described in Table 37. The power signals are +1.8 V, +3.3 V, and +5.0 V. The expansion bus signals provide the 16 MSB of the data bus and the 1 MSB of the address bus. The common (among all mezzanine cards) and dedicated (this mezzanine card only) future expansion signals connect to the network processor module and are intended for use with future peripherals. The SPI signals connect to the IXP465 network processor SPI peripheral. The I^2C signals connect to the IXP465 I^2C peripheral. The GPIO signals connect to the GPIO FPGA. The mezzanine card ID signals are used for board ID when stacking. The Legend describing the color-codes for the signals follows the table.

Table 37. MII-1 Mezzanine Card Expansion Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
1.8 V	1	C_PCI_4	41	3.3 V	81
1.8 V	2	C_PCI_5	42	3.3 V	82
GND	3	C_PCI_6	43	3.3 V	83
GND	4	C_PCI_7	44	3.3 V	84
EX_DATA17	5	C_PCI_8	45	GND	85
EX_DATA16	6	C_PCI_9	46	GND	86
EX_DATA19	7	EX_BE_N3	47	C_FN_27	87
EX_DATA18	8	EX_BE_N2	48	C_FN_28	88

Table 37. MII-1 Mezzanine Card Expansion Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	9	EX_BE_N1	49	C_FN_29	89
GND	10	EX_BE_N0	50	C_FN_30	90
EX_DATA21	11	EX_BURST	51	GND	91
EX_DATA20	12	EX_PAR3	52	GND	92
EX_DATA23	13	EX_PAR2	53	C_FN_31	93
EX_DATA22	14	EX_PAR1	54	MII1_GPIO5	94
GND	15	EX_PAR0	55	MII1_GPIO6	95
GND	16	C_NPE_0	56	MII1_GPIO7	96
EX_DATA25	17	C_NPE_1	57	GND	97
EX_DATA24	18	C_NPE_2	58	GND	98
EX_DATA27	19	C_NPE_3	59	MII1_GPIO8	99
EX_DATA26	20	C_NPE_4	60	MII1_GPIO9	100
GND	21	C_NPE_5	61	MII1_GPIO10	101
GND	22	C_NPE_6	62	MII1_GPIO11	102
EX_DATA29	23	C_NPE_7	63	GND	103
EX_DATA28	24	C_NPE_8	64	GND	104
EX_DATA31	25	C_NPE_9	65	MII1_GPIO12	105
EX_DATA30	26	C_NPE_10	66	MII1_GPIO13	106
GND	27	C_NPE_11	67	MII1_GPIO14	107
GND	28	C_NPE_12	68	MII1_GPIO15	108
EX_ADDR24	29	CLK32_MII1	69	GND	109
SSPS_CLK	30	C_FN_16	70	GND	110
SSPS_FRM	31	C_FN_17	71	GND (ID0)	111
SSPS_TXD	32	C_FN_18	72	3.3 V (ID1)	112
SSPS_RXD	33	C_FN_19	73	3.3 V (ID2)	113
SSPS_EXTCLK	34	C_FN_20	74	3.3 V (ID3)	114
5.0 V	35	C_FN_21	75	3.3 V (ID4)	115
5.0 V	36	C_FN_22	76	3.3 V (ID5)	116
C_PCI_0	37	C_FN_23	77	3.3 V (ID6)	117
C_PCI_1	38	C_FN_24	78	3.3 V (ID7)	118
C_PCI_2	39	C_FN_25	79	I2C_SDA	119
C_PCI_3	40	C_FN_26	80	I2C_SCL	120

Legend	
power signals	purple
expansion bus signals	green
common future expansion signals	blue

Legend (Continued)	
dedicated future expansion signals (this card only)	black
SPI signals	red
I^2C signals)	gold
GPIO signals	maroon
Clock signal	lavender

3.9.3 MII-2 Mezzanine Cards

The following features have been designed into the IXDP465 platform interface standard connector for the MII-2 mezzanine card:

- Connector part number Amp 5-179010-5
- Pin-out similar to that used on the IXDP425 development platform
- Connection to MII on NPE-A
- Uses expansion bus chip select 7
- Uses expansion bus ready 2

The mezzanine card expansion connector contains the following signal groups:

- IXP465 SPI
- IXP465 I^2C
- IXP465 extended expansion bus
- 16 GPIO
- Mezzanine card ID byte (for stacking)
- 32 pins for future expansion (common to all mezzanine cards)
- 17 pins for future expansion (dedicated to this mezzanine card)
- Additional power

The IXDP465 platform MII-2 standard connector signal definition is described in Table 38. The power signals are +2.5 V, +3.3 V, +5.0 V and +12.0 V. The expansion bus signals provide the 16 LSB of the data bus, the 24 LSB of the address bus, chip select 7, clocking, and control to the mezzanine card. The interrupt signal from the mezzanine card is routed to the GPIO FPGA. The MII signals are connected to NPE-A. The MII signals are common across the MII devices. The GPIO signals route to the GPIO FPGA. The Legend describing the color-codes for the signals follows the table.

Note: The JTAG signals are not used.

Table 38. MII-2 Mezzanine Card Standard Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
-	1	EX_ADDR11	41	5.0 V	81
-	2	EX_ADDR10	42	3.3 V	82
-	3	EX_ADDR13	43	MII2_GPIO2	83
-	4	EX_ADDR12	44	MII2_GPIO3	84
EX_DATA1	5	EX_ADDR15	45	GND	85
EX_DATA0	6	EX_ADDR14	46	GND	86
EX_DATA3	7	GND	47	-	87
EX_DATA2	8	GND	48	MII2_GPIO4	88
MII2_GPIO0	9	EX_ADDR17	49	-	89
MII2_GPIO1	10	EX_ADDR16	50	RST_N	90
EX_DATA5	11	EX_ADDR19	51	-	91
EX_DATA4	12	EX_ADDR18	52	ETHA_TXEN	92
EX_DATA7	13	EX_ADDR21	53	-	93
EX_DATA6	14	EX_ADDR20	54	ETHA_RXDV	94
GND	15	EX_ADDR23	55	GND	95
GND	16	EX_ADDR22	56	ETHA_RXCLK	96
EX_DATA9	17	GND	57	ETHA_RXDATA3	97
EX_DATA8	18	GND	58	GND	98
EX_DATA11	19	EX_CLK_MII2	59	ETHA_RXDATA2	99
EX_DATA10	20	EX_RD_N	60	ETHA_TXCLK	100
-	21	GND	61	ETHA_RXDATA1	101
-	22	EX_WR_N	62	ETHA_COL	102
EX_DATA13	23	EX_ALE	63	ETHA_RXDATA0	103
EX_DATA12	24	EX_RDY_N2	64	ETHA_TXDATA3	104
EX_DATA15	25	EX_IOWAIT_N	65	GND	105
EX_DATA14	26	ETHA_INT_N	66	ETHA_TXDATA2	106
GND	27	EX_CS_N7	67	ETHA_TXDATA1	107
GND	28	3.3 V	68	GND	108
EX_ADDR1	29	-	69	ETHA_TXDATA0	109
EX_ADDR0	30	3.3 V	70	ETH_MDC	110
EX_ADDR3	31	5.0 V	71	ETHA_CRS	111
EX_ADDR2	32	3.3 V	72	ETH_MDIO	112
EX_ADDR5	33	5.0 V	73	12 V	113
EX_ADDR4	34	3.3 V	74	2.5 V	114
EX_ADDR7	35	5.0 V	75	12 V	115
EX_ADDR6	36	3.3 V	76	2.5 V	116
GND	37	5.0 V	77	12 V	117

Table 38. MII-2 Mezzanine Card Standard Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	38	3.3 V	78	2.5 V	118
EX_ADDR9	39	5.0 V	79	12 V	119
EX_ADDR8	40	3.3 V	80	2.5 V	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
GPIO signals	maroon
MII signals (connected to NPE-B	black
MII signals (common)	red
not used (JTAG signals)	gray
interrupt signal	gold

The IXDP465 platform MII-2 expansion connector signal definition is described in Table 39. The power signals are +1.8 V, +3.3 V, and +5.0 V. The expansion bus signals provide the 16 MSB of the data bus and the 1 MSB of the address bus. The common (among all mezzanine cards) and dedicated (this mezzanine card only) future expansion signals connect to the network processor module and are intended for use with future peripherals. The SPI signals connect to the IXP465 network processor SPI peripheral. The I^2C signals connect to the IXP465 I^2C peripheral. The GPIO signals connect to the GPIO FPGA. The mezzanine card ID signals are used for board ID when stacking. The Legend describing the color-codes for the signals follows the table.

Table 39. MII-2 Mezzanine Card Expansion Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
1.8 V	1	C_PCI_4	41	3.3 V	81
1.8 V	2	C_PCI_5	42	3.3 V	82
GND	3	C_PCI_6	43	3.3 V	83
GND	4	C_PCI_7	44	3.3 V	84
EX_DATA17	5	C_PCI_8	45	GND	85
EX_DATA16	6	C_PCI_9	46	GND	86
EX_DATA19	7	EX_BE_N3	47	C_FN_43	87
EX_DATA18	8	EX_BE_N2	48	C_FN_44	88
GND	9	EX_BE_N1	49	C_FN_45	89
GND	10	EX_BE_N0	50	C_FN_46	90
EX_DATA21	11	EX_BURST	51	GND	91
EX_DATA20	12	EX_PAR3	52	GND	92
EX_DATA23	13	EX_PAR2	53	C_FN_47	93
EX_DATA22	14	EX_PAR1	54	MII2_GPIO5	94
GND	15	EX_PAR0	55	MII2_GPIO6	95

Table 39. MII-2 Mezzanine Card Expansion Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	16	C_NPE_0	56	MII2_GPIO7	96
EX_DATA25	17	C_NPE_1	57	GND	97
EX_DATA24	18	C_NPE_2	58	GND	98
EX_DATA27	19	C_NPE_3	59	MII2_GPIO8	99
EX_DATA26	20	C_NPE_4	60	MII2_GPIO9	100
GND	21	C_NPE_5	61	MII2_GPIO10	101
GND	22	C_NPE_6	62	MII2_GPIO11	102
EX_DATA29	23	C_NPE_7	63	GND	103
EX_DATA28	24	C_NPE_8	64	GND	104
EX_DATA31	25	C_NPE_9	65	MII2_GPIO12	105
EX_DATA30	26	C_NPE_10	66	MII2_GPIO13	106
GND	27	C_NPE_11	67	MII2_GPIO14	107
GND	28	C_NPE_12	68	MII2_GPIO15	108
EX_ADDR24	29	CLK32_MII2	69	GND	109
SSPS_CLK	30	C_FN_32	70	GND	110
SSPS_FRM	31	C_FN_33	71	GND (ID0)	111
SSPS_TXD	32	C_FN_34	72	3.3 V (ID1)	112
SSPS_RXD	33	C_FN_35	73	3.3 V (ID2)	113
SSPS_EXTCLK	34	C_FN_36	74	3.3 V (ID3)	114
5.0 V	35	C_FN_37	75	3.3 V (ID4)	115
5.0 V	36	C_FN_38	76	3.3 V (ID5)	116
C_PCI_0	37	C_FN_39	77	3.3 V (ID6)	117
C_PCI_1	38	C_FN_40	78	3.3 V (ID7)	118
C_PCI_2	39	C_FN_41	79	I2C_SDA	119
C_PCI_3	40	C_FN_42	80	I2C_SCL	120

Legend	
power signals	purple
expansion bus signals	green
common future expansion signals	blue
dedicated future expansion signals (this card only)	black
SPI signals	red
I2C signals)	gold
GPIO signals	maroon
Clock signal	lavender

3.10 USB Device

A Type-B USB device receptacle is provided at the board edge. A 1.5 KΩ pull-up resistor is applied on D+ USB pin to indicate the IXDP465 baseboard is a full-speed USB device. This pull-up is enabled/disabled through software control. (The USB design is identical to that on the IXDP425 / IXCDP1100 platform.)

Table 40 shows the USB device connector pin definition.

Table 40. USB Device Connector Pin Definition

USB Device (J8)	Signal
1	5.0V_USB (input)
2	USB_DNEG
3	USB_DPOS
4	GND

The IXDP465 baseboard cannot be powered as a downstream device through the USB interface due to the board's high power requirements.

The interface is capable of operation at 1.5 Mbits/s and 12 Mbits/s.

3.11 USB Host

A Type-A USB **host** receptacle is provided at the board edge. The USB host interface is compliant with USB 2.0. Table 41 shows the USB host connector pin definition.

Table 41. USB Host Connector Pin Definition

USB Device (J7)	Signal
1	5.0V_USB (output)
2	USB_HNEG
3	USB_HPOS
4	GND

The interface is capable of operation at 1.5 Mbits/s and 12 Mbits/s.

3.12 Serial Ports

Two dedicated asynchronous serial I/O ports (UARTs) with flow control are provided. Both ports are routed to 9-pin DB connectors with RTS and CTS flow control. Both serial ports include support for full modem control through four GPIOs. The interface supports baud rates of 1200 to 921.6 Kbits/s.

The ports are wired according to the RS-232 specification for data communication equipment. Straight serial cable connects to the host PC. Table 42 shows the pin definitions for the serial port DB-9 connectors.

Table 42. Serial Port DB-9 Connector Pin Definitions

UART0 (J9)	Signal	UART1 (J5)	Signal
1	UART0_DCD_B_L	1	UART1_DCD_B_L
2	UART0_TXD_B_L	2	UART1_TXD_B_L
3	UART0_RXD_B_L	3	UART1_RXD_B_L
4	UART0_DTR_B_L	4	UART1_DTR_B_L
5	UART0_GND_B_L	5	UART1_GND_B_L
6	UART0_DSR_B_L	6	UART1_DSR_B_L
7	UART0_CTS_B_L	7	UART1_CTS_B_L
8	UART0_RTS_B_L	8	UART1_RTS_B_L
9	UART0_RI_B_L	9	UART1_RI_B_L

To allow full modem control on the UART connections, four GPIOs generate the RS-232 signals (DTR, DSR, RI, and DCD) that are not explicitly generated by the IXDP465 platform. Because of pin limitations in the GPIO FPGA and the low priority of modem signaling, the modem control signals are shared with the GPIO from MII-2.

Note: Allowing full modem control on the UART connections provides legacy support for the IXDP425 / IXCDP1100 platform.

Hardware modifications (the addition of 0 Ω resistors) were necessary to enable modem control signals for both serial ports. Table 43 shows the modem signals that are shared with MII-2 GPIO and the associated resistor that has been added to the IXDP465 platform.

Table 43. Serial Port DB-9 Modem Signal Alternate Functions

Signal	Shared MII-2 GPIO	Resistor
UART0_DCD	MII2_GPIO<10>	R301N
UART0_DSR	MII2_GPIO<11>	R299N
UART0_RI	MII2_GPIO<12>	R297N
UART0_DTR	MII2_GPIO<13>	R295N
UART1_DCD	MII2_GPIO<6>	R300N
UART1_DSR	MII2_GPIO<7>	R298N
UART1_RI	MII2_GPIO<8>	R296N
UART1_DTR	MII2_GPIO<9>	R294N

3.12.1 DB-9 Connector EMI Considerations

To reduce susceptibility to EMI from the cable, 0.1 µF capacitors are placed on all nine signals, including ground. These capacitors are discharged (routed) to earth ground.

3.12.2 Serial Port Pull-Ups / Pull-Downs

Receive signal lines are pulled down through a 5 KΩ resistor on the RS-232 side within the transceiver. Since data signals are inverted, the IXDP465 baseboard sees a pull-up on these lines. To allow additional signal conditioning in case the internal pull-down is not strong enough, an unpopulated pull-up has been placed on the IXDP465 baseboard-side Receive signals. A 10 KΩ resistor strength is suggested for these pull-ups in the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

The transceiver does not include pull-ups on transmitter inputs. Unused inputs must be pulled to valid logic levels. Therefore, DSR, RI, and DCD are pulled high to ensure that these inputs are valid when full modem control is not used. Since the transceiver inverts its inputs, the DSR, RI, and DCD signals are de-asserted (active high) when they are driven through the connector. Table 44 shows the serial port resistor signals and values.

Table 44. Serial Port Resistors

Signal	Pull to Value	Resistor Value
URT_CTS0_N	None	None
URT_CTS1_N	None	None
URT_RXD0	None	None
URT_RXD1	None	None
URT_DSR0	+3.3 V	10 KΩ
URT_DSR1	+3.3 V	10 KΩ
URT_RI0	+3.3 V	10 KΩ
URT_RI1	+3.3 V	10 KΩ
URT_DCD0	+3.3 V	10 KΩ
URT_DCD1	+3.3 V	10 KΩ
URT_DTR0	None	None
URT_DTR1	None	None

3.13 GPIO

The GPIOs are mapped to many purposes on the IXDP465 platform. An FPGA routes GPIO to I/O (any GPIO to any I/O) or interrupt signals for all peripherals, eliminating the need for jumpers. This FPGA places the routing of signals to all 16 GPIOs under software control. Any I/O from the mezzanine cards (or onboard peripherals) is routed internally by the FPGA through software control to any of the GPIOs. Each GPIO has a green LED indicator attached to it, which when illuminated, indicates a low state (0 VDC). The LEDs are shown in Figure 14 on page 82. DIP switches are placed on each LED to allow the LED to be disconnected from the GPIO and reduce loading. See Figure 7 on page 37 for the DIP switch locations. The default setting for these switches is LEDs illuminated (ON position).

GPIO15 is a user-programmable output with the default state being a 33 MHz clock output. The clock supports a maximum frequency of 33 MHz, with various duty cycle steps.

The default state for GPIO14 is an input that is configured as an output (user-programmable). The clock supports a maximum frequency of 33 MHz, with various duty cycle steps.

The GPIO is designed for easy access by probing through a header. Table 45 lists the GPIO header pin definitions.

Table 45. GPIO Header Pin Definition

Pin	Signal	Pin	Signal
1	3.3 V	11	GPIO8
2	5.0 V	12	GPIO9
3	GPIO0	13	GPIO10
4	GPIO1	14	GPIO11
5	GPIO2	15	GPIO12
6	GPIO3	16	GPIO13
7	GPIO4	17	GPIO14
8	GPIO5	18	GPIO15
9	GPIO6	19	GND
10	GPIO7	20	GND

3.13.1 GPIO FPGA Access

Because of pin limitations on the FPGA, access to this device is through indirect addressing. Only the lower two address bits of the expansion bus are available to the FPGA for address decode. To access the GPIO configuration registers, the software must first set up the configuration register address in the Indirect Address register and then the actual access can occur by reading or writing to the Indirect Data register. **FPGA_BASE_ADD** is found in the address decode table for expansion bus chip select 2. Table 46 lists the FPGA registers.

Table 46. GPIO FPGA Access Registers

Expansion Bus Address	Register	Access Type (8-bit)
FPGA_BASE_ADD + 0	Indirect Address	R/W
FPGA_BASE_ADD + 1	Indirect Data	R/W
FPGA_BASE_ADD + 2	Revision	RO
FPGA_BASE_ADD + 3	Scratch Pad	R/W

3.13.2 GPIO FPGA Control Signals

The GPIO FPGA is configured and accessed through the expansion bus (chip select 2). Table 47 defines the signals (and FPGA pin locations) for the expansion bus connection.

Table 47. GPIO FPGA Access Signals (Sheet 1 of 2)

Signal	Description	FPGA Pin #	Signal	Description	FPGA Pin #
FPGA_PROG_N	Used during configuration of FPGA	106	GPIO3	Network Processor GPIO3	33
FPGA_INIT_N	Used during configuration of FPGA	107	GPIO4	Network ProcessorGPIO4	34
FPGA_DONE	Used during configuration of FPGA	104	GPIO5	Network Processor GPIO5	35
FPGA_CS_N	Used during configuration of FPGA, and during normal access by IXP465 network processor	160	GPIO6	Network Processor GPIO6	36
FPGA_MODE0	Used during configuration of FPGA. This signal must be tied to GND.	52	GPIO7	Network Processor GPIO7	37
FPGA_MODE1	Used during configuration of FPGA. This signal must be tied to 3.3 V with a 10 kΩ resistor.	50	GPIO8	Network Processor GPIO8	41
FPGA_MODE2	Used during configuration of FPGA. This signal must be tied to GND.	54	GPIO9	Network Processor GPIO9	42
FPGA_CFG_WR_N	Used during configuration of FPGA. This signal must be tied to GND.	161	GPIO10	Network Processor GPIO10	43
FPGA_TCK	Unused. This signal must be tied to 3.3 V with a 1 kΩ resistor.	207	GPIO11	Network Processor GPIO11	44
FPGA_TMS	Unused. This signal must be tied to 3.3 V with a 10 kΩ resistor.	2	GPIO12	Network Processor GPIO12	45
FPGA_TDI	Unused. This signal must be tied to 3.3 V with a 10 kΩ resistor.	159	GPIO13	Network Processor GPIO13	46
FPGA_TDO	Unused. This signal must be tied to 3.3 V with a 10 kΩ resistor.	157	GPIO14	Network Processor GPIO14	47
EX_ADDR1	Expansion bus address 1. Used for address decode of internal FPGA registers.	111	GPIO15	Network Processor GPIO15	48
EX_ADDR0	Expansion bus address 10 Used for address decode of internal FPGA registers.	112	GPIO16†	Network Processor GPIO16	5
EX_DATA7	Expansion bus data 7. Used during configuration and register access.	108	GPIO17†	Network Processor GPIO17	6
EX_DATA6	Expansion bus data 6. Used during configuration and register access.	115	GPIO18†	Network Processor GPIO18	7

† Network Processor GPIO16 - GPIO31 are not available on the IXP465 network processor and are reserved for future use.

Table 47. GPIO FPGA Access Signals (Sheet 2 of 2)

Signal	Description	FPGA Pin #	Signal	Description	FPGA Pin #
EX_DATA5	Expansion bus data 5. Used during configuration and register access.	119	GPIO19†	Network Processor GPIO19	8
EX_DATA4	Expansion bus data 4. Used during configuration and register access.	126	GPIO20†	Network Processor GPIO20	9
EX_DATA3	Expansion bus data 3. Used during configuration and register access.	135	GPIO21†	Network Processor GPIO21	10
EX_DATA2	Expansion bus data 2. Used during configuration and register access.	142	GPIO22†	Network Processor GPIO22	14
EX_DATA1	Expansion bus data 1. Used during configuration and register access.	146	GPIO23†	Network Processor GPIO23	15
EX_DATA0	Expansion bus data 0. Used during configuration and register access.	153	GPIO24†	Network Processor GPIO24	16
EX_WR_N	Expansion bus write signal. Used during configuration and register access.	80, 155	GPIO25†	Network Processor GPIO25	17
EX_RD_N	Expansion bus read signal. Used during register access.	182	GPIO26†	Network Processor GPIO26	18
EX_CLK_FPGA	Expansion bus clock signal. Used during register access.	77	GPIO27†	Network Processor GPIO27	20
RST_N	System reset signal. Initializes default register values.	185	GPIO28†	Network Processor GPIO28	21
GPIO0	Network Processor GPIO0	29	GPIO29†	Network Processor GPIO29	22
GPIO1	Network Processor GPIO1	30	GPIO30†	Network Processor GPIO30	23
GPIO2	Network Processor GPIO2	31	GPIO31†	Network Processor GPIO31	24

† Network Processor GPIO16 - GPIO31 are not available on the IXP465 network processor and are reserved for future use.

3.13.3 GPIO FPGA Configuration Registers

To avoid conflicts where multiple hardware drivers are driving the same signal simultaneously, the following rule must be followed to properly configure the I/O. The destination signal (input) must be configured first, then the source (output) is configured. As an example, if GPIO4 is to be connected to **HSS0_INT_N**, then GPIO4 must be configured first, since it is an input, then **HSS0_INT_N** is configured since it is an output. All signals (GPIO from the network processor, and all signals from the mezzanine cards) are configured as inputs after a reset. Each mezzanine card GPIO has two configuration registers associated with the signal. The **Attach** register defines to which network processor GPIO the signal is attached. The **Direction** register defines the signal direction. The mezzanine card signal direction must be the opposite direction of the network processor GPIO. Table 48 defines the configuration register bit definitions.

Table 48. GPIO FPGA Configuration Register Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0
Dir	Attach6	Attach5	Attach4	Attach3	Attach2	Attach1	Attach0

The **Dir** bit defines the mezzanine card GPIO signal direction. Table 49 defines the **Dir** bit settings.

Table 49. GPIO FPGA Direction Bit Definition

Dir	Direction (from FPGA Pin to Network Processor)
0	Input[a]
1	Output

a. Default direction is **Input** to the FPGA after reset.

The **attach** value defines the mezzanine card GPIO signal that the associated network processor GPIO is attached to, or it is not attached. Table 50 shows the GPIO attach values, the associated mezzanine card GPIO signal, and the FPGA pin to which the signal is routed.

Table 50. GPIO FPGA Attach Values and FPGA Pin Assignments (Sheet 1 of 2)

Att	Signal	FPGA Pin #	Att	Signal	FPGA Pin #	Att	Signal	FPGA Pin #	Att	Signal	FPGA Pin #
0	ETHB_GPIO0	187	32	ETHA_GPIO0	132	64	HSS1_GPIO0	102	96	Reserved	n/a
1	ETHB_GPIO1	188	33	ETHA_GPIO1	133	65	HSS1_GPIO1	57	97	Reserved	n/a
2	ETHB_GPIO2	189	34	ETHA_GPIO2	134	66	HSS1_GPIO2	58	98	Reserved	n/a
3	ETHB_GPIO3	191	35	ETHA_GPIO3	136	67	HSS1_GPIO3	59	99	Reserved	n/a
4	ETHB_GPIO4	192	36	ETHA_GPIO4	138	68	HSS1_GPIO4	60	10	Reserved	n/a
5	ETHB_GPIO5	193	37	ETHA_GPIO5	139	69	HSS1_GPIO5	61	101	Reserved	n/a
6	ETHB_GPIO6	194	38	ETHA_GPIO6	140	70	HSS1_GPIO6	62	102	Reserved	n/a
7	ETHB_GPIO7	195	39	ETHA_GPIO7	141	71	HSS1_GPIO7	63	103	Reserved	n/a
8	ETHB_GPIO8	199	40	ETHA_GPIO8	147	72	HSS1_GPIO8	67	104	Reserved	n/a
9	ETHB_GPIO9	200	41	ETHA_GPIO9	148	73	HSS1_GPIO9	68	105	Reserved	n/a
10	ETHB_GPIO10	201	42	ETHA_GPIO10	149	74	HSS1_GPIO10	69	106	Reserved	n/a
11	ETHB_GPIO11	202	43	ETHA_GPIO11	150	75	HSS1_GPIO11	70	107	Reserved	n/a
12	ETHB_GPIO12	203	44	ETHA_GPIO12	151	76	HSS1_GPIO12	71	108	Reserved	n/a
13	ETHB_GPIO13	204	45	ETHA_GPIO13	152	77	HSS1_GPIO13	73	109	Reserved	n/a
14	ETHB_GPIO14	205	46	ETHA_GPIO14	109	78	HSS1_GPIO14	74	110	Reserved	n/a
15	ETHB_GPIO15	206	47	ETHA_GPIO15	110	79	HSS1_GPIO15	75	111	Reserved	n/a
16	ETHC_GPIO0	162	48	HSS0_GPIO0	81	80	PCI_INTA_N[1]	113	112	Reserved	n/a
17	ETHC_GPIO1	163	49	HSS0_GPIO1	82	81	PCI_INTB_N[2]	114	113	Reserved	n/a

Notes:
1. PCI_INTA_N is an output from FPGA attached to network processor GPIO11 after reset as PCI Host interrupt.
2. PCI_INTB_N is an output from FPGA attached to network processor GPIO10 after reset as PCI Host interrupt.
3. PCI_INTC_N is an output from FPGA attached to network processor GPIO9 after reset as PCI Host interrupt.
4. PCI_INTD_N is an output from FPGA attached to network processor GPIO8 after reset as PCI Host interrupt.
5. Network processor GPIOs default to Not Attached after a reset, except where indicated.

Table 50. GPIO FPGA Attach Values and FPGA Pin Assignments (Sheet 2 of 2)

Att	Signal	FPGA Pin #	Att	Signal	FPGA Pin #	Att	Signal	FPGA Pin #	Att	Signal	FPGA Pin #
18	ETHC_GPIO2	164	50	HSS0_GPIO2	83	82	PCI_INTC_N[3]	120	114	Reserved	n/a
19	ETHC_GPIO3	165	51	HSS0_GPIO3	84	83	PCI_INTD_N[4]	121	115	Reserved	n/a
20	ETHC_GPIO4	166	52	HSS0_GPIO4	86	84	ETHA_INT_N	125	116	Reserved	n/a
21	ETHC_GPIO5	167	53	HSS0_GPIO5	87	85	ETHB_INT_N	127	117	Reserved	n/a
22	ETHC_GPIO6	168	54	HSS0_GPIO6	88	86	ETHC_INT_N	129	118	Reserved	n/a
23	ETHC_GPIO7	172	55	HSS0_GPIO7	89	87	HSS0_INT_N	49	119	Reserved	n/a
24	ETHC_GPIO8	173	56	HSS0_GPIO8	90	88	HSS1_INT_N	27	120	Reserved	n/a
25	ETHC_GPIO9	174	57	HSS0_GPIO9	94	89	UTP_GPIO0	154	121	Reserved	n/a
26	ETHC_GPIO10	175	58	HSS0_GPIO10	95	90	GASP_INT_N	101	122	Reserved	n/a
27	ETHC_GPIO11	176	59	HSS0_GPIO11	96	91	UTP_GPIO1	3	123	Reserved	n/a
28	ETHC_GPIO12	178	60	HSS0_GPIO12	97	92	UTP_GPIO2	4	124	Reserved	n/a
29	ETHC_GPIO13	179	61	HSS0_GPIO13	98	93	UTP_GPIO3	122	125	Reserved	n/a
30	ETHC_GPIO14	180	62	HSS0_GPIO14	99	94	DSL_INT_N	123	126	Reserved	n/a
31	ETHC_GPIO15	181	63	HSS0_GPIO15	100	95	Reserved	n/a	127	Reserved	Not Attached[5]

Notes:
1. PCI_INTA_N is an output from FPGA attached to network processor GPIO11 after reset as PCI Host interrupt.
2. PCI_INTB_N is an output from FPGA attached to network processor GPIO10 after reset as PCI Host interrupt.
3. PCI_INTC_N is an output from FPGA attached to network processor GPIO9 after reset as PCI Host interrupt.
4. PCI_INTD_N is an output from FPGA attached to network processor GPIO8 after reset as PCI Host interrupt.
5. Network processor GPIOs default to Not Attached after a reset, except where indicated.

Table 51. Alternate GPIO Functions

Standard GPIO Signal	Alternate GPIO Signal	Signal Description	Resistor Reference Designator
ETHA_GPIO10	UTP_GPIO4	GPIO4 signal from the IXDP425 development platform UTOPIA connector	R32N
ETHA_GPIO11	MDINT_N1	Interrupt from the LXT9785 Octal Ethernet PHY	R33N
ETHA_GPIO12	MDINT_N2	Interrupt from the LXT9785 Octal Ethernet PHY	R34N
ETHA_GPIO13	UTP_RDY_N	Ready signal from the ADSL mezzanine card	R35N
ETHA_GPIO14	UTP_MODE	Mode signal from the ADSL mezzanine card	R36N
ETHA_GPIO15	UTP_GPIO5	GPIO5 signal from the IXDP425 development platform UTOPIA connector.	R37N

Note: Because of hardware limitations, some GPIOs are shared with the mezzanine card for NPE-A. These shared signals involve installing 0 Ω resistors that do not come factory installed. For further information, please reference the baseboard schematics for exact resistor installation options that support different NPE-A related platform configurations.

3.14 I²C Interface

This interface conforms to the I²C bus standard developed by Phillips Corporation. (For detailed information, refer to *Peripherals for Microcontrollers*.) The interface consists of a Serial Data/Address signal (SDA) and a Serial Clock (SCL). The interface supports two performance modes; standard (100 kbits/s) and fast (400 kbits/s).

A 512 byte I²C EEPROM (Philips PCF8594C-2TD) is connected to the IXP465 network processor through the I²C peripheral interface. The I²C interface is routed to each mezzanine card through the expansion connector. A jumper is included that write-protects the device when it's not installed. See Figure 11 for the jumper location.

All mezzanine cards respond to inquiries across the I²C interface with their board status. This status includes the **Board ID** (type) and **Board Revision**. The status information provided by the I²C interface is defined in Table 52.

Table 52. I²C Status Information

Bit	7	6	5	4	3	2	1	0
Status	Board ID				Board Revision			

The **Board ID**s for IXDP465 platform mezzanine cards are listed in Table 53.

Table 53. Mezzanine Card Board IDs

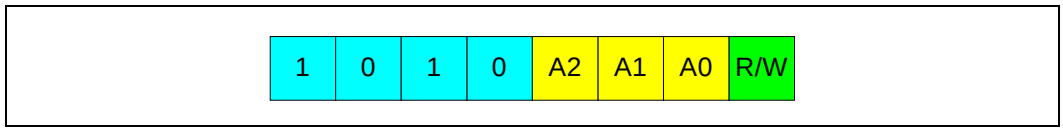
Board ID	Mezzanine Card
0000	Reserved
0001	Network Processor Module (x16)
0010	Reserved
0011	Reserved
0100	Analog Voice 4x1
0101	Quad T1/E1
0110	Reserved
0111-1111	Reserved

The network processor module has jumpers that allow switching between using GPIO and the I²C network processor pins. The default factory configuration uses the I²C pins of the IXP465 network processor. See Figure 17 on page 98 for the JP46 jumper location.

3.14.1 I²C Addressing

To avoid conflicts where multiple I²C devices are connected to the same bus, unique addresses must be used. The IXDP465 platform has an onboard EEPROM, the CPLD on the CPU mezzanine card, plus up to five other mezzanine cards connected to the I²C bus. Figure 12 shows the I²C address byte.

Figure 12. I²C Address Byte



The first four bits (shown in blue) are a fixed alternating pattern. The next three bits (shown in yellow) are the address bits for each peripheral. The last bit (shown in green) defines if this is a read or a write. The EEPROM on the IXDP465 platform must have A2-A0 set to 000 for access. Any other pattern can be used in the design of mezzanine cards.

The I²C EEPROM is 512 bytes. Table 54 lists the I²C addresses.

Table 54. I²C EEPROM Addresses

I²C Address	Length (in Bytes)	Description
0x000	256	Free form configuration string (used by VxWorks)
0x100	6	Ethernet MAC address for NPE-B0
0x106	6	Ethernet MAC address for NPE-C
0x10C	6	Ethernet MAC address for NPE-A
0x112	6	Ethernet MAC address for NPE-B1
0x118	6	Ethernet MAC address for NPE-B2
0x11E	6	Ethernet MAC address for NPE-B3
0x124	20	Ethernet IP address for NPE-B0
0x138	20	Ethernet IP address for NPE-C
0x14C	20	Ethernet IP address for NPE-A
0x160	20	Ethernet IP address for NPE-B1
0x174	20	Ethernet IP address for NPE-B2
0x188	20	Ethernet IP address for NPE-B3
0x19C	20	Ethernet IP address for PCI-NIC Slot-0
0x1B0	20	Ethernet IP address for PCI-NIC Slot-1
0x1C4	20	Ethernet IP address for PCI-NIC Slot-2
0x1D8	20	Ethernet IP address for PCI-NIC Slot-3
0x1EC	20	Reserved

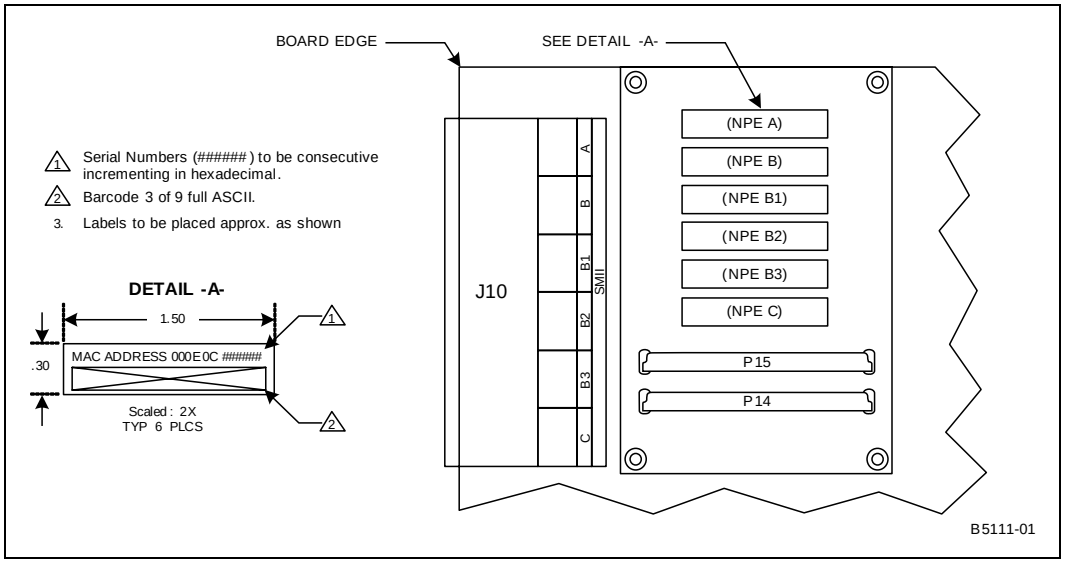
Notes:

1. MAC addresses are 6 bytes long and stored as binary. For example, 00:0E:0C:74:FF:08 is stored as 0x00, 0x0E, 0x0C, 0x74, 0xFF, 0x08
2. IP addresses are up to 20 bytes long and stored as character strings. For example, 192.168.111.222 is stored as 0x31, 0x39, 0x32, 0x2E, 0x31, 0x36, 0x38, 0x2E, 0x31, 0x31, 0x31, 0x2E, 0x32, 0x32, 0x32, 0x00

Most of the illustrations and photos in this manual show the factory default installation of the MII Ethernet PHY mezzanine card plugged into the MII-0 NPE-B position. As a result, the six NPE MAC address labels on IXDP465 baseboard top side are not visible because they are underneath

the MII Ethernet card. Figure 13 illustrates the location and identification of the six labels which are positioned next to the multi-pack MII interfaces. If MAC addresses are required for development, the MII Ethernet card must be temporarily removed to view the MAC address labels.

Figure 13. MAC Address Labels



3.15 SPI Interface

The SPI interface on the IXDP465 platform supports the following interfaces:

- National Semiconductor Corporation* MICROWIRE*
- Texas Instruments Incorporated* Synchronous Serial Protocol (SSP)
- Motorola* Serial Peripheral Interface (SPI)

This interface operates in a master mode and supports serial bit rates from 7.2 KHz to 1.84 MHz. DMA support is not required for this interface.

The SPI interface is routed to each mezzanine card through the expansion connector.

3.16 LED Indicators

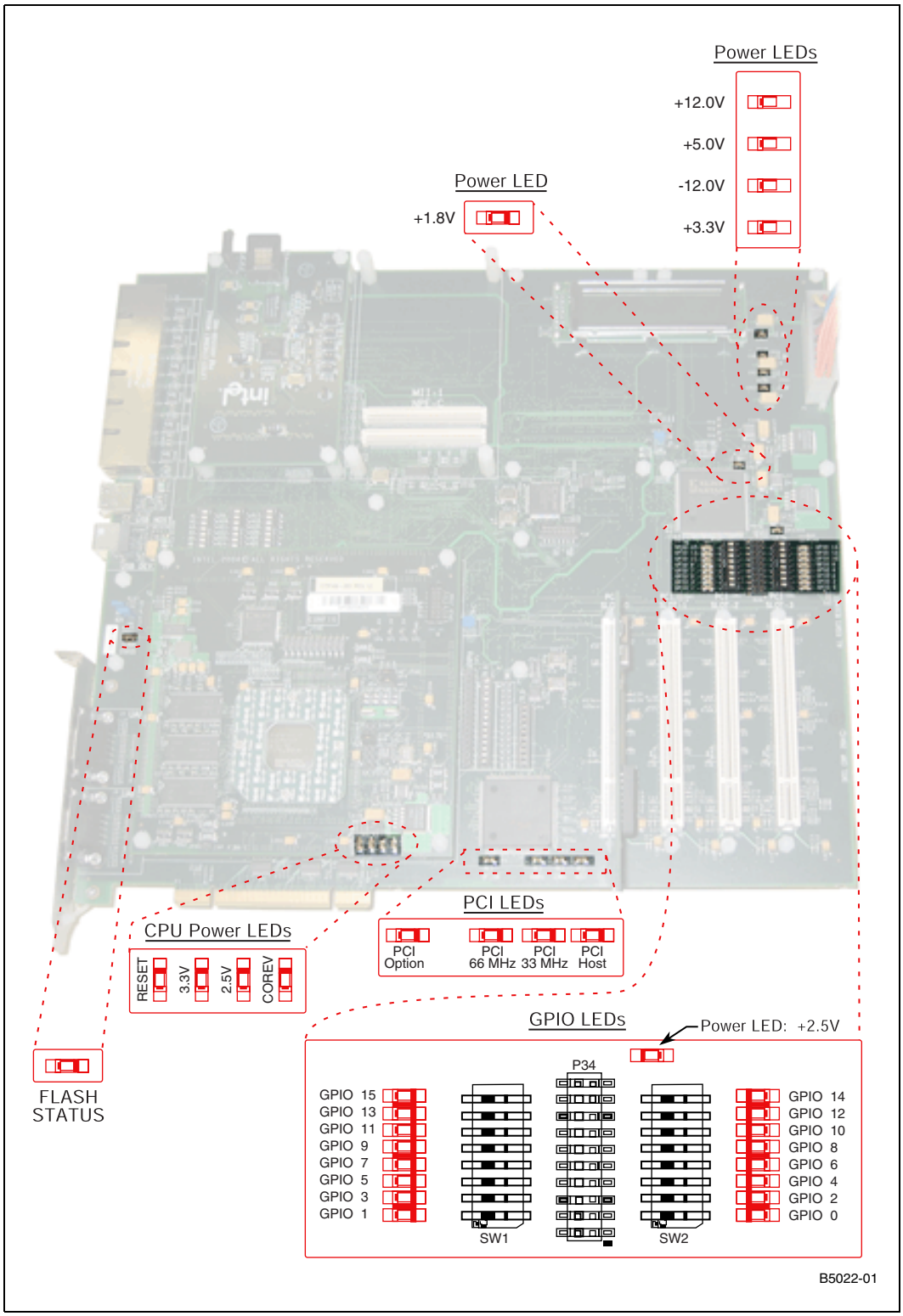
Figure 55 describes the LEDs placed on the IXDP465 platform as indicators.

Figure 14 shows the LED locations for all LEDs on the IXDP465 platform.

Table 55. Intel® IXDP465 Development Platform LED Indicator Definitions

LED Name (See Figure 14)	LED Indication when ON	Color	Default Settings	Location
Power LED: +12 V	+12 V power is on	Green	ON	Baseboard
Power LED: +5 V	+5 V power is on	Green	ON	Baseboard
Power LED: -12 V	-12 V power is on	Green	ON	Baseboard
Power LED: +3.3 V	+3.3 V power is on	Green	ON	Baseboard
Power LED: +1.8 V	+1.8 V power is on	Green	ON	Baseboard
PCI LED: Option	PCI operating as option	Green	OFF	Baseboard
PCI LED: 66 MHz	PCI operating at 66 MHz	Green	ON	Baseboard
PCI LED: 33 MHz	PCI operating at 33 MHz	Green	OFF	Baseboard
PCI LED: Host	PCI operating as host	Green	ON	Baseboard
CPU Power LED: Reset	IXP465 system is in reset	Green	OFF	NPM
CPU Power LED: 3.3 V	+3.3 V power is applied to IXP465	Green	ON	NPM
CPU Power LED: 2.5 V	+2.5 V power is applied to IXP465	Green	ON	NPM
CPU Power LED: COREV	+1.3 V/+1.5 V power is applied to IXP465	Green	ON	NPM
GPIO LEDs: GPIO 0 - GPIO 15	GPIO[15:0] driven low	Green	ON	Baseboard
GPIO LEDs: Power LED	+2.5 V power is on	Green	ON	Baseboard
FLASH STATUS	Flash device is being programmed	Yellow	OFF	Baseboard

Figure 14. LED Locations



3.17 Debug Circuitry

An Intel® 10/100 EthernetPro Adapter card using the Intel® 82559 Ethernet PHY component can be plugged into a PCI slot and used as the debug Ethernet port.

3.18 JTAG Interface

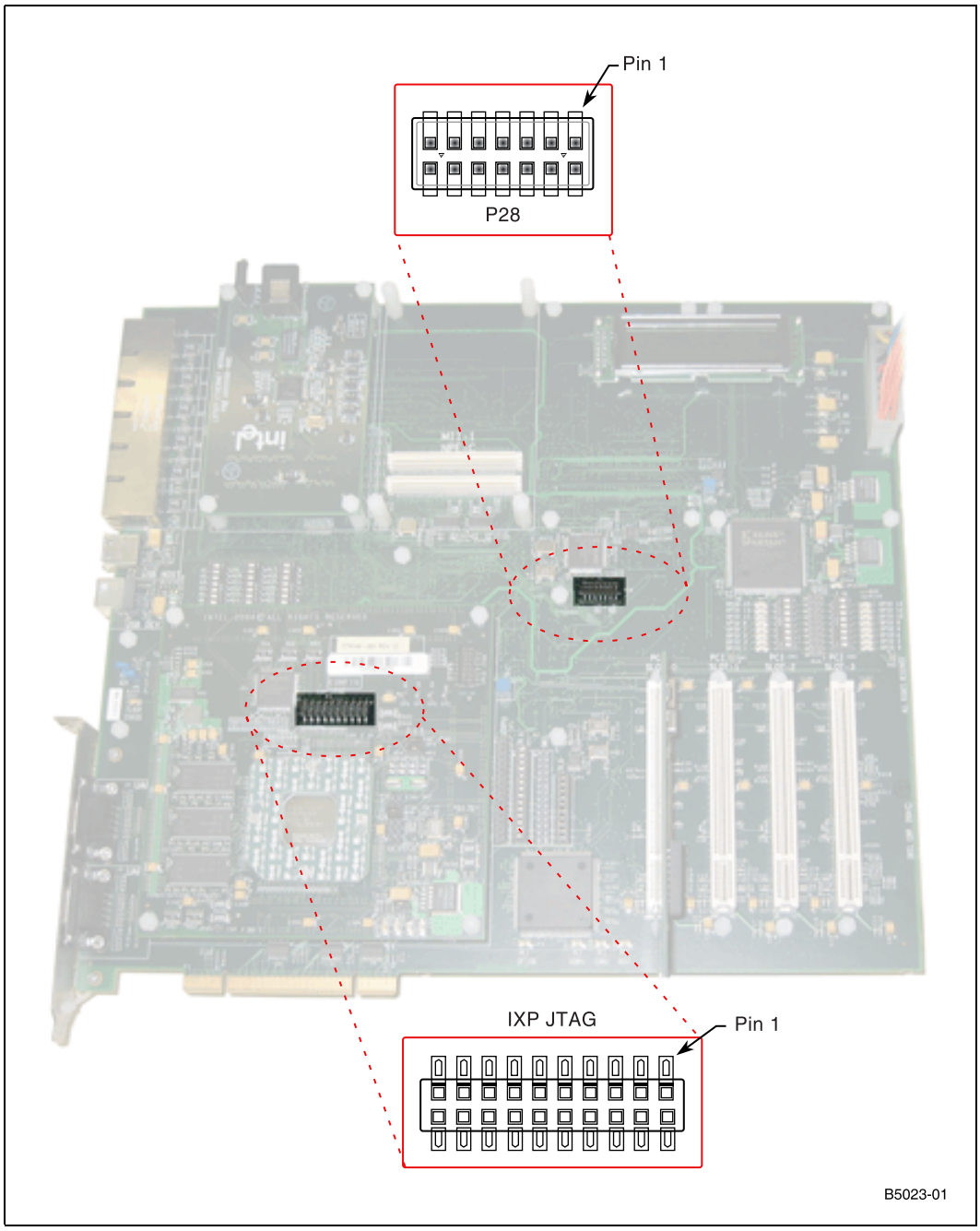
The IXP465 network processor is controlled during debug through a JTAG interface to the processor. The Macraigor Raven* and Wind River visionPROBE* / visionICE* systems plug into the JTAG interface through a 20-pin connector. Figure 15 shows the JTAG interface location.

The main difference between the Raven and visionICE systems is the specific implementation of **nTRST** for each debugger. The Macraigor Raven implementation actively drives **nTRST** (high and low). The Wind River visionPROBE / visionICE can configure **nTRST** Active or Open Collector (only drive low). The application note, *Recommended JTAG Circuitry for Debug with Intel® XScale Microarchitecture* (Intel® Document Number 273538), recommends a 10 kΩ pull-down on **TRST**. Table 56 shows the emulator header pin definitions.

Table 56. Emulator Connector Pin Assignments

Pin	Signal	Pin	Signal
1	+3.3 V	2	+3.3 V
3	IXP_TRST_N	4	GND
5	IXP_TDI	6	GND
7	IXP_TMS	8	GND
9	IXP_TCLK	10	GND
11	GND	12	GND
13	IXP_TDO	14	GND
15	SYSRESET_IXP_N	16	GND
17	GND	18	GND
19	GND	20	GND

Figure 15. JTAG Emulator and CPLD Programming Headers



3.19 Power

Power rails are generated on the IXDP465 platform through a connector to an external standard ATX power supply. The following voltages are provided: 3.3 V, 5 V, 12 V, -12 V, and GND.

The power sequence is:

1. +12.0 V, -12.0 V, +5.0 V, and +3.3 V
2. +2.5 V
3. +1.3 V/+1.5 V (+1.5 V for IXP465 network processor operating at 667 MHz only)

The only power sequencing requirement on the board comes from the IXP465 network processor, which requires that +3.3 V and +2.5 V comes up before +1.3 V/+1.5 V. (This voltage is generated on the network processor module.)

When the IXDP465 platform is the host PCI system, power must be provided by an external power supply connected to the platform plug connection. When the IXDP465 baseboard is used as an option card in a PCI system, power is still provided by the external module (eliminating complications generated by the PCI 25W limitation).

The +1.3 V/+1.5 V core voltage required by the IXP465 network processor has been designed directly onto the IXDP465 platform network processor module. +1.3 V/+1.5 V is generated from +3.3 V using the National Semiconductor LP3966ES-ADJ power regulator.

To meet the overall power requirements, the IXDP465 platform uses an external ATX supply. Table 57 depicts the IXDP465 platform's typical power distribution, although mezzanine cards can draw more power as long as the total system wattage does not exceed 180W. If needed, a higher wattage supply can be purchased separately.

Table 57. IXDP465 Development Platform Power Distribution

Peripheral	Power Dissipation (max)
Host PCI Slot 0	25 W
Host PCI Slot 1	25 W
Host PCI Slot 2	25 W
Host PCI Slot 3	25 W
Network Processor module	30 W
HSS-0 mezzanine card	7 W
HSS-1 mezzanine card	7 W
MII-0 mezzanine card	7 W
MII-1 mezzanine card	7 W
MII-2 mezzanine card	7 W
ADSL mezzanine card	7 W
IXDP465 baseboard	8 W
Total	180 W

The power module plugs into the baseboard through a standard ATX 20-pin power supply connector (P1). Table 58 defines the pinout for this connector.

Table 58. ATX Power Supply Connector Pin Assignments

Connector Pin #	Signal
1	+3.3 V
2	+3.3 V
3	GND
4	+5.0 V
5	GND
6	+5.0 V
7	GND
8	NC
9	NC
10	+12.0 V
11	+3.3 V
12	-12.0 V
13	GND
14	ATX_ENB_N
15	GND
16	GND
17	GND
18	NC
19	+5.0 V
20	+5.0 V

The power supply shipped with the IXDP465 platform is the Autec PSG180B-80. This is an 180 W, 6 output 1U power supply. Table 59 lists the power supply maximum current output.

Table 59. PSG180B-80 Power Supply Output Specifications

Voltage	+5.0 V	+12.0 V	+3.3 V	-12.0 V
Max Current	25.0 A	11.0 A	22.0 A	3.0 A
Regulation	±5%	±5%	±5%	±5%
Ripple	50 mV	120 mV	50 mV	120 mV

The IXDP465 platform has the capability to monitor the total wattage required by the IXP465 network processor for a given application. There are three jumpers on the Network Processor Module for monitoring current. See Figure 17 on page 98 for the voltage jumpers location.

3.19.1 Monitoring +3.3 V Current

To monitor the IXP465 network processor's current requirements for a given application, perform the hardware modifications described below.

For the +3.3 V rail:

1. Remove R443 and R444 from the IXP465 network processor module (near the IXP 3.3 V jumper).
2. Add a wire loop across the IXP 3.3 V jumper.
3. Attach an inductive current probe to the wire loop to measure the current.

See Figure 17 on page 98 for the IXP 3.3 V jumper location.

3.19.2 Monitoring +2.5 V Current

To monitor the IXP465 network processor's current requirements for a given application, perform the hardware modifications described below.

For the +2.5 V rail:

1. Remove R445 and R446 from the IXP465 network processor module (near the JP46 IXP 2.5 V jumper).
2. Add a wire loop across JP46.
3. Attach an inductive current probe to the wire loop to measure the current.

See Figure 17 on page 98 for the JP46 IXP 2.5 V jumper location.

3.19.3 Monitoring Core Voltage Current (+1.3 V/+1.5 V)

To monitor the IXP465 network processor's current requirements for a given application, perform the hardware modifications described below.

For the core voltage rail:

1. Remove R447 and R448 from IXP465 network processor module (near the JP47 IXP COREV jumper).
2. Add a wire loop across the JP47.
3. Attach an inductive current probe to the wire loop to measure the current.

See Figure 17 on page 98 for the JP47 IXP COREV jumper location.

3.20 Reset Logic

The system reset is generated for several cases on the IXDP465 platform:

- Power rails are not at appropriate levels
- System reset generated out of JTAG circuitry (ICE or boundary scan)
- PCI Option Mode reset

The IXDP465 platform is reset when a system reset is generated. In addition, it is reset when it is in PCI Option mode and the PCI host asserts reset.

JTG_TRST_N must be asserted (driven low) during reset. Otherwise, the TAP controller may not initialize and lock the processor. There is a weak (10 kΩ) pull-down resistor on **JTG_TRST_N**.

3.21 Clocking

The following interfaces require oscillators on the board:

- IXP465 system clock - 33.33 MHz
- UTOPIA transmit and receive clock - 33.33 MHz (may be disabled through jumper option)
- PCI host clock - 33.0 MHz and 66.0 MHz selectable
- Expansion bus clock - 80.0 MHz external oscillator or GPIO15-selectable (jumper option)
- SMII clock - 125 MHz

The expansion bus and PCI can share their 33.00 MHz oscillator. The expansion bus clock is selected from the following frequencies under software control (processor read/write of clock control CPLD):

- 33.0 MHz
- 40.0 MHz
- 66.0 MHz
- 80.0 MHz

Although UTOPIA also requires 33 MHz oscillators, a separate oscillator allows the oscillator frequency to be altered or disabled independently. The IXDP465 platform contains a 33.33 MHz oscillator that is used for test mode only. Installation of JP9 and JP11 places a 33.33 MHz signal on both the **UTP_OP_CLK** and the **UTP_IP_CLK**. See Figure 11 for these jumper locations and Table 30 for the JP3 UTOPIA jumper block pin assignments.

The PCI clock is driven from the PCI option fingers when the IXDP465 platform is in Option mode and is driven by the Clock Control CPLD when the IXDP465 platform is the host. The clock is driven through a clock driver in Host mode and clock selection is automatic.

The core voltage is adjustable with processor speed. For example, for 667 MHz operations, the 667 MHz jumper must be removed. See Figure 17 on page 98 for the jumper location.

The expansion bus clock is generated by the clock control CPLD. The frequency of this clock is software-selectable.

The UTOPIA transmit and receive clock is disabled through a jumper option when the clock is driven from the Network Processor Module (i.e. when the IXP465 network processor is acting as the PHY). See Figure 11 on page 53 for the jumper location and settings.

The HSS clocks are sourced either out of the IXP465 network processor or from an HSS mezzanine card. There is no oscillator on the IXDP465 baseboard for an HSS clock. The IXP465 network processor drives the clock at a software-programmable frequency out to the HSS mezzanine cards. The IXDP465 platform defaults to an external HSS clock source. External clocks are placed on the mezzanine cards as the HSS clock source, and a 32.768 MHz clock signal (propagated by the IXDP465 platform) is available to all mezzanine cards for telephony applications.

3.22 Clock Control CPLD

The Clock Control CPLD is used for the following:

- Address Decode for expansion bus chip select 2
  - CPLD Internal Registers
  - GPIO FPGA Chip Select
  - LCD Display Control
- Expansion Bus Clock Generation
  - 33 MHz
  - 40 MHz
  - 66 MHz
  - 80 MHz
- Expansion Bus Address Configuration Switch Overrides
- PCI Functions
  - Host Clock Generation
  - Option Sensing
  - Isolation Buffer Control
  - LEDs

The Clock Control CPLD is pre-programmed by the factory with the features defined in this manual. A JTAG Header is provisioned on the platform, to allow re-programming of the CPLD for designs that require customized modes. See Figure 15 on page 84 for the header location.

3.22.1 Address Decode

The Clock Control CPLD uses the upper five address bits of the expansion bus (**EX_ADDR24 - EX_ADDR20**) to further divide the address space for expansion bus slot #2. This decoding is necessary to multiplex this CPLD's internal registers, the GPIO FPGA's internal registers, and to access the LCD display. Table 60 shows the external address decode performed by this CPLD.

Table 60. Clock Control CPLD External Address Decode

EX_ADDR "xx"					Expansion Bus Resource	Physical Expansion Bus Address
24	23	22	21	20		
0	0	0	0	0	Clock Gen CPLD Registers	0x54000000 – 0x5407FFFF
0	0	0	0	1	GPIO FPGA Chip Select	0x54100000 – 0x541FFFFF
0	0	0	1	0	LCD Display Instruction	0x54200000 – 0x542FFFFF
0	0	0	1	1	LCD Display Data	0x54300000 – 0x543FFFFF
1	1	1	x	x	Reserved	0x54400000 – 0x54FFFFFF

Note: Since the IXDP465 platform uses a 32 Mbyte flash device, "extended" addressing must be used for the expansion bus decode versus the 16 Mbyte addressing used on the IXDP425 platform. (0x54xxxxxx versus 0x52xxxxxx)

3.22.1.1 CPLD Internal Registers

The Clock Control CPLD uses the lower five address bits of the expansion bus (**EX_ADDR4 - EX_ADDR0)** to further divide the address space for expansion bus slot #2. Table 61 shows the internal address decode performed by this CPLD.

Table 61. Clock Control CPLD Internal Address Decode

EX_ADDR "xx"					Expansion Bus Resource	Physical Expansion Bus Address	Access Type
4	3	2	1	0			
0	0	0	0	0	Control Status	0x54000000	R/W
0	0	0	0	1	PCI Host Present	0x54000001	RO
0	0	0	1	0	PCI Host 66 MHz Enable	0x54000002	RO
0	0	0	1	1	FPGA Programming	0x54000003	R/W
1	1	1	X	X	Reserved	0x54000004 - 0x5400000F	--

Note: Since the IXDP465 platform uses a 32 Mbyte flash device, "extended" addressing must be used for the expansion bus decode versus the 16 Mbyte addressing used on the IXDP425 platform. (0x54xxxxxx versus 0x52xxxxxx)

3.22.1.1.1 Control/Status Register

The expansion bus is software programmable for 33 MHz, 40 MHz, 66 MHz, or 80 MHz. The USB device pull-up enable is also software programmable. The LCD timer status is Read Only. The Expansion Bus Clock select is a Read or Write register whose bit definitions are defined in Table 62.

Table 62. Control Status Register Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0
LCD_TIME (4)	LCD_TIME (3)	LCD_TIME (2)	LCD_TIME (1)	LCD_TIME (0)	USB_DEV_PU_ENB	F1	F0

Table 63 lists the definitions of the Control Status register's expansion bus frequency control bits. The expansion bus clock frequency is controlled by **F(1:0**) of the Control Status register. The default frequency after a reset is 33 MHz.

Table 63. Expansion Bus Frequency Select Bit Definitions

F1	F0	Expansion Bus Frequency
0	0	33 MHz (default after reset)
0	1	40 MHz
1	0	66 MHz
1	1	80 MHz

The Control Status Register's USB Device Pull-Up Enable (**USB_DEV_PU_ENB**) bit allows (under software control) enabling and disabling the pull-up on the USB Device positive signal of the differential output pair. This indicates to the USB Host that a valid USB device is present. Any

IXDP465 platform reset disables this pull-up (default after reset is disabled), and indicates to the host that no device is present. Once this pull-up is re-enabled through software, the USB Host re-configures/re-initializes for the “new” device.

The Control Status register’s **LCD_TIME(4:0)** bits indicate how many expansion bus clock cycles are left before the next LCD access begins. Before the LCD Display Instruction register or the LCD Display Data register is written, the software verifies these bits have a value of **00000**. The default value after reset is **00000**.

3.22.1.1.2 PCI Host Present Register

The PCI Host Present Register (Table 64) is a Read-Only register that allows the software to determine if a board is physically plugged into one of the four PCI host slots (valid in PCI Host mode only). The software can also determine the power that the add-in card requires by the state of these bits. PCI Host Slot #3 is represented by D7 - D6, Slot #2 by D5 - D4, Slot #1 by D3 - D2 and Slot #0 by D1 - D0.

Table 64. PCI Host Present Register Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0
S3-2	S3-1	S2-2	S2-1	S1-2	S1-1	S0-2	S0-1

Note: Where **Sn-2** and **Sn-1** are:
00 = Add-in card present (7.5 W max)
01 = Add-in card present (15 W max)
10 = Add-in card present (25 W max)
11 = No add-in card present

3.22.1.1.3 PCI Host 66 MHz Enable Register

The PCI Host 66 MHz Enable register (Table 65) is a Read-Only register that allows the software to determine if a board plugged into one of the four PCI host slots (valid in PCI Host mode only) is capable of 66 MHz operation. PCI Host Slot #3 is represented by D3, Slot #2 by D2, Slot #1 by D1 and Slot #0 by D0.

Table 65. PCI Host 66 MHz Enable Register Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	M66EN3	M66EN2	M66EN1	M66EN0

Note: Where **X** is undefined and **M66ENn** is:
0 = 33 MHz only
1 = 33 MHz or 66 MHz

3.22.1.1.4 FPGA Programming Register

The FPGA Programming register (Table 66) is a Read or Write register that is used for programming (configuration) the GPIO FPGA.

Table 66. FPGA Programming Register Bit Definitions

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	DONE	INIT_N	PROG_N

Notes:

1. Where **X** is undefined and **PROG_N** is an active low output:
   0 = Program the FPGA
   1 = Normal Operation
2. Where **INIT_N** is an active low input output (RO - write has no effect):
   0 = FPGA initializing internal resources (after PROG_N active)
   1 = Normal Operation
3. Where **INIT_N** is an active high input output (RO - write has no effect):
   0 = Programming not complete
   1 = Programming complete

3.22.1.2 GPIO FPGA Chip Select

The GPIO FPGA Chip Select is a pass through, active low chip select that is generated when the proper address range is accessed on the expansion bus.

3.22.1.3 LCD Display Instruction Register

The LCD Display Instruction is a Write Only register that sends commands (such as Reset, Blank Display, Position Cursor, etc.) to the LCD display. After each write of the display, the Control/Status register **LCD_TIME** bits must be monitored before the next command is sent to the LCD display. Refer to the *Seiko L1672 LCD display (Model L167200J00)* data sheet for programming information.

3.22.1.4 LCD Display Data Register

The LCD Display Data is a Write Only register that sends alpha-numeric character data to the LCD display. After each write of the display, the Control/Status register **LCD_TIME** bits must be monitored before the next display data is sent to the LCD display. Refer to the *Seiko L1672 LCD display (Model L167200J00)* data sheet for programming information.

3.22.2 Expansion Bus Address Switch Configuration Overrides

The clock control CPLD overrides the user-selectable switches attached to the expansion bus to ensure that the hardware is set to the proper configuration values.This is necessary for proper PCI operation (Host vs. Option) and proper flash width. The remaining configuration straps are not overridden. Table 67 shows the configuration straps that are overridden by the clock control CPLD.

Table 67. Configuration Straps Override

Configuration Strap Overridden (Expansion Bus address)	Hardware "Locked" Value
8/16_FLASH (0)	0 = 16-bit (logic 0 by CPLD) 1 = 8-bit (illegal)
PCI_HOST (1)	0 = PCI Option (when **PCI_OPT_GND** logic 0) 1 = PCI Host (when **PCI_OPT_GND** logic 1)
PCI_ARB (2)	0 = Arbiter disabled (when **PCI_OPT_GND** logic 0) 1 = Arbiter Enabled (when **PCI_OPT_GND** logic 1)
PCI_TEST (3)	0 = PCI Test Mode (illegal) 1 = PCI Normal Operation (logic 1 by CPLD)
32_FLASH (7)	0 = 8/16-bit (logic 0 by CPLD) 1 = 32-bit (illegal)

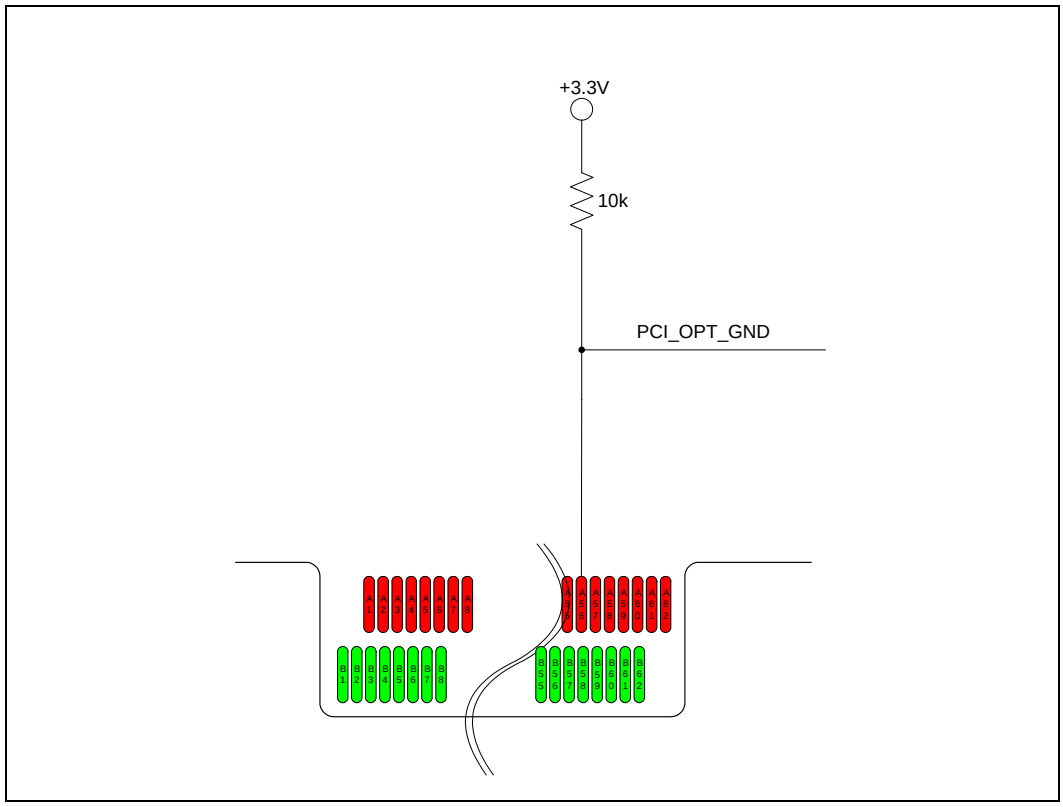
3.22.3 PCI Host Clock Generation

The clock control CPLD, when in Host mode, monitors the **M66EN** signal from each of the four host slots during **Reset Active** to determine the PCI Host slots frequency. If any of the four are not in their active state (logic 1), then the PCI host clock frequency is 33 MHz. If all four are in their active state, then the PCI host clock frequency is 66 MHz.

3.22.4 PCI Option Sensing

The IXDP465 platform automatically determines at reset time whether or not it is plugged into a PCI slot. If it determines that it is plugged in, it places itself in the PCI Option mode state. In this case, the clock control CPLD will override whatever the user configuration strap settings are set to. If not, then it automatically places itself in the Host mode state. In this case, the clock control CPLD overrides whatever the user configuration strap settings are set to. Figure 16 depicts the circuit that generates the **PCI_HOST_N** and **PCI_OPT_N** signals that generate the proper configuration bootstraps as well as in the PCI clock control CPLD (**PCI_OPT_CLK** or onboard generated host clock).

Figure 16. PCI Mode Select Circuit Diagram



3.22.5 PCI Isolation Buffer Control

The PCI Bus is divided into three segments. One section connects to the network processor module. The second is connected to the four PCI slots (Host mode). The third is connected to the PCI fingers (Option mode). A set of tri-state buffers isolates these sections. The PCI mode select circuit shown in Figure 16 determines which set of buffers is enabled and which are tri-stated. The Enables for these buffers are controlled by the Clock Control CPLD.

3.22.6 PCI LEDs

There are four LEDs that indicate the PCI status on the IXDP465 platform. Table 68 shows what each one means when it is on. LED control is performed by the Clock Control CPLD (based on PCI mode and Host Clock Frequency). When in PCI Option mode, the only LED illuminated is the **OPTION MODE** LED. In Host mode, two of the final three will be illuminated, the **HOST MODE** LED and either the **33 MHz** LED or **66 MHz** LED.

See Figure 14 on page 82 for the LED location.

Table 68. LED Definitions

LED	LED Indication When ON	Color
PCI Host	PCI is in host mode	Green
PCI Option	PCI is in option mode	Green
PCI 66 MHz	PCI is 66 MHz (host mode only)	Green
PCI 33 MHz	PCI is 33 MHz (host mode only)	Green

3.23 Mechanical Guidelines

The IXDP465 platform fits in a PCI chassis. The board height is not restricted to PCI standard. While the board can plug into a full size PCI slot, the cover does not have to fit and the adjacent slots do not have to be usable, i.e. the board can violate the board-to-board spacing restrictions of PCI.

3.24 Environmental Guidelines

The IXDP465 platform complies with the environmental conditions defined in Table 69.

Table 69. Environmental Ranges

	Temperature Range	Humidity Range	As Measured From....
Operational	0 - 50ºC (Ambient temp. external to System containing product)	0% - 80% non-condensing	Measured from the component with the most power consumption on the board (processor). Must be less than 70ºC with ambient of 50ºC. Ambient temperature must be maintained at 50ºC as measured at least 2 inches from the system under test.
Non-Operational	-20 - 70ºC	0% - 80% non-condensing	Ambient, for a 30-day duration.

3.25 Regulatory Guidelines

The IXDP465 platform complies with all regulations for sale of laboratory telecommunications equipment in the following countries/regions:

- USA
- Canada
- EU
- Asia
- Australia/New Zealand

Note: This product contains encryption logic and must meet all applicable export regulations for sale outside of the USA.

Network Processor Module Hardware Design 4

This chapter covers the following Network Processor Module (NPM) that is compatible with the IXDP465 baseboard.

- IXP465 Network Processor Module (x16 DDR memory model)

4.1 IXP465 Network Processor Module (x16 Memory Model)

4.1.1 Introduction

This section presents the target specifications for the IXP465 Network Processor Module (NPM), x16 memory model, and provides information on which devices are supported through the connectors.

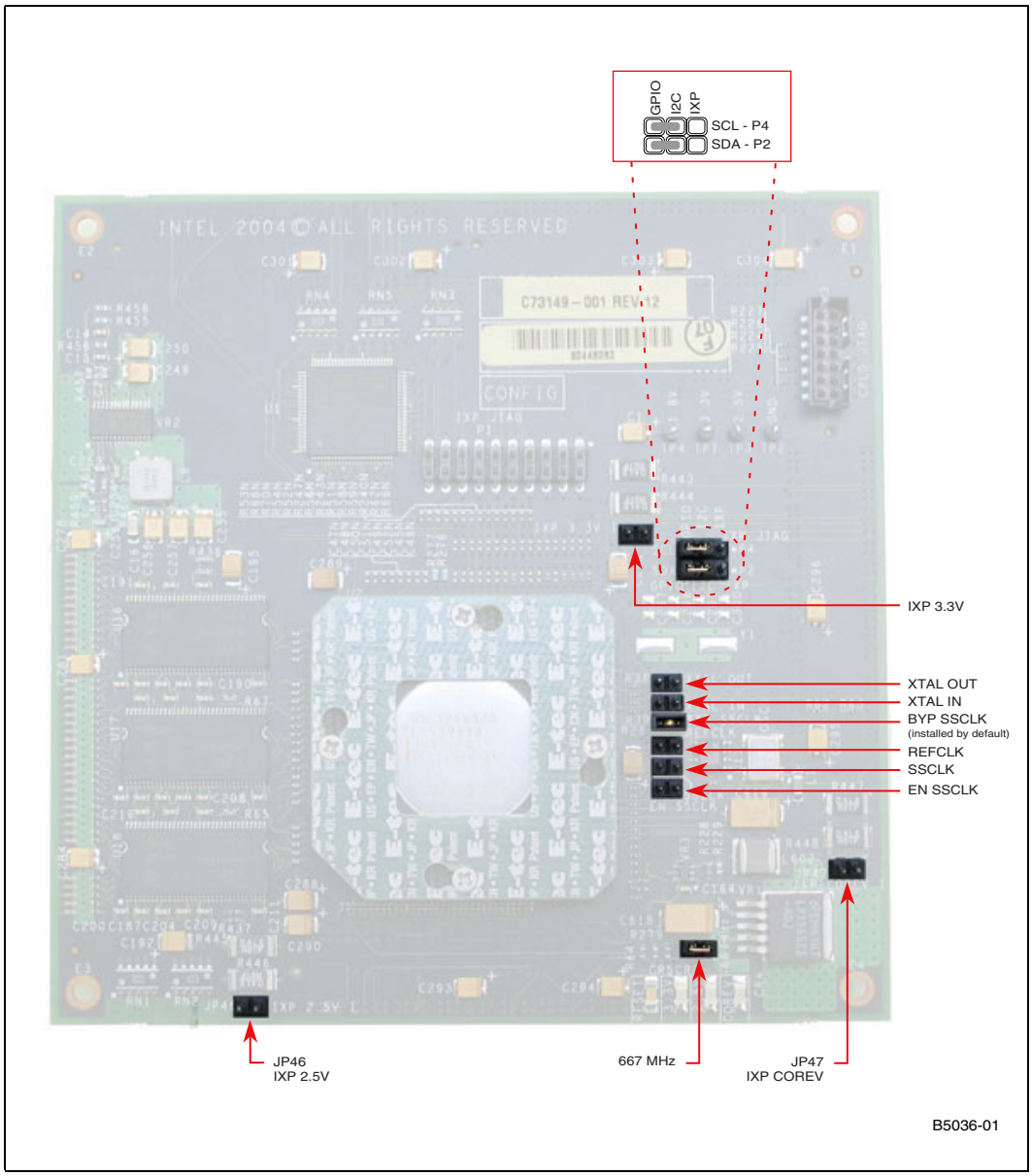
The Intel® IXP465 Network Processor is the next generation of processor in the IXP4XX family. The IXP465 network processor design has many peripheral components that must be verified. The Intel® IXDP465 Development Platform validates that these peripherals are functional. This IXP465 NPM consists of the IXP465 network processor, its associated memory subsystem (DDR in a x16 configuration) and connectors for attachment to the IXDP465 platform.

To pass FCC Class B emissions, spread spectrum clocking is used. Two different footprints are available for an external clock:

- Canned oscillator
- Spread spectrum clocking chip

The IXP465 network processor uses a set of jumpers for clock configuration. Figure 17 shows the jumper locations on the Network Processor Module. The clock is taken directly from the oscillator output when the **BYP SSCLK** jumper is installed (default setting). The clock is driven through the spread spectrum IC (as a buffer only, no frequency alterations occur) when the **REFCLK** jumper is installed. The clock is driven through the spread spectrum IC with frequency alterations when the **SSCLK** jumper is installed. Also, the spread spectrum enable (**EN SSCLK**) jumper must be installed. Since the crystal option for the IXP465 network processor is not supported, do not install the **XTAL_IN** or **XTAL_OUT** jumpers.

Figure 17. Network Processor Module Jumper Locations and Default Settings



Four 120-pin connectors meet the IXP465 network processor module signaling and power requirements. (These are the same connectors as used on the IXDP425 development platform network processor.) The connectors are low-profile, 13 mm stack height surface mount, with center ground planes. The connectors are divided into four groups of signals: NPE and peripherals, expansion bus, PCI Bus, and future needs.

The 1.3 V core voltage (1.5 V for the 667 MHz version) for the IXP465 is generated on this module.

The JTAG header on this module is for standalone debugging. A JTAG header with compatible connectors/converters for the following ICE interfaces is provided:

- Raven ICE*
- Vision ICE*

A 10 nF decoupling capacitor is placed for each V_{CC} and V_{CCP} pin in keeping with the silicon design guidelines.

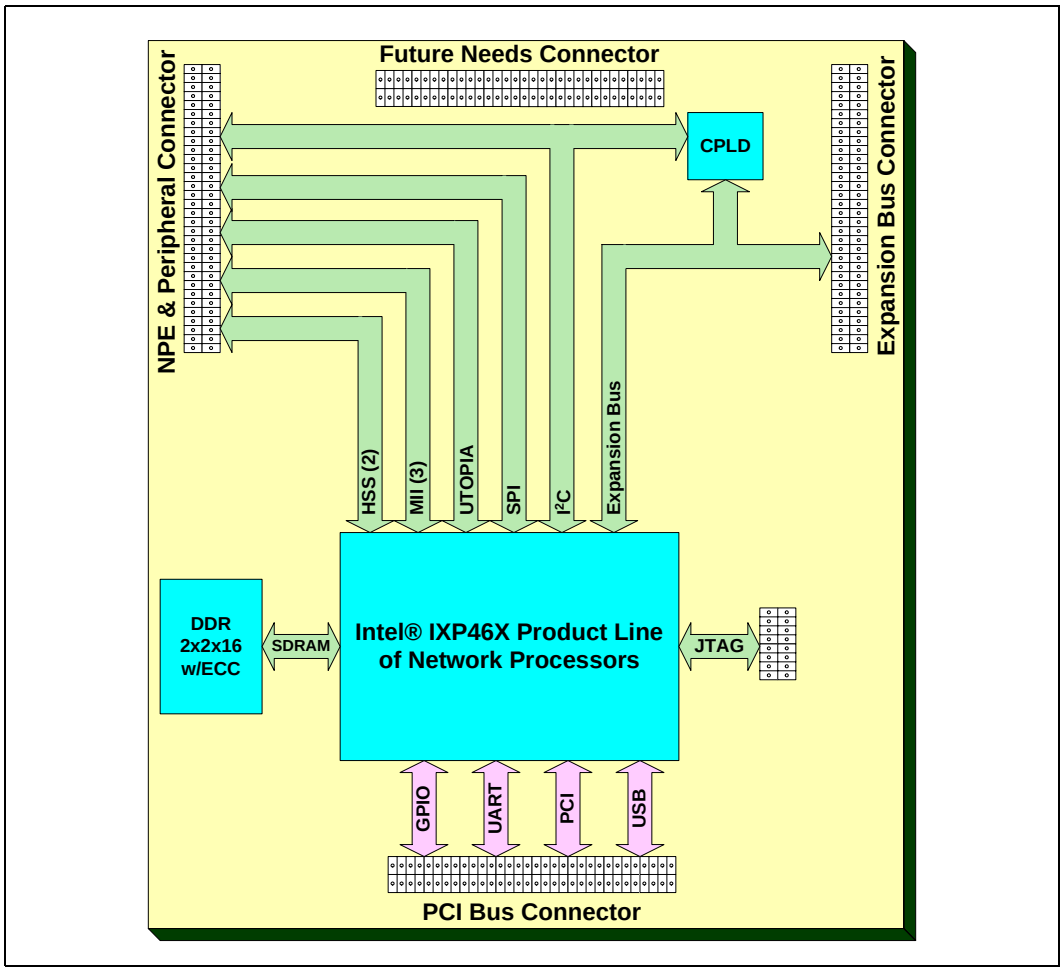
The IXP465 network processor runs at 266, 400, 533 or 667 MHz, selectable through configuration straps (with 533 MHz the default). The IXP465 supports DDR Type 1 SDRAM operating at 266 MHz for 8-bit- and 16-bit-wide devices only. The banks are accessed 32 bits at a time. The maximum configuration is two banks. Table 70 lists the supported memory configurations. The IXP465 network processor module is designed to support the full range of DDR memory from 32 Mbytes through 512 Mbytes. The module ships with 128 Mbytes and includes a user-configurable option for ECC.

Table 70. IXP465 Network Processor Module Supported Memory Configurations

Total Memory	128 Mbyte Device	256 Mbyte Device	512 Mbyte Device	1024 Mbyte Device
32 Mbytes	2 chips 8M x16			
64 Mbytes	4 chips 8M x16	2 chips 16M x16		
128 Mbytes		4 chips 16M x16	2 chips 32M x16	
256 Mbytes			4 chips 32M x16	2 chips 64M x16
512 Mbytes				4 chips 64M x16

A 10 nF decoupling capacitor is placed near each power pin. A 4.7 µF capacitor is placed for each bank.

Figure 18. IXP465 Network Processor x16 Module Logical Block Diagram

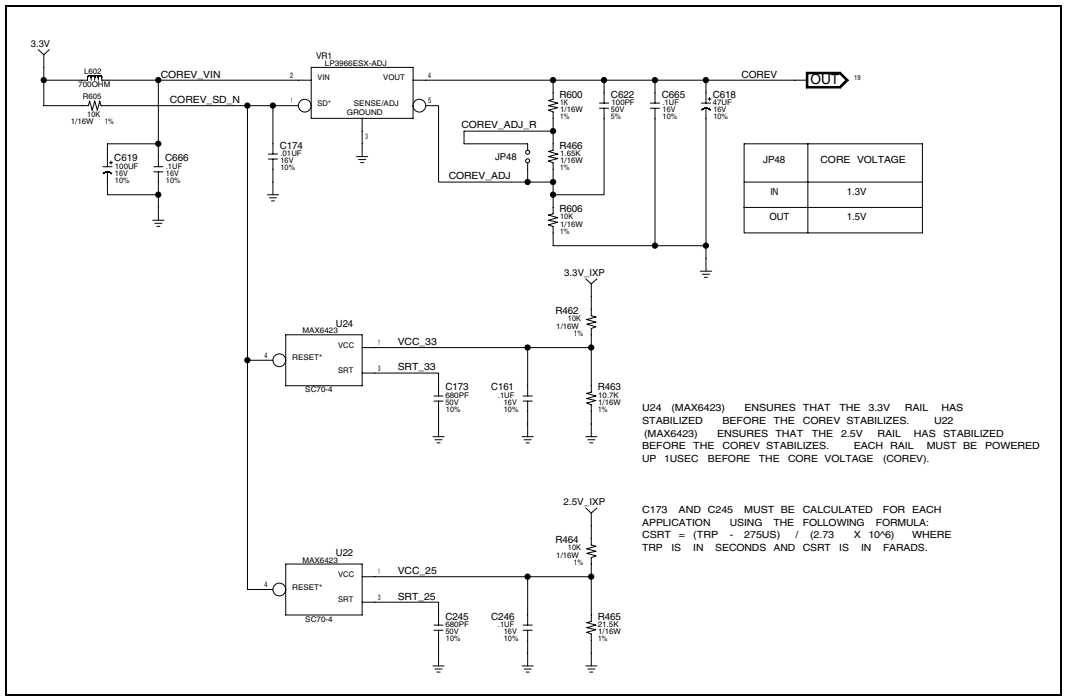


4.1.2 IXP465 Core Voltage Generation

The core voltage required for the IXP465 network processor is 1.3 V, except for the 667 MHz version, where the core voltage is 1.5 V. The maximum current generated by this circuit is 3.0 A (~2 A required). The circuit that generates the core voltage is shown inFigure 19.

Note: Figure 19 is provided for reference only. For greater detail, see the schematics files in the Intel® IXDP465 Development Platform Documentation Kit.

Figure 19. IXP465 Core Voltage Generation Logic



The output voltage is controlled by the resistor network attached to the adjust signal (**ADJ**) by the following equation:

```
Vout = (R1/R2 + 1) * 1.216 = 1.3376 V
```

From the manufacturer's data sheet, the filter capacitor on the adjust signal must be between 68 pF and 100 pf. It is recommended that the output capacitor (C618) must be at least 47 pF.

The delay circuit driving the shutdown signal must be at least 1µs after +3.3 V and +2.5 V to achieve its positive rail. Since the voltage for the IXP465 I/O has a 5% tolerance, this circuit guarantees release of **SHUTDOWN_N** no higher than 3.135 V.

The resistor divider network guarantees that the timer will not start until the +3.3 V has achieved 85% to 98% of its voltage, taking into account tolerances on the supply and VIN of the MAX6423-16. This avoids the lengthy rise time of the +3.3 V supply seen on heavily loaded PCI systems. The resistor divider network also guarantees that the timer will not start until the +2.5 V has achieved 85% to 98% of its voltage, taking into account tolerances on the supply and VIN of the MAX6423-16. This avoids the lengthy rise time of the +2.5 V supply seen on heavily loaded PCI systems.

A heat sink of at least 1/2 square inch (1 oz. unmasked copper) is necessary for proper heat dissipation.

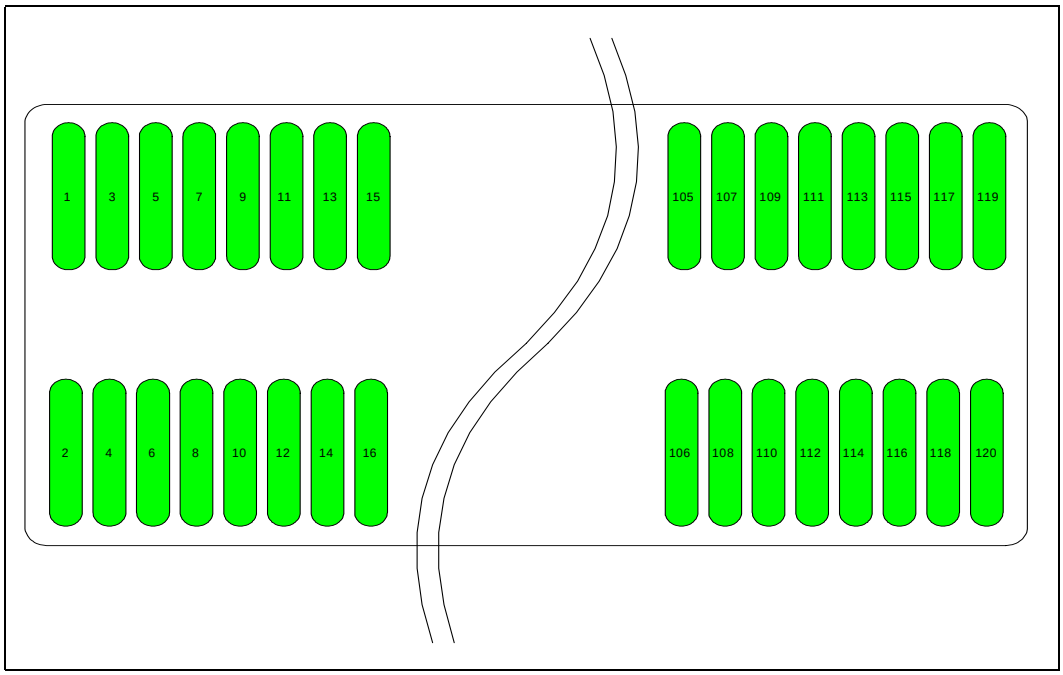
To achieve the output voltage for 667 MHz (1.5 V) the **JP48** jumper shown in Figure 17 on page 98 must be removedto series the 1.65 KΩ(R466) resistor into the regulator compensation circuit.

Note: JP48 is currently identified as 667 on the Network Processor Module. To find the location of this jumper, see Figure 17 on page 98.

4.1.3 PCI Bus Connector

The PCI connector contains the signaling from the IXP465 network processor for the PCI Bus, the USB, the two UARTS and the GPIO. The connector signal definition was chosen to allow for the best case PCI routing to the PCI option fingers on the IXDP465 platform. Figure 20 depicts the mezzanine card connector pin-out on the IXDP465 platform. The even numbered pins are nearest to the bottom of the card, near the PCI fingers on the platform, and farthest from the network processor.

Figure 20. IXDP465 Development Platform Mezzanine Card Connector Pin-out



To match the PCI bus connector with the PCI fingers on the IXDP465 platform, the PCI fingers pin definition must be analyzed. Figure 21 depicts the PCI fingers, with the fingers shown in green at the bottom of the figure being on the PCI B side (or component side), while the fingers shown in red at the top of the figure are on the PCI A side (or solder side).

Figure 21. IXDP465 Mezzanine Card Connector Pin-out

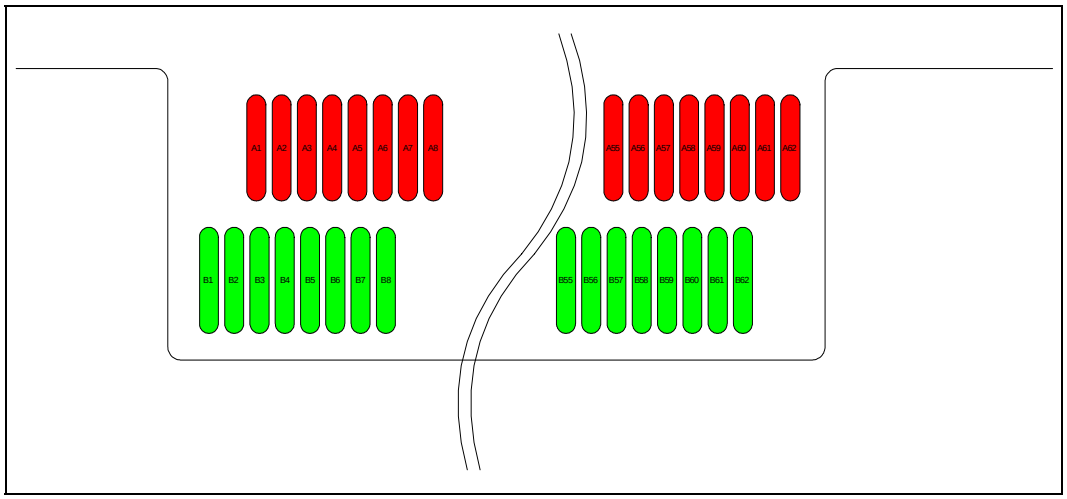


Table 71 shows the PCI Bus connector signal assignment. The signals include all IXP465 signals. There are 10 reserved signals that must be left unconnected. The USB signals connect directly to the IXP465. The 16 GPIO signals connect directly to the IXP465. The PCI signals connect directly to the IXP465, and the pin locations were chosen to allow for direct connection to the PCI fingers without crossover. The PCI finger number is shown in the table for reference.

Table 71. IXP465 Network Processor Module PCI Bus Connector Signals (Sheet 1 of 2)

Signal	Pin #	PCI Pin #	Signal	Pin #	PCI Pin #	Signal	Pin #	PCI Pin #
C_PCI_0	1	-	GND	41	-	GPIO10	81	-
C_PCI_1	2	-	PCI_ADD29	42	B21	GPIO11	82	-
USB_DPOS	3	-	PCI_ADD28	43	A22	GPIO12	83	-
USB_DNEG	4	-	GND	44	-	PCI_SERR_N	84	B42
USB_HPOS	5	-	PCI_ADD26	45	A23	PCI_PAR	85	A43
USB_HNEG	6	-	PCI_ADD27	46	B23	GND	86	-
USB_HPEN	7	-	GND	47	-	PCI_ADD15	87	A44
USB_HPWR	8	-	PCI_ADD25	48	B24	PCI_CBE_N1	88	B44
GPIO0	9	-	PCI_ADD24	49	A25	GND	89	-
GPIO1	10	-	GND	50	-	PCI_ADD14	90	B45
PCI_INTA_N	11	A6	PCI_IDSEL	51	A26	PCI_ADD13	91	A46
GND	12	-	PCI_CBE_N3	52	B26	C_PCI_2	92	-
PCI_REQ_N1	13	-	GND	53	-	PCI_ADD11	93	A47
PCI_GNT_N1	14	-	PCI_ADD23	54	B27	PCI_ADD12	94	B47
PCI_REQ_N2	15	-	PCI_ADD22	55	A28	C_PCI_3	95	-
PCI_GNT_N2	16	-	GND	56	-	PCI_ADD10	96	B48
PCI_REQ_N3	17	-	PCI_ADD20	57	A29	PCI_ADD9	97	A49
PCI_GNT_N3	18	-	PCI_ADD21	58	B29	C_PCI_4	98	-
GPIO2	19	-	GND	59	-	GPIO13	99	-

Table 71. IXP465 Network Processor Module PCI Bus Connector Signals (Sheet 2 of 2)

Signal	Pin #	PCI Pin #	Signal	Pin #	PCI Pin #	Signal	Pin #	PCI Pin #
GPIO3	20	-	PCI_ADD19	60	B30	GPIO14	100	-
TXDATA0	21	-	PCI_ADD18	61	A31	GPIO15	101	-
RXDATA0	22	-	GND	62	-	C_PCI_5	102	-
CTS_N0	23	-	PCI_ADD16	63	A32	PCI_CBE_N0	103	A52
RTS_N0	24	-	PCI_ADD17	64	B32	PCI_ADD8	104	B52
TXDATA1	25	-	GND	65	-	C_PCI_6	105	-
RXDATA1	26	-	PCI_CBE_N2	66	B33	PCI_ADD7	106	B53
CTS_N1	27	-	PCI_FRAME_N	67	A34	PCI_ADD6	107	A54
RTS_N1	28	-	+2.5 V	68	-	C_PCI_7	108	-
+12.0 V	29	-	+2.5 V	69	-	PCI_ADD4	109	A55
+12.0 V	30	-	PCI_IRDY_N	70	B35	PCI_ADD5	110	B55
PCI_RST_N	31	-	PCI_TRDY_N	71	A36	C_PCI_8	111	-
PCI_CLK	32	B16	+5.0 V	72	-	PCI_ADD3	112	B56
PCI_GNT_N0	33	A17	+5.0 V	73	-	PCI_ADD2	113	A57
GPIO4	34	-	PCI_DEVSEL_N	74	B37	C_PCI_9	114	-
GPIO5	35	-	PCI_STOP_N	75	A38	PCI_ADD0	115	A58
PCI_REQ_N0	36	B18	GND	76	-	PCI_ADD1	116	B58
GPIO6	37	-	GPIO8	77	-	+3.3 V	117	-
GPIO7	38	-	GPIO9	78	-	+3.3 V	118	-
PCI_ADD30	39	A20	GND	79	-	+3.3 V	119	-
PCI_ADD31	40	B20	PCI_PERR_N	80	B40	+3.3 V	120	-

Legend	
power signals	purple
PCI signals	green
reserved	gray
USB signals	gold
GPIO signals	maroon

4.1.4 Expansion Bus Connector

The expansion connector contains the signaling from the IXP465 network processor for the Expansion Bus. Table 72 shows the expansion bus connector signal assignment. The signals include all IXP465 signals. There are nine reserved signals. The reserved signals must be left unconnected. The expansion bus signals connect directly to the IXP465.

Table 72. IXP465 Network Processor Module Expansion Bus Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
C_EXP_0	1	GND	41	EX_DATA0	81
C_EXP_1	2	EX_CLK	42	EX_DATA1	82
C_EXP_2	3	EX_ALE	43	EX_DATA2	83
C_EXP_3	4	GND	44	EX_DATA3	84
C_EXP_4	5	EX_WAIT_N	45	EX_DATA4	85
C_EXP_5	6	EX_SLAVE_CS_N	46	EX_DATA5	86
C_EXP_6	7	GND	47	EX_DATA6	87
C_EXP_7	8	EX_IOWAIT_N	48	EX_DATA7	88
C_EXP_8	9	EX_BURST	49	EX_DATA8	89
EX_ADDR0	10	GND	50	EX_DATA9	90
EX_ADDR1	11	EX_RDY_N0	51	EX_DATA10	91
EX_ADDR2	12	EX_RDY_N1	52	EX_DATA11	92
EX_ADDR3	13	GND	53	EX_DATA12	93
EX_ADDR4	14	EX_RDY_N2	54	EX_DATA13	94
EX_ADDR5	15	EX_RDY_N3	55	EX_DATA14	95
EX_ADDR6	16	GND	56	EX_DATA15	96
EX_ADDR7	17	EX_PAR0	57	EX_DATA16	97
EX_ADDR8	18	EX_PAR1	58	EX_DATA17	98
EX_ADDR9	19	GND	59	EX_DATA18	99
EX_ADDR10	20	EX_PAR2	60	EX_DATA19	100
EX_ADDR11	21	EX_PAR3	61	EX_DATA20	101
EX_ADDR12	22	GND	62	EX_DATA21	102
EX_ADDR13	23	EX_REQ_N1	63	EX_DATA22	103
EX_ADDR14	24	EX_REQ_N2	64	EX_DATA23	104
EX_ADDR15	25	GND	65	EX_DATA24	105
EX_ADDR16	26	EX_REQ_N3	66	EX_DATA25	106
EX_ADDR17	27	EX_REQ_GNT_N	67	EX_DATA26	107
EX_ADDR18	28	+2.5 V	68	EX_DATA27	108
EX_ADDR19	29	+2.5 V	69	EX_DATA28	109
EX_ADDR20	30	EX_GNT_N1	70	EX_DATA29	110
EX_ADDR21	31	EX_GNT_N2	71	EX_DATA30	111
EX_ADDR22	32	+5.0 V	72	EX_DATA31	112
EX_ADDR23	33	+5.0 V	73	EX_BE_N0	113
EX_ADDR24	34	EX_GNT_N3	74	EX_BE_N1	114
EX_WR_N	35	EX_GNT_REQ_N	75	EX_BE_N2	115
EX_RD_N	36	GND	76	EX_BE_N3	116
EX_CS_N0	37	EX_CS_N4	77	+3.3 V	117

Table 72. IXP465 Network Processor Module Expansion Bus Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_CS_N1	38	EX_CS_N5	78	+3.3 V	118
EX_CS_N2	39	EX_CS_N6	79	+3.3 V	119
EX_CS_N3	40	EX_CS_N7	80	+3.3 V	120

Legend	
power signals	purple
expansion bus signals	green
reserved	gray

4.1.5 NPE and Peripheral Connector

The NPE and Peripheral connector contains the signaling from the IXP465 for the HSS, MII, UTOPIA, SPI and I^2C interfaces.

Table 73. IXP465 Network Processor Module NPE and Peripheral Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
C_NPE_0	1	GND	41	ETHB_TXEN	81
C_NPE_1	2	ETHC_TXCLK	42	ETHB_RXDATA0	82
C_NPE_2	3	ETHC_RXCLK	43	ETHB_RXDATA1	83
C_NPE_3	4	GND	44	ETHB_RXDATA2	84
C_NPE_4	5	UTP_OP_CLK	45	ETHB_RXDATA3	85
C_NPE_5	6	UTP_IP_CLK	46	ETHB_RXDV	86
C_NPE_6	7	GND	47	ETHB_COL	87
C_NPE_7	8	UTP_OP_DATA0	48	ETHB_CRS	88
C_NPE_8	9	UTP_OP_DATA1	49	UTP_OP_FCO	89
HSS_TX_FRAME0	10	GND	50	UTP_OP_SOC	90
HSS_TX_DATA0	11	UTP_OP_DATA2	51	UTP_OP_FCI	91
HSS_TX_CLK0	12	UTP_OP_DATA3	52	UTP_IP_FCO	92
HSS_RX_FRAME0	13	GND	53	UTP_IP_SOC	93
HSS_RX_DATA0	14	UTP_OP_DATA4	54	UTP_IP_FCI	94
HSS_RX_CLK0	15	UTP_OP_DATA5	55	UTP_IP_ADDR0	95
HSS_TX_FRAME1	16	GND	56	UTP_IP_ADDR1	96
HSS_TX_DATA1	17	UTP_OP_DATA6	57	UTP_IP_ADDR2	97
HSS_TX_CLK1	18	UTP_OP_DATA7	58	UTP_IP_ADDR3	98
HSS_RX_FRAME1	19	GND	59	UTP_P_ADDR4	99
HSS_RX_DATA1	20	UTP_IP_DATA0	60	I2C_SDA	100
HSS_RX_CLK1	21	UTP_IP_DATA1	61	I2C_SCL	101

Table 73. IXP465 Network Processor Module NPE and Peripheral Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
UTP_OP_ADDR0	22	GND	62	SSP_CLK	102
UTP_OP_ADDR1	23	UTP_IP_DATA2	63	SSP_FRM	103
UTP_OP_ADDR2	24	UTP_IP_DATA3	64	SSP_TXD	104
UTP_OP_ADDR3	25	GND	65	SSP_RXD	105
UTP_OP_ADDR4	26	UTP_IP_DATA4	66	SSP_EXTCLK	106
ETH_MDC	27	UTP_IP_DATA5	67	C_NPE_9	107
ETH_MDIO	28	+2.5 V	68	C_NPE_10	108
ETHC_TXEN	29	+2.5 V	69	C_NPE_11	109
ETHC_RXDATA0	30	UTP_IP_DATA6	70	C_NPE_12	110
ETHC_RXDATA1	31	UTP_IP_DATA7	71	C_NPE_13	111
ETHC_RXDATA2	32	+5.0 V	72	C_NPE_14	112
ETHC_RXDATA3	33	+5.0 V	73	C_NPE_15	113
ETHC_RXDV	34	ETHB_TXCLK	74	C_NPE_16	114
ETHC_COL	35	ETHB_RXCLK	75	C_NPE_17	115
ETHC_CRS	36	GND	76	C_NPE_18	116
ETHC_TXDATA0	37	ETHB_TXDATA0	77	+3.3 V	117
ETHC_TXDATA1	38	ETHB_TXDATA1	78	+3.3 V	118
ETHC_TXDATA2	39	ETHB_TXDATA2	79	+3.3 V	119
ETHC_TXDATA3	40	ETHB_TXDATA3	80	+3.3 V	120

Legend	
power signals	purple
MII signals	green
HSS signals	red
I2C signals	black
SPI signals	blue
UTOPIA signals	gold
reserved	gray

4.1.6 Future Needs Connector

The Future Needs connector contains the power signaling and expansion bus arbitration signals. The remaining pins are reserved for future needs, and are not routed on this module (they will be routed on the IXDP465 platform baseboard to mezzanine card connectors).

Table 74. IXP465 Network Processor Module Future Needs Connector Pin Definitions (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_REQ_N3	1	GND	41	C_FN_66	81
EX_GNT_N3	2	C_FN_40	42	C_FN_67	82
EX_REQ_N2	3	C_FN_41	43	C_FN_68	83
EX_GNT_N2	4	GND	44	C_FN_69	84
EX_REQ_N1	5	C_FN_42	45	C_FN_70	85
EX_GNT_N1	6	C_FN_43	46	C_FN_71	86
EX_REQ_GNT_N	7	GND	47	C_FN_72	87
EX_GNT_REQ_N	8	C_FN_44	48	C_FN_73	88
EX_WAIT_N	9	C_FN_45	49	C_FN_74	89
EX_SLAVE_CS_N	10	GND	50	C_FN_75	90
C_FN_10	11	C_FN_46	51	C_FN_76	91
C_FN_11	12	C_FN_47	52	C_FN_77	92
C_FN_12	13	GND	53	C_FN_78	93
C_FN_13	14	C_FN_48	54	C_FN_79	94
C_FN_14	15	C_FN_49	55	C_FN_80	95
C_FN_15	16	GND	56	C_FN_81	96
C_FN_16	17	C_FN_50	57	C_FN_82	97
C_FN_17	18	C_FN_51	58	C_FN_83	98
C_FN_18	19	GND	59	C_FN_84	99
C_FN_19	20	C_FN_52	60	C_FN_85	100
C_FN_20	21	C_FN_53	61	C_FN_86	101
C_FN_21	22	GND	62	C_FN_87	102
C_FN_22	23	C_FN_54	63	C_FN_88	103
C_FN_23	24	C_FN_55	64	C_FN_89	104
C_FN_24	25	GND	65	C_FN_90	105
C_FN_25	26	C_FN_56	66	C_FN_91	106
C_FN_26	27	C_FN_57	67	C_FN_92	107
C_FN_27	28	+2.5 V	68	C_FN_93	108
C_FN_28	29	+2.5 V	69	C_FN_94	109
C_FN_29	30	C_FN_58	70	C_FN_95	110
C_FN_30	31	C_FN_59	71	C_FN_96	111
C_FN_31	32	+5.0 V	72	C_FN_97	112
C_FN_32	33	+5.0 V	73	C_FN_98	113
C_FN_33	34	C_FN_60	74	C_FN_99	114
C_FN_34	35	C_FN_61	75	C_FN_100	115
C_FN_35	36	C_FN_	76	SYS_RST_N	116

Table 74. IXP465 Network Processor Module Future Needs Connector Pin Definitions (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
C_FN_36	37	C_FN_62	77	+3.3 V	117
C_FN_37	38	C_FN_63	78	+3.3 V	118
C_FN_38	39	C_FN_64	79	+3.3 V	119
C_FN_39	40	C_FN_65	80	+3.3 V	120

Legend	
power signals	purple
expansion bus signals	green
reserved	black

Mezzanine Card Hardware Design 5

This chapter covers the following mezzanine cards that are used with the IXDP465 baseboard:

5.1 IXPDSM465 ADSL UTOPIA Level 2 Mezzanine Card

5.1.1 Introduction

The IXPDSM465 ADSL UTOPIA level 2 mezzanine card for the IXDP465 baseboard uses the Alcatel MTK-20150 chipset, which consists of the Alcatel MTC-20156 and Alcatel MTC-20154. The MTC-20156 is the DMT modem, ATM framer, and controller chip of the chipset. The MTC-20154 is the supporting analog front end. The 2x60 pin J3 connector on the IXPDSM465 ADSL card plugs into the 2x60 pin UTOPIA level 2 connector on the IXDP465 baseboard. See Section 3.5, “UTOPIA Connector” for a description of this UTOPIA connector on the baseboard. Figure 22 shows connectors on the card and Figure 23 shows the JTAG header and jumper locations.

The IXPDSM465 ADSL mezzanine card design supports multiple channels through the single channel Alcatel MTK-20150 chipset using a stackable design.

+12 V, +5 V, +3.3 V and +2.5 V digital voltage rails are provided from the IXDP465 baseboard to the UTOPIA level 2 connector. Other voltages, both digital and analog, required for the card are derived from these voltages on the IXPDSM465 ADSL card. The –12 V voltage rail is derived from the +3.3 V voltage rail on the card. JP4, JP5, JP6 headers provide access to the GND plane.

The majority of the signals needed to support the DSL card are Expansion Bus and UTOPIA level 2 data interface signals. The Alcatel DMT on the ADSL card receives its **UTP_RX_CLK** and **UTP_TX_CLK** through the 33.33 MHz oscillator already implemented on the IXDP465 baseboard. The same oscillator on the baseboard provides **UTP_OP_CLK** and **UTP_IP_CLK** signals to the IXP465 network processor.

Figure 22. ADSL Card Block Diagram

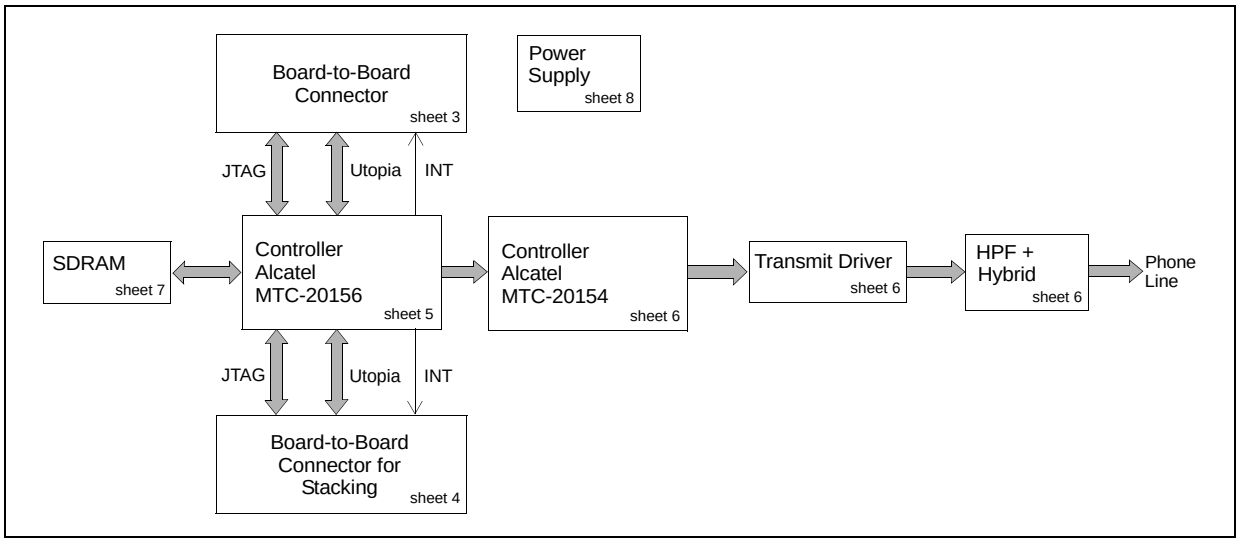
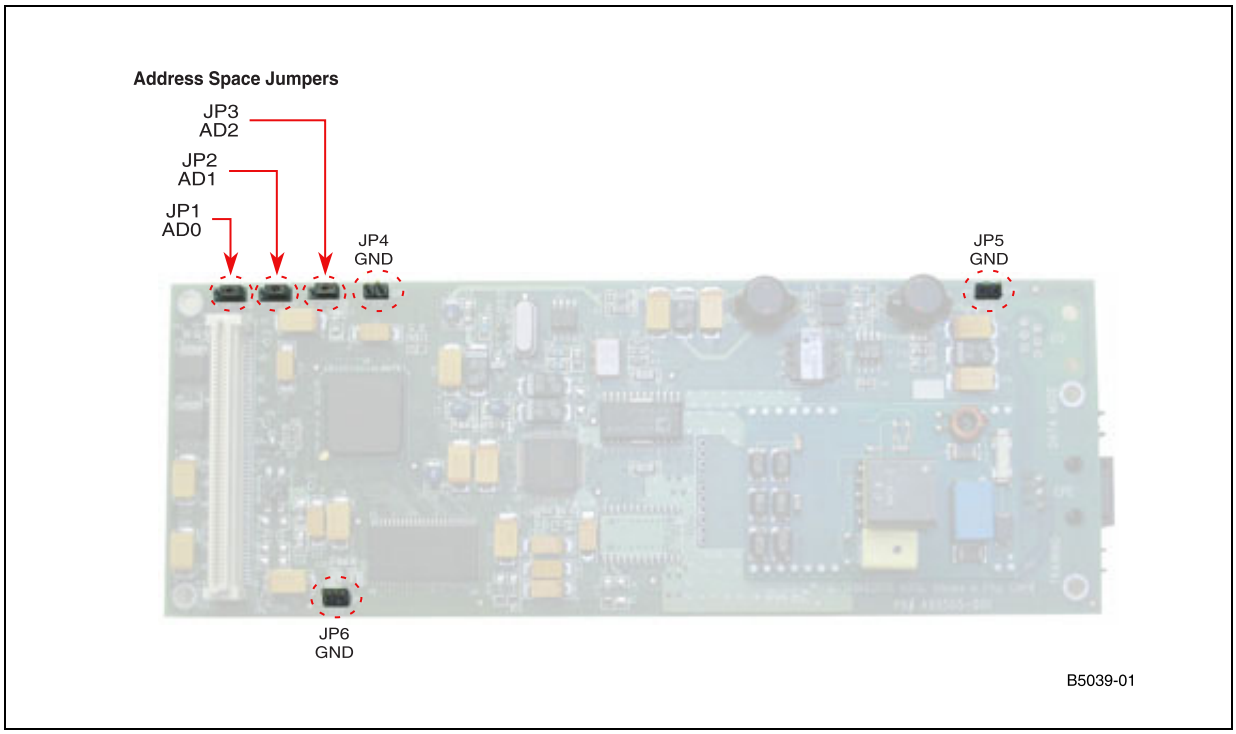


Figure 23. ADSL Card Component Placement

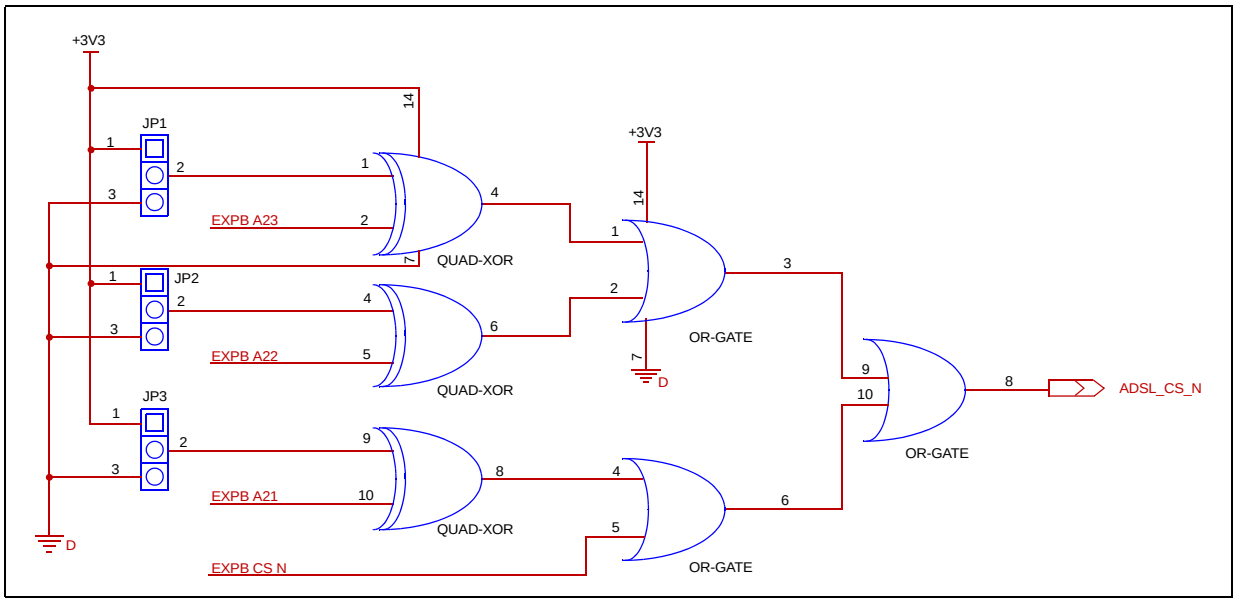


To have multi-channel PHY support, multiple IXPDSM465 ADSL cards are stacked on top of each other through the board-to-board stacking connector.

Each card has a plug connector on the bottom side and a receptacle connector on the top side to allow them to stack as shown in Figure 3 on page 21.

Each ADSL card has its own address space and three 3-pin jumpers that allow a user-defined address space for that particular card (JP3, JP2, JP1). A single expansion bus chip select along with the expansion bus addresses defined on each card allows individual communication to each device. Figure 24 shows the ADSL Stacking Logic. The top three expansion bus address lines are compared to the address set on the jumpers. If the address matches and an expansion bus chip select has been asserted, then the expansion bus chip select drives that particular card. The interrupt on each card is open-drain to allow sharing of the interrupt sent to the IXP465 network processor.

Figure 24. ADSL Stacking Logic



5.1.2 ADSL Card Signals

The IXPDSM465 ADSL mezzanine card plugs into the UTOPIA level 2 connector on the IXDP465 baseboard using a 2x60 pin connector on the ADSL card. This connector is compatible with the UTOPIA level 2 connector on the baseboard. The ADSL card connector has on-board signals used by the devices (MTC-20156 DMT, MTC-20154 AFE, transmit driver, LEDs) on the ADSL card that are routed to it. These signals include the following:

- Power/ground
- UTOPIA signals
- Other connector signals
- JTAG signals
- Expansion bus signals

The signals that exist on the ADSL UTOPIA level 2 mezzanine card are listed in Table 75. The Legend describing the color-codes for the signals follows the table.

Table 75. ADSL Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
12.0 V	1	GND	41	UTP_IP_FCI	81
12.0 V	2	GND	42	UTP_OP_DATA0	82
GND	3	EX_ALE	43	GND	83

Table 75. ADSL Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	4	3.3 V	44	UTP_OP_DATA1	84
DSL_INT_N	5	-	45	UTP_OP_DATA7	85
EX_ADDR0	6	3.3 V	46	UTP_OP_DATA3	86
GND	7	-	47	UTP_OP_DATA4	87
EX_ADDR2	8	3.3 V	48	UTP_OP_DATA5	88
EX_ADDR1	9	GND	49	UTP_OP_DATA6	89
GND	10	GND	50	GND	90
EX_ADDR3	11	3.3 V	51	GND	91
EX_ADDR4	12	3.3 V	52	UTP_OP_FCI	92
GND	13	-	53	UTP_IP_DATA7	93
EX_ADDR6	14	-	54	UTP_OP_SOC	94
EX_ADDR5	15	2.5 V	55	UTP_IP_DATA3	95
EX_ADDR8	16	2.5 V	56	GND	96
EX_ADDR7	17	GND	57	UTP_IP_DATA5	97
GND	18	GND	58	UTP_IP_DATA4	98
EX_ADDR9	19	EX_ADDR21	59	UTP_IP_SOC	99
EX_CLK_ADSL	20	EX_ADDR22	60	UTP_IP_DATA6	100
GND	21	GND	61	UTP_IP_FCO	101
GND	22	GND	62	UTP_GPIO3	102
EX_DATA0	23	3.3 V	63	GND	103
EX_DATA2	24	EX_IOWAIT_N	64	GND	104
EX_DATA1	25	3.3 V	65	UTP_IP_ADDR4	105
EX_DATA4	26	GND	66	UTP_OP_ADDR4	106
UTP_GPIO0	27	GND	67	UTP_IP_ADDR3	107
UTP_GPIO1	28	EX_ADDR23	68	UTP_OP_ADDR3	108
EX_DATA3	29	UTP_IP_CLK	69	GND	109
EX_DATA6	30	GND	70	UTP_OP_ADDR2	110
EX_DATA5	31	GND	71	UTP_IP_ADDR2	111
EX_DATA7	32	UTP_OP_CLK	72	GND	112
GND	33	UTP_IP_DATA1	73	UTP_IP_ADDR1	113
GND	34	GND	74	UTP_OP_ADDR1	114
EX_WR_N	35	-	75	UTP_IP_ADDR0	115
EX_RD_N	36	UTP_OP_DATA2	76	UTP_OP_ADDR0	116
UTP_GPIO2	37	UTP_IP_DATA0	77	UTP_GPIO4	117
GASP_INT_N	38	UTP_OP_FCO	78	UTP_GPIO5	118
RST_N	39	UTP_IP_DATA2	79	5.0 V	119
EX_CS_N	40	GND	80	5.0 V	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
UTOPIA signals	red
Other signals	black
not used (JTAG signals)	gray

5.2 IXPETM465 Ethernet Mezzanine Card

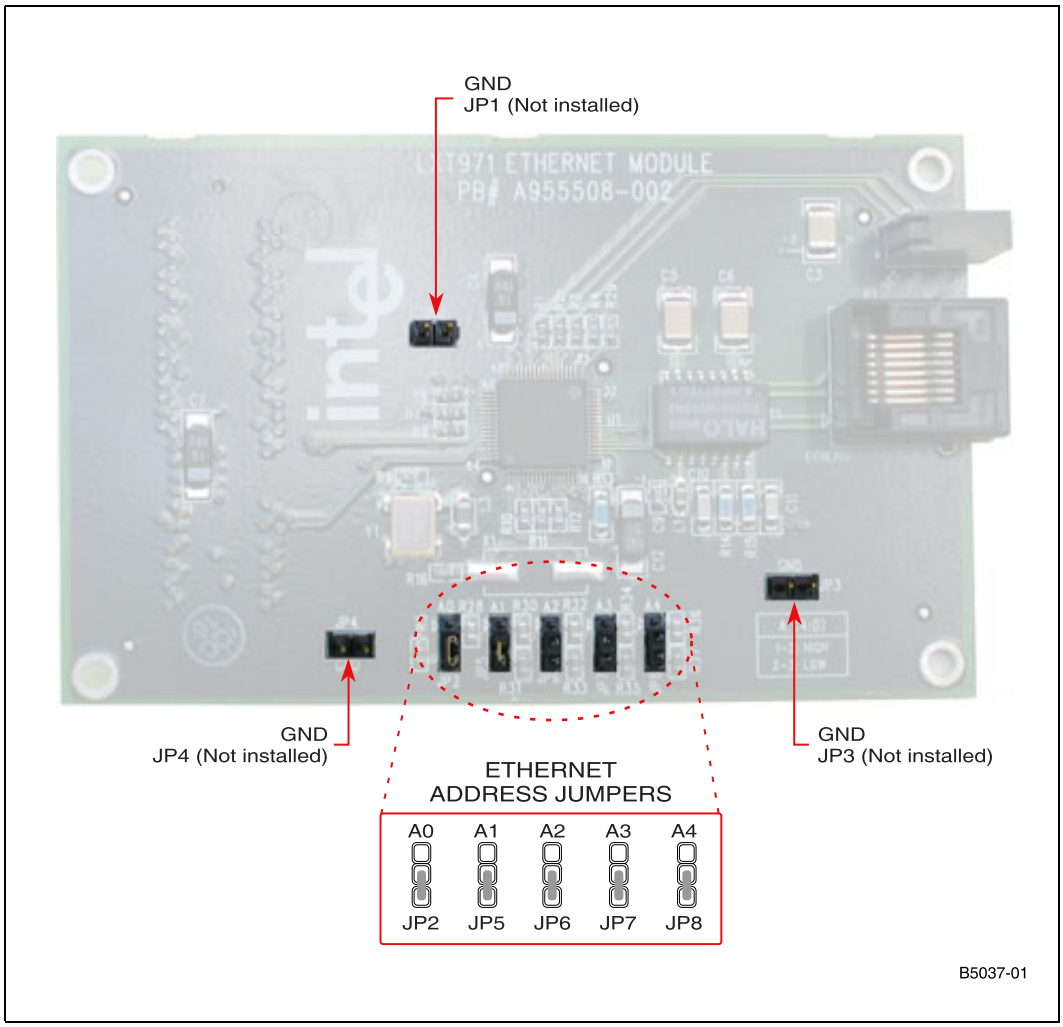
5.2.1 Introduction

The IXPETM465 Ethernet mezzanine card plugs into one of the three MII connectors on the IXDP465 baseboard through the 2x60 pin J1 connector: **MII-0 NPE B**, **MII-1 NPE C**, or **MII-2 NPE A**. See Section 3.9 for the IXDP465 baseboard connector description. The MII Ethernet PHY mezzanine card uses the LXT971A PHY, a dual-speed, full-duplex 10/100 Fast Ethernet transceiver. It provides a Media Independent Interface (MII) for connecting to one of the three 10/100 Media Access Controllers (MACs) within the IXP465 network processor. Figure 26 shows the connectors on the Ethernet mezzanine card.

The *Intel®LXT971A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet* contains more information about the LXT971A.

Figure 25 identifies eight jumper locations (JP1-JP8) on the Ethernet PHY mezzanine card. The five address jumpers (JP2, JP5, JP6, JP7, JP8) on the card define this Ethernet address, which must be defaulted to Address 0 by setting all jumpers to shunt pin 2 and pin 3. The remaining three ground jumpers (JP1, JP3, JP4) are not installed.

Figure 25. Ethernet Card Jumper Locations and Default Settings



The IXDP465 platform can accommodate up to three IXPETM465 Ethernet mezzanine cards. Each MII Ethernet PHY mezzanine card maps its own address to the IXP465 network processor's PHY map. Table 76 shows the PHY mapping for the jumpers.

Table 76. Jumper/Address Bit Mapping

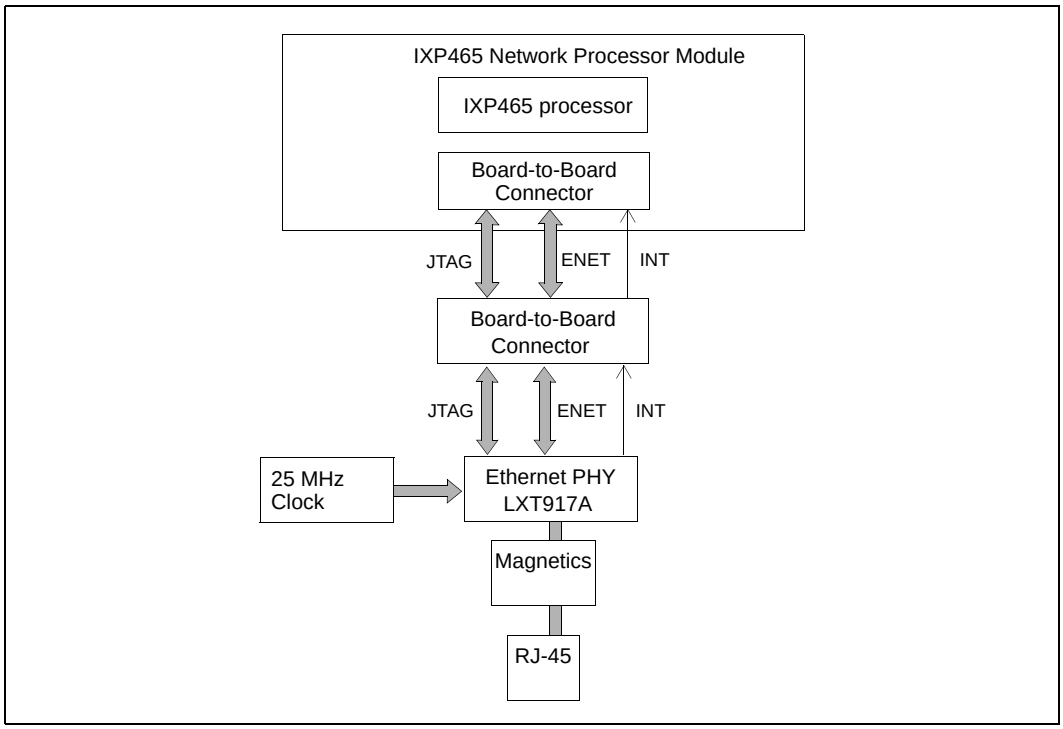
Jumper	JP8	JP7	JP6	JP5	JP2	PHY Address
Address Bit	A4	A3	A2	A1	A0	
	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	00 (0)
	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	01 (1)
	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3)	02 (2)
	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	03 (3)
	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3	Low (pins 2-3)	04 (4)
	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3	High (pins 1-2)	05 (5)
	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	06 (6)
	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	07 (7)
	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	08 (8)
	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	09 (9)
	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3)	A (10)
	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	B (11)
	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	C (12)
	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	D (13)
	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	E (14)
	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	F (15)
	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	10 (16)
	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	11 (17)
	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3)	12 (18)
	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	13 (19)
	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	14 (20)
	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	15 (21)
	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	16 (22)
	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	17 (23)
	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	Low (pins 2-3)	18 (24)
	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	High (pins 1-2)	19 (25)
	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	Low (pins 2-3	1A (26)
	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	High (pins 1-2)	1B (27)
	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	Low (pins 2-3)	1C (28)
	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	High (pins 1-2)	1D (29)
	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	Low (pins 2-3)	1E (30)
	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	High (pins 1-2)	1F (31)

The LXT971A clock (**REFCLK-X1**) on each MII Ethernet card is clocked using a 25 MHz oscillator on the IXDP465 baseboard. A 25 MHz crystal can be used if desired but this is not populated on the IXPETM465 card. The LXT971A **TX_CLK** and **RX_CLK** supply transmit and receive clocks to the IXP465 network processor through the connector (**ENET_TX_CLK**, **ENET_RX_CLK**).

There are three LEDs (DL1) located at the sides of the MII Ethernet PHY mezzanine card. They indicate 10/100 mode, link, and activity status.

+3V3_ENET analog power is generated on the MII Ethernet PHY mezzanine card from the +3.3 V power delivered to it by the IXDP465 baseboard. This is needed for the LXT971A PHY and the transformer.

Figure 26. MII Ethernet Card Connectors



5.2.2 Ethernet Card Signals

The IXPETM465 Ethernet mezzanine card plugs into a 2x60 pin connector (J1) on the mezzanine card that is compatible with the **NPE-B** (P14), **NPE-C** (P16), or **NPE-A** (P18) connector on the IXDP465 baseboard. The mezzanine card connector carries on-board signals used by devices (LXT971A, oscillator, LEDs) on the MII Ethernet card. These signals include the following:

- Power/ground
- MII signals
- JTAG signals
- Other connector signals

Note: Expansion bus, GPIO, and expansion bus clock signals on NPE connectors on the IXDP465 baseboard are not used on the IXPETM465 card, and therefore are not routed to the IXPETM465 connector.

The signals used on the IXPETM465 Ethernet mezzanine card are listed in Table 77. The Legend describing the color-codes for the signals follows the table.

Table 77. Ethernet PHY Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
-	1	EX_ADDR11	41	5.0 V	81
-	2	EX_ADDR10	42	3.3 V	82
-	3	EX_ADDR13	43	MII0_GPIO2	83
-	4	EX_ADDR12	44	MII0_GPIO3	84
EX_DATA1	5	EX_ADDR15	45	GND	85
EX_DATA0	6	EX_ADDR14	46	GND	86
EX_DATA3	7	GND	47	-	87
EX_DATA2	8	GND	48	MII0_GPIO4	88
MII0_GPIO0	9	EX_ADDR17	49	-	89
MII0_GPIO1	10	EX_ADDR16	50	RST_N	90
EX_DATA5	11	EX_ADDR19	51	-	91
EX_DATA4	12	EX_ADDR18	52	ETHB_TXEN	92
EX_DATA7	13	EX_ADDR21	53	-	93
EX_DATA6	14	EX_ADDR20	54	ETHB_RXDV	94
GND	15	EX_ADDR23	55	GND	95
GND	16	EX_ADDR22	56	ETHB_RXCLK	96
EX_DATA9	17	GND	57	ETHB_RXDATA3	97
EX_DATA8	18	GND	58	GND	98
EX_DATA11	19	EX_CLK_MII0	59	ETHB_RXDATA2	99
EX_DATA10	20	EX_RD_N	60	ETHB_TXCLK	100
-	21	GND	61	ETHB_RXDATA1	101
-	22	EX_WR_N	62	ETHB_COL	102
EX_DATA13	23	EX_ALE	63	ETHB_RXDATA0	103
EX_DATA12	24	EX_RDY_N0	64	ETHB_TXDATA3	104
EX_DATA15	25	EX_IOWAIT_N	65	GND	105
EX_DATA14	26	ETHB_INT_N	66	ETHB_TXDATA2	106
GND	27	EX_CS_N4	67	ETHB_TXDATA1	107
GND	28	3.3 V	68	GND	108
EX_ADDR1	29	-	69	ETHB_TXDATA0	109
EX_ADDR0	30	3.3 V	70	ETH_MDC	110
EX_ADDR3	31	5.0 V	71	ETHB_CRS	111
EX_ADDR2	32	3.3 V	72	ETH_MDIO	112
EX_ADDR5	33	5.0 V	73	12 V	113
EX_ADDR4	34	3.3 V	74	2.5 V	114
EX_ADDR7	35	5.0 V	75	12 V	115

Table 77. Ethernet PHY Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_ADDR6	36	3.3 V	76	2.5 V	116
GND	37	5.0 V	77	12 V	117
GND	38	3.3 V	78	2.5 V	118
EX_ADDR9	39	5.0 V	79	12 V	119
EX_ADDR8	40	3.3 V	80	2.5 V	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
GPIO signals	maroon
MII signals (connected to NPE-B)	black
MII signals (common)	red
not used (JTAG signals)	gray
interrupt signal	gold
RST_N	lavender

5.3 IXPVM465 Analog Voice Mezzanine Card

5.3.1 Introduction

The IXPVM465 Analog Voice mezzanine card (4x1) provides four ports of FXS (phone) and one port of FXO (central office) connectivity. When power is not applied to the IXDP465 baseboard, relays must automatically switch control from the baseboard and connect the four FXS port connectors directly to the FXO port connector (isolating it from the IXDP465 baseboard FXS and FXO circuitry). When power is applied, the relays are switched under software control.

This design is compatible with the IXDP425 development platform. The HSS Analog Voice 4x1 mezzanine card plugs into the IXDP465 baseboard through the standard 120-pin connector also used by the IXDP425 development platform. The pin-out is the same as the HSS connectors on the IXDP425, with the second (alternate) HSS port being routed to the IXDP425 connector's unused pins, allowing the device to be stackable up to eight cards high. The stacking connector is physically identical as is the signaling with the exception of routing the alternate HSS port up to the next card.

A Silicon Laboratories* Si3210 circuit is used for the FXS solution and a Silicon Laboratories* Si3050 part is used for the FXO solution. A standard four-circuit RJ11 gang jack is used for the FXS connectors and a single RJ11 jack is used for the FXO connector.

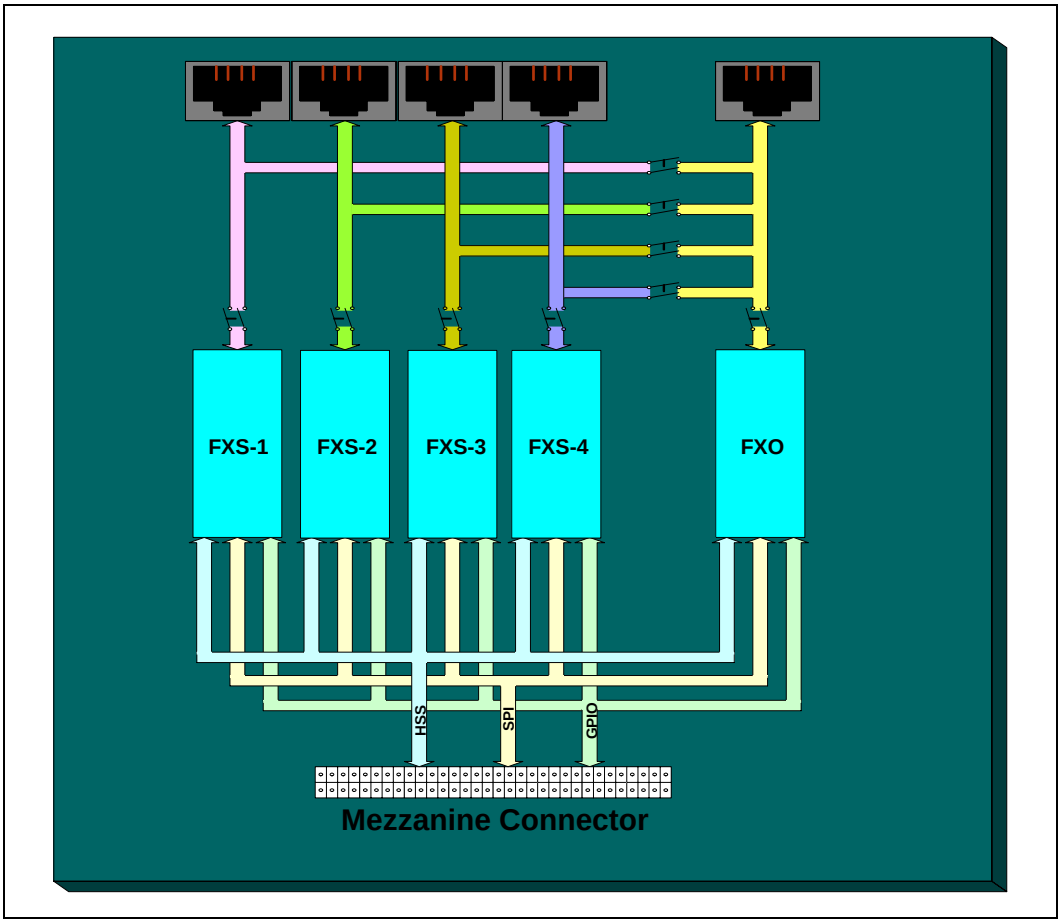
The IXDP465 platform achieves control and status of:

- the FXS and FXO ports via the SPI interface (GPIO for the IXDP425 development platform)
- the voice interface via the HSS interface

GPIO is used for hook state control, ring indication, and interrupts.

Figure 27 contains the block diagram for this mezzanine card.

Figure 27. Analog Voice Card Logical Block Diagram



5.3.2 Analog Voice Card Connector Interfaces

5.3.2.1 IXDP465 Interface Standard Connector

The IXDP465 interface standard connector contains the expansion bus interface, GPIO, HSS interface and power signals. This connector is pin-for-pin compatible with the IXDP425 HSS interface connectors. All signals necessary to communicate with the analog voice ports are available on this connector. Table 78 lists the IXDP465 interface standard connector signal definitions. The Legend describing the color-codes for the signals follows the table.

Table 78. IXDP465 Interface Standard Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
-	1	EX_ADDR11	41	5.0 V	81
-	2	EX_ADDR10	42	3.3 V	82
-	3	EX_ADDR13	43	GPIO2	83
-	4	EX_ADDR12	44	GPIO3	84
EX_DATA1	5	EX_ADDR15	45	GND	85
EX_DATA0	6	EX_ADDR14	46	GND	86
EX_DATA3	7	GND	47	-	87
EX_DATA2	8	GND	48	GPIO4	88
GPIO0	9	EX_ADDR17	49	-	89
GPIO1	10	EX_ADDR16	50	RST_N	90
EX_DATA5	11	EX_ADDR19	51	-	91
EX_DATA4	12	EX_ADDR18	52	HSS_TXFRAME1	92
EX_DATA7	13	EX_ADDR21	53	-	93
EX_DATA6	14	EX_ADDR20	54	HSS_TXCLK1	94
GND	15	EX_ADDR23	55	GND	95
GND	16	EX_ADDR22	56	HSS_TXDATA1	96
EX_DATA9	17	GND	57	HSS_TXDATA0	97
EX_DATA8	18	GND	58	GND	98
EX_DATA11	19	EX_CLK	59	HSS_TXFRAME0	99
EX_DATA10	20	EX_RD_N	60	HSS_RXDATA0	100
-	21	GND	61	-	101
-	22	EX_WR_N	62	HSS_RXFRAME0	102
EX_DATA13	23	EX_ALE	63	HSS_TXCLK0	103
EX_DATA12	24	EX_RDY_N	64	-	104
EX_DATA15	25	EX_IOWAIT_N	65	GND	105
EX_DATA14	26	INT_OUT_N	66	HSS_RXCLK0	106
GND	27	EX_CS_N	67	-	107
GND	28	3.3 V	68	GND	108
EX_ADDR1	29	-	69	HSS_RXCLK1	109
EX_ADDR0	30	3.3 V	70	-	110
EX_ADDR3	31	5.0 V	71	HSS_RXFRAME1	111
EX_ADDR2	32	3.3 V	72	HSS_RXDATA1	112
EX_ADDR5	33	5.0 V	73	12 V	113
EX_ADDR4	34	3.3 V	74	2.5 V	114
EX_ADDR7	35	5.0 V	75	12 V	115
EX_ADDR6	36	3.3 V	76	2.5 V	116
GND	37	5.0 V	77	12 V	117

Table 78. IXDP465 Interface Standard Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	38	3.3 V	78	2.5 V	118
EX_ADDR9	39	5.0 V	79	12 V	119
EX_ADDR8	40	3.3 V	80	2.5 V	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
GPIO signals	maroon
HSS0 signals (primary)	black
HSS1 signals (secondary)	red
not used (JTAG signals)	gray
interrupt signal	gold
RST_N	lavender

5.3.2.2 IXDP465 Interface Expansion Connector

The IXDP465 interface expansion connector contains the extended expansion bus interface (IXP465-specific), GPIO, SPI, I^2C, ID, future needs, and power signals. Table 79 shows the IXDP465 interface expansion connector signal definitions. The Legend describing the color-codes for the signals follows the table.

Table 79. IXDP465 Interface Expansion Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
1.8 V	1	C_PCI_4	41	3.3 V	81
1.8 V	2	C_PCI_5	42	3.3 V	82
GND	3	C_PCI_6	43	3.3 V	83
GND	4	C_PCI_7	44	3.3 V	84
EX_DATA17	5	C_PCI_8	45	GND	85
EX_DATA16	6	C_PCI_9	46	GND	86
EX_DATA19	7	EX_BE_N3	47	C_FN_59	87
EX_DATA18	8	EX_BE_N2	48	C_FN_60	88
GND	9	EX_BE_N1	49	C_FN_61	89
GND	10	EX_BE_N0	50	C_FN_62	90
EX_DATA21	11	EX_BURST	51	GND	91
EX_DATA20	12	EX_PAR3	52	GND	92
EX_DATA23	13	EX_PAR2	53	C_FN_63	93
EX_DATA22	14	EX_PAR1	54	GPIO5	94
GND	15	EX_PAR0	55	GPIO6	95

Table 79. IXDP465 Interface Expansion Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	16	C_NPE_0	56	GPIO7	96
EX_DATA25	17	C_NPE_1	57	GND	97
EX_DATA24	18	C_NPE_2	58	GND	98
EX_DATA27	19	C_NPE_3	59	GPIO8	99
EX_DATA26	20	C_NPE_4	60	GPIO9	100
GND	21	C_NPE_5	61	GPIO10	101
GND	22	C_NPE_6	62	GPIO11	102
EX_DATA29	23	C_NPE_7	63	GND	103
EX_DATA28	24	C_NPE_8	64	GND	104
EX_DATA31	25	C_NPE_9	65	GPIO12	105
EX_DATA30	26	C_NPE_10	66	GPIO13	106
GND	27	C_NPE_11	67	GPIO14	107
GND	28	C_NPE_12	68	GPIO15	108
EX_ADDR24	29	**CLK32_IN**	**69**	GND	109
SSPS_CLK	30	C_FN_48	70	GND	110
SSPS_FRM	31	C_FN_49	71	ID0	111
SSPS_TXD	32	C_FN_50	72	ID1	112
SSPS_RXD	33	C_FN_51	73	ID2	113
SSPS_EXTCLK	34	C_FN_52	74	ID3	114
5.0 V	35	C_FN_53	75	ID4	115
5.0 V	36	C_FN_54	76	ID5	116
C_PCI_0	37	C_FN_55	77	ID6	117
C_PCI_1	38	C_FN_56	78	ID7	118
C_PCI_2	39	C_FN_57	79	I2C_SDA	119
C_PCI_3	40	C_FN_58	80	I2C_SCL	120

Legend	
power signals	purple
expansion bus signals	green
common future needs expansion signals.	blue
dedicated future needs expansion signals (this card only)	black
SPI signals	red
I^2C signals)	gold
GPIO signals	maroon
ID signals	teal

5.3.2.3 Stacking Interface Standard Connector

The stacking interface standard connector contains the expansion bus interface, GPIO, HSS interface, and power signals to enable stacking multiple boards on an IXDP465 HSS site. This connector is pin-for-pin compatible with the IXDP425 development platform HSS interface connectors. All signals necessary to communicate with the analog ports are available on this connector. Table 80 shows the stacking interface standard connector signal definitions. The Legend describing the color-codes for the signals follows the table.

Table 80. Stacking Interface Standard Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
-	1	EX_ADDR11	41	5.0 V	81
-	2	EX_ADDR10	42	3.3 V	82
-	3	EX_ADDR13	43	GPIO2	83
-	4	EX_ADDR12	44	GPIO3	84
EX_DATA1	5	EX_ADDR15	45	GND	85
EX_DATA0	6	EX_ADDR14	46	GND	86
EX_DATA3	7	GND	47	-	87
EX_DATA2	8	GND	48	GPIO4	88
GPIO0	9	EX_ADDR17	49	-	89
GPIO1	10	EX_ADDR16	50	RST_N	90
EX_DATA5	11	EX_ADDR19	51	-	91
EX_DATA4	12	EX_ADDR18	52	HSS_TXFRAME1	92
EX_DATA7	13	EX_ADDR21	53	-	93
EX_DATA6	14	EX_ADDR20	54	HSS_TXCLK1	94
GND	15	EX_ADDR23	55	GND	95
GND	16	EX_ADDR22	56	HSS_TXDATA1	96
EX_DATA9	17	GND	57	HSS_TXDATA0	97
EX_DATA8	18	GND	58	GND	98
EX_DATA11	19	EX_CLK	59	HSS_TXFRAME0	99
EX_DATA10	20	EX_RD_N	60	HSS_RXDATA0	100
-	21	GND	61	-	101
-	22	EX_WR_N	62	HSS_RXFRAME0	102
EX_DATA13	23	EX_ALE	63	HSS_TXCLK0	103
EX_DATA12	24	EX_RDY_N	64	-	104
EX_DATA15	25	EX_IOWAIT_N	65	GND	105
EX_DATA14	26	INT_IN_N	66	HSS_RXCLK0	106
GND	27	EX_CS_N	67	-	107
GND	28	3.3 V	68	GND	108
EX_ADDR1	29	-	69	HSS_RXCLK1	109
EX_ADDR0	30	3.3 V	70	-	110
EX_ADDR3	31	5.0 V	71	HSS_RXFRAME1	111

Table 80. Stacking Interface Standard Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_ADDR2	32	3.3 V	72	HSS_RXDATA1	112
EX_ADDR5	33	5.0 V	73	12 V	113
EX_ADDR4	34	3.3 V	74	2.5 V	114
EX_ADDR7	35	5.0 V	75	12 V	115
EX_ADDR6	36	3.3 V	76	2.5 V	116
GND	37	5.0 V	77	12 V	117
GND	38	3.3 V	78	2.5 V	118
EX_ADDR9	39	5.0 V	79	12 V	119
EX_ADDR8	40	3.3 V	80	2.5 V	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
GPIO signals	maroon
HSS0 signals (primary)	black
HSS1 signals (secondary)	red
not used (JTAG signals)	gray
interrupt signal	gold
RST_N	lavender

5.3.2.4 Stacking Interface Expansion Connector

The stacking interface expansion connector contains the extended expansion bus interface (IXDP465-specific), GPIO, SPI, I^2C, ID, future needs, and power signals. Table 81 shows the stacking interface expansion connector signal definitions. The Legend describing the color-codes for the signals follows the table.

Table 81. Stacking Interface Expansion Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
1.8 V	1	C_PCI_4	41	3.3 V	81
1.8 V	2	C_PCI_5	42	3.3 V	82
GND	3	C_PCI_6	43	3.3 V	83
GND	4	C_PCI_7	44	3.3 V	84
EX_DATA17	5	C_PCI_8	45	GND	85
EX_DATA16	6	C_PCI_9	46	GND	86
EX_DATA19	7	EX_BE_N3	47	C_FN_59	87
EX_DATA18	8	EX_BE_N2	48	C_FN_60	88
GND	9	EX_BE_N1	49	C_FN_61	89

Table 81. Stacking Interface Expansion Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	10	EX_BE_N0	50	C_FN_62	90
EX_DATA21	11	EX_BURST	51	GND	91
EX_DATA20	12	EX_PAR3	52	GND	92
EX_DATA23	13	EX_PAR2	53	C_FN_63	93
EX_DATA22	14	EX_PAR1	54	GPIO5	94
GND	15	EX_PAR0	55	GPIO6	95
GND	16	C_NPE_0	56	GPIO7	96
EX_DATA25	17	C_NPE_1	57	GND	97
EX_DATA24	18	C_NPE_2	58	GND	98
EX_DATA27	19	C_NPE_3	59	GPIO8	99
EX_DATA26	20	C_NPE_4	60	GPIO9	100
GND	21	C_NPE_5	61	GPIO10	101
GND	22	C_NPE_6	62	GPIO11	102
EX_DATA29	23	C_NPE_7	63	GND	103
EX_DATA28	24	C_NPE_8	64	GND	104
EX_DATA31	25	C_NPE_9	65	GPIO12	105
EX_DATA30	26	C_NPE_10	66	GPIO13	106
GND	27	C_NPE_11	67	GPIO14	107
GND	28	C_NPE_12	68	GPIO15	108
EX_ADDR24	29	CLK32_OUT	69	GND	109
SSPS_CLK	30	C_FN_48	70	GND	110
SSPS_FRM	31	C_FN_49	71	-	111
SSPS_TXD	32	C_FN_50	72	ID0	112
SSPS_RXD	33	C_FN_51	73	ID1	113
SSPS_EXTCLK	34	C_FN_52	74	ID2	114
5.0 V	35	C_FN_53	75	ID3	115
5.0 V	36	C_FN_54	76	ID4	116
C_PCI_0	37	C_FN_55	77	ID5	117
C_PCI_1	38	C_FN_56	78	ID6	118
C_PCI_2	39	C_FN_57	79	I2C_SDA	119
C_PCI_3	40	C_FN_58	80	I2C_SCL	120

Legend	
power signals	purple
expansion bus signals	green
common future needs expansion signals.	blue

Legend (Continued)	
dedicated future needs expansion signals (this card only)	black
SPI signals	red
I^2C signals)	gold
GPIO signals	maroon
ID signals	teal
not used	gray
CLK32_OUT pin 69 (one signal in group)	lavender

5.3.3 Analog Voice Card Stacking

The IXDP465 platform supports stacking up to eight IXPVM465 Analog Voice mezzanine cards. The board ID accesses the following four interfaces: expansion bus accesses, clocking, framing, and PCM voice interface.

5.3.3.1 Board ID

Eight signals on the IXDP465 expansion interface connector define a unique address on each of the stacked analog voice mezzanine cards. Since this connector does not exist on the IXDP425 development platform, a mechanism has been implemented on the IXPVM465 Analog Voice mezzanine card (4x1) to emulate connection to the IXDP465 platform when the card is used on an IXDP425 platform.

The IXDP465 platform ties ID0 to ground, and ID7 - ID1 to 3.3 V. The IXDVM465 Analog Voice mezzanine card pulls down ID0 (using a 100 kΩ resistor) and pulls up ID7 - ID1 (using a 49.9 kΩ resistor) to function on the IXDP425 platform. The signals must be shifted from the IXDP465 interface expansion connector to the stacking interface expansion connector (i.e., IXDP465 ID6 - ID0 shifted to Stacking ID7- ID1, with the 100 kΩ pull-down on the next module up-the-chain filling in a logic low for ID0). Table 82 shows the unique IDs for each stacked analog voice 4x1 mezzanine card.

Table 82. Analog Voice Card Unique Stacking IDs

Stacking Slot	ID7 - ID0
0	11111110
1	11111100
2	11111000
3	11110000
4	11100000
5	11000000
6	10000000
7	00000000

5.3.3.2 Expansion Bus Accesses

The IXDP465 platform expansion bus contains 25 address bits (**EX_ADDR24 - EX_ADDR0**). The expansion address signals **EX_ADDR23** through **EX_ADDR21** select one of up to eight stacked mezzanine cards. Table 83 shows the unique IDs along with the upper expansion bus address signals of each stacked Analog Voice 4x1 card used for expansion bus accesses.

Table 83. Analog Voice Card Unique Stacking IDs and Expansion Bus Addresses

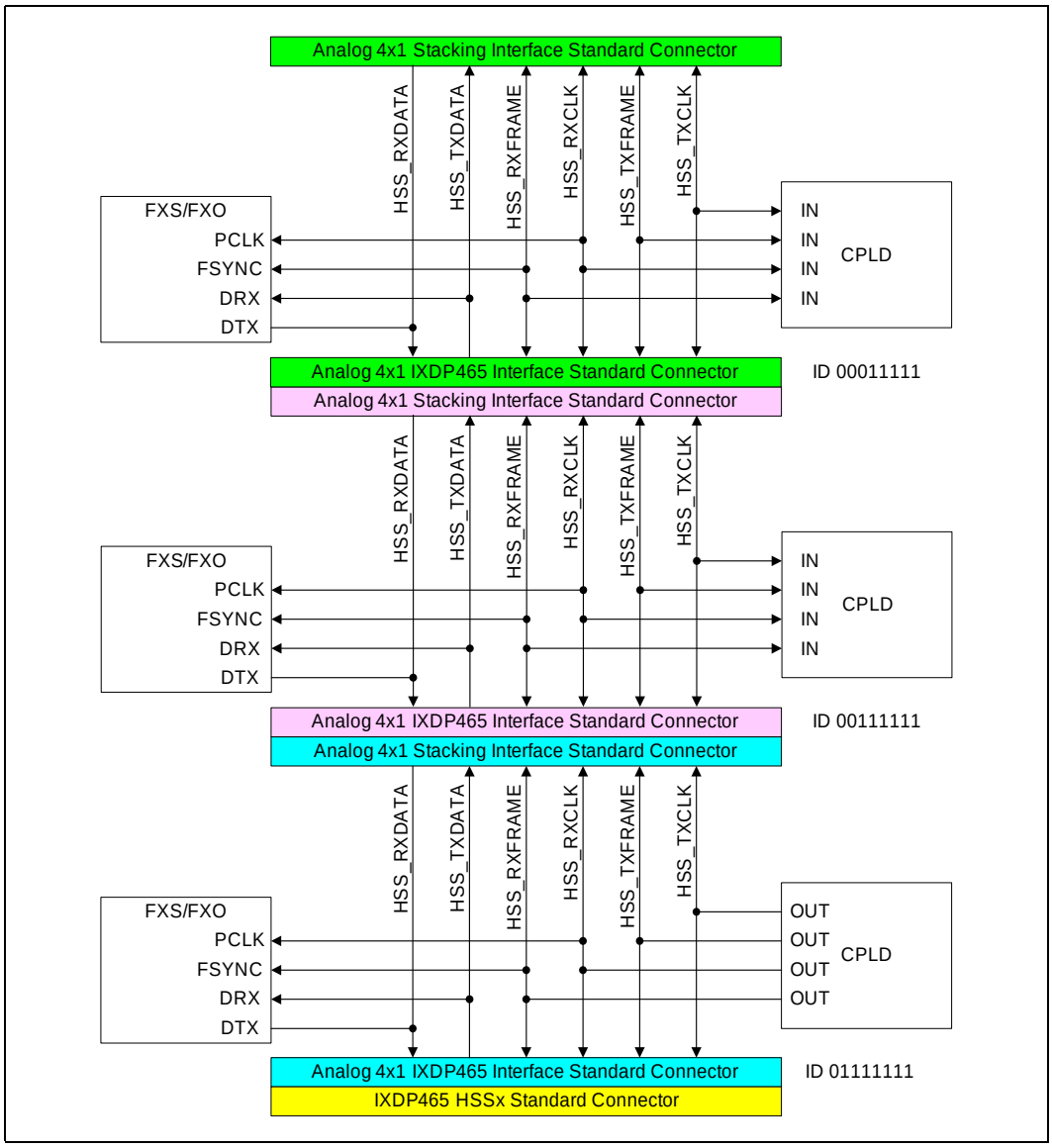
Stacking Slot	ID7 - ID0	EX_ADDR23 - EX_ADDR21
0	11111110	000
1	11111100	001
2	11111000	010
3	11110000	011
4	11100000	100
5	11000000	101
6	10000000	110
7	00000000	111

Note: The IXP425 network processor on the IXDP425 development platform only uses 24 bits. **EX_ADDR24** does not exist, so for compatibility, it is not used on the IXPVM465 Analog Voice mezzanine card for address decode.

5.3.3.3 Clocking/Framing

The PCM (analog voice) bus clocking and framing source is dependent on the board ID. The HSS interface on the IXDP465 platform host network processor is used as the communication path for the PCM data. Since the HSS internal clock generation has too much jitter for analog applications, an external clock is generated by the Analog Voice mezzanine card CPLD, along with the frame. Only the first (of eight maximum) mezzanine card drives these signals, with the HSS and the rest of the stacked mezzanine cards receiving them. Figure 28 shows a PCM interface signal flow drawing.

Figure 28. Analog Voice Card Stacking PCM Interface



The IXDP465 platform delivers a 32.768 MHz clock to each of the mezzanine cards on the IXDP465 interface expansion connector (**CLK32_IN**). The IXDP425 development platform does not provide a 32.768 MHz clock. Therefore, an optional 32.768 MHz oscillator circuit that is not populated for the IXDP465 platform Analog Voice mezzanine cards is designed into the Analog Voice mezzanine card. Only the first board in the stack uses this and propagates it to the next card in the stack. See Section 5.3.5, “Analog Voice Card CPLD” for further information.

5.3.4 Analog Voice Card SPI Interface

The SPI interface accesses control and status information from the FXO and FXS channels. Since the interface is different for FXO and FXS, two SPI protocols are used. For the IXDP465 platform, the dedicated SPI interface is used, while on the IXDP425 development platform, three GPIOs emulate the SPI interface.

5.3.4.1 FXO SPI Interface

The SPI interface for access control and status information for the FXO (Si3050) uses a 24-bit serial interface. Four signals from the CPLD control this interface. These signals are routed to the SPI interface for IXDP465 applications or to GPIO for IXDP425 applications. The signals are **FXO_CS_N** (shown as CSB in Figure 29 and Figure 30), **SCLK**, **SDI**, and **SDO**. Figure 29 shows a typical SPI read of status information from the FXO port.

Figure 29. FXO Read Operation Using 8-Bit SPI

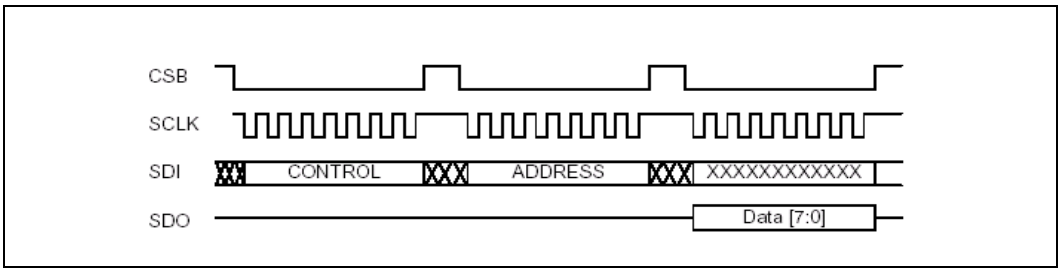


Figure 30 shows a typical SPI write of control information to the FXO port.

Figure 30. FXO Write Operation Using 8-Bit SPI

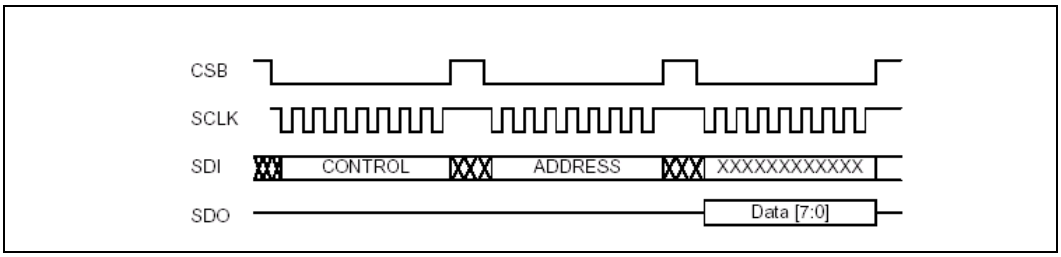


Figure 31 and Table 84 define the control byte for accesses through the SPI interface.

Figure 31. SPI Control Byte

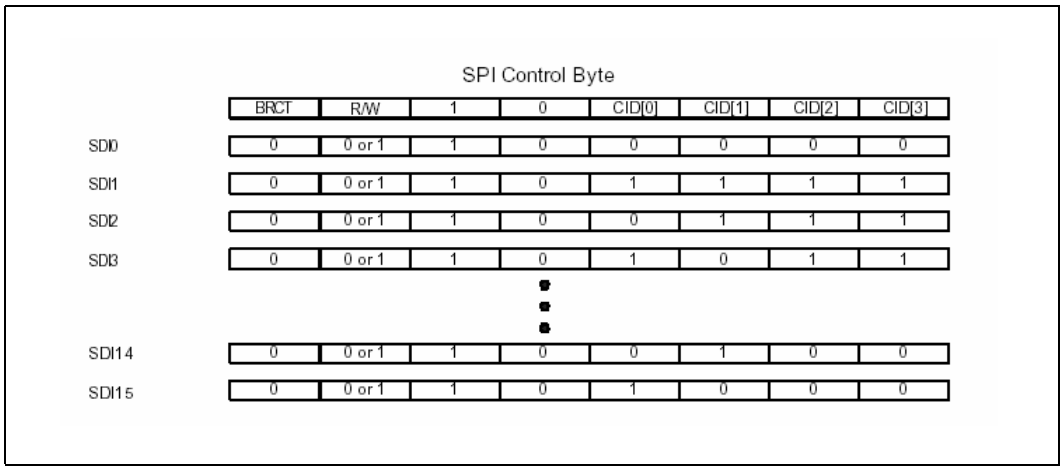


Table 84. Control Byte Bit Definition

7	BRCT	Indicates a broadcast operation for all devices in the daisy chain. This is only valid for Write operations because it causes contention on the SDO pin during a Read.
6	R/W	Read/Write Bit: **1** = Read operation **0** = Write operation
5	1	This bit must always be 1.
4	0	This bit must always be 0.
3:0	CID[0:3]	This field indicates the channel that is targeted by the operation. The 4-bit channel value is provided with the LSB first. The devices reside on the daisy chain with device 0 nearest to the controller and device 15 farthest away in the SDI/SDITHRU chain. See Figure 31. As the CID information propagates down the daisy chain, each channel decrements the CID by one. The device that receives a value of 0 in the CID field responds to the SPI transaction. See Figure 31. If a broadcast to all devices connected to the chain is requested, the CID does not decrement. In this case, the same 8- or 16-bit data is presented to all channels regardless of the CID values.

5.3.4.2 FXS SPI Interface

The SPI interface for access control and status information for the FXS (Silicon Laboratories* Si3210) uses a 16-bit serial interface. Four signals from the CPLD control this interface. These signals are routed to the SPI interface for IXDP465 applications or to GPIO for IXDP425 applications. The signals are **FXSn_CS_N** (shown as **$\overline{\text{CS}}$** in Figure 32, Figure 33, and Figure 34), **SCLK, SDI** and **SDO**. The four FXS ports are daisy-chained as shown in Figure 32.

Figure 32. FXS Port SPI Daisy-Chaining

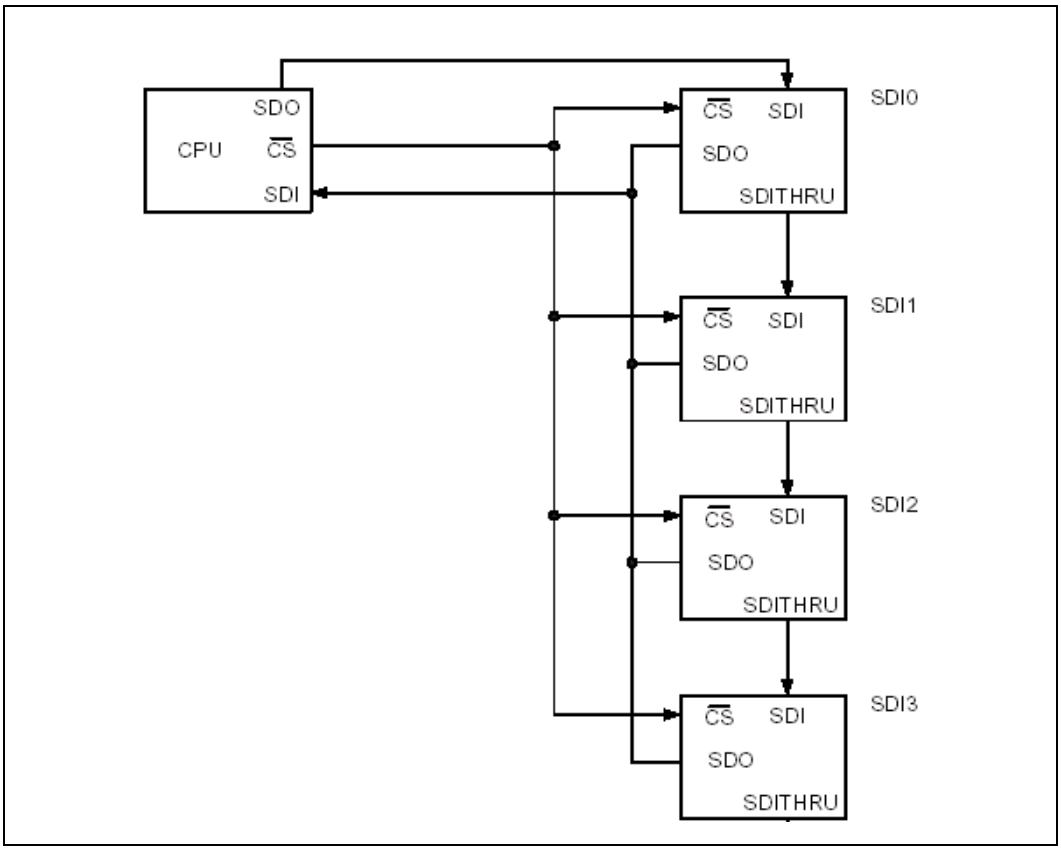


Figure 33 shows a typical SPI read of status information from the FXS port.

Figure 33. FXS Read Operation Through 8-Bit SPI

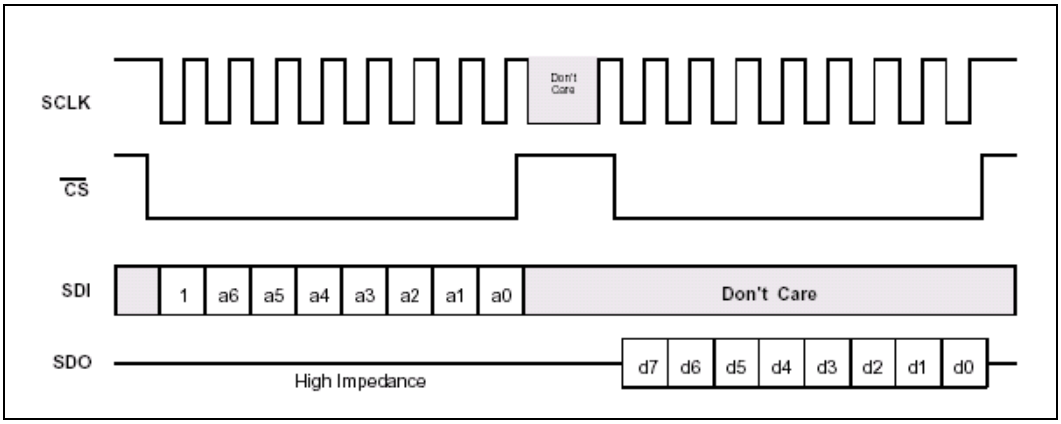
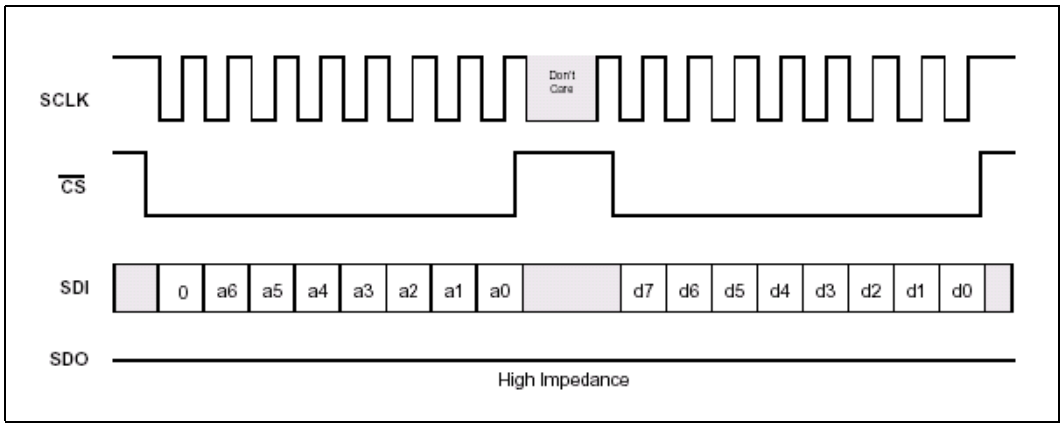


Figure 34 shows a typical SPI write of control information to the FXS port.

Figure 34. FXS Write Operation Through 8-Bit SPI



5.3.5 Analog Voice Card CPLD

The CPLD on the IXPVM465 Analog Voice mezzanine card:

- generates the following signals: PCM clocks, PCM frame synchronization pulses, analog port resets, analog port chip selects, interrupt to the IXDP465 platform, engaged/disengage relays, and the master clock
- reports board and interrupt status

Table 85 defines the CPLD pin definitions.

Table 85. Analog Voice Card CPLD Pin Assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	TEST3	26	1.8 V	51	3.3 V	76	EX_DATA3
2	SSPS_CLK	27	EX_CLK	52	SCLK	77	ID6
3	TEST2	28	TEST5	53	FXO_TGD_N	78	ID7
4	TEST1	29	RELAY_P	54	ID5	79	FXO_RGDT_N
5	3.3 V	30	EX_WR_N	55	ID4	80	FXO_RESET_N
6	EX_ADDR0	31	GND	56	ID3	81	FXS0_RESET_N
7	EX_ADDR1	32	EX_RD_N	57	1.8 V	82	FXS1_RESET_N
8	EX_ADDR2	33	INT_OUT_N	58	ID2	83	TDO
9	EX_ADDR3	34	FXO_INT_N	59	ID1	84	GND
10	EX_ADDR4	35	FXS0_INT_N	60	ID0	85	FXS2_RESET_N
11	EX_ADDR21	36	FXS1_INT_N	61	EX_DATA0	86	FXS3_RESET_N
12	EX_ADDR22	37	FXS2_INT_N	62	GND	87	FXO_RC_N
13	EX_ADDR23	38	3.3 V	63	EX_DATA1	88	3.3 V
14	HSS_RXCLK0	39	FXS3_INT_N	64	EX_DATA2	89	FXO_TGDE_N
15	HSS_RXDATA0	40	INT_N_IN	65	GPIO0	90	FXS0_CS_N
16	HSS_RXFRAME0	41	I2C_SCL	66	GPIO1	91	FXS1_CS_N

Table 85. Analog Voice Card CPLD Pin Assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
17	HSS_TXCLK0	42	I2C_SDA	67	GPIO2	92	FXS2_CS_N
18	HSS_TXDATA0	43	SSPS_FRM	68	GPIO3	93	FXS3_CS_N
19	HSS_TXFRAME0	44	SSPS_RXD	69	GND	94	FXO_CS_N
20	3.3 V	45	TDI	70	GPIO4	95	EX_CS_N
21	GND	46	SSPS_TXD	71	EX_DATA7	96	CLK32_OUT
22	CLK32_IN	47	TMS	72	EX_DATA6	97	SSPS_EXTCLK
23	CLK32.768M_L_R	48	TCK	73	EX_DATA5	98	3.3 V
24	RST_N	49	SDI	74	EX_DATA4	99	TEST4
25	GND	50	SDO	75	GND	100	GND

5.3.5.1 Internal CPLD Registers

The expansion bus accesses internal CPLD registers. The CPLD must decode the proper upper expansion bus address based upon its ID in the stack. See Section 5.4.2.4, “Stacking Interface Expansion Connector” for further details. The lower five expansion address bits decode which register is accessed. Table 86 lists the internal CPLD registers on the Analog Voice mezzanine card.

Table 86. Internal CPLD Registers

Register Name	EX_ADDR4 – EX_ADDR0	Access Type
Board Status	00000	Read Only
Analog IC Chip Selects	00001	Read/Write
Interrupt Status	00010	Read Only
Relay Control	00011	Read/Write
IXDP425/IXDP465 Mode	00100	Read/Write
PCM Mode	00101	Read/Write
Port Reset	00110	Read/Write
Reserved	00111 - 11111	n/a

The Board Status register is a read only register that contains the same information that is accessed using the I^2C interface. See Section 5.3.5.5, “I2C Interface” for details.

Analog IC Chip Selects Register

The Analog IC Chip Selects register is a read/write register that selects which analog port is accessed by the SPI interface. See Section 5.3.5.2, “SPI Interface” for details. Care must be taken to ensure that only one chip select is in the active state (logic low). The value of this register after reset is xxxxxx11. The table below defines this register’s bit definition.

7	6	5	4	3	2	1	0
x	x	x	x	x	x	FXO	FXS

Interrupt Status Register

The Interrupt Status register is a read only and active high (bit is high, interrupt is pending) register that indicates which analog port is requesting interrupt service. Multiple ports can request interrupt service simultaneously. The table below defines this register's bit definition.

7	6	5	4	3	2	1	0
x	x	x	FXO	FXS3	FXS2	FXS1	FXS0

Relay Control Register

The Relay Control register is a read/write register that selects the five switchover relays state. The active (logic high) or inactive (logic low) relay state is set by writing this register. The value of this register after reset is xxxxxxx0. The table below defines this register's bit definition.

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	Relay

IXDP425/IXDP465 Mode Register

The IXDP425/IXDP465 Mode register is a read/write register that selects the clock source for analog clocking and framing and it also selects which interface to run all SPI signals on. A logic low (0) on bit 0 indicates that the analog clock source is the IXDP465 Interface Expansion connector, while a logic high (1) indicates that the clock source is an onboard oscillator (for IXDP425 support).

A logic low (0) on bit 1 indicates that the IXP465 network processor SPI interface is being used for all SPI signals (only on the IXDP465 platform), while a logic high (1) will use GPIO for the SPI interface (IXDP425 or IXDP465 development platforms). The value of this register after reset is xxxxxx00. The table below defines this register's bit definitions.

7	6	5	4	3	2	1	0
x	x	x	x	x	x	SSPS/ GPIO Mode	Analog Clock Source

PCM Mode Register

The PCM Mode register is a read/write register that selects the mode of operation for the PCM bus. When operating in µ-Law or A-Law mode, an 8-bit PCM data width is required. When operating in linear mode, a 16-bit PCM data width is required. The value of this register after reset is xxxxx000. The table below defines this register's bit definition.

7	6	5	4	3	2	1	0
x	x	x	x	x	I2C_ Enb	PCM1	PCM0

The **I2C_Enb** bit is for mezzanine card identification (discovery) purposes only. This function is performed at power up to identify the type of mezzanine cards installed on the IXDP465 platform. The I^2C bus is shared between the onboard IXDP465 platform serial EEPROM and all five mezzanine card slots. This bit is enabled (1) only during discovery of the IXDP465 platform mezzanine cards and must be disabled (0) during normal operation.

PCM(1:0) selects the PCM clock frequency. This determines the number of bits per frame. The number of slots per frame is dependent upon the data type (µ-Law, A-Law, linear). The data type is important to the IXP465 network processor HSS and the Silicon Laboratories* analog interface IC configuration, not this CPLD configuration. Table 87 shows the bits and slots per frame for each PCM configuration.

Table 87. PCM Modes

PCM Mode	Data Type	Bits per Frame	Slots per Frame	PCM Clock
00	16-bit	256	16	2.048 MHz
00	8-bit	256	32	2.048 MHz
01	16-bit	512	32	4.096 MHz
01	8-bit	512	64	4.096 MHz
10	16-bit	1024	64	8.192 MHz
10	8-bit	1024	128	8.192 MHz
11	X	X	X	Reserved

Analog Port Reset Register

The Analog Port Reset register is a read/write register that resets each analog port. A logic low (0) indicates the port is in a Reset state, while a logic high (1) indicates that the port is in a normal mode of operation. The value of this register after reset is xxx00000

The table below defines this register's bit definition.

7	6	5	4	3	2	1	0
x	x	x	FXS3	FXS2	FXS1	FXS0	FXO

5.3.5.2 SPI Interface

The CPLD controls which analog port is being accessed using the SPI interface through the Analog Chip Select register. The FXO SPI Interface and the FXS SPI Interface are not identical, so care must be taken when communicating with the analog ports through these interfaces.

5.3.5.3 PCM Clocks and Framing

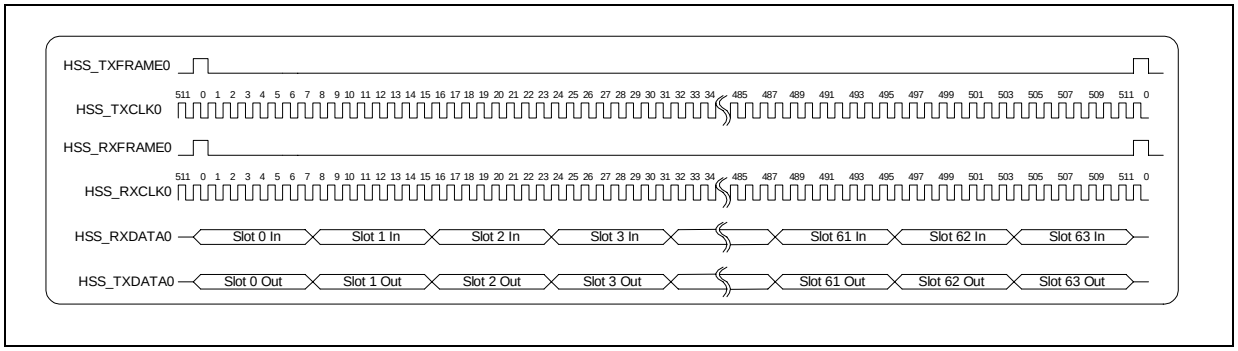
The CPLD generates the PCM clocks and framing information from the 32.768 MHz clock. Only the CPLD on the first IXPVM465 Analog Voice mezzanine card in the stack generates these signals. CPLDs on modules further up the stack receive these signals from the first mezzanine card. (See Section 5.3.3.3, "Clocking/Framing" for further details). The maximum number of Analog Voice cards in a stack is eight. With five slots of PCM (voice) data per card, the PCM is designed to support 64 slots. Table 88 defines the clock frequency and number of bits in a frame (clocks between frame synchronization pulses).

The CPLD must generate a frame synchronization pulse at the following rates:

- In 2.048 MHz mode: frame synchronization pulse every 256 PCM clocks
- In 4.096 MHz mode: frame synchronization pulse every 512 PCM clocks
- In 8.192 MHz mode: frame synchronization pulse every 1024 PCM clocks

Figure 35 shows the 4.096 MHz mode (with the 8-bit data type) clocking and framing generated by the CPLD.

Figure 35. PCM Operation with 8-Bit Slots



Each analog port must transmit and receive its analog voice data on a unique PCM slot. Table 88 defines the PCM slot configuration.

Table 88. PCM Slot Assignments

Slot	Board/Channel	Slot	Board/Channel	Slot	Board/Channel	Slot	Board/Channel
0	0 / FXO	16	3 / FXS0	32	6 / FXS1	48	-
1	0 / FXS0	17	3 / FXS1	33	6 / FXS2	49	-
2	0 / FXS1	18	3 / FXS2	34	6 / FXS3	50	-
3	0 / FXS2	19	3 / FXS3	35	7 / FXO	51	-
4	0 / FXS3	20	4 / FXO	36	7 / FXS0	52	-
5	1 / FXO	21	4 / FXS0	37	7 / FXS1	53	-
6	1 / FXS0	22	4 / FXS1	38	7 / FXS2	54	-
7	1 / FXS1	23	4 / FXS2	39	7 / FXS3	55	-
8	1 / FXS2	24	4 / FXS3	40	-	56	-
9	1 / FXS3	25	5 / FXO	41	-	57	-
10	2 / FXO	26	5 / FXS0	42	-	58	-
11	2 / FXS0	27	5 / FXS1	43	-	59	-
12	2 / FXS1	28	5 / FXS2	44	-	60	-
13	2 / FXS2	29	5 / FXS3	45	-	61	-
14	2 / FXS3	30	6 / FXO	46	-	62	-
15	3 / FXO	31	6 / FXS0	47	-	63	-

5.3.5.4 Master Clock

The CPLD generates an output clock that is fed to the next board in the stack, because all analog ports in the stack must run from the same 32.768 MHz clock to function properly. The clock source is controlled by the analog clock source register. See "IXDP425/IXDP465 Mode Register" on page 136 for details.

5.3.5.5 I²C Interface

The CPLD supports I²C Reads only; Write is not supported. The Board Status register contains detailed information about the board.

Status Register

A typical example of the Status register for the HSS Analog Voice mezzanine card is shown in the table below. This example is based on: Board ID = 4 (shown in light gray) and board revision = 2 (shown in dark gray).

7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	0

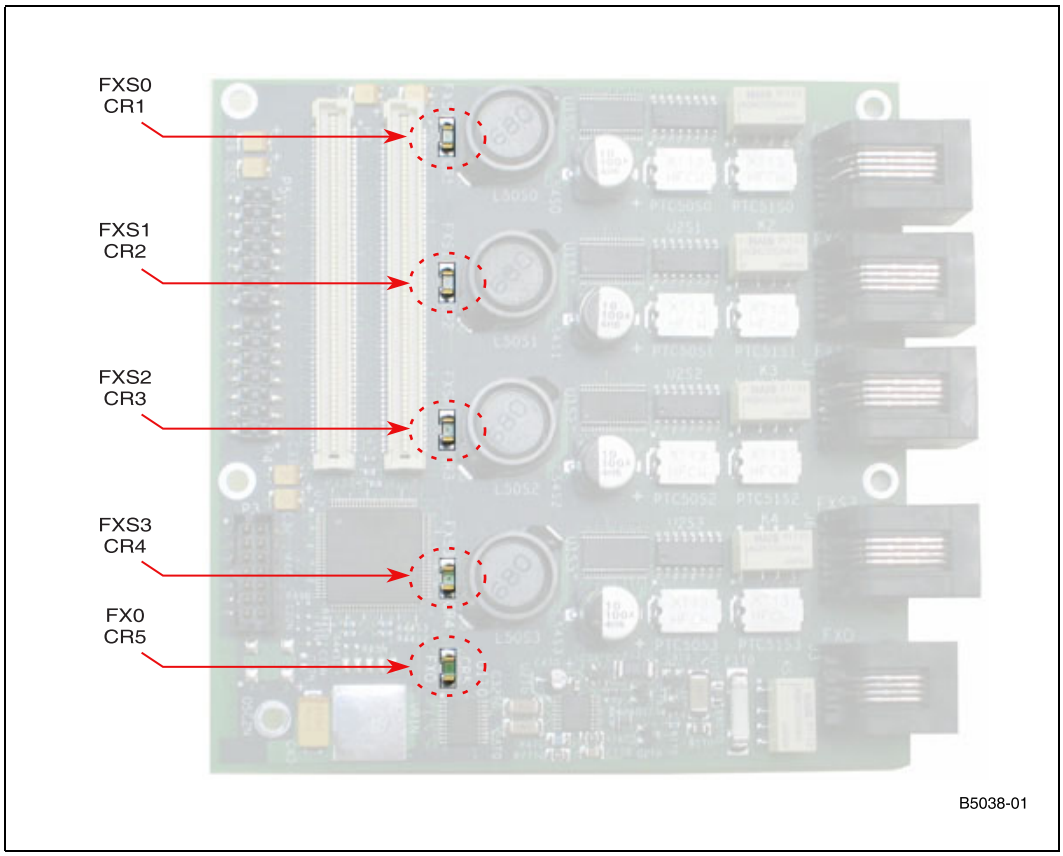
5.3.5.6 Relay Control

The CPLD controls the five relays with the **RELAY_P** signal. When the **RST_N** signal is active, the CPLD drives **RELAY_P** to an inactive state (logic 0). The relays are engaged or disengaged through expansion bus writing of the relay control register. See Section 5.3.5.1, "Internal CPLD Registers" for more information.

5.3.5.7 LED Indicators

There are five LEDs that indicate the status of each analog port. When the port is being held in a Reset (under software control), the LEDs are not illuminated. When the ports are in an active state, the LEDs are illuminated. Figure 36 shows the LED locations.

Figure 36. Analog Voice Mezzanine Card Port Status LEDs



5.4 IXPFRM465 Quad T1/E1 Mezzanine Card

5.4.1 Introduction

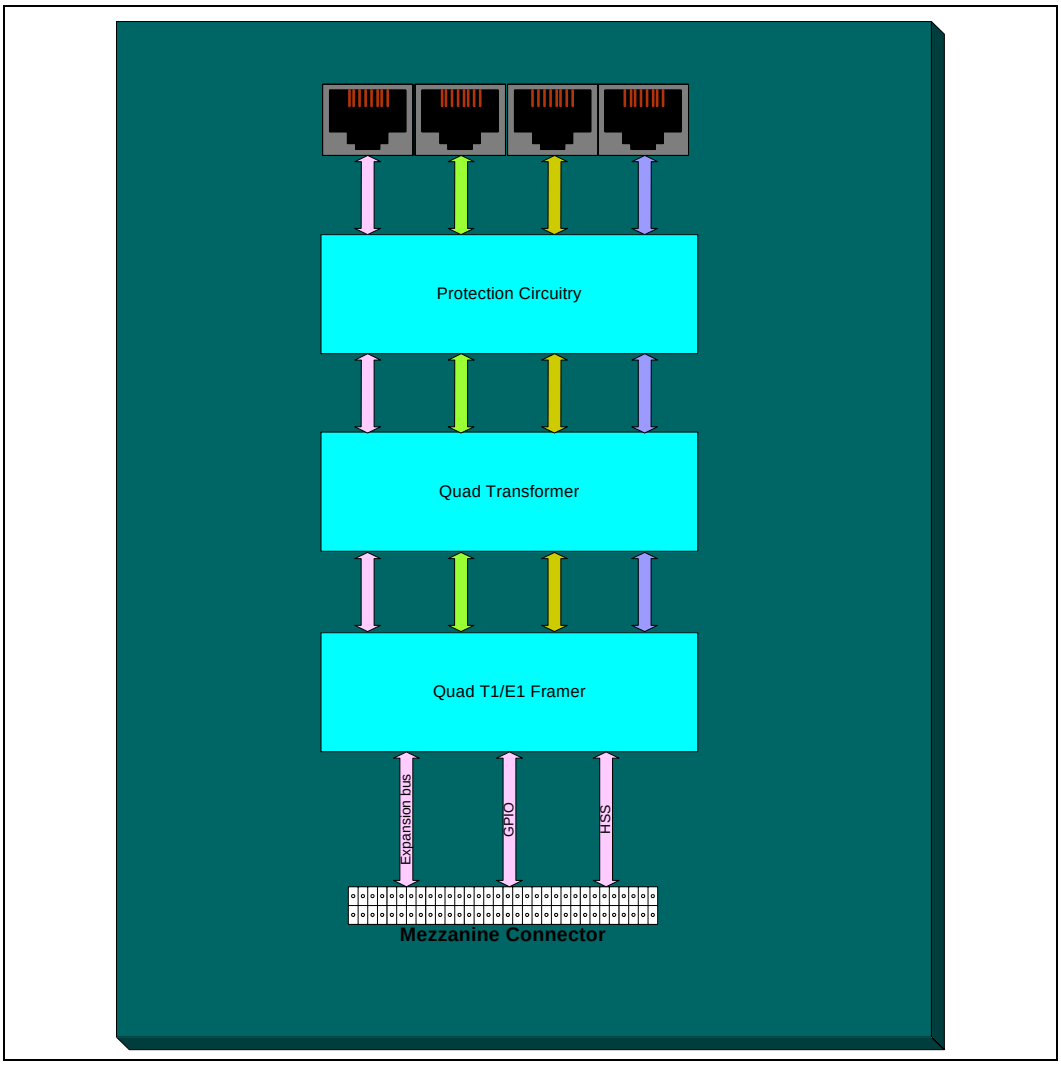
The IXPFRM465 Quad T1/E1 mezzanine card plugs into the baseboard through the standard 120-pin connector, which is the same as that used on the Intel® IXDP425 / IXCDP1100 Development Platform. The pin-out is the same as the HSS connectors on the IXDP425 / IXCDP1100 platform, with the second (alternate) HSS port being routed to IXDP425 connector unused pins, allowing the device to be stackable (two high). The stacking connector is physically identical and the signaling is copied, with the exception of routing the alternate HSS port up to the second card.

The IXDP465 platform achieves control and status of:

- the T1 ports via the expansion bus interface
- the voice interface via the HSS interface

GPIO is used for interrupts. Figure 37 shows the IXPFRM465 Quad T1/E1 mezzanine card components.

Figure 37. Quad T1/E1 Mezzanine Card Logical Block Diagram



5.4.2 Quad T1/E1 Card Connector Interfaces

5.4.2.1 IXDP465 Interface Standard Connector

The IXDP465 interface standard connector contains the expansion bus interface, GPIO, HSS interface, and power signals. This connector is pin-for-pin compatible with the IXDP425 HSS interface connectors. All signals necessary to communicate with the analog ports are available on this connector. Table 89 defines the IXDP465 interface standard connector signals. The Legend describing the color-codes for the signals follows the table.

Table 89. IXDP465 Interface Standard Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
-	1	EX_ADDR11	41	5.0 V	81
-	2	EX_ADDR10	42	3.3 V	82
-	3	EX_ADDR13	43	GPIO2	83
-	4	EX_ADDR12	44	GPIO3	84
EX_DATA1	5	EX_ADDR15	45	GND	85
EX_DATA0	6	EX_ADDR14	46	GND	86
EX_DATA3	7	GND	47	-	87
EX_DATA2	8	GND	48	GPIO4	88
GPIO0	9	EX_ADDR17	49	-	89
GPIO1	10	EX_ADDR16	50	RST_N	90
EX_DATA5	11	EX_ADDR19	51	-	91
EX_DATA4	12	EX_ADDR18	52	HSS_SEC_TXFRAME	92
EX_DATA7	13	EX_ADDR21	53	-	93
EX_DATA6	14	EX_ADDR20	54	HSS_SEC_TXCLK	94
GND	15	EX_ADDR23	55	GND	95
GND	16	EX_ADDR22	56	HSS_SEC_TXDATA	96
EX_DATA9	17	GND	57	HSS_PRI_TXDATA	97
EX_DATA8	18	GND	58	GND	98
EX_DATA11	19	EX_CLK	59	HSS_PRI_TXFRAME	99
EX_DATA10	20	EX_RD_N	60	HSS_PRI_RXDATA	100
-	21	GND	61	-	101
-	22	EX_WR_N	62	HSS_PRI_RXFRAME	102
EX_DATA13	23	EX_ALE	63	HSS_PRI_TXCLK	103
EX_DATA12	24	EX_RDY_N	64	-	104
EX_DATA15	25	EX_IOWAIT_N	65	GND	105
EX_DATA14	26	INT_OUT_N	66	HSS_PRI_RXCLK	106
GND	27	EX_CS_N	67	-	107
GND	28	3.3 V	68	GND	108
EX_ADDR1	29	-	69	HSS_SEC_RXCLK	109
EX_ADDR0	30	3.3 V	70	-	110
EX_ADDR3	31	5.0 V	71	HSS_SEC_RXFRAME	111
EX_ADDR2	32	3.3 V	72	HSS_SEC_RXDATA	112
EX_ADDR5	33	5.0 V	73	12 V	113
EX_ADDR4	34	3.3 V	74	2.5 V	114
EX_ADDR7	35	5.0 V	75	12 V	115
EX_ADDR6	36	3.3 V	76	2.5 V	116
GND	37	5.0 V	77	12 V	117

Table 89. IXDP465 Interface Standard Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
GND	38	3.3 V	78	2.5 V	118
EX_ADDR9	39	5.0 V	79	12 V	119
EX_ADDR8	40	3.3 V	80	2.5 V	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
GPIO signals	maroon
HSS signals (primary)	black
HSS signals (secondary)	red
not used (JTAG signals)	gray
interrupt signal	gold

5.4.2.2 IXDP465 Interface Expansion Connector

The IXDP465 interface expansion connector contains the extended expansion bus interface (IXP465-specific), GPIO, SPI, I2C, ID, future needs, and power signals. Table 90 defines the IXDP465 interface expansion connector signals. The Legend describing the color-codes for the signals follows the table.

Table 90. IXDP465 Interface Expansion Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
1.8 V	1	C_PCI_4	41	3.3 V	81
1.8 V	2	C_PCI_5	42	3.3 V	82
GND	3	C_PCI_6	43	3.3 V	83
GND	4	C_PCI_7	44	3.3 V	84
EX_DATA17	5	C_PCI_8	45	GND	85
EX_DATA16	6	C_PCI_9	46	GND	86
EX_DATA19	7	EX_BE_N3	47	C_FN_59	87
EX_DATA18	8	EX_BE_N2	48	C_FN_60	88
GND	9	EX_BE_N1	49	C_FN_61	89
GND	10	EX_BE_N0	50	C_FN_62	90
EX_DATA21	11	EX_BURST	51	GND	91
EX_DATA20	12	EX_PAR3	52	GND	92
EX_DATA23	13	EX_PAR2	53	C_FN_63	93
EX_DATA22	14	EX_PAR1	54	GPIO5	94
GND	15	EX_PAR0	55	GPIO6	95
GND	16	C_NPE_0	56	GPIO7	96

Table 90. IXDP465 Interface Expansion Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_DATA25	17	C_NPE_1	57	GND	97
EX_DATA24	18	C_NPE_2	58	GND	98
EX_DATA27	19	C_NPE_3	59	GPIO8	99
EX_DATA26	20	C_NPE_4	60	GPIO9	100
GND	21	C_NPE_5	61	GPIO10	101
GND	22	C_NPE_6	62	GPIO11	102
EX_DATA29	23	C_NPE_7	63	GND	103
EX_DATA28	24	C_NPE_8	64	GND	104
EX_DATA31	25	C_NPE_9	65	GPIO12	105
EX_DATA30	26	C_NPE_10	66	GPIO13	106
GND	27	C_NPE_11	67	GPIO14	107
GND	28	C_NPE_12	68	GPIO15	108
EX_ADDR24	29	CLK32.768M_R_R	69	GND	109
SSPS_CLK	30	C_FN_48	70	GND	110
SSPS_FRM	31	C_FN_49	71	ID0	111
SSPS_TXD	32	C_FN_50	72	ID1	112
SSPS_RXD	33	C_FN_51	73	ID2	113
SSPS_EXTCLK	34	C_FN_52	74	ID3	114
5.0 V	35	C_FN_53	75	ID4	115
5.0 V	36	C_FN_54	76	ID5	116
C_PCI_0	37	C_FN_55	77	ID6	117
C_PCI_1	38	C_FN_56	78	ID7	118
C_PCI_2	39	C_FN_57	79	I2C_SDA	119
C_PCI_3	40	C_FN_58	80	I2C_SCL	120

Legend	
power signals	purple
expansion bus signals	green
common future needs expansion signals.	blue
dedicated future needs expansion signals (this card only)	black
SPI signals	red
I^2C signals)	gold
GPIO signals	maroon
ID signals	teal

5.4.2.3 Stacking Interface Standard Connector

The stacking interface standard connector contains the expansion bus interface, GPIO, HSS interface, and power signals. This connector is pin-for-pin compatible with the IXDP425 HSS interface connectors. All signals necessary to communicate with the analog ports are available on this connector. Table 91 defines the stacking interface standard connector signals. The Legend describing the color-codes for the signals follows the table.

Table 91. Stacking Interface Standard Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
-	1	EX_ADDR11	41	5.0 V	81
-	2	EX_ADDR10	42	3.3 V	82
-	3	EX_ADDR13	43	GPIO2	83
-	4	EX_ADDR12	44	GPIO3	84
EX_DATA1	5	EX_ADDR15	45	GND	85
EX_DATA0	6	EX_ADDR14	46	GND	86
EX_DATA3	7	GND	47	-	87
EX_DATA2	8	GND	48	GPIO4	88
GPIO0	9	EX_ADDR17	49	-	89
GPIO1	10	EX_ADDR16	50	RST_N	90
EX_DATA5	11	EX_ADDR19	51	-	91
EX_DATA4	12	EX_ADDR18	52	HSS_SEC_TXFRAME	92
EX_DATA7	13	EX_ADDR21	53	-	93
EX_DATA6	14	EX_ADDR20	54	HSS_SEC_TXCLK	94
GND	15	EX_ADDR23	55	GND	95
GND	16	EX_ADDR22	56	HSS_SEC_TXDATA	96
EX_DATA9	17	GND	57	HSS_PRI_TXDATA	97
EX_DATA8	18	GND	58	GND	98
EX_DATA11	19	EX_CLK	59	HSS_PRI_TXFRAME	99
EX_DATA10	20	EX_RD_N	60	HSS_PRI_RXDATA	100
-	21	GND	61	-	101
-	22	EX_WR_N	62	HSS_PRI_RXFRAME	102
EX_DATA13	23	EX_ALE	63	HSS_PRI_TXCLK	103
EX_DATA12	24	EX_RDY_N	64	-	104
EX_DATA15	25	EX_IOWAIT_N	65	GND	105
EX_DATA14	26	HSS_INT_OUT_N	66	HSS_PRI_RXCLK	106
GND	27	EX_CS_N	67	-	107
GND	28	3.3 V	68	GND	108
EX_ADDR1	29	-	69	HSS_SEC_RXCLK	109
EX_ADDR0	30	3.3 V	70	-	110
EX_ADDR3	31	5.0 V	71	HSS_SEC_RXFRAME	111
EX_ADDR2	32	3.3 V	72	HSS_SEC_RXDATA	112

Table 91. Stacking Interface Standard Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_ADDR5	33	5.0 V	73	12 V	113
EX_ADDR4	34	3.3 V	74	2.5 V	114
EX_ADDR7	35	5.0 V	75	12 V	115
EX_ADDR6	36	3.3 V	76	2.5 V	116
GND	37	5.0 V	77	12 V	117
GND	38	3.3 V	78	2.5 V	118
EX_ADDR9	39	5.0 V	79	12 V	119
EX_ADDR8	40	3.3 V	80	2.5 V	120

Legend	
power signals	purple
IXP4XX Network Processor extended expansion bus signals	green
GPIO signals	maroon
HSS0 signals (primary)	black
HSS1 signals (secondary)	red
not used (JTAG signals)	gray
interrupt signal	gold
RST_N	lavender

5.4.2.4 Stacking Interface Expansion Connector

The stacking interface expansion connector contains the extended expansion bus interface (IXP465-specific), GPIO, SPI, I^2C, ID, future needs, and power signals. Table 92 defines the stacking interface expansion connector signals. The Legend describing the color-codes for the signals follows the table.

Table 92. Stacking Interface Expansion Connector Signals (Sheet 1 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
1.8 V	1	C_PCI_4	41	3.3 V	81
1.8 V	2	C_PCI_5	42	3.3 V	82
GND	3	C_PCI_6	43	3.3 V	83
GND	4	C_PCI_7	44	3.3 V	84
EX_DATA17	5	C_PCI_8	45	GND	85
EX_DATA16	6	C_PCI_9	46	GND	86
EX_DATA19	7	EX_BE_N3	47	C_FN_59	87
EX_DATA18	8	EX_BE_N2	48	C_FN_60	88
GND	9	EX_BE_N1	49	C_FN_61	89
GND	10	EX_BE_N0	50	C_FN_62	90

Table 92. Stacking Interface Expansion Connector Signals (Sheet 2 of 2)

Signal	Pin #	Signal	Pin #	Signal	Pin #
EX_DATA21	11	EX_BURST	51	GND	91
EX_DATA20	12	EX_PAR3	52	GND	92
EX_DATA23	13	EX_PAR2	53	C_FN_63	93
EX_DATA22	14	EX_PAR1	54	GPIO5	94
GND	15	EX_PAR0	55	GPIO6	95
GND	16	C_NPE_0	56	GPIO7	96
EX_DATA25	17	C_NPE_1	57	GND	97
EX_DATA24	18	C_NPE_2	58	GND	98
EX_DATA27	19	C_NPE_3	59	GPIO8	99
EX_DATA26	20	C_NPE_4	60	GPIO9	100
GND	21	C_NPE_5	61	GPIO10	101
GND	22	C_NPE_6	62	GPIO11	102
EX_DATA29	23	C_NPE_7	63	GND	103
EX_DATA28	24	C_NPE_8	64	GND	104
EX_DATA31	25	C_NPE_9	65	GPIO12	105
EX_DATA30	26	C_NPE_10	66	GPIO13	106
GND	27	C_NPE_11	67	GPIO14	107
GND	28	C_NPE_12	68	GPIO15	108
EX_ADDR24	29	CLK32_OUT	69	GND	109
SSPS_CLK	30	C_FN_48	70	GND	110
SSPS_FRM	31	C_FN_49	71	-	111
SSPS_TXD	32	C_FN_50	72	ID0	112
SSPS_RXD	33	C_FN_51	73	ID1	113
SSPS_EXTCLK	34	C_FN_52	74	ID2	114
5.0 V	35	C_FN_53	75	ID3	115
5.0 V	36	C_FN_54	76	ID4	116
C_PCI_0	37	C_FN_55	77	ID5	117
C_PCI_1	38	C_FN_56	78	ID6	118
C_PCI_2	39	C_FN_57	79	I2C_SDA	119
C_PCI_3	40	C_FN_58	80	I2C_SCL	120

Legend	
power signals	purple
expansion bus signals	green
common future needs expansion signals.	blue
dedicated future needs expansion signals (this card only)	black

Legend (Continued)	
SPI signals	red
I^2C signals)	gold
GPIO signals	maroon
ID signals	teal
not used	gray
CLK32_OUT pin 69 (one signal in group)	lavender

5.4.3 Quad T1/E1 Card Stacking

The IXDP465 platform design supports stacking up to two IXPFRM465 Quad T1/E1 mezzanine cards. The board ID accesses these two interfaces.

5.4.3.1 Board ID

Eight signals on the IXDP465 expansion interface connector define a unique address on each stacked HSS Quad T1/E1 mezzanine card. Since this connector does not exist on the IXDP425 development platform, a mechanism has been implemented on the Quad T1/E1 mezzanine card to emulate connection to the IXDP465 platform when the card is used on an IXDP425 platform.

The IXDP465 platform ties ID0 to ground, and ID7 - ID1 to 3.3 V. The Quad T1/E1 mezzanine card pulls down ID0 (using a 100 kΩ resistor) and pulls up ID7 - ID1 (using a 49.9 kΩ resistor) to function on the IXDP425 platform. The signals must be shifted from the IXDP465 interface expansion connector to the stacking interface expansion connector (i.e., IXDP465 ID6 - ID0 shifted to Stacking ID7- ID1, with the 100 kΩ pull-down on the next module up-the-chain filling in a logic low for ID0). Table 93 shows the unique IDs for each stacked HSS Quad T1/E1 mezzanine card.

Table 93. T1/E1 Unique Stacking IDs

Stacking Slot	ID7 - ID0
0	11111110
1	11111100
2	11111000
3	11110000
4	11100000
5	11000000
6	10000000
7	00000000

The IXDP465 expansion bus contains twenty-five address bits (**EX_ADDR24 - EX_ADDR0**). The expansion address signals **EX_ADDR23** through **EX_ADDR21** select one of two stacked modules. Table 94 shows the unique IDs along with the upper expansion bus address signals for each stacked Quad T1/E1 mezzanine card. These signals are used for expansion bus accesses.

Table 94. T1/E1 Unique Stacking IDs and Expansion Bus Addresses

Stacking Slot	ID7 - ID0	EX_ADDR23 - EX_ADDR21
0	11111110	000
1	11111100	001
2	11111000	010
3	11110000	011
4	11100000	100
5	11000000	101
6	10000000	110
7	00000000	111

Note: The IXP425 network processor on the IXDP425 development platform only uses 24 bits. **EX_ADDR24** does not exist, so for compatibility, it is not used on the Quad T1/E1 mezzanine card for address decode.

5.4.4 Quad T1/E1 Card CPLD

The CPLD on the IXPFRM465 Quad T1/E1 mezzanine card generates the PCM clocks, PCM frame synchronization pulses, oscillator enables, and board interrupt status. Table 95 shows the CPLD pin assignments.

Table 95. CPLD Pin Assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	-	26	1.8 V	51	3.3 V	76	EX_DATA3
2	CT_CLK	27	E1_T1_CLK	52	E1_CLK_EN	77	ID6
3	CPLD_TEST2	28	CPLD_TEST5	53	T1_CLK_EN	78	ID7
4	CPLD_TEST1	29	CPLD_TEST6	54	ID5	79	SSPS_RXD
5	3.3 V	30	BRSIG4	55	ID4	80	CLK32.768MHZ_EN
6	EX_ADDR0	31	GND	56	ID3	81	SSPS_EXTCLK
7	EX_ADDR1	32	BRSIG3	57	1.8 V	82	HSS_PRI_RXDATA
8	EX_ADDR2	33	BRSIG2	58	ID2	83	TDO
9	EX_ADDR3	34	BRSIG1	59	ID1	84	GND
10	EX_ADDR4	35	EX_WR_N	60	ID0	85	CMVFPB
11	EX_ADDR21	36	EX_RD_N	61	EX_DATA0	86	CMVFPC
12	EX_ADDR22	37	PIO	62	GND	87	MVBTD/CCSBRD
13	EX_ADDR23	38	3.3 V	63	EX_DATA1	88	3.3 V
14	HSS_PRI_RXCLK	39	I2C_SDA	64	EX_DATA2	89	E1_T1_CS_N
15	CPLD_TEST3	40	I2C_SCL	65	GPIO0	90	MVBRD
16	HSS_PRI_RXFRAME	41	BTSIG1	66	GPIO1	91	RSYNC
17	HSS_PRI_TXCLK	42	BTSIG2	67	GPIO2	92	E1_T1_INT_N
18	HSS_PRI_TXDATA	43	BTSIG3	68	GPIO3	93	EX_CS_N

Table 95. CPLD Pin Assignments (Sheet 2 of 2)

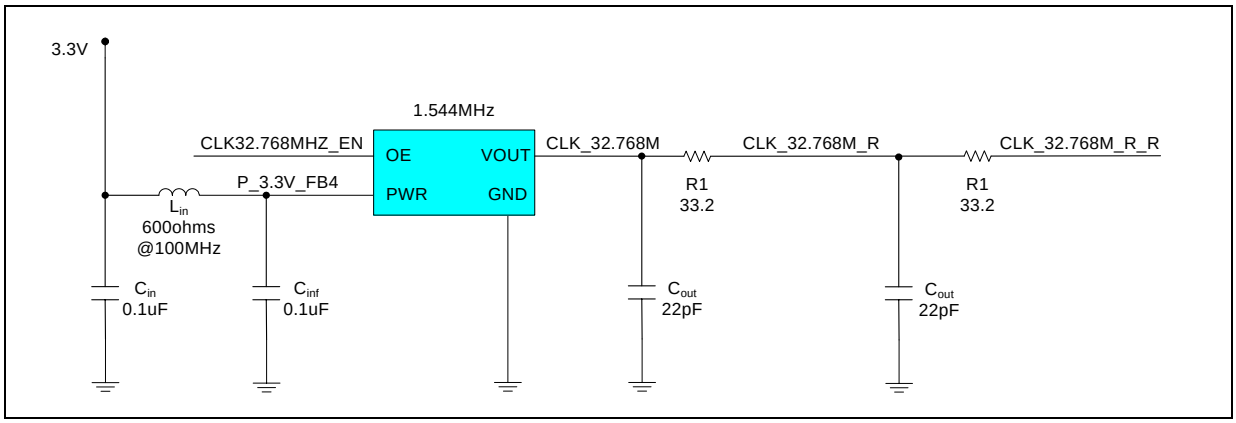
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
19	HSS_PRI_TXFRAME	44	BTSIG4	69	GND	94	HSS_INT_IN_N
20	3.3 V	45	TDI	70	GPIO4	95	CLK_32.768M_R_R
21	GND	46	CMV8MCLK	71	EX_DATA7	96	SSPS_FRM
22	EX_CLK	47	TMS	72	EX_DATA6	97	SSPS_TXD
23	SSPS_CLK	48	TCK	73	EX_DATA5	98	3.3 V
24	RST_N	49	CCSBTD	74	EX_DATA4	99	CPLD_TEST4
25	GND	50	HSS_INT_OUT_N	75	GND	100	GND

5.4.4.1 CPLD Clock

The input clock to the CPLD is a 32.768 MHz 50ppm oscillator. This oscillator provides the clocking for the TDM interface as well as the clock to the other T1/E1 cards in the chain. The oscillator is installed only when using the card in a standalone configuration or when the card is installed on the IXDP425 baseboard. The IXDP465 platform provides the 32.768 MHz clock through the IXDP465 interface expansion connector. Figure 38 shows the CPLD clock circuitry.

Note: Two jumpers, JP14 and JP15 are connected to the T1/E1 framer TDM interface pins. They are not currently used on the IXDP465 platform by default, but they are used for easy access to the TDM signals for debugging. JP14 connects the signals using the HMVIP mode of TDM on the framer and JP15 connects the signals to the backplane interface TDM mode of the framer. Since the IXP465 network processor supports only 32 ports of voice on each HSS port, HMVIP is the recommended mode of operation. No jumpers need to be installed in these locations for the Quad T1/E1 card to use this mode. See Figure 40 on page 153 for the jumper location.

Figure 38. TDM Interface External Clock Circuitry

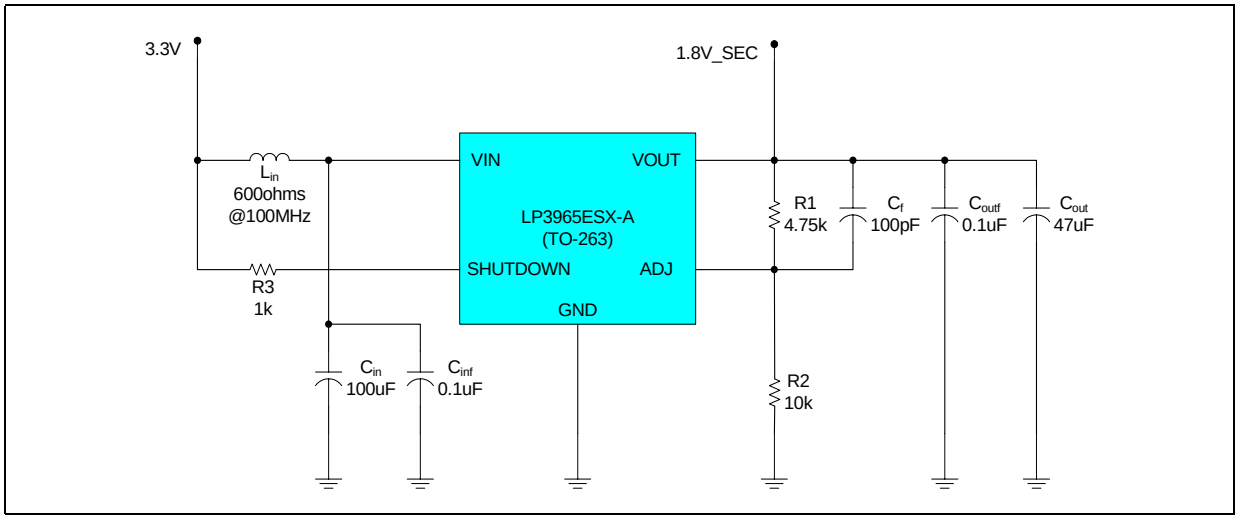


5.4.4.2 CPLD Core Voltage

The CPLD core voltage is generated by a 1.8 V linear regulator. The regulator is only installed when using a standalone configuration or when the card is installed on the IXDP425 baseboard. The IXDP465 platform provides the core voltage through the IXDP465 interface expansion connector. There is a jumper located on the Quad T1/E1 card that must be installed when using the

card standalone or on the IXDP425 development platform. This jumper (**JP13**) connects the signal **1.8V_SEC** to the 1.8 V signal. See Figure 40 for the location of this jumper. Figure 39 shows the core voltage regulator circuitry.

Figure 39. Quad T1/E1 Mezzanine Card CPLD Core Voltage Regulator



5.4.4.3 CPLD Voltage Filtering

The CPLD has two sources for input voltages. The bank power is supplied by the 3.3 V supply. Each power pin is decoupled with a 0.01 µF capacitor.

The CPLD core input voltage is powered by 1.8 V. Each 1.8 V power pin is decoupled with a 0.01 µF capacitor.

Table 96 lists the CPLD voltage pins that are filtered using the capacitor values.

Table 96. Quad T1/E1 Card CPLD Voltage Filtering

Pin	Signal
5	3.3 V
20	3.3 V
38	3.3 V
51	3.3 V
88	3.3 V
98	3.3 V
26	1.8 V
57	1.8 V

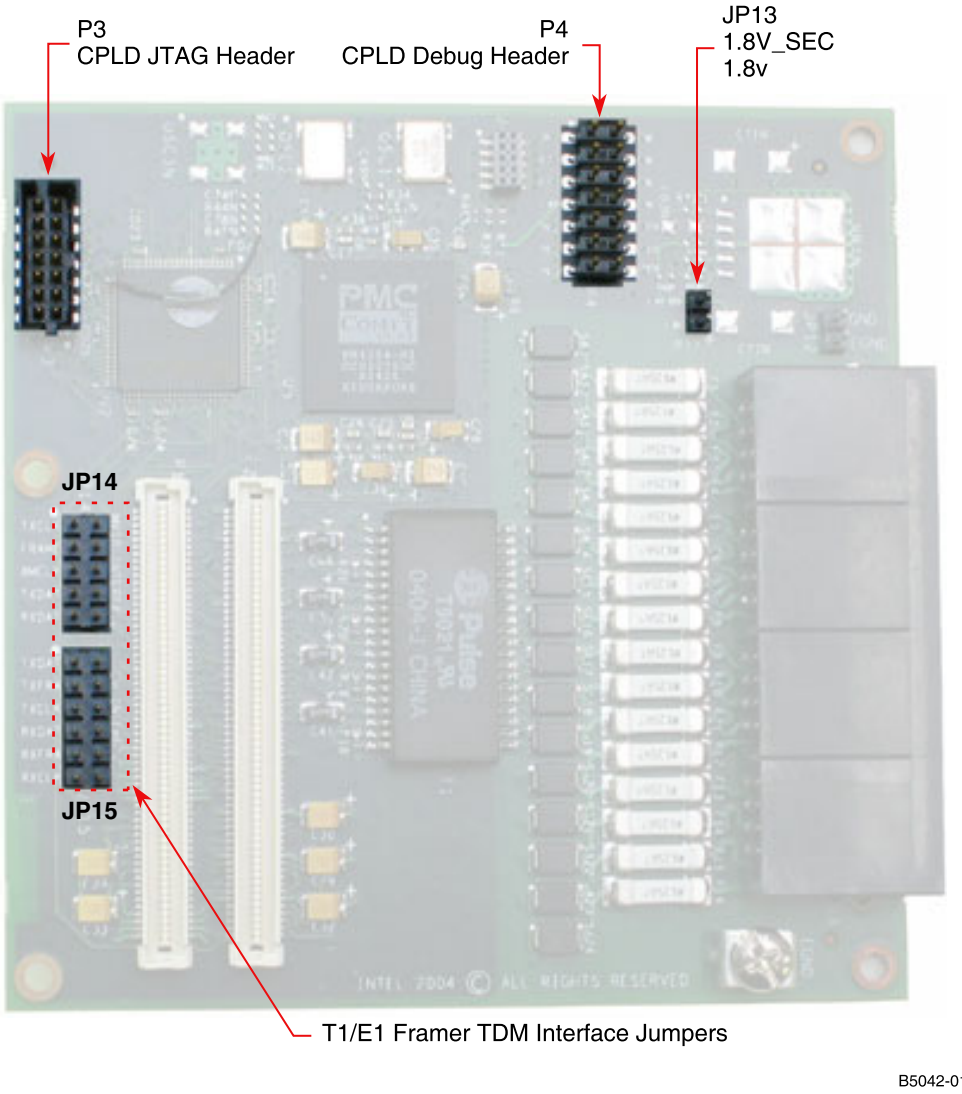
5.4.4.4 CPLD JTAG Interface

The CPLD JTAG interface consists of a 14-pin header (**P3**) for programming the CPLD. The connector uses the signals listed in Table 97. The CPLD signals **TMS** and **TDI** are pulled up to 3.3 V through a 10 kΩ resistor. The signal **TCK** has a 33.2 Ω series resistor and is also pulled up to 3.3 V through a 1 kΩ resistor. See Figure 40 for the JTAG connector location.

Table 97. Quad T1/E1 Card CPLD JTAG Interface Pin Assignments

Pin	Signal	Pin	Signal
1	GND	8	TDO
2	3.3 V	9	GND
3	GND	10	TDI
4	TMS	11	GND
5	GND	12	NC
6	TCK	13	GND
7	GND	14	NC

Figure 40. Quad T1/E1 Mezzanine Card Jumper and CPLD Header Locations



5.4.5 T1/E1 Interface

The IXPFRM465 Quad T1/E1 mezzanine card interface for the line signaling uses a PMC-Sierra* Framer/LIU (Quad Comet). The Framer/LIU device supports four (4) T1/E1 channels. The interfaces to the device are described in the following sections:

- Section 5.4.5.1, “Processor Interface”
- Section 5.4.5.2, “Line Interface”
- Section 5.4.5.3, “Power Interface”

- Section 5.4.5.4, “Clock Interface”
- Section 5.4.5.5, “Quad Port Transformer Interface”
- Section 5.4.5.6, “Protection Interface”
- Section 5.4.5.7, “RJ-45 Connector Interface”

5.4.5.1 Processor Interface

Table 98 lists the Framer/LIU processor interface pin definitions.

Table 98. Quad Framer Processor Interface Pin Assignments

Pin	Signal
B13	EX_ADDR0
A14	EX_ADDR1
B14	EX_ADDR2
A15	EX_ADDR3
B15	EX_ADDR4
A16	EX_ADDR5
B16	EX_ADDR6
C15	EX_ADDR7
C16	EX_ADDR8
D16	EX_ADDR9
D15	EX_ADDR10
B3	EX_DATA0
A2	EX_DATA1
A1	EX_DATA2
B1	EX_DATA3
C1	EX_DATA4
C2	EX_DATA5
D2	EX_DATA6
D3	EX_DATA7
D14	EX_RD_N
E15	EX_WR_N
E16	E1_T1_CS_N
E14	EX_ALE
E13	RST_N
F15	E1_T1_INT_N

5.4.5.2 Line Interface

Table 99 defines the Quad Framer line interface pin definitions.

Table 99. Quad Framer Line Interface Pin Assignments

Pin	Signal	Pin	Signal
C7	RXTIP1	P7	RXTIP3
A7	RXRING1	T7	RXRING3
A8	RVREF1	T8	RVREF3
B4	TXTIP11/21	P4	TXTIP13/23
B6	TXTIP11/21	R6	TXTIP13/23
C5	TXCM1	P5	TXCM3
A3	XRING11/21	R4	XRING13/23
D5	XRING11/21	N5	XRING13/23
D10	RXTIP2	N10	RXTIP4
C10	RXRING2	P10	RXRING4
C9	RVREF2	P9	RVREF4
A13	TXTIP12/22	R13	TXTIP14/24
A11	TXTIP12/22	T11	TXTIP14/24
D12	TXCM2	N12	TXCM4
C13	XRING12/22	T13	XRING14/24
B11	XRING12/22	R11	XRING14/24

5.4.5.3 Power Interface

Table 100 lists the Quad Framer power interface pin definitions. Each 3.3 V and 2.5 V pin is filtered using a 0.01 µF capacitor. All other pins require special filtering as shown in Figure 41 through Figure 44.

Table 100. Quad Framer Power Interface Pin Assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal
C6	GND	H15	2.5 V
D11	GND	K15	2.5 V
P6	GND	M13	2.5 V
N11	GND	J16	2.5 V
C4	GND	H2	3.3 V
B12	GND	K14	3.3 V
N4	GND	C3	3.3 V
R12	GND	D4	3.3 V
B5	GND	K4	3.3 V
A12	GND	N2	3.3 V
R5	GND	G16	3.3 V
T12	GND	N14	3.3 V

Table 100. Quad Framer Power Interface Pin Assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal
N8	GND	A6	TAVD11
D7	GND	C11	TAVD12
A9	GND	T6	TAVD13
N7	GND	P11	TAVD14
R9	GND	A4,A5	TAVD21_TAVD31
D6	GND	D13,C12	TAVD22_TAVD32
B10	GND	T4,T5	TAVD23_TAVD33
N6	GND	P13,P12	TAVD24_TAVD34
R10	GND	N9	CAVD
D9	GND	B8,B7	RAVD11_RAVD21
T14	GND	B9,A10	RAVD12_RAVD22
G1	2.5 V	R8,R7	RAVD13_RAVD23
H3	2.5 V	T9,T10	RAVD14_RAVD24
J1	2.5 V	C8	QAVD1
L1	2.5 V	R14	QAVD1

Figure 41. Transmit Analog Power Decoupling 1

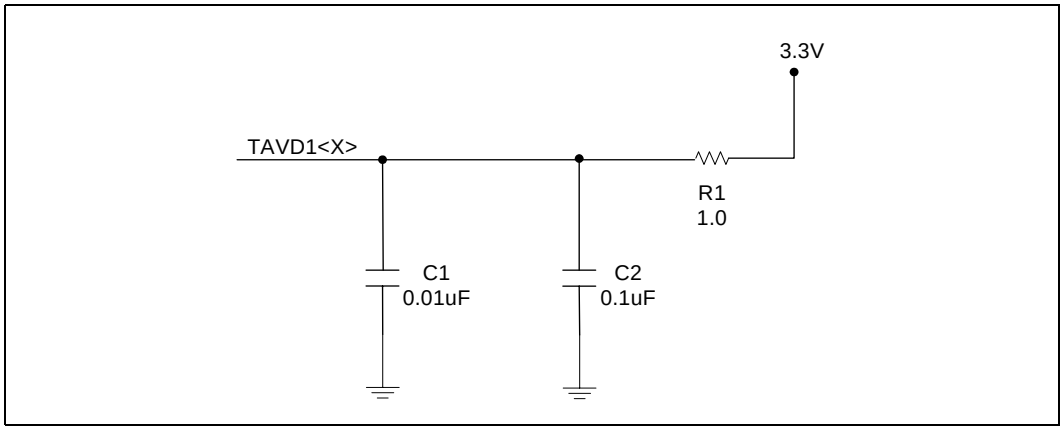


Figure 42. Receive Analog Power Decoupling 1 and 2

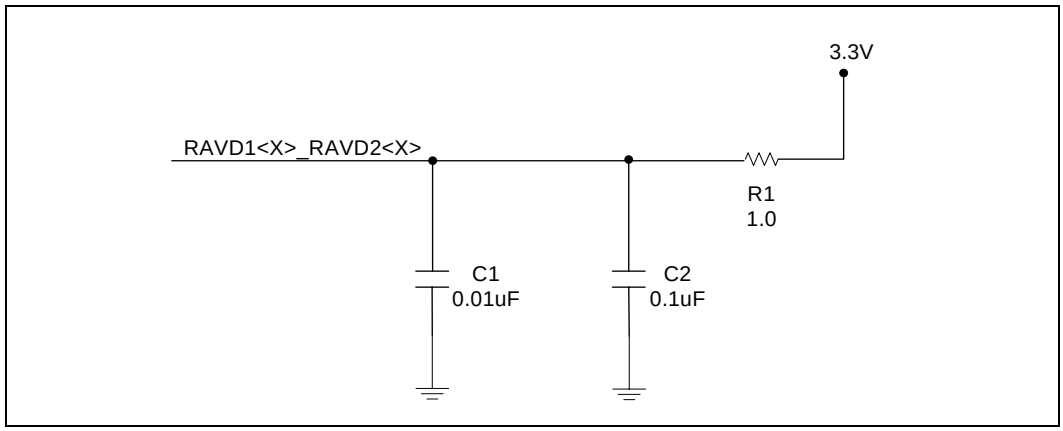


Figure 43. Transmit Analog Power Decoupling 2 and 3

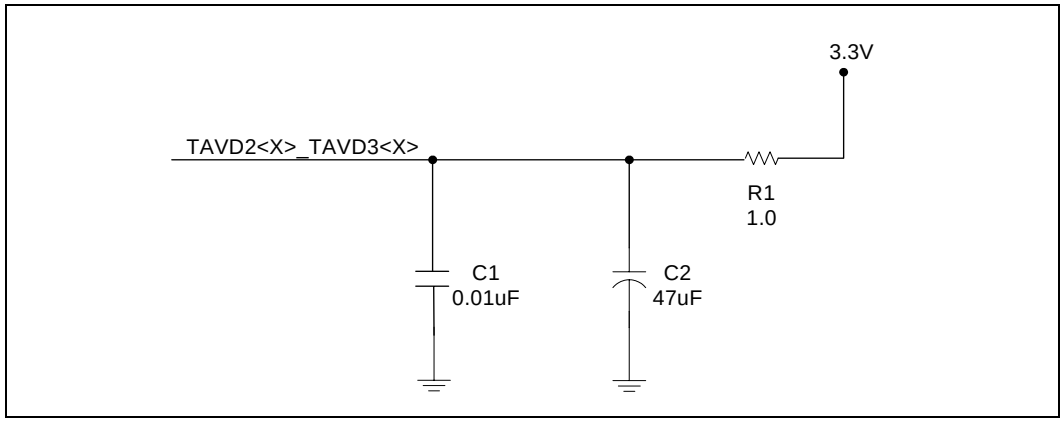
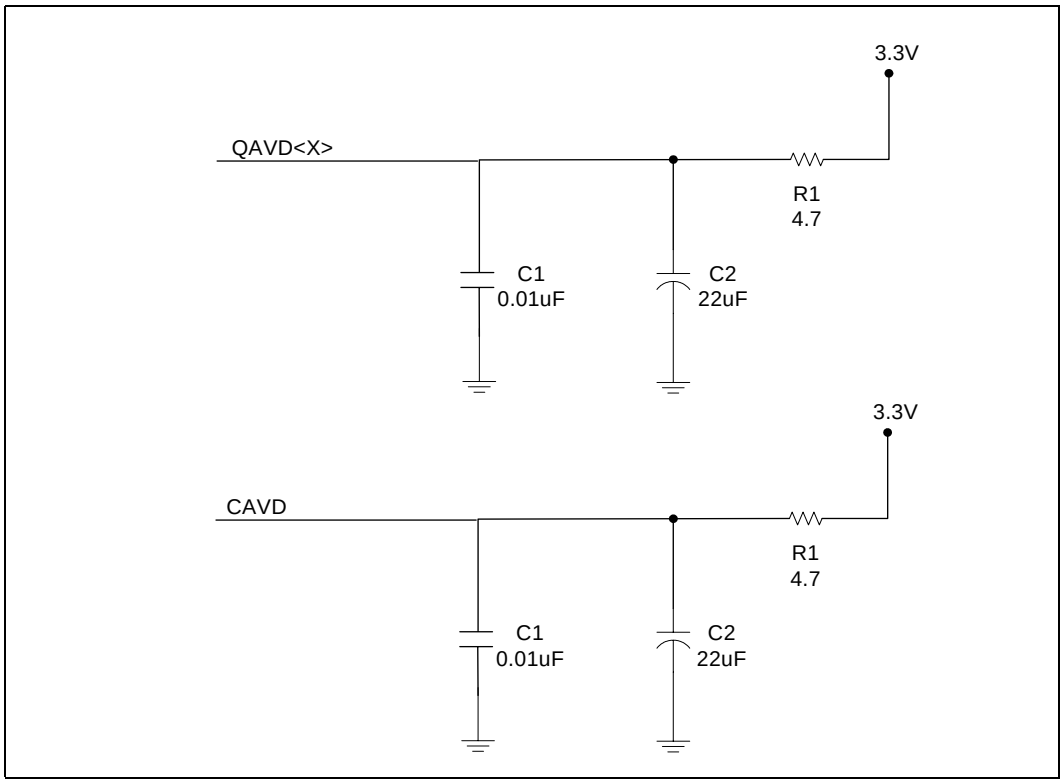


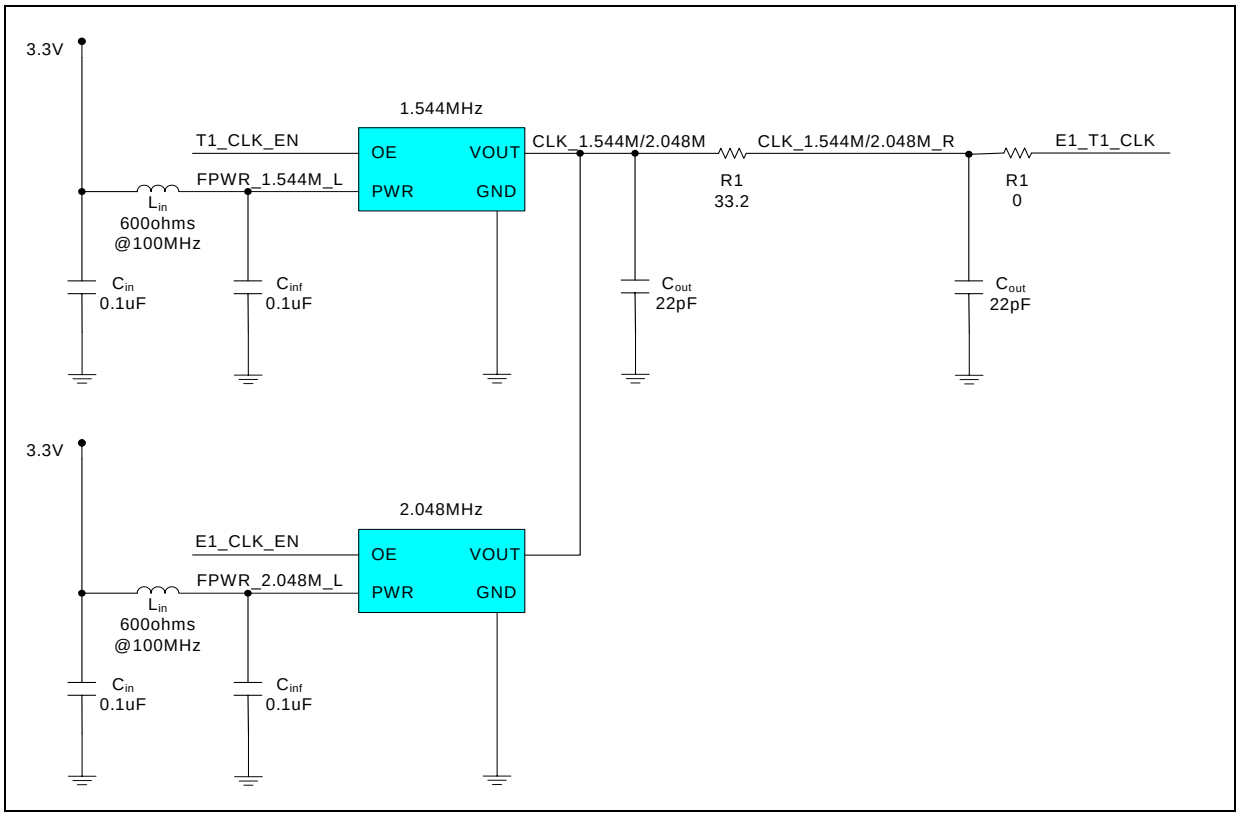
Figure 44. Quiet Analog Power Decoupling



5.4.5.4 Clock Interface

The Comet Quad Framer/LIU is designed to operate in either T1 or E1 mode. A 1.544 MHz oscillator circuit is the interface to the Quad Framer device clock input for T1 operation. A 2.048 MHz oscillator circuit is the interface to the Quad Framer clock input for E1 operation. The oscillator enable pins are software-controlled to allow for easy switching between T1 and E1 modes of operation. Figure 45 represents the circuitry required for the T1/E1 clock input.

Figure 45. T1/E1 Input Clock Circuitry



5.4.5.5 Quad Port Transformer Interface

The Quad T1/E1 mezzanine card interface to the line signaling on the PMC-Sierra* Framer/LIU is through a quad port transformer. The transformer provides IC-side protection on each channel to suppress low voltage transients. Table 101 defines the transformer interface pin definitions.

Table 101. Quad Port Transformer Interface Pin Assignments (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	TXTIP14/24	21	RXRING1_T
2	3.3 V	22	RXTIP1_T
3	XRING14/24	23	XRING11/21_T
4	RXTIP4	24	NC
5	RXRING4	25	TXTIP11/21_T
6	TXTIP13/23	26	RXRING2_T
7	GND	27	RXTIP2_T
8	XRING13/23	28	XRING12/22_T
9	RXTIP3	29	NC
10	RXRING3	30	TXTIP12/22_T
11	TXTIP12/22	31	RXRING3_T

Table 101. Quad Port Transformer Interface Pin Assignments (Sheet 2 of 2)

Pin	Signal	Pin	Signal
12	3.3 V	32	RXTIP3_T
13	XRING12/22	33	XRING13/23_T
14	RXTIP2	34	NC
15	RXRING2	35	TXTIP13/23_T
16	TXTIP11/21	36	RXRING4_T
17	GND	37	RXTIP4_T
18	XRING11/21	38	XRING14/24_T
19	RXTIP1	39	NC
20	RXRING1	40	TXTIP14/24_T

5.4.5.6 Protection Interface

The Quad T1/E1 mezzanine card is designed to protect against over-voltage and over-current power surges from lightning strikes or AC power cross disturbances. The protection circuitry consists of four (4) fuses in conjunction with six (6) Teccor* SIDACtor* devices for each port. This combination satisfies the regulatory requirements. The fuses provide the over-current protection and the Teccor* SIDACtor* devices provide the over-voltage protection. Figure 46 represents the required analog interface circuitry for one channel. This circuitry must be repeated for the number of channels required. Figure 47 represents the required protection circuitry for one channel. This circuitry must be repeated for the number of channels required.

Figure 46. External Analog Interface Circuitry for One Channel

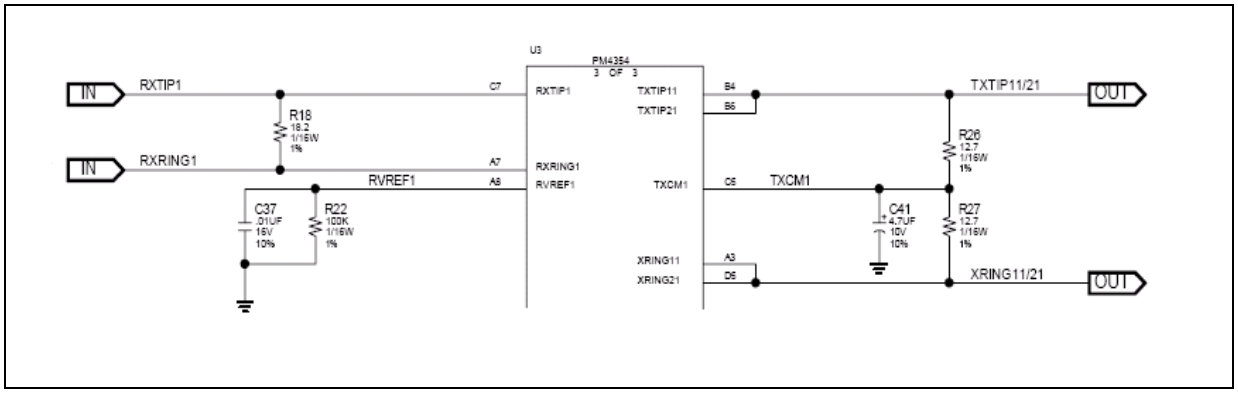
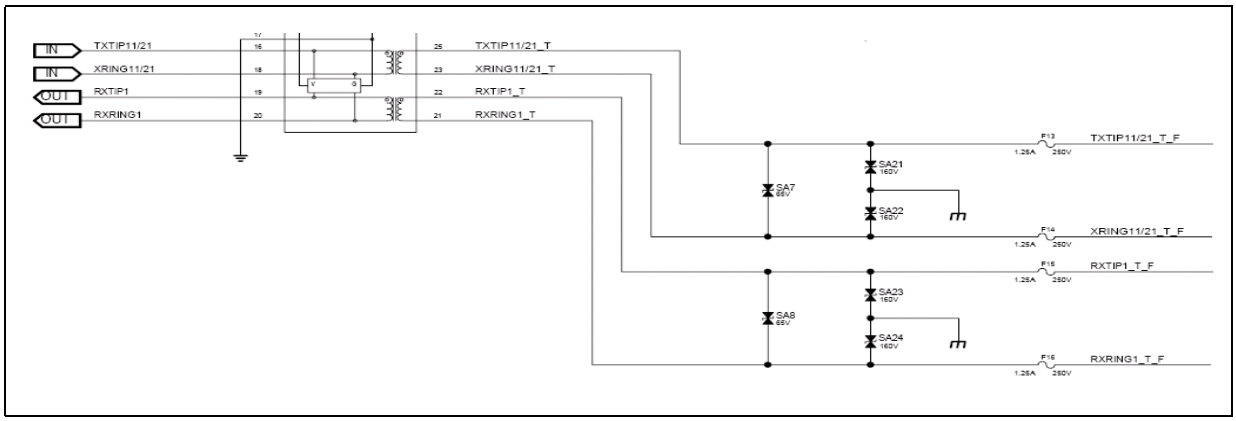


Figure 47. External Protection Circuitry for One Channel



5.4.5.7 RJ-45 Connector Interface

The Quad T1/E1 mezzanine card connects to the T1/E1 lines through an RJ-45 connector. This connector is a 4-port ganged jack. The housing is shielded for EMC compliance with only two (2) ground tabs on the connector. There are no ground tabs on the rear of the connector due to the creepage and clearance specifications that need to be met for compliance. Table 102 defines the pinout required on the RJ-45 jack.

Table 102. RJ-45 Connector Pin Assignments

Pin	Signal
1	RXRING(X)
2	RXTIP(X)
3	NC
4	TXRING(X)
5	TXTIP(X)
6	NC
7	NC
8	NC

Updating the IXDP465 Flash Memory A

RedBoot* is the primary boot loader and it is used to boot Linux*, plus some other sections of flash that are populated with bootrom (for VxWorks*). RedBoot is also used to update RedBoot.

Note: The IXDP465 platform ships with RedBoot v2.01 installed. It reports its version as follows:

```
RedBoot(tm) bootstrap and debug environment [ROM]
Red Hat certified release, version 2.01 - built 08:07:53, Feb 22 2005
Platform: IXDP465 Development Platform (XScale) BE
Copyright (C) 2000, 2001, 2002, 2003, 2004 Red Hat, Inc.
```

Once you have the IXDP465 platform running with your OS set up and running, you may want to organize the flash content for your particular design. Leaving the RedBoot image in place is recommended.

A host system connects through a network or serial port to provide the images. The procedures in this section assume that you have a host system set up to support loading images from a TFTP server. Host system setup and installation are beyond the scope of this document. For detailed information about using the RedBoot* v2.01 software and host system requirements, see the *Intel® IXP400 Software: RedBoot* v2.01 Software Release Notes*.

This appendix provides the following procedures needed to maintain the boot images in flash:

- Updating flash -- generic steps that apply to any bootloader or image to be placed into flash and made available at system Start Up to run.
- Creating a backup copy of RedBoot
- Using RedBoot to update RedBoot
- Using the Abatron* BDI2000 to load RedBoot

These procedures cover typical scenarios for using the IXDP465 platform.

Note: RedBoot commands entered at the RedBoot command prompt are prefaced with an “>” and appear in **boldface** type.

A.1 Generic Flash Updating Using RedBoot

1. Place the image to be loaded in the **tftp** root directory. On Linux, this is **`/tftpboot`**
2. Switch off the power to the board.
3. Verify that **JP127 /JP128** (labeled **A23** and **A24** on the PWB) are installed.

   For jumper location, see Figure 11, “Jumper Locations and Default Settings” on page 53.
4. Connect the board to the network and serial console.
5. Switch on the power to the board.

6. Boot to the RedBoot prompt:
   Press **^C** (Ctrl-C) if necessary to cancel the boot script execution.
   The default **fconfig** setting has no boot script.
7. Use the **fis list** command to view the existing flash partitions and their content.
   Selecting flash images to run is done using jumpers as described in Table 20, "Flash Sectioning" on page 40. The flash segments selected with the **JP127/JP128** jumpers and mapped to 0x00000000 at boot up are specified in Table 19, "IXDP465 Expansion Bus Address Mapping" on page 39.

Note: If you are updating an existing image that is in the FIS partition list, then you must unlock the partition before you can update it, using the command **`fis unlock <NAME>`**
If there was no previous image, then it is not possible to give NAME as an argument for the fis unlock command, so it is recommended to unlock it using the command
`fis unlock -f <FLASH-ADDRESS> -l <IMAGE LENGTH>`
When the update is complete, lock the partition using the command **`fis lock <NAME>`**. See Section A.3, "Using RedBoot to Update RedBoot" for an example.

8. Load the image into RAM using the RedBoot **load** command:

   > **`load -r -v -b 0x00100000 image.bin`**

9. Check the output of the **load** command for the image length.
   RedBoot reports this address range: `0x00100000-0x00181234`.

   The image length to store is **`0x00181234`** minus **`0x00100000`**.
   This value is used when storing the image to flash.

10. Use the **fis unlock** command to prevent the occurrence of an error report which states "Illegal command "Not a String" 0x25DB8"

    > **`fis unlock -f <FLASH-ADDRESS> -l <IMAGE_LENGTH>`**

11. Use the **fis create** command to store the image to flash.

    > **`fis create <IMAGE-NAME> -b 0x00100000 -l <IMAGE_LENGTH> -f <FLASH-ADDRESS> -e 0x00000000`**

Note: The **fis create** command is entered on a single line.

<**IMAGE-NAME**>, <**IMAGE-LENGTH**>, and <**FLASH_ADDRESS**> are placeholders for arguments that are required by the **fis create** command.

- <**IMAGE-NAME**>: the name that identifies the image in flash. A corresponding **load** command can use this name.
- <**IMAGE-LENGTH**>: the length in bytes of the image previously loaded into RAM. Use the length as determined in step 9.
- <I**MAGE-ADDRESS**>: the location in flash where the image will be written. If the image will be loaded at boot up by jumper selection, use the address specified in Table 20 on page 40.

  The flash addresses available to be mapped to 0x0 by the jumpers are:
  `0x50800000,0x51000000,0x51800000`
  Check the output of the **fis list** command to see which segments have been programmed as available.

A.2 Creating a Backup Copy of RedBoot

As a precaution before updating the primary RedBoot image, create a backup RedBoot image in flash. The backup version can be used in case there is a problem updating the primary RedBoot image and/or the new image fails to operate properly.

To load an additional copy of RedBoot into flash, follow these steps:

1. Verify that **JP127 /JP128** (labeled **A23** and **A24** on the PWB) are installed.

   For jumper location, see Figure 11, "Jumper Locations and Default Settings" on page 53.

2. Load the redboot_ROM.bin image into flash:

```
> load -r -v -b 0x00100000 redboot_ROM.bin
> fis create Redboot.bak -b 0x00100000 -l 0x0007A000 -f 0x51000000 -e
0x00000000
```

Note: The **fis create** command is entered on a single line.

3. Switch off the power to the board and remove the JP128 jumper.
4. Verify that RedBoot boots. The following information is displayed:

```
+... waiting for BOOTP information
Ethernet eth0: MAC address 00:07:e9:16:34:72
IP: 192.168.200.100/255.255.255.0, Gateway: 192.168.200.254
Default server: 192.168.200.254

RedBoot (tm) bootstrap and debug environment [ROM]
Red Hat certified release, version 2.01 - built 08:07:53, Feb 22 2005

Platform: IXDP465 Development Platform (XScale) BE
Copyright (C) 2000, 2001, 2002, 2003, 2004 Red Hat, Inc.

RAM: 0x00000000-0x08000000, [0x0002a488-0x07fd1000] available
FLASH: 0x50000000 - 0x52000000, 256 blocks of 0x00020000 bytes each.
== Executing boot script in 3.000 seconds - enter ^C to abort
```

Once you have verified that the RedBoot image is functional, you can update the primary image.

A.3 Using RedBoot to Update RedBoot

Note: RedBoot must execute from RAM to program the image into flash, since the primary RedBoot image runs from flash.

To update the primary image, follow these steps:

1. Load and execute **redboot_RAM.srec**:

```
> load -v redboot_RAM.srec
Using default protocol (TFTP)
Entry point: 0x00100040, address range: 0x00100000-0x001761d4

> go
```

```
... waiting for BOOTP information
Ethernet eth0: MAC address 00:07:e9:16:34:72
IP: 192.168.200.100/255.255.255.0, Gateway: 192.168.200.254
Default server: 192.168.200.254

RedBoot(tm) bootstrap and debug environment [RAM]
Red Hat certified release, version 2.01 - built 08:06:48, Feb 22 2005

Platform: IXDP465 Development Platform (XScale) BE
Copyright (C) 2000, 2001, 2002, 2003, 2004 Red Hat, Inc.

RAM: 0x00000000-0x08000000, [0x00196c68-0x07fd1000] available
FLASH: 0x50000000 - 0x52000000, 256 blocks of 0x00020000 bytes each.

== Executing boot script in 3.000 seconds - enter ^C to abort
```

2. Load the primary RedBoot image to overwrite the current image in flash:

```
> load -r -v -b 0x00200000 redboot_ROM.bin
Using default protocol (TFTP)
\
Raw file loaded 0x00200000-0x00278edb, assumed entry at 0x00200000
> fis unlock RedBoot
... Unlock from 0x50000000-0x50080000:....
> fis create RedBoot -b 0x00200000 -l 0x0007A000 -f 0x50000000 -e
0x00000000
An image named 'RedBoot' exists - continue (y/n)? y
... Erase from 0x50000000-0x50080000:....
... Program from 0x00200000-0x0027a000 at 0x50000000:....
... Unlock from 0x51fe0000-0x52000000: .
... Erase from 0x51fe0000-0x52000000: .
... Program from 0x07fe0000-0x08000000 at 0x51fe0000: .
... Lock from 0x51fe0000-0x52000000: .
> fis lock RedBoot
... Lock from 0x50000000-0x50080000: ....
```

Note: Since RedBoot is running from RAM up to 0x00196c68, the image must be placed above this address, at 0x00200000.

3. Reset the board by powering it off and on and verify that RedBoot starts up.

```
> +
Checking for SMII configuration...EthAcc: (Mac) cannot enable port 2,
MAC address not set
Initializing SMII for [NPE-B][NPE-C][NPE-A]...done.
Trying NPE-B...no PHY found
... waiting for BOOTP information
Ethernet eth0: MAC address 00:0e:0c:63:cd:cf
IP: 192.168.200.100/255.255.255.0, Gateway: 192.168.200.254
Default server: 192.168.200.254

RedBoot(tm) bootstrap and debug environment [ROM]
Red Hat certified release, version 2.01 - built 08:07:53, Feb 22 2005
```

```
Platform: IXDP465 Development Platform (XScale) BE
Copyright (C) 2000, 2001, 2002, 2003, 2004 Red Hat, Inc.

RAM: 0x00000000-0x08000000, [0x0002a488-0x07fd1000] available
FLASH: 0x50000000 - 0x52000000, 256 blocks of 0x00020000 bytes each.
Redboot>
```

4. Use the RedBoot **fis list** command to review the flash segment contents as known to RedBoot.

   Example

```
RedBoot> fis list
Name              FLASH addr  Mem addr    Length      Entry point
RedBoot           0x50000000  0x50000000  0x00080000  0x00000000
redboot.bak       0x50800000  0x50800000  0x00080000  0x00000000
FIS directory     0x51FE0000  0x51FE0000  0x0001F000  0x00000000
RedBoot config    0x51FFF000  0x51FFF000  0x00001000  0x00000000
```

A.4 Using an External Debugger to Update RedBoot

Refer to the Abatron* BDI2000 documentation for information about preparing to use the BDI2000 debugger. The following steps assume the default configuration:

- A TFTP server set up and running on your host system
- **redboot.bin** and the BDI2000 configuration files for your hardware in your default TFTP directory.

Use telnet to connect to the BDI2000 and program flash as follows:

```
update@myhost:~$ telnet bdi2000
Trying 192.168.200.100...
Connected to bdi2000.
Escape character is '^]'.
BDI Debugger for XScale (030918)
================================
Core#0> erase
Erasing flash at 0x50000000
Erasing flash at 0x50020000
Erasing flash at 0x50040000
Erasing flash at 0x50060000
Erasing flash at 0x50080000
Erasing flash passed
Core#0> prog redboot.bin BIN
Programming redboot.bin, please wait ....
Programming flash passed
Core#0> verify
Verifying redboot.bin, please wait ....
Verifying target memory passed
Core#0>
```