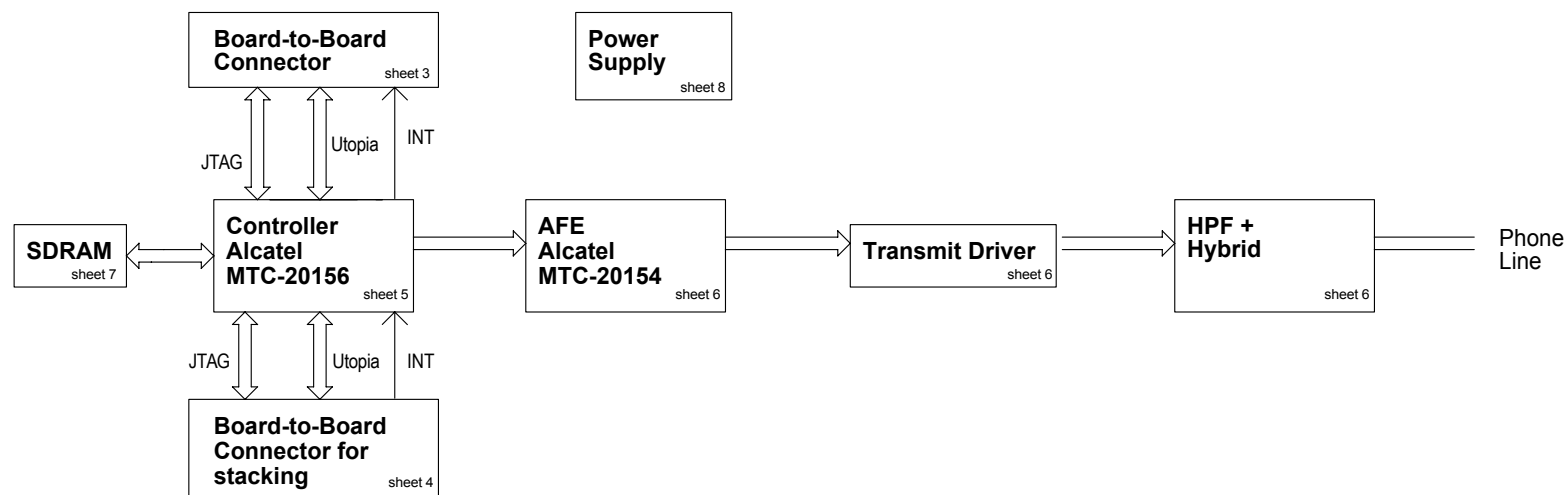



# ADSL ANNEX A PHY CARD

## for BIXMB425AD Network Processor Base Card



THIS SCHEMATIC IS PROVIDED 'AS IS' WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NONINFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE. Intel disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this specification. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

<b>Intel Corp</b> 2200 Mission College Blvd Santa Clara, CA 95052			
<b>Title</b> <b>BIXD110 ADSL ANNEX A PHY CARD</b>			
<b>Size</b> Custom	<b>Page Title</b>  Title Page / Block Diagram	<b>Rev</b> 1.0	
<b>Date:</b> Tuesday, June 04, 2002	<b>Sheet</b> 1     of     8		

SCHEMATIC ANNOTATIONS

VOLTAGE RAILS	
+12VIN	Provided from IXP425 baseboard.
+12V	Generated on module.
CPE_DRV_12VPOS	Derived from the +12V rail.
CO_DRV_12VPOS	Derived from the +12V rail.
+5V	Not used on this module. Provided from IXP425 baseboard.
+3V3	Provided by IXP425 baseboard.
20156_3V3	Derived from the +3V3 rail.
20154_A23V3	Derived from the +3V3 rail.
20154_D3V3	Derived from the +3V3 rail.
+2V5	Provided from IXP425 baseboard.
20156_2V5	Derived from the +2V5 rail.
-12V	Derived from the +3V3 rail.
CPE_DRV_12VNEG	Derived from the -12V rail.
CO_DRV_12VNEG	Derived from the -12V rail.
GROUNDS	
GND_DIGITAL	Digital Ground Plane (designated by "D" on ground symbol)
GND_ANALOG	Analog Ground Plane (designated by "A" on ground symbol)
GND_POWERSUPPLY	Power Supply Ground Plane (designated by "PSGND" near ground symbol)
SHIELD	Shield ground.
DESIGN NOTES	
0.0 ohm resistors are placed to allow accessibility to nodes that may be of interest.	
_DNP	Do Not Populate this component if this designation is found on component's schematic.

REVISION HISTORY


Rev 0.95	* Schematics for prototype build.
Rev 0.99	* Updated with a NMOS transistor and a pull up resistor on IO_WAIT signal
Rev 0.99	* Updated with an 0 ohm resistor on IO_WAIT signal

THIS SCHEMATIC IS PROVIDED 'AS IS' WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NONINFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE. Intel disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this specification. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

Intel Corp

2200 Mission College Blvd

Santa Clara, CA 95052



Title

BIXD110 ADSL ANNEX A PHY CARD

Size

Custom

Page Title

Schematic Notes

Rev

1.00

Date:

Tuesday, June 04, 2002

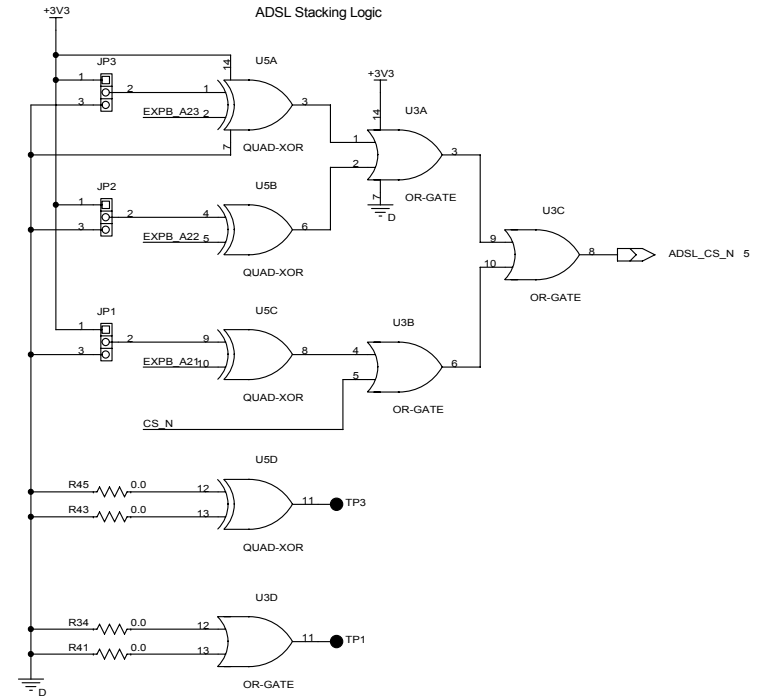
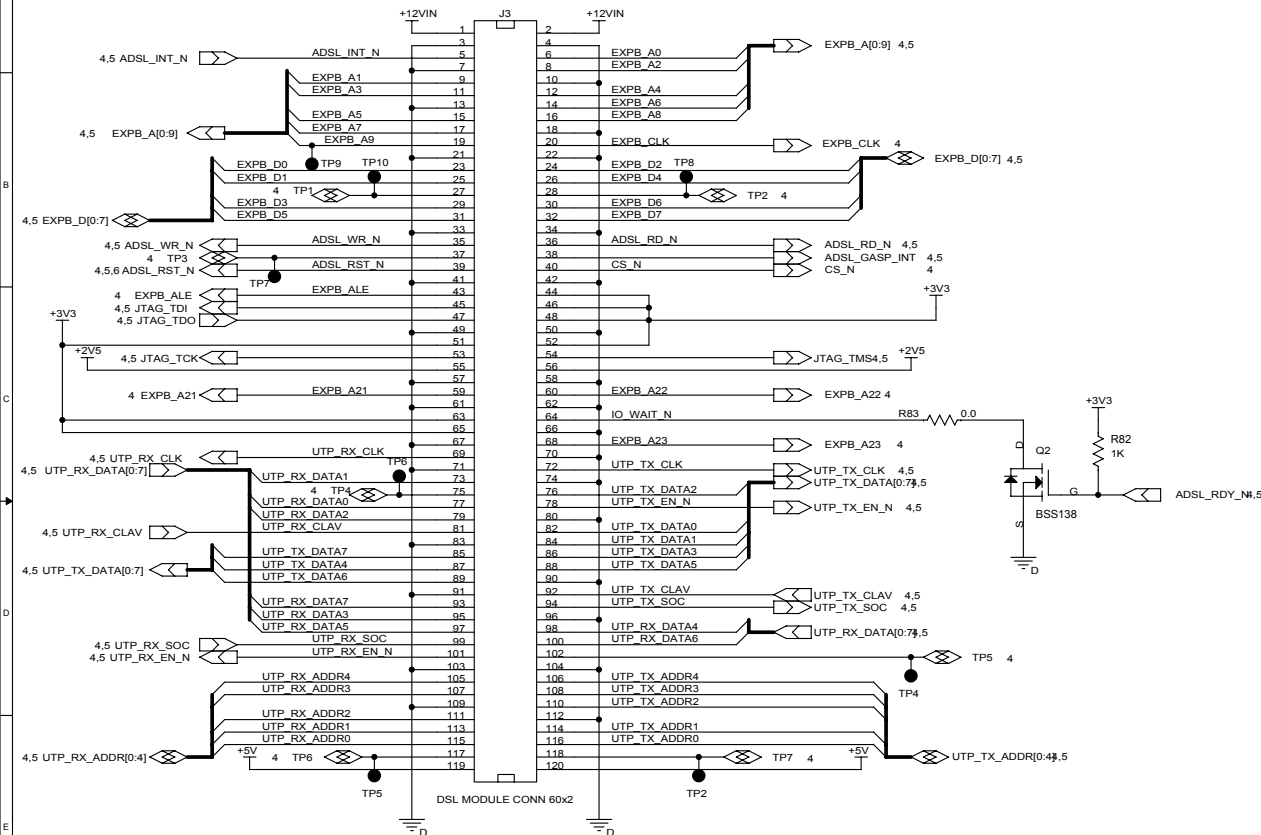
Sheet

2

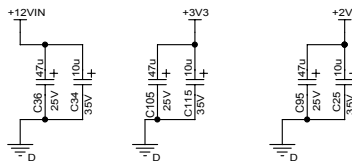
of


8

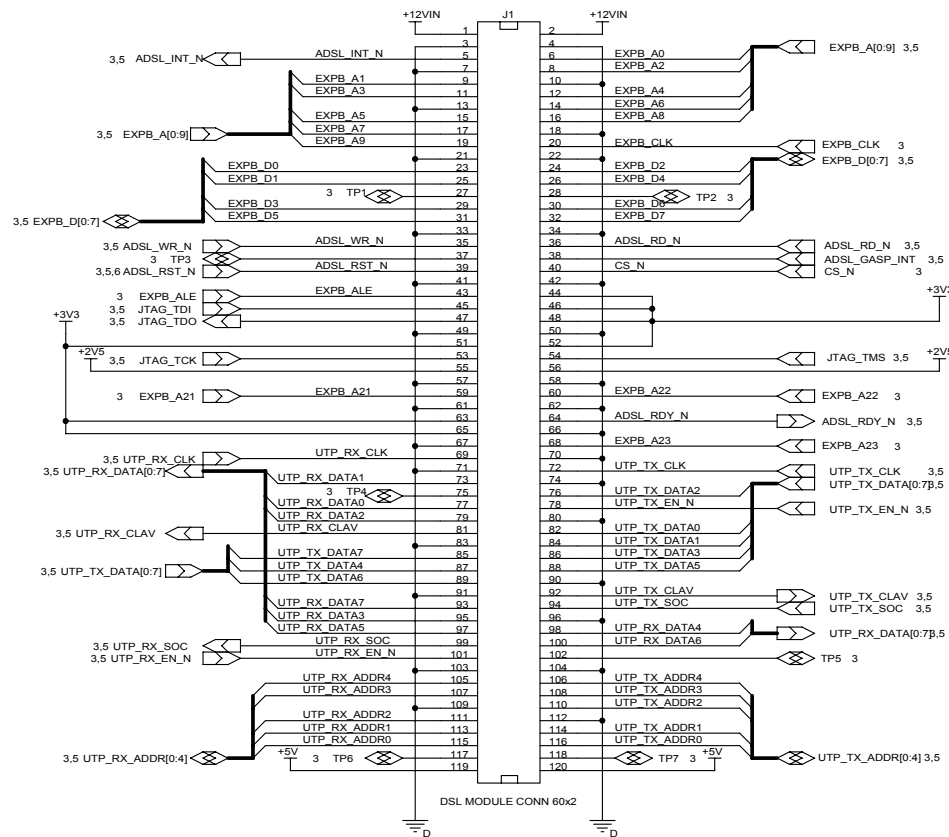
Note: Each stacked module will be in a different address space. Jumpers JP1,JP2,JP3 must have a different population scheme for each stacked module.




#### Decoupling

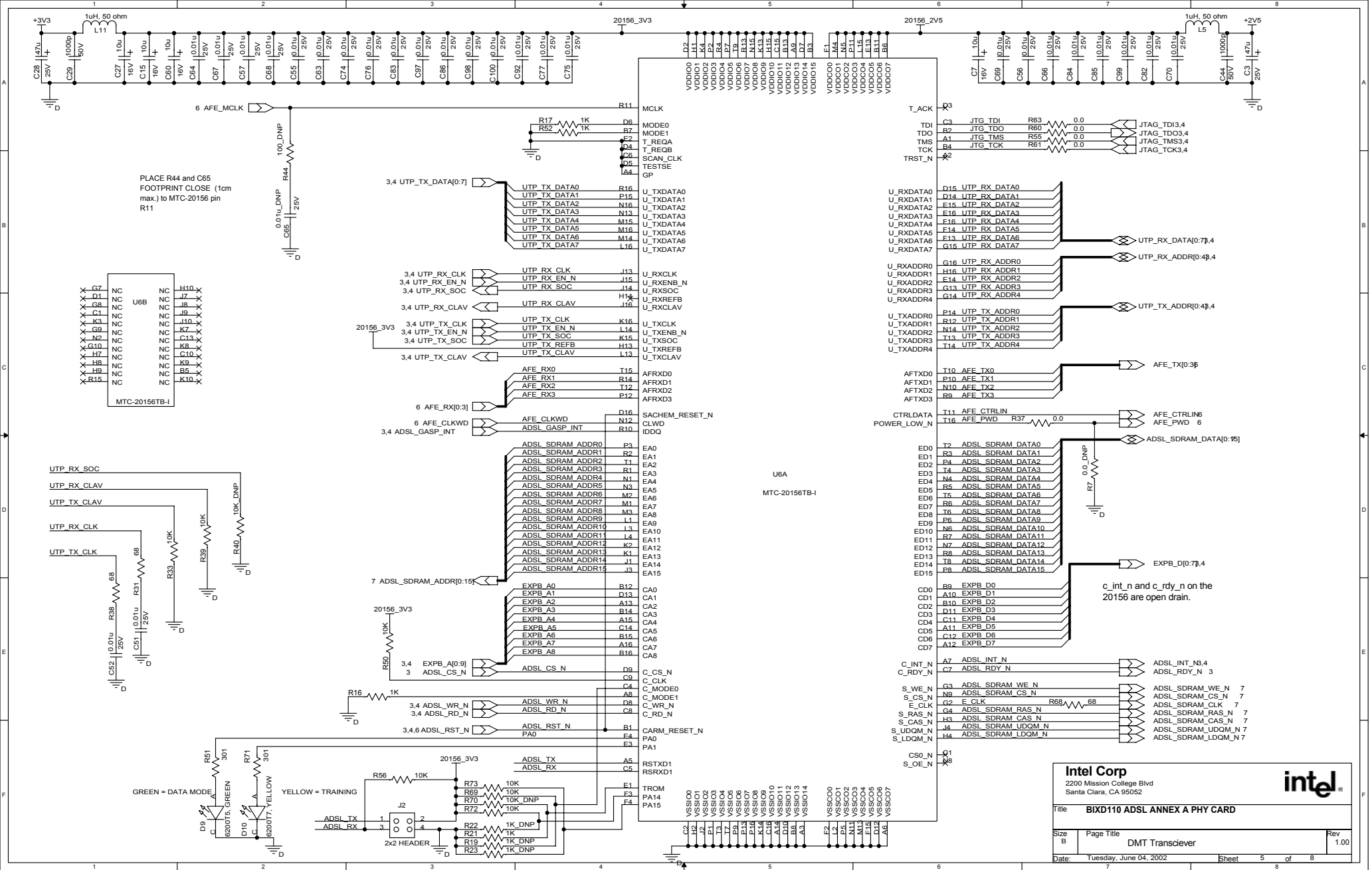


<b>Intel Corp</b> 2200 Mission College Blvd Santa Clara, CA 95052					
<b>Title</b> <b>BIXD110 ADSL ANNEX A PHY CARD</b>					
<b>Size Custom</b>	<b>Page Title</b>  Host Interface				<b>Rev</b>  1.00
<b>Date:</b>	Tuesday, June 04, 2002	<b>Sheet</b>	3	<b>of</b>	8

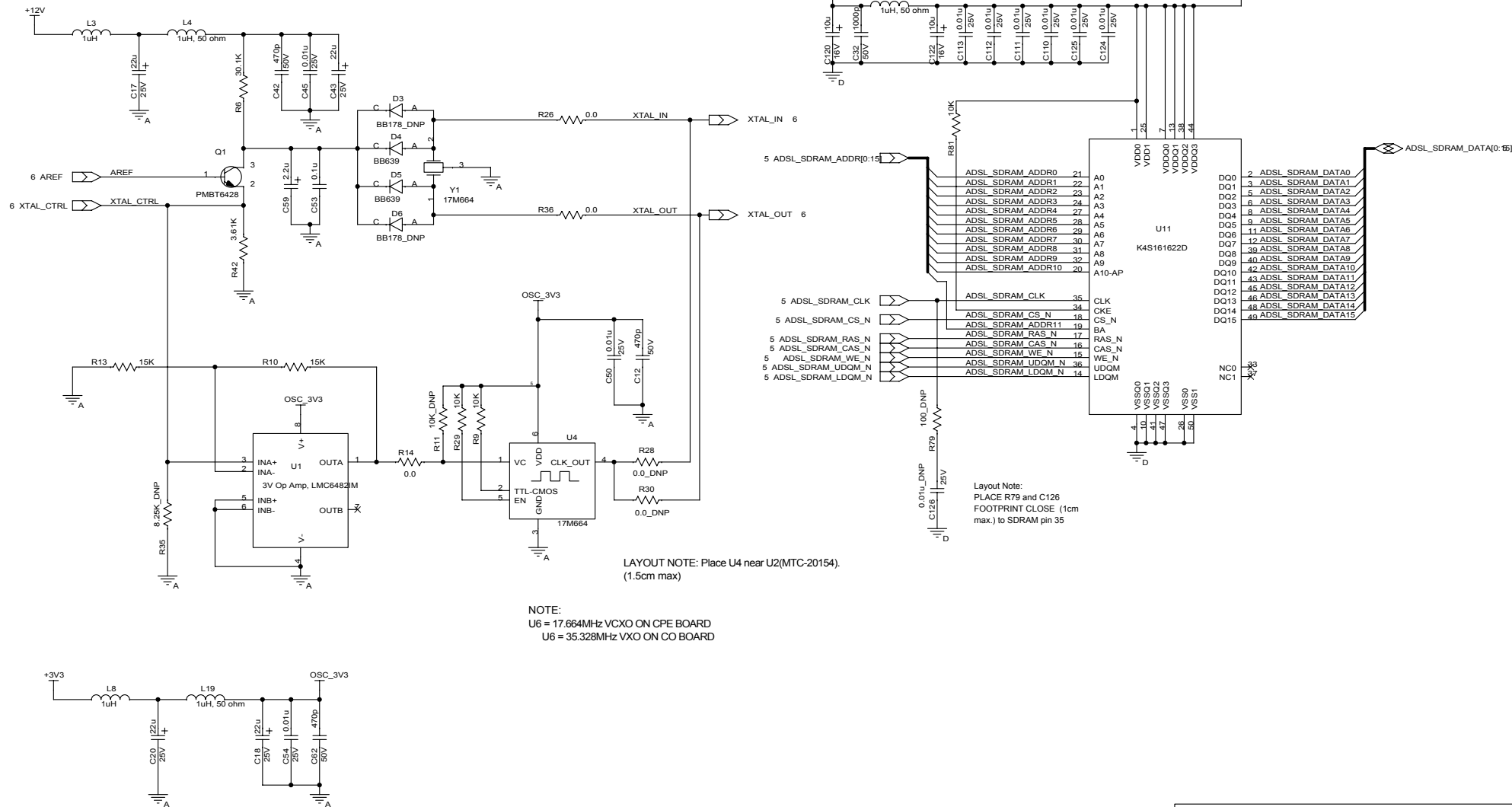


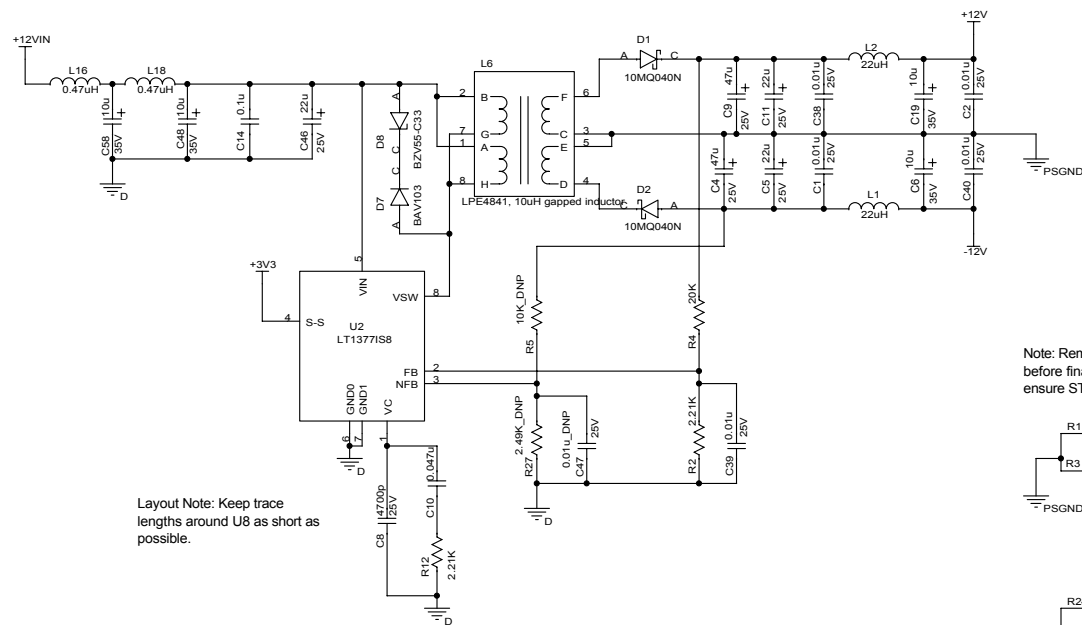
Note: This is the connector on the top side of the module. It is used to allow up to 4 Alcatel ADSL Modules to be stacked to enable multiple-channel use.

<b>Intel Corp</b> 2200 Mission College Blvd Santa Clara, CA 95052			
<b>Title</b> <b>BIXD110 ADSL ANNEX A PHY CARD</b>			
<b>Size</b> Custom	<b>Page Title</b>  Stackable Connector		<b>Rev</b> 1.00
<b>Date:</b>	Tuesday, June 04, 2002	<b>Sheet</b>	4 of 8





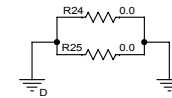
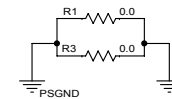




Layout Note: Keep trace lengths around U8 as short as possible.

Layout Note: Route "PSGND" net separately from "GND" net. "PSGND" net has to be a wide track, but not a plane.

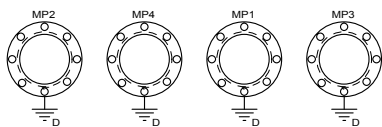
Note: Remove R1 and R3 before finalizing layout. These ensure STAR Distribution.



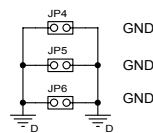
Note: R24 and R25 are the connection points from AGND to DGND.


Layout Note: Place both resistors side by side and add large copper bonding area to allow at least 5 vias.

The Grounded mounting holes, MP1-MP4, are to be placed in the four corners of the board.



Silkscreen:



<b>Intel Corp</b> 2200 Mission College Blvd Santa Clara, CA 95052			
Title <b>BIXD110 ADSL ANNEX A PHY CARD</b>			
Size B	Page Title <b>Power Supply</b>		Rev 1.0
Date:	Tuesday, June 04, 2002	Sheet 8 of 8	