DDR X16

SHEETS: 15 (BANK 0)
SHEETS: 16 (BANK 1)

POWER INDICATOR LEDS

SHEET 19

VOLTAGE REGULATION

SHEET 19

POWER FILTERS

SHEET 17,18

DDR TERM X16

SHEET 13,14

IXP46X

SHEETS: 4,5,6,7,9,10,11,12

EXPANSION BUS REGISTER CPLD

SHEET 8

CLOCK & RESET

SHEET 20

SIGNAL FILTERS

SHEET 14

BASEBOARD CONNECTORS

SHEETS:2,3

REFERENCE DESIGNATOR LEGEND
(REFDES MAX LENGTH 7 CHARACTERS)

CCCXW
- C = COMPONENT
  OSC = OSCILATOR
- X = REFDES NUMBER
  (0-9)
- W = WILDCARD (OPTIONAL)
  N=DNP

CCNXW
- C = COMPONENT
  RN = RESISTOR NETWORK
- N = REFDES NUMBER
  (0-9)
- X = REFDES NUMBER
  (0-9, A-Z)
- W = WILDCARD (OPTIONAL)
  N=DNP

CNXXW
- C = COMPONENT
  R = RESISTOR
- N = REFDES NUMBER
  (0-9)
- X = REFDES NUMBER
  (0-9, A-Z)
- W = WILDCARD (OPTIONAL)
  N=DNP

INTEL

GETZVILLE, NY 14068



| | | | |
|---|---|---|---|
| DRAWN_BY: K. Lewandowski | LOCAL PAGE: 1 OF 20 | TITLE: IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Tue May 03 16:58:01 2005 | DWG.#: C73145 / REV: 02 |

## PCI BUS INTERFACE CONNECTOR

C_PCI<9..0>
PCI_AD<31..0>
GPIO<15..0>
PCI_REQ_N<3..0>
PCI_GNT_N<3..0>
PCI_CBE_N<3..0>
UART_TXDATA<1..0>
UART_CTS_N<1..0>
UART_RXDATA<1..0>
UART_RTS_N<1..0>

J7
C_PCI<0>
USB_DPOS_R
USB_HPOS
USB_HPEN
GPIO<0>
PCI_INTA_N
PCI_REQ_N<1>
PCI_REQ_N<2>
PCI_REQ_N<3>
GPIO<2>
UART_TXDATA<0>
UART_CTS_N<0>
UART_TXDATA<1>
UART_CTS_N<1>
PCI_RST_N
PCI_GNT_N<0>
GPIO<5>
GPIO<6>
PCI_AD<30>
GND
PCI_AD<28>
PCI_AD<26>
GND
PCI_AD<24>
PCI_IDSEL
GND
PCI_AD<22>
PCI_AD<20>
GND
PCI_AD<18>
PCI_AD<16>
GND
PCI_FRAME_N
2.5V
PCI_TRDY_N
PCI_STOP_N
GPIO<8>
GND
GPIO<10>
GPIO<12>
PCI_PAR
PCI_AD<15>
GND
PCI_AD<13>
PCI_AD<11>
C_PCI<3>
PCI_AD<9>
GPIO<13>
GPIO<15>
PCI_CBE_N<0>
C_PCI<6>
PCI_AD<6>
PCI_AD<4>
C_PCI<8>
PCI_AD<2>
PCI_AD<0>
3.3V
3.3V

J7
C_PCI<1>
USB_DNEG_R
USB_HNEG
USB_HPWR
GPIO<1>
GND
PCI_GNT_N<1>
PCI_GNT_N<2>
PCI_GNT_N<3>
GPIO<3>
UART_RXDATA<0>
UART_RTS_N<0>
UART_RXDATA<1>
UART_RTS_N<1>
PCI_CLK
GPIO<4>
PCI_REQ_N<0>
GPIO<7>
PCI_AD<31>
PCI_AD<29>
GND
PCI_AD<27>
PCI_AD<25>
GND
PCI_CBE_N<3>
PCI_AD<23>
GND
PCI_AD<21>
PCI_AD<19>
GND
PCI_AD<17>
PCI_CBE_N<2>
2.5V
PCI_IRDY_N
PCI_DEVSEL_N
GND
GPIO<9>
PCI_PERR_N
GPIO<11>
PCI_SERR_N
GND
PCI_CBE_N<1>
PCI_AD<14>
C_PCI<2>
PCI_AD<12>
PCI_AD<10>
C_PCI<4>
GPIO<14>
C_PCI<5>
PCI_AD<8>
PCI_AD<7>
C_PCI<7>
PCI_AD<5>
PCI_AD<3>
C_PCI<9>
PCI_AD<1>
3.3V
3.3V

C293 22UF 10V 20%
C294 22UF 10V 20%

## EXPANSION BUS INTERFACE CONNECTOR

EX_BE_N<3..0>
EX_DATA<31..0>
EX_CS_N_R<7..0>
EX_PAR<3..0>
EX_RDY_N<3..0>
EX_ADDR<24..0>

J6
EX_ADDR<1>
EX_ADDR<3>
EX_ADDR<5>
EX_ADDR<7>
EX_ADDR<9>
EX_ADDR<11>
EX_ADDR<13>
EX_ADDR<15>
EX_ADDR<17>
EX_ADDR<19>
EX_ADDR<21>
EX_ADDR<23>
EX_WR_N_R
EX_CS_N_R<0>
EX_CS_N_R<2>
GND
EX_ALE_R
GND
EX_BURST
EX_RDY_N<0>
GND
EX_RDY_N<3>
EX_PAR<0>
GND
EX_PAR<3>
GND
2.5V
EX_CS_N_R<4>
EX_CS_N_R<6>
EX_DATA<0>
EX_DATA<2>
EX_DATA<4>
EX_DATA<6>
EX_DATA<8>
EX_DATA<10>
EX_DATA<12>
EX_DATA<14>
EX_DATA<16>
EX_DATA<18>
EX_DATA<20>
EX_DATA<22>
EX_DATA<24>
EX_DATA<26>
EX_DATA<28>
EX_DATA<30>
EX_BE_N<0>
EX_BE_N<2>
3.3V
3.3V

J6
EX_ADDR<0>
EX_ADDR<2>
EX_ADDR<4>
EX_ADDR<6>
EX_ADDR<8>
EX_ADDR<10>
EX_ADDR<12>
EX_ADDR<14>
EX_ADDR<16>
EX_ADDR<18>
EX_ADDR<20>
EX_ADDR<22>
EX_ADDR<24>
EX_RD_N_R
EX_CS_N_R<1>
EX_CS_N_R<3>
EX_CLK
GND
EX_IOWAIT_N
GND
EX_RDY_N<1>
EX_RDY_N<2>
GND
EX_PAR<1>
EX_PAR<2>
GND
2.5V
GND
EX_CS_N_R<5>
EX_CS_N_R<7>
EX_DATA<1>
EX_DATA<3>
EX_DATA<5>
EX_DATA<7>
EX_DATA<9>
EX_DATA<11>
EX_DATA<13>
EX_DATA<15>
EX_DATA<17>
EX_DATA<19>
EX_DATA<21>
EX_DATA<23>
EX_DATA<25>
EX_DATA<27>
EX_DATA<29>
EX_DATA<31>
EX_BE_N<1>
EX_BE_N<3>
3.3V
3.3V

C301 22UF 10V 20%
C302 22UF 10V 20%

INTEL
GETZVILLE, NY 14068



| | | | |
|---|---|---|---|
| DRAWN_BY: K. Lewandowski | LOCAL PAGE: 2 OF 20 | TITLE: IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Wed Jul 13 15:38:12 2005 | DWG.#: C73145 / REV: 02 |

NPE AND PERIPHERAL INTERFACE CONNECTOR

UTP_IP_ADDR<4..0>
ETHB_RXDATA<3..0>
ETHB_TXDATA_R<3..0>
UTP_IP_DATA<7..0>
UTP_OP_DATA<7..0>
ETHC_TXDATA_R<3..0>
ETHC_RXDATA<3..0>
UTP_OP_ADDR<4..0>
HSS_RXDATA<1..0>
HSS_TXCLK_R<1..0>
HSS_TXFRAME<1..0>
HSS_RXCLK_R<1..0>
HSS_RXFRAME<1..0>
HSS_TXDATA<1..0>

J8

HSS_TXDATA<0>
HSS_RXFRAME<0>
HSS_RXCLK_R<0>
HSS_TXDATA<1>
HSS_RXFRAME<1>
HSS_RXCLK_R<1>
UTP_OP_ADDR<1>
UTP_OP_ADDR<3>
ETH_MDC_R
ETHC_TXEN_R
ETHC_RXDATA<1>
ETHC_RXDATA<3>
ETHC_COL
ETHC_TXDATA_R<0>
ETHC_TXDATA_R<2>
GND
ETHC_RXCLK
UTP_OP_CLK
GND
UTP_OP_DATA<1>
UTP_OP_DATA<2>
GND
UTP_OP_DATA<5>
UTP_OP_DATA<6>
GND
UTP_IP_DATA<1>
UTP_IP_DATA<2>
GND
UTP_IP_DATA<5>
2.5V
UTP_IP_DATA<7>

ETHB_RXCLK
ETHB_TXDATA_R<0>
ETHB_TXDATA_R<2>
ETHB_TXEN_R
ETHB_RXDATA<1>
ETHB_RXDATA<3>
ETHB_COL
UTP_OP_FCO
UTP_OP_FCI
UTP_IP_SOC
UTP_IP_ADDR<0>
UTP_IP_ADDR<2>
UTP_IP_ADDR<4>
I2C_SCL
SSP_SFRM
SSP_RXD

3.3V
3.3V
3.3V
C295 22UF 10V 20%

J8

HSS_TXFRAME<0>
HSS_TXCLK_R<0>
HSS_RXDATA<0>
HSS_TXFRAME<1>
HSS_TXCLK_R<1>
HSS_RXDATA<1>
UTP_OP_ADDR<0>
UTP_OP_ADDR<2>
UTP_OP_ADDR<4>
ETH_MDIO
ETHC_RXDATA<0>
ETHC_RXDATA<2>
ETHC_RXDV
ETHC_CRS
ETHC_TXDATA_R<1>
ETHC_TXDATA_R<3>
ETHC_TXCLK
GND
UTP_IP_CLK
UTP_OP_DATA<0>
GND
UTP_OP_DATA<3>
UTP_OP_DATA<4>
GND
UTP_OP_DATA<7>
UTP_IP_DATA<0>
GND
UTP_IP_DATA<3>
UTP_IP_DATA<4>
2.5V
UTP_IP_DATA<6>

ETHB_TXCLK
GND
ETHB_TXDATA_R<1>
ETHB_TXDATA_R<3>
ETHB_RXDATA<0>
ETHB_RXDATA<2>
ETHB_RXDV
ETHB_CRS_R
UTP_OP_SOC
UTP_IP_FCO
UTP_IP_FCI
UTP_IP_ADDR<1>
UTP_IP_ADDR<3>
I2C_SDA
SSP_SCLK
SSP_TXD
SSP_EXTCLK

3.3V
3.3V
3.3V

2.5V
C296 22UF 10V 20%

MOUNTING HOLES

E1 E3
E2 E4

FUTURE EXPANSION INTERFACE CONNECTOR

EX_GNT_N<3..1>
EX_REQ_N<3..1>

J5

EX_REQ_N<3>
EX_REQ_N<2>
EX_REQ_N<1>
EX_REQ_GNT_N
EX_WAIT_N

J5

EX_GNT_N<3>
EX_GNT_N<2>
EX_GNT_N<1>
EX_GNT_REQ_N
EX_SLAVE_CS_N

GND
GND
GND
GND
GND
GND
GND
GND
GND

2.5V
2.5V
2.5V
C303 22UF 10V 20%

1.8V
1.8V
3.3V
3.3V
3.3V
C1 22UF 10V 20%

1.8V
1.8V
SYSRESET_N
3.3V
3.3V
3.3V
C304 22UF 10V 20%

# NPE/FUTURE BUS INTERFACE CONNECTOR

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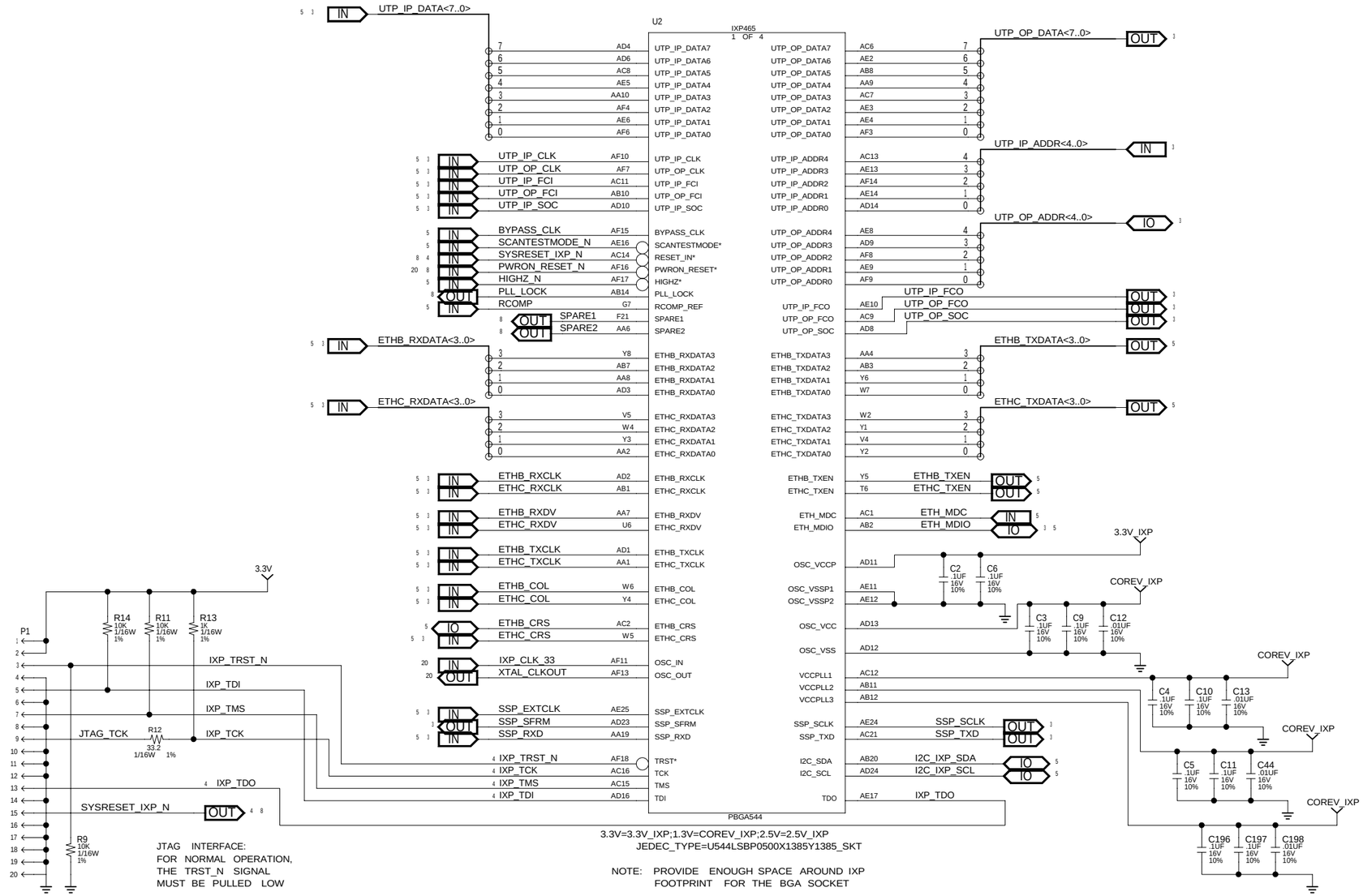
| DRAWN_BY: | LOCAL PAGE: | TITLE: | | |
|---|---|---|---|---|
| K. Lewandowski | 3 OF 20 | IXP46x Network Processor x16 Module | | |
| ENGINEER: | | DATE LAST MODIFIED: | DWG.#: | REV: |
| K.Lewandowski | | Wed Jul 13 15:38:14 2005 | C73145 | 02 |



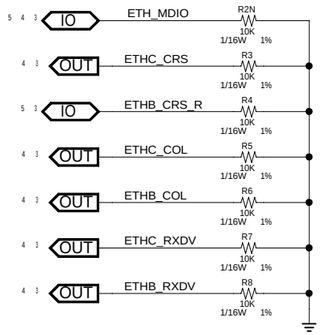

# MII/UTP/SPI/I2C/JTAG INTERFACES

INTEL
GETZVILLE, NY 14068

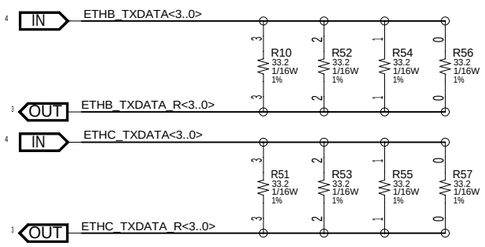


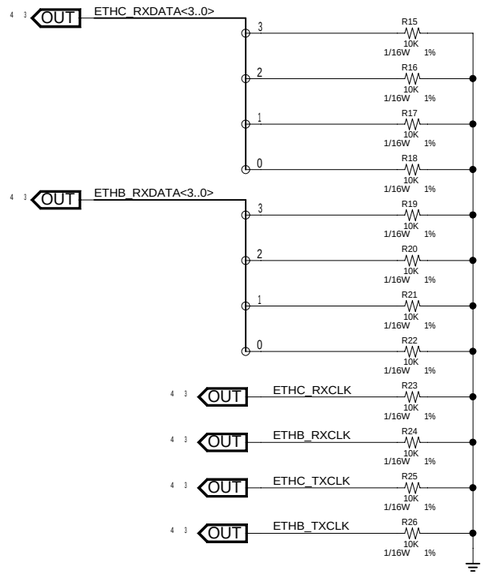
| | | | |
|---|---|---|---|
| DRAWN_BY: K. Lewandowski | LOCAL PAGE: 4 OF 20 | TITLE: IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Wed Jul 13 15:38:14 2005 | DWG.#: C73145 / REV: 02 |

ETHERNET NOTE:
10K PULL DOWN RESISTORS ARE REQUIRED ON THE FOLLOWING SIGNALS WHEN NOT BEING USED

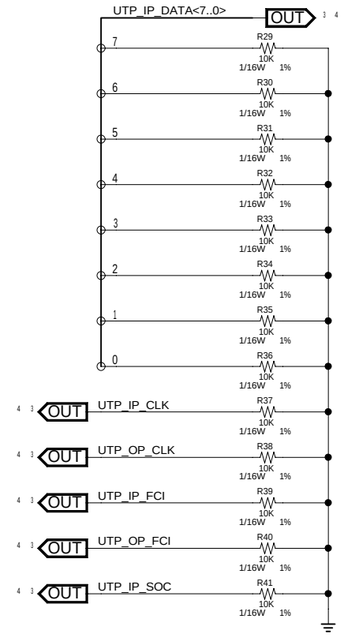



MII SERIES TERMINATION RECOMMENDED BY ETHERNET PHY MANUFACTURER

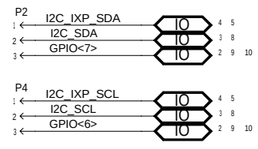


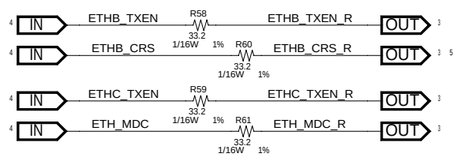




UTOPIA 2 NOTE:
10K PULL DOWN RESISTORS ARE REQUIRED ON THE FOLLOWING SIGNALS WHEN NOT BEING USED

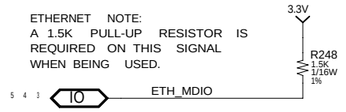



JUMPERS P2 AND P4 ALLOW EITHER GPIO OR IXP I2C INTERFACE TO BE USED FOR I2C

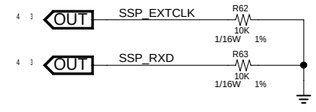


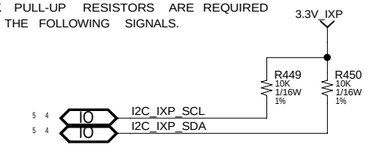

ETHERNET NOTE:
A 1.5K PULL-UP RESISTOR IS REQUIRED ON THIS SIGNAL WHEN BEING USED.



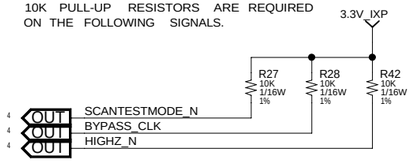

SSP NOTE:
10K PULL DOWN RESISTORS ARE REQUIRED ON THE FOLLOWING SIGNALS WHEN NOT BEING USED

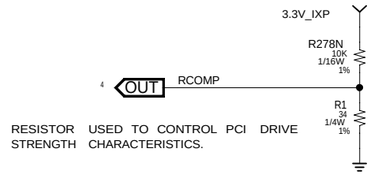



10K PULL-UP RESISTORS ARE REQUIRED ON THE FOLLOWING SIGNALS.




10K PULL-UP RESISTORS ARE REQUIRED ON THE FOLLOWING SIGNALS.



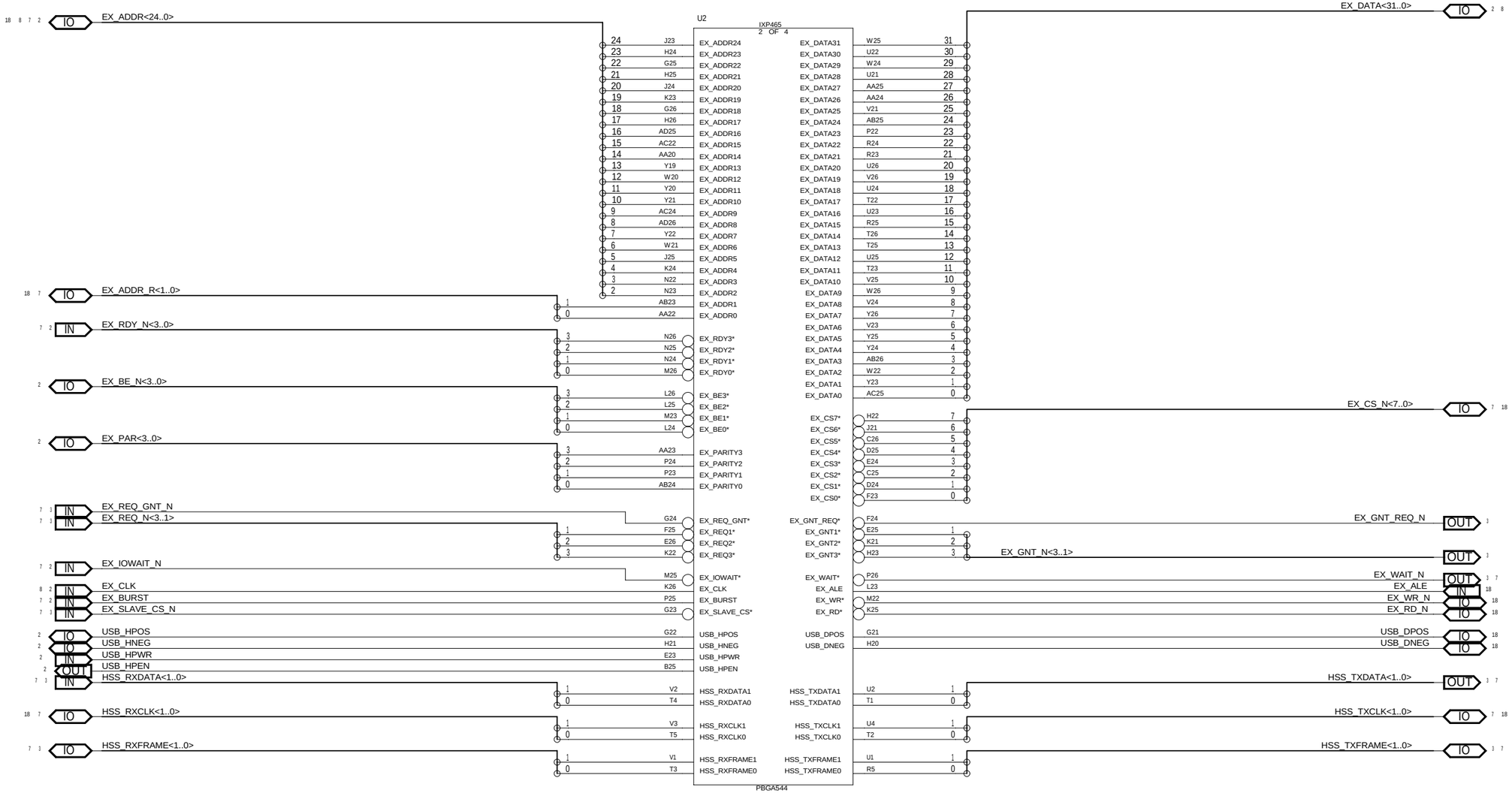

RESISTOR USED TO CONTROL PCI DRIVE STRENGTH CHARACTERISTICS.

# MII/UTP/SPI/I2C/JTAG INTERFACES

INTEL
GETZVILLE, NY 14068



| | | | |
|---|---|---|---|
| DRAWN_BY: K. Lewandowski | LOCAL PAGE: 5 OF 20 | TITLE: IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Wed Jul 13 15:38:15 2005 | DWG.#: C73145 / REV: 02 |




# EXPB, USB, HSS INTERFACE

INTEL
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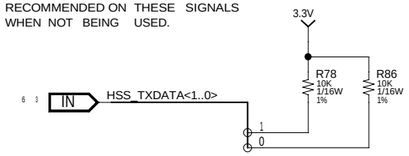
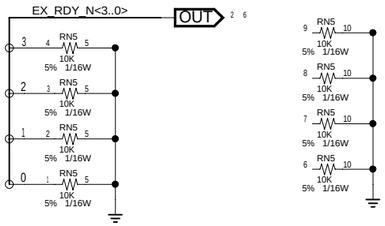
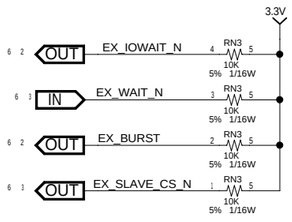
| | | | |
|---|---|---|---|
| DRAWN_BY: K. Lewandowski | LOCAL PAGE: 6 OF 20 | TITLE: IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Wed Jul 13 15:38:16 2005 | DWG.#: C73145 / REV: 02 |

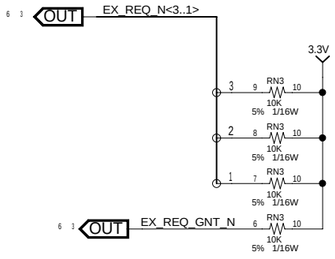
A 10K PULL-UP RESISTOR IS RECOMMENDED ON THESE SIGNALS WHEN NOT BEING USED.



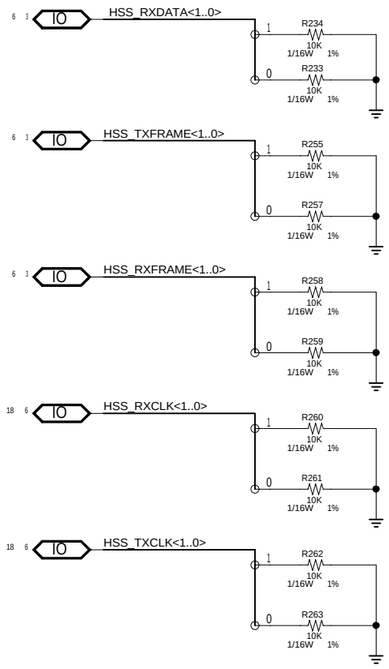

10K PULL-DOWN RESISTORS ARE RECOMMENDED ON THESE SIGNALS WHEN NOT BEING USED.

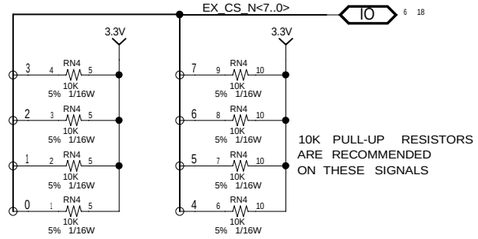


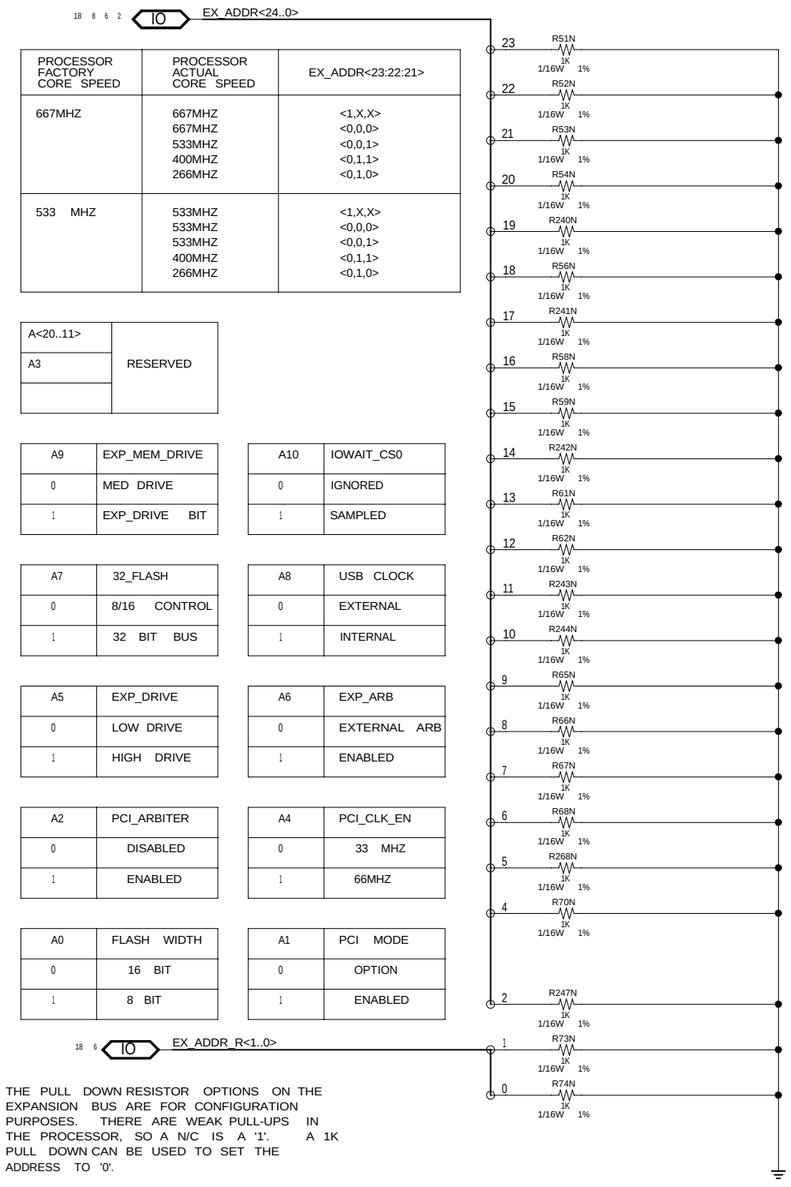




10K PULL DOWN RESISTORS ARE RECOMMENDED ON THESE SIGNALS WHEN NOT BEING USED.




10K PULL-UP RESISTORS ARE RECOMMENDED ON THESE SIGNALS




| PROCESSOR FACTORY CORE SPEED | PROCESSOR ACTUAL CORE SPEED | EX_ADDR<23:22:21> |
|---|---|---|
| 667MHZ | 667MHZ | <1,X,X> |
| | 667MHZ | <0,0,0> |
| | 533MHZ | <0,0,1> |
| | 400MHZ | <0,1,1> |
| | 266MHZ | <0,1,0> |
| 533 MHZ | 533MHZ | <1,X,X> |
| | 533MHZ | <0,0,0> |
| | 533MHZ | <0,0,1> |
| | 400MHZ | <0,1,1> |
| | 266MHZ | <0,1,0> |

| | |
|---|---|
| A<20..11> | RESERVED |
| A3 | |
| | |

| | |
|---|---|
| A9 | EXP_MEM_DRIVE |
| 0 | MED DRIVE |
| 1 | EXP_DRIVE BIT |

| | |
|---|---|
| A10 | IOWAIT_CS0 |
| 0 | IGNORED |
| 1 | SAMPLED |

| | |
|---|---|
| A7 | 32_FLASH |
| 0 | 8/16 CONTROL |
| 1 | 32 BIT BUS |

| | |
|---|---|
| A8 | USB CLOCK |
| 0 | EXTERNAL |
| 1 | INTERNAL |

| | |
|---|---|
| A5 | EXP_DRIVE |
| 0 | LOW DRIVE |
| 1 | HIGH DRIVE |

| | |
|---|---|
| A6 | EXP_ARB |
| 0 | EXTERNAL ARB |
| 1 | ENABLED |

| | |
|---|---|
| A2 | PCI_ARBITER |
| 0 | DISABLED |
| 1 | ENABLED |

| | |
|---|---|
| A4 | PCI_CLK_EN |
| 0 | 33 MHZ |
| 1 | 66MHZ |

| | |
|---|---|
| A0 | FLASH WIDTH |
| 0 | 16 BIT |
| 1 | 8 BIT |

| | |
|---|---|
| A1 | PCI MODE |
| 0 | OPTION |
| 1 | ENABLED |




THE PULL DOWN RESISTOR OPTIONS ON THE EXPANSION BUS ARE FOR CONFIGURATION PURPOSES. THERE ARE WEAK PULL-UPS IN THE PROCESSOR, SO A N/C IS A '1'. A 1K PULL DOWN CAN BE USED TO SET THE ADDRESS TO '0'.

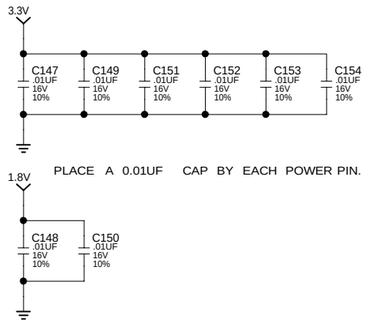
# EXPB, USB, HSS INTERFACE

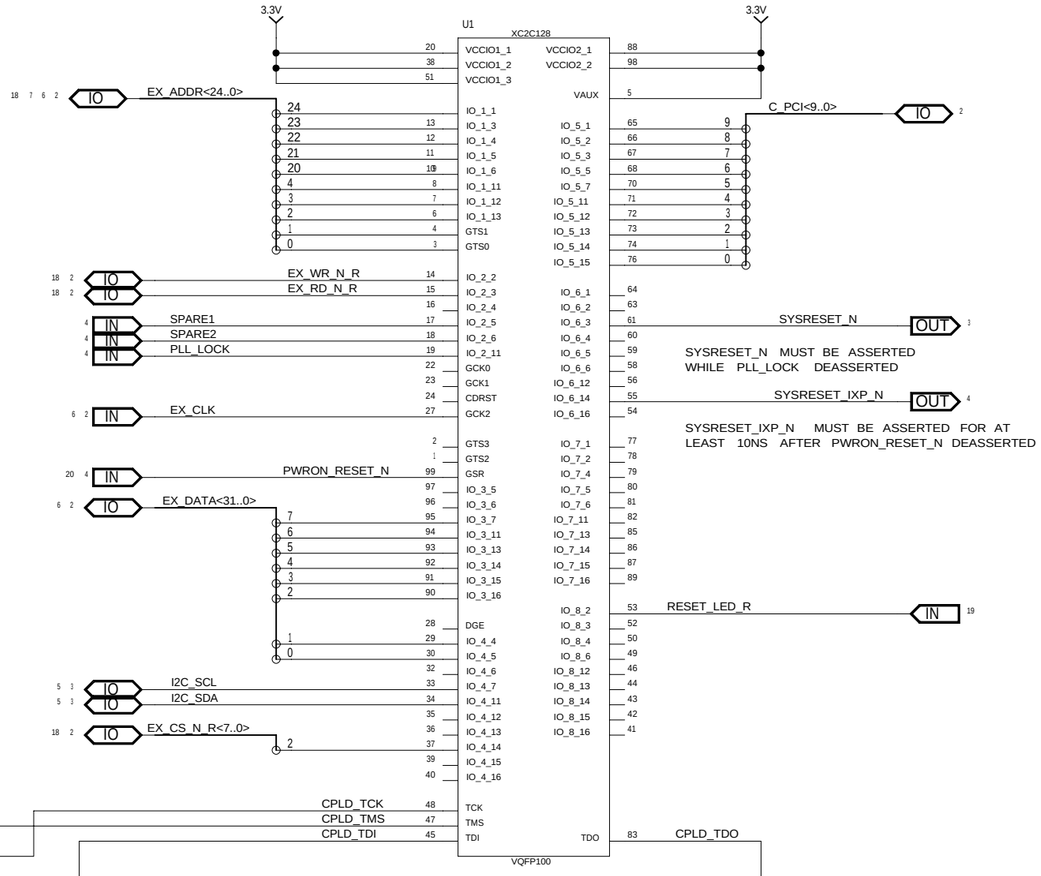
INTEL
GETZVILLE, NY 14068



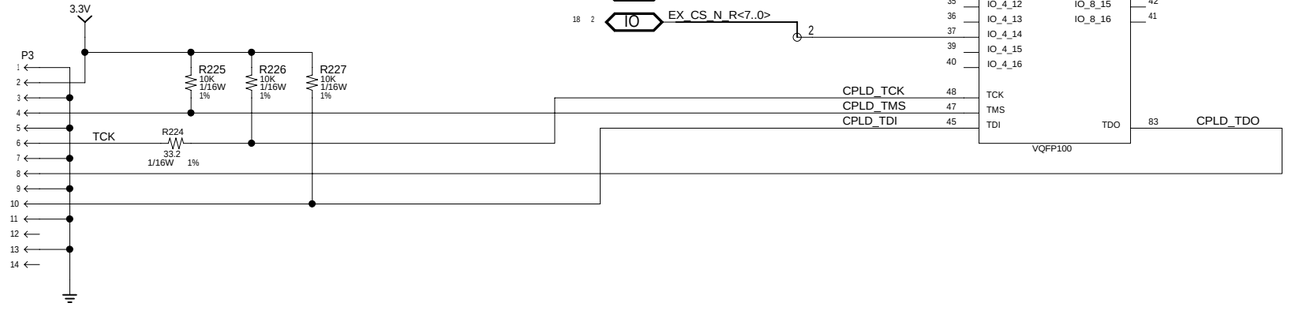
| | | | |
|---|---|---|---|
| DRAWN_BY: K. Lewandowski | LOCAL PAGE: 7 OF 20 | TITLE: IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Wed Jul 13 15:38:17 2005 | DWG.#: C73145 / REV: 02 |

| CAPACITOR | DEVICE | PIN |
|---|---|---|
| C147 | U1 | 5 |
| C149 | U1 | 20 |
| C151 | U1 | 38 |
| C152 | U1 | 51 |
| C153 | U1 | 88 |
| C154 | U1 | 98 |
| C148 | U1 | 26 |
| C150 | U1 | 57 |




CPLD JTAG INTERFACE CONNECTOR




# EXPANSION BUS CPLD REGISTERS

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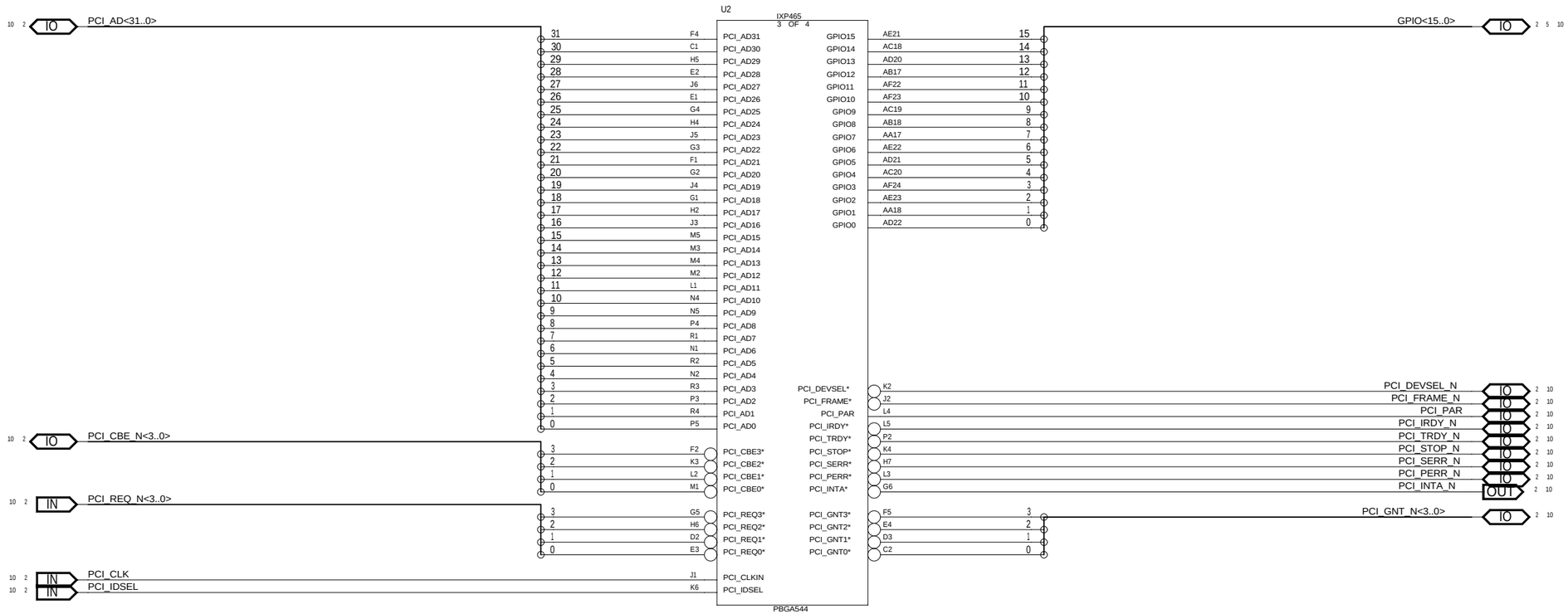
| DRAWN_BY: | LOCAL PAGE: | TITLE: | |
|---|---|---|---|
| K. Lewandowski | 8 OF 20 | IXP46x Network Processor x16 Module | |
| ENGINEER: | | DATE LAST MODIFIED: | DWG.#: / REV: |
| K.Lewandowski | | Wed Jul 13 15:38:17 2005 | C73145 / 02 |




3.3V=3.3V_IXP;1.3V=COREV_IXP;2.5V=2.5V_IXP
U544LSBP0500X1385Y1385_SKT

# PCI, GPIO INTERFACE

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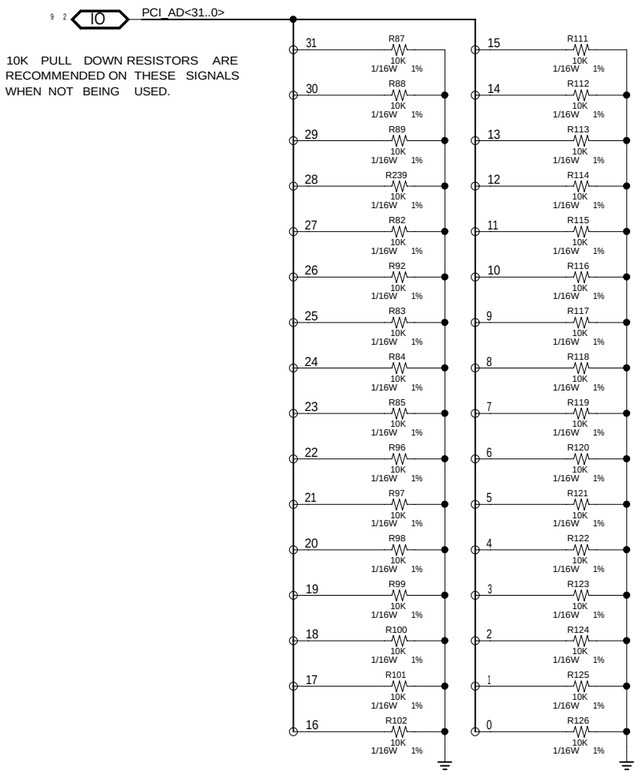
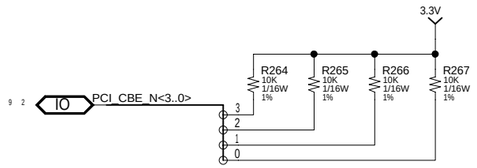
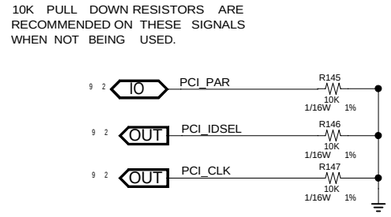
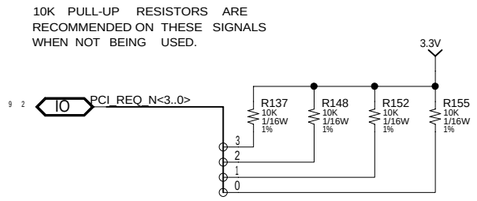
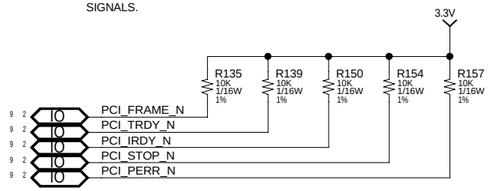
| | | | |
|---|---|---|---|
| DRAWN_BY: K. Lewandowski | LOCAL PAGE: 9 OF 20 | TITLE: IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Wed Jul 13 15:38:18 2005 | DWG.#: C73145 / REV: 02 |

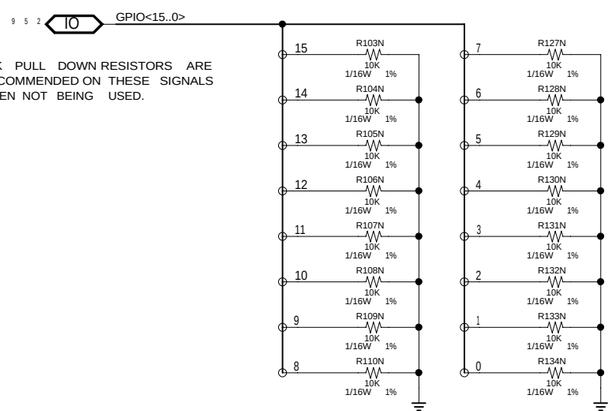


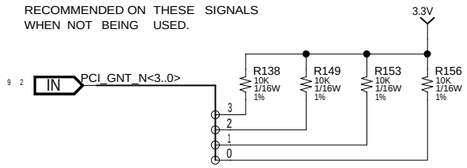



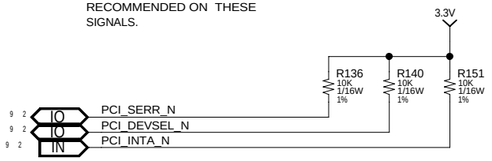




# PCI, GPIO INTERFACE

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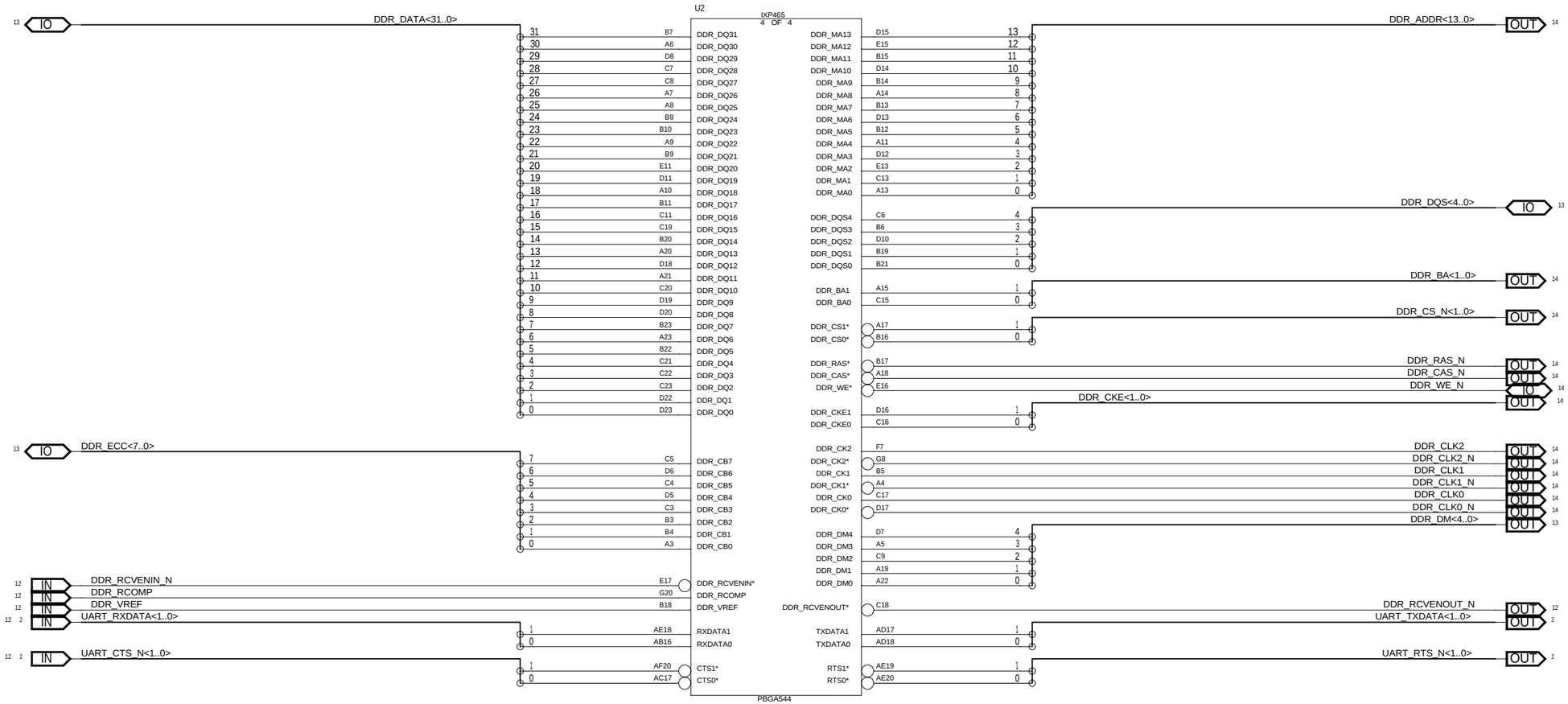
| DRAWN_BY: | LOCAL PAGE: | TITLE: | |
|---|---|---|---|
| K. Lewandowski | 10 OF 20 | IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Wed Jul 13 15:38:19 2005 | DWG.#: C73145 / REV: 02 |




3.3V=3.3V_IXP;1.3V=COREV_IXP;2.5V=2.5V_IXP
JEDEC_TYPE=U544LSBP0500X1385Y1385_SKT

# DDR, UART INTERFACES

| | | | | | |
|---|---|---|---|---|---|
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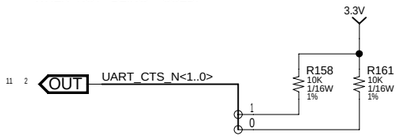
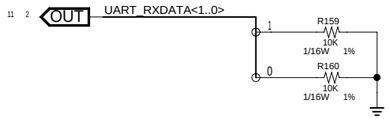
10K PULL-UP RESISTORS ARE RECOMMENDED ON THESE SIGNALS WHEN NOT BEING USED.

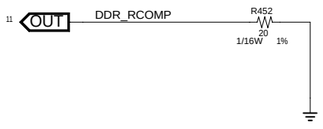



10K PULL DOWN RESISTORS ARE RECOMMENDED ON THESE SIGNALS WHEN NOT BEING USED.

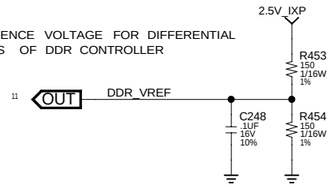



DDR_RCVENOUT_N MUST BE CONNECTED TO DDR_RCVENIN_N AND BE TRACE LENGTH MATCHED TO THE CLOCK TRACE PLUS THE AVERAGE DQ TRACE LENGTH


RESISTOR FOR PROCESS/TEMPERATURE ADJUSTMENTS




REFERENCE VOLTAGE FOR DIFFERENTIAL INPUTS OF DDR CONTROLLER




| DDR TECHNOLOGY | DDR ARRANGEMENT | NUMBER OF CHIPS WITH ECC | NUMBER OF BANKS | TOTAL MEMORY SIZE |
|---|---|---|---|---|
| 128 MBIT | 8M X 16<br>8M X 16 | 3<br>6 | 1<br>2 | 32 MBYTES<br>64 MBYTES |
| 256 MBIT | 16M X 16<br>16M X 16 | 3<br>6 | 1<br>2 | 64 MBYTES<br>128 MBYTES |
| 512 MBIT | 32M X 16<br>32M X 16 | 3<br>6 | 1<br>2 | 128 MBYTES<br>256 MBYTES |
| 1 GBIT | 64M X 16<br>64M X 16 | 3<br>6 | 1<br>2 | 256 MBYTES<br>512 MBYTES |

# DDR, UART INTERFACES

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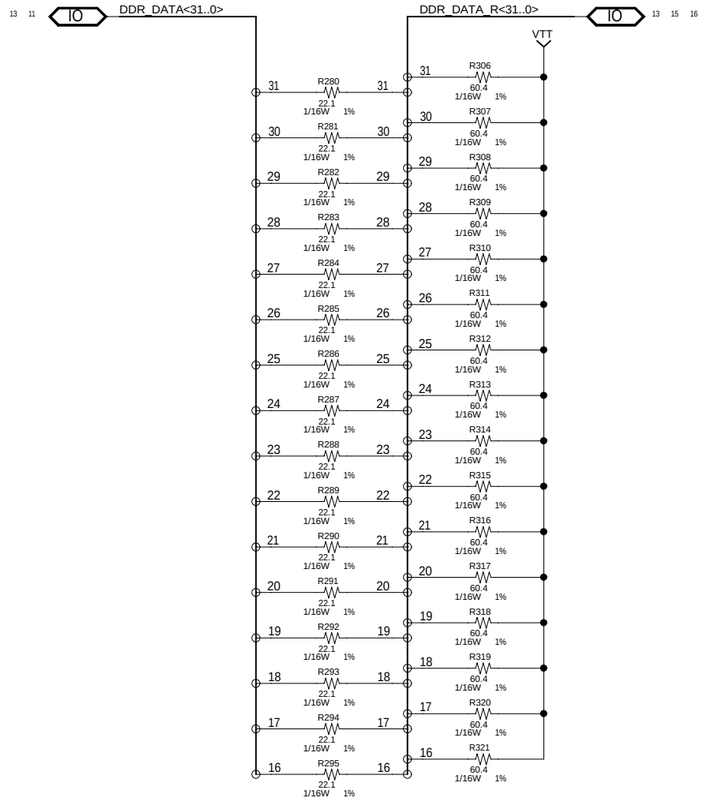
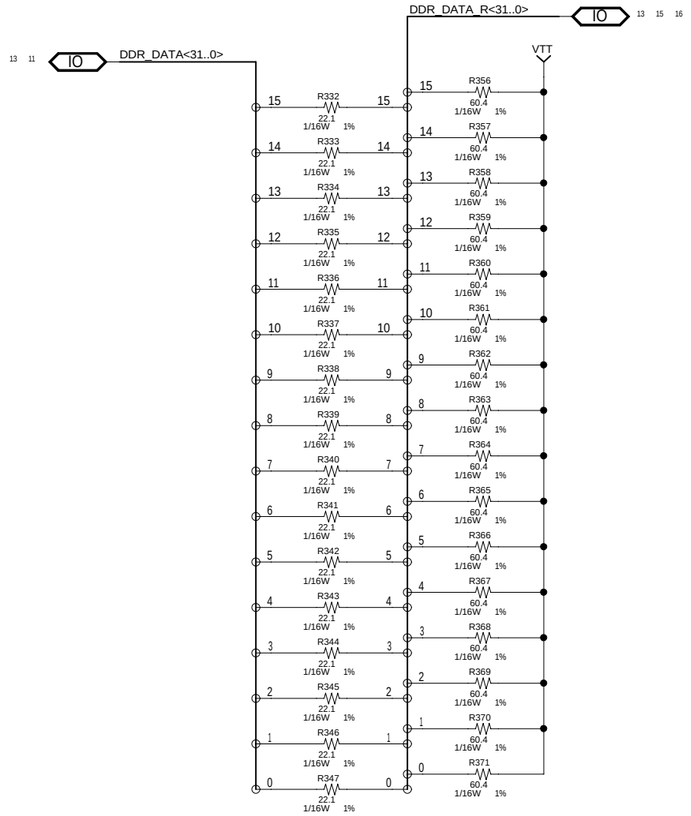
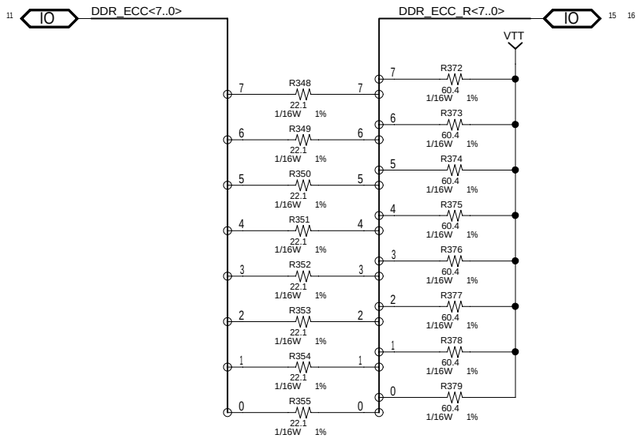
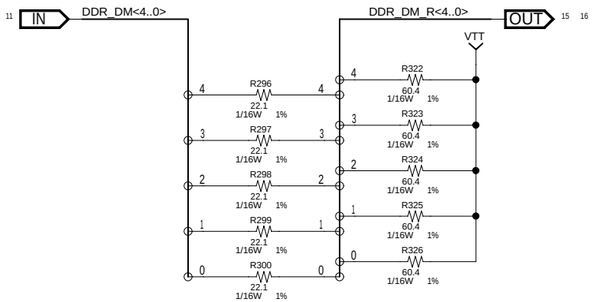
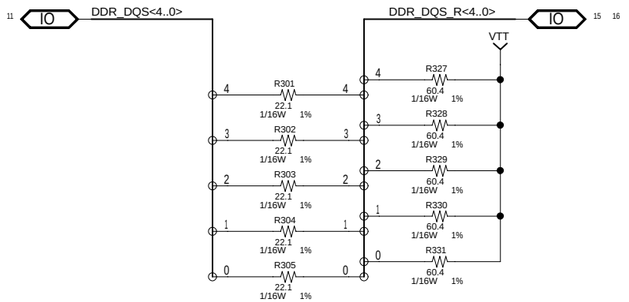
| ENGINEER: | | DATE LAST MODIFIED: | DWG.#: REV: |
| K.Lewandowski | | Wed Jul 13 15:38:20 2005 | C73145 02 |




# DDR TERMINATIONS

INTEL
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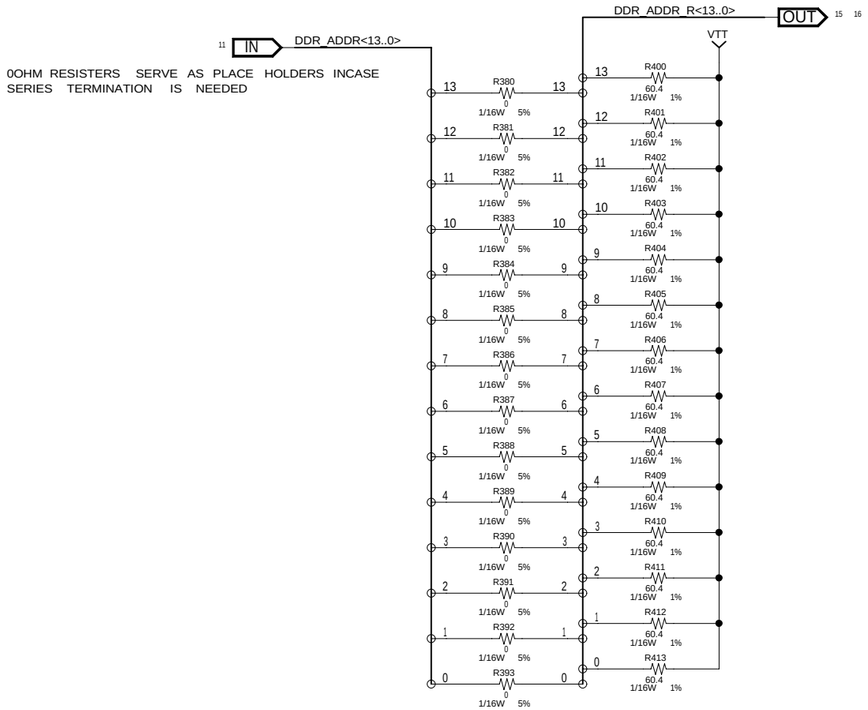
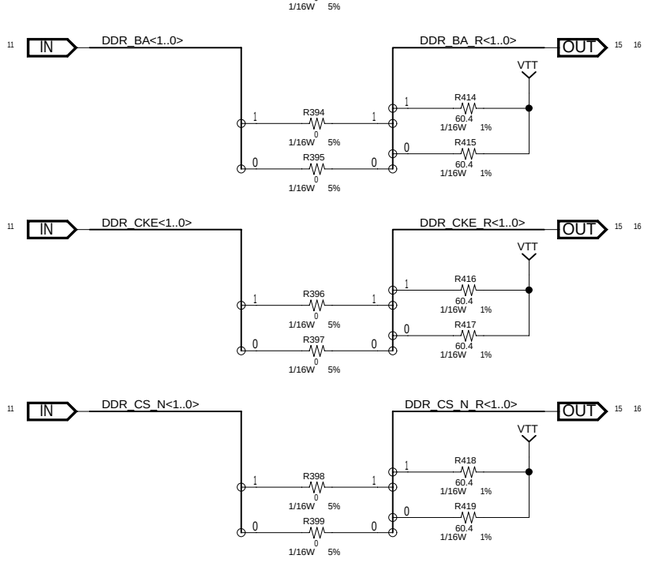
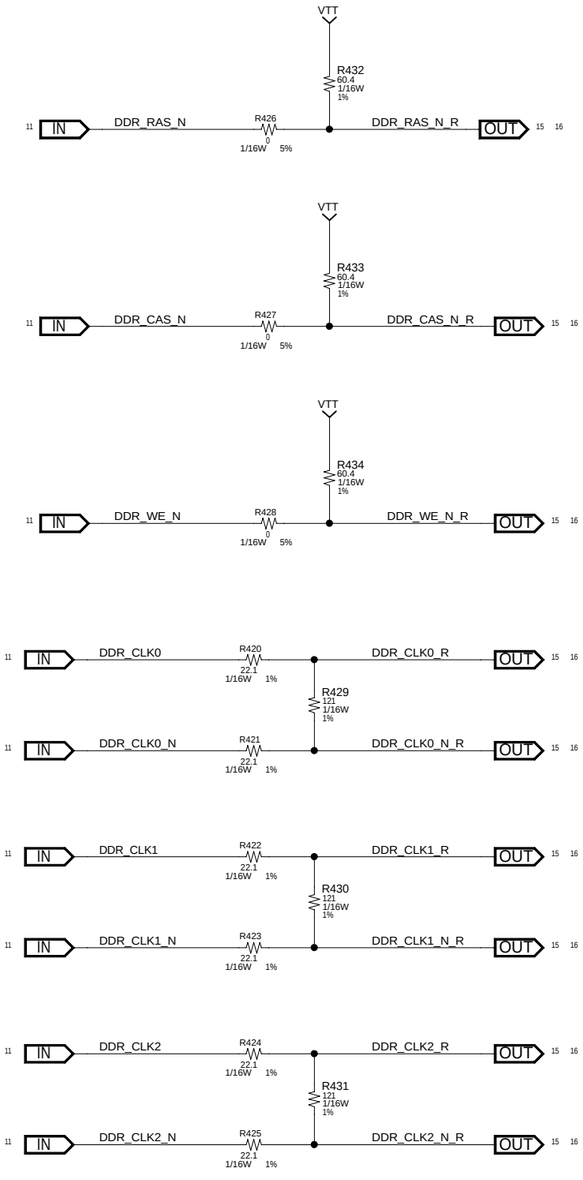
| | | | |
|---|---|---|---|
| DRAWN_BY: K. Lewandowski | LOCAL PAGE: 13 OF 20 | TITLE: IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Wed Jul 13 15:38:21 2005 | DWG.#: C73145 / REV: 02 |




0OHM RESISTERS SERVE AS PLACE HOLDERS INCASE SERIES TERMINATION IS NEEDED




THESE SIGNALS REQUIRE SERIES DAMPENING RESISTORS THAT SHOULD BE PLACED AS CLOSE TO THE PROCESSOR PIN AS POSSIBLE. IT IS RECOMMENDED THAT VALUES ARE TUNED BASED ON SIGNAL INTEGRITY SIMULATIONS USING THE PROCESSORS IBIS MODEL.

# DDR TERMINATIONS

INTEL
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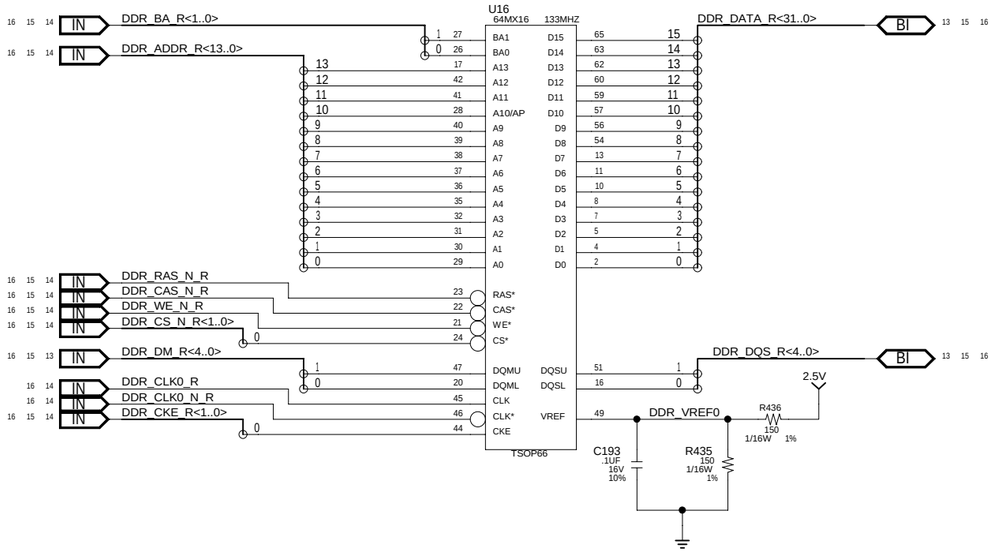
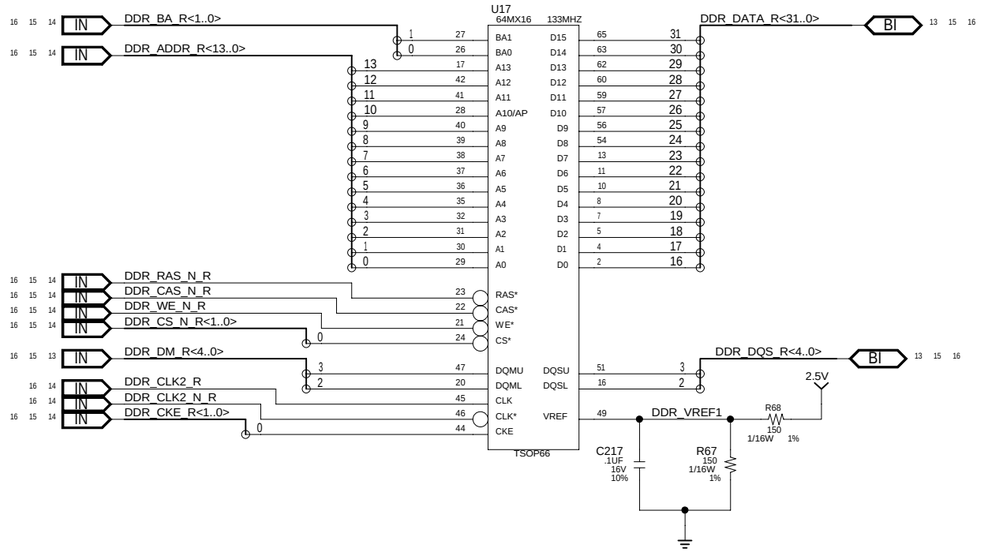
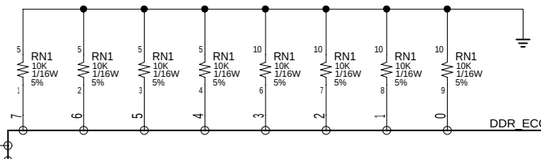
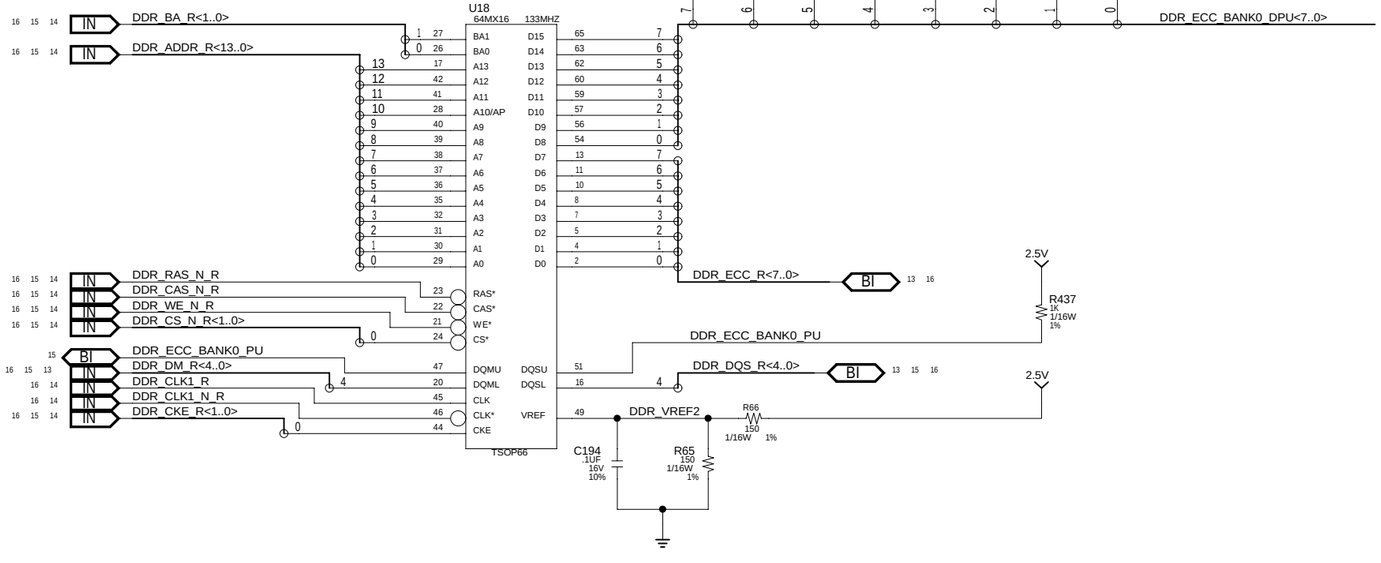
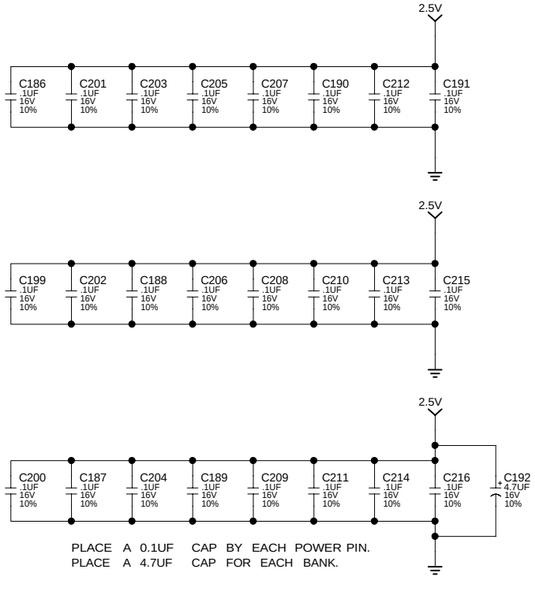
| | | | |
|---|---|---|---|
| DRAWN_BY: K. Lewandowski | LOCAL PAGE: 14 OF 20 | TITLE: IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Wed Jul 13 15:38:21 2005 | DWG.#: C73145 / REV: 02 |




DDR BANK 0

| CAPACITOR | DEVICE | PIN |
|---|---|---|
| C186 | U16 | 1 |
| C201 | U16 | 3 |
| C203 | U16 | 9 |
| C205 | U16 | 15 |
| C207 | U16 | 18 |
| C190 | U16 | 33 |
| C212 | U16 | 55 |
| C191 | U16 | 61 |
| C199 | U17 | 1 |
| C202 | U17 | 3 |
| C188 | U17 | 9 |
| C206 | U17 | 15 |
| C208 | U17 | 18 |
| C210 | U17 | 33 |
| C213 | U17 | 55 |
| C215 | U17 | 61 |
| C200 | U18 | 1 |
| C187 | U18 | 3 |
| C204 | U18 | 9 |
| C189 | U18 | 15 |
| C209 | U18 | 18 |
| C211 | U18 | 33 |
| C214 | U18 | 55 |
| C216 | U18 | 61 |

INTEL
GETZVILLE, NY 14068



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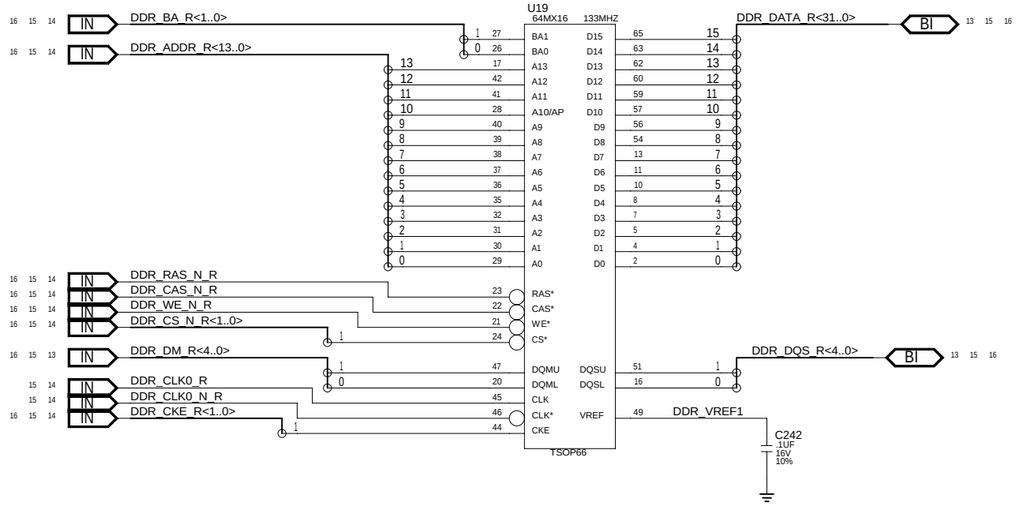
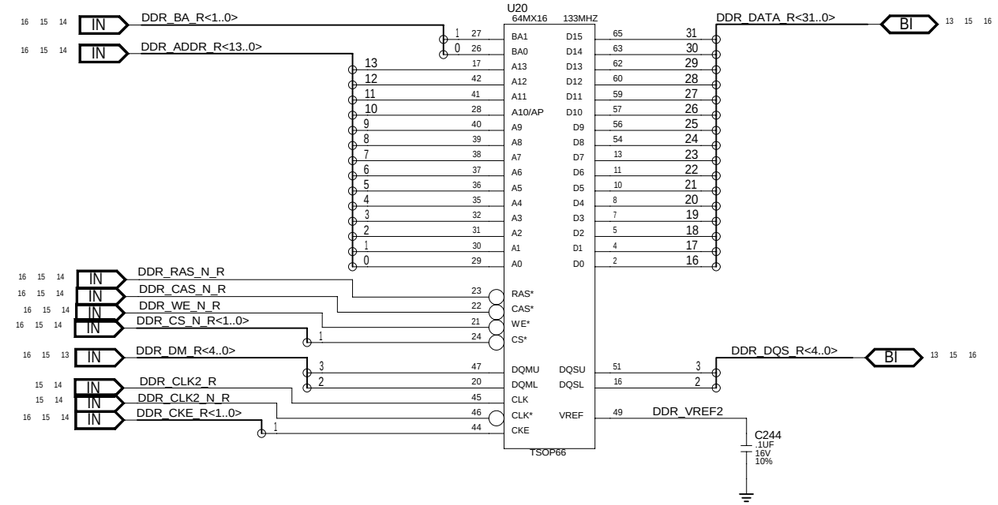
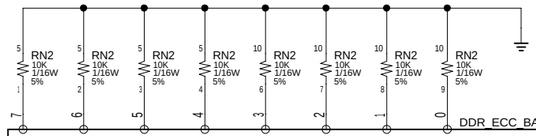
LOCAL PAGE: 15 OF 20
TITLE: IXP46x Network Processor x16 Module
ENGINEER: K.Lewandowski
DATE LAST MODIFIED: Wed Jul 13 15:38:22 2005
DWG.#: C73145
REV: 02

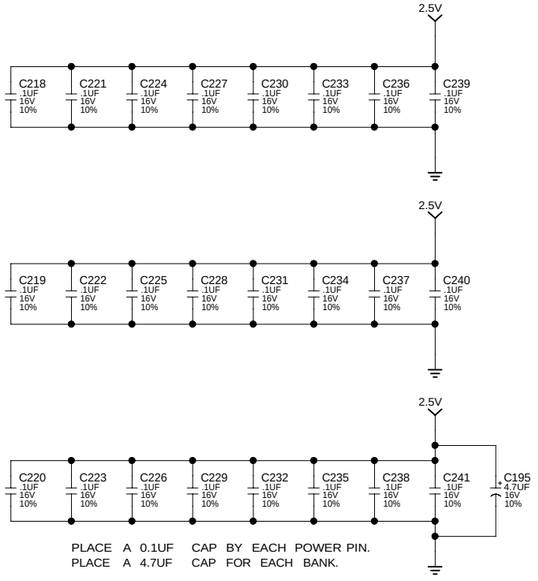









# DDR BANK 1

| CAPACITOR | DEVICE | PIN |
|---|---|---|
| C218 | U19 | 1 |
| C221 | U19 | 3 |
| C224 | U19 | 9 |
| C227 | U19 | 15 |
| C230 | U19 | 18 |
| C233 | U19 | 33 |
| C236 | U19 | 55 |
| C239 | U19 | 61 |
| C219 | U20 | 1 |
| C222 | U20 | 3 |
| C225 | U20 | 9 |
| C228 | U20 | 15 |
| C231 | U20 | 18 |
| C234 | U20 | 33 |
| C237 | U20 | 55 |
| C240 | U20 | 61 |
| C220 | U21 | 1 |
| C223 | U21 | 3 |
| C226 | U21 | 9 |
| C229 | U21 | 15 |
| C232 | U21 | 18 |
| C235 | U21 | 33 |
| C238 | U21 | 55 |
| C241 | U21 | 61 |

INTEL

GETZVILLE, NY 14068

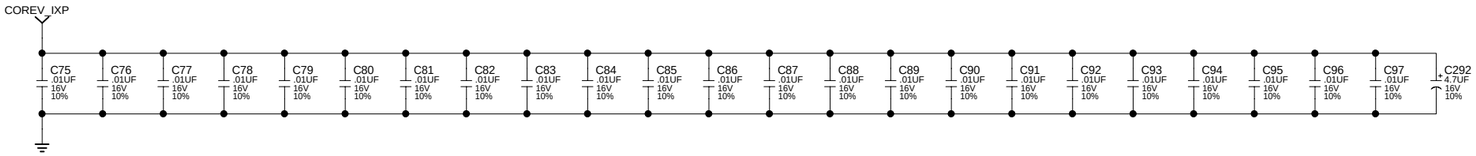


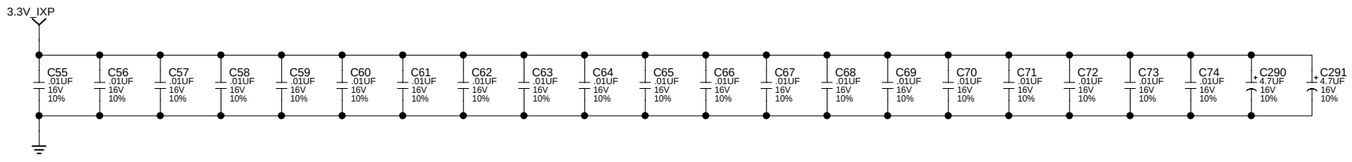
| DRAWN_BY: | LOCAL PAGE: | TITLE: | |
|---|---|---|---|
| K. Lewandowski | 16 OF 20 | IXP46x Network Processor x16 Module | |
| ENGINEER: | | DATE LAST MODIFIED: | DWG.#: / REV: |
| K.Lewandowski | | Wed Jul 13 15:38:23 2005 | C73145 / 02 |

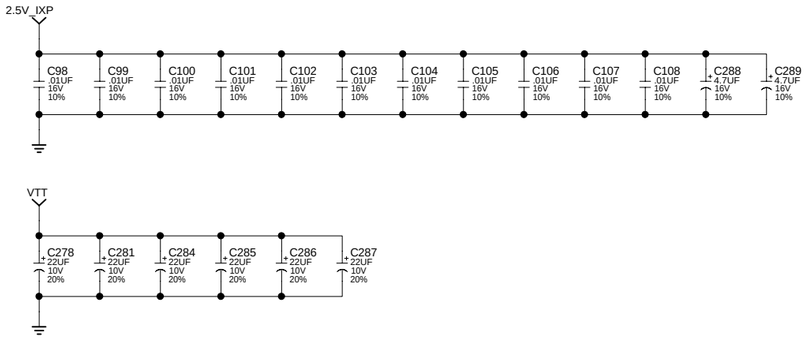
| CAPACITOR | DEVICE | PIN | CAPACITOR | DEVICE | PIN | CAPACITOR | DEVICE | PIN | CAPACITOR | DEVICE | PIN | CAPACITOR | DEVICE | PIN | CAPACITOR | DEVICE | PIN |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C55 | U2 | D1,F3 | C65 | U2 | AB15,AE15 | C75 | U2 | J7,K7 | C85 | U2 | Y18 | C95 | U2 | F12,F13 | C105 | U2 | D21 |
| C56 | U2 | H1 | C66 | U2 | AB19,AF19 | C76 | U2 | L6,M6 | C86 | U2 | U20,V20 | C96 | U2 | F10,F11 | C106 | U2 | A24 |
| C57 | U2 | N3 | C67 | U2 | L22 | C77 | U2 | N6,P6 | C87 | U2 | T21,R21 | C97 | U2 | G9,G10 | C107 | U2 | E8 |
| C58 | U2 | U3,W1 | C68 | U2 | AB22 | C78 | U2 | R6,U7 | C88 | U2 | P21,N21 | C98 | U2 | F9 | C108 | U2 | E7 |
| C59 | U2 | AC3 | C69 | U2 | W23 | C79 | U2 | V6,V7 | C89 | U2 | M21,L21 | C99 | U2 | E9 | | | |
| C60 | U2 | AC5,AD5 | C70 | U2 | B24 | C80 | U2 | Y9,Y10 | C90 | U2 | J20,K20 | C100 | U2 | C10 | | | |
| C61 | U2 | AC10 | C71 | U2 | D26 | C81 | U2 | AA11,AA12 | C91 | U2 | R22 | C101 | U2 | E12 | | | |
| C62 | U2 | Y7 | C72 | U2 | J26 | C82 | U2 | AA13,AB13 | C92 | U2 | G18,G19 | C102 | U2 | C14 | | | |
| C63 | U2 | AE7 | C73 | U2 | R26 | C83 | U2 | AA14,AA15 | C93 | U2 | G17,F16 | C103 | U2 | A16 | | | |
| C64 | U2 | AF12 | C74 | U2 | AC26 | C84 | U2 | AA16,Y17 | C94 | U2 | F14,F15 | C104 | U2 | E20 | | | |

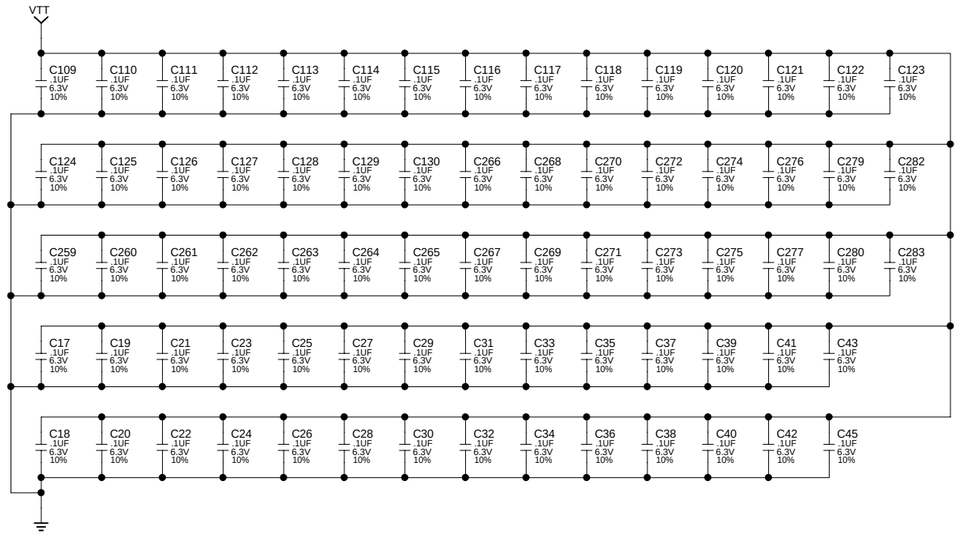
BYPASS CAPACITOR TABLE PROVIDED TO IDENTIFY WHICH PINS THE CAPACITORS ARE TO BE PLACED NEAR FOR FILTERING

CAPACITORS WITH TWO PIN NUMBERS WILL PROVIDE POWER FILTERING FOR BOTH PINS AS THERE WILL BE A COMMON BALL ESCAPE PATH FOR THE PINS




# FILTER COMPONENTS

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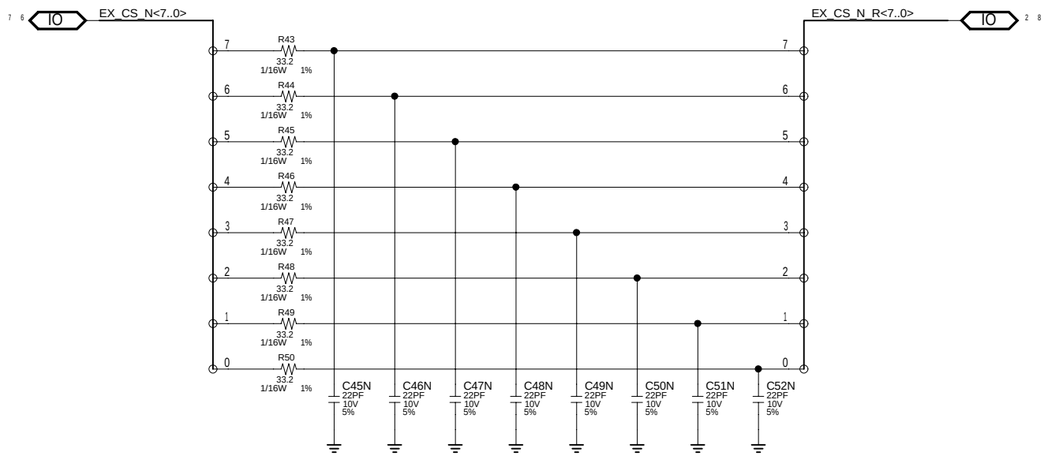
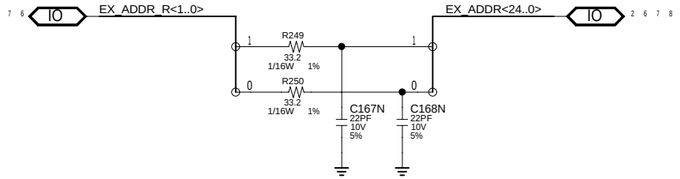
| K. Lewandowski | 17 OF 20 | IXP46x Network Processor x16 Module | |
| ENGINEER: K.Lewandowski | | DATE LAST MODIFIED: Wed Jul 13 15:38:24 2005 | DWG.#: C73145 / REV: 02 |




PLACE CAPACITORS IF FILTERING COMPLIENCE NEEDED

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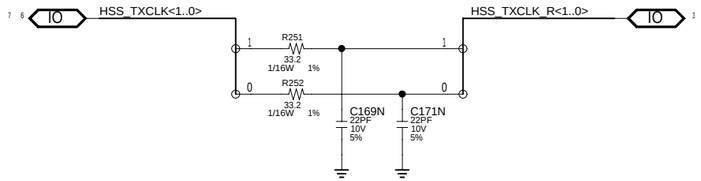


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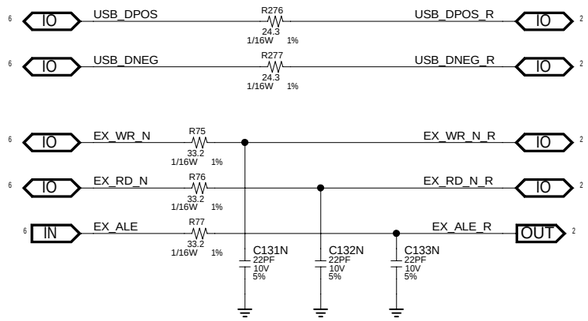


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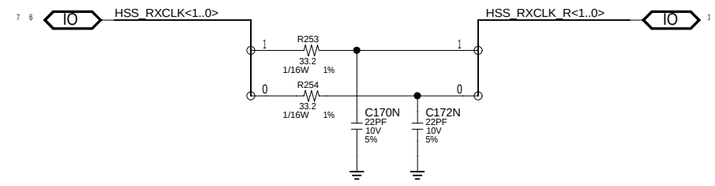


PLACE CAPACITORS IF FILTERING COMPLIENCE NEEDED

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| DRAWN_BY: K. Lewandowski | LOCAL PAGE: 18 OF 20 | TITLE: IXP46x Network Processor x16 Module | |
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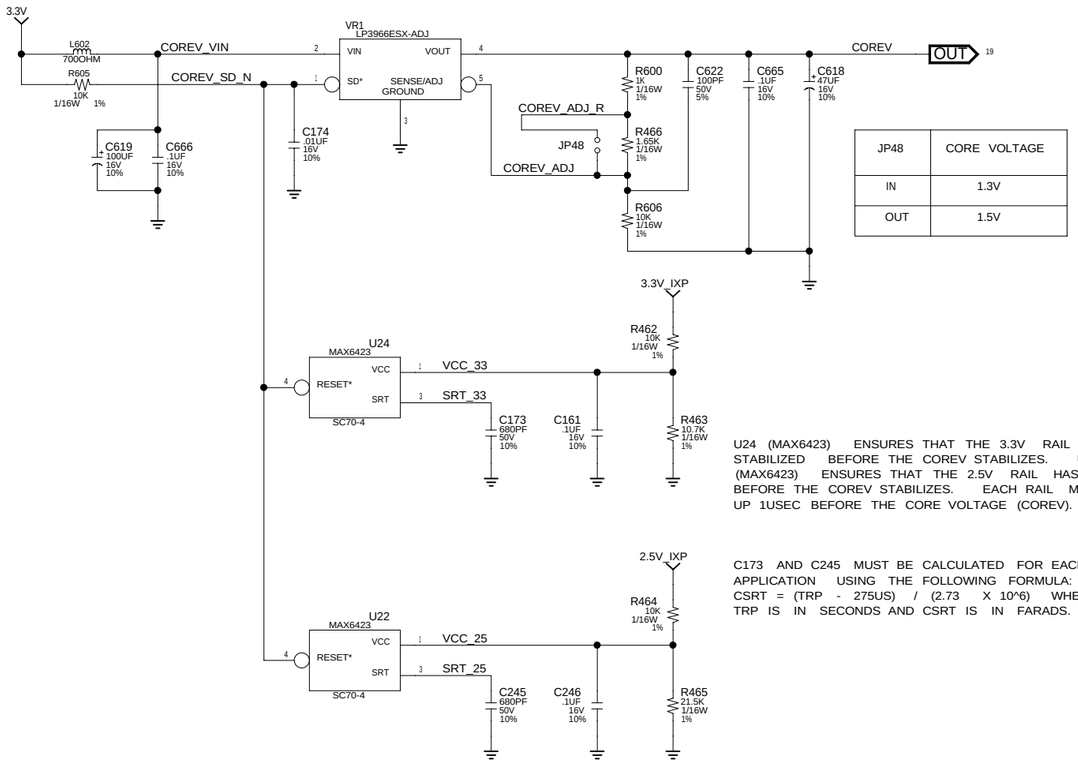
## VOLTAGE REGULATOR FOR THE IXP CORE

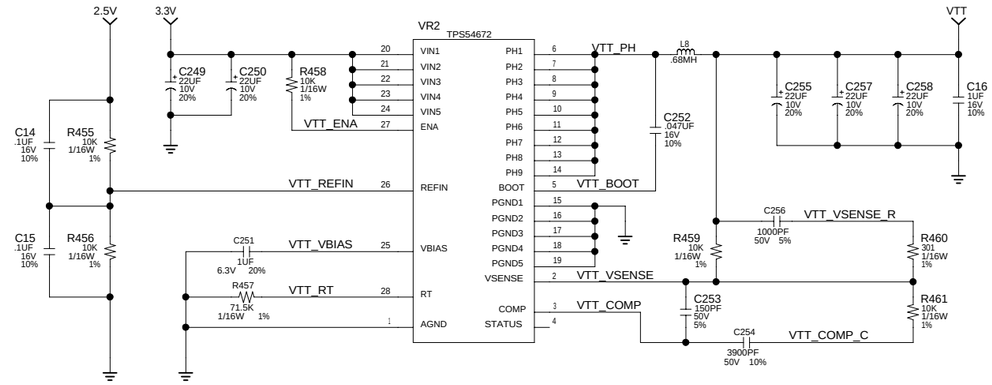



| JP48 | CORE VOLTAGE |
|---|---|
| IN | 1.3V |
| OUT | 1.5V |

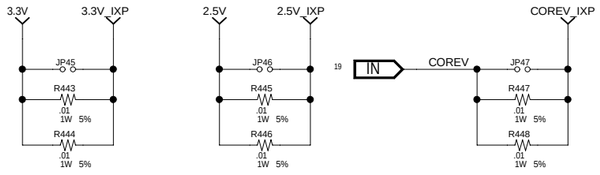
U24 (MAX6423) ENSURES THAT THE 3.3V RAIL HAS STABILIZED BEFORE THE COREV STABILIZES. U22 (MAX6423) ENSURES THAT THE 2.5V RAIL HAS STABILIZED BEFORE THE COREV STABILIZES. EACH RAIL MUST BE POWERED UP 1USEC BEFORE THE CORE VOLTAGE (COREV).

C173 AND C245 MUST BE CALCULATED FOR EACH APPLICATION USING THE FOLLOWING FORMULA: CSRT = (TRP - 275US) / (2.73 X 10^6) WHERE TRP IS IN SECONDS AND CSRT IS IN FARADS.

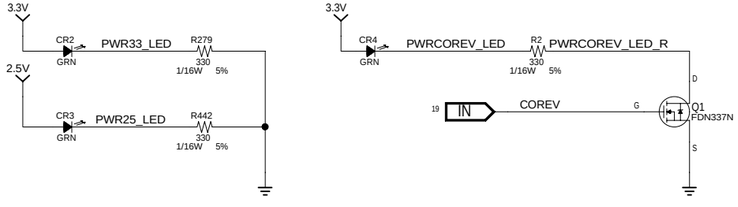
## 1.25 VOLTAGE REGULATOR FOR DDR SIGNAL TERMINATION



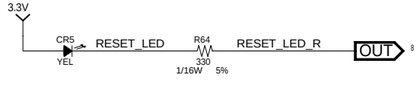

## IXP CURRENT MEASUREMENT CONNECTORS



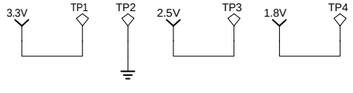

## POWER INDICATOR LEDS




## RESET INDICATOR LED




(PLACE 0.2" APART ON CENTER)




# CORE VOLTAGE, VTT, POWER CONNECTORS CURRENT MEASUREMENT HEADERS, LEDS

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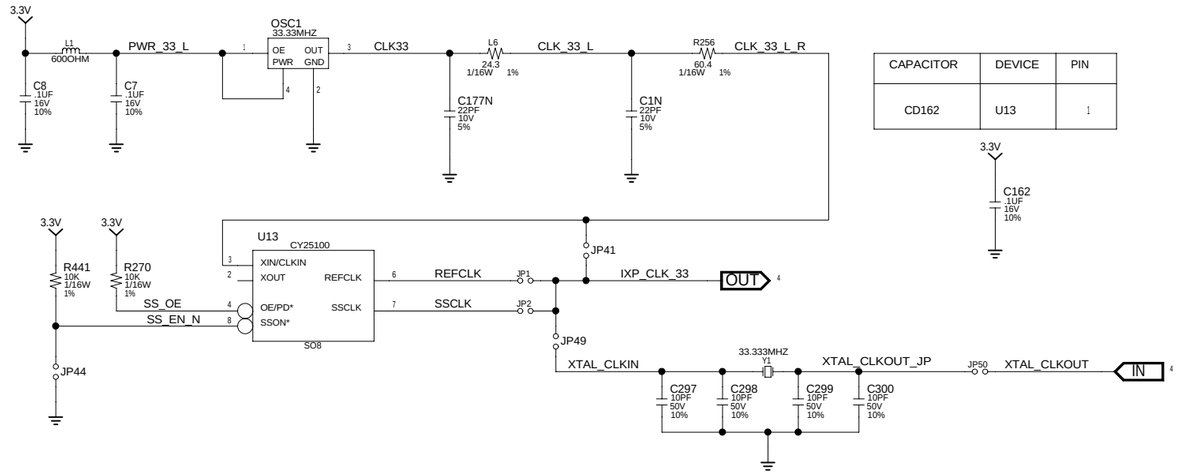
CLOCK GENERATION CIRCUITRY FOR THE IXP

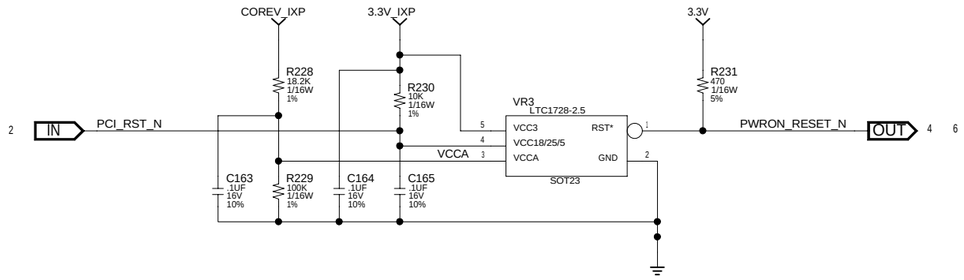



| CAPACITOR | DEVICE | PIN |
|---|---|---|
| CD162 | U13 | 1 |




| JP44 | SPREAD SPECTRUM |
|---|---|
| IN | ENABLED |
| OUT | DISABLED |

POWER MONITOR CIRCUIT USED TO RESET THE IXP




# IXP CLOCK AND RESET

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| K.Lewandowski | | Wed Jul 13 15:38:27 2005 | C73145 | 02 |