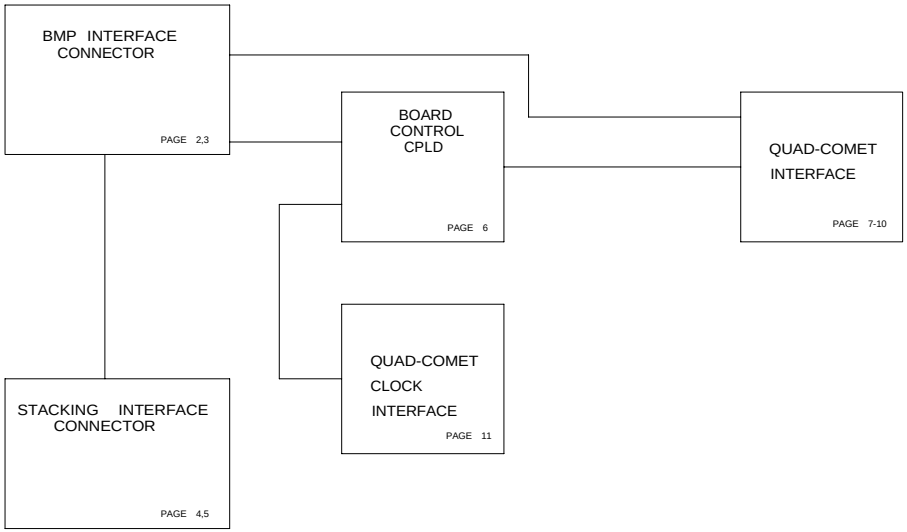
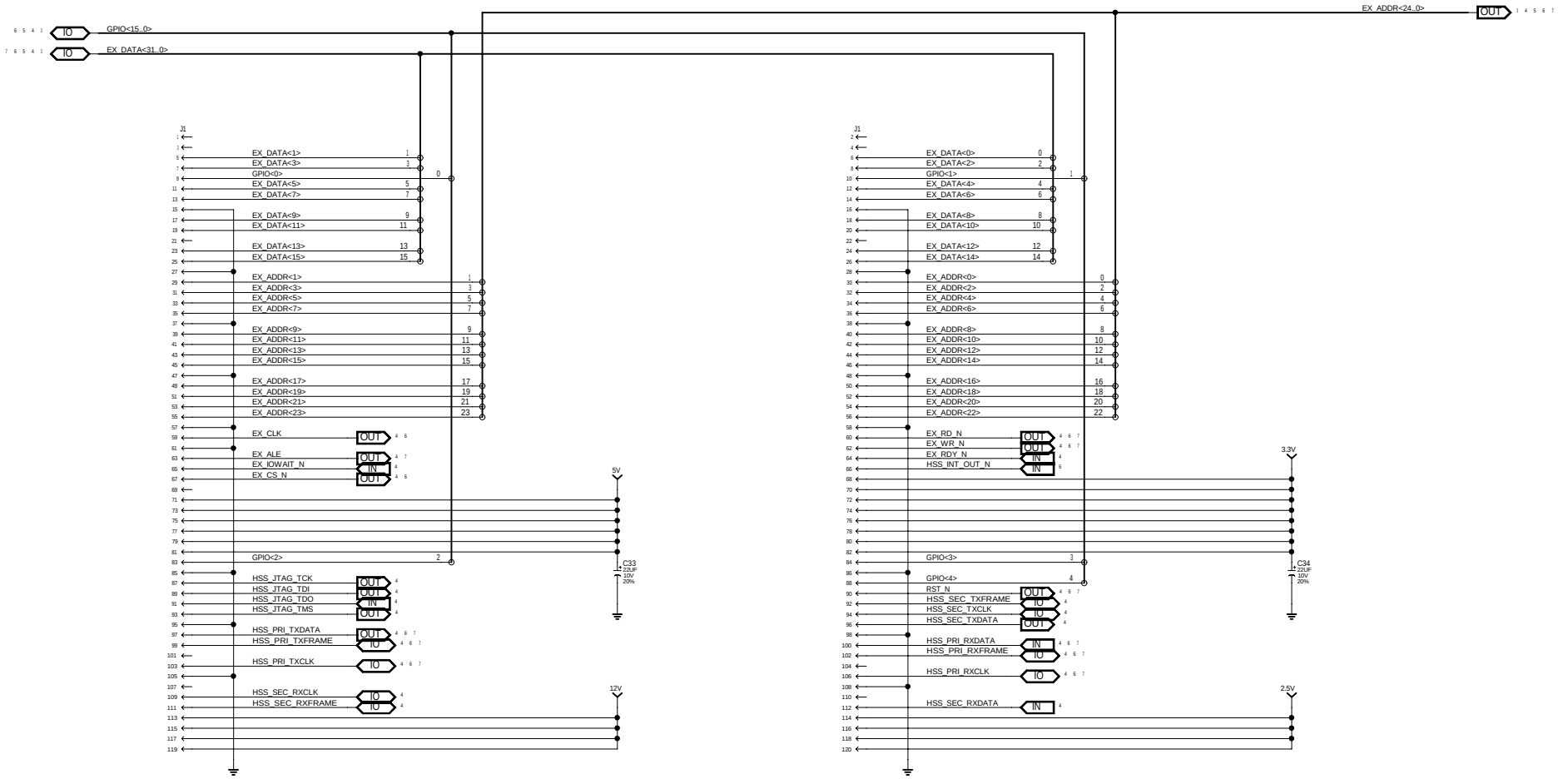


REFERENCE DESIGNATOR LEGEND
(REFDES MAX LENGTH 7 CHARACTERS)

CCCXXXW C = COMPONENT (1-3 CHARACTERS)
OSC = OSCILLATOR
VR = VOLTAGE REGULATOR
R = RESISTOR
X = REFDES NUMBER
(0-9)
W = WILDCARD (OPTIONAL)
N=DNP

INTEL
GETZVILLE, NY 14068

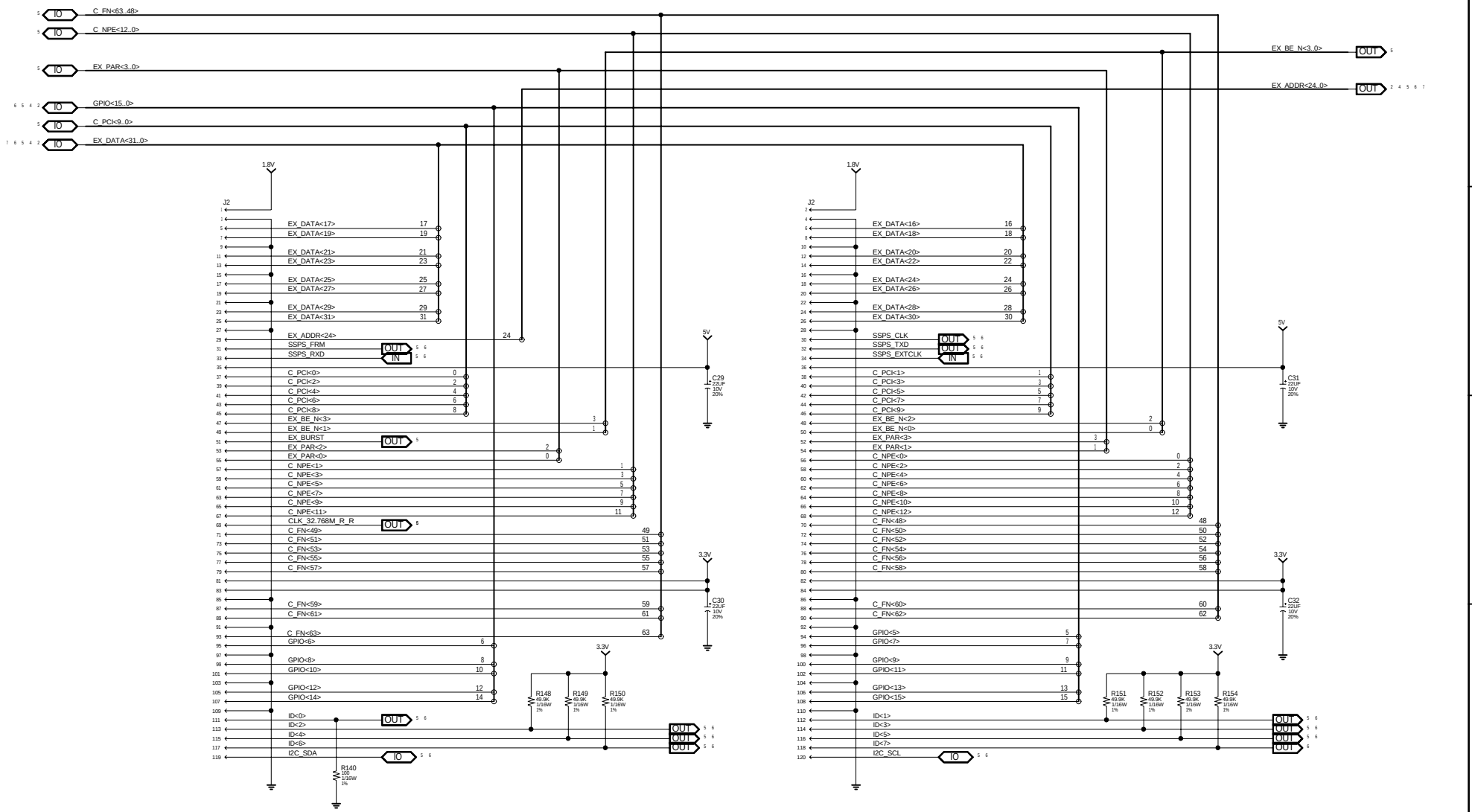
DRAWN_BY: Gene DeFabio	LOCAL PAGE: 1 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Mon Oct 11 11:12:06 2004	DWG.#: C73146 / REV: 2



BMP INTERFACE STANDARD CONNECTOR

INTEL
GETZVILLE, NY 14068

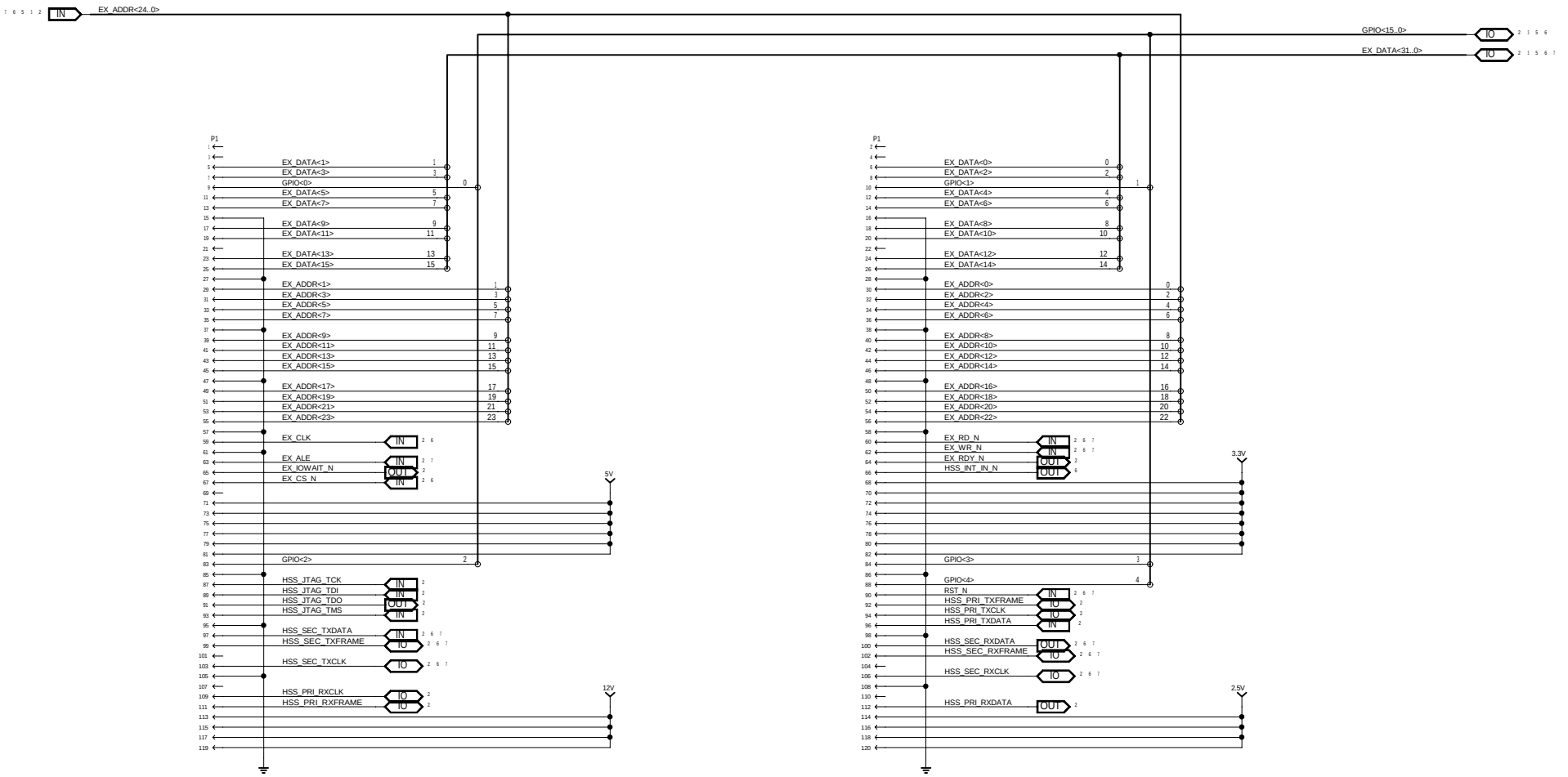
DRAWN_BY: Gene DeFabio	LOCAL PAGE: 2 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Thu May 12 16:34:09 2005	DWG.#: C73146 / REV: 2



BMP EXPANSION INTERFACE CONNECTOR

INTEL
GETZVILLE, NY 14068

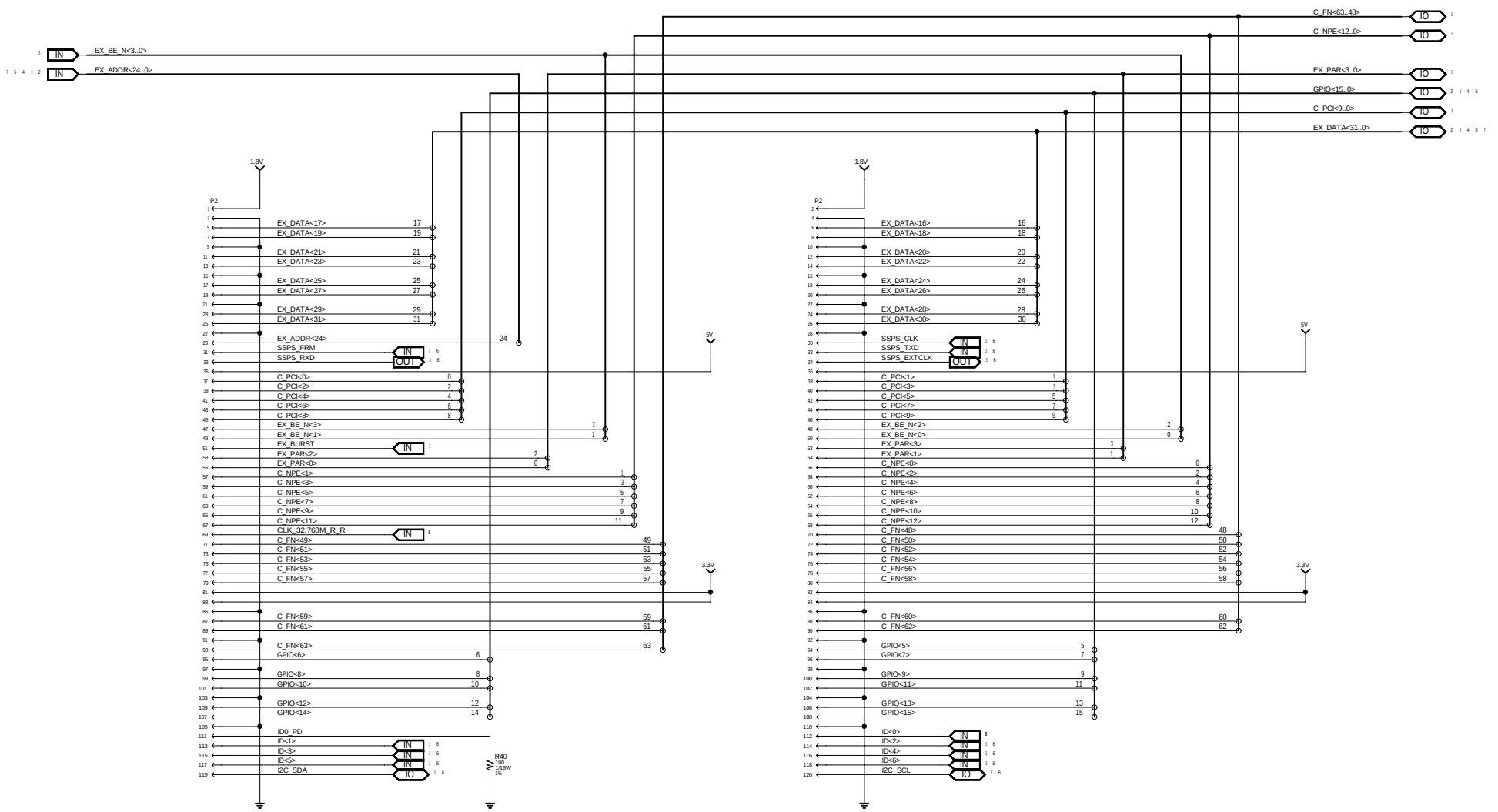
DRAWN_BY: Gene DeFabio	LOCAL PAGE: 3 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Thu May 12 16:34:10 2005	DWG.#: C73146 / REV: 2



STACKING INTERFACE STANDARD CONNECTOR

INTEL
GETZVILLE, NY 14068

DRAWN_BY: Gene DeFabio	LOCAL PAGE: 4 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Thu May 12 16:34:11 2005	DWG.#: C73146 / REV: 2



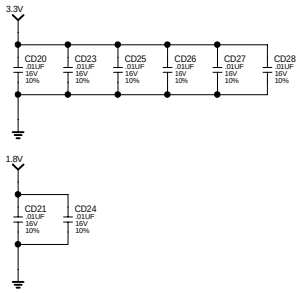
STACKING INTERFACE EXPANSION CONNECTOR

INTEL
GETZVILLE, NY 14068

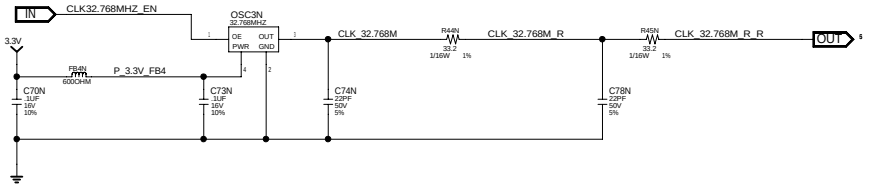
DRAWN_BY: Gene DeFabio	LOCAL PAGE: 5 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Thu May 12 16:34:12 2005	DWG.#: C73146 / REV: 2

PLACE A 0.01UF CAP BY EACH POWER PIN.

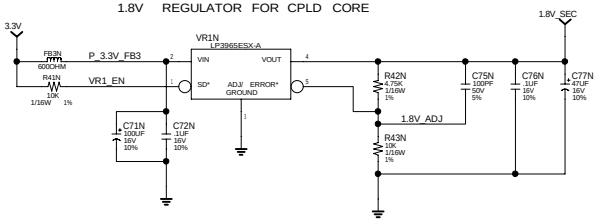
CAPACITOR	DEVICE	PIN
CD20	U2	5
CD23	U2	20
CD25	U2	38
CD26	U2	51
CD27	U2	88
CD28	U2	98
CD21	U2	26
CD24	U2	57



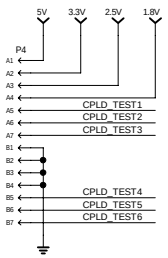
32.768MHZ CLOCK

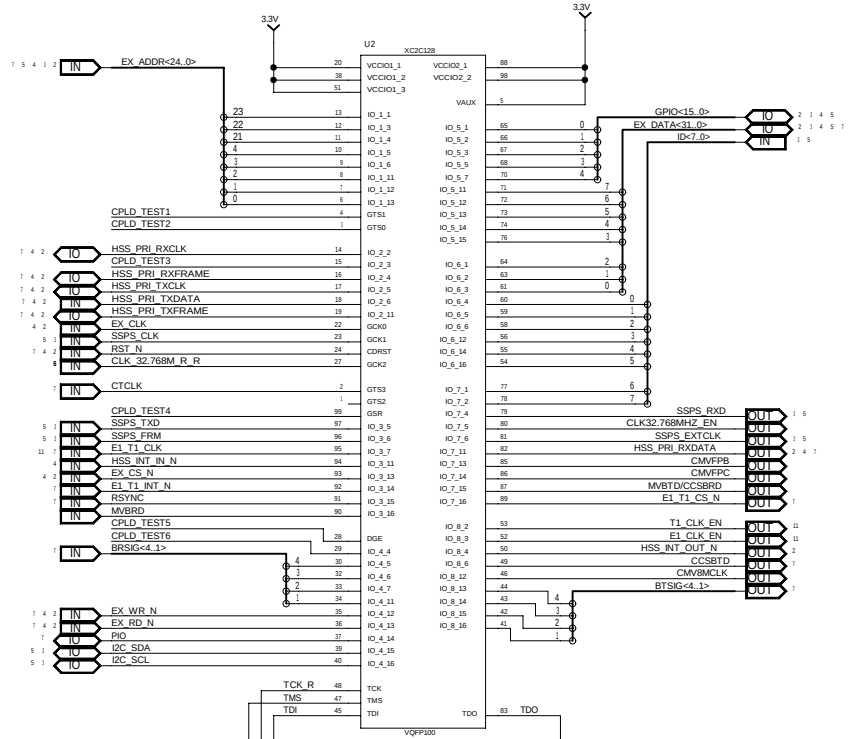


1.8V REGULATOR FOR CPLD CORE



CPLD TEST HEADER

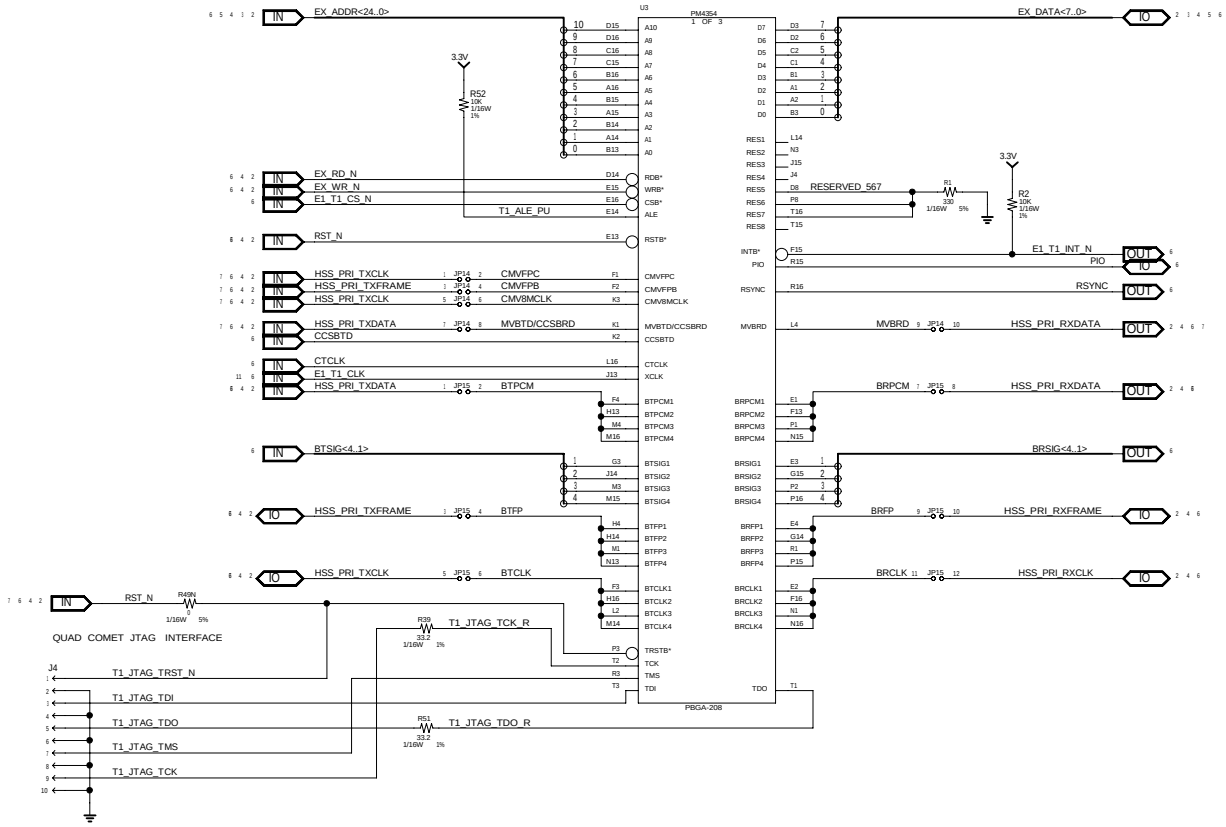




BOARD CONTROL CPLD

INTEL
GETZVILLE, NY 14068

DRAWN_BY: Gene DeFabio	LOCAL PAGE: 6 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Thu May 12 16:34:12 2005	DWG.#: C73146 / REV: 2

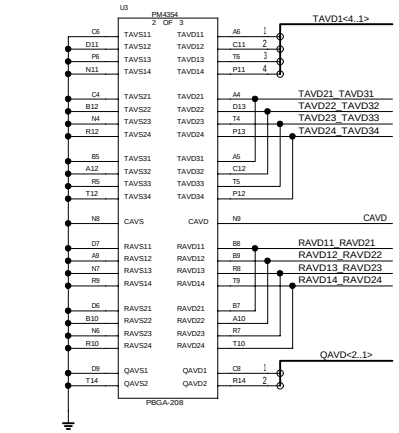


COMET-QUAD PROC/E1/T1 INTERFACE

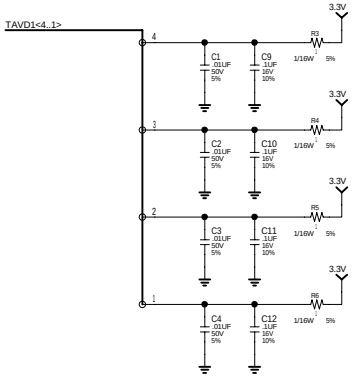
INTEL
GETZVILLE, NY 14068

DRAWN_BY: Gene DeFabio	LOCAL PAGE: 7 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Thu May 12 16:34:13 2005	DWG.#: C73146 REV: 2

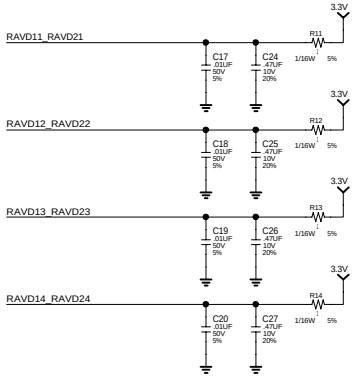
NOTE: ALL SIGNALS ON THIS PAGE
TERMINATE ON THIS PAGE



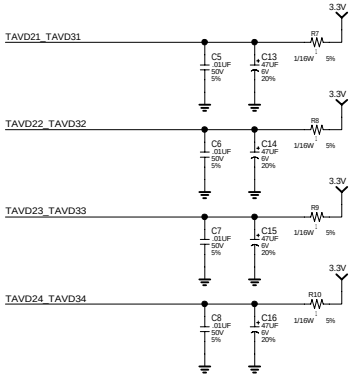
TRANSMIT ANALOG POWER DECOUPLING 1



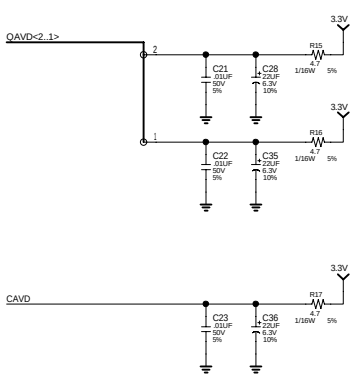
RECEIVE ANALOG POWER DECOUPLING 1 & 2

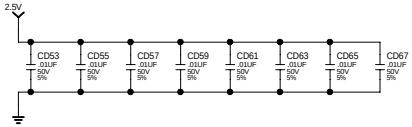


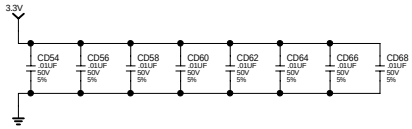
TRANSMIT ANALOG POWER DECOUPLING 2 & 3



QUIET ANALOG POWER DECOUPLING 1 & 2







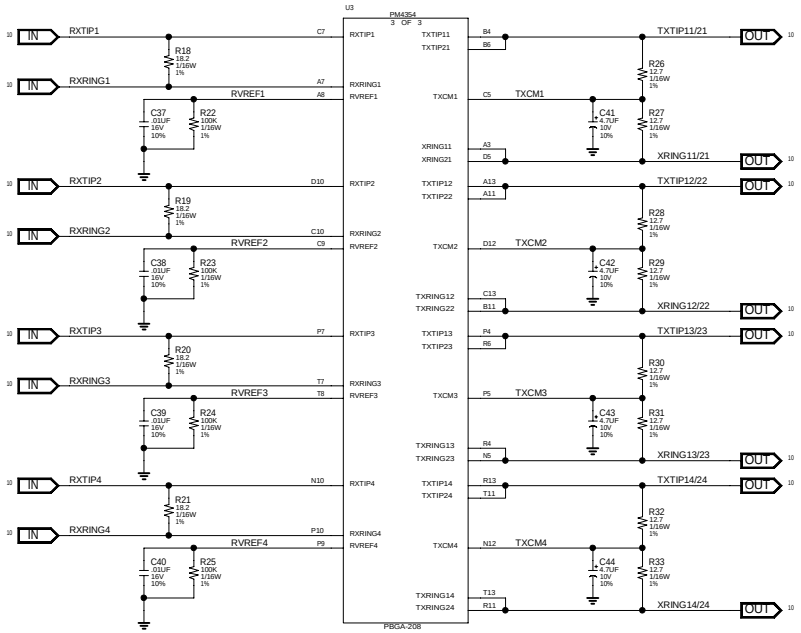
CAPACITOR	DEVICE	PIN
CD53	U3	G1
CD55	U3	H3
CD57	U3	J1
CD59	U3	L1
CD61	U3	H15
CD63	U3	K15
CD65	U3	M13
CD67	U3	J16

CAPACITOR	DEVICE	PIN
CD54	U3	H2
CD56	U3	K14
CD58	U3	C3
CD60	U3	D4
CD62	U3	K4
CD64	U3	N2
CD66	U3	G16
CD68	U3	N14

COMET-QUAD POWER INTERFACE

INTEL
GETZVILLE, NY 14068

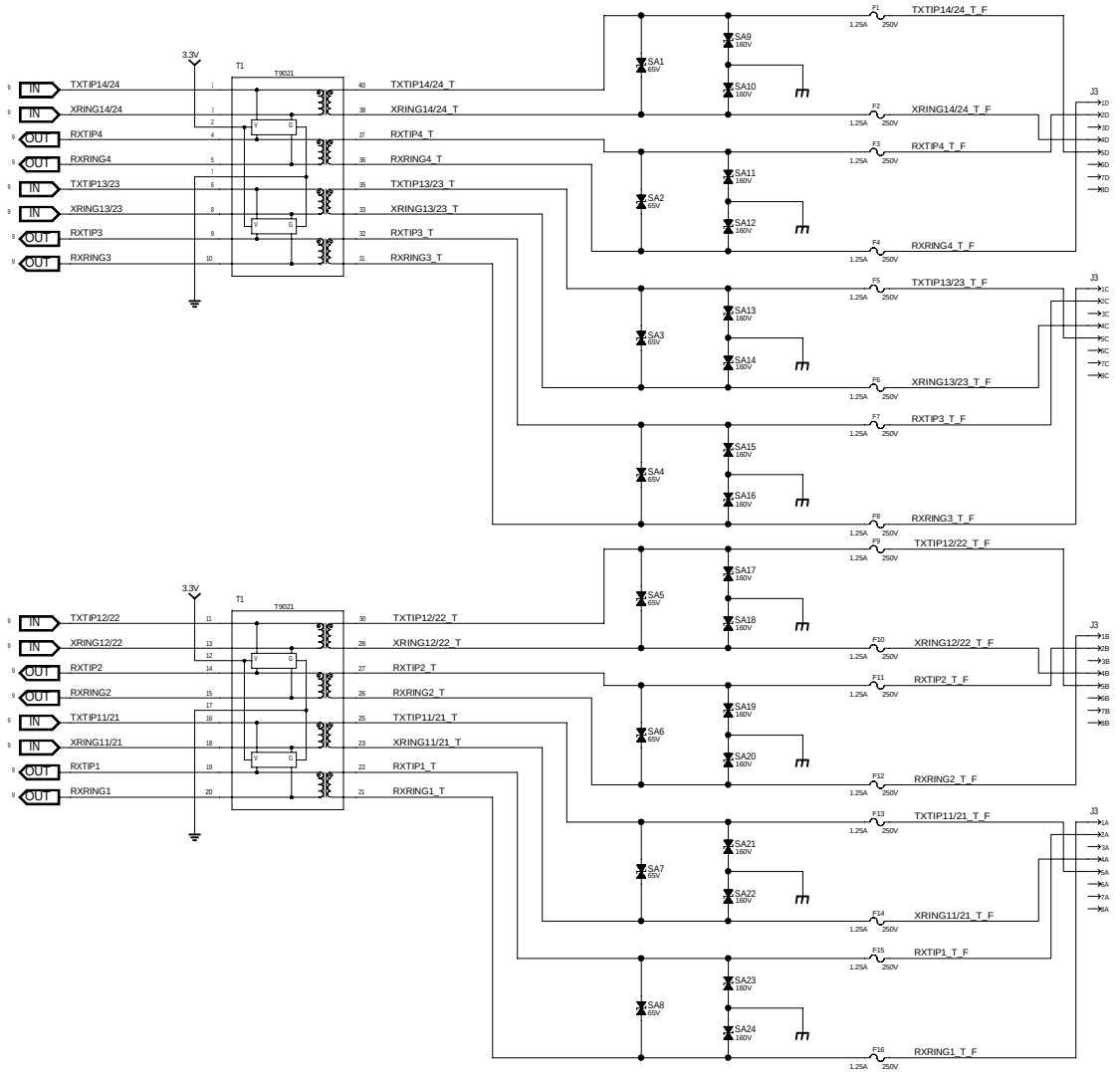
DRAWN_BY: Gene DeFabio	LOCAL PAGE: 8 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Thu May 12 16:34:14 2005	DWG.#: C73146 / REV: 2



COMET-QUAD LINE INTERFACE

INTEL
GETZVILLE, NY 14068

DRAWN_BY: Gene DeFabio	LOCAL PAGE: 9 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Thu May 12 16:34:14 2005	DWG.#: C73146 / REV: 2



COMET-QUAD PROTECTION CIRCUITRY

INTEL
GETZVILLE, NY 14068

DRAWN_BY: Gene DeFabio	LOCAL PAGE: 10 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Thu May 12 16:34:15 2005	DWG.#: C73146 / REV: 2

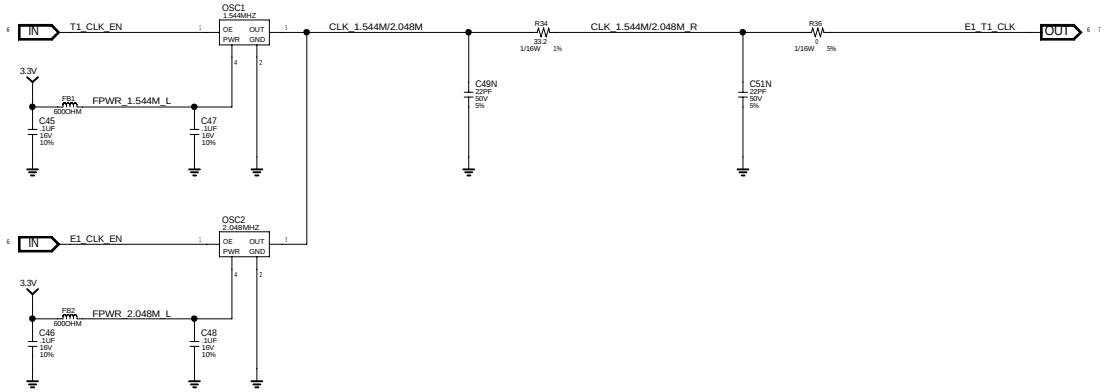
NOTE: EACH CONFIGURATION NEEDS TO BE EVALUATED TO MEET SPECIFIC EMC REQUIREMENTS. THE COMPONENT VALUES NEED TO BE CALCULATED FOR THE FREQUENCY CUTOFF DESIRED.

OPTION 1 - INSTALL R34 AND R36 ONLY.

OPTION 2 - INSTALL R34,R36, AND C49N.

OPTION 3 - INSTALL C49N, C51N, R34(WITH AN INDUCTOR), AND R36.

T1 CLOCK GENERATION CIRCUITRY



OPTIONAL 1.8V REGULATOR CONNECTION

OPTIONAL GROUND CONNECTION

BOARD MOUNTING HOLES

CHASSIS GROUND CONNECTION

COMET-QUAD E1/T1 INPUT CLOCK

INTEL
GETZVILLE, NY 14068

DRAWN_BY: Gene DeFabio	LOCAL PAGE: 11 OF 11	TITLE: T1/E1 Mezzanine Card	
ENGINEER: Gene DeFabio		DATE LAST MODIFIED: Thu May 12 16:34:16 2005	DWG.#: C73146 REV: 2