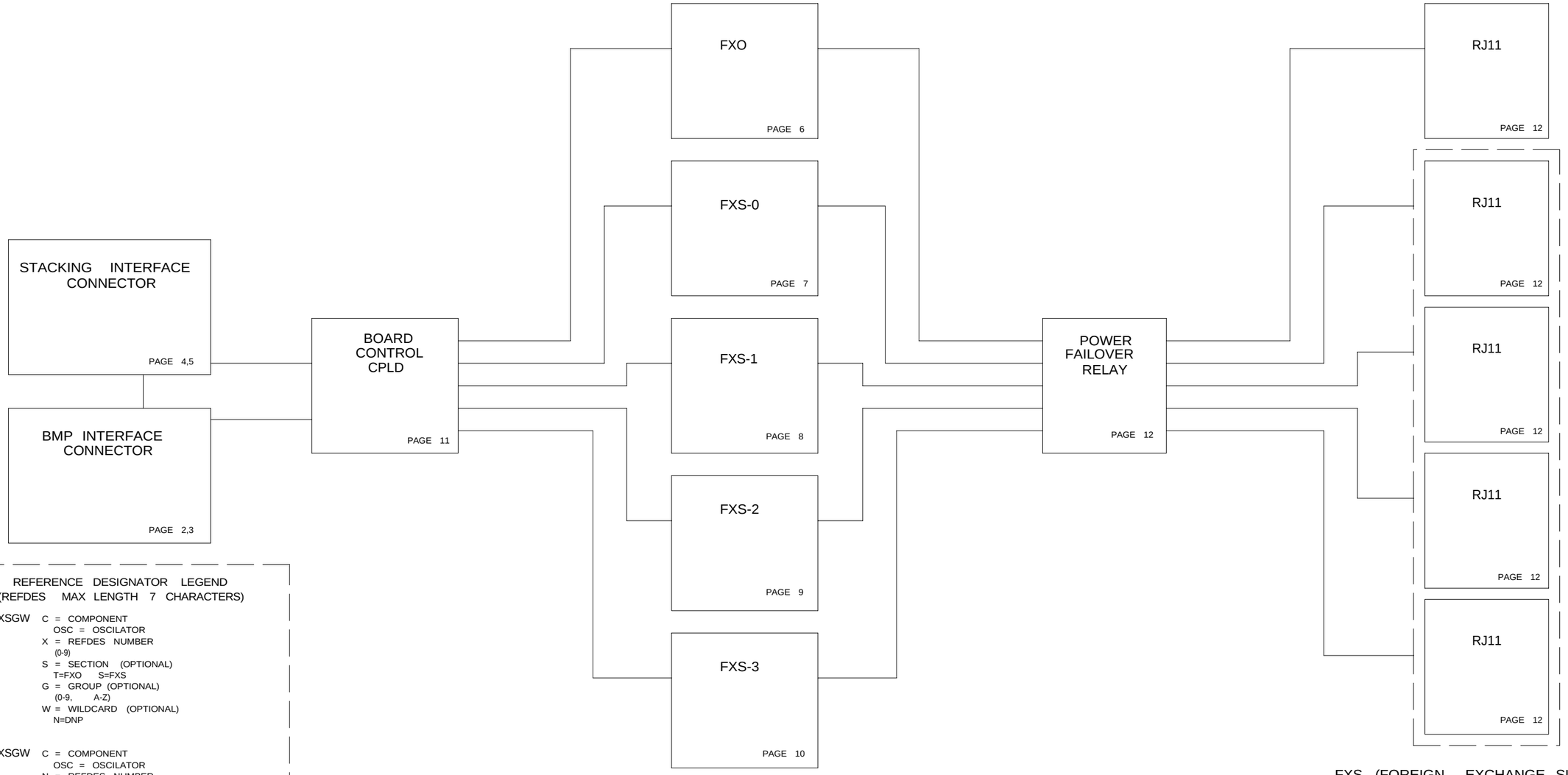
FXO (FOREIGN EXCHANGE OFFICE)



FXS (FOREIGN EXCHANGE SUBSCRIBER)

REFERENCE DESIGNATOR LEGEND
(REFDES MAX LENGTH 7 CHARACTERS)

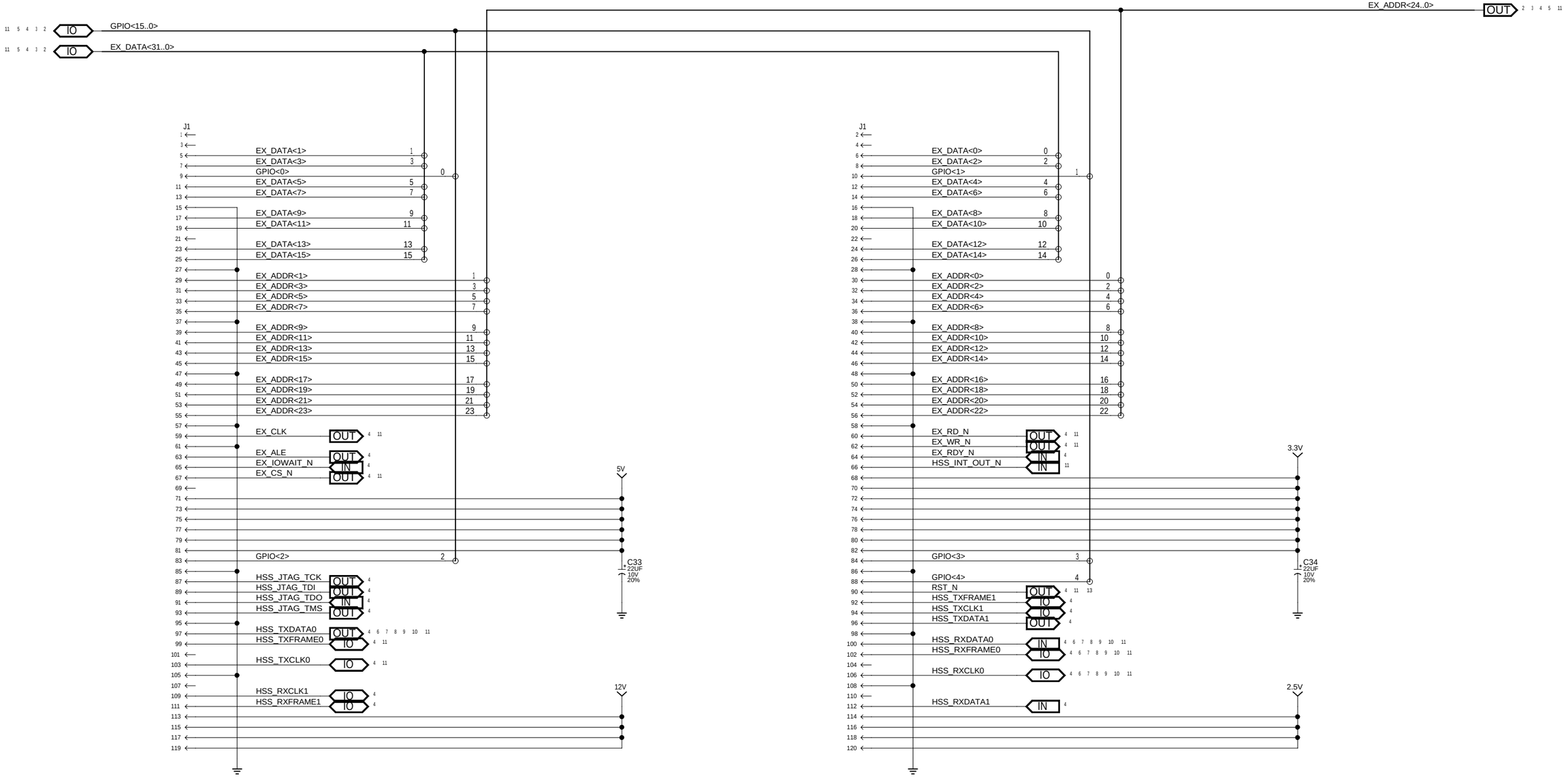
CCCXSGW
- C = COMPONENT
  OSC = OSCILATOR
- X = REFDES NUMBER
  (0-9)
- S = SECTION (OPTIONAL)
  T=FXO S=FXS
- G = GROUP (OPTIONAL)
  (0-9, A-Z)
- W = WILDCARD (OPTIONAL)
  N=DNP

CCNXSGW
- C = COMPONENT
  OSC = OSCILATOR
- N = REFDES NUMBER
  (0-9)
- X = REFDES NUMBER
  (0-9, A-Z)
- S = SECTION (OPTIONAL)
  T=FXO S=FXS
- G = GROUP (OPTIONAL)
  (0-9, A-Z)
- W = WILDCARD (OPTIONAL)
  N=DNP

CNXXSGW
- C = COMPONENT
  OSC = OSCILATOR
- N = REFDES NUMBER
  (0-9)
- X = REFDES NUMBER
  (0-9, A-Z)
- S = SECTION (OPTIONAL)
  T=FXO S=FXS
- G = GROUP (OPTIONAL)
  (0-9, A-Z)
- W = WILDCARD (OPTIONAL)
  N=DNP

INTEL
GETZVILLE, NY 14068

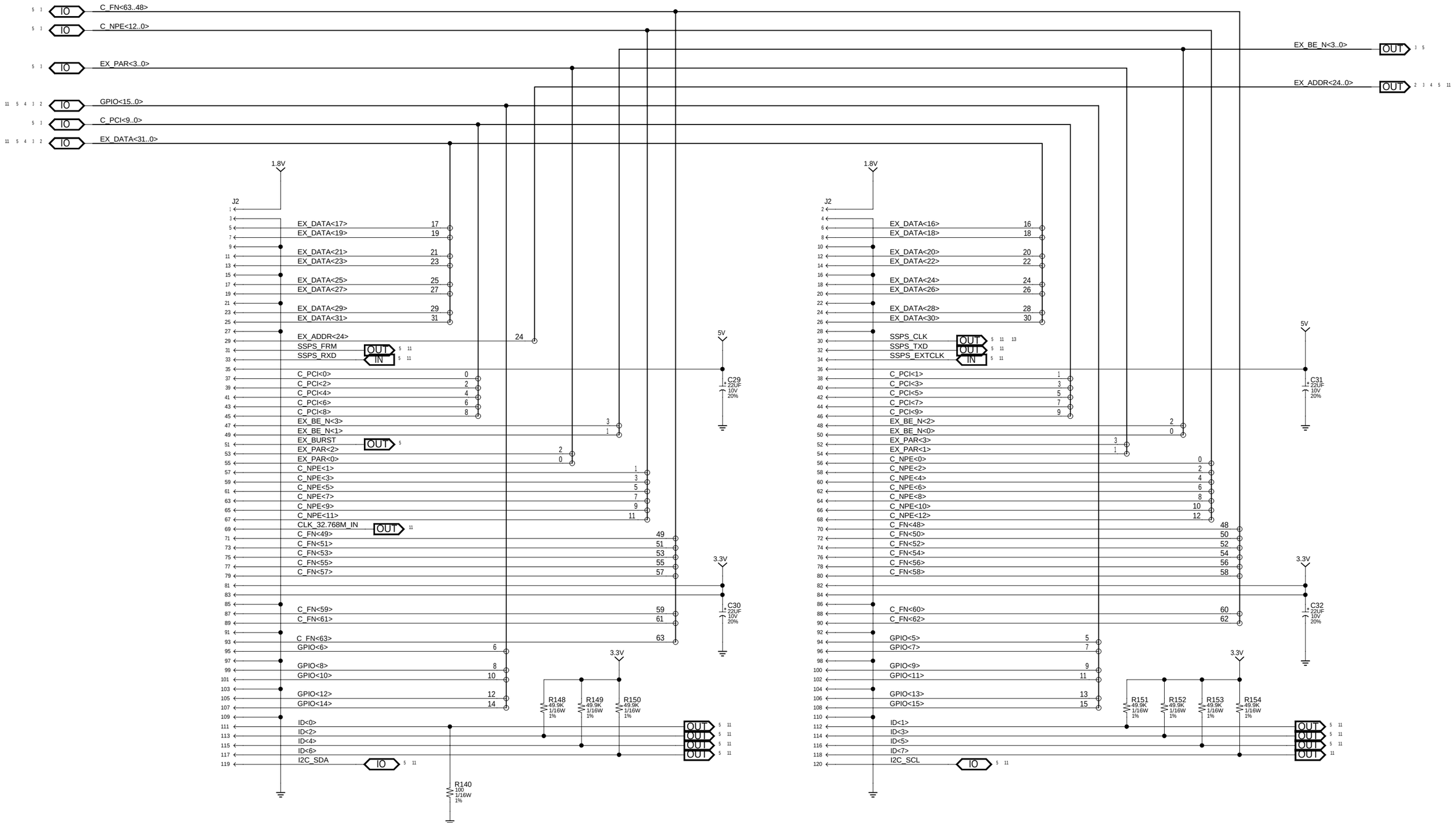
DRAWN_BY: R Sokolovskiy	LOCAL PAGE: 1 OF 13	TITLE: Analog 4X1 Module	
ENGINEER: R Sokolovskiy		DATE LAST MODIFIED: Thu Sep 23 15:29:00 2004	DWG.#: C73147 / REV: 02



BMP INTERFACE STANDARD CONNECTOR

INTEL
GETZVILLE, NY 14068

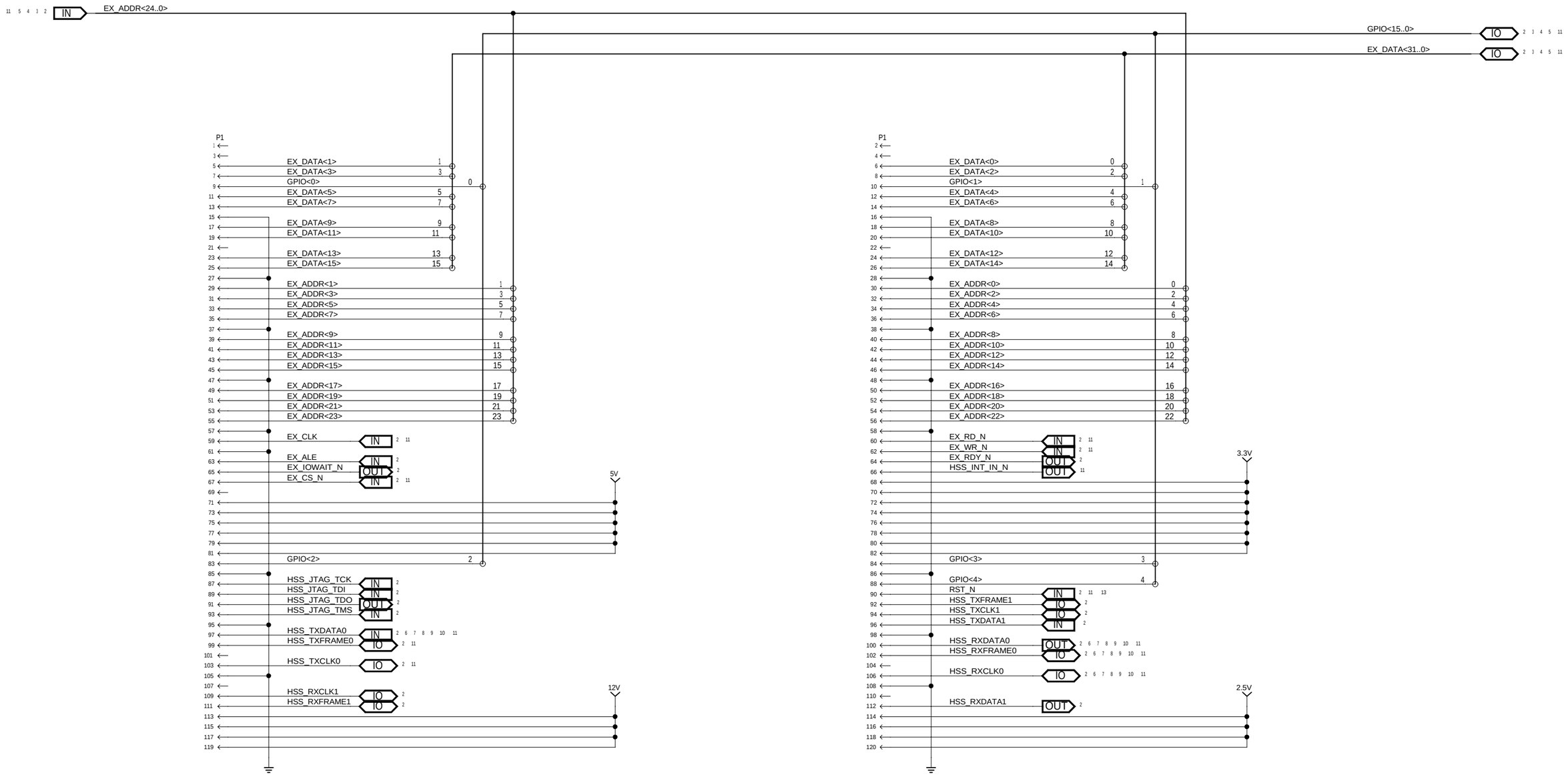
DRAWN_BY: R Sokolovskiy	LOCAL PAGE: 2 OF 13	TITLE: Analog 4X1 Module	
ENGINEER: R Sokolovskiy		DATE LAST MODIFIED: Mon Mar 14 17:04:06 2005	DWG.#: C73147 / REV: 02



BMP INTERFACE EXPANSION CONNECTOR

INTEL
GETZVILLE, NY 14068

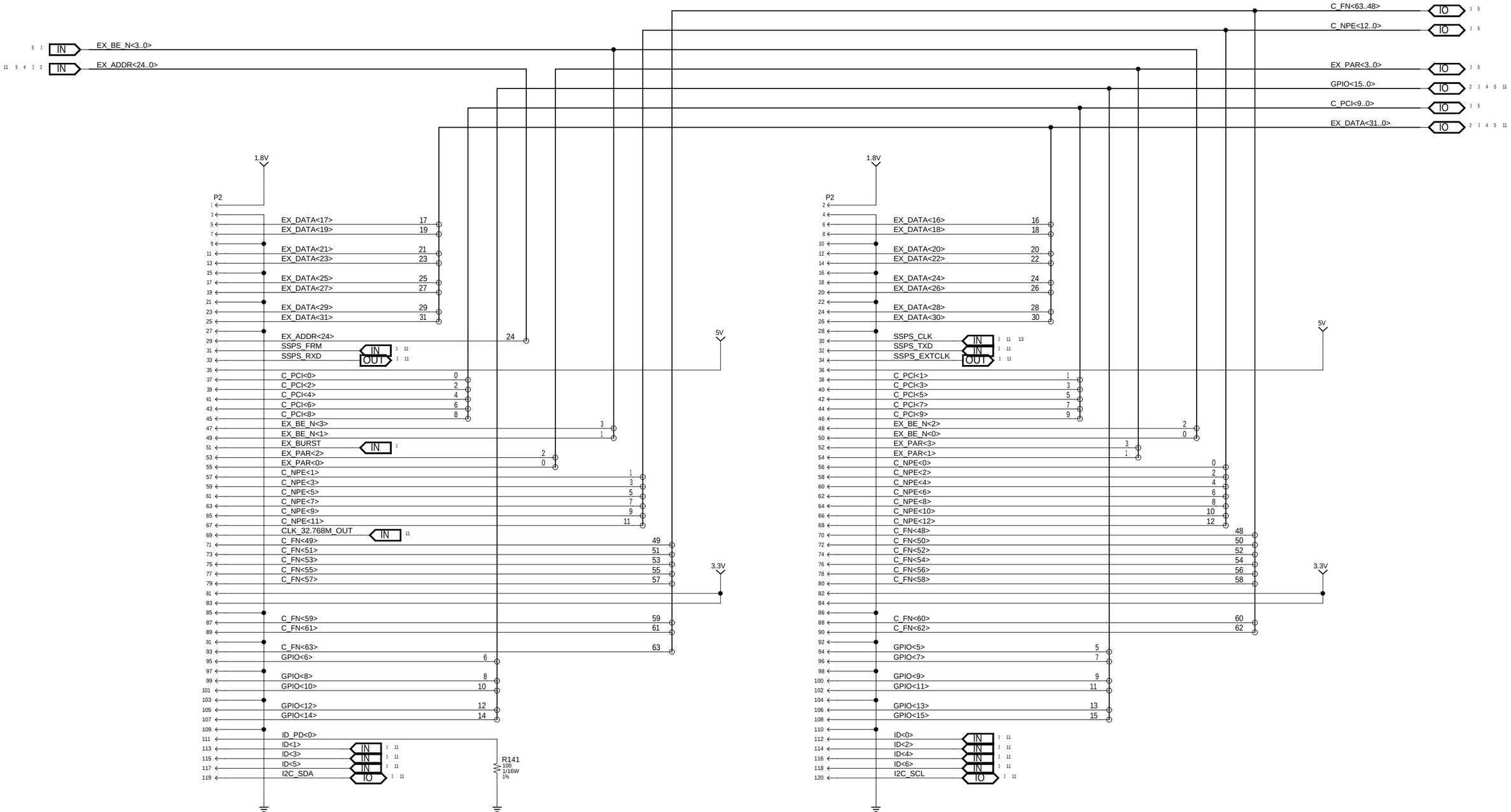
DRAWN_BY: R Sokolovskiy	LOCAL PAGE: 3 OF 13	TITLE: Analog 4X1 Module	
ENGINEER: R Sokolovskiy		DATE LAST MODIFIED: Mon Mar 14 17:04:07 2005	DWG.#: C73147 / REV: 02



STACKING INTERFACE STANDARD CONNECTOR

INTEL
GETZVILLE, NY 14068

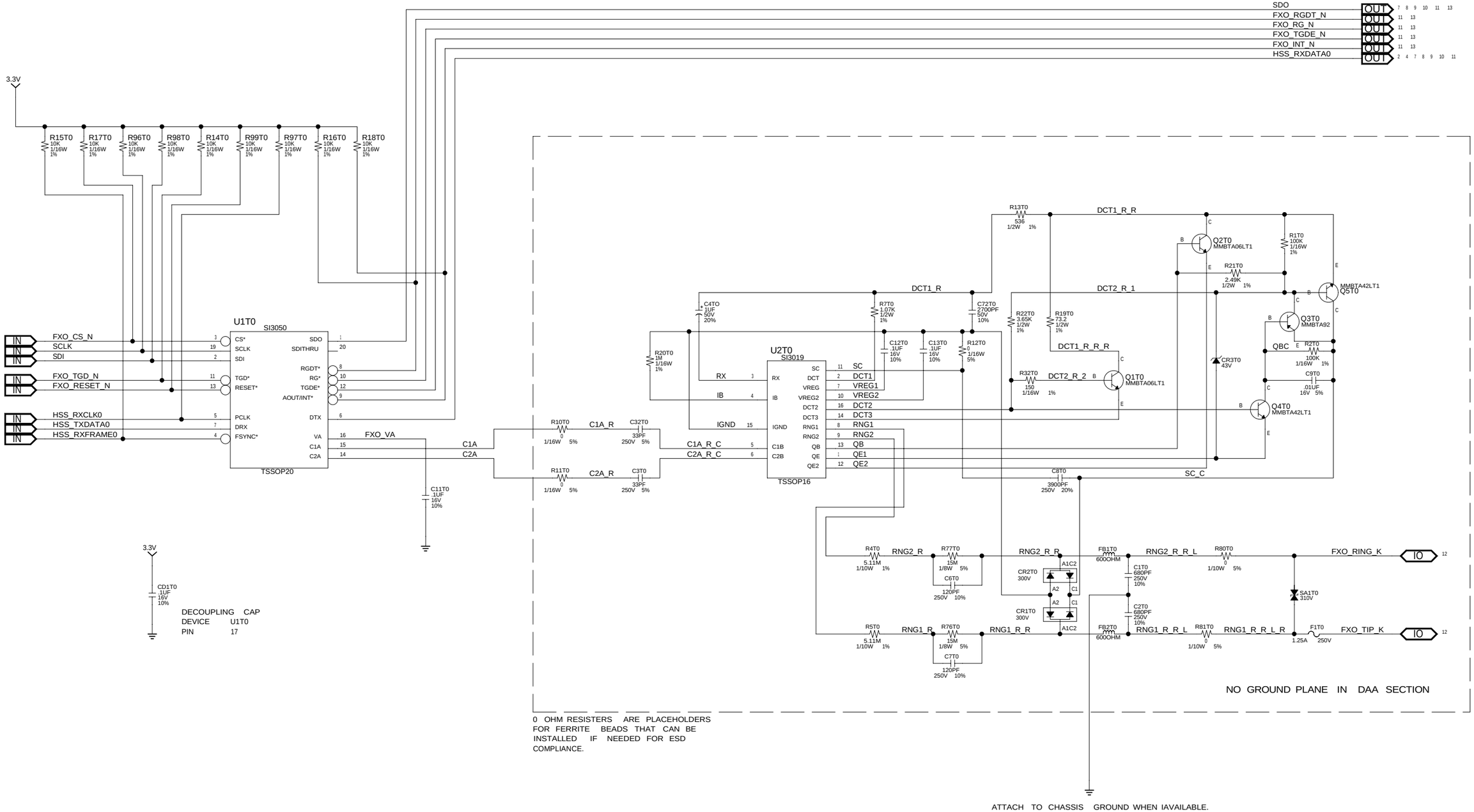
DRAWN_BY: R Sokolovskiy	LOCAL PAGE: 4 OF 13	TITLE: Analog 4X1 Module	
ENGINEER: R Sokolovskiy		DATE LAST MODIFIED: Mon Mar 14 17:04:08 2005	DWG.#: C73147 / REV: 02



STACKING INTERFACE EXPANSION CONNECTOR

INTEL
GETZVILLE, NY 14068

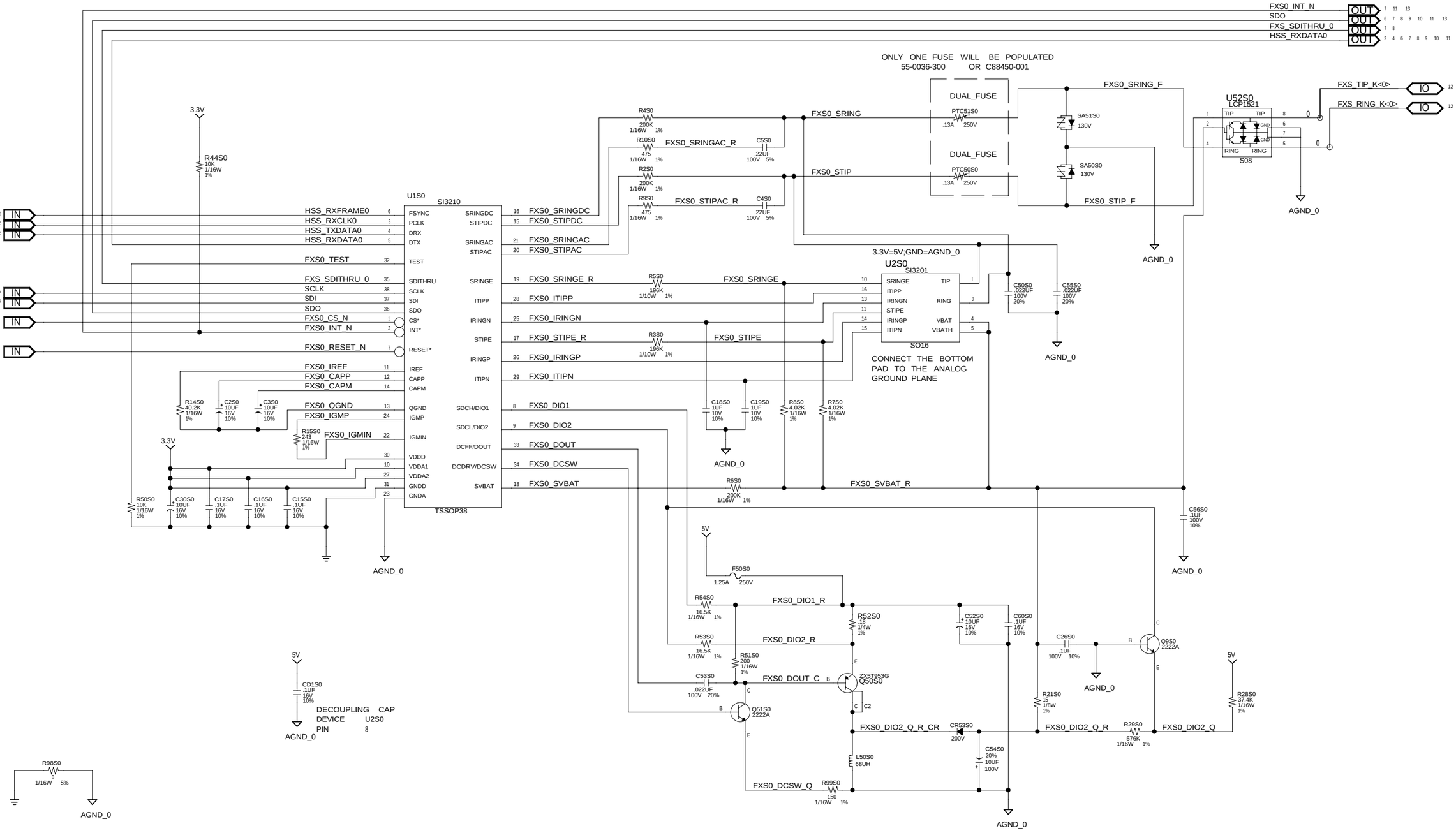
DRAWN_BY: R Sokolovskiy	LOCAL PAGE: 5 OF 13	TITLE: Analog 4X1 Module	
ENGINEER: R Sokolovskiy		DATE LAST MODIFIED: Mon Mar 14 17:04:08 2005	DWG.#: C73147 / REV: 02



FXO INTERFACE

INTEL
GETZVILLE, NY 14068

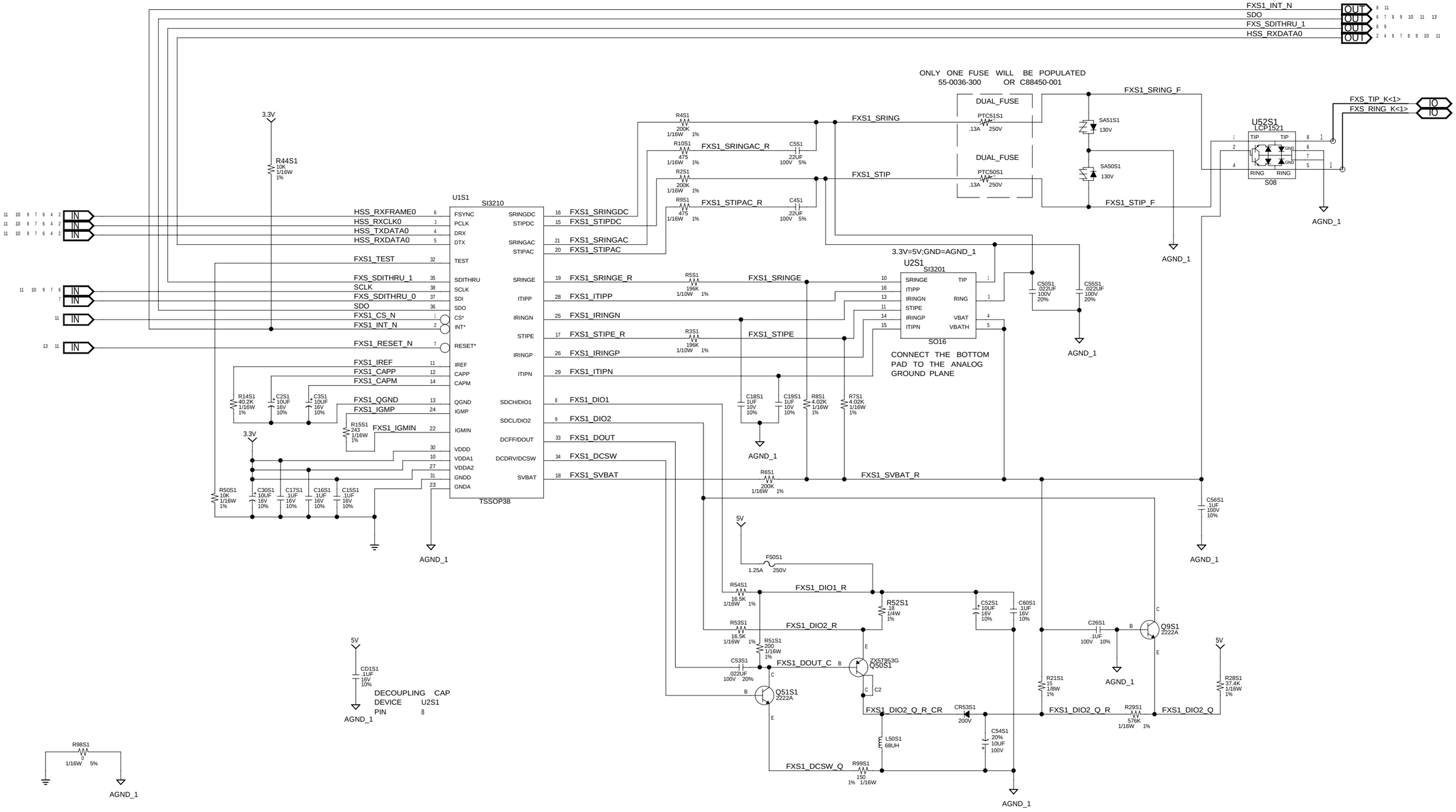
DRAWN_BY:	LOCAL PAGE:	TITLE:		
R Sokolovskiy	6 OF 13	Analog 4X1 Module		
ENGINEER:		DATE LAST MODIFIED:	DWG.#:	REV:
R Sokolovskiy		Mon Mar 14 17:04:09 2005	C73147	02



FXS-0 INTERFACE

INTEL
GETZVILLE, NY 14068

DRAWN_BY:	LOCAL PAGE:	TITLE:		
R Sokolovskiy	7 OF 13	Analog 4X1 Module		
ENGINEER:		DATE LAST MODIFIED:	DWG.#:	REV:
R Sokolovskiy		Mon Mar 14 17:04:10 2005	C73147	02



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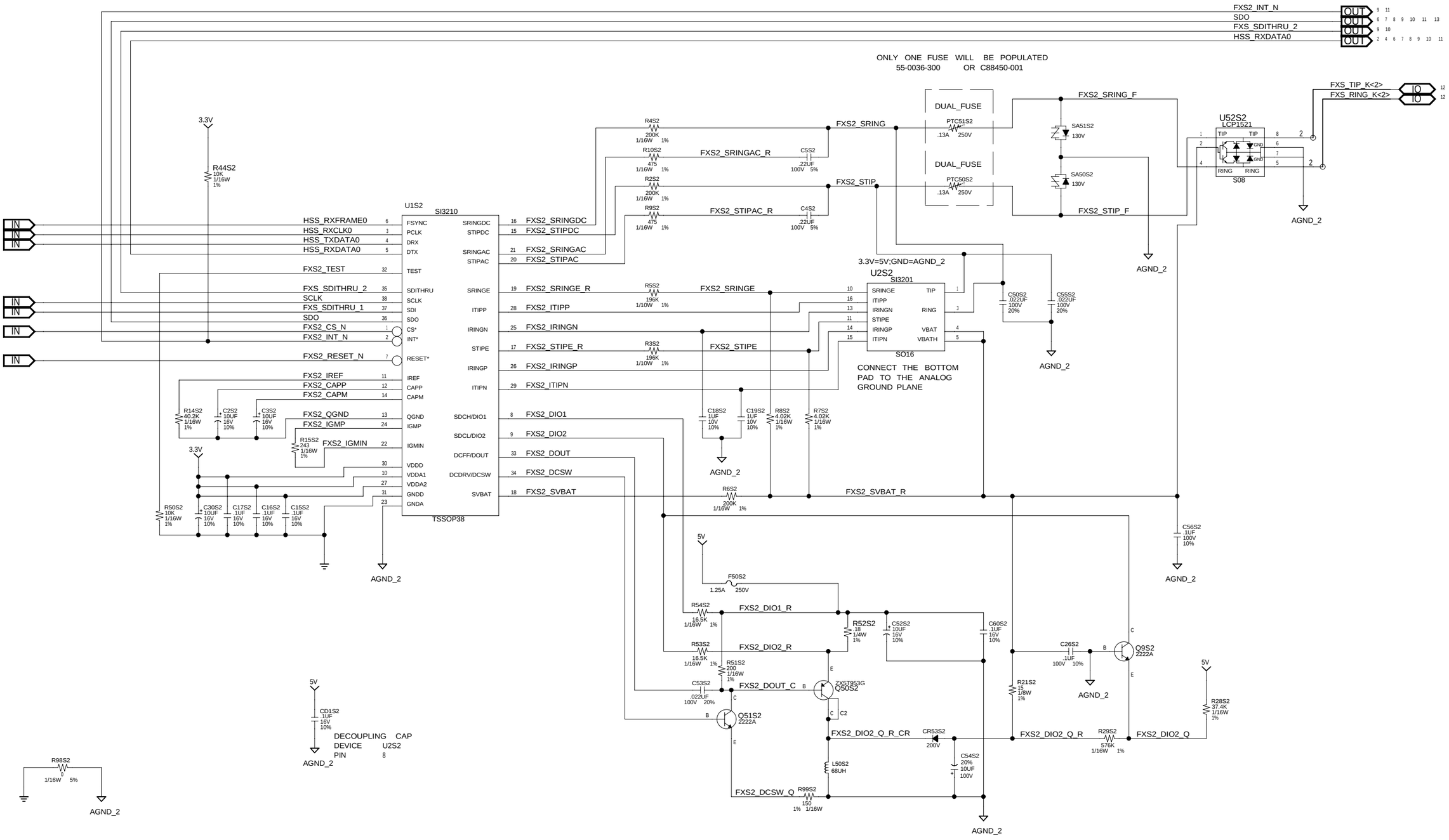

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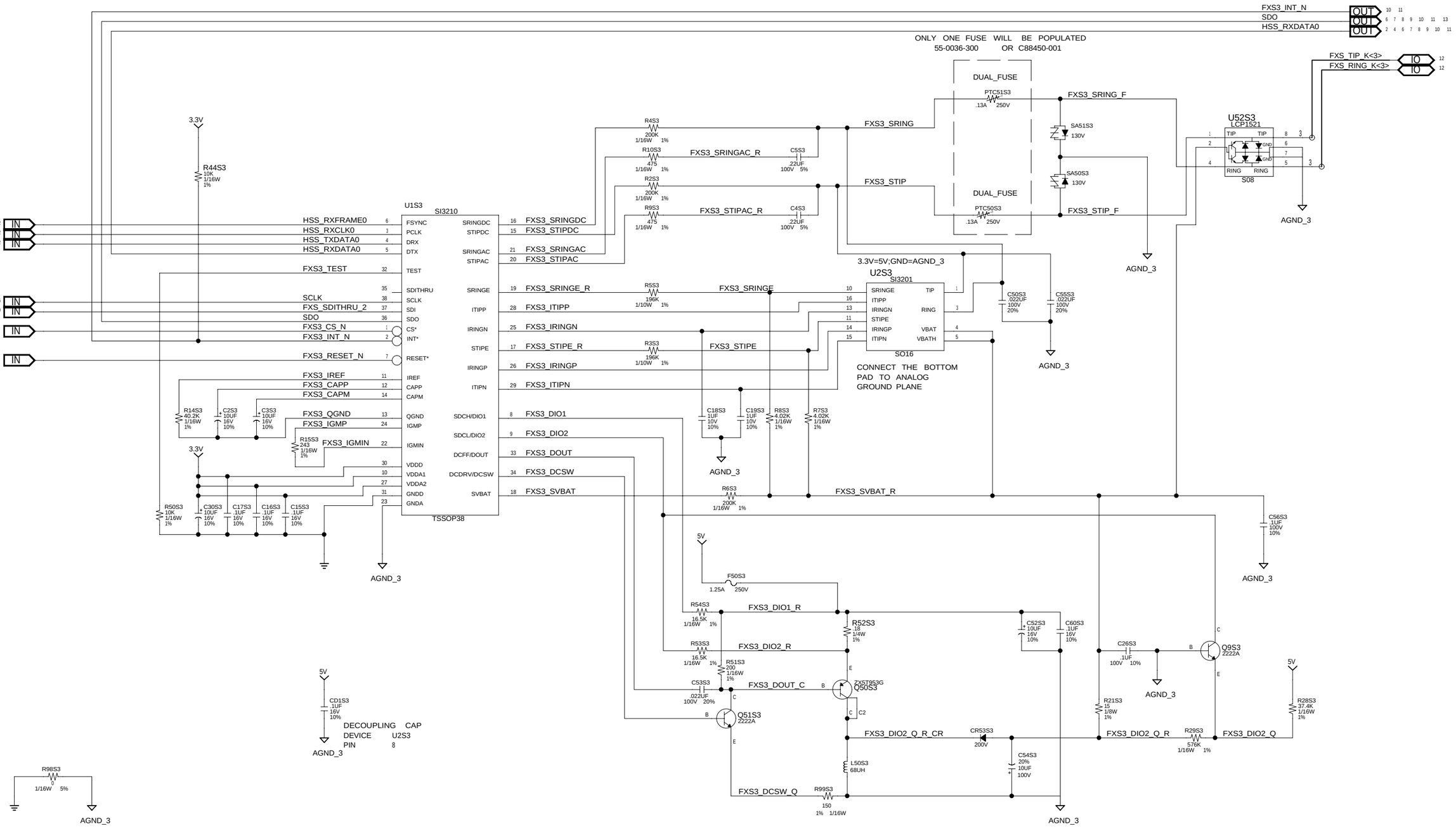

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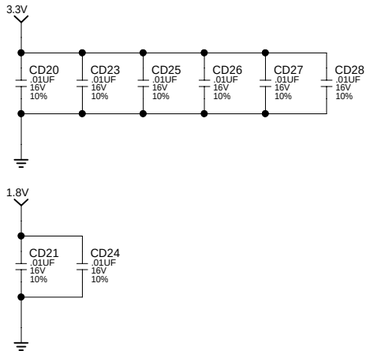
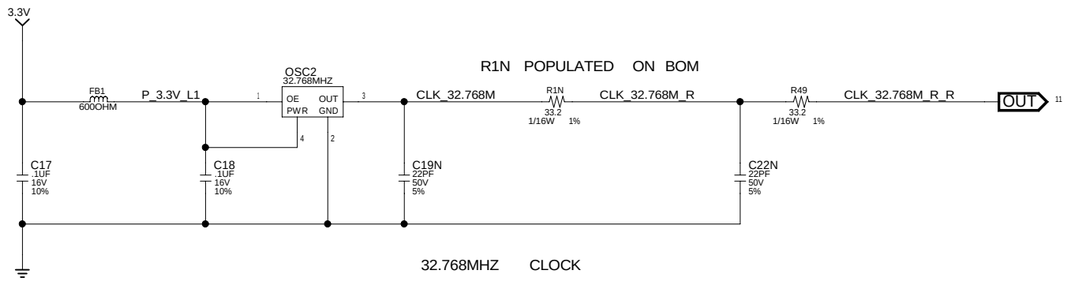
CAPACITOR	DEVICE	PIN
CD20	U2	5
CD23	U2	20
CD25	U2	38
CD26	U2	51
CD27	U2	88
CD28	U2	98
CD21	U2	26
CD24	U2	57

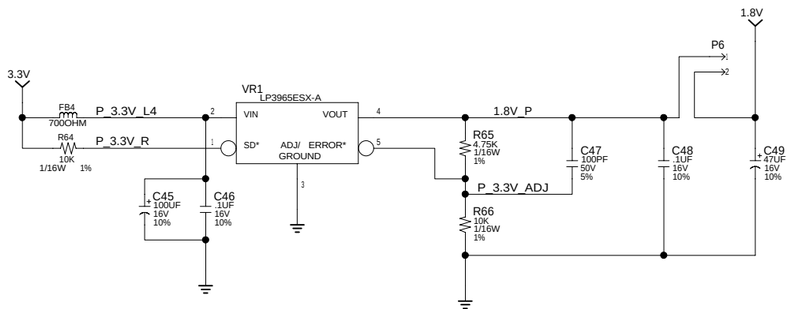


PLACE A 0.01UF CAP BY EACH POWER PIN.

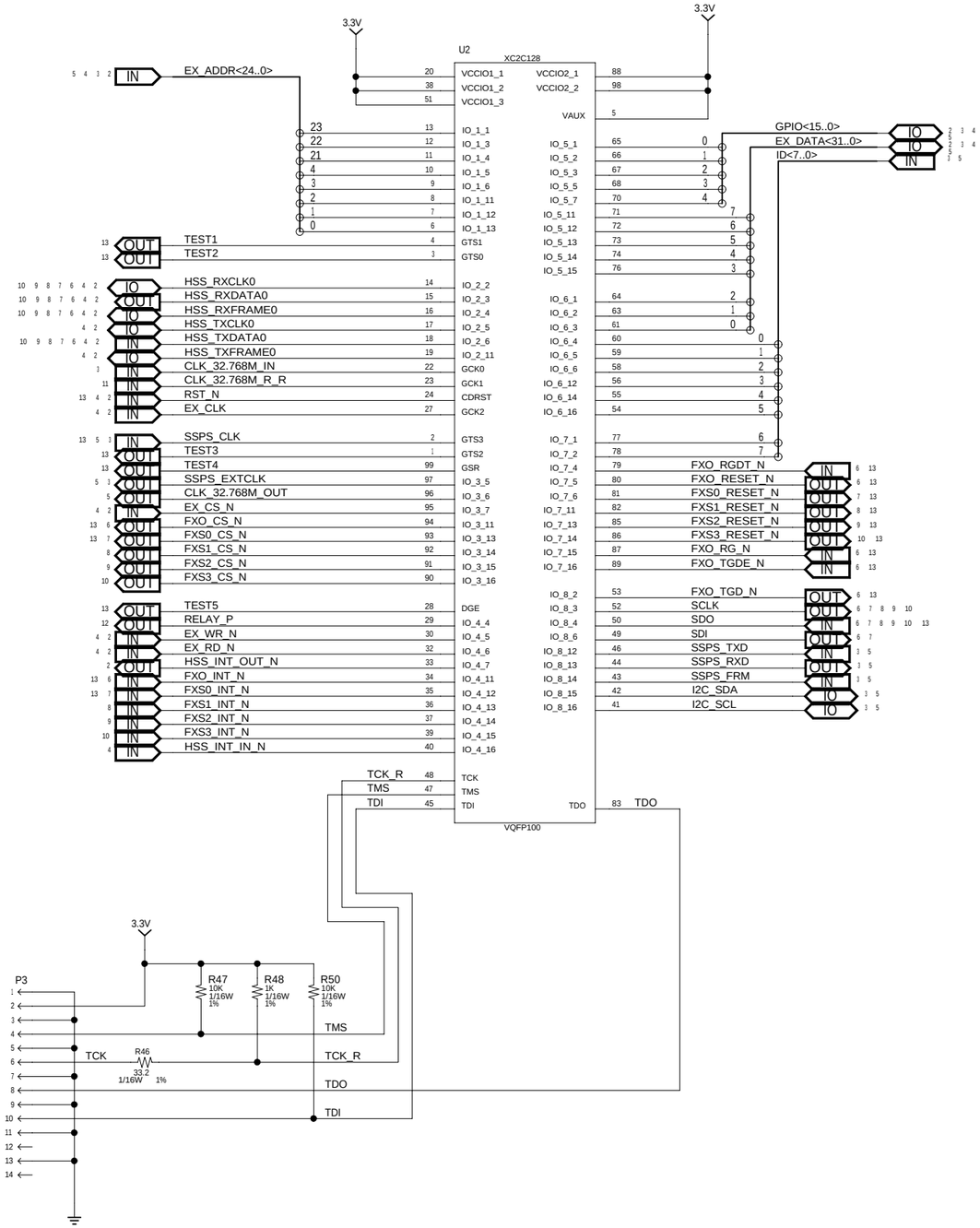
R1N POPULATED ON BOM



32.768MHZ CLOCK



1.8V REGULATOR FOR CPLD CORE



BOARD CONTROL CPLD

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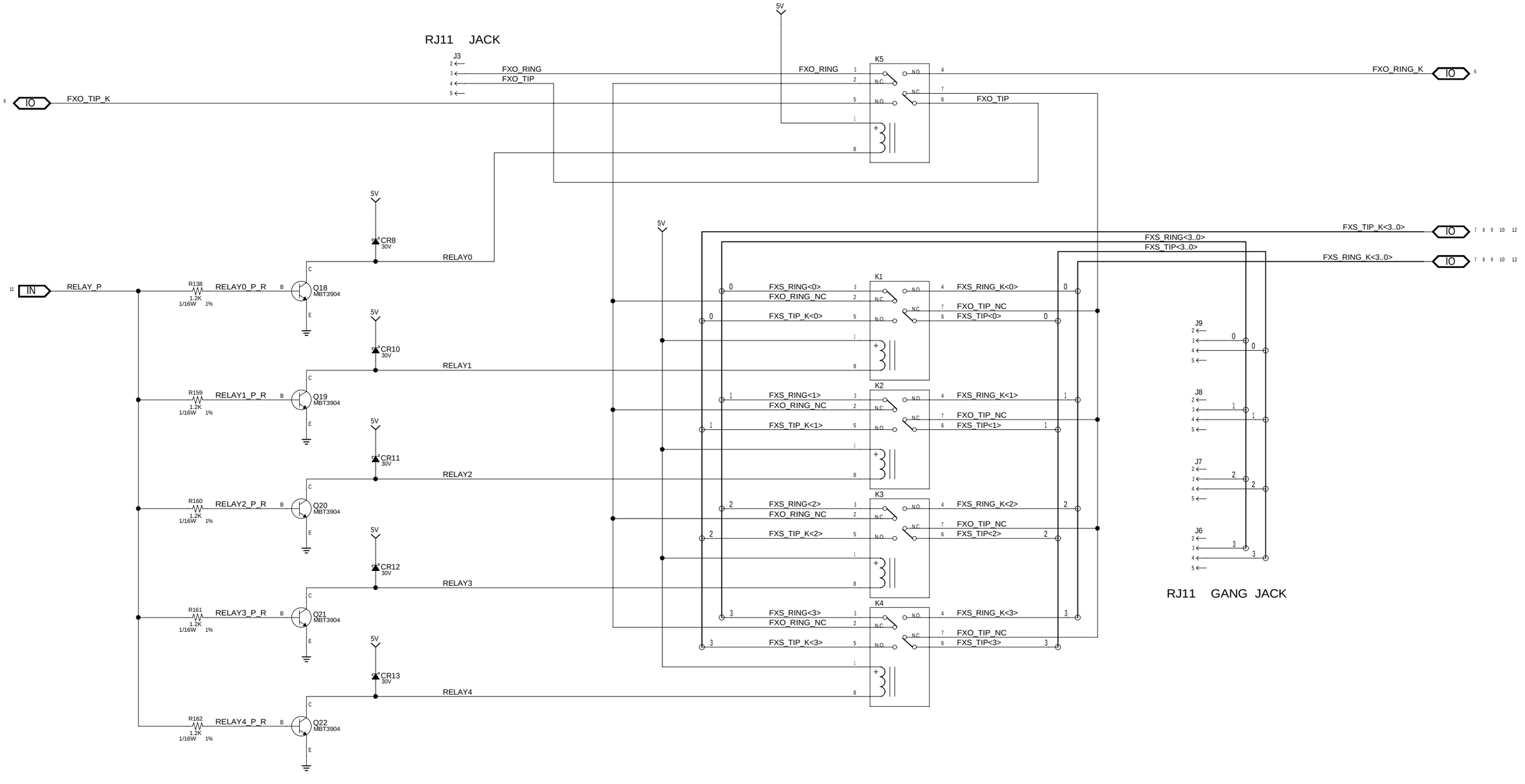
DRAWN_BY:	LOCAL PAGE:	TITLE:		
R Sokolovskiy	11 OF 13	Analog 4X1 Module		
ENGINEER:		DATE LAST MODIFIED:	DWG.#:	REV:
R Sokolovskiy		Mon Mar 14 17:04:13 2005	C73147	02

RJ11 JACK



RJ11 GANG JACK

POWER FAILOVER RELAYS

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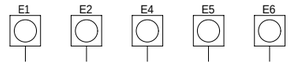
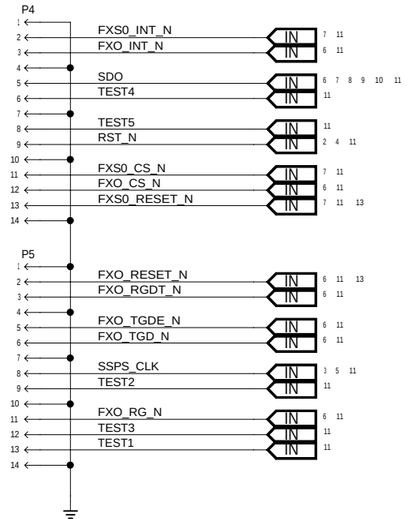
GETZVILLE, NY 14068

DRAWN_BY: R Sokolovskiy	LOCAL PAGE: 12 OF 13	TITLE: Analog 4X1 Module	
ENGINEER: R Sokolovskiy		DATE LAST MODIFIED: Mon Mar 14 17:04:13 2005	DWG.#: C73147 / REV: 02



MOUNTING HOLES

PORT LEDS



TEST POINTS

INTEL GETZVILLE, NY 14068		DRAWN_BY: R Sokolovskiy ENGINEER: R Sokolovskiy	LOCAL PAGE: 13 OF 13	TITLE: Analog 4X1 Module DATE LAST MODIFIED: Mon Mar 14 17:04:14 2005	DWG.#: C73147 REV: 02