intel® Technical Advisory

TA-0346-012

5200 NE Elam Young Parkway
Hillsboro, OR 97124

May, 20,2002

SKA4 BIOS 52.7 Release Notes

Products Affected

Product Type	Product Code
SKA4 Server Baseboard	BKO2HE
SRKA4 Server Platform	SKODVHI, SKODVBK, SKODVBS, ISP4400 SKODVBKHI
SPKA4 Server Platform	SKOC2HI, SKOC2BS, SKOC2BSxx

General Installation Instructions

1. Run *SKA4_BIOS_xx_x. EXE* to extract BIOS.EXE.

2. Put a blank diskette in A: and run *BIOS.EXE A:* to extract the BIOS files to a diskette. Label the diskette SKA4 BIOS version xx.x.

The recommended load order for updating BIOS is as follows:

1. Put in the SKA4 BIOS diskette and run *IFLASH* to update the BIOS.

2. Clear CMOS. This can be done either by entering BIOS setup during POST and pressing F9 to load defaults, or by simultaneously pressing the system reset button and power on button while the system is on and holding it for four or more seconds.

BIOS 52.7 Description

Intel is releasing **Production** BIOS 52.7 (Build 2070) for all SKA4 boards and systems.

BIOS 52.7 fixes an SMBIOS Table Issue (maximum) processor speeds not being reported t (See *Change Notes* below.)

BIOS 52.7 Change Notes

The following changes since BIOS 52.0 are incorporated into this release.

1. The maximum internal processor speed is not being reported correctly in previous versions of KOA BIOS. ISC 3.x reports the maximum processor speeds as 750 MHz in the platform instrumentation module. ISC retrieves the maximum speed from the SMBIOS tables. The SMBIOS tables have been fixed to reflect the 900MHz processor.

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2. The Utility used to roll BIOS 52.6 to production corrupted the recovery boot code causing the system to do a recovery boot instead of a flash update. The utility has been recompiled and re-licensed to prevent further issues

3. Microcode has not changed since BIOS 50.1

Processor	UpdateID	Date
00000671	00000014	08/11/1998
00000673	0000002E	09/10/1999
00000672	00000038	09/22/1999
000006A0	00000003	01/10/2000
000006A1	00000001	03/06/2000
000006A4	00000001	06/16/2000

BIOS 52.6 Description

Intel is releasing **Production** BIOS 52.6 (Build 2070) for all SKA4 boards and systems.

BIOS 52.6 fixes an SMBIOS Table Issue (maximum) processor speeds not being reported (See *Change Notes* below.)

BIOS 52.6 Change Notes

The following changes since BIOS 52.0 are incorporated into this release.

4. The maximum internal processor speed is not being reported correctly in previous versions of KOA BIOS. ISC 3.x reports the maximum processor speeds as 750 MHz in the platform instrumentation module. ISC retrieves the maximum speed from the SMBIOS tables. The SMBIOS tables have been fixed to reflect the 900MHz processor.

5. Microcode has not changed since BIOS 50.1

Processor	UpdateID	Date
00000671	00000014	08/11/1998
00000673	0000002E	09/10/1999
00000672	00000038	09/22/1999
000006A0	00000003	01/10/2000
000006A1	00000001	03/06/2000
000006A4	00000001	06/16/2000

BIOS 52.4 Description

Intel is releasing **Production** BIOS 52.4 (Build 2065) for all SKA4 boards and systems.

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BIOS 52.4 fixes some minor adapter inconsistencies, in setup, adds support for PCI-X adapters, and adds compatibility with hardware changes made in the SKA4 751519- 605 and later baseboard revisions. (See *Change Notes* below.)

BIOS 52.4 Change Notes

The following changes since BIOS 52.0 are incorporated into this release.

6. Addition of a decision tree to detect the presence of 66MHz if enabled. The decision tree was left out of BIOS 52.1 this is needed for the –605 and later SKA4 baseboards

7. Add support for PCI-X adapters and zero's out the upper 32 bits to force the adapters to operate in a 32bit mode.

8. A fix has been added which removes the Intel Logo screen if a Raid adapter is detected on the PCI bus. This fixes an inconsistency where certain Raid adapters cannot boot properly if the logo screen is enabled.

9. Microcode has not changed since BIOS 50.1

Processor	UpdateID	Date
00000671	00000014	08/11/1998
00000673	0000002E	09/10/1999
00000672	00000038	09/22/1999
000006A0	00000003	01/10/2000
000006A1	00000001	03/06/2000
000006A4	00000001	06/16/2000

BIOS 52.1 Description

Intel is releasing **Production** BIOS 52.1 (Build 2061) for all SKA4 boards and systems.

BIOS 52.1 fixes some minor language translation inconsistencies in setup, fixes a PCI bus performance issue, and adds compatibility with hardware changes made in the SKA4 751519-605 revision. (See *Change Notes* below.)

BIOS 52.1 Change Notes

The following changes since BIOS 52.0 are incorporated into this release.

10. Addition of translations in BIOS setup for French, German, Italian, Spanish, and Japanese. The translations were left out of BIOS 52.0

11. Internal BIOS changes have been made to support the hardware changes implemented in baseboard revision 751519-605 (*see TA-0414 for detailed information about these hardware changes.*)

    The BIOS setup option to change the speed of the PCI-A bus between 33 MHz and 66 MHz will not be displayed on –605 rev baseboards and the PCI-A bus speed will be set to 33 MHz. This setup option will remain visible if BIOS 52.1 is executed on baseboard revisions prior to –605. BIOS 52.1 are backward compatible with all production baseboards. BIOS releases prior to BIOS 52.1 are not compatible with the –605-rev baseboard.

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12. Under certain circumstances the PCI bus would limit data transfers to short burst duty cycles. This often occurred under high IO bandwidth consumption circumstances, and would adversely affect the performance throughput of the PCI bus. Chipset register modifications were made to prevent this short burst situation.

13. Microcode has not changed since BIOS 50.1

Processor	UpdateID	Date
00000671	00000014	08/11/1998
00000673	0000002E	09/10/1999
00000672	00000038	09/22/1999
000006A0	00000003	01/10/2000
000006A1	00000001	03/06/2000
000006A4	00000001	06/16/2000

BIOS 52.0 Description

Intel is releasing **production** BIOS 52.0 (Build 2058) for all SKA4 boards and systems.

BIOS 52.0 detects the presence of ISC 2.3 or ISC 2 .3 (See *Change Notes* below.)

BIOS 52.0 Change Notes

The following changes since BIOS 50.3 change is incorporated into this release.

1. BIOS 52.0 detect the presence of ISC 3.0 if it is enabled in the System Setup Utility. It is loaded and ISC 3.0 looks for a DHCP host. If ISC 3.0 is not enabled in SSU the BIOS loads ISC2.3

2. Microcode has not changed since BIOS 50.1

Processor	UpdateID	Date
00000671	00000014	08/11/1998
00000673	0000002E	09/10/1999
00000672	00000038	09/22/1999
000006A0	00000003	01/10/2000
000006A1	00000001	03/06/2000
000006A4	00000001	06/16/2000

BIOS 50.3 Description

Intel is releasing **production** BIOS 50.3 for SKA4 boards and systems.

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BIOS 50.3 adds back in a BIOS setup feature for a " Memory Gap" option that was inadvertently dropped from bios setup in BIOS 50.2. The Memory Gap option was originally implemented in BIOS 50.0 (See item 12 in the *BIOS 50.0 Change Notes* below.)

BIOS 50.3 Change Notes

The following changes since BIOS 50.3 change is incorporated into this release.

1. The "Memory Gap" - option when enabled in setup creates a gap at the 4gb space .The gap protects memory allocated to the PCI space, and allows Microsoft Windows NT 4.0 drivers to operate properly.

2. Microcode has not changed since BIOS 50.1

Processor	UpdateID	Date
00000671	00000014	08/11/1998
00000673	0000002E	09/10/1999
00000672	00000038	09/22/1999
000006A0	00000003	01/10/2000
000006A1	00000001	03/06/2000
000006A4	00000001	06/16/2000

BIOS 50.2 Description

Intel is releasing **production** BIOS 50.2 for SKA4 boards and systems.

SKA4 BIOS 50.2 adds a feature that allows users to select the bus speed for the two 64 bit slot on PCI segment A (PCI-A). PCI-A bus speed defaults to 33 MHz, but can be set to 66 MHz through the BIOS setup screen. Please see TA-0341-x for further information regarding running PCI-A at 66 MHz.

This release corrects a system boot problem that would cause the system to halt the boot process with a 1-3-3-1beep code (post code 28, no system memory found). When this problem would occur, BIOS would be locked into a condition that would prevent it from seeing any valid system memory. In order to clear this error the CMOS battery would have to be removed, or additional banks of memory would have to be installed in the system.

Intel Pentium® III Xeon™ 900 MHz processor support is included in this release.

BIOS 50.2 Change Notes

The following changes since BIOS 50.1 are incorporated into this release.

1. An option has been added to BIOS setup to allow selection of the PCI-A segment bus speed. Default operation is 33 MHz; 66 MHz operation is optional. The option is on the BIOS setup screen:

   `Advanced → PCI Configuration → Hot Plug PCI Control → PCI slots A1/A2 bus speed`

   Corrected BIOS logical operation during memory sizing to correct a condition that would cause BIOS to not recognize

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any valid system memory. When this condition would occur, the system would halt during the boot process and issue a beep code 1-3-3-1.

2. Intel Pentium® III Xeon™ 900 MHz and Pentium® III Xeon™ 700 MHz B0 processor support is included in this release.

3. Updated Phoenix POST banner to "2001".

4. The recovery BIOS is unchanged since BIOS 50.1

5. Microcode has been updated from BIOS 50.1

Processor	UpdateID	Date
00000671	00000014	08/11/1998
00000673	0000002E	09/10/1999
00000672	00000038	09/22/1999
000006A0	00000003	01/10/2000
000006A1	00000001	03/06/2000
000006A4	00000001	06/16/2000

BIOS 50.1 Description

Intel is releasing **production** BIOS 50.1 for SKA4 boards and systems.

This release will automatically configure the SKA4 baseboard's two 66 MHz capable PCI slots to run at 33 MHz. Implementing this BIOS will ensure the two 66 MHz slots operate at 33 MHz even if populated with 66 MHz capable adapters.

Please see TA-0341-X for further details.

This release supports the changes related to server management and the implementation of ISC 3.0 (Intel Server Control). These changes are not compatible with ISC 2.3. If ISC 2.3 is used, and no upgrade to ISC 3.0 is planned, do not install this BIOS. **If you install this BIOS, ISC 2.3 will not function properly**.

In addition, this BIOS must be installed with corresponding versions of BMC and FRUSDR. These components must be installed as a set. Failure to do so will result in numerous system error messages and erratic operation of the server. The release of system firmware is as follows:

- BIOS 50 or later.
- BMC 1.13 or later.
- FRUSDR 4.3.6 or later.

All required system BIOS and firmware can be found in the SKA4 System Firmware Set. Downloading this file may be an easier method to update the system firmware. To extract the files first unzip the download file to a directory then perform the following steps:

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BIOS 50.1 Change Notes

The following changes since BIOS 50 are incorporated into this release.

1. BIOS will automatically configure the two 66 MHz PCI slots to run at 33 MHz.

2. The recovery BIOS is unchanged since BIOS 50.

3. Microcode Updates: No change from BIOS 50.

Processor	UpdateID	Date
00000671	00000014	08/11/1998
00000673	0000002E	09/10/1999
00000672	00000038	09/22/1999
000006A0	00000003	01/10/2000
000006A1	00000001	03/06/2000

BIOS 50.0 Description

Intel is releasing **production** BIOS 50 for SKA4 boards and systems.

This release incorporates many changes related to server management and the implementation of ISC 3.0 (Intel Server Control). These changes are not compatible with ISC 2.3. If ISC 2.3 is used, and no upgrade to ISC 3.0 is planned, do not install this BIOS. **If you install this BIOS, ISC 2.3 will not function properly**.

In addition, this BIOS must be installed with corresponding versions of BMC and FRUSDR. These components must be installed as a set. Failure to do so will result in numerous system error messages and erratic operation of the server. The release of system firmware is as follows:

- BIOS 50 or later.
- BMC 1.13 or later.
- FRUSDR 4.3.6 or later.

BIOS 50.0 Release Notes

The following changes since BIOS 42 are incorporated into this release.

1. Recovery BIOS has been changed to disable Bootblock POST codes to the on board LEDs (LEDs have been depopulated from the board).

2. Corrected a system hang situation during system boot if a system was configured with more than one add-in NIC and the system was configured to run DPC.

3. SC 3.0 (Intel Server Control) functionality has been incorporated into BIOS 50.

4. The default partition type for the service partition has changed in BIOS to 18 (12 H). This change requires a new ROM DOS kernel to be installed for the service partition. This ROM DOS kernel must be loaded from the system resource CD containing ISC 3.0 (currently in beta release). Please refer to the ISC 3.0 documentation for more information.

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5. Booting to the service partition locally and remotely is now possible.

6. The PEP (Platform Event Paging), PEF (Platform Event Filtering), and EMP (Emergency Management Port) setup options are no longer in the BIOS setup screens. These options are now in SSU and have to be configured with SSU from ISC 3.0.

7. LAN console redirection. The BIOS console can be redirected through the LAN port to another machine running ISC 3.0 software. The LAN console will use IP address information (static or DHCP) as defined in SSU. The BIOS will try to lease an IP address every time the system is booted; therefore, the LAN messages will be displayed on screen every boot.

8. Both the LAN console and serial console setup nodes can be enabled at the same time in setup; however, only one of the consoles can be active and in use at any time. If LAN console is enabled, BIOS will attempt to detect the presence of LAN connection, and if present, connect the console via the LAN connection.

9. Both LAN console and serial console work with BIOS in Diag screen mode only; the splash screen should be disabled for these purposes.

10. Fixed a problem where the option to boot from PXE device was missing from the boot menu. This occurred as a result of using DPC.

11. Fixed a memory allocation conflict with PHP controllers and add-in adapters that are similar to the AMI493 SCSI card and utilize the Intel i960RN bridge chip. This resolves reported problems of the system not being able to see the disk drives.

12. Improved compatibility between certain NT4.0 drivers and Microsoft Windows NT4.0 when installed on a system with 4GB of system memory. Some NT4.0 drivers do not query BIOS or the OS for memory size, but instead determine the memory size based on other methods. Some of these drivers do not determine the correct memory size when the top of physical memory aligns with the bottom of PCI space. A BIOS option has been added to enable a "memory gap" which inserts a gap between the top of physical memory and the bottom of PCI space. Enabling the memory gap may improve the compatibility of certain NT4.0 drivers on 4GB systems.

13. Corrected a problem displaying Japanese text in BIOS setup.

14. Previously when password on boot was enabled, the password prompt would not appear after the LAN console screen and the system would appear hung with a blank screen while it was waiting for a password to be entered. This has been corrected and the password on boot feature works correctly locally and remotely.

15. Previously, if the logo screen was enabled in BIOS setup, requesting console redirection would cause the BIOS to always default to diag screen even after console redirection was turned off. With BIOS 46 if the logo screen is enabled in setup the BIOS will use diag mode during console redirection over LAN/serial with DPC or CSSU, and during a service partition boot. On completion of these operations, the BIOS will restore the screen to the state requested in BIOS setup.

16. The recovery BIOS is unchanged since BIOS 27.

17. Microcode updates.

Processor	UpdateID	Date

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00000672	00000038	09/22/1999
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000006A1	00000001	03/06/2000

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